TIMA Laboratory

2023

Annual report

Foreword

TIMA Laboratory is a joint research laboratory between the Centre National de la Recherche Scientifique (CNRS), the Grenoble Institute of Technology (Grenoble INP) and the Université Grenoble Alpes (UGA).

TIMA addresses some of the most urgent and ambitious challenges related to the design of integrated circuits and Systems-on-chip (SoC). The research activities cover the specification, design, verification, test, CAD tools and design methods for integrated systems, including analog and digital components, smart sensors and actuators, up to multiprocessor SoCs together with their operating system. More in particular, researchers at TIMA cover the following topics:

- Low power design
- Asynchronous design
- New sampling and data processing techniques
- MEMS, Smart Sensors and Actuators
- Design of AMS/RF/mmW devices, circuits and systems
- Modeling, control and calibration of AMS/RF devices, circuits and systems
- Robustness, reliability and test
- Hardware security and embedded trust
- New hardware computing and digital design
- Hardware/Software co-design
- Simulation and verification
- Embedded AI

The laboratory is structured in the following four research teams:

Architectures and Methods for Resilient Systems (AMfoRS): Robustness and dependability evaluations of embedded systems; Hardened and robust architecture; Design for reliability with respect to variability, aging, and soft errors; Modeling, analysis and testing at the system level; Hardware security and embedded trust; New computational approaches and technologies

Circuits, Devices and System Integration (CDSI): Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

Reliable RF and Mixed-signal Systems (RMS): Design for test of analog, mixed-signal and RF circuits; Estimation of test metrics; Calibration of RF devices; Embedded control for efficient energy management; Prediction and control of quality and energy management; High-level modeling of heterogeneous and multi-physic systems

System Level Synthesis (SLS): Highly efficient architectures for general purpose computing or AI-dedicated algorithms; system-level modeling and design methodology (specification, simulation and verification of hardware/software systems on chip); design exploration and synthesis of hardware

TIMA takes an active part in the organization of the Grenoble Alpes research community, being linked to the poles "Mathematics, Informatics and Communication" (MSTIC) and "Physics, Engineering and Materials" (PEM). TIMA is also a member of the Carnot Institute LSI, the Laboratory of Excellence Persyval and the local federation of micro and nanoelectronics laboratories FMNT.

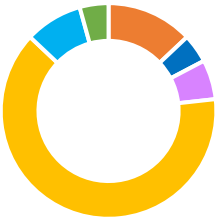
The 2023 edition of the TIMA annual report presents a brief and synthetic presentation of the scientific achievements of each research team.

Giorgio DI NATALE
Director

Summary

TIMA at a glance

Workforce 2023



185 members

- **24** Professors & associate professors
- **8** Researchers & emeritus
- **11** Permanent ITA
- **118** Students (69 PhD students + 49 interns)
- **16** Post-docs – Engineers – Experts – Teaching Assistants (ATER)
- **8** Visitors

Scientific production 2023

33	59	5	3	9
Journal articles	Conference papers and posters	Books and book chapters	Patents	Defended theses and HDR

Resources 2023 **> 9 024 k€**

Institutions support > 1 050 K€

Contractual resources > 7 974 K€

1 120 k€ Europe	**2 084 k€** PEPR	**1 242 k €** ANR
1 229 k€ State	**103 k€** Région	**697 k€** Parent institutions
876 k€ CIFRE	**416 k€** Industry	**202 k€** SATT

25 represented nationalities

Focus research and innovation

List of our active projects and contracts in 2023

Project	Funding framework	Principal investigator	Managing institution
NEUROPULS	EUROPE	**Ioana VATAJELU**	CNRS
SHIFT EU	EUROPE	**Philippe FERRARI**	UGA
SWAN-on-chip	EUROPE	**Florence PODEVIN**	Grenoble INP
Resilient Trust	EUROPE	**Giorgio DI NATALE**	Grenoble INP
ARCHI-CESAM	ANR (PEPR)	**Arthur PERAIS**	Grenoble INP
ARSENE	ANR (PEPR)	**Paolo MAISTRI**	UGA
HOLIGRAIL	ANR (PEPR)	**Frédéric PÉTROT**	Grenoble INP
NF-SYSTERA	ANR (PEPR)	**Sylvain BOURDEL**	Grenoble INP
NF-YACARI	ANR (PEPR)	**Philippe FERRARI**	Grenoble INP
SPINCOM	ANR (PEPR)	**Florence PODEVIN**	Grenoble INP
BAC4NOSE	ANR	**Ioana VATAJELU**	Grenoble INP
EMINENT	ANR	**Ioana VATAJELU**	Grenoble INP
IMHOTEP	ANR	**Florence PODEVIN**	Grenoble INP
MAPLURINUM	ANR	**Olivier MULLER**	Grenoble INP
MITIX	ANR	**Paolo MAISTRI**	CNRS
PiezoKnee	ANR	**Skandar BASROUR**	UGA
POP	ANR	**Giorgio DI NATALE**	Grenoble INP
PRECISE	ANR	**Jean-Daniel ARNOULD**	Grenoble INP
RAKES	ANR	**Frédéric PÉTROT**	Grenoble INP
SMART IMAGER	ANR	**Laurent FESQUET**	Grenoble INP
EAUDI	DGA (State)	**Skandar BASROUR**	UGA
MucoPiezoRheo	BPI (State)	**Skandar BASROUR**	UGA
SHIFT BPI	BPI (State)	**Philippe FERRARI**	UGA
MAMBO	DGAC (State)	**Libor RUFER**	UGA
FAIR	AURA (Région)	**Skandar BASROUR**	Grenoble INP
MULTIRAD	AURA (Région)	**Rodrigo POSSAMAI BASTOS**	UGA
80 PRIME 2022	CNRS	**Ioana VATAJELU**	CNRS

Project	Funding framework	Principal investigator	Managing institution
CAFET	UGA	**Mounir BENABDENBI**	UGA
CLAM	UGA	**Paolo MAISTRI**	UGA
IRGA SETH	UGA	**Martial DEFOORT**	UGA
MASHWave	UGA	**Manuel BARRAGAN**	UGA
MIAI Digital Hardware AI Architectures	UGA	**Frédéric PÉTROT**	UGA
NPATH-LOW-POWER	UGA	**Florence PODEVIN**	UGA
Thèse APACHE	UGA	**Katell MORIN-ALLORY**	UGA
Thèse SARTORI	UGA	**Rodrigo POSSAMAI BASTOS**	UGA
SYNCONNECT	UGA	**Ioana VATAJELU**	UGA
Thèse Nathan BAIN	STMicroelectronics (CIFRE)	**Frédéric PÉTROT**	INPG Entreprise SA
Thèse Oumayma BELKHADRA	NXP (CIFRE)	**Sylvain BOURDEL**	INPG Entreprise SA
Thèse Jérémy BELOT	HAWAI.TECH (CIFRE)	**Laurent FESQUET**	INPG Entreprise SA
Thèse Khalil BOUCHOUCHA	STMicroelectronics (CIFRE)	**Sylvain BOURDEL**	FLORALIS
Thèse Giovanni BRITTON	STMicroelectronics (CIFRE)	**Salvador MIR**	CNRS
Thèse Florent CROZET	STMicroelectronics (CIFRE)	**Stéphane MANCINI**	INPG Entreprise SA
Thèse Tiziano FIORUCCI	STMicroelectronics (CIFRE)	**Giorgio DI NATALE**	FLORALIS
Thèse Adrien GODARD	STMicroelectronics (CIFRE)	**Laurent FESQUET**	FLORALIS
Thèse Diana KALEL	STMicroelectronics (CIFRE)	**Katell MORIN-ALLORY**	FLORALIS
Thèse Antoine LINARES	SiFive (CIFRE)	**Giorgio DI NATALE**	INPG Entreprise SA
Thèse Pierre MALBEC	STMicroelectronics (CIFRE)	**Jean-Daniel ARNOULD**	FLORALIS
Thèse Valentin MARTINOLI	Thalès (CIFRE)	**Régis LEVEUGLE**	FLORALIS
Thèse Cristiano MERIO	STMicroelectronics (CIFRE)	**Laurent FESQUET**	FLORALIS
Thèse Luc NOIZETTE	Nuclétudes (CIFRE)	**Régis LEVEUGLE**	Grenoble INP
Thèse Pierre RAVENEL	Kalray (CIFRE)	**Frédéric PÉTROT**	FLORALIS
Thèse Emilien TALY	STMicroelectronics (CIFRE)	**Ioana VATAJELU**	FLORALIS
Thèse Damiano ZUCCALA	STMicroelectronics (CIFRE)	**Katell MORIN-ALLORY**	FLORALIS
CIMITRANS	BPI (Industry)	**Sylvain BOURDEL**	Grenoble INP
EMIR	SATT	**Laurent FESQUET**	Grenoble INP

TIMA's staff

Giorgio DI NATALE
Director

Laurent FESQUET
Deputy Director

Florence PODEVIN
Deputy Director
(since 09/06/2023)

Administrative and Financial pole

Viviana GIORDANO
Manager - Human resources - Special events – Communication

Laurence BEN TITO
Executive & laboratory assistant - Publications

Murielle RUSTAT (since 28/08/2023)
Budgets, contracts

Aurore GAYRAUD
Teams finance administrator

Youness RAJAB
Teams finance administrator - Common expenses administrator
Budgets, contracts

Computer Service

Frédéric CHEVROT
Manager - Systems, networks and park manager

Ahmed KHALID
Computer park manager

Development Service

Adrien PROST-BOUCLE
Manager

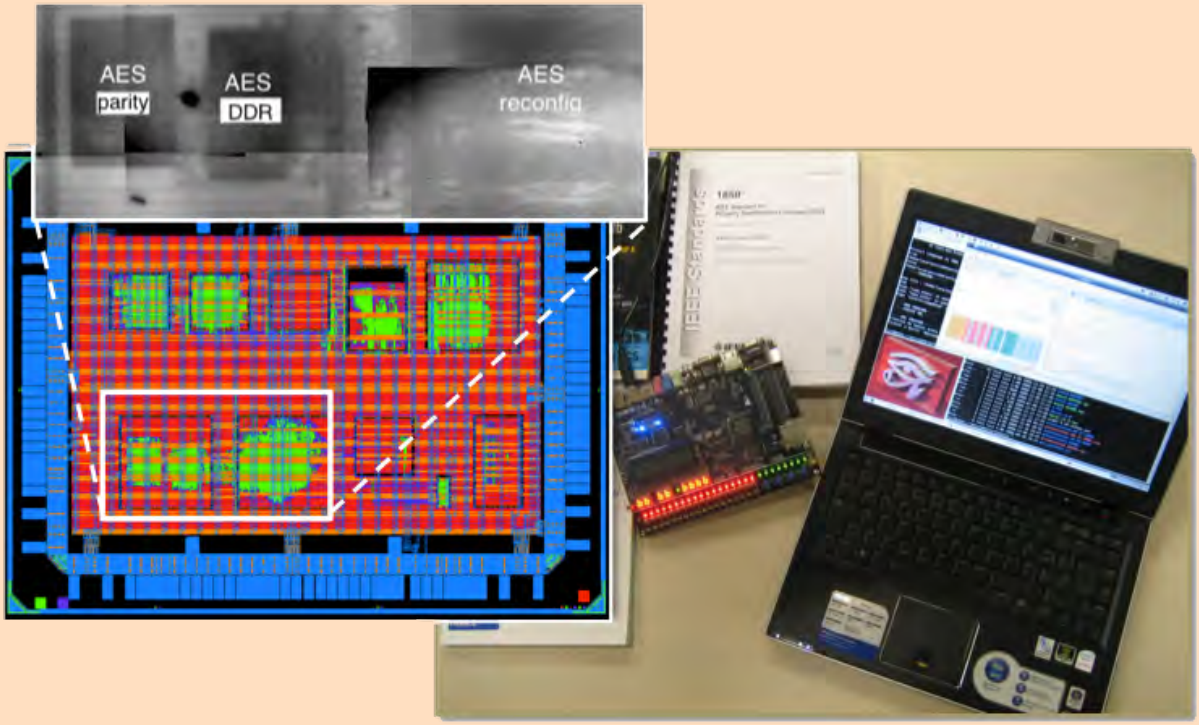
Alice DE BIGNICOURT
Development engineer, webmaster

Mamadou DIALLO
Development engineer

Christelle RABACHE
Development engineer

TIMA
CNRS — GRENOBLE INP — UGA

AMfoRS team



Architectures and Methods for Resilient Systems

Architectures and Methods for Resilient Systems (AMfoRS team)

http://tima.univ-grenoble-alpes.fr/tima/fr/amfors/amforsoverview.html

The **AMfoRS** team addresses dependability and trust of digital systems at multiple abstraction levels for specific application domains (e.g., automotive, avionics, smartcards, IoT), by guaranteeing that digital circuits possess properties such as quality, reliability, safety, security, availability. The work of the team is focused on design and analysis methods, techniques and tools to assess and improve circuits dependability and trust, for the above-mentioned domains.

Research activities

Robustness and dependability

Many domains have functional safety among the classical list of design constraints e.g., ISO 26262 standard in automotive. Our work aims at improving **early evaluations of dependability** w.r.t. errors induced by environmental disturbances. The goal, to reduce development and production costs, is to be able to evaluate accurately and at an early stage of the design the potential functional effects of soft and permanent errors. We have recently proposed a **cross-layer fault simulation method** to perform the robustness evaluation of critical embedded systems, based on fault injections in both Transaction Level Model (TLM) and Register Transfer Level (RTL) descriptions to make a trade-off between simulation time and realism of the simulated high level faulty behaviors, Another important characteristic of the approach is taking into account the global system specifications in order to discriminate actually critical faults from faults leading to effects with no real consequences on the system behavior. The approach has been applied to an airborne case study. In 2021, the approach has been improved with an iterative flow allowing both the global reduction of the fault injection durations and the improvement of the TLM models along the iterations in order to achieve a good correlation between the consequences of faults injected at TLM and RTL levels.

Another study started in 2021 aims at better evaluating (and predicting) the impact of the software workload on the dependability of complex digital components such as microcontrollers and SoCs. Ultimately, one goal is to define a set of representative benchmarks, allowing a dependability evaluation on critical systems before the actual application program is available. The first step was to develop a versatile profiling tool based on a virtual platform adapted to many processors, coresponding to a modified version of QEMU. This analysis flow has been applied on the RISC-V target and Mibench softwares, allowing us to better understand the impact of software load on SoC fault tolerance. Our proposed metric called “Likelihood Percentage” demonstrated that a high level evaluation with our tool can be very efficient to obtain significant information on program behaviour, coherent with results obtained from both a reference instruction set simulator and a hardware architecture. We have also shown that our profiling tool allows us to compare the behaviour of several programs and exhibits specific characteristics. This data helps in understanding how the processor architecture will be used for each application and therefore what level of fault tolerance can be expected depending on the software load. We formulated three hypotheses that will have to be confirmed with more program examples, the use of several hardware platforms and finally actual tests under particle beams.

In the field of automatic quality or safety assurance level evaluation, we have proposed the first approach towards the automation of the extraction processes of both the valid and faulty state machines within a System-on-a-Chip. The data automatically extracted by this method is a relevant input for behavioural modelization and FMEA (Failure Modes and Effects Analysis) analysis. The method is based on a semi-automated approach for the systematic extraction of failure modes of a digital design in the hypothesis of a single-event upset (SEU) or stuck-at in flip-flops. This procedure aims to enhance human driven failure analysis and provide inputs for RAMS (Reliability, Availability, Maintainability, and Safety) frameworks in the process of quality assurance of complex devices. The main objective is to transport and apply RAMS methods and tools in the area of SoCs design. Experimental results have been conducted on an I2C - AHB system, laying the base for a complete and more complex analysis on an entire SoC [CI3]

Due to technology scaling and transistor size getting smaller and closer to atomic size, the last generation of CMOS technologies presents more variability in various physical parameters. Moreover, circuit wear-out degradation leads to additional temporal variations, potentially resulting in timing and functional failures. To handle such problems, one conventional method consists in providing more safety margins (also called guard bands) at design-time. Therefore, the usage of delay violation **monitors** becomes a must. Placing the monitors is a critical task as the designer has to carefully select the place that will age the most and may become a potential point of failure in a given design.

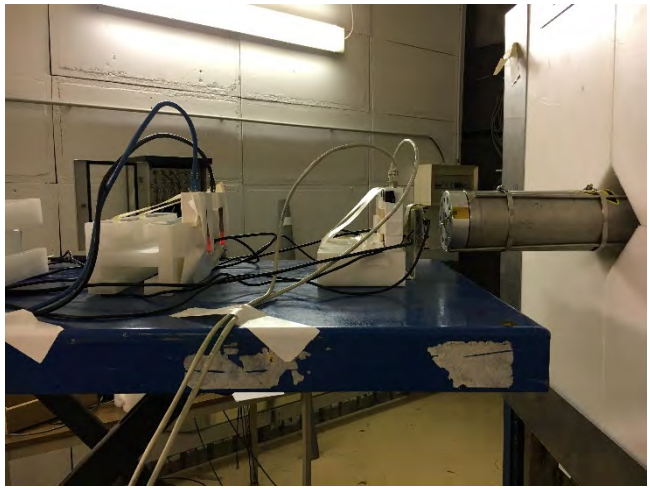
We have explored the use of **Machine Learning techniques** in order to drive the automated selection of potential insertion points of such monitors. Digital delay analysis of basic gates using multiple linear regression has been modeled, predicted, and validated against original data using spice simulation. We have compared multiple linear regression algorithms and used them to study the aging mechanism of CMOS basic gates using supervised learning algorithms. We have showed how it is possible to reliably estimate activity-related path aging and tune the prediction framework by extracting activity profiles from simulations on a synthesized design, which allows a finer grain estimation by obtaining activity profiles at both the path and gate-level.

High-energy particle radiation effects in computing systems

In space environments, aviation altitudes, and ground levels, computing systems' components are liable to high-energy particle radiation-induced transient, accumulative, permanent, and destructive effects. At atmospheric altitudes, for example, neutron environment is primarily responsible for inducing radiation-induced transient effects in avionics and their computing systems. Moreover, the advent of artificial intelligence (AI) systems further extends the computing system applications with self-driving cars, climate-smart agriculture technologies, intelligent medical devices, autonomous monitoring robots/drones, nanosatellites, and spacecraft, making them even more ubiquitous. Within the new era of autonomous things, AI computing solutions are being developed also for the edge of applications, close to sensors, in order to minimize data transfer to/from the cloud and reduce related risks in case of unavailable connections. On the other hand, edge computing is normally resource-constrained in terms of latency, power, and memory, demanding the development of tiny and also reliable machine learning (ML) systems.

In this context, our recent works have assessed and compared the effectiveness of three prominent ML algorithms for tiny ML computing systems in tolerating neutron-induced soft errors. Radiation test-based results suggest that the case-study ML algorithms retain a certain intrinsic level of effectiveness in tolerating neutron effects even thought without any mitigation technique. Notably, random forest algorithm has performed no misclassification during different radiation testing campaigns carried out with 14-MeV and thermal neutron beams.

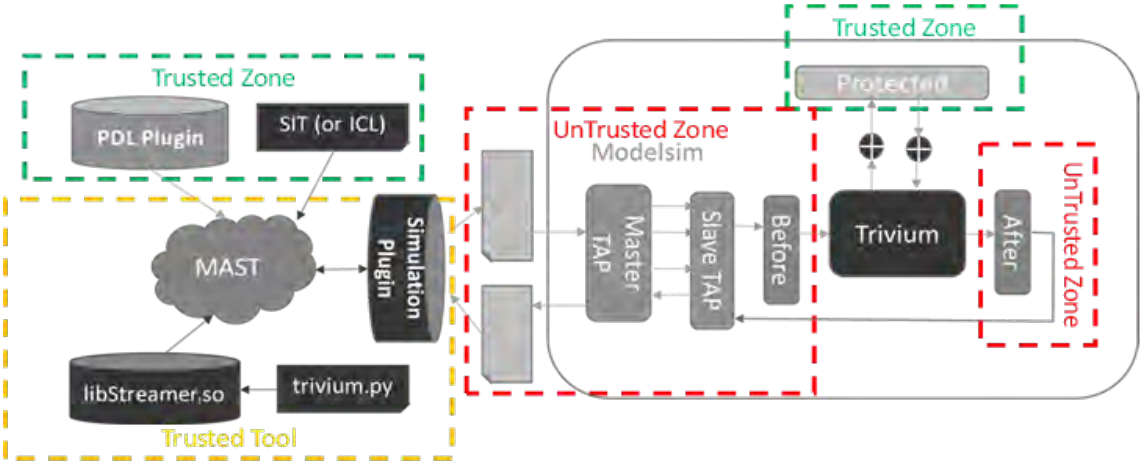
Furthermore, we have also recently assessed neutron radiation effects on the attitude estimation (AE) processing typically embedded in inertial navigation systems (INS) and modern autonomous things. Findings highlight the importance of radiation-induced critical failures that are able to upset INS embedding AE processing modules. Radiation tests were conducted running three strategies for computing different advanced AE algorithms on a case-study processing module exposed to 14-MeV neutron and thermal neutron radiation. Results and analysis suggest that the contribution of radiation-induced soft errors to be mitigated on the AE processing modules is essentially related to single event functional interrupts that can lead inertial navigation to critical failures.



TIMA is also participating of NASA/GFSC's SET program (https://lws-set.gsfc.nasa.gov/) since 2005. The experimental FPGA-based board called COTS-2, devised and designed at TIMA, was included in the NASA/GFSC's SET payload, embedded in the AFRL's DSX spacecraft that was successfully launched on June 25, 2019 at the NASA's Kennedy Space Center (Florida, USA). The DSX spacecraft was in operation until May 31, 2021, weekly providing data to TIMA researchers since June 2019. The NASA/GFSC's SET payload aimed at getting experimental data to study how to better protect satellites/spacecraft against effects of energetic radiation particles present at a medium Earth orbit (MEO) of space, operating around Earth between 6000 km and 12000 km above sea level. The TIMA's COTS-2 board includes an SRAM-based FPGA in which the implemented computing system design was protected by using a classical state-of-the-art fault-tolerance scheme based on Triple Modular Redundancy (TMR). First spaceflight results provide experimental evidences of the risks of using TMR-based schemes in COTS FPGAs operating within MEO.

System-level test and standards

The IEEE 1687-2014 standard and its evolutions like the IEEE P1687.1 (under development) propose solutions for the access and usage of Embedded Instruments, but Electronic Design Automation (EDA) is still limited to only a small subset of the new features. In this context we have improved our innovative Test Flow and Environment called **"Manager for SoC Test" (MAST)**, a software backend able to provide features and performance superior to the industrial legacy solutions. We have proposed innovative solutions that exploits the dynamic nature of the standard to integrate Security features directly into the flow. Our framework extends MAST with novel solutions developed within the team, namely Stream cyphers and Dynamic authentication. We were notably able to integrate Scan Encryption directly inside the EDA tool, allowing Encryption to be natively integrated as a P1687.1 element and be freely mixed inside the Design-of-Test (DfT) infrastructure while retaining full interactive capabilities, while legacy solutions are limited to top-level encryption with offline processing. We then merged this new feature with the ongoing work on Scan Authentication, obtaining the Encryption SIB (eSIB, see Hardware Security and Trust), an Authentication-based Secure Access framework able to provide a trusted, configurable, efficient, and transparent interface to the test infrastructure depending on user-defined security levels. Security-wise, secret sharing is limited to a minimum; from a performance point of view, the tool fully leverages its strength in terms of topology resolution and concurrent execution. Last but not least, we are able to clearly separate the system in Trusted and Untrusted areas, providing an optimal user experience, as se curity is handled automatically and transparently.



Hardware security

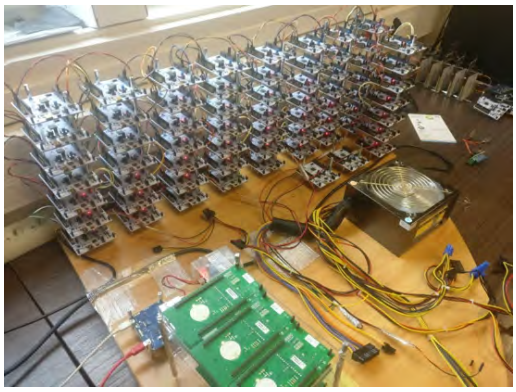
The team works on the design of cryptographic/secure primitives, and the analysis of security threats, by proposing effective countermeasures. We work on algorithms, schemes, and protocols. We have improved our Authenticated and Secure access to the test infrastructure by presenting the **Encryption SIB**, which provides segment-level confidentiality thanks to the dynamic topology supported by our MAST tool (see System-Level test). Our framework not only supports secure procedures such as user authentication or data encryption, but provides these functionalities with a flexible approach that is totally transparent to the user. We also evaluate the resistance of post-quantum cryptography algorithms against physical attacks, which is necessary besides their theoretical evaluation by cryptanalysis. We highlighted a weakness in the Classic McEliece cryptosystem, which can be attacked by laser fault injection. We are working right now on extending this attack to rely only on side-channel analysis, which incurs a much less restrictive attacker model.

Concerning the security threats, we work regularly on implementation attacks. In 2021, we have improved our experimental platform for **physical attacks** on embedded systems. We have acquired the equipment for active EM fault injection and we are currently building a motorized stage to perform extensive experimental campaigns, thanks to the partial support by CNRS (INS2I) and UGA. We have also worked on an emulation platform on FPGA, aimed at evaluating the effects of EM Fault Injection (EMFI) early in the design flow without the need of either EMFI equipment, nor the final ASIC implementation. In an effort to generalize the characterization of fault attacks on complex systems such as CPUs and microcontrollers, we have started working on a **Cross-Layer Methodology** aiming

at understanding and modelling the fault occurrence mechanisms within the microarchitecture of modern processors, and map this model to upper levels with the final goal of designing optimal countermeasures.
We have addressed the problem of cache timing attacks, which have become very popular in recent years. Eviction set construction is a common step for many such attacks, and algorithms for building them are evolving rapidly. On the other hand, countermeasures are also being actively researched and developed. However, most countermeasures have been designed to secure last-level caches and few of them actually protect the entire memory hierarchy. Cache randomization is a well-known mitigation technique against cache attacks that has a low-performance overhead. We have proposed solutions to determine whether address randomization on first-level caches is worth considering from a security perspective. The work included the implementation of a noise-free cache simulation framework that enables the analysis of the behavior of eviction set construction algorithms. We show that randomization at the first level of caches (L1) brings about improvements in security but is not sufficient to mitigate all known algorithms, such as the recently developed Prime–Prune–Probe technique [CI-14]
In the same context, a study has first shown that Intel mitigations to avoid attacks against secure enclaves (SGX) can be efficient, but not sufficient in all attack scenarios. We have also evaluated the feasibility of the Prime&Probe attack on a system with the CVA6 RISC-V processor. With a bare-metal implementation, it has been shown that the attack works, although a noticeable effort was necessary in terms of reverse engineering of the cache accesses and analysis of the behavior. An attack considered as “turnkey” is not so easy to implement, even without mitigations. Adding additional processes as perturbators, the attack is more complex but still succeeds after analysis of the cache behavior. Currently, work is on-going with the attack implemented under Linux.
In the context of **Control Flow Hardening**, we have proposed the use of nonlinear codes. Hardware-based control flow monitoring techniques enable to detect both errors in the control flow and the instruction stream being executed on a processor. However, these techniques may fail to detect malicious carefully tuned manipulation of the instruction stream in a basic block. We have shown how using a non-linear encoder and checker can cope with this weakness [RI-8]

Hardware trust

The quest of low production cost and short time-to- market, as well as the complexity of modern integrated circuits pushed towards a globalization of the supply chain of silicon devices. Such production paradigm raised a number of trust threats. We are actively working on the proposition of novel solutions to address this problem. In particular, we are proposing novel methods, architectures and protocols for the identification and authentication of hardware devices based on Physically Unclonable Functions (PUFs), as well as mitigation techniques for Hardware Trojans.



Concerning the PUFs, we have proposed: (i) an experimental platform for the evaluation of SRAM-based PUFs; (ii) a theoretical method for the assessment of the reliability of PUFs; (iii) the use of emerging technologies (resistive and magnetic memories) as building block for new PUF architectures; (iv) a novel concept for the enrollment of strong PUF based on machine learning; (v) a new protocol for key exchange which does not require cryptographic primitives [CI-8] [O-1]
In the context of Hardware Trojans (HTs), we worked on the use of software obfuscation to protect systems against HTs that aim at stealing information from the microprocessor while it is executing a program. The method is enhanced by a Genetic Algorithm-based approach to optimize the obfuscation level while minimizing the introduced overhead. We proved the effectiveness and efficiency of the proposed methodology on the Ariane 64bit RISC-V microprocessor running a set of MiBench benchmarks and cryptographic programs.
We also proposed an HT attack for analog circuits, in the context of Systems-on-Chip (SoCs) comprising both digital and analog Intellectual Property (IP) blocks. The HT trigger is placed inside a dense digital IP block where it can be effectively hidden, whereas the HT payload is in the form of a digital pattern transported via the test bus or generated within the test bus, reaching the Design-for-Test (DfT) or programmability interface of the victim analog IP with the test bus. The HT payload unexpectedly activates the DfT and sets the victim analog IP into some possibly partial and undocumented test mode or changes the nominal programmability [RI-3].

New hardware computing approaches

Today's computing systems are facing several issues related to architectural and technological limitations. To mitigate these issues, novel computing paradigms, such as **Computing-in-Memory**, **Neuromorphic Computing** and **Approximate Computing**, are being researched, in conjunction with novel emerging technologies such as memristive and spintronic devices. Concerning these devices, our research aims at using enhanced compact models to perform failure analysis, and define pertinent fault models to establish design-for-test and design-for-reliability methodologies. Concerning the Computing-in-Memory paradigm, we are investigating feasible design solutions, with a special focus on applications for security [CI-10] [CI-13]. Concerning Neuromorphic Computing, we are focusing on the design of efficient Spiking Neural Networks with on-line unsupervised learning and the reliability analysis and test of such networks. Concerning the Approximate Computing paradigm, which has been gaining momentum both in the industry and in academia, we are studying the trade-offs between selective approximation (or occasional violation of specifications) and power consumption. We have focused on Floating Point dynamic approximation, with an impact evaluated i) at algorithm and application level and ii) at hardware level with the design of a configurable FPU ([RI-2] and [RI-9]) . We are also working on an extension of a tool initially developed for dependability evaluation (EARS) in order to identify from RTL descriptions the operators that are the less sensitive to approximations for a given application. In 2021, EARS has been modified to include new metrics and also to better link the multi-bit elements in the RTL description (e.g., operators) to the analysis results. Several benchmarks have also been prepared; the next step is to compare the results of EARS with the results of the manual benchmarks analyses.

Involvement in research activities:

- Elena Ioana VATAJELU: responsable axe systèmes robustes fiables et sécurisés GDR SoC2
- Elena Ioana VATAJELU: Member of IEEE CEDA Executive Committee
- Participation to the IEEE P1687.1 Working Group
- Participation to the Grenoble Alpes CyberSecurity Institute
- Chair of TTTC – IEEE Computer Society
- Chair of TTEP Educational Program of TTTC
- In charge of Microelectronics within FMNT

Platforms and demonstrators:

- A comprehensive platform for hardware/software co-design based on the RISC-V processor architecture. The platform supports several RISC-V implementations (such as the Rocket Chip or CVA6) and it features high modularity and tuning capabilities (https://tima-amfors.gricad-pages.univ-grenoble-alpes.fr/learnv/).
- Hardware demonstrator for Secure Access to 1687 Test Infrastructure
- Experimental platforms for Physical Attacks and PUF evaluation
- Emulation platform for EM Fault Injection
- Accelerated radiation testing platform for assessing computing systems under high-energy neutron radiation effects

Recent highlights

January 24, 2023: HDR thesis defence of Elena Ioana VATAJELU: Emerging Memories for Dependable Computing
https://tima.univ-grenoble-alpes.fr/news/hdr-thesis-defence-Elena Ioana-vatajelu-amfors-team-emerging-memories-dependable-computing

February 7, 2023: HDR thesis defence of Mounir BENABDENBI: Contributions to the Test, Fault Tolerance and Approximate Computing of System on a Chip
https://tima.univ-grenoble-alpes.fr/news/hdr-thesis-defence-mounir-benabdenbi-amfors-team-contributions-test-fault-tolerance-and-approximate

March 3, 2023: Scientific Day: Hardware Security
These Scientific Days are meant to present the research topics and to disseminate the recent advances of TIMA researchers. These presentations are open to everybody, whether they are members of TIMA or not.
Program: 2023_03_03_amfors_hardware_security.pdf

April 5, 2023: Paolo MAISTRI's speech at FIC 2023 (Forum International de la Cybersécurité)
Paolo's speech (TIMA - AMfoRS team) at FIC 2023 - Hacking Lab:
https://www.youtube.com/watch?v=h4z0mn-sLt4&list=PLsaypbHfNQukAVvWa4o3bTZMwX-b9vkn_&index=9

April 25, 2023: DATE 2023 - Outstanding Performance Servicing DATE
Congratulations to Giorgio DI NATALE

May 5, 2023: DDECS 2023 Best student paper award
Congratulations to Sergio VINAGRERO GUTIERREZ, Pietro INGLESE, Giorgio DI NATALE, Elena Ioana VATAJELU

June 9, 2023: Elena-Elena Ioana VATAJELU's talk at IEEE CASS RS Talks 2023

Elena Ioana VATAJELU's talk at IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil
Title: Versatility of Emergent Memory Technologies: Friend or Foe?

September 27, 2023: Elena-Elena Ioana VATAJELU's interview for CNRS INS2I newsletter

Elena-Elena Ioana VATAJELU's interview for CNRS INS2I newsletter (27/09/2023)
Title: L'informatique neuromorphique en quête d'un calcul plus efficace en ressources (french only)
https://www.ins2i.cnrs.fr/fr/cnrsinfo/linformatique-neuromorphique-en-quete-dun-calcul-plus-efficace-en-ressources

November 16, 2023: CARDIS 2023 Best Student Paper Award

Congratulations to Ihab ALSHER, Brice COLOMBIER and Paolo MAISTRI for receiving the CARDIS 2023 Best student paper Award for their work entitled:
"Microarchitectural Insights into Unexplained Behaviors under Clock Glitch Fault Injection"

Academic and research members

Mounir BENABDENBI

Position
Associate Professor at Grenoble INP - Phelma school

Responsibilities
Researcher in AMfoRS team

Cyrille CHAVET

Position
Associate Professor at Grenoble INP - Phelma school since 01/09/2023

Responsibilities
Researcher in AMfoRS team since 01/09/2023

Giorgio DI NATALE

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team
Director of TIMA Lab. Since 01/01/2021

Régis LEVEUGLE

Position
Professor at Grenoble INP - Phelma school

Responsibilities
Researcher in AMfoRS team

Paolo MAISTRI

Position
Researcher at CNRS

Responsibilities
Leader of AMfoRS team
Researcher in AMfoRS team

Michele PORTOLAN

Position
Associate Professor at Grenoble INP - Phelma school

Responsibilities
Researcher in AMfoRS team

Rodrigo POSSAMAI BASTOS

Position
Associate Professor at UGA - IM2AG school

Responsibilities
Researcher in AMfoRS team

Elena-Elena Ioana VATAJELU

Position
Researcher at CNRS

Responsibilities
Researcher in AMfoRS team
Responsible for Gender equality

Raoul VELAZCO

Position
Emeritus research Director at CNRS until 20/10/2023

Responsibilities
Researcher in AMfoRS team until 20/10/2023

Nacer-Eddine ZERGAINOH

Position
Associate Professor at UGA - Polytech school

Responsibilities
Researcher in AMfoRS team

CNRS (French National Center for Scientific Research)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
POLYTECH school (École Polytechnique de l'Université Grenoble Alpes)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. ALSHAER Ihab
Title of thesis: **Cross-Layer Fault Analysis for Microprocessor Architectures (CLAM)**
Completed on: **October 16, 2023**
Previous degrees: Engineer

2. BOULIFA Roua
Title of thesis: **Robust and Secure RISC-V Architecture**
Expected date of defense: **2025**
Previous degrees: Master - Université de Tunis - El Manar - Le kef, Tunisia (2022)

3. DADDINOUNOU Salah
Title of thesis: **Test and reliability of emerging memory-based spiking neural networks**
Expected date of defense: **2024**
Previous degrees: Master - Université Paris-Sud Orsay – Paris, France (2019)

4. DOUADI Aghiles
Title of thesis: **Design and evaluation of countermeasures against power-off laser fault injection attacks**
Expected date of defense: **2025**
Previous degrees: Master STS - Université de Bourgogne – Dijon, France (2022)

5. EL AMRAOUI Sami
Title of thesis: **Fault Injection on** Digital **Circuits: Modelling and Protecting against ElectroMagnetic Pulses**
Expected date of defense: **2025**
Previous degrees: Engineer – INPT (Institut National des Postes et Télécommunications) – Rabat, Moroco (2022)

6. FIORUCCI Tiziano
Title of thesis: **Qualification methodology for ISO26262 certification of automotive SoC systems**
Completed on: **June 6, 2023**
Previous degrees: Master - Università degli Studi di Roma Tor Vergata - Roma – Italy (2019)

7. INGLESE Pietro
Title of thesis: **Exploration of security threats in In-Memory Computing Paradigms**
Completed on: **December 7, 2023**
Previous degrees: Engineer – Politecnico di Torino - Italy (2019)

8. KOROLEVA Aleksandra
Title of thesis: **Study and development of La2NiO4 memristive devices for bio-inspired computing**
Expected date of defense: **2025**
Previous degrees: Master of Science - Moscow Institute of Physics and Technology – Russia (2019)

9. KOUAMO Jules
Title of thesis: **Architectures and Software Methods for Mixed System Testing**
Expected date of defense: **2026**
Previous degrees: Master of Computer science – Yaoundé University – Cameroon (2023)

10. KRAEMER SARZI SARTORI Tarso
Title of thesis: **Mitigation of radiation effects on the attitude estimation processing of autonomous things**
Completed on: **October 17, 2023**
Previous degrees: Master – Aerospace engineering – Federal University of Santa Maria, Brazil (2020)

11. LAURINI Luiz Henrique
Title of thesis: **Online Functional Testing and Designing Methods for Embedded Computing Systems**
Expected date of defense: **2026**
Previous degrees: Master of EEA – Université Grenoble Alpes – France (2023)

12. MARTINOLI Valentin
Title of thesis: **Secure Processors with respect to Micro Architectural Attacks**
Completed on: **March 23, 2023**
Previous degrees: Engineer – Ecole des Mines – Saint-Etienne / Gardanne, France (2019)

13. NOIZETTE Luc
Title of thesis: **Predictive fault tolerance analysis methodology for complex components with consideration of the application**
Expected date of defense: **2024**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2020)

14. OULDEI TEBINA Nasr-Eddine
Title of thesis: **Sensitivity Analysis and Design Methodology for Secure Digital Circuits against X-Rays**
Expected date of defense: **2024**
Previous degrees: Master - Université de Montpellier Montpellier, France (2020)

15. SUZANO DA FONSECA Juan
Title of thesis: **3D Heterogeneous technologies for Digital secured & sovereign solutions**
Expected date of defense: **2025**
Previous degrees: Engineer - CPE Lyon, France (2021)

16. TALY Emilien
Title of thesis: **Design of a very low power Artificial Intelligence system (Tensor Processing Unit - TPU) based on memory computation**
Expected date of defense: **2024**
Previous degrees: Master – Université de Montpellier, France (2020)

17. VINAGRERO GUTIERREZ Sergio
Title of thesis: **Design and Evaluation of Resistive-based Security Primitives (Physically Unclonable Function & True Random** Number **Generator)**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA (Université Grenoble Alpes), France (2021)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. DADDINOUNOU (ATER)	Salah	ALGERIA	3 months
2. NGUYEN (engineer)	Ngoc-Anh	VIET NAM	4,5 months

Visitors

Name	Forename	Country	Duration
1. DE AZAMBUJA	Jose Rodrigo	FRANCE	2 months

Trainees

Name	Forename	Country	Duration
1. BASSO PEREIRA	Isabella	FRANCE	4 months
2. BOUAAMRI	Malak	MOROCCO	3 months
3. BURGHOORN	Gijs Juurd	NETHERLANDS	7 months
4. CHARLES	Matthieu	FRANCE	6 months
5. CLEMENT	Arthur	FRANCE	2,5 months
6. DUCHADEAU	Romain	FRANCE	3 months
7. HOLLMANN	Kevin	FRANCE	3 months
8. IBRAIM	Alua	KAZASTAN	2,5 months
9. KULAGIN	Vasilii	FRANCE	3,5 months
10.LAURINI	Luiz Henrique	BRAZIL	6 months
11.OLIVEIRA	Aquiles	BRAZIL	2,5 months
12.SABIA PEREIRA CARPES	Victor	BRAZIL	3 months
13.ZYNGER CAPAVERDE	Betina		2,5 months

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2023.

ANR

BAC4NOSE (2023 – 2027)
Scientific manager: Elena Ioana VATAJELU

EMINENT (2019 – 2023)
Scientific manager: Elena Ioana VATAJELU

MITIX (2020 – 2027)
Scientific manager: Paolo MAISTRI

POP (2021 – 2025)
Title: Attaque laser de primitives de sécurité non alimentées
Scientific manager: Giorgio DI NATALE

CIFRE

Thèse Tiziano FIORUCCI (2020 – 2023)
Title: Qualification methodology for ISO26262 certification of automotive SoCsystems
Thesis director: Giorgio DI NATALE
Industrial partner: STMicroelectronics

Thèse Antoine LINARES (2020 – 2023)
Title: Flexible Hardware for Intrinsic Secure Computing
Thesis director: Giorgio DI NATALE
Industrial partner: SiFive

Thèse Valentin MARTINOLI (2020 – 2023)
Title: Secure Processors with respect to Micro Architectural Attacks
Thesis director: Régis LEVEUGLE
Industrial partner: Thalès

Thèse Luc NOIZETTE (2021 – 2024)
Title: Predictive fault tolerance analysis methodology for complex components with consideration of the application
Thesis director: Régis LEVEUGLE
Industrial partner: Nucletudes

Thèse Emilien TALY (2021 – 2024)
Title: Design of a very low power Artificial Intelligence system (Tensor Processing Unit - TPU) based on memory computation
Thesis director: Elena Ioana VATAJELU
Industrial partner: STMicroelectronics

EUROPE

NEUROPULS (2023 – 2026)
Program: Horizon Europe
Scientific manager: Elena Ioana VATAJELU

PEPR

ARSENE (2022 – 2026)
Program: Cyber
Scientific manager: Paolo MAISTRI

REGION

MULTIRAD (2020 – 2023)
Program: Pack Ambition International
Scientific manager: Rodrigo POSSAMAI BASTOS

TUTELLE

80 PRIME 2022 (2023 – 2024)
Program: Prime
Scientific manager: Elena Ioana VATAJELU

CAFET (2023 – 2024)
Program: Labex Persyval
Scientific manager: Mounir BENABDENBI

CLAM (2020 – 2023)
Program: Equipe-Action Labex Persyval
Title: Cross-Layer Fault Analysis for Microprocessor Architectures
Scientific manager: Paolo MAISTRI

SYNCONNECT (2022 – 2024)
Program: MIAI
Scientific manager: Elena Ioana VATAJELU

Thèse SARTORI (2020 – 2023)
Program: Labex Persyval
Scientific manager: Rodrigo POSSAMAI BASTOS

Organization and participation of international conferences, workshops, forums

AI-TREATS 2023 – 3rd IEEE Workshop on AI Hardware: Test, Reliability and Security
May 25-26, 2023 - Venice, ITALY
Rank: NC
general chair: VATAJELU Elena-Elena Ioana

DATE 2023 - Design, Automation & Test in Europe
April 17-19, 2023 - Antwerp, BELGIUM
Rank: A+
DATE Fellow: DI NATALE Giorgio
proceedings chair: VATAJELU Elena-Elena Ioana
topic member: VATAJELU Elena-Elena Ioana

DDECS 2023 - 26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems
May 3-5, 2023 - Tallinn, ESTONIA
Rank: B
technical program committee: LEVEUGLE Régis, MAISTRI Paolo, PORTOLAN Michele
topic chair: VATAJELU Elena-Elena Ioana

DFT 2023 - 36th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems
October 3-5, 2023 - Juan-les-Pins, FRANCE
Rank: A
technical program committee: DI NATALE Giorgio

ETS 2023 - 28th IEEE European Test Symposium
May 22-26, 2023 - Venice, ITALY
Rank: A
organization committee: DI NATALE Giorgio
steering committee: DI NATALE Giorgio, VATAJELU Elena-Elena Ioana
technical program committee: BENABDENBI Mounir, LEVEUGLE Régis, PORTOLAN Michele
topic chair: VATAJELU Elena-Elena Ioana

GDR SoC 2 2023 - 17ème Colloque du GDR SoC2
June 12-14, 2023 - Lyon, FRANCE
Rank: NC
animation committee: VATAJELU Elena-Elena Ioana

GDR SoC 2 2023 – Barcamp X-GDR Défis d'Implémentation de l'IA – Sécurité, Fiabilité, Soutenabilité et Nouvelles Technologies
December 13-15, 2023 – Aussois, FRANCE
Rank: NC
general chair: VATAJELU Elena-Elena Ioana

IOLTS 2023 - 29th IEEE International Symposium on On-Line Testing and Robust System Design
July 3-5, 2023 - Chania (Crete), GREECE
Rank: B
emeritus chair: NICOLAIDIS Michael
program committee: DI NATALE Giorgio, PORTOLAN Michele
steering committee: NICOLAIDIS Michael

ISVLSI 2023 - IEEE Computer Society Annual Symposium on VLSI
June 20-23, 2023 - Iguazu Falls, BRAZIL
Rank: A
track chair: VATAJELU Elena-Elena Ioana

LATS 2023 - 24th IEEE Latin-American Test Symposium
March 21-24, 2023 - Veracruz, MEXICO
Rank: NC
past chair: VELAZCO Raoul
program committee: BENABDENBI Mounir, LEVEUGLE Régis, PORTOLAN Michele, POSSAMAI BASTOS Rodrigo, VATAJELU Elena-Elena Ioana
publicity chair: VATAJELU Elena-Elena Ioana
steering committee: VELAZCO Raoul

PESW 2023 - 11th Prague Embedded Systems Workshop
June 29-July 1, 2023 - Prague, CZECH REP.
Rank: NC
program committee: DI NATALE Giorgio

RADECS 2023 - RADiation and its Effects on Components and Systems
September 25-29, 2023 - Toulouse, FRANCE
Rank: NC
program committee: POSSAMAI BASTOS Rodrigo

SBCCI 2023 - 36th Symposium on Integrated Circuits and Systems Design
August 28-September 1, 2023 – Rio de Janeiro, BRAZIL
Rank: B
program committee: POSSAMAI BASTOS Rodrigo
track co-chair: POSSAMAI BASTOS Rodrigo

SETS 2023 – South-European Test Symposium
March 6-10, 2023 – Bourg Saint-Maurice, FRANCE
Rank: NC
general chair: VATAJELU Elena Ioana

TSS 2023 – Test Spring School
May 19-22, 2023 – Venice, ITALY
Rank: NC
co-general chair: VATAJELU Elena Ioana

VTS 2023 - 41st IEEE VLSI Test Symposium
April 24-26, 2023 - San Diego (CA), USA
Rank: A
registration chair: VATAJELU Elena-Elena Ioana

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
Phelma school PHysique – ELectronique - MAtériaux				
Manager of SEOC/PHELMA branch	PORTOLAN Michele	01/09/2017		
Polytech Grenoble				
Manager of 4th & 5th years internship	ZERGAINOH Nacer-Eddine	01/09/2021		
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Manager of Office Automation and Informatics	POSSAMAI BASTOS Rodrigo	01/09/2017		Formation à tous les parcours du Département Licence Sciences et Technologies de l'UGA
UGA DLST Département licence sciences et technologies / Science and technology degree department				
Head of Licence 2 (L2) course in Mathematics - Computer Science International (MIN Int)	POSSAMAI BASTOS Rodrigo	01/01/2022		
TIMA Laboratory				
TIMA Laboratory				
Parity referent	VATAJELU Elena Ioana	01/09/2022		
Partnership and Development Correspondent	PORTOLAN Michele	01/09/2022		
Research structures				
MSTIC pole Mathématiques, sciences et technologies de l'information et de la communication				
Council member of MSTIC cluster	LEVEUGLE Régis	01/09/2015		Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC

Scientific production

International journals

Gava Jonas*, Hanneman Alex, Abich Geancarlo*, Garibotti Rafael***, Cuenca-Asensi Sergio****, Possamai Bastos Rodrigo, Reis Ricardo*, Ost Luciano****
A Lightweight Mitigation Technique for Resource-constrained Devices Executing DNN Inference Models under Neutron Radiation
IEEE Transactions on Nuclear Science, Volume: , pp. 1-1, 2023
**UFRGS - Université fédérale du Rio Grande do Sul, **Loughborough University, ***PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ****Universidad de Alicante*

Khuu Thoai-Khanh*, Koroleva Aleksandra*, Degreze Arnaud*, Vatajelu Elena Ioana, Lefèvre Gauthier, Jimenez Carmen*, Blonkowski Serge**, Jalaguier Eric**, Bsiesy Ahmad***, Burriel Mónica***
Analogue Memristive Devices based on La2NiO4+δas Synapses for Spiking Neural Networks
Journal of Physics D: Applied Physics, Volume: , 2023
**Laboratoire des Matériaux et du Génie Physique, **Laboratoire d'Electronique de Technologie de l'Information, ***Laboratoire de Spectrométrie Physique*

Gava Jonas*, Moura Nicolas, Lucena Joaquim**, Da Rocha Vinicius**, Garibotti Rafael**, Calazans Ney**, Cuenca-Asensi Sergio***, Possamai Bastos Rodrigo, Reis Ricardo*, Ost Luciano******
Assessment of Radiation-Induced Soft Errors on Lightweight Cryptography Algorithms Running on a Resource-constrained Device
IEEE Transactions on Nuclear Science, Volume: , 2023
**UFRGS - Université fédérale du Rio Grande do Sul, **PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ***Universidad de Alicante, ****Loughborough University*

Serrano-Cases Alejandro*, Martinez-Alvarez Antonio, Possamai Bastos Rodrigo, Cuenca-Asensi Sergio****
Bare-Metal Redundant Multi-Threading on Multicore SoCs under Neutron Irradiation
IEEE Transactions on Nuclear Science, Volume: , pp. 1, 2023
**Barcelona Supercomputing Center - Centro Nacional de Supercomputacion, **Universidad de Alicante*

Kraemer Sarzi Sartori Tarso*, Kraemer Sarzi Sartori Tarso, Laurini Luiz Henrique, Fourati Hassen*, Possamai Bastos Rodrigo
Effectiveness of Attitude Estimation Processing Approaches in Tolerating Radiation Soft Errors
IEEE Transactions on Nuclear Science, Volume: , 2023
**GIPSA-Lab*

Farahmandi Farimah*, Srivastava Ankur, Di Natale Giorgio, Tehranipoor Mark***
Introduction to the Special Issue on CAD for Security: Pre-silicon Security Sign-off Solutions Through Design Cycle
ACM Journal on Emerging Technologies in Computing Systems, Volume: 19, pp. 1-4, 2023
**Department of Electrical and Computer Engineering [Gainesville] , **Department of Electrical and Computer Engineering [Univ. of Maryland]*

Laurini Luiz Henrique, Dos Santos Martins Joao Baptista*, Possamai Bastos Rodrigo
Investigation of Edge Computing Hardware Architectures Processing Tiny Machine Learning under Neutron-induced Radiation Effects
Microelectronics Reliability, Volume: , 2023
**Universidade Federal de Santa Maria*

Kraemer Sarzi Sartori Tarso, Fourati Hassen*, Possamai Bastos Rodrigo
Learning-based Mitigation of Soft Error Effects on Quaternion Kalman Filter Processing
Sensors Journal , Volume: , pp. 1-1, 2023
**GIPSA-Lab*

Possamai Bastos Rodrigo, Gorchs Picas Marti, Velazco Raoul
Medium-Earth Orbit Spaceflight Radiation Effects in Triple Modular System on Programmable Device
IEEE Transactions on Nuclear Science, Volume: , pp. 1, 2023

Vinagrero Gutierrez Sergio, Di Natale Giorgio, Vatajelu Elena Ioana
Python Framework for Modular and Parametric SPICE Netlists Generation
Electronics, Volume: 12, pp. 3970, 2023

Papavramidou Panagiota, Nicolaidis Michael
Reducing Power Dissipation in Memory Repair for High Fault Rates
IEEE Transactions on Very Large Scale Integration (VLSI) Systems , Volume: 31, pp. 2112-2125, 2023

Anghel Lorena*, Cantoro Riccardo, Masante Riccardo**, Portolan Michele, Sartoni Sandro**, Sonza Reorda Matteo****
Self-Test Library Generation for In-field Test of Path Delay faults
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: , pp. 1-1, 2023
**Spintec, **Politecnico di Torino*

Inglese Pietro, Vatajelu Elena Ioana, Di Natale Giorgio
Side Channel and Fault Analyses on Memristor-Based Logic In-Memory
IEEE Design & Test, Volume: , pp. 1, 2023

Rajappa Anuj Justus*, Reiter Philippe*, Kraemer Sarzi Sartori Tarso, Laurini Luiz Henrique, Fourati Hassen, Mercelis Siegfried*, Famaeya Jeroen*, Possamai Bastos Rodrigo**
SMART: Selective MAC zero-optimization for neural network reliability under radiation
Microelectronics Reliability, Volume: , 2023
**Universiteit Antwerpen = University of Antwerpen [Antwerpen] , **GIPSA-Lab*

Vinagrero Gutierrez Sergio, Martin Honorio*, de Bignicourt Alice, Vatajelu Elena Ioana, Di Natale Giorgio
SRAM-Based PUF Readouts
Scientific Data, Volume: 10, 2023
**Universidad Carlos III of Madrid - Electronics Technology Department*

Dyer Clive*, Ryden Keith A.*, Morris Paul*, Hands Alex D. P.*, McNulty Peter J., Vaillé Jean-Roch***, Dusseau Laurent***, Cellere Giorgio****, Paccagnella Alessandro****, Barnaby Hugh J.*****, Benedetto Adalin R.*****, Velazco Raoul, Possamai Bastos Rodrigo, Brewer Dana******, Barth Janet L.*******, Barth Janet L.********, LaBel Kenneth A.********, LaBel Kenneth A.*********, Campola Michael J.********, Zheng Yihua********, Xapsos Michael A.********
The Living With a Star Space Environment Testbed Payload
IEEE Transactions on Nuclear Science, Volume: , pp. 1, 2023
Surrey Space Centre [Guildford] - University of Surrey , **Department of Physics and Astronomy, Clemson University, ***Université de Montpellier, ****Department of Information Engineering [Padova], *** School of Electrical, Computer and Energy Engineering - Arizona State University, ******NASA Headquarters, ******* Cornell Technical Services, ********NASA Goddard Space Flight Center, *********Science Systems and Applications, Inc. [Lanham]*

Noizette Luc, Miller Florent*, Colladant Thierry, Helen Youri***, Leveugle Régis**
Understanding the Link Between Complex Digital Devices Soft Error Rate and the Running Software
IEEE Transactions on Nuclear Science, Volume: 70, pp. 1747-1754, 2023
**Nucletudes, **Direction générale de l'Armement , ***DGA Maîtrise de l'information (Bruz)*
Martin Honorio*, Dupuis Sophie , Di Natale Giorgio***, Entrena Luis***
Using Approximate Circuits Against Hardware Trojans
IEEE Design & Test, Volume: 40, pp. 8-16, 2023
**UC3M - Universidad Carlos III de Madrid, ** LIRMM Montpellier*

Invited conference talks

Possamai Bastos Rodrigo
MultiRad Platform for Testing Case-Study Algorithm Applications in Computing Systems under Neutron Radiation
Invited talk presented at the Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, April 27 , Porto Alegre, BRAZIL
Possamai Bastos Rodrigo
Reliability of Computing Systems and Components Facing Cosmic Ray Radiation Effects
Invited talk presented in the work group FIMA (Modèles Aléatoires pour la Fiabilité et la Maintenance des Systèmes) of the IMdR (Institut pour la Maîtrise des Risques), Grenoble, France, March 2 , 2023
Possamai Bastos Rodrigo
Reliability of Computing Systems and Components Facing Cosmic Ray Radiation Effects
Invited talk presented as a course within the ”Formation continue : ingénierie système appliquée au spatial : instrumentation spatiale et données” organized by the CSUG (Centre spatial universitaire de Grenoble) of the UGA. Grenoble, October 26 , 2023
Possamai Bastos Rodrigo
Reliability of Computing Systems and Components Facing Cosmic Ray Radiation Effects
Invited talk presented as a course and practical activities with thermal neutron source at the ILL (Institut Laue Langevin) within the IRT-Nanoelec training ”Synchrotron X-ray and neutron applied to nano-electronics” for PhD students of the doctoral school EEATS of the UGA. Training organized by the radiation facilities ILL and ESRF (European Synchrotron Radiation Facility). Grenoble, March 30 and 31 2023
Noizette Luc, Miller Florent*, Colladant Thierry, Helen Youri**, Leveugle Régis**
Soft-SoC robustness evaluation using X-rays: a case study and differences with other beams
36th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS'23), 2023
**Nucletudes, **Direction générale de l'Armement*

International conferences

Benevenuti Fabio*, Gobatto Leonardo*, Possamai Bastos Rodrigo, Azambuja José Rodrigo*, Kastensmidt Fernanda Lima*
Assessing the Arm Cortex-M under Radiation with and without a Real-time Operating System
Conference on Radiation Effects on Components and Systems (RADECS 2023), 2023
**UFRGS - Université fédérale du Rio Grande do Sul*
Douadi Aghiles, Di Natale Giorgio, Maistri Paolo, Vatajelu Elena Ioana, Beroulle Vincent*
A Study of High Temperature Effects on Ring Oscillator based Physical Unclonable Functions
29th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS 2023), pp. 1-6, 2023
**Laboratoire de Conception et d'Intégration des Systèmes*
Vatajelu Elena Ioana
Emerging non-volatile memories: Operation Principles & Main Applications
Ecole thématique portant sur l'architecture des systèmes matériels et logiciels embarqués, et les méthodes de conception associées (ARCHI 2023)
Di Natale Giorgio
Ensuring trustworthiness and integrity of CPS hardware components
CPS Summer School 2023
Cantoro Riccardo*, Sartoni Sandro*, Sonza Reorda Matteo*, Anghel Lorena, Portolan Michele**
Evaluating the Impact of Aging on Path-Delay Self-Test Libraries
IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2023), pp. 1-7, 2023
**Politecnico di Torino, **Spintec*
Esmaeilian Maryam*, Douadi Aghiles, Kazemi Zahra*, Beroulle Vincent*, Amir-Pasha Mirbaha*, Fazeli Mahdi, Vatajelu Elena Ioana, Maistri Paolo, Di Natale Giorgio**
Experimental Evaluation of Delayed-Based Detectors Against Power-off Attack
IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS 2023), 2023
**Laboratoire de Conception et d'Intégration des Systèmes, **Halmstad University*
Leveugle Régis
Hardening by design: methods and perspectives
8th European Cyber Week, Seminar BITFLIP by DGA
Fleck Marcos Antônio Junior*, Pereira Elisa*, Gava Jonas, Moraes Fernando Gehm*, Calazans Ney*, Meneguzzi Felipe*, Possamai Bastos Rodrigo, Reis Ricardo**, Ost Luciano***, Garibotti Rafael***
Impact of Radiation-Induced Soft Error on Object Detection Algorithm of Unmanned Surface Vehicles
Conference on Radiation Effects on Components and Systems (RADECS 2023), 2023
**PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, **UFRGS - Université fédérale du Rio Grande do Sul, ***Loughborough University*
Laurini Luiz Henrique, Dos Santos Martins Joao Baptista*, Possamai Bastos Rodrigo
Investigation of Edge Computing Hardware Architectures Processing Tiny Machine Learning under Neutron-induced Radiation Effects
European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2023), 2023
**Universidade Federal de Santa Maria*
Alshaer Ihab*, Alshaer Ihab, Colombier Brice, Deleuze Christophe*, Beroulle Vincent*, Maistri Paolo**
Microarchitectural Insights into Unexplained Behaviors under Clock Glitch Fault Injection
22nd Smart Card Research and Advanced Application Conference (CARDIS 2023), pp. 1-20, 2023
**Laboratoire de Conception et d'Intégration des Systèmes, **Laboratoire Hubert Curien*
Vatajelu Elena Ioana
Neuromorphic Computing: Spiking vs. For mal Neural Networks, a Reliability Perspective
HiPEAC2023 - NEUROCOM Workshop

Pavanello Fabio*, Marchand Cédric*, O'Connor Ian*, Orobtchouk Régis*, Mandorlo Fabien*, Letartre Xavier*, Cueff Sébastien*, Vatajelu Elena Ioana, Di Natale Giorgio, Cluzel Benoit, Coillet Aurélien**, Charbonnier Benoit***, Noé Pierre***, Kaván František****, Zoldak Martin****, Szaj Michal****, Bienstman Peter*****, Van Vaerenbergh Thomas*****, Rührmair Ulrich******, Flores Paulo*******, Guerra e Silva Luis*******, Chaves Ricardo*******, Silveira Luis Miguel*******, Ceccato Mariano********, Gizopoulos Dimitris*********, Papadimitriou George*********, Karakostas Vasileios*********, Brando Axel**********, Cazorla Francisco Javier**********, Canal Ramon**********, Closas Pau**********, Gusi Amigo Adrià**********, Crovetti Paolo Stefano**********, Carpegna Alessio**********, Tzamn Melendez Carmona**********, Di Carlo Stefano**********, Savino Alessandro**********
NEUROPULS: NEUROmorphic energy-efficient secure accelerators based on Phase change materials aUgmented siLicon photonicS
IEEE European Test Symposium 2023, 2023
Ecole Centrale de Lyon, **Laboratoire Interdisciplinaire Carnot de Bourgogne, ***Laboratoire d'Electronique de Technologie de l'Information, ** Argotech a.s., *****Universiteit Gent (Ghent University), ******Fakultät für Physik - Ludwig-Maximilians-Universität [München/Munich], *******Instituto de Engenharia de Sistemas e Computadores, ********Department of Computer Science [Verona], *********Department of Informatics and Telecomunications [Kapodistrian Univ], *********Barcelona Supercomputing Center - Centro Nacional de Supercomputacion, **********UPC - Universitat Politècnica de Catalunya, ***********Albora Technologies Limited [Barcelona], ************Department of Electronics and Telecommunications (Dipartimento di Elettronica e Telecomunicazioni) [Politecnico di Torino] , *************Department of Computer Engineering (Dipartimento di Automatica e Informatica) Politecnico di Torino*
Vinagrero Gutierrez Sergio, Di Natale Giorgio, Vatajelu Elena Ioana
On-Line Method to Limit Unreliability and Bit-Aliasing in RO-PUF
IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS 2023), 2023
Vinagrero Gutierrez Sergio, Inglese Pietro, Di Natale Giorgio, Vatajelu Elena Ioana
Open Automation Framework for Complex Parametric Electrical Simulations
International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2023), 2023
Koroleva Aleksandra*, Khuu Thoai-khanh*/, Ternon Céline*, Burriel Mónica*, Vatajelu Elena Ioana**
Optimization of La2NiO4+δ – based memristive devices for spiking neural networks
International Conference on Memristive Phenomena in Chalcogenides and Beyond
** LMGP Laboratoire des matériaux et du génie physique, ** LTM - Laboratoire des technologies de la microélectronique*
Bain Nathan*, Bain Nathan, Guizzetti Roberto*, Taly Emilien*, Taly Emilien, Oudrhiri Ali*, Paille Bruno*, Urard Pascal*, Pétrot Frédéric
Quantization Modes for Neural Network Inference: ASIC Implementation Trade-offs
International Joint Conference on Neural Networks (IJCNN 2023), 2023
**STMicroelectronics [Crolles]*
Ouldei Tebina Nasr-Eddine, Maingault Laurent*, Zergainoh Nacer-Eddine, Hubert Guillaume, Maistri Paolo**
Ray-Spect: Local Parametric Degradation for Secure Designs
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**Laboratoire d'Electronique de Technologie de l'Information, **ONERA / DPHY - Université de Toulouse [Toulouse]*
Portolan Michele, Keim Martin*, Rearick Jeff, Ehrenberg Heiko*****
Refreshing the JTAG Family
IEEE 41st VLSI Test Symposium (VTS 2023), 2023
Siemens Digital Industries Software, **Advanced Micro Devices [Austin], * GOEPEL electronics LLC*
Ouldei Tebina Nasr-Eddine, Zergainoh Nacer-Eddine, Hubert Guillaume*, Maistri Paolo
Simulation Methodology for Assessing X-Ray Effects on Digital Circuits
IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2023), pp. 1-6, 2023
**ONERA / DPHY - Université de Toulouse [Toulouse]*
Rajappa Anuj Justus*, Reiter Philippe*, Kraemer Sarzi Sartori Tarso, Laurini Luiz Henrique, Fourati Hassen, Mercelis Siegfried***, Hellinckx Peter***, Possamai Bastos Rodrigo**
SMART: Selective MAC zero-optimzation for neural network reliability under radiation
34th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2023), 2023
**Internet Technology and Data Science Lab, **GIPSA-Lab, ***Universiteit Antwerpen = University of Antwerpen [Antwerpen]*
Gava Jonas*, Kraemer Sarzi Sartori Tarso, Hanneman Alex, Garibotti Rafael***, Calazans Ney***, Fourati Hassen******, Possamai Bastos Rodrigo, Reis Ricardo*, Ost Luciano****
Soft Error Assessment of Attitude Estimation Algorithms Running in a Resource-constrained Device under Neutron Radiation
Conference on Radiation Effects on Components and Systems (RADECS 2023), 2023
**UFRGS - Université fédérale du Rio Grande do Sul, **Loughborough University, ***PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ****GIPSA-Lab*
Noizette Luc, Miller Florent*, Colladant Thierry, Helen Youri** , Leveugle Régis**
Soft-SoC robustness evaluation using X-rays: a case study and differences with other beams
36th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS'23)
**NUCLETUDES, ** DGA*
Pavanello Fabio*, Vatajelu Elena Ioana, Bosio Alberto*, Van Vaerenbergh Thomas, Bienstman Peter***, Charbonnier Benoit******, Carpegna Alessio*******, Di Carlo Stefano*******, Savino Alessandro*******
Special Session: Neuromorphic hardware design and reliability from traditional CMOS to emerging technologies
IEEE VLSI Test Symposium (VTS 2023), 2023
**Ecole Centrale de Lyon, **Hewlett Packard Labs [Diegem], ***Universiteit Gent (Ghent University), ****Laboratoire d'Electronique de Technologie de l'Information, *****Department of Computer Engineering (Dipartimento di Automatica e Informatica) Politecnico di Torino*
Vatajelu Elena Ioana
Systems Fault tolerance of memristor-based neural networks : a comparative study between formal and spiking neural networks
36th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2023)
Vatajelu Elena Ioana
Versatilité des technologies de mémoire émergentes et leurs applications
Ecole d'hiver Francophone sur les Technologies de Conception des Systèmes embarqués Hétérogènes (FETCH 2023)

National conferences

El Amraoui Sami, Maistri Paolo, Leveugle Régis
Perspectives pour la Modélisation et la Protection contre les Fautes Electromagnétiques
17ème Colloque National du GDR SoC2, 2023

Theses

Alshaer Ihab
Cross-Layer Fault Analysis for Microprocessor Architectures (CLAM)
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Oct 16, 2023
Benabdenbi Mounir
Contributions to the Test, Fault Tolerance and Approximate Computing of System on a Chip
HDR, Université Grenoble Alpes, spécialité "", Feb 07, 2023
Fiorucci Tiziano
Qualification methodology for ISO26262 certification of automotive SoC systems
These de Doctorat, Université Grenoble Alpes, spécialité "", Jun 06, 2023
Inglese Pietro
Exploration of security threats in In-Memory Computing Paradigms
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Dec 07, 2023
Kraemer Sarzi Sartori Tarso
Mitigation of radiation effects on the attitude estimation processing for autonomous things
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Oct 17, 2023
Martinoli Valentin
Secure Processors with respect to Micro Architectural Attacks
These de Doctorat, Université Grenoble Alpes, spécialité "", Mar 23, 2023
Vatajelu Elena Ioana
Emerging Memories for Dependable Computing
HDR, Université Grenoble Alpes, spécialité "", Jan 24, 2023

CDSI team

Circuits, Devices and System Integration

Circuits, Devices and System Integration (CDSI team)

Keywords: Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

The CDSI team

The team activity covers a broad spectrum of activities from MEMS to systems. Indeed, the team postulates high performances are achieved thanks to disruptive technologies, which are at the frontiers of different fields of applications. Nevertheless, the team is built on two key pillars, sensing and event processing.

Event-based techniques are key for enhancing integrated circuits and systems because they offer a unique opportunity to rethink circuit design, which does not take well into account most of the non-functional specifications, such as power, security, safety or electromagnetic emissions. This paves the way to ultra-low power systems, enhanced secured systems, proven design methods but also near sensor computing.

Sensing is the second key. Taking advantage of smart sensors and actuators requires globally envisioning systems, favors a smart sensing approach limiting useless information and pushes new experiments and usage.

Event-based technologies

Event-based approach

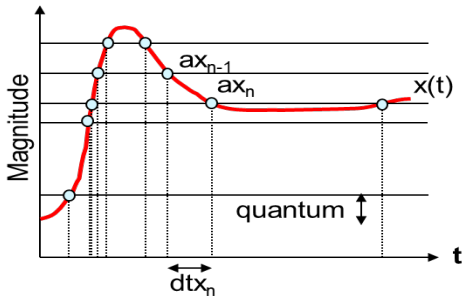


Figure 1: Level Crossing Sampling Scheme

Event-based is a quite simple idea, which suggests operating a circuit only when needed. Nevertheless, this is countercurrent when looking the semiconductor industry. Indeed, everything is clocked synchronized, analog-to-digital conversion is clock-sampled. In practice, clock is used as an event generator giving the pace of the circuits generating a large number of events and producing useless activity, computation, storage or communication. The event-based approach tends generating sparse events related to natural events such as a pressure variation or a heartbeat. Therefore, the team works on alternative analog-to-digital converters able to drastically reduce the number of samples and, hence, limit useless activity and energy consumption (see Figure 1).

Asynchronous Circuits

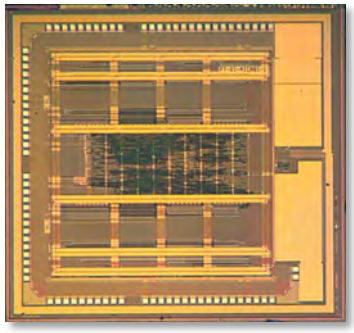


Figure 2: Asynchronous microcontroller with on-chip NFC antenna

Since more than 20 years, the team works on new synchronization paradigms, which are not based on a clock but on handshake signals. Such techniques reveal many opportunities for rethinking the circuit design process and opening new degrees of freedom. The first expected advantage is probably the reusability of existing blocks that can simply be connected together, making the assembly of a system a kind of LEGO build. Indeed, the timing assumptions are locally fulfilled guarantying an easy block association. Moreover, many other advantages are of interest such a lower power consumption, a better robustness, lower electromagnetic emissions, safer and more secured circuits…

Targeting Ultra-low power

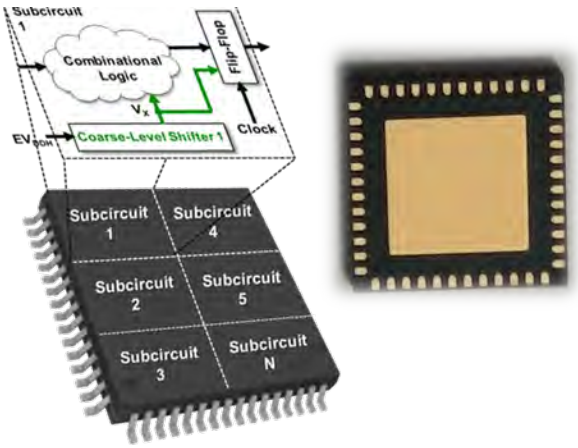


Figure 3: FDSOI 28 nm asynchronous testchip managing several local fine-grain body-bias domains

Today power is a main concern for chip design. The event-based strategy is probably the best technique for reducing power at least by one order of magnitude. Indeed, a sparse sampling scheme produces much less data, which are non-uniformly spaced in time. Each datum is no more than an event that can be sporadically processed by asynchronous circuits. Indeed, these latter are data-driven and consume energy only when computing. Moreover, the intrinsic robustness of asynchronous circuits favors their use at low-voltage, near- or subthreshold. Indeed, lowering the voltage is an efficient and well-known strategy to save power. Its main drawback is the decrease of the circuit speed. The Fully Depleted Silicon on Insulator (FDSOI) technology allows mitigating this speed drop thanks to forward body biasing. As asynchronous circuits use communication protocols indicating circuit activity, the handshake signals are perfectly suited for controlling local body-bias domains ensuring low-energy expenses for body biasing and compensating the speed loss.

All these mechanisms can be implemented for mitigating the energy and helping the adoption of energy harvesting in batteryless systems.

Security

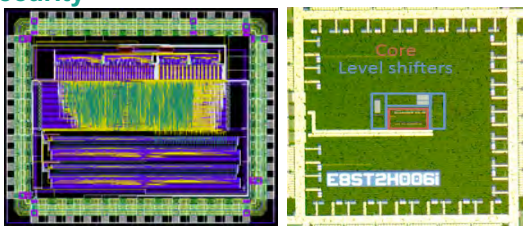


Figure 4: TRNG with entropy monitoring (left) and Ultra-low power TRNG (right) (30 pJ/bit@0.3 V)

Another opportunity offered by the asynchronous circuits is its ability to make more difficult the side-channel analysis and attacks in trusted devices. Indeed, the absence of clock synchronization, the specific encoding and the computation time control makes them of interest for developing trusted platforms. They also offer disruptive strategies for true random number generators (TRNG) and physically unclonable functions (PUF) while consuming a few energy.

Design flow and proven technology

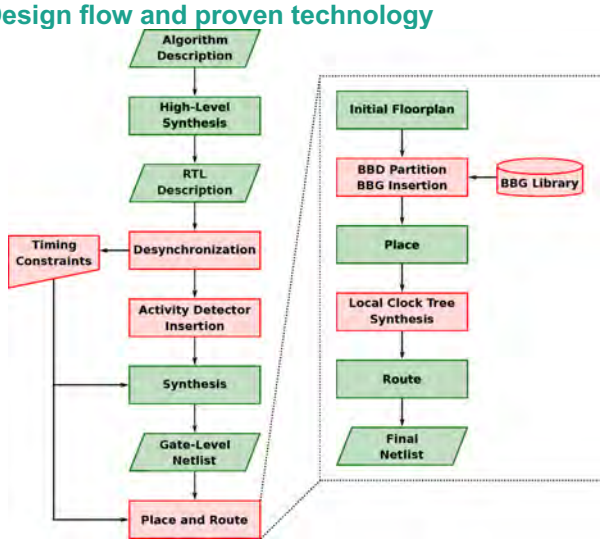


Figure 5: Asynchronous circuit HLS to layout design flow

Developing non-conventionally synchronized circuits is not obvious because of the lack of dedicated CAD tools. Although the first good idea is to implement such tools, there is some overcoming hurdles. The first one is clearly the quasi-absence of trained people with the know-how for designing efficient and performant asynchronous circuits. The second is the impact, the reliability and the engineer confidence into a new design flow. Therefore, for more than 10 years, the team is developing dedicated flows based on the standard commercial tools with a particular emphasis on a proven by construction synthesis.

Near-sensor computing

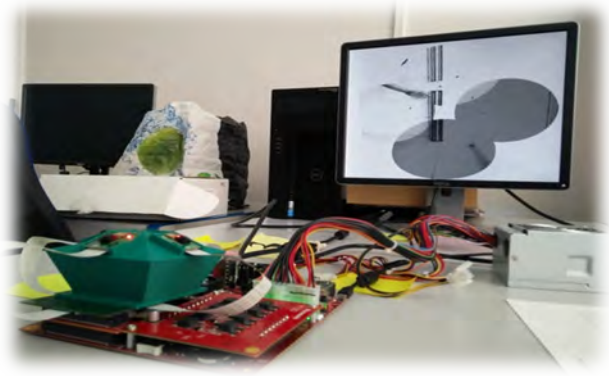


Figure 6: Panoptic camera for laparoscopy

With the dissemination of autonomous and connected objects, it appeared the need to limit the amount of transmitted raw data, especially in RF communications where the problem is more acute. Therefore, developing tiny sensor platforms able to preprocessed data before transmitting information is becoming a challenging topic. Indeed, enhancing the sensing techniques and immediately processing the raw data with a reduced energy budget is the grail in near-sensor computing. The team developed several strategies based on event-based techniques or improving the adequacy between the algorithms and the circuit architecture. This is typically the case for many image-processing applications such as panoptic camera for laparoscopy.

Smart-sensing technologies

In-sensor computing

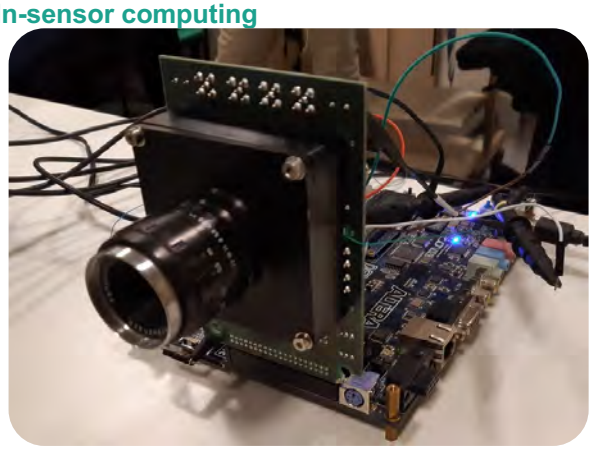


Figure 7: Event-based camera

As previously stated, smart sensing is a key for envisioning systems with advanced features such as detection, pattern recognition or low-power. Beyond the state of art of sensor technology, the enhancement can be obtained thanks to new architectures or in-sensor computing. One of the approach concerns image sensors, which usually permanently read the image. This is a waste of energy and time for acquiring an image. In order to reduce these issues, the image capture can be performed thanks to an event-based readout, which only samples a pixel when this latter fires. In this case, the firing pixel indicates that its value has to be changed in the image memory. Such a strategy is applied for reducing the power consumption and increasing the speed sensor thanks to a dedicated readout canceling the spatial and temporal redundancies.

Measuring time

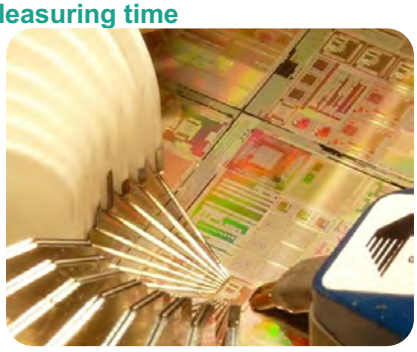


Figure 8: Asynchronous multiphase oscillator (under test) used in TDC

Using an event-based sensing implies a duality with the standard Nyquist analog-to-digital conversion because the quantization is no more applied to the amplitude but to the time elapsed between two successive events. Therefore, designing advanced Time-to-Digital Converters (TDC) is an important block for many sensors or even for some security primitives such as TRNG or PUF.

Harvesting for ultra-low power systems

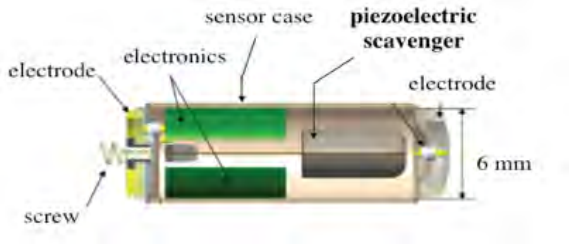


Figure 9: Piezoelectric scavenger for automous pacemaker (Vibration: 10 - 25 Hz, Size: L = 30 mm, Ø= 6 mm, energy: 5 - 10 µJ)

With the advent of the Internet of Things, the system requirements in term of power are extremely demanding, especially for smart sensing and actuating. A typical highlight targets the medical implant such as pacemakers. Indeed, they need today a battery, which lasts less than 10 years. Then the pacemaker has to be explanted because this is not a rechargeable battery. Wireless power transfer may overcome this issue via acoustic wave propagation, using piezoelectric transducers to generate and harvest acoustic power. The MEMS are particularly well-suited for this purpose, for small autonomous and smart objects.

Security (chaotic approach)

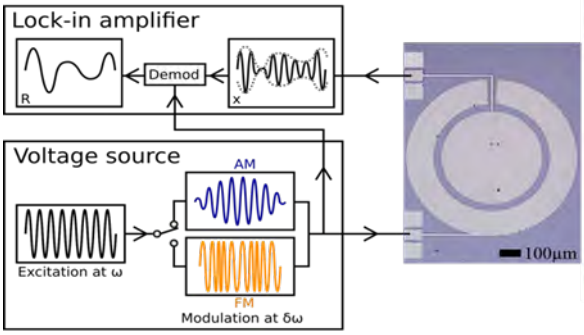


Figure 10: Experimental Setup and modulations in the Duffing's regime. The MEMS (photography) is driven by a voltage modulated voltage source (AM or FM). The Lock-in-Amplifier extracts the displacement magnitude of the MEMS to observe the chaos.

MEMS have opened the doors to intense researches covering most of the technology fields. It is not surprising that they can be of interest for security. They offer original solutions for designing chaotic generators using the dynamical bistability of a Duffing's microresonator. This approach is particularly relevant for generating true random numbers because MEMS already exist on various systems such as mobile phones and are useable for extracting chaos. Moreover, this could be employed for securing communications in various transduction schemes. In acoustics, chaotic MEMS can be used as ultrasonic jammers. In optics, synchronization of chaotic MEMS takes benefit from both high complexity yet controllable chaos and large data rate for secured telecom applications.

New Sensors and actuators

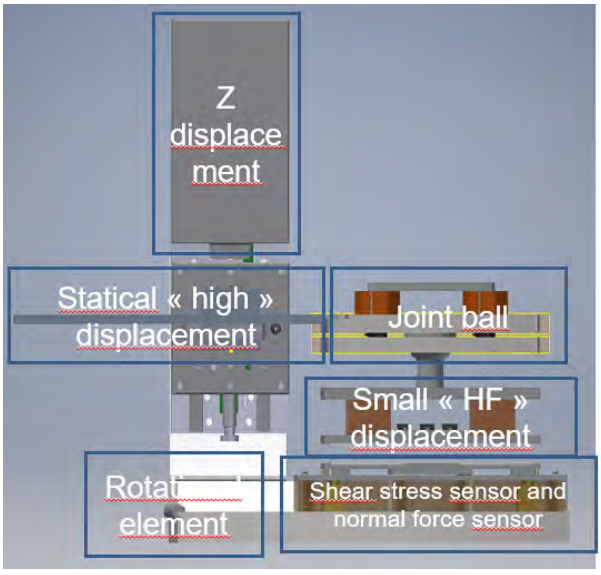


Figure 11: The 3D representation of the new piezo rheometer with description of its functions

The team is also developing a new kind of piezo-based sensors and actuators for applications in rheometry, earphones, or microphones.

The piezorheometer permits to obtain high frequency strain compared to standard equipment. This rheometer combines piezoelectric actuator, slaved by accelerometers to give accurate strain to a media, with piezolectrics ceramics which are the sensors to extract the stress given to this media. With a precise extraction of the imposed strain synchronized with the stress, the shear modulus is calculated. Innovation comes from the slaving of the actuators. Moreover, this kind of rheometer only applied small strain so a linear piezoelectric actuator has been implemented to evaluate the shear modulus from very low to very high strain. Finally, this rheometer will be as precise as classical rheometer but less expensive and with a smaller volume.

Figure 12: ActivMotion earphones concept

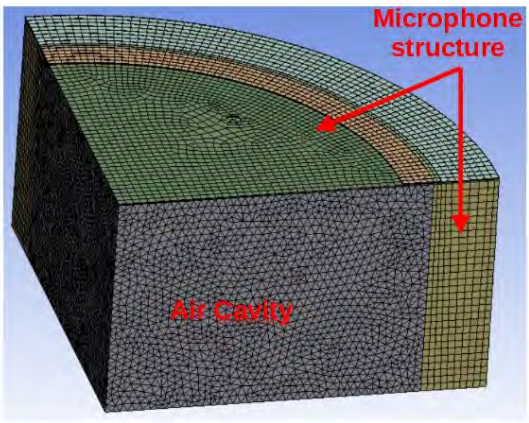


Figure 13: Finite element model for MEMS piezoelectric microphone.

Piezoelectric actuators can also be implemented in earphones to replace the widely used electrodynamic transducers. They offer new possibilities in term of design and integration, which ActivMotion is pushing. In their concept, the user's ears become the emitting surface which allows for new earphone ergonomics. High power density piezoelectric actuators working at low voltages are ideal for this use case. With the resonance control of the actuator, a linear performance over the audible frequency range is obtained.

CDSI team is also part of the project MAMBO aiming at reducing airplanes noises. The knowledge of noise sources in airplanes is crucial and requires specific microphones characteristics to measure them (high pressure, wide dynamic and frequency range, low SNR,…). In this context, the team work is focused on the conception of a MEMS piezoelectric microphone using finite element method and lumped element equivalent circuit to predict the microphone performances for aeroacoustic measurements.

Recent highlights

March 17, 2023: Best Paper Award at SIGNAL 2023

Congratulations to Florent CROZET and Stéphane MANCINI.

Academic and research members

Skandar BASROUR

Position
Professor at UGA – Polytech school

Responsibilities
Researcher in CDSI team

Martial DEFOORT

Position
Researcher at CNRS

Responsibilities
Researcher in CDSI team

Sylvain ENGELS

Position
Associate Professor PAST at Grenoble INP - Phelma school

Responsibilities
Researcher in CDSI team

Laurent FESQUET

Position
Associate Professor at Grenoble INP - Phelma school

Responsibilities
Deputy Director of TIMA Lab. since 01/2021
Leader of CDSI team
Researcher in CDSI team

Stéphane MANCINI

Position
Associate Professor at Grenoble INP - Ensimag school

Responsibilities
Researcher in CDSI team

Katell MORIN-ALLORY

Position
Associate Professor at Grenoble INP - Phelma school

Responsibilities
Researcher in CDSI team

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
GRENOBLE INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AKBARI Masoud
Title of thesis: **Open air fabrication of oxide-based cantilever gas sensors**
Completed on: **September 22, 2023**
Previous degrees:

2. AKRARAI Mohamed
Title of thesis: **Smart Event-Based Image Sensor for wake-up applications**
Completed on: **June 19, 2023**
Previous degrees: Engineer - INPT (Institut National des Postes et Télécommunications) - Rabat, Morocco (2018)

3. CROZET Florent
Title of thesis: **Extreme Learning Machine for embedded neural networks**
Expected date of defense: **2024**
Previous degrees: Master - Université de Clermont-Ferrand-I – Clermont-Ferrand, France (2019)

4. DE GIOVANNI Adrien
Title of thesis: **Design of a piezoelectric micro-actuator with mechanical amplification for extra-auricular earphones**
Expected date of defense: **2024**
Previous degrees: Engineer – ENSAM (Ecole Nationale Supérieure d'Arts et Métiers) – Paris, France (2020)

5. GODARD Adrien
Title of thesis: **Development of an ultra-low-power asynchronous embedded RISC processor**
Expected date of defense: **2026**
Previous degrees: Engineer – Grenoble INP – Phelma – Grenoble, France (2023)

6. KALEL Diana
Title of thesis: **Development of an advanced flow of structural, formal and semi-formal verification of asynchronous paths using appropriate formal verification methods and tools, for high-performance integrated processor-based subsystems**
Expected date of defense: **2024**
Previous degrees: Master – Ain Shams University – Cairo, Egypt (2019)

7. LESAGE Xavier
Title of thesis: **Smart batteryless InfraRed Image Sensor**
Expected date of defense: **2025**
Previous degrees: Master of Science – Karlsruher Institut fuer Technologie (KIT) - Karlsruhe, Germany (2021)

8. LIM Olivier
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2023**
Previous degrees: Master UGA (Université Grenoble Alpes) (2020)

9. MERIO Cristiano
Title of thesis: **Using artificial intelligence for near field communication and low-energy signal demodulation**
Expected date of defense: **2025**
Previous degrees: Engineer – Grenoble INP (2022)

10. MOUSSA Hasan
Title of thesis: **Event-based Smart RF Architectures**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA (Université Grenoble Alpes) (2021)

11. NAIMI Ali
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2025**
Previous degrees: Engineer - INPT (Institut National des Postes et Télécommunications) - Rabat, Morocco (2022)

12. TACYNIAK Pierre
Title of thesis: **Study of a secured wireless acoustic power transfer for medical implants**
Expected date of defense: **2024**
Previous degrees: Master ENSAM (Ecole Nationale Supérieure d'Arts et Métiers) – Paris, France (2021)

13. THAJTE Azzadine
Title of thesis: **Built-in Asynchronous Detection for Hardware Cryptography (BAD4HaCr)**
Expected date of defense: **2026**
Previous degrees: Master – Université de Bretagne Occidentale – Brest/Rennes, France (2022)

14. TRAN Rosalie
Title of thesis: **Smart Event-Based Image Processing**
Thesis stopped on July 13, 2023
Previous degrees: Engineer – Grenoble INP – Phelma – Grenoble, France (2021)

15. ZUCCALA Damiano
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2025**
Previous degrees: Master in Physics - Università degli Studi dell'Insubria – Como, Italy (2021)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. BOCCALERO	Gregorio	ITALY	11 months
2. ESTEVES	Josue	FRANCE	2 months
3. PASSY KENGANI	Marco Erickson	CONGO	3,5 months

Visitors

Name	Forename	Country	Duration
1. FUMAT	Samuel		5 months
2. MANQUAT	Hugo	FRANCE	3 months

Trainees

NAME	FORENAME	COUNTRY	DURATION
1. BOUCHARD	Elliot	FRANCE	1,5 month
2. GONSALVES SANTOS	Jéssica	FRANCE	1 month
3. KULAGIN	Vasilii	FRANCE	1,5 month
4. NEAIMEH	Fouad		2,5 months
5. SAUER DE ARAUJO	Luca	BRAZIL	3 months
6. WELZEL	Fernando	FRANCE	4 months
7. YAHMADI	Mohamed		2,5 months

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2023.

ANR

PiezoKnee (2023 - 2026)
Scientific manager: Skandar BASROUR

SMART IMAGER (2022 - 2025)
Program: IRT
Scientific manager: Laurent FESQUET

CIFRE

Thèse Jérémy BELOT (2020 – 2023)
Title: Towards compact, low energy and with adjustable accuracy Bayesian computers
Thesis director: Laurent FESQUET
Industrial partner: Hawai.Tech

Thèse Florent CROZET (2022 – 2025)
Title: Extreme Learning Machine for embedded neural networks
Thesis director: Stéphane MANCINI
Industrial partner: STMicroelectronics

Thèse Adrien GODARD (2023 - 2026)
Title: Development of an ultra-low-power asynchronous embedded RISC processor
Thesis director: Laurent FESQUET
Industrial partner: STMicroelectronics

Thèse Diana KALEL (2021 - 2024)
Title: Development of an advanced flow of structural, formal and semi-formal verification of asynchronous paths using appropriate formal verification methods and tools, for high-performance integrated processor-based subsystems
Thesis director: Katell MORIN-ALLORY
Industrial partner: STMicroelectronics

Thèse Cristiano MERIO (2022 - 2025)
Title: Using artificial intelligence for near field communication and low-energy signal demodulation
Thesis director: Laurent FESQUET
Industrial partner: STMicroelectronics

Thèse Damiano ZUCCALA (2022 - 2024)
Title: Real-Time unconventional adaptive cameras for multimodal acquisition
Thesis director: Katell MORIN-ALLORY
Industrial partner: STMicroelectronics

ÉTAT

EAUDI (2021 – 2025)
Title: Ecouteur extra AUriculaire Dissimulé
Scientific manager: Skandar BASROUR

MAMBO (2021 – 2027)
Title: Méthodes Avancées pour la Modélisation du Bruit moteur et aviOn
Scientific manager: Libor RUFER

MucoPiezoRheo (2020 – 2023)
Scientific manager: Skandar BASROUR

REGION

FAIR (2018 – 2023)
Program: Pack Ambition Recherche
Title: Conception et fabrication par Fabrication Additive de produits Intelligents
Scientific manager: Skandar BASROUR

SATT

EMIR (2021 – 2023)
Title: Event-based Microbolometer for IR sensors and ultra low power applications
Scientific manager: Laurent FESQUET

TUTELLE

IRGA SETH (2023 – 2024)
Scientific manager: Martial DEFOORT

Thèse APACHE (2022 - 2025)
Program: IRGA
Thesis director: Katell MORIN-ALLORY

Organization and participation of international conferences, workshops, forums

ASYNC 2023 - 28th IEEE International Symposium on Asynchronous Circuits and Systems
July 16-19, 2023 - Beijing, CHINA
Rank: A+
program chair: FESQUET Laurent

CENICS 2023 - 16th International Conference on Advances in Circuits, Electronics and Micro-electronics
September 25-29, 2023 – Porto, PORTUGAL
Rank: NC
technical program committee: FESQUET Laurent

DATE 2023 - Design, Automation & Test in Europe (DATE 2023)
April 17-19, 2023 - Antwerp, BELGIUM
Rank: A+
topic chair: MORIN-ALLORY Katell

JNRSE 2023 - Journées Nationales sur la Récupération et le Stockage de l'Energie
June 12-13, 2023 - Paris, FRANCE
Rank: NC
organization committee: BASROUR Skandar
program committee: BASROUR Skandar

NMN 2023 - 1st Nonlinear Micro/Nanosystems symposium
May 30 & 31, 2023 - Grenoble, FRANCE
Rank: NC
general chair: DEFOORT Martial

SIGNAL 2023 – 8th International Conference on Advances in Signal, Image and Video
March 13-17, 2023 – Barcelona, SPAIN
Rank: NC
technical program committee: FESQUET Laurent

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
Phelma school PHysique – ELectronique - MAtériaux				
Manager of SEI branch	MORIN-ALLORY Katell	01/09/2017		
Graduate school@UGA				
Coordinator of SUMMIT program	BASROUR Skandar	01/09/2020		
Research structures				
CIME Nanotech Centre Interuniversitaire de MicroElectronique et Nanotechnologies				
CIME platform relationship	MORIN-ALLORY Katell	01/09/2022		
Deputy Director	FESQUET Laurent	01/09/2017		
Manager of Communicating objects platform	MANCINI Stéphane	01/09/2017		
FMNT Fédération des Micro et Nanotechnologies				
Deputy Director	BASROUR Skandar	01/01/2021		
Parent institutions				
Grenoble INP Grenoble Institute of Technology				
Board of Directors member (elected member)	MANCINI Stéphane	12/12/2019	01/01/2024	Strategy, jobs, promotion files, invited professors, teaching assistants

Scientific production

International journals

Nastro Alessandro*, Baù Marco*, Ferrari Marco*, Rufer Libor, Basrour Skandar, Ferrari Vittorio***
Cell Alignment in Aqueous Solution Employing a Flexural Plate Wave Piezoelectric MEMS Transducer
IEEE Access, Volume: Open access, 2023
**Department of Information Engineering [University of Brescia], **--*

Gassab Marwa*, Papanastasiou Dorina, Sylvestre Alain***, Bellet Daniel**, Dridi Cherif*, Basrour Skandar**
Dielectric Study of Cost-Effective, Eco-Friendly PVA-Glycerol Matrices with AgNW Electrodes for Transparent Flexible Humidity Sensors
Advanced Materials Interfaces, Volume: 10, 2023
**NANOMISENE RD Laboratory [Sousse], **Laboratoire des Matériaux et du Génie Physique, ***Laboratoire de Génie Electrique de Grenoble*

Lesage Xavier*, Lesage Xavier, Tran Rosalie, Mancini Stéphane, Fesquet Laurent
Velocity and Color Estimation Using Event-Based Clustering
Sensors, Volume: 23, 2023
**ORIOMA SAS*

Patents

Alshakoush Ali, Bourdel Sylvain, Podevin Florence, Lauga-Larroze Estelle, Fesquet Laurent
Mélangeur à N Chemins à réjection d'harmoniques - Brevet N° FR3125934A1, delivered on Feb 03, 2023

Lauwers Thomas*, Basrour Skandar, Coutard Jean-Guillaume*, Glière Alain*, Laffont Guillaume*
Optical device for detecting an acoustic wave
Brevet N° United States Patent Application 2023/0037289 A1, delivered on Feb 09, 2023
**Laboratoire d'Electronique de Technologie de l'Information*

Defoort Martial, Basrour Skandar, Fesquet Laurent
Chaotic physical true random number generator and associated method - Brevet N° 20230266945, delivered on Aug 24, 2023

Invited conferences talks

Fesquet Laurent
Event-based Image Sensing and Processing for Low-Power Applications
IEEE Vision workshop, Sensors and smart (AI) processing, 2023

Fesquet Laurent
Sensing and Processing Image at Low-Power
FMNT/Summit Workshop, Low-power for a sustainable electronic, 2023

International conferences

Kalel Diana, Brignone Jean-Christophe*, Fesquet Laurent, Morin-Allory Katell
A Generic CDC Modeling for Data Stability Verification
IEEE 30th International Conference on Electronics, Circuits and Systems (ICECS 2023), 2023
**STMicroelectronics [Grenoble]*

Esteves Josue, Rufer Libor*, Ekeom Didace, Defoort Martial, Basrour Skandar**
Approaches to piezoelectric micromachined microphone design: comparative study
Forum Acusticum 2023 (10th Convention of the European Acoustics Association), 2023
**--, **Microsonics*

Merio Cristiano, Lesage Xavier, Naimi Ali, Engels Sylvain, Morin-Allory Katell, Fesquet Laurent
Data-driven Pruning for Bundled-data Circuits
28th International Symposium on Asynchronous Circuits and Systems (ASYNC 2023, 2023

Nastro Alessandro*, Bertelli Stefano*, Ferrari Marco*, Rufer Libor, Basrour Skandar, Ferrari Vittorio***
Flexural Plate Wave Piezoelectric MEMS Pressure Sensor
EUROSENSORS 2024, pp. 97(1), 185, 2023
**Department of Information Engineering [University of Brescia], **--*

Nastro Alessandro*, Bertelli Stefano*, Ferrari Marco*, Rufer Libor, Basrour Skandar, Ferrari Vittorio***
Flexural Plate Wave Piezoelectric MEMS Pressure Sensor
EUROSENSORS 2024, pp. 97(1), 185, 2023
**Department of Information Engineering [University of Brescia], **--*

Zuccalà Damiano, Daveau Jean-Marc*, Roche Philippe*, Morin-Allory Katell
Formal Temporal Characterization of Register Vulnerability in Digital Circuits
IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2023)
**ST-CROLLES - STMicroelectronics*

Fesquet Laurent, Tran Rosalie, Lesage Xavier, Akrarai Mohamed, Mancini Stéphane, Sicard Gilles*
Low-Throughput Event-Based Image Sensors and Processing
Design, Automation & Test in Europe Conference & Exhibition (DATE 2023), 2023
**Laboratoire d'Electronique de Technologie de l'Information*

Moussa Hasan, Gonsalves Santos Jéssica, Lauga-Larroze Estelle, Ibrahim Sana, Podevin Florence, Bourdel Sylvain, Fesquet Laurent
Making Digital N-Path Mixers
38th Conference on Design of Circuits and Integrated Systems (DCIS 2023), 2023

Merio Cristiano, Lesage Xavier, Naimi Ali, Engels Sylvain, Morin-Allory Katell, Fesquet Laurent
Method for Data-Driven Pruning in Micropipeline Circuits
31st IFIP/IEEE Conference on Very Large Scale Integration (VLSI-SoC 2023), 2023

Lim Olivier*, Lim Olivier, Mancini Stéphane, Dalla Mura Mauro*, Dalla Mura Mauro**
Potential of an Embedded Hyperspectral Compressive Imaging System for Remote Sensing Applications
2023 IEEE International Geoscience and Remote Sensing Symposium (IGARSS 2023), pp. 4238-4241, 2023
**GIPSA-Lab, **Institut Universitaire de France*

Crozet Florent*, Mancini Stéphane, Nicolas Marina*
Pseudo-Randomisation Partielle et Quantification pour la compression des réseaux de neurones convolutifs
GRETSI 2023
**ST-GRENOBLE - STMicroelectronics [Grenoble]*
Damiano Zuccalà Damiano, Daveau Jean-Marc*, Roche Philippe*, Morin-Allory Katell
Real-Time Switched Capacitor Based Power Side-Channel Attack Detection
VLSI-SOC 2023
**ST-CROLLES - STMicroelectronics [Crolles]*

National conferences

Fesquet Laurent, Lesage Xavier, Merio Cristiano, Naimi Ali, Engels Sylvain
Développer la compétence recherche en école d'ingénieurs - 17èmes journées pédagogiques du CNFM (JPCNFM 2023), 2023
Fesquet Laurent
Gestion du flot de conception sur une plateforme CAO - 17èmes journées pédagogiques du CNFM (JPCNFM 2023), 2023
Lim Olivier*, Mancini Stéphane, Dalla Mura Mauro*/**
Estimation de performances d'un imageur hyperspectral compressif sur système embarqué pour des applications de télédétection
GRETSI 2023 - XXIXème Colloque Francophone de Traitement du Signal et des Images
**GIPSA-SIGMAPHY, **IUF - Institut universitaire de France*

Theses

Akrarai Mohamed
Event-based Image Sensor for low-power
These de Doctorat, Université Grenoble Alpes, spécialité "", Jun 19, 2023

RMS team

Reliable RF and Mixed-signal Systems

Reliable RF and Mixed-signal Systems (RMS team)

Description

The Reliable RF and Mixed-signal Systems group (**R**MS) is focused on the design, test and control of analog/mixed-signal/RF/mm-Wave integrated circuits and systems. 2021 has been a transition year for the **R**MS team, in preparation for the integration of the researchers in RFIC-Lab within the team in 2022. In this regard, the research axes of the team have evolved to better describe the wider scope of the team activities after the integration. Our research can be declined into the following four main axes:

Design of AMS-RF integrated circuits and systems

Novel AMS-RF design solutions are required in a wide variety of state-of-the-art applications, including communications, computing, imaging, etc. In this regard, the **R**MS group explores the multiple challenges of state-of-the-art AMS-RF current and emerging design paradigms, especially focusing on low-power and/or low-voltage applications. Our research includes the development of low-power mixed-signal and RF design techniques, state-of-the-art area-efficient high-resolution and ultra-low power data converters for imaging applications, integrated control electronics for quantum computing, and advanced RF design techniques for 5G and beyond-5G applications.

Integration and miniaturization of RF-mmW circuits

In this research axe our activities are focused on exploring novel integration solutions, including “More Moore” approaches, such as taking advantage of optimized Back-End-Of-Line metal stacks for integrating novel 3D passive structures, and “More-Than-Moore” approaches, where heterogeneous 2.5D and 3D solutions using mmW interposers.

Design for test and reliability of AMS-RF/mmW circuits and systems

Testing AMS-RF/mmW functions in a complex integrated system represent nowadays a major challenge for the IC industry. Our research in this area is focused on two main research lines: a) the development of AMS-RF-mmW state-of-the-art on-chip test instruments for Built-In Self-Test (BIST) applications and dedicated DfT techniques; and b) the development of novel indirect test methodologies based on the applications of advanced machine learning algorithms.

Control, optimization and self-healing of AMS/RF and mm-Wave circuits

In parallel with the test challenge, performance calibration and tuning are of key interest in the IC industry. Performance calibration in the production line enables a yield enhancement, while providing tuning capabilities during the lifetime of the circuit opens the door to self-healing applications and enhanced reliability. In this line, we develop optimized, minimally intrusive tuning knobs for performance calibration, together with novel performance control algorithms based on machine learning models.

Research milestones

- Non-intrusive mm-wave test: we have outlined and experimentally demonstrated a machine learning-based non-intrusive test methodology for mm-Wave circuits.
- Advanced modeling of mm-wave couplers for design enhancement: design-oriented model considering frequency-dependent electrical losses.
- Inversion-based design methodology for low-power LNA design.
- Design-oriented modeling of short-channel MOS transistors: based on the ACM model, we have developed a 7-parameter MOS transistor DC model including the main short-channel effects in advanced nanometric technologies.
- Quantum dot test structures have been fabricated in FD-SOI technology and the characteristic Coulomb blockade diagrams have been successfully measured.
- Ultra low-power and area-efficient high resolution analog to digital converter
- Low noise read-out for integrated quantum random number CMOS sensors
- First-ever OBT technique for mm-wave circuits: we have demonstrated the potential of Oscillation-Based Test techniques for the test and calibration of phased arrays.
- Development of Embedded Test Instruments for the static and dynamic test of state-of-the-art ADCs and for the characterization of clock jitter.
- Development of machine learning-based image quality evaluation and correction techniques.
- Low-cost controller synthesis: we have developed a software platform for automatic generation of logic control codes for a wide variety of low-cost microcontroller targets.
- Scheduling control for lifetime optimization in Wireless Sensor Nodes technologies: we have proposed a novel solution to the Maximum Lifetime Coverage Problem (MLCP) that takes into account the non-zero energy of nodes in sleep mode.

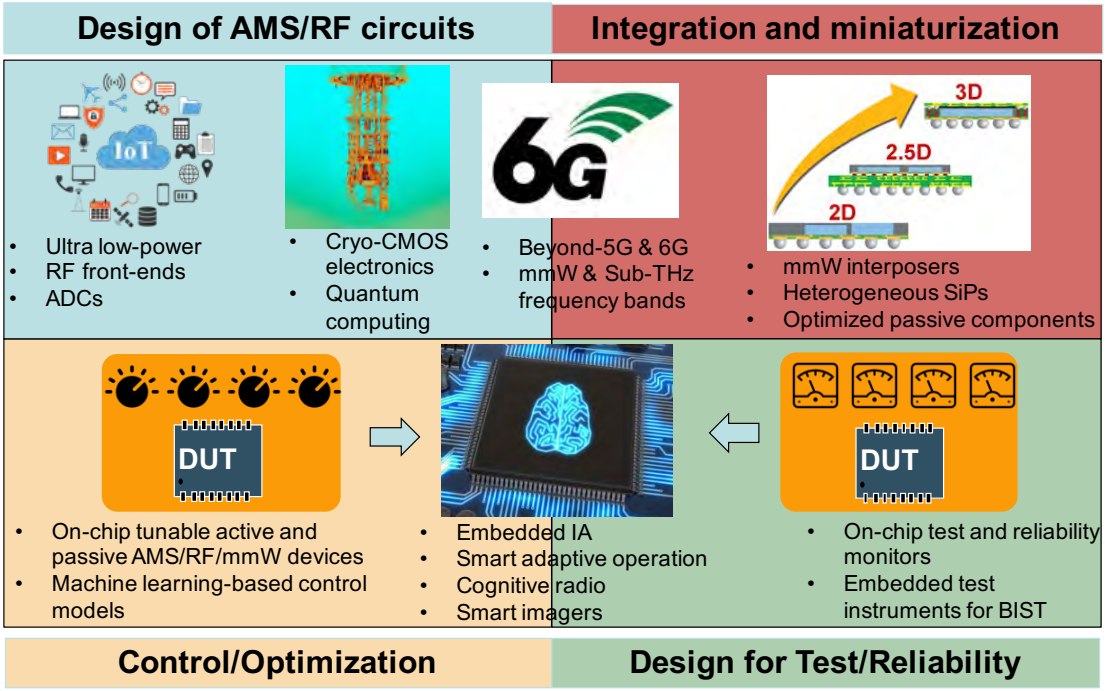


Figure 1: **R**MS research activities at a glance

Recent highlights

International Cooperation

GISS project (Ghana Instrumentation Sensors and Systems)
Scientific Manager: Daniel DZAHINI
Partners: Ashesi University
City: Berekuso
Country: GHANA
Start the: May 17, 2022 until May 17, 2024

April 3, 2023: Joint IEEE & SoC2 Day On Inversion Coefficient and its Applications

Chairman: Sylvain BOURDEL
https://tima.univ-grenoble-alpes.fr/news/joint-ieee-soc2-day-inversion-coefficient-and-its-applications

June 28, 2023: Best Paper Award at NEWCAS 2023

Congratulations to Mohamed Khalil BOUCHOUCHA, Manuel BARRAGAN and Sylvain BOURDEL for receiving the NEWCAS 2023 Best Paper Award for their work entitled:

"A 5-DC-Parameter MOSFET Model for Circuit Simulation in QucsStudio and Spectre"

September 18, 2023: Seminar by Prof. Sugako Otani (Renesas Electronics, Tokyo) & Prof. Makoto Ikeda (University of Tokyo)

https://tima.univ-grenoble-alpes.fr/news/seminar-prof-sugako-otani-renesas-electronics-tokyo-prof-makoto-ikeda-university-tokyo

November 10, 2023: Scientific Day: Embedded Control Strategies for Energy provision Management and Enhancement of Consumption

https://tima.univ-grenoble-alpes.fr/news/scientific-day-embedded-control-strategies-energy-provision-management-and-enhancement-consumption

December 11, 2023: Seminar by Prof. Jai Narayan Tripathi (Assistant Professor at Indian Institute of Technology Jodhpur, Rajasthan, India)

https://tima.univ-grenoble-alpes.fr/news/seminar-prof-jai-narayan-tripathi-assistant-professor-indian-institute-technology-jodhpur-rajasthan

Academic and research members

Jean-Daniel ARNOULD

Position
Associate Professor at Grenoble INP - Phelma school

Responsibilities
Researcher in RMS team

Manuel BARRAGAN

Position
Researcher at CNRS

Responsibilities
Leader of RMS team
Researcher in RMS team

Sylvain BOURDEL

Position
Full professor at Grenoble INP – Phelma school

Responsibilities
Researcher in RMS team

Daniel DZAHINI

Position
Research engineer at CNRS

Responsibilities
Researcher in RMS team

Philippe FERRARI

Position
Full professor at UGA – IUT1

Responsibilities
Researcher in RMS team

Estelle LAUGA-LARROZE

Position
Associate professor at UGA – IUT1

Responsibilities
Researcher in RMS team

Salvador MIR

Position
Research Director at CNRS

Responsibilities
Researcher in RMS team

Emmanuel PISTONO

Position
Associate professor at UGA – IUT1

Responsibilities
Researcher in RMS team

Florence PODEVIN

Position
Full professor at Grenoble INP – Phelma school

Responsibilities
Deputy director (since 09/06/2023)
Researcher in RMS team

Emmanuel SIMEU

Position
Full professor at UGA – Polytech school

Responsibilities
Researcher in RMS team

CNRS (French National Center for Scientific Research)
Grenoble INP (Grenoble Institute of Technology)
PHELMA school (Physique-Electronique-Matériaux)
POLYTECH school (École Polytechnique de l'Université Grenoble Alpes)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AGOUZOUL Abdelali
Title of thesis: **Synthesis of optimized control system of alternative energies for the building**
Expected date of defence: **2024**
Previous degrees: Engineer – EMSI (École Marocaine des Sciences de l'Ingénieur) - Casablanca, Maroc (2021)

2. ALSUKOUR Mohammad
Title of thesis: **Synthesis High-density 3D integration of electronic components by hybrid bonding with MOS transistors for millimeter-scale applications**
Expected date of defence: **2026**
Previous degrees: Engineer – University of Amman, Jordan (2022)

3. BELKHADRA Oumayma
Title of thesis: **Self-tuning power amplifier in advanced CMOS technology for automotive radar**
Expected date of defence: **2024**
Previous degrees: Engineer – Enseirb-Matmeca - Bordeaux, France (2020)

4. BENDJEDDOU Imadeddine
Title of thesis: **Energy-efficient wake-up radio system based on spintronic devices**
Expected date of defense: **2024**
Previous degrees: Master – UGA (Université Grenoble Alpes) – France (2019)

5. BONTEMS William Illich
Title of thesis: **Design of a 15-bit analog to digital converter for ultra low power applications**
Expected date of defense: **2024**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

6. BOUCHOUCHA Mohamed Khalil
Title of thesis: **Design methodology based on the inversion coefficient for RF and mmW circuits optimization using 28 nm FDSOI technology**
Expected date of defense: **2024**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

7. BOUKHEZAR Larbi
Title of thesis: **Agile front-end topology at millimetre frequencies using in situ calibration solutions. Application to the design of D-band phase shifters, Comparison of active and passive approaches**
Expected date of defence: **2026**
Previous degrees: Master Université Grenoble Alpes, France (2022)

8. BOUZAR Tarek
Title of thesis: **Contribution to the design of miniature high frequency probes for precision microwave measurements on silicon wafers**
Expected date of defense: **2025**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2022)

9. BRITTON OROZCO Giovani Crasby
Title of thesis: **Design of an FD-SOI read / control circuit dedicated to the field of quantum computing under Cryogenic conditions**
Expected date of defense: **2024**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2020)

10. BUREAU Benjamin
Title of thesis: **Investigation of single spin qubits fabricated with industrial processes as a resource for quantum application with hybrid quantum circuits**
Expected date of defence: **2026**
Previous degrees: Engineer – Ecole Centrale de Lyon, France (2023)

11. DA COSTA GUEDES Thalis
Title of thesis: **Study and development of new structures against electrostatic discharges (ESD) for radio frequency and millimetre wave applications**
Expected date of defence: **2026**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2022)

12. DOBRIN Catalin Andrei
Title of thesis: **Design of self-adjusting Radiofrequency circuits to optimize the energy efficiency of applications**
Expected date of defence: **2026**
Previous degrees: Master – Université Grenoble Alpes, France (2023)

13. GENTIL LÉ Joao Eduardo
Title of thesis: **Study of RF circuits in D Band in BiCMOS 55nm technologies**
Expected date of defence: **2026**
Previous degrees: Diplôme étranger – Baccalauréat en génie – Université de Sao Paulo, Brazil (2021)

14. HAI Joycelyn
Title of thesis: **RF Reliability in C065SOI FEM mmW : Device Model and Application to Power Amplifier**
Expected date of defense: **2024**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

15. IBRAHIM Sana
Title of thesis: **Clock Generation For Low Power Receiver based on N-Path Mixers**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2020)

16. MADHVARAJ Manasa
Title of thesis: **IPS for mixed-signal/high speed integrated circuits dependability and control**
Expected date of defense: **2024**
Previous degrees: Master SJCE, Visvesvaraya Technological University – Mysore, India (2015)

17. MALBEC Pierre
Title of thesis: **Analysis of the pollutions of a switch mode power supply on a Bluetooth Low Energy type Radio Frequency transmitter embedded on a same System on Chip**
Expected date of defense: **2024**
Previous degrees: Master – Université de Montpellier – France (2020)

18. MAMGAIN Ankush
Title of thesis: **On-chip generation of high-frequency sinusoidal signals using harmonic cancellation techniques**
Expected date of defense: **2024**
Previous degrees: Master MTech – IIIT Delhi - New Delhi, India (2018)

19. MOHSEN Fadel
Title of thesis: **HRNPM_based low power receivers - Spintronic diodes based wake-up radios**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2022)

20. NAOUI Ayoub
Title of thesis: **Integration of RF switches based on chalcogenide phase change materials: application to millimeter wave imaging**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2021)

21. OCCELLO Olivier
Title of thesis: **Self-learning self-test and self-calibration for integrated millimeter-wave systems**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2020)

22. OTMANI Mehdi
Title of thesis: **Towards More Efficient 5G/6G Wireless Communication Systems: Design and of a Hybrid RF Front-End Module**
Expected date of defence: **2026**
Previous degrees: Engineer – Bordeaux INP – Enseirb Matmeca (2023)

23. OUATTARA David
Title of thesis: **Design of phase shifters based on new architectures for mm-wave applications: 5G/6G & automotive radar**
Completed on: **March 23, 2023**
Previous degrees: Bordeaux INP - ENSEIRB-Matméca Talence - Bordeaux, France (2019)

24. PALOMINO MARCELO Gustavo Adolfo

Title of thesis: **Implementation of heterogeneous technologies for the integration of "front-end" type systems in D band (140-170 GHz)**
Expected date of defence: **2026**
Previous degrees: Master in electric engineer – State University of Campinas, Brazil (2021)

25. PINO MONROY Dayana Andrea

Title of thesis: **RF design methodology based on MOS transistors for circuit / technology optimization**
Completed on: **March 30, 2023**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2019)

26. POUPON Julien

Title of thesis: **Study of the Gm/ID design methodology for low-power RF/mmW frequency synthesizers in SOI technology**
Expected date of defense: **2025**
Previous degrees: Engineer – Bordeaux INP - ENSEIRB-Matméca Talence - Bordeaux, France (2022)

27. WEHBI Mohammed

Title of thesis: **Design of patch filters for millimeter-wave applications in BiCMOS 55-nm technology**
Completed on: **March 6, 2023**
Previous degrees: Master - Arab University of Beyrouth - Lebanon (2017)

28. ZIDANE Hajar

Title of thesis: **Sub-THz circuits based on substrate integrated waveguides in integrated and above-IC technologies**
Expected date of defence: **2026**
Previous degrees: Master – Université Grenoble Alpes, France (2023)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. BENDJEDDOU	Imadeddine	ALGERIA	9 months
2. BOUCHOUCHA	Mohamed Khalil	TUNISIA	1 month
3. CORSI	Jordan	FRANCE	12 months
4. EL CHAAR	Mohamad	LEBANON	9 months
5. HELLIER	Pierre-Louis	France	3 months

Visitors

Name	Forename	Country	Duration
1. DE MARCO	Raffaele	ITALY	3 months
2. HAMID ALLAH	Abdelhak	MOROCCO	2 months
3. LACORTE CANIATO SERRANO	Ariana	BRAZIL	8 months
4. LELLOUCH	Alexandre	FRANCE	4 months
5. PLAMPLONA REHDER	Gustavo	BRAZIL	8 months

Trainees

Name	Forename	Country	Duration
1. AKARRACHI	Widad	FRANCE	3 months
2. ALSUKOUR	Mohammad	FRANCE	3 months
3. BRIDET	Adrien	FRANCE	4 months
4. DOBRIN	Catalin Andrei	France	9 months
5. FOURCADE	Léandre	FRANCE	3 months
6. GRANADOS	Irwin	FRANCE	4 months
7. HOURDRY	Benjamin	FRANCE	3 months
8. JEANNIN	Lucie	FRANCE	4,5 months
9. KHACHAB	Mohamad	LEBANON	3 months
10.KHIBANE	Nouhaila	FRANCE	3 months
11.LI	Xiao	FRANCE	10,5 months
12.MEKHALDI	Amine	FRANCE	3 months
13.MO	Manqi	CHINA	6 months
14.OLIVEIRA	Aquiles	BRAZIL	3 months
15.SABIA PEREIRA CARPES	Victor	BRAZIL	3 months
16.SILVA	Felipe	BRAZIL	2,5 months
17.SIMIONATO	Eligia	BRAZIL	3 months
18.WANG	Zitian	FRANCE	3 months
19.XUAN	Hanwen	FRANCE	3 months
20.ZIDANE	Hajar	FRANCE	9 months

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2023.

ANR

IMHOTEP (2022 – 2024)
Scientific manager: Florence PODEVIN

PRECISE (2022 – 2025)
Scientific manager: Jean-Daniel ARNOULD

CIFRE

CIFRE Oumayma BELKHADRA (2021 – 2024)
Title: Self-tuning power amplifier in advanced CMOS technology for automotive radar
Thesis director: Sylvain BOURDEL
Industrial partner: NXP

CIFRE Mohamed Khalil BOUCHOUCHA (2020 – 2023)
Title: Design methodology based on the inversion coefficient for RF and mmW circuits optimization using 28 nm FDSOI technology
Thesis director: Sylvain BOURDEL
Industrial partner: STMicroelectronics

CIFRE Larbi BOUKHEZAR (2023 – 2026)
Title: Agile front-end topology at millimetre frequencies using in situ calibration solutions. Application to the design of D-band phase shifters, Comparison of active and passive approaches
Thesis director: Philippe FERRARI
Industrial partner: STMicroelectronics

CIFRE Giovanni BRITTON (2020 – 2023)
Title: Design of an FD-SOI read / control circuit dedicated to the field of quantum computing under Cryogenic conditions
Thesis director: Salvador MIR
Industrial partner: STMicroelectronics

CIFRE Benjamin BUREAU (2023 – 2026)
Title: Investigation of single spin qubits fabricated with industrial processes as a resource for quantum application with hybrid quantum circuits
Thesis director: Salvador MIR
Industrial partner: STMicroelectronics
Academic partner: University of Sherbrooke

CIFRE Thalis DA COSTA GUEDES (2023 – 2026)
Title: Study and development of new structures against electrostatic discharges (ESD) for radio frequency and millimetre wave applications
Thesis director: Philippe FERRARI
Industrial partner: STMicroelectronics

CIFRE Pierre MALBEC (2020 – 2023)
Title: Analysis of the pollutions of a switch mode power supply on a Bluetooth Low Energy type Radio Frequency transmitter embedded on a same System on Chip
Thesis director: Jean-Daniel ARNOULD
Industrial partner: STMicroelectronics

ETAT

SHIFT BPI (2022 – 2025)
Program: KDT JU
Scientific manager: Philippe FERRARI

EUROPE

SHIFT EU (2022 – 2025)
Program: KDT JU
Scientific manager: Philippe FERRARI

SWAN-on-chip (2022 – 2025)
Program: HORIZON
Scientific manager: Florence PODEVIN

INDUSTRIE

CIMITRANS (2023 – 2027)
Program: France 2030
Scientific manager: Sylvain BOURDEL

PEPR

NF-SYSTERA (2023 – 2027)
Program: 5G
Scientific manager: Philippe FERRARI

NF-YACARI (2023 – 2027)
Program: 5G
Scientific manager: Sylvain BOURDEL

SPINCOM (2023/2027)
Program: SPIN
Scientific manager: Florence PODEVIN

TUTELLE

MASHWave (2022 – 2024)
Title: MAchine learning-based Self-Healing of mmW ICs
Program: IRGA
Scientific manager: Manuel BARRAGAN

NPATH LOW-POWER (2022 - 2024)
Program: IRGA
Scientific manager: Florence PODEVIN

Organization and participation of international conferences, workshops, forums

ESSCIRC-ESSDERC 2023 - IEEE 49th European Solid-State Circuits Conference / IEEE 53rd European Solid-State Device Research Conference
September 11-14, 2023 - Lisbon, PORTUGAL
Rank: A
technical program committee: BARRAGAN Manuel

ETS 2023 - 28th IEEE European Test Symposium
May 22-26, 2023 - Venice, ITALY
Rank: A
technical program committee: BARRAGAN Manuel, MIR Salvador

ICCAD 2023 - 7th International Conference on Control, Automation and Diagnosis (ICCAD (Control Automation and Diagnosis)'2023)
May 10-12, 2023 – Rome, ITALY
Rank: NC
program chair: SIMEU Emmanuel

IOLTS 2023 - 29th IEEE International Symposium on On-Line Testing and Robust System Design
July 3-5, 2023 - Chania (Crete), GREECE
Rank: B
program committee: BARRAGAN Manuel, MIR Salvador, SIMEU Emmanuel

LASCAS 2023 - IEEE 14th Latin American Symposium on Circuits and Systems
February 28-March 3, 2023- Quito, ECUADOR
Rank: B
technical program committee: MIR Salvador

LATS 2023 - 24th IEEE Latin-American Test Symposium
March 21-24, 2023 - Veracruz, MEXICO
Rank: NC
program committee: MIR Salvador

NEWCAS 2023 - 21st IEEE International NEWCAS Conference
June 26-28, 2023 - Edinburgh (Scotland), UNITED KINGDOM
technical committee: BARRAGAN Manuel

VLSI-SoC 2023 - 31st IFIP/IEEE International Conference on Very Large Scale Integration
October 16-18, 2023 - Dubai, UNITED ARABIAN EMIRATES
Rank: A
publication co-chair: MIR Salvador
steering committee: MIR Salvador
technical program committee: MIR Salvador

VTS 2023 - 41st IEEE VLSI Test Symposium
April 24-26, 2023 - San Diego (CA), USA
Rank: A
program committee: BARRAGAN Manuel, MIR Salvador

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
Polytech Grenoble				
Manager of Risks Prevention department	SIMEU Emmanuel	01/09/2017		
Restricted council member	SIMEU Emmanuel	01/09/2017		Examine promotion files, invited professors, teaching assistants
School council member	SIMEU Emmanuel	01/09/2017		Elected members - School Strategy, relations with industrial partners
TIMA Laboratory				
Research structures				
EEATS doctoral school Électronique, Électrotechnique, Automatique, Traitement du Signal				
Council member of EEATS doctoral school	SIMEU Emmanuel	01/09/2017		

Scientific production

International journals

Ouattara David, Durand Cédric*, Bourdel Sylvain, Paillardet Frédéric, Vincent Loïc***, Corsi Jordan, Ferrari Philippe**
120 GHz 2-bit reflection-type phase shifter based on PIN diodes switched-lines
Electronics Letters, Volume: , 2023
**STMicroelectronics [Crolles], **STMicroelectronics [Genève], ***Centre Interuniversitaire de Micro-Electronique*

Pino Monroy Dayana Andrea*, Pino Monroy Dayana Andrea, Scheer Patrick*, Bouchoucha Mohamed Khalil*, Bouchoucha Mohamed Khalil, Galup-Montoro Carlos, Barragan Manuel, Cathelin Philippe*, Fournier Jean-Michel, Cathelin Andreia*, Bourdel Sylvain**
Corrections to “Design-Oriented All-Regime All-Region 7-Parameter Short-Channel MOSFET Model Based on Inversion Charge”
IEEE Access, Volume: 11, 2023
**STMicroelectronics [Crolles], **UFSC - Universidade Federal de Santa Catarina = Federal University of Santa Catarina [Florianópolis]*

Artemio Schoulten Felipe*, Vauché Rémy*, Gaubert Jean*, Bourdel Sylvain, Mariano André Augusto**
Design of a multi-standard IR-UWB emitter in a 28 nm FD-SOI technology based on the frequency transposition pulse synthesis
Journal of Integrated Circuits and Systems, Volume: 18, pp. 1-11, 2023
**Institut Matériaux Microélectronique Nanosciences de Provence, **Universidade Federal do Paraná [Curitiba]*

De Saxce Joseph*, Siah Chun Fei, Tan Chong Wei**, Passerieux Damien*, Bila Stéphane*, Podevin Florence, Tay Beng Kang**, Coquet Philippe**, Coquet Philippe***, Baillargeat Dominique***
E-Band Vertically Aligned Carbon Nanotubes-Based Air-Filled Waveguide
IEEE Microwave and Wireless Technology Letters, Volume: , pp. 1-4, 2023
**XLIM, **CNRS International - NTU - Thales Research Alliance, ***Institut d'électronique, de microélectronique et de nanotechnologie*

Bendjeddou Imadeddine, Jotta Garcia Mafalda*, Sidi El Valli Ahmed, Litvinenko Artem**, Cros Vincent*, Ebels Ursula**, Jenkins Alex***, Ferreira Ricardo***, Dutra Roberta***, Morche Dominique****, Pistono Emmanuel, Bourdel Sylvain, Le Guennec Yannis*****, Podevin Florence**
Electrical Modeling of Spin-Torque Diodes Used as Radio Frequency Detectors: A Step-by-Step Methodology for Parameter Extraction
IEEE Transactions on Microwave Theory and Techniques, Volume: , pp. 1-11, 2023
**Unité mixte de physique CNRS/Thalès (PALAISEAU), **Spintec, ***International Iberian Nanotechnology Laboratory, ****Laboratoire d'Electronique de Technologie de l'Information, *****GIPSA-Lab*

Zahran Sherif*, Moscato Stefano, Fonte Alessandro**, Oldoni Matteo***, Traversa Antonio A.**, Tresoldi Dario**, Ferrari Philippe, Amendola Giandomenico*, Boccia Luigi***
Flippable and Hermetic E-Band RWG to GCPW Transition With Substrate Embedded Backshort
IEEE Transactions on Microwave Theory and Techniques, Volume: 71, pp. 2582 - 2593, 2023
**Millimeter-wave Antennas and Integrated Circuits Laboratory , **SIAE Microelettronica [Milan], ***Dipartimento di Elettronica, Informazione e Bioingegneria (POLIMI)*

Melis Tommaso*, Simeu Emmanuel, Auvray Etienne, Saury Luc***
Light Emission Tracking and Measurements for Analog Circuits Fault Diagnosis in Automotive Applications
Journal of Electronic Testing: Theory and Applications (JETTA), Volume: , 2023
**STMicroelectronics [Grenoble], **Fastnet-technologies*

Bontems William, Dzahini Daniel
Methodology for a Low-Power and Low-Circuit-Area 15-Bit SAR ADC Using Split-Capacitor Mismatch Compensation and a Dynamic Element Matching Algorithm
Chips, Volume: 2, pp. 31-43, 2023

Corsi Jordan, Plamplona Rehder Gustavo*, Ferrari Philippe, Lacorte Caniato Serrano Ariana Maria Da Conceiçao*, Pistono Emmanuel
Modeling and Design of a Partially Air-Filled Slow Wave Substrate Integrated Waveguide
IEEE Transactions on Microwave Theory and Techniques, Volume: 71, pp. 750-762, 2023
**University of Sao Paulo*

Cilici Florent*, Margalef-Rovira Marc*, Lauga-Larroze Estelle, Bourdel Sylvain, Leger Gildas***, Vincent Loïc****, Mir Salvador, Barragan Manuel**
Nonintrusive Machine Learning-Based Yield Recovery and Performance Recentering for mm-Wave Power Amplifiers: A Two-Stage Class-A Power Amplifier Case Study
IEEE Transactions on Microwave Theory and Techniques, Volume: 72, pp. 3046-3064, 2023
**NXP semiconductors*
***ST-CROLLES - STMicroelectronics [Crolles]*
****IMSE-CNM - Instituto de Microelectrónica de Sevilla*
*****CIME Nanotech*

Charlet Ismaël*, Guerber Sylvain*, Naoui Ayoub*, Naoui Ayoub, Naoui Ayoub, Charbonnier Benoit*, Dupré Cécilia*, Lugo-Alvarez José*, Héllion Clémence*, Allain Marjolaine*, Podevin Florence, Perret Etienne**, Reig Bruno***
Optical Actuation Performance of Phase-Change RF Switches
Electron Device Letters, Volume: Early access, pp. 1-1, 2023
**Laboratoire d'Electronique de Technologie de l'Information, **Laboratoire de Conception et d'Intégration des Systèmes*

Kriekouki Ioanna*, Kriekouki Ioanna, Kriekouki Ioanna, Philippopoulos Pericles***, Beaudoin Félix***, Mir Salvador, Barragan Manuel, Pioro-Ladrière Michel**, Galy Philippe***
Simulation process flow for the implementation of industry-standard FD-SOI quantum dot devices
Solid-State Electronics , Volume: 209, pp. Article 108777, 2023
**STMicroelectronics [Crolles], **Institut Quantique [Sherbrooke], ***Nanoacademic Technologies Inc.*

Kriekouki Ioanna*, Kriekouki Ioanna, Kriekouki Ioanna, Beaudoin Félix***, Philippopoulos Pericles***, Zhou Chenyi***, Camirand-Lemyre Julien**, Rochette Sophie**, Rohrbacher Claude**, Mir Salvador, Barragan Manuel, Pioro-Ladrière Michel**, Galy Philippe***
Understanding conditions for the single electron regime in 28 nm FD-SOI quantum dots: Interpretation of experimental data with 3D quantum TCAD simulations
Solid-State Electronics , Volume: 204, 2023
**STMicroelectronics [Crolles], **Institut Quantique [Sherbrooke], ***Nanoacademic Technologies Inc.*

Patents

Alshakoush Ali, Bourdel Sylvain, Podevin Florence, Lauga-Larroze Estelle, Fesquet Laurent
Mélangeur à N Chemins à réjection d'harmoniques
Brevet N° FR3125934A1, delivered on Feb 03, 2023

International conferences

Alves Neto Deni Germano*, Missel Adotnes Cristina*, Maranhão Gabriel*, Bouchoucha Mohamed Khalil, Bouchoucha Mohamed Khalil, Barragan Manuel, Cathelin Andreia**, Schneider Marcio Cherem*, Bourdel Sylvain, Galup-Montoro Carlos***
A 5-DC-parameter MOSFET model for circuit simulation in QucsStudio and SPECTRE
21st IEEE Interregional NEWCAS Conference (NEWCAS 2023), 2023
** Department of Electrical and Electronics Engineering, **STMicroelectronics [Crolles]*
Seré Andres*, Barboni Leonardo*, Bourdel Sylvain, Silveira Fernando*
Active inductors modelling and trade-offs reexamined
IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS 2023), 2023
**UDELAR, Facultad de Ingenieria, Universidad de la Republica, Montevideo, Uruguay*
Mamgain Ankush, Mir Salvador, Tripathi Jai Narayan*, Barragan Manuel
A harmonic cancellation-based high-frequency on-chip sinusoidal signal generator with calibration using a coarse-fine delay cell
IEEE International Symposium on Circuits and Systems (ISCAS 2023), 2023
**Indian Institute of Technology Jodhpur*
Doan Phi-Long, Corsi Jordan, Tay Beng Kang*, Jiang Rongtao*, De Saxce Joseph, Coquet Philippe*, Coquet Philippe***, Wang Jianxiong*, Baillargeat Dominique**, Pistono Emmanuel, Podevin Florence**
Air-Filled and Slow-Wave CNT-Based Substrate Integrated Waveguide
53rd European Microwave Conference (EuMC 2023), pp. 850-853, 2023
**CNRS International - NTU - Thales Research Alliance, **XLIM, ***Institut d'électronique, de microélectronique et de nanotechnologie*
Dzahini Daniel, Leheurteux Etienne*, Gallin-Martel Laurent, Zeloufi Mohamed***
A low crosstalk 768-channel of 14-bit analog to digital converters for high resolution array of detectors
Topical Workshop on Electronics for Particle Physics (TWEPP 2023), 2023
** XDIGIT , **LPSC - Laboratoire de Physique Subatomique et de Cosmologie*
Saïd Aïcha*, Hameau Frédéric*, Vauché Rémy, Siligaris Alexandre*, Podevin Florence, Bourdel Sylvain**
A Millimeter Wave High Isolation Resistive Coupler In 45nm RFSOI Technology for Sensing Application
Asia-Pacific Microwave Conference (APMC 2023), pp. 611-613, 2023
**Laboratoire d'Electronique de Technologie de l'Information, **Institut Matériaux Microélectronique Nanosciences de Provence*
Mamgain Ankush, Madhvaraj Manasa, Mir Salvador, Barragan Manuel, Tripathi Jai Narayan*
A sub-picosecond resolution jitter instrument for GHz frequencies based on a sub-sampling TDA
21st IEEE Interregional NEWCAS Conference (NEWCAS 2023), 2023
**Indian Institute of Technology Jodhpur*
Bouchoucha Mohamed Khalil*, Bouchoucha Mohamed Khalil, Barragan Manuel, Cathelin Andreia*, Bourdel Sylvain
A wideband sub-6GHz continuously tunable gm-boosted CG Low Noise Amplifier in 28 nm FD-SOI CMOS technology
IEEE 49th European Solid State Circuits Conference (ESSCIRC 2023), 2023
**STMicroelectronics [Crolles]*
Zahran Sherif*, Zahran Sherif, Alati Antonio*, de Marco Raffaele*, Moscato Stefano, Fonte Alessandro**, Amendola Giandomenico*, Ferrari Philippe, Boccia Luigi***
Bondwire Integration Challenges in E-band Systems: from PCB to Die Level
53rd European Microwave Conference (EuMC 2023), 2023
**Millimeter-wave Antennas and Integrated Circuits Laboratory , **SIAE Microelettronica [Milan]*
Pino Monroy Dayana Andrea*, Scheer Patrick*, Bouchoucha Mohamed Khalil*, Galup-Montoro Carlos, Barragan Manuel, Fournier Jean-Michel, Cathelin Andreia*, Bourdel Sylvain**
Design-oriented model for short-channel MOS transistors based on inversion charge
IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS 2023), 2023
**STMicroelectronics [Crolles], **UFSC - Universidade Federal de Santa Catarina = Federal University of Santa Catarina [Florianópolis]*
Agouzoul Abdelali, Simeu Emmanuel, Tabaa Mohamed*
Enhancement of Building Energy Consumption Using a Digital Twin based Neural Network Model Predictive Control
International Conference on Control, Automation and Diagnosis (ICCAD 2023), 2023
**Laboratoire Pluridisciplinaire de recherche et innovation*
Zahran Sherif*, Boccia Luigi*, Podevin Florence, Amendola Giandomenico*, Ferrari Philippe
Fully Integrable BiCMOS Classical Rat-Race Coupler Based on BEOL CPS Transmission Lines
International Microwave and Antenna Symposium (IMAS 2022), 2023
**Millimeter-wave Antennas and Integrated Circuits Laboratory*
Zahran Sherif*, Zahran Sherif, Boccia Luigi*, Podevin Florence, Amendola Giandomenico*, Ferrari Philippe
Fully Integrable BiCMOS Classical Rat-Race Coupler Based on Coplanar Striplines
International Microwave and Antenna Symposium (IMAS 2023), 2023
**Millimeter-wave Antennas and Integrated Circuits Laboratory*
Naoui Ayoub*, Naoui Ayoub, Reig Bruno*, Perret Etienne, El Chaar Mohamad, Podevin Florence**
Indirect electrical-control through heating of a GeTe phase change switch and Its application to reflexion type phase shifting
International Microwave & Antennas Symposium (IMAS 2023), pp. 13-18, 2023
**Laboratoire d'Electronique de Technologie de l'Information, **Laboratoire de Conception et d'Intégration des Systèmes*
Barthélémy Hervé*, Barthélémy Florent, Vauché Rémy*, Bourdel Sylvain**
Inductive relaxation oscillator with current-limiting
21st IEEE Interregional NEWCAS Conference (NEWCAS 2023), 2023
**Institut Matériaux Microélectronique Nanosciences de Provence, **École nationale supérieure de physique, électronique, matériaux (Grenoble INP)*
Hai Joycelyn*, Cacho Florian*, Federspiel Xavier*, Garba-Seybou Tidjani*, Divay Alexis, Lauga-Larroze Estelle, Arnould Jean-Daniel**
Integrated Test Circuit for Off-State Dynamic Drain Stress Evaluation
IEEE International Reliability Physics Symposium (IRPS 2023), 2023
**STMicroelectronics [Crolles], **Laboratoire d'Electronique de Technologie de l'Information*

Moussa Hasan, Gonsalves Santos Jéssica, Lauga-Larroze Estelle, Ibrahim Sana, Podevin Florence, Bourdel Sylvain, Fesquet Laurent
Making Digital N-Path Mixers
38th Conference on Design of Circuits and Integrated Systems (DCIS 2023), 2023
Britton Orozco Giovani Crasby, Mir Salvador, Lauga-Larroze Estelle, Dormieu Benjamin*, Berlingard Quentin, Cassé Mickaël**, Galy Philippe***
Noise modeling using look-up tables and DC measurements for cryogenic applications
31st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2023), pp. 1-6, 2023
**STMicroelectronics [Crolles], **Laboratoire d'Electronique de Technologie de l'Information*
Srinivassane Naveen*, Saïd Aïcha*, Hameau Frédéric*, Vauché Rémy, Podevin Florence, Bourdel Sylvain**
Oscillator Based Bio-Sensor for Skin Sweating Detection: A Feasibility Survey
18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME 2023), 2023
**Laboratoire d'Electronique de Technologie de l'Information, **Institut Matériaux Microélectronique Nanosciences de Provence*
Bouchoucha Mohamed Khalil*, Bouchoucha Mohamed Khalil, Coustans Mathieu*, Barragan Manuel, Cathelin Andreia*, Bourdel Sylvain
Performance benchmark of State-of-the-art Sub-6-GHz wideband LNAs Based on an Extensive Survey
IEEE International Symposium on Circuits and Systems (ISCAS 2023), 2023
**STMicroelectronics [Crolles]*
Bouchoucha Mohamed Khalil*, Bouchoucha Mohamed Khalil, Pino Monroy Dayana Andrea*, Pino Monroy Dayana Andrea, Scheer Patrick*, Cathelin Philippe*, Fournier Jean-Michel, Barragan Manuel, Cathelin Andreia*, Bourdel Sylvain
Resistive Feedback LNA design using a 7-parameter design-oriented model for advanced technologies
IEEE International Symposium on Circuits and Systems (ISCAS 2023), 2023
**STMicroelectronics [Crolles]*
Kriekouki Ioanna*/, Philippopoulos Pericles***, Beaudoin Félix***, Mir Salvador, Barragan Manuel, Pioro-Ladrière Michel**, Galy Philippe***
Simulation process flow for the implementation of industry-standard FD-SOI quantum dot devices
Joint International Eurosol Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS) 2023
**ST-CROLLES - STMicroelectronics [Crolles]*
***UdeS - Institut Quantique [Sherbrooke]*
****Nanoacademic Technologies Inc.*
Mamgain Ankush, Mir Salvador, Tripathi Jai Narayan*, Barragan Manuel
Special Session: A high-frequency sinusoidal signal generation using harmonic cancellation
IEEE 24th Latin American Test Symposium (LATS 2023) , pp. 1-2 (Proceedings of LATS), 2023
**Indian Institute of Technology Jodhpur*
Madhvaraj Manasa, Mir Salvador, Barragan Manuel
Special Session: On-chip jitter BIST with sub-picosecond resolution at GHz frequencies
IEEE 24th Latin American Test Symposium (LATS 2023), pp. 1-2 (Proceedings of LATS), 2023
Palomino Marcelo Gustavo Adolfo*, Griep Gabriel, Griep Gabriel*, Marcati Gustavo*, Lacorte Caniato Serrano Ariana Maria Da Conceiçao*, Plamplona Rehder Gustavo*, Ferrari Philippe**
Suspended CPW Integration on Nanoporous Alumina Interposer for Millimeter Wave Applications
53rd European Microwave Conference (EuMC 2023), 2023
**University of São Paulo, **Instituto de Pesquisas Tecnologicas*
Malbec Pierre*, Malbec Pierre, Malbec Pierre***, Arnould Jean-Daniel, Vollaire Christian*, Duchamp Jean-Marc**, Chesneau David*****
Switched-Mode Power Supply Impact on a Bluetooth Low Energy Receiver Inside a Microcontroller
53rd European Microwave Conference (EuMC 2023), 2023
**Ampère, **Laboratoire de Génie Electrique de Grenoble, ***STMicroelectronics [Grenoble]*
Zimmer Thomas*, Bouzar Tarek*, Arnould Jean-Daniel, Fregonese Sebastien*
What causes the fluctuations in fmax with respect to frequency?
35th BipAK 2023 (Bipolar Arbeit Kreis)
**IMS - Laboratoire de l'intégration, du matériau au système*

Other communications

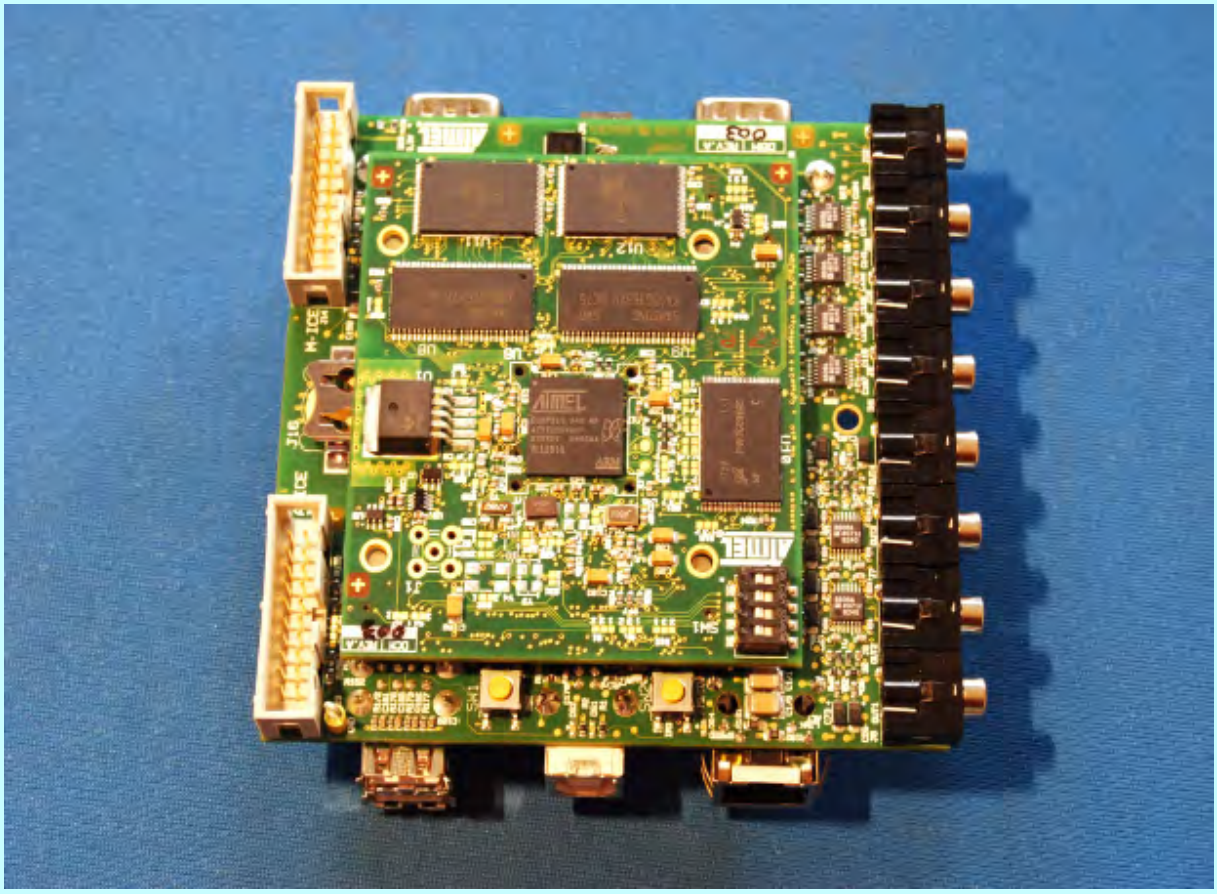
Artemio Schoulten Felipe*, Vauché Rémy*, Gaubert Jean*, Bourdel Sylvain, Mariano André Augusto**
Conception d'un émetteur-récepteur pour les communications par impulsion à courte portée
Séminaire recherche de l'IUT d'Aix-Marseille, Marseille, FRANCE
**Institut Matériaux Microélectronique Nanosciences de Provence, **Universidade Federal do Paraná [Curitiba]*
Bontems William, Dzahini Daniel
Design of a very low power 12 bits 40 MS/s ADC based on a time-interleaved SAR architecture
Topical Workshop on Electronics for Particle Physics (TWEPP 2023), Geremeas (Sardinia), ITALY

Theses

Ouattara David
Design of phase shifters based on new architectures for mm-wave applications: 5G/6G & automotive radar
These de Doctorat, Université Grenoble Alpes, spécialité "", Mar 23, 2023
Pino Monroy Dayana Andrea
RF design methodology based on MOS transistors for circuit / technology optimization
These de Doctorat, Université Grenoble Alpes, spécialité "", Mar 30, 2023
Wehbi Mohammed
Design of patch filters for millimeter-wave applications in BiCMOS 55-nm technology
These de Doctorat, Université Grenoble Alpes, spécialité "", Mar 06, 2023

TiMA
CNRS — GRENOBLE INP — UGA

SLS team



System Level Synthesis

System Level Synthesis (SLS team)

Research activities

The SLS team focuses on (a) highly efficient architectures for general purpose computing or AI-dedicated algorithms, (b) system-level modeling and design methodology : specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware. The work of the team is included in the Laboratory themes “Hardware/software codesign” and “Simulation and verification of systems” described below.

Hardware/software codesign

Our research on high performance general purpose processors explores the use of value prediction in processor design. We have shown that simple value prediction can be implemented by reusing existing pipeline structures, leading to increased performance with reduced overheads. We have also shown that predicting values enables the dynamic "reduction" of some instructions (e g., transforming an add into a nop at runtime), which further improves performance. So far, we have considered value prediction for out-of-order microarchitectures only. In the meantime, through a collaboration with University of Murcia in Spain, we have shown that conservative implementations of atomic read-modify-write instructions (which are used to write higher-level synchronization primitives) in x86 processors incurred significant overhead and proposed a more aggressive implementation to significantly reduce the time spent synchronizing threads.

Multi-core and many-core architectures have evolved towards a set of clusters. Each cluster integrates a set of cores, a cache memory and a local memory shared by all the cores of the cluster. We have worked on hardware methods for distributing memory bank accesses in many-core architectures by experimenting on the MPPA Kalray processor. In addition, we have proposed an innovative hardware support for synchronization locks. This decentralized solution manages dynamic re-homing of locks in a dedicated memory, close to the latest access-granted core.

On the dedicated architecture side, the team is still working on Artificial Intelligence. After our work on high-throughput ternary neural network, we have collaborated with the university of Salerno on the design of a tiny Binary Neural Network for human recognition applications.

Through a collaboration with OVHcloud, we also worked on a dedicated IP used in their mitigation systems to face Distributed Denial-of-Service (DDOS) attacks. In this domain, hard- ware development has to be agile. By introducing the Chisel hardware construction language in the hardware design flow, we showcase how Chisel unleashes the power of agile development methodologies through development iterations. We have also shown through a General Matrix Multiply implementation case study that Chisel can be used to generate highly parametrizable circuits, bringing huge benefits in design exploration, reuse and designer productivity.

Simulation and verification of systems

Modeling and simulation of cyber-physical devices is challenging because of their heterogeneity: discrete events simulation progresses by discrete timesteps while continuous time simulation does so in a time continuum. The SystemC AMS synchronization strategy is based on fixed timesteps and can generate inaccuracies overcame only at expanse of simulation speed. We have proposed a new continuous time and discrete events synchronization algorithm on top of the SystemC framework and have proven its causality, completeness and liveness. In addition, we have also proposed an adaptive algorithm to adjust the synchronization step to provide near to optimum simulation speed. Results on various cases studies have demonstrated that our algorithm circumvents these challenges, attains high accuracy with respect to established tools, and improves simulation speed. This work aims at enlarging the modeling and simulation capabilities of SystemC as a heterogeneous design tool.

Today’s SoCs require a complex design and verification process. In early design stages, high-level debugging of the SoC functionality is feasible on TLM (Transaction-Level Modeling) descriptions. To ease debugging of such SoC’s models, Assertion-Based Verification (ABV) enables the runtime verification of temporal properties. In the last design stages, RTL (Register Transfer Level) descriptions of hardware blocks expose microarchitectural details. To gain confidence in the validity of system level properties after this TLM-to-RTL synthesis, transaction level assertions must be reverifiable on RTL models. To address that issue, we propose refinement rules for the automatic system level to signal level transformation of PSL assertions (Property Specification Language, IEEE standard 1850).

Many scientific applications require higher accuracy than what can be represented on 64 bits of the floating-point IEEE 754 standard, and to that end make use of dedicated arbitrary precision software libraries such as MPRF. To reach a good performance/accuracy trade-off, developers use variable precision, requiring e.g. more accuracy as the computation progresses. Hardware accelerators for this kind of computations do not exist yet, and independently of the actual quality of the underlying arithmetic computations, defining the right instruction set architecture, memory representations, etc, for them is a challenging task. We have investigated the support for arbitrary and variable precision arithmetic in a dynamic binary translator (QEMU implementation), to help gain an insight of what such an accelerator could provide as an interface to compilers, and thus programmers. Through collaborations, we also worked on a FP representation supporting both static and dynamically variable precision: by designing its compilation flow to hardware FP instructions or software libraries, and by demonstrating its performance, far better than the Boost programming interface for the MPFR library on the PolyBench suite. Simulations of manycores architectures take a lot of time with gem5 (simulator used for manycores architectures), to improve this point we explore the accuracy of QEMU. QEMU used the DBT (Dynamic Binary Translation) mechanism which transforms instructions from a target ISA to a host ISA. In our experimentations, the target ISA is RISC-V, several of the team works used RISC-V eco-system. To reduce the simulation time of manycores architectures with QEMU, we propose to pin vCPUs (virtual CPUs simulated by QEMU) to physical CPUs on the host,

e.g. forcing vCPU to run on a chosen physical CPU. PARSEC benchmarks are used to obtain results. Unfortunately, pinning vCPUs does not improve the execution time of our programs. Simulators based on the DBT are fast because they focus on instructions and do not modeling architecture. We propose to add the cache representation in QEMU to improve the accuracy.

Recent highlights

Online learning and prototyping of digital systems

Scientific Manager: ROUSSEAU Frédéric
Partners: National University Galway
City: Galway
Country: IRELAND
Start the: Jan 01, 2017 until Dec 31, 2024

Academic and research members

Liliana ANDRADE

Position
Associate professor at UGA - Polytech school

Responsibilities
Researcher in SLS team

Julie DUMAS

Position
Associate professor at Grenoble INP – Ensimag school

Responsibilities
Researcher in SLS team

Olivier MULLER

Position
Associate professor at Grenoble INP – Ensimag school

Responsibilities
Leader of SLS team
Researcher in SLS team

Arthur PERAIS

Position
Researcher at CNRS

Responsibilities
Researcher in SLS team

Frédéric PÉTROT

Position
Professor at Grenoble INP – Ensimag school

Responsibilities
Researcher in SLS team

Laurence PIERRE

Position
Professor at UGA – IM2AG school

Responsibilities
Researcher in SLS team

Frédéric ROUSSEAU

Position
Professor at UGA – Polytech school

Responsibilities
Researcher in SLS team

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. BADAROUX Marie
Title of thesis: **Fast and accurate simulation of multi/many-core SoCS**
Expected date of defence: **2024**
Previous degrees: Engineer – Grenoble INP – Ensimag - Grenoble, France (2020)

2. BAIN Nathan
Title of thesis: **Methods for the learning and adapting formal neural networks to the constraints of hardware accelerators for applications optimized in power and / or throughput**
Expected date of defence: **2023**
Previous degrees: Engineer – Grenoble INP – Phelma - Grenoble, France (2020)

3. CATHELINEAU Benjamin
Title of thesis: **Test and reliability analysis for cyber-physical system models**
Thesis stopped on August 31, 2023
Previous degrees: Master UGA (Université Grenoble Alpes) – Grenoble, France (2022)

4. CHRIST Maxime
Title of thesis: **Learning in very low precision**
Thesis stopped on August 31, 2023
Previous degrees: Engineer - INSA Lyon, France (2017)

5. DESHPANDE Chandana
Title of thesis: **Building an Efficient 128-bit General Purpose Processor**
Expected date of defense: **2025**
Previous degrees: Master - Visvesvaraya Technological University – Bangalore, India (2014)

6. ISAAC—CHASSANDE Valentin
Title of thesis: **Design of a Memory System for Sparse Data Processing**
Expected date of defense: **2025**
Previous degrees: Master UGA Polytech - Grenoble, France (2022)

7. LE BERRE Timothée
Title of thesis: **Neural Nets with Hybrid Quantization: Theory, Design, and Hardware Acceleration**
Expected date of defense: **2026**
Previous degrees: Master Sorbonne Université - Paris, France (2023)

8. MILLION Davy
Title of thesis: **Open Source Heterogeneous Multi-Core Chiplet Architecture Exploration**
Expected date of defense: **2026**
Previous degrees: Master Université Clermont Auvergne – Clermont-Ferrand, France (2022)

9. RAVENEL Pierre
Title of thesis: **Improving the performance of in-order processors under hardware complexity constraints**
Expected date of defense: **2025**
Previous degrees: Engineer – Grenoble INP – Ensimag - Grenoble, France (2022)

10. TOMASI RIBEIRO Eduardo
Title of thesis: **Single address space for massively parallel computers**
Expected date of defense: **2025**
Previous degrees: Engineer – Grenoble INP – Ensimag - Grenoble, France (2019)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. PINZARI	Ana	FRANCE	12 months

Visitors

No visitors in 2023

Trainees

Name	Forename	Country	Duration
1. BITAUDEAU	Luca	FRANCE	2 months
2. LE BERRE	Timothée	FRANCE	5,5 months
3. SEBAN	Jules	FRANCE	2 months
4. TROUCHET	Ninon	FRANCE	1,5 month

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2023.

ANR

MAPLURINUM (2021 - 2025)
Title: Machinae pluribus unum - (faire) une seule machine avec plusieurs
Scientific manager: Olivier MULLER

RAKES (2019 – 2023)
Scientific manager: Frédéric PETROT

CIFRE

Thèse Nathan BAIN (2020 – 2023)
Title: Methods for the learning and adapting formal neural networks to the constraints of hardware accelerators for applications optimized in power and / or throughput
Thesis director: Frédéric PETROT
Industrial partner: STMicroelectronics

Thèse Pierre RAVENEL (2022 – 2025)
Title: Improving the performance of in-order processors under hardware complexity constraints
Thesis director: Frédéric PETROT
Industrial partner: Kalray

PEPR

ARCHI-CESAM (2023 – 2030)
Program: CLOUD
Scientific manager: Arthur PERAIS

HOLIGRAIL (2023 – 2027)
Program: Intelligence Artificielle
Scientific manager: Frédéric PETROT

TUTELLE

MIAI (2019 – 2023)
Program: MIAI
Scientific manager: Frédéric PETROT

Organization and participation of international conferences, workshops, forums

ARCHI 2023 - Ecole thématique portant sur l'architecture des systèmes matériels et logiciels embarqués, et les méthodes de conception associées
March 27-21, 2023 - Sarcenas, FRANCE
Rank: NC
general chair: PERAIS Arthur

COMPAS 2023 - Conférence francophone d'informatique en Parallélisme, Architecture et Système
July 4-7, 2023 – Annecy, FRANCE
Rank: NC
reading committee: MULLER Olivier

DATE 2023 - Design, Automation & Test in Europe (DATE 2023)
April 17-19, 2023 - Antwerp, BELGIUM
Rank: A+
topic member : PIERRE Laurence

MPSoC 2023 - 21st Multicore and Multiprocessor SoCs
June 25-30, 2023 - Fort Collins, USA
Rank: NC
co-finance chair : ROUSSEAU Frédéric
local organization: MULLER Olivier, ROUSSEAU Frédéric
publicity chair: PETROT Frédéric
technical program committee: PETROT Frédéric

RSP 2023 - 34th International Workshop on Rapid System Prototyping
September 21, 2023 - Hamburg, GERMANY
Rank: B
publication chair: MULLER Olivier
program chair: ROUSSEAU Frédéric
steering committee: PETROT Frédéric, ROUSSEAU Frédéric

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
ENSIMAG school École nationale supérieure d'informatique et de mathématiques appliquées de Grenoble				
Restricted council member	PETROT Frédéric	01/09/2017		Examine promotion files, invited professors, teaching assistants
	MULLER Olivier	01/09/2017		
School council member	MULLER Olivier	01/09/2017		Elected members - School Strategy, relations with industrial partners
	PETROT Frédéric	01/09/2017		
Polytech Grenoble				
Manager of E2I branch	ANDRADE Liliana	01/10/2019		5th year - Apprenticeship training
Deputy director in charge of education and training	ROUSSEAU Frédéric	01/09/2018		
Restricted council member	ROUSSEAU Frédéric	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Research commission member	PIERRE Laurence	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR Council member	PIERRE Laurence	01/09/2017		
TIMA Laboratory				
TIMA Laboratory				
Scientific animation	ANDRADE Liliana	01/09/2022		
Laboratory contact for european projects	ROUSSEAU Frédéric	01/09/2017		
EEATS doctoral school Électronique, Électrotechnique, Automatique, Traitement du Signal				
HDR commission president	ROUSSEAU Emmanuel	01/01/2020		
HDR commission member of EEATS doctoral school	ROUSSEAU Frédéric	01/09/2013		
MSTII doctoral school Mathématiques, Sciences et Technologies de l'Information, Informatique				
Council member of MSTII doctoral school	PIERRE Laurence	01/09/2017		
HDR commission member of MSTII doctoral school	PETROT Frédéric	01/09/2017		
MSTIC pole Mathématiques, sciences et technologies de l'information et de la communication				
TIMA representative of MSTIC cluster	PETROT Frédéric	01/09/2016		

Scientific production

International journals

Ferres Bruno, Muller Olivier, Rousseau Frédéric
A Chisel Framework for Flexible Design Space Exploration through a Functional Approach
ACM Transactions on Design Automation of Electronic Systems, Volume: 28, pp. 1-31, 2023
Deshpande Chandana S., Perais Arthur, Pétrot Frédéric
Toward Practical 128-bit General Purpose Microarchitectures
IEEE Computer Architecture Letters, Volume: 22, pp. 81-84, 2023

International conferences

Perais Arthur, Sheikh Rami*
Branch Target Buffer Organizations
56th IEEE/ACM International Symposium on Microarchitecture (MICRO 2023) , 2023
**ARM Inc.*
Badaroux Marie, Dumas Julie, Pétrot Frédéric
Fast Instruction Cache Simulation is Trickier than You Think
Proceedings of the DroneSE and RAPIDO: System Engineering for constrained embedded systems (RAPIDO 2023), pp. 48-53, 2023
Bain Nathan*, Bain Nathan, Guizzetti Roberto*, Taly Emilien*, Taly Emilien, Oudrhiri Ali*, Paille Bruno*, Urard Pascal*, Pétrot Frédéric
Quantization Modes for Neural Network Inference: ASIC Implementation Trade-offs
International Joint Conference on Neural Networks (IJCNN 2023), 2023
**STMicroelectronics [Crolles]*
Feliu Josué*, Perais Arthur, Jiménez Daniel A., Ros Alberto*****
Rebasing Microarchitectural Research with Industry Traces
IEEE International Symposium on Workload Characterization (IISWC 2023)
**UPV - Universitat Politècnica de València, **Texas A&M University [College Station], ***Universidad de Murcia*
Morgan Fearghal*, Bakó László, O'Loughlin Declan*, George Roshan*, Beretta Arthur*, Rousseau Frédéric, Gallivan Ian*, Timlin-Canning Niall*, Bupathi Abishek*, Byrne John Patrick*, Callaly Franck***
Vicilogic: Linking Online Learning, Assessment and Prototyping with Remote FPGA
International Conference on Remote Engineering and Virtual Instrumentation (REV 2023), 2023
**NUI - National University of Ireland [Galway], **Hungarian University of Transylvania*

Book chapters

Wicaksana Arief, Muller Olivier, Rousseau Frédéric, Sasongko Arif
Cohérence des communications lors de la migration de tâches matérielles
Systèmes multiprocesseurs sur puce 1 - Architectures, pp. 309-343, 2023
Faravelon Antoine, Gruber Olivier*, Pétrot Frédéric
Élimination des appels externes des accès mémoire dans la traduction binaire dynamique
Systèmes multiprocesseurs sur puce 1 - Architectures, pp. 171-203, 2023
**Laboratoire d'Informatique de Grenoble*
Vianes Arthur, Rousseau Frédéric
Méthodes matérielles de distribution des accès en banc mémoire
Systèmes multiprocesseurs sur puce 1 - Architectures, pp. 205-240, 2023
Pinzari Ana, Baumela Thomas, Andrade Porras Liliana Lilibeth, Coppola Marcello*, Pétrot Frédéric
Power Optimized Wafermap Classification for Semiconductor Process Monitoring
Embedded Artificial Intelligence, pp. 1-13, 2023
**ST-GRENOBLE - STMicroelectronics [Grenoble]*

Books & Edited Publications

Andrade Porras Liliana Lilibeth, Rousseau Frédéric
Systèmes multiprocesseurs sur puce 1 - Architectures
, ISTE - International Scientific and Technical Encyclopedia, 2023
Andrade Porras Liliana Lilibeth, Rousseau Frédéric
Systèmes multiprocesseurs sur puce 2 - Applications
, ISTE - International Scientific and Technical Encyclopedia, 2023

Other communications

Bacou Mathieu*, Chader Adam*, Deshpande Chandana S., Fabre Christian, Fuguet César**, Michaud Pierre***, Perais Arthur, Pétrot Frédéric, Thomas Gaël*, Tomasi Ribeiro Eduardo, Tomasi Ribeiro Eduardo****
128-bit Addresses for the Masses (of Memory and Devices)
Workshop on Hot Topics in System Infrastructure (HotInfra 2023), Orlando, UNITED STATES
**Télécom SudParis, **Laboratoire d'Intégration des Systèmes et des Technologies, ***IRISA - Institut de Recherche en Informatique et Systèmes Aléatoires*
Ravenel Pierre, Ravenel Pierre*, Perais Arthur, Dupont De Dinechin Benoît*, Pétrot Frédéric
A gem5-based CVA6 Framework for Microarchitectural Pathfinding
RISC-V Summit Europe 2023, Barcelona, SPAIN
**Kalray*
Tomasi Ribeiro Eduardo*, Fuguet César*, Fabre Christian*, Pétrot Frédéric
Towards simulation of an unified address space for 128-bit massively parallel computers
RISC-V Summit Europe 2023
**LSTA - Laboratoire Systèmes-sur-puce et Technologies Avancées*
Bacou Mathieu*, Chader Adam*, Deshpande Chandana S., Fabre Christian, Fuguet César**, Michaud Pierre***, Perais Arthur, Pétrot Frédéric, Thomas Gaël*, Tomasi Ribeiro Eduardo, Tomasi Ribeiro Eduardo****
We had 64-bit, yes. What about second 64-bit?
RISC-V Summit Europe 2023, Barcelona, SPAIN
**Télécom SudParis, **Laboratoire d'Intégration des Systèmes et des Technologies, ***IRISA - Institut de Recherche en Informatique et Systèmes Aléatoires*

Laboratory life

Scientific events

Congratulations to Ioana VATAJELU and Mounir BENABDENBI for their HDR theses

Ioana VATAJELU and Mounir BENABDENBI (AMfoRS team) both defended their HDR theses (habilitation to conduct research).

January 24, 2023
Ioana VATAJELU (AMfoRS team)
“Emerging Memories for Dependable Computing”
More information: https://tima.univ-grenoble-alpes.fr/actualites/hdr-thesis-defence-ioana-vatajelu-amfors-team-emerging-memories-dependable-computing

February 07, 2023
Mounir BENABDENBI (AMfoRS team)
“Contributions to the Test, Fault Tolerance and Approximate Computing of System on a Chip”
More information: https://tima.univ-grenoble-alpes.fr/actualites/hdr-thesis-defence-mounir-benabdenbi-amfors-team-contributions-test-fault-tolerance-and-approximate

TIMA Laboratory's 30th anniversary

June 20, 2023

TIMA Laboratory has celebrated its 30th anniversary on June 20, 2023.

This was a day of science and conviviality, to present our history and our future projects.

Round table: a number of industry leaders have shared their perspectives on the challenges facing the electronics industry, its technological obstacles and its development in Europe, France and the Grenoble area.

Thank you to our panelists, from left to right:
M. Jean-René LÈQUEPEYS – CEA
M. Yannick TEGLIA – Thalès
M. Philippe MAGARSHACK - ST Microelectronics
M. Benoit DUPONT DE DINECHIN – Kalray
M. Daniel SAIAS – Asygn

All former TIMA directors honoured us with their presence.

From left to right:
M. Bernard COURTOIS: TIMA-CMP director from 1994 to 2006
Mrs Dominique BORRIONE: TIMA director from 2007 to 2014
M. Salvador MIR: TIMA director from 2015 to 2020
M. Giorgio DI NATALE: current TIMA director since 2021

TIMA welcoming newcomers and PhD day

November 30, 2023

TIMA PhD day has taken place in amphitheater C (Grenoble INP).

TIMA doctoral students had the opportunity to present themselves (studies / past work experience, thesis subject, presentation of their native country).

Social life / Quality of life at work (QWL)

Team building around Grenoble

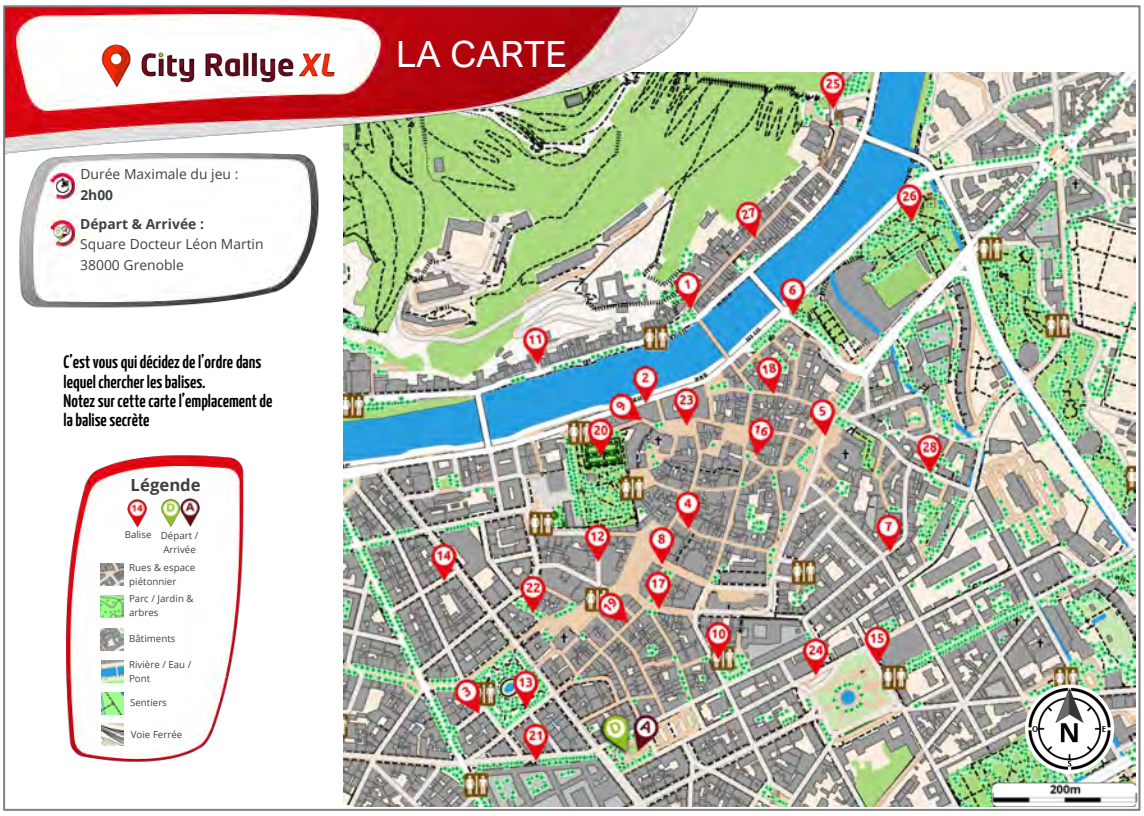
June 26, 2023

A conviviality day has been organized on June 26th, 2023.

It was a great rally in the town of Grenoble.

There were 8 teams of 5 people.

They had to walk around the city, with challenges to complete and places to guess.



A step ahead of 2024 …

Here are some news of early 2024 we can't wait to announce in the next annual report !

Congratulations to Michele PORTOLAN for his HDR these

Michele PORTOLAN (AMfoRS team) has defended his HDR these (habilitation to conduct research) on March 19th, 2024

"Evolutions of the Software Flow for Automated Testing"

https://tima.univ-grenoble-alpes.fr/news/hdr-thesis-defence-michele-portolan-amfors-team-evolutions-software-flow-automated-testing

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