TIMA Laboratory


# 2022

## Annual report

# Contents



# TIMA's staff

**Since 01/01/2021**

**Giorgio DI NATALE**
Director

**Laurent FESQUET**
Deputy Director

## Administrative and Financial pole

**Anne-Laure FOURNERET** (until 16/08/2022)
**Viviana GIORDANO** (from 01/09/2022)
Manager - Human resources - Special events – Communication

**Laurence BEN TITO**
Executive & laboratory assistant - Publications

**Mathilde GARÇON** (until 31/07/2022)
Budgets, contracts

**Aurore GAYRAUD**
Teams finance administrator

**Youness RAJAB**
Teams finance administrator - Common expenses administrator
Budgets, contracts (from 16/05/2022)

## Computer Service

**Frédéric CHEVROT**
Manager - Systems, networks and park manager

**Nicolas GARNIER**
Systems, networks and park manager

**Ahmed KHALID**
Computer park manager

## Development Service

**Adrien PROST-BOUCLE** (from 01/01/2022)
Manager

**Alice DE BIGNICOURT**
Development engineer, webmaster

**Mamadou DIALLO**
Development engineer

**Christelle RABACHE** (from 01/07/2022)
Development engineer

# Foreword

TIMA Laboratory is a joint research laboratory between the Centre National de la Recherche Scientifique (CNRS), the Grenoble Institute of Technology (Grenoble INP) and the Université Grenoble Alpes (UGA).

TIMA addresses some of the most urgent and ambitious challenges related to the design of integrated circuits and Systems-on-chip (SoC). The research activities cover the specification, design, verification, test, CAD tools and design methods for integrated systems, including analog and digital components, smart sensors and actuators, up to multiprocessor SoCs together with their operating system. More in particular, researchers at TIMA cover the following topics:

- Low power design
- Asynchronous design
- New sampling and data processing techniques
- MEMS, Smart Sensors and Actuators
- Design of AMS/RF/mmW devices, circuits and systems
- Modeling, control and calibration of AMS/RF devices, circuits and systems
- Robustness, reliability and test
- Hardware security and embedded trust
- New hardware computing and digital design
- Hardware/Software co-design
- Simulation and verification
- Embedded AI

The laboratory is structured in the following four research teams:

**Architectures and Methods for Resilient Systems (AMfoRS)**: Robustness and dependability evaluations of embedded systems; Hardened and robust architecture; Design for reliability with respect to variability, aging, and soft errors; Modeling, analysis and testing at the system level; Hardware security and embedded trust; New computational approaches and technologies

**Circuits, Devices and System Integration (CDSI)**: Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

**Reliable RF and Mixed-signal Systems (RMS)**: Design for test of analog, mixed-signal and RF circuits; Estimation of test metrics; Calibration of RF devices; Embedded control for efficient energy management; Prediction and control of quality and energy management; High-level modeling of heterogeneous and multi-physic systems

**System Level Synthesis (SLS)**: Highly efficient architectures for general purpose computing or AI-dedicated algorithms; system-level modeling and design methodology (specification, simulation and verification of hardware/software systems on chip); design exploration and synthesis of hardware

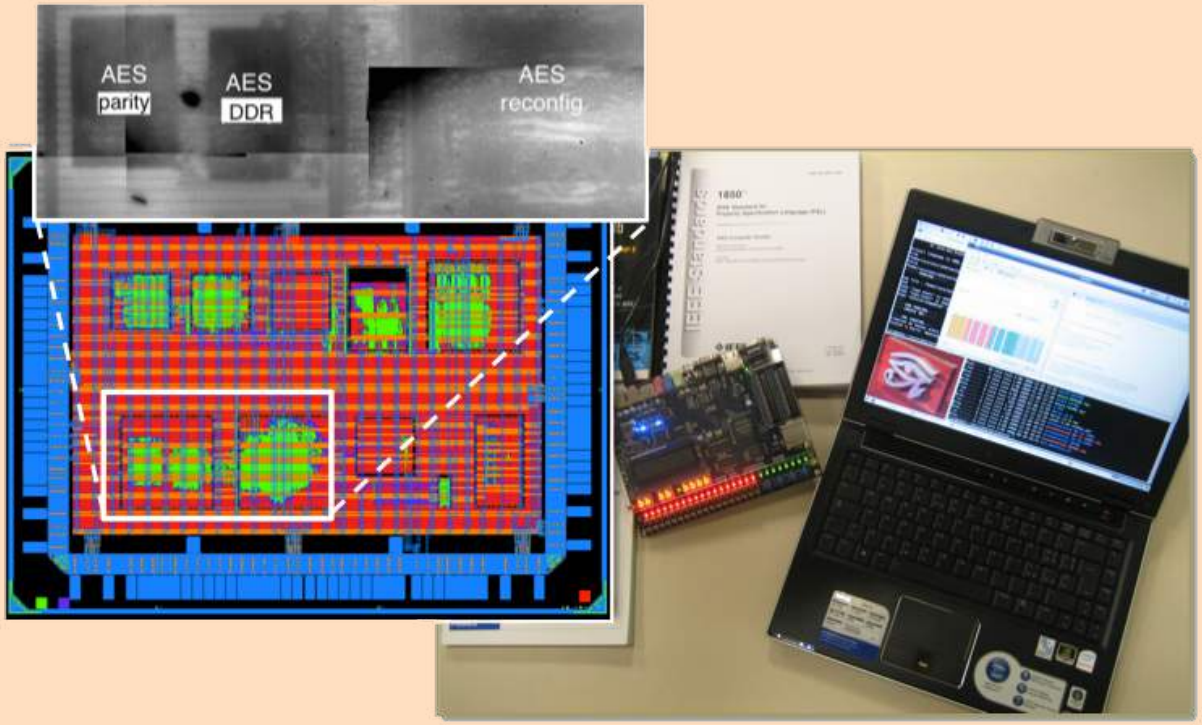
TIMA takes an active part in the organization of the Grenoble Alpes research community, being linked to the poles "Mathematics, Informatics and Communication" (MSTIC) and "Physics, Engineering and Materials" (PEM). TIMA is also a member of the Carnot Institute LSI, the Laboratory of Excellence Persyval and the local federation of micro and nanoelectronics laboratories FMNT.

The 2022 edition of the TIMA annual report presents a brief and synthetic presentation of the scientific achievements of each research team.

Giorgio DI NATALE
Director since 01/01/2021

TIMA
CNRS — GRENOBLE INP — UGA

# AMfoRS team




## Architectures and Methods for Resilient Systems

# Architectures and Methods for Resilient Systems (AMfoRS team)

http://tima.univ-grenoble-alpes.fr/tima/fr/amfors/amforsoverview.html

The **AMfoRS** team addresses dependability and trust of digital systems at multiple abstraction levels for specific application domains (e.g., automotive, avionics, smartcards, IoT), by guaranteeing that digital circuits possess properties such as quality, reliability, safety, security, availability. The work of the team is focused on design and analysis methods, techniques and tools to assess and improve circuits dependability and trust, for the above-mentioned domains.

## Research activities

### Robustness and dependability

Many domains have functional safety among the classical list of design constraints e.g., ISO 26262 standard in automotive. Our work aims at improving **early evaluations of dependability** w.r.t. errors induced by environmental disturbances. The goal, to reduce development and production costs, is to be able to evaluate accurately and at an early stage of the design the potential functional effects of soft and permanent errors. We have recently proposed a **cross-layer fault simulation method** to perform the robustness evaluation of critical embedded systems, based on fault injections in both Transaction Level Model (TLM) and Register Transfer Level (RTL) descriptions to make a trade-off between simulation time and realism of the simulated high level faulty behaviors, Another important characteristic of the approach is taking into account the global system specifications in order to discriminate actually critical faults from faults leading to effects with no real consequences on the system behavior. The approach has been applied to an airborne case study. In 2021, the approach has been improved with an iterative flow allowing both the global reduction of the fault injection durations and the improvement of the TLM models along the iterations in order to achieve a good correlation between the consequences of faults injected at TLM and RTL levels.

Another study started in 2021 aims at better evaluating (and predicting) the impact of the software workload on the dependability of complex digital components such as microcontrollers and SoCs. Ultimately, one goal is to define a set of representative benchmarks, allowing a dependability evaluation on critical systems before the actual application program is available. The first step was to develop a versatile profiling tool based on a virtual platform adapted to many processors, coresponding to a modified version of QEMU. This analysis flow has been applied on the RISC-V target and Mibench softwares, allowing us to better understand the impact of software load on SoC fault tolerance. Our proposed metric called “Likelihood Percentage” demonstrated that a high level evaluation with our tool can be very efficient to obtain significant information on program behaviour, coherent with results obtained from both a reference instruction set simulator and a hardware architecture. We have also shown that our profiling tool allows us to compare the behaviour of several programs and exhibits specific characteristics. This data helps in understanding how the processor architecture will be used for each application and therefore what level of fault tolerance can be expected depending on the software load. We formulated three hypotheses that will have to be confirmed with more program examples, the use of several hardware platforms and finally actual tests under particle beams.

In the field of automatic quality or safety assurance level evaluation, we have proposed the first approach towards the automation of the extraction processes of both the valid and faulty state machines within a System-on-a-Chip. The data automatically extracted by this method is a relevant input for behavioural modelization and FMEA (Failure Modes and Effects Analysis) analysis. The method is based on a semi-automated approach for the systematic extraction of failure modes of a digital design in the hypothesis of a single-event upset (SEU) or stuck-at in flip-flops. This procedure aims to enhance human driven failure analysis and provide inputs for RAMS (Reliability, Availability, Maintainability, and Safety) frameworks in the process of quality assurance of complex devices. The main objective is to transport and apply RAMS methods and tools in the area of SoCs design. Experimental results have been conducted on an I2C - AHB system, laying the base for a complete and more complex analysis on an entire SoC [CI3]

Due to technology scaling and transistor size getting smaller and closer to atomic size, the last generation of CMOS technologies presents more variability in various physical parameters. Moreover, circuit wear-out degradation leads to additional temporal variations, potentially resulting in timing and functional failures. To handle such problems, one conventional method consists in providing more safety margins (also called guard bands) at design-time. Therefore, the usage of delay violation **monitors** becomes a must. Placing the monitors is a critical task as the designer has to carefully select the place that will age the most and may become a potential point of failure in a given design.

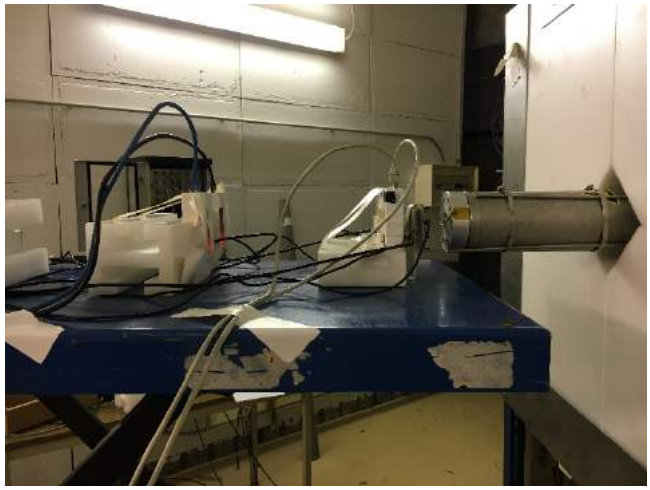
We have explored the use of **Machine Learning techniques** in order to drive the automated selection of potential insertion points of such monitors. Digital delay analysis of basic gates using multiple linear regression has been modeled, predicted, and validated against original data using spice simulation. We have compared multiple linear regression algorithms and used them to study the aging mechanism of CMOS basic gates using supervised learning algorithms. We have showed how it is possible to reliably estimate activity-related path aging and tune the prediction framework by extracting activity profiles from simulations on a synthesized design, which allows a finer grain estimation by obtaining activity profiles at both the path and gate-level.

### High-energy particle radiation effects in computing systems

In space environments, aviation altitudes, and ground levels, computing systems' components are liable to high-energy particle radiation-induced transient, accumulative, permanent, and destructive effects. At atmospheric altitudes, for example, neutron environment is primarily responsible for inducing radiation-induced transient effects in avionics and their computing systems. Moreover, the advent of artificial intelligence (AI) systems further extends the computing system applications with self-driving cars, climate-smart agriculture technologies, intelligent medical devices, autonomous monitoring robots/drones, nanosatellites, and spacecraft, making them even more ubiquitous. Within the new era of autonomous things, AI computing solutions are being developed also for the edge of applications, close to sensors, in order to minimize data transfer to/from the cloud and reduce related risks in case of unavailable connections. On the other hand, edge computing is normally resource-constrained in terms of latency, power, and memory, demanding the development of tiny and also reliable machine learning (ML) systems.

In this context, our recent works have assessed and compared the effectiveness of three prominent ML algorithms for tiny ML computing systems in tolerating neutron-induced soft errors. Radiation test-based results suggest that the case-study ML algorithms retain a certain intrinsic level of effectiveness in tolerating neutron effects even thought without any mitigation technique. Notably, random forest algorithm has performed no misclassification during different radiation testing campaigns carried out with 14-MeV and thermal neutron beams.

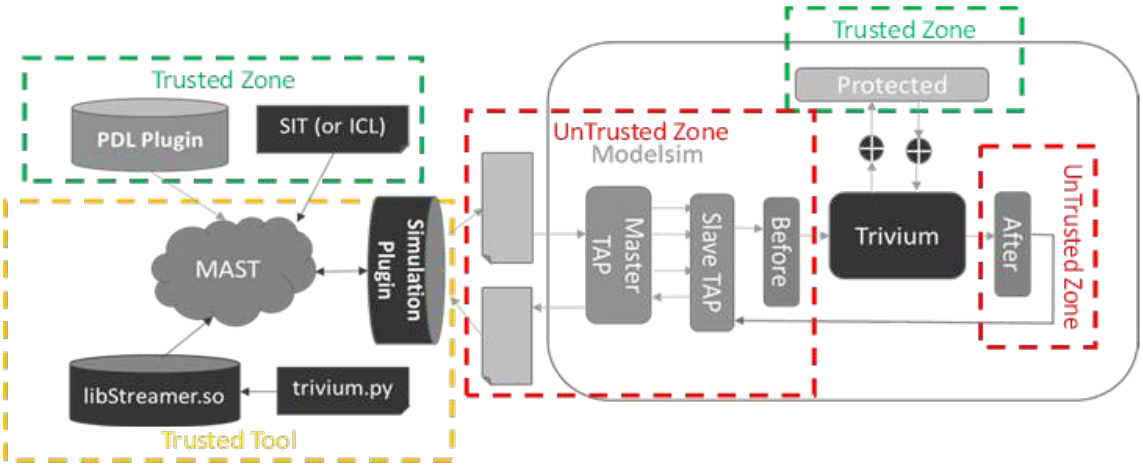
Furthermore, we have also recently assessed neutron radiation effects on the attitude estimation (AE) processing typically embedded in inertial navigation systems (INS) and modern autonomous things. Findings highlight the importance of radiation-induced critical failures that are able to upset INS embedding AE processing modules. Radiation tests were conducted running three strategies for computing different advanced AE algorithms on a case-study processing module exposed to 14-MeV neutron and thermal neutron radiation. Results and analysis suggest that the contribution of radiation-induced soft errors to be mitigated on the AE processing modules is essentially related to single event functional interrupts that can lead inertial navigation to critical failures.



TIMA is also participating of NASA/GFSC's SET program (https://lws-set.gsfc.nasa.gov/) since 2005. The experimental FPGA-based board called COTS-2, devised and designed at TIMA, was included in the NASA/GFSC's SET payload, embedded in the AFRL's DSX spacecraft that was successfully launched on June 25, 2019 at the NASA's Kennedy Space Center (Florida, USA). The DSX spacecraft was in operation until May 31, 2021, weekly providing data to TIMA researchers since June 2019. The NASA/GFSC's SET payload aimed at getting experimental data to study how to better protect satellites/spacecraft against effects of energetic radiation particles present at a medium Earth orbit (MEO) of space, operating around Earth between 6000 km and 12000 km above sea level. The TIMA's COTS-2 board includes an SRAM-based FPGA in which the implemented computing system design was protected by using a classical state-of-the-art fault-tolerance scheme based on Triple Modular Redundancy (TMR). First spaceflight results provide experimental evidences of the risks of using TMR-based schemes in COTS FPGAs operating within MEO.

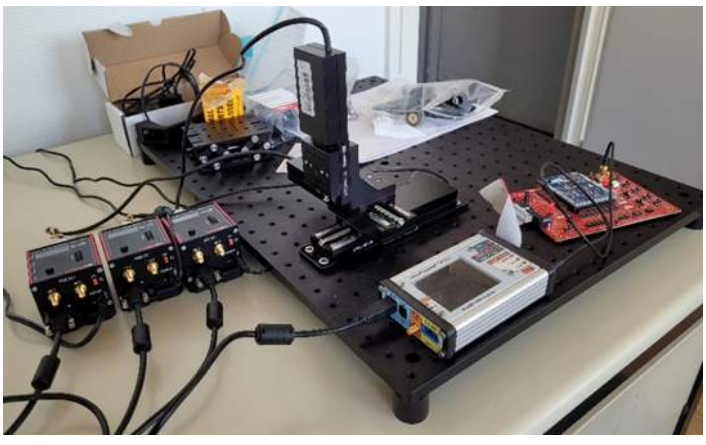
## System-level test and standards

The IEEE 1687-2014 standard and its evolutions like the IEEE P1687.1 (under development) propose solutions for the access and usage of Embedded Instruments, but Electronic Design Automation (EDA) is still limited to only a small subset of the new features. In this context we have improved our innovative Test Flow and Environment called **"Manager for SoC Test" (MAST)**, a software backend able to provide features and performance superior to the industrial legacy solutions. We have proposed innovative solutions that exploits the dynamic nature of the standard to integrate Security features directly into the flow. Our framework extends MAST with novel solutions developed within the team, namely Stream cyphers and Dynamic authentication. We were notably able to integrate Scan Encryption directly inside the EDA tool, allowing Encryption to be natively integrated as a P1687.1 element and be freely mixed inside the Design-of-Test (DfT) infrastructure while retaining full interactive capabilities, while legacy solutions are limited to top-level encryption with offline processing. We then merged this new feature with the ongoing work on Scan Authentication, obtaining the Encryption SIB (eSIB, see Hardware Security and Trust), an Authentication-based Secure Access framework able to provide a trusted, configurable, efficient, and transparent interface to the test infrastructure depending on user-defined security levels. Security-wise, secret sharing is limited to a minimum; from a performance point of view, the tool fully leverages its strength in terms of topology resolution and concurrent execution. Last but not least, we are able to clearly separate the system in Trusted and Untrusted areas, providing an optimal user experience, as se curity is handled automatically and transparently.




## Hardware security

The team works on the design of cryptographic/secure primitives, and the analysis of security threats, by proposing effective countermeasures. We work on algorithms, schemes, and protocols. We have improved our Authenticated and Secure access to the test infrastructure by presenting the **Encryption SIB**, which provides segment-level confidentiality thanks to the dynamic topology supported by our MAST tool (see System-Level test). Our framework not only supports secure procedures such as user authentication or data encryption, but provides these functionalities with a flexible approach that is totally transparent to the user. We also evaluate the resistance of post-quantum cryptography algorithms against physical attacks, which is necessary besides their theoretical evaluation by cryptanalysis. We highlighted a weakness in the Classic McEliece cryptosystem, which can be attacked by laser fault injection. We are working right now on extending this attack to rely only on side-channel analysis, which incurs a much less restrictive attacker model.



Concerning the security threats, we work regularly on implementation attacks. In 2021, we have improved our experimental platform for **physical attacks** on embedded systems. We have acquired the equipment for active EM fault injection and we are currently building a motorized stage to perform extensive experimental campaigns, thanks to the partial support by CNRS (INS2I) and UGA. We have also worked on an emulation platform on FPGA, aimed at evaluating the effects of EM Fault Injection (EMFI) early in the design flow without the need of either EMFI equipment, nor the final ASIC implementation. In an effort to generalize the characterization of fault attacks on complex systems such as CPUs and microcontrollers, we have started working on a **Cross-Layer Methodology** aiming

at understanding and modelling the fault occurrence mechanisms within the microarchitecture of modern processors, and map this model to upper levels with the final goal of designing optimal countermeasures.
We have addressed the problem of cache timing attacks, which have become very popular in recent years. Eviction set construction is a common step for many such attacks, and algorithms for building them are evolving rapidly. On the other hand, countermeasures are also being actively researched and developed. However, most countermeasures have been designed to secure last-level caches and few of them actually protect the entire memory hierarchy. Cache randomization is a well-known mitigation technique against cache attacks that has a low-performance overhead. We have proposed solutions to determine whether address randomization on first-level caches is worth considering from a security perspective. The work included the implementation of a noise-free cache simulation framework that enables the analysis of the behavior of eviction set construction algorithms. We show that randomization at the first level of caches (L1) brings about improvements in security but is not sufficient to mitigate all known algorithms, such as the recently developed Prime–Prune–Probe technique [CI-14]
In the same context, a study has first shown that Intel mitigations to avoid attacks against secure enclaves (SGX) can be efficient, but not sufficient in all attack scenarios. We have also evaluated the feasibility of the Prime&Probe attack on a system with the CVA6 RISC-V processor. With a bare-metal implementation, it has been shown that the attack works, although a noticeable effort was necessary in terms of reverse engineering of the cache accesses and analysis of the behavior. An attack considered as “turnkey” is not so easy to implement, even without mitigations. Adding additional processes as perturbators, the attack is more complex but still succeeds after analysis of the cache behavior. Currently, work is on-going with the attack implemented under Linux.
In the context of **Control Flow Hardening**, we have proposed the use of nonlinear codes. Hardware-based control flow monitoring techniques enable to detect both errors in the control flow and the instruction stream being executed on a processor. However, these techniques may fail to detect malicious carefully tuned manipulation of the instruction stream in a basic block. We have shown how using a non-linear encoder and checker can cope with this weakness [RI-8]

### Hardware trust

The quest of low production cost and short time-to- market, as well as the complexity of modern integrated circuits pushed towards a globalization of the supply chain of silicon devices. Such production paradigm raised a number of trust threats. We are actively working on the proposition of novel solutions to address this problem. In particular, we are proposing novel methods, architectures and protocols for the identification and authentication of hardware devices based on Physically Unclonable Functions (PUFs), as well as mitigation techniques for Hardware Trojans.

Concerning the PUFs, we have proposed: (i) an experimental platform for the evaluation of SRAM-based PUFs; (ii) a theoretical method for the assessment of the reliability of PUFs; (iii) the use of emerging technologies (resistive and magnetic memories) as building block for new PUF architectures; (iv) a novel concept for the enrollment of strong PUF based on machine learning; (v) a new protocol for key exchange which does not require cryptographic primitives [CI-8] [O-1]
In the context of Hardware Trojans (HTs), we worked on the use of software obfuscation to protect systems against HTs that aim at stealing information from the microprocessor while it is executing a program. The method is enhanced by a Genetic Algorithm-based approach to optimize the obfuscation level while minimizing the introduced overhead. We proved the effectiveness and efficiency of the proposed methodology on the Ariane 64bit RISC-V microprocessor running a set of MiBench benchmarks and cryptographic programs.
We also proposed an HT attack for analog circuits, in the context of Systems-on-Chip (SoCs) comprising both digital and analog Intellectual Property (IP) blocks. The HT trigger is placed inside a dense digital IP block where it can be effectively hidden, whereas the HT payload is in the form of a digital pattern transported via the test bus or generated within the test bus, reaching the Design-for-Test (DfT) or programmability interface of the victim analog IP with the test bus. The HT payload unexpectedly activates the DfT and sets the victim analog IP into some possibly partial and undocumented test mode or changes the nominal programmability [RI-3].

### New hardware computing approaches

Today's computing systems are facing several issues related to architectural and technological limitations. To mitigate these issues, novel computing paradigms, such as **Computing-in-Memory**, **Neuromorphic Computing** and **Approximate Computing**, are being researched, in conjunction with novel emerging technologies such as memristive and spintronic devices. Concerning these devices, our research aims at using enhanced compact models to perform failure analysis, and define pertinent fault models to establish design-for-test and design-for-reliability methodologies. Concerning the Computing-in-Memory paradigm, we are investigating feasible design solutions, with a special focus on applications for security [CI-10] [CI-13]. Concerning Neuromorphic Computing, we are focusing on the design of efficient Spiking Neural Networks with on-line unsupervised learning and the reliability analysis and test of such networks. Concerning the Approximate Computing paradigm, which has been gaining momentum both in the industry and in academia, we are studying the trade-offs between selective approximation (or occasional violation of specifications) and power consumption. We have focused on Floating Point dynamic approximation, with an impact evaluated i) at algorithm and application level and ii) at hardware level with the design of a configurable FPU ([RI-2] and [RI-9]) . We are also working on an extension of a tool initially developed for dependability evaluation (EARS) in order to identify from RTL descriptions the operators that are the less sensitive to approximations for a given application. In 2021, EARS has been modified to include new metrics and also to better link the multi-bit elements in the RTL description (e.g., operators) to the analysis results. Several benchmarks have also been prepared; the next step is to compare the results of EARS with the results of the manual benchmarks analyses.

### Involvement in research activities:

- Participation to the IEEE P1687.1 Working Group
- Participation to the Grenoble Alpes CyberSecurity Institute
- Chair of TTTC – IEEE Computer Society
- Chair of TTEP Educational Program of TTTC
- In charge of Microelectronics within FMNT

### Platforms and demonstrators:

- A comprehensive platform for hardware/software co-design based on the RISC-V processor architecture. The platform supports several RISC-V implementations (such as the Rocket Chip or CVA6) and it features high modularity and tuning capabilities (https://tima-amfors.gricad-pages.univ-grenoble-alpes.fr/learnv/).
- Hardware demonstrator for Secure Access to 1687 Test Infrastructure
- Experimental platforms for Physical Attacks and PUF evaluation
- Emulation platform for EM Fault Injection
- Accelerated radiation testing platform for assessing computing systems under high-energy neutron radiation effects

## Recent highlights

### International Cooperation

**Infrastructure for Secure, Reliable, and Low-Power Computing Systems**
Scientific Manager: Rodrigo POSSAMAI BASTOS
Partners: PUCRS (Pontifícia Universidade Católica do Rio Grande do Sul)
City: Porto Alegre
Country: BRAZIL
Start the: Nov 01, 2018 until Oct 31, 2022

### April 26, 2022: My thesis in 180 seconds (MT 180): Salah DADDINOUNOU in the regional final

Our student Salah DADDINOUNOU reached the regional final with his thesis:
“Test and reliability of impulse neural networks based on emergent memories". mémoires émergentes”.
https://youtu.be/G4ON_TiShtI
https://www.linkedin.com/feed/update/urn:li:activity:6924654329329012736/
My thesis in 180 seconds is an opportunity for doctoral students to present their research topic in French and in simple terms, to a novice and diverse audience diverse audience - https://mt180.fr/

### May 26, 2022: ETS 2022 PhD Forum Contest Award for Sergio VINAGRERO GUTIERREZ

Congratulations to Sergio VINAGRERO GUTIERREZ for receiving the ETS 2022 PhD Forum Contest Award for his work on Memristor-Based Security Primitives


### June 6, 2022: Project MITI 80 PRIME CNRS : Memristors find new use in neural networks

More details: https://www.minatec.org/en/memristors-find-new-use-in-neural-networks/

### June 21, 2022: Scientific Day: Test, Safety and Security of Nano-electronic Systems

These Scientific Days are meant to present the research topics and to disseminate the recent advances of TIMA researchers. These presentations are open to everybody, whether they are members of TIMA or not.
Program: 2022_06_21_amfors_lirmm_test_safety_nanoelectronic_systems_v2.pdf

### September 2, 2022: Congratulations to Ihab ALSHAER for receiving the DSD 2022 Best Paper Award for his work entitled "Variable-Length Instruction Set: Feature or Bug ?"

### September 13, 2022: Michele PORTOLAN elected Secretary of the IEEE 1687-2014 Revision Working Group

# Academic and research members

## Mounir BENABDENBI

**Position**
Associate Professor at Grenoble INP - Phelma school

**Responsibilities**
Researcher in AMfoRS team

## Brice COLOMBIER

**Position**
Associate Professor at Grenoble INP - Phelma school until 31/08/2022

**Responsibilities**
Researcher in AMfoRS team until 31/08/2022

## Giorgio DI NATALE

**Position**
Research Director at CNRS

**Responsibilities**
Researcher in AMfoRS team
Director of TIMA Lab. Since 01/01/2021

## Régis LEVEUGLE

**Position**
Professor at Grenoble INP - Phelma school

**Responsibilities**
Researcher in AMfoRS team

## Paolo MAISTRI

**Position**
Researcher at CNRS

**Responsibilities**
Leader of AMfoRS team
Researcher in AMfoRS team

## Mihail NICOLAIDIS

**Position**
Research Director at CNRS

**Responsibilities**
Researcher in AMfoRS team

## Michele PORTOLAN

**Position**
Associate Professor at Grenoble INP - Phelma school

**Responsibilities**
Researcher in AMfoRS team

## Rodrigo POSSAMAI BASTOS

**Position**
Associate Professor at UGA - IM2AG school

**Responsibilities**
Researcher in AMfoRS team

## Elena-Ioana VATAJELU

**Position**
Researcher at CNRS

**Responsibilities**
Researcher in AMfoRS team

## Raoul VELAZCO

**Position**
Emeritus research Director at CNRS

**Responsibilities**
Researcher in AMfoRS team

## Nacer-Eddine ZERGAINOH

**Position**
Associate Professor at UGA - Polytech school

**Responsibilities**
Researcher in AMfoRS team

*CNRS (French National Center for Scientific Research)*
*Grenoble INP (Grenoble Institute of Technology)*
*IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)*
*PHELMA school (Physique-Electronique-Matériaux)*
*POLYTECH school (École Polytechnique de l'Université Grenoble Alpes)*
*UGA (Université Grenoble Alpes)*

## Ph. D. candidates

### 1. ALI POUR Amir
Title of thesis: **PUF based Secure Computing for Resource Constraint Cyber Physical Object**
Completed on: **December 8, 2022**
Previous degrees: Engineer (2020)

### 2. ALSHAER Ihab
Title of thesis: **Cross-Layer Fault Analysis for Microprocessor Architectures (CLAM)**
Expected date of defense: **2023**
Previous degrees: Engineer

### 3. BOULIFA Roua
Title of thesis: **Robust and Secure RISC-V Architecture**
Expected date of defense: **2025**
Previous degrees: Master - Université de Tunis - El Manar - Le kef, Tunisia (2022)

### 4. DADDINOUNOU Salah
Title of thesis: **Test and reliability of emerging memory-based spiking neural networks**
Expected date of defense: **2023**
Previous degrees: Master - Université Paris-Sud Orsay – Paris, France (2019)

### 5. DOUADI Aghiles
Title of thesis: **Design and evaluation of countermeasures against power-off laser fault injection attacks**
Expected date of defense: **2025**
Previous degrees: Master STS - Université de Bourgogne – Dijon, France (2022)

### 6. EL AMRAOUI Sami
Title of thesis: **Fault Injection on** Digital **Circuits: Modelling and Protecting against ElectroMagnetic Pulses**
Expected date of defense: **2025**
Previous degrees: Engineer – INPT (Institut National des Postes et Télécommunications) – Rabat, Moroco (2022)

### 7. FIORUCCI Tiziano
Title of thesis: **Qualification methodology for ISO26262 certification of automotive SoC systems**
Expected date of defense: **2023**
Previous degrees: Master - Università degli Studi di Roma Tor Vergata - Roma – Italy (2019)

### 8. INGLESE Pietro
Title of thesis: **Exploration of security threats in In-Memory Computing Paradigms**
Expected date of defense: **2023**
Previous degrees: Engineer – Politecnico di Torino - Italy (2019)

### 9. JAAMOUN Amine
Title of thesis: **Strategies for securing a memory hierarchy against software side channel attacks**
Completed on: **December 12, 2022**
Previous degrees: Master 2 Systèmes électroniques et systèmes informatiques – Université Pierre et Marie Curie - Paris 6, France (2020)

### 10. JUSTUS RAJAPPA Anuj
Title of thesis: **Reliable energy efficient machine learning in harsh environments**
Expected date of defense: **2024**
Previous degrees: Master of Science – St Joseph College - Trichy, India (2019)

### 11. KOROLEVA Aleksandra
Title of thesis: **Study and development of La2NiO4 memristive devices for bio-inspired computing**
Expected date of defense: **2025**
Previous degrees: Master of Science - Moscow Institute of Physics and Technology – Russia (2019)

### 12. KRAEMER SARZI SARTORI Tarso

Title of thesis: **Mitigation of radiation effects on the attitude estimation processing of autonomous things**
Expected date of defense: **2023**
Previous degrees: Master – Aerospace engineering – Federal University of Santa Maria, Brazil (2020)

### 13. MARTINOLI Valentin

Title of thesis: **Secure Processors with respect to Micro Architectural Attacks**
Expected date of defense: **2023**
Previous degrees: Engineer – Ecole des Mines – Saint-Etienne / Gardanne, France (2019)

### 14. NOIZETTE Luc

Title of thesis: **Predictive fault tolerance analysis methodology for complex components with consideration of the application**
Expected date of defense: **2024**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2020)

### 15. OULDEI TEBINA Nasr-Eddine

Title of thesis: **Sensitivity Analysis and Design Methodology for Secure Digital Circuits against X-Rays**
Expected date of defense: **2024**
Previous degrees: Master - Université de Montpellier Montpellier, France (2020)

### 16. SUZANO DA FONSECA Juan

Title of thesis: **3D Heterogeneous technologies for Digital secured & sovereign solutions**
Expected date of defense: **2025**
Previous degrees: Engineer - CPE Lyon, France (2021)

### 17. TALY Emilien

Title of thesis: **Design of a very low power Artificial Intelligence system (Tensor Processing Unit - TPU) based on memory computation**
Expected date of defense: **2024**
Previous degrees: Master – Université de Montpellier, France (2020)

### 18. VINAGRERO GUTIERREZ Sergio

Title of thesis: **Design and Evaluation of Resistive-based Security Primitives (Physically Unclonable Function & True Random** Number **Generator)**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA (Université Grenoble Alpes), France (2021)

## Other members

### Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. SHIMOU | Yasser | MOROCCO | 3 months |

### Visitors

No positions in 2022

### Trainees

| | | | |
|---|---|---|---|
| 1. ALVES DOS SANTOS | Guilherme Akira | BRAZIL | 2 months |
| 2. BURGHOORN | Gijs Juurd | NETHERLANDS | 7 months |
| 3. CAMPONOGARA | Luis Felipe | BRAZIL | 5 months |
| 4. CAO | Yiheng | FRANCE | 6 months |
| 5. CHARLES | Matthieu | FRANCE | 2 months |
| 6. CORREA CUETO | Marcelo | BRAZIL | 6 months |
| 7. DEGREZE | Arnaud | FRANCE | 5 months |
| 8. EL AMRAOUI | Sami | FRANCE | 5 months |
| 9. EL AYAT | Rami | FRANCE | 2,5 months |
| 10.GORCHS PICAS | Marti | SPAIN | 4 months |
| 11.KACI CHAOUCHE | Mohand | FRANCE | 1 month |
| 12.LAURINI | Luiz Henrique | BRAZIL | 10 months |
| 13.LE BARS | Gwenvael | FRANCE | 4,5 months |
| 14.MANNAA | Sara | LEBANON | 6 months |
| 15.MEZAOULI | Mohammed | FRANCE | 3 months |
| 16.ROUGIER | Florent | FRANCE | 1,5 months |
| 17.SANTOS DUARTE | Jardel Kaique | FRANCE | 5 months |
| 18.SARTONI | Sandro | ITALY | 3 months |
| 19.SUAU | Paul | FRANCE | 2 months |
| 20.TARDY | Clément | FRANCE | 2 months |

## Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2022.

### ANR

**CAD4RMD (2021 – 2022)**
Title: CAD Tool and Design Space Exploration for Resistive-based Memory Devices Integration in non-Von Neuman Architectures
Scientific manager: Ioana VATAJELU

**EMINENT (2019 – 2023)**
Scientific manager: Ioana VATAJELU

**EM2G (2021 – 2022)**
Title: EMulation de fautes EM par Glitch d'horloge locaux
Scientific manager: Paolo MAISTRI

**EPOQAP (2021 – 2022)**
Title: Évaluation des algorithmes de cryptographie post-quantique contre les attaques physiques
Scientific manager: Brice COLOMBIER

**POP (2021 – 2025)**
Title: Attaque laser de primitives de sécurité non alimentées
Scientific manager: Brice COLOMBIER

### ANRT

**CIFRE Antoine LINARES (2020 – 2023)**
Title: Flexible Hardware for Intrinsic Secure Computing
Scientific manager: Giorgio DI NATALE
Industrial partner: SiFive

### EPST

**CLAM (2020 – 2023)**
Program: Equipe-Action Labex Persyval
Title: Cross-Layer Fault Analysis for Microprocessor Architectures
Scientific manager: Paolo MAISTRI

**State (2020 – 2023)**
Scientific manager: Rodrigo POSSAMAI BASTOS

### INDUSTRY

**Processeurs Sécurisés et Attaques de micro architectures (2020 – 2023)**
Scientific manager: Régis LEVEUGLE

### REGION

**MULTIRAD (2020 – 2023)**
Program: Pack Ambition International
Scientific manager: Rodrigo POSSAMAI BASTOS

**SAFE-AIR (2017 – 2022)**
Program: Pack Ambition Recherche
Title: Safety Evaluation of Aircraft Systems using Virtual Platforms
Scientific manager: LEVEUGLE Régis

## Organization and participation of international conferences, workshops, forums

**Design, Automation and Test in Europe Conference (DATE'2022)**
March 14-23, 2022, Virtual event
Rank: A+
proceeding chair: VATAJELU Elena-Ioana
topic member: DI NATALE Giorgio, VATAJELU Elena-Ioana

**25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS'2022)**
April 6-8, 2022, Prague, CZECH REP.
Rank: B
technical committee: LEVEUGLE Régis, MAISTRI Paolo, PORTOLAN Michele, VATAJELU Elena-Ioana

**27th IEEE European Test Symposium (ETS'2022)**
May 23-27, 2022, Barcelona, SPAIN
Rank: A
program committee: BENABDENBI Mounir, DI NATALE Giorgio, LEVEUGLE Régis
special session chair: DI NATALE Giorgio
steering committee: DI NATALE Giorgio, VATAJELU Elena-Ioana
topic chair: VATAJELU Elena-Ioana

**16ème Colloque du GDR SoC2 (GDR SOC 2'2022)**
June 27-29, 2022, Strasbourg, FRANCE
Rank: NC
animation committee: VATAJELU Elena-Ioana

**28th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2022)**
September 12-14, 2022, Torino, ITALY
Rank: B
emeritus chair: NICOLAIDIS Michael
program committee: DI NATALE Giorgio, LEVEUGLE Régis, PORTOLAN Michele, VATAJELU Elena-Ioana
steering committee: NICOLAIDIS Michael

**IEEE Computer Society Annual Symposium on VLSI (ISVLSI'2022)**
July 4-6, 2022, Nicosia, CYPRUS
Rank: A
technical program committee: DI NATALE Giorgio, VATAJELU Elena-Ioana

**23rd IEEE Latin-American Test Symposium (LATS'2022)**
September 5-8, 2022, Montevideo, URUGUAY
Rank: NC
general chair: VELAZCO Raoul

**17th ACM International Symposium on Nanoscale Architectures (NANOARCH'2022)**
December 7-9, 2022, Virtual event
Rank: B
technical committee: VATAJELU Elena-Ioana

**10th Prague Embedded Systems Workshop (PESW'2022)**
June 30-July 2, 2022, Horoměřice, CZECH REP.
program committee: DI NATALE Giorgio, VATAJELU Elena-Ioana

**11th International Workshop on Security Proofs for Embedded Systems (PROOFS'2022)**
September 22, 2022, Leuven, BELGIUM
program committee: DI NATALE Giorgio

**18th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA'2022)**
December 5-9, 2022, Zurich, SWITZERLAND
co-general chair: VELAZCO Raoul

**Test Spring School (TSS'2022)**
May 20-23, 2022, Barcelona, SPAIN
program chair: VATAJELU Elena-Ioana

**40th IEEE VLSI Test Symposium (VTS'2022)**
April 25-27, 2022, San Diego (CA), USA
steering committee: NICOLAIDIS Michael

## Responsibilities

| Role | TIMA member | Starts | Ends | Comments |
|---|---|---|---|---|
| **Faculties / Schools** | | | | |
| **Phelma school<br>PHysique – ELectronique - MAtériaux** | | | | |
| Co-responsible of SEI branch | BENABDENBI Mounir | 01/09/2017 | | |
| Manager of SEOC/PHELMA branch | PORTOLAN Michele | 01/09/2017 | | |
| **UFR IM2AG<br>Informatique, Mathématiques et Mathématiques Appliquées** | | | | |
| Manager of Office Automation and Informatics | POSSAMAI BASTOS Rodrigo | 01/09/2017 | | Formation à tous les parcours du Département Licence Sciences et Technologies de l'UGA |
| **TIMA Laboratory** | | | | |
| Parity referent | VATAJELU Elena-Ioana | 01/09/2022 | | |
| Partnership and Development Correspondent | PORTOLAN Michele | 01/09/2022 | | |
| **Research structures** | | | | |
| **CIME Nanotech<br>Centre Interuniversitaire de MicroElectronique et Nanotechnologies** | | | | |
| Manager of Design platform | BENABDENBI Mounir | 01/09/2017 | | |
| **MSTIC pole<br>Mathématiques, sciences et technologies de l'information et de la communication** | | | | |
| Council member of MSTIC cluster | LEVEUGLE Régis | 01/09/2015 | | Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC |

# Scientific production

## International journals (RI)

**RI-1 Kraemer Sarzi Sartori Tarso, Fourati Hassen*, Létiche Manon**, Possamai Bastos Rodrigo**
Assessment of Radiation Effects on Attitude Estimation Processing for Autonomous Things
IEEE Transactions on Nuclear Science, Volume: , pp. 1-1, 2022
**GIPSA-Lab, **ILL - Institut Laue-Langevin*

**RI-2 Possamai Bastos Rodrigo, Garay Trindade Matheus, Garibotti Rafael*, Gava Jonas**, Reis Ricardo**, Ost Luciano****
Assessment of Tiny Machine-Learning Computing Systems under Neutron-Induced Radiation Effects
IEEE Transactions on Nuclear Science, Volume: , pp. 1-1, 2022
**PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, **UFRGS - Université fédérale du Rio Grande do Sul*

**RI-3 Martinoli Valentin, Tourneur Elouan*, Teglia Yannick*, Leveugle Régis**
CCALK: (When) CVA6 Cache Associativity Leaks the Key
Journal of Low Power Electronics and Applications (JLPEA) - Open access, Volume: 13, 2022
**Thalès DIS*

**RI-4 Alshaer Ihab*, Alshaer Ihab, Colombier Brice, Deleuze Christophe*, Maistri Paolo, Beroulle Vincent***
Cross-Layer Inference Methodology for Microarchitecture-aware Fault Models
Microelectronics Reliability, Volume: 139, 2022
**Laboratoire de Conception et d'Intégration des Systèmes*

**RI-5 Cassano Luca*, Iamundo Mattia*, Lopez Tomas Antonio*, Nazzari Alessandro*, Di Natale Giorgio**
DETON: DEfeating hardware Trojan horses in microprocessors through software ObfuscatioN
Journal of Systems Architecture (JSA), Volume: 129, 2022
**Dipartimento di Elettronica, Informazione e Bioingegneria (POLIMI)*

**RI-6 Ali Pour Amir*, Afghah Fatemeh**, Hély David*, Beroulle Vincent*, Di Natale Giorgio, Korenda Ashwija Reddy***, Cambou B.*****
Helper Data Masking for Physically Unclonable Function-based Key Generation Algorithms
IEEE Access, Volume: 10, pp. 40150 - 40164, 2022
**Laboratoire de Conception et d'Intégration des Systèmes, **Clemson University, ***Northern Arizona University*

**RI-7 Benevenuti Fabio*, Goncalves Marcio*, Pereira Jr Evaldo Carlos**, Vaz Rafael**, Gonçalez Odair Lelis**, Possamai Bastos Rodrigo, Létiche Manon***, Kastensmidt Fernanda*, Azambuja José Rodrigo***
Investigating the reliability impacts of neutron-induced soft errors in aerial image classification CNNs implemented in a softcore SRAM-based FPGA GPU
Microelectronics Reliability, Volume: , 2022
**UFRGS - Université fédérale du Rio Grande do Sul, **Instituto de Estudos Avançados, ***ILL - Institut Laue-Langevin*

**RI-8 Jaamoum Amine*, Hiscock T.*, Di Natale Giorgio**
Noise-Free Security Assessment of Eviction Set Construction Algorithms with Randomized Caches
Applied Sciences, Volume: 12, pp. 2415, 2022
**Laboratoire d'Electronique de Technologie de l'Information*

**RI-9 Colombier Brice, Dragoi Vlad-Florin*, Cayrel Pierre-Louis**, Grosso Vincent****
Profiled Side-channel Attack on Cryptosystems based on the Binary Syndrome Decoding Problem
IEEE Transactions on Information Forensics and Security , Volume: , 2022
**Aurel Vlaicu University of Arad, **Laboratoire Hubert Curien*

**RI-10 Ali Pour Amir*, Hély David*, Beroulle Vincent*, Di Natale Giorgio**
Strong PUF Enrollment with Machine Learning: A Methodical Approach
MDPI Electronics, Volume: 11, pp. 653, 2022
**Laboratoire de Conception et d'Intégration des Systèmes*

## International conferences (CI)

**CI-1 Gava Jonas*, Abich Geancarlo*, Garibotti Rafael**, Cuenca-Asensi Sergio***, Possamai Bastos Rodrigo, Reis Ricardo*, Ost Luciano******
A Lightweight Mitigation Technique for Resource-constrained Devices under Neutron Radiation
Conference on Radiation Effects on Components and Systems (RADECS 2022), 2022
**UFRGS - Université fédérale du Rio Grande do Sul, **PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ***Universidad de Alicante, ****Loughborough University*

**CI-2 Maistri Paolo, Po Jia Yun**
A Low-Cost Methodology for EM Fault Emulation on FPGA
Design, Automation and Test in Europe Conference (DATE 2022), 2022

**CI-3 Ali Pour Amir*, Ali Pour Amir, Hély David*, Beroulle Vincent*, Di Natale Giorgio**
An Efficient Approach to Model Strong PUF with Multi-Layer Perceptron using Transfer Learning
International Symposium on Quality Electronic Design (ISQED 2022), 2022
**Laboratoire de Conception et d'Intégration des Systèmes*

**CI-4 Gava Jonas*, Moura Nicolas**, Da Rocha Vinicius**, Garibotti Rafael**, Cuenca-Asensi Sergio***, Possamai Bastos Rodrigo, Reis Ricardo*, Ost Luciano***
Assessment of Radiation-Induced Soft Error on Lightweight Cryptography Algorithms
Conference on Radiation Effects on Components and Systems (RADECS 2022), 2022
**UFRGS - Université fédérale du Rio Grande do Sul, **PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ***Universidad de Alicante*

**CI-5 Portolan Michele, Pavlidis Antonios*, Di Natale Giorgio, Faehn Eric**, Stratigopoulos Haralampos***
Circuit-to-Circuit Attacks in SoCs via Trojan-Infected IEEE 1687 Test Infrastructure
IEEE International Test Conference (ITC 2022), 2022
**LIP6 - Laboratoire d'Informatique de Paris 6, **STMicroelectronics [Crolles]*

**CI-6 Bolchini Cristiana*, Bosio Alberto*, Cassano Luca**, Deveautour Bastien*, Di Natale Giorgio, Miele Antonio Rosario**, O'Connor Ian*, Vatajelu Ioana**
Dependability of Alternative Computing Paradigms for Machine Learning: hype or hope?
IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2022), 2022
**INL - Institut des nanotechnologies de Lyon, **Politecnico di Milano*

**CI-7 Kraemer Sarzi Sartori Tarso, Fourati Hassen*, Rajappa Anuj Justus**, Reiter Philippe**, Possamai Bastos Rodrigo**
Effectiveness of Attitude Estimation Processing Approaches in Tolerating Radiation Soft Errors
Conference on Radiation Effects on Components and Systems (RADECS 2022), 2022
**GIPSA-Lab, **Internet Technology and Data Science Lab*
**CI-8 Ali Pour Amir*, Ali Pour Amir, Hély David*, Beroulle Vincent*, Di Natale Giorgio**
Elaborating on Sub-Space Modeling as an Enrollment Solution for Strong PUF
18th IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS 2022), 2022
**Laboratoire de Conception et d'Intégration des Systèmes*
**CI-9 Bordes Nicolas*, Maistri Paolo**
Electromagnetic Leakage Assessment of a Proven Higher-Order Masking of AES S-Box
25th Euromicro Conference on Digital System Design (DSD 2022), 2022
**Laboratoire Jean Kuntzmann*
**CI-10 Dragoi Vlad-Florin*, Dragoi Vlad-Florin**, Colombier Brice, Cayrel Pierre-Louis***, Grosso Vincent*****
Integer Syndrome Decoding in the Presence of Noise
IEEE Information Theory Workshop (ITW 2022), pp. 482-487, 2022
**Aurel Vlaicu University of Arad, **Université de Rouen Normandie, ***Laboratoire Hubert Curien*
**CI-11 Benevenuti Fabio*, Goncalves Marcio*, Pereira Jr Evaldo Carlos**, Vaz Rafael**, Gonçalez Odair Lelis**, Possamai Bastos Rodrigo, Létiche Manon***, Kastensmidt Fernanda*, Azambuja José Rodrigo***
Investigating the Reliability Impacts of Neutron-induced Soft Errors in Aerial Image Classification CNNs Implemented in a Softcore SRAM-based FPGA GPU
European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2022), 2022
**UFRGS - Université fédérale du Rio Grande do Sul, **Instituto de Estudos Avançados, ***ILL - Institut Laue-Langevin*
**CI-12 Von Staudt Hans-Martin*, Portolan Michele, Cote Jean-François**, Waayers Tom***, Rearick Jeff******
I Wish IJTAG would do this
27th IEEE European Test Symposium (ETS 2022), 2022
**Dialog Semiconductor, **Siemens [Floride], ***NXP Semiconductors (Eindhoven, Netherlands), ****Advanced Micro Devices [Austin]*
**CI-13 Possamai Bastos Rodrigo, Gorchs Picas Marti, Correa Cueto Marcelo, Velazco Raoul**
MEO Spaceflight Results of Radiation Effects in COTS FPGA-implemented Triple Modular System
Conference on Radiation Effects on Components and Systems (RADECS 2022), 2022
**CI-14 Vinagrero Gutierrez Sergio, Di Natale Giorgio, Vatajelu Ioana**
On-Line Reliability Estimation of Ring Oscillator PUF
IEEE European Test Symposium (ETS 2022), 2022
**CI-15 Cassano Luca*, Lazzeri Elia*, Litovchenko Nikita*, Di Natale Giorgio**
On the optimization of Software Obfuscation against Hardware Trojans in Microprocessors
IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2022), 2022
**Politecnico di Milano*
**CI-16 Martinoli Valentin, Teglia Yannick*, Bouagoun Abdellah*, Leveugle Régis**
Recovering Information on the CVA6 RISC-V CPU with a Baremetal Micro-Architectural Covert Channel
IEEE 28th International Symposium on On-Line Testing and Robust System Design (IOLTS 2022), 2022
**Thalès DIS*
**CI-17 Serrano-Cases Alejandro*, Martinez-Alvarez Antonio**, Possamai Bastos Rodrigo, Cuenca-Asensi Sergio****
Redundant Portable Multi-Threading for Soft Error Mitigation on Multicore Systems on Chip
Conference on Radiation Effects on Components and Systems (RADECS 2022), 2022
**Barcelona Supercomputing Center - Centro Nacional de Supercomputacion, **Universidad de Alicante*
**CI-18 Ali Pour Amir*, Ali Pour Amir**, Ali Pour Amir, Afghah Fatemeh*, Hély David***, Beroulle Vincent**, Di Natale Giorgio**
Secure PUF-based Authentication and Key Exchange Protocol using Machine Learning
IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2022), 2022
**Clemson University, **Laboratoire de Conception et d'Intégration des Systèmes, ***Laboratoire d'Electronique de Technologie de l'Information*
**CI-19 Fiorucci Tiziano, Di Natale Giorgio, Daveau Jean-Marc*, Roche Philippe***
Software Product Reliability Based on Basic Block Metrics Recomposition
IEEE 28th International Symposium on On-Line Testing and Robust System Design (IOLTS 2022), 2022
**STMicroelectronics [Crolles]*
**CI-20 Ali Pour Amir*, Ali Pour Amir, Hély David*, Beroulle Vincent*, Di Natale Giorgio**
Sub-Space Modeling: An Enrollment Solution for XOR Arbiter PUF using Machine Learning
International Symposium on Quality Electronic Design (ISQED 2022), 2022
**Laboratoire de Conception et d'Intégration des Systèmes*
**CI-21 Daddinounou Salah, Vatajelu Ioana**
Synaptic Control for Hardware Implementation of Spike Timing Dependent Plasticity
International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2022), pp. 106-111, 2022
**CI-22 Noizette Luc, Miller Florent*, Colladant Thierry**, Helen Youri***, Leveugle Régis**
Understanding of the link between complex digital devices Soft Error Rate and the running software
European Conference on Radiation and its Effects on Components and Systems (RADECS 2022), 2022
**Nucletudes, **Direction générale de l'Armement , ***DGA Maîtrise de l'information (Bruz)*
**CI-23 Noizette Luc, Miller Florent*, Colladant Thierry**, Helen Youri***, Leveugle Régis**
Using application profiling based on a virtual platform for SoC fault tolerance assessment
17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME 2022), 2022
**Nucletudes, **Direction générale de l'Armement , ***DGA Maîtrise de l'information (Bruz)*
**CI-24 Alshaer Ihab*, Alshaer Ihab, Colombier Brice, Deleuze Christophe*, Beroulle Vincent*, Maistri Paolo**
Variable-Length Instruction Set: Feature or Bug?
25th Euromicro Conference on Digital System Design (DSD 2022), 2022
**Laboratoire de Conception et d'Intégration des Systèmes*
**CI-25 Ouldei Tebina Nasr-Eddine, Zergainoh Nacer-Eddine, Maistri Paolo**
X-Ray Fault Injection: Reviewing Defensive Approaches from a Security Perspective
IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2022), 2022

## Book chapters (CH)

**CH-1 Roux Julie, Roux Julie*, Morin-Allory Katell, Beroulle Vincent*, Bossuet Lilian**, Cezilly Frédéric***, Berthoz Frédéric***, Genevrier Gilles***, Cerisier François****, Leveugle Régis**
FMEA on critical systems: A cross-layer approach based on high-level models
VLSI-SoC: Technology Advancement on SoC Design, pp. 113-133, 2022
**Laboratoire de Conception et d'Intégration des Systèmes, **Laboratoire Hubert Curien , ***Thalès Valence, ****AEDVICES CONSULTING*

## National journals (RN)

**RN-1 Lehouque Grégoire*, Costani Antoine*, Portolan Michele, Fesquet Laurent**
L'apprentissage par projet en microélectronique numérique Vers l'acquisition d'un savoir-faire
J3eA – Journal sur l'enseignement des sciences et technologies de l'information et des systèmes, Volume: 21, pp. 7, 2022
**École nationale supérieure de physique, électronique, matériaux (Grenoble INP)*
**RN-2 Benabdenbi Mounir, Leveugle Régis**
Test des circuits intégrés numériques - Conception orientée testabilité
Techniques de l'Ingénieur, Volume: , 2022

## Other communications (O)

**O-1 Fiorucci Tiziano, Daveau Jean-Marc*, Arbaretier Emmanuel**, Di Natale Giorgio, Roche Philippe*, Jacquet Thomas****
MBSA Approaches Applied to Next Decade Digital Components
IEEE European Test Symposium (ETS 2022), Barcelona, SPAIN
**STMicroelectronics [Crolles], **APSYS [Elancourt]*
**O-2 Fiorucci Tiziano, Fiorucci Tiziano*, Jacquet Thomas**, Jacquet Thomas***, Daveau Jean-Marc**, Di Natale Giorgio, Arbaretier Emmanuel***, Roche Philippe***
MBSA Approaches Applied to Next Decade Digital System-On-a-Chip Components
Congrès Lambda Mu 23 « Innovations et maîtrise des risques pour un avenir durable » - 23e Congrès de Maîtrise des Risques et de Sûreté de Fonctionnement, Institut pour la Maîtrise des Risques, Paris Saclay, FRANCE
**STMicroelectronics [Crolles], **LEAD - Laboratoire d'Etude de l'Apprentissage et du Développement [Dijon], ***AIRBUS Protect*
**O-3 Martinoli Valentin, Teglia Yannick*, Bouagoun Abdellah*, Leveugle Régis**
Recovering information on a RISC-V CPU with a baremetal micro-architectural covert channel
Workshop on Practical Hardware Innovations in Security Implementation and Characterization (PHISIC 2022), Gardanne, FRANCE
**Thalès DIS*

## Theses (T)

**T-1 Ali Pour Amir**
PUF based Secure Computing for Resource Constrained Cyber Physical Objects
These de Doctorat, Université Grenoble Alpes, spécialité "", Dec 08, 2022
**T-2 Jaamoum Amine**
Strategies for securing cache memories against software side-channel attacks
These de Doctorat, Université Grenoble Alpes, spécialité "", Dec 12, 2022

TiMA
CNRS — GRENOBLE INP — UGA

# CDSI team

## Circuits, Devices and System Integration

# Circuits, Devices and System Integration (CDSI team)

**Keywords:** Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

## The CDSI team

The team activity covers a broad spectrum of activities from MEMS to systems. Indeed, the team postulates high performances are achieved thanks to disruptive technologies, which are at the frontiers of different fields of applications. Nevertheless, the team is built on two key pillars, sensing and event processing.

Event-based techniques are key for enhancing integrated circuits and systems because they offer a unique opportunity to rethink circuit design, which does not take well into account most of the non-functional specifications, such as power, security, safety or electromagnetic emissions. This paves the way to ultra-low power systems, enhanced secured systems, proven design methods but also near sensor computing.

Sensing is the second key. Taking advantage of smart sensors and actuators requires globally envisioning systems, favors a smart sensing approach limiting useless information and pushes new experiments and usage.

## Event-based technologies

### Event-based approach

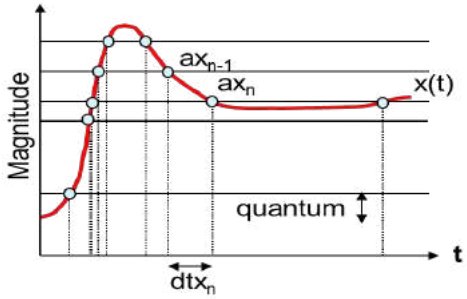



Figure 1: Level Crossing Sampling Scheme

Event-based is a quite simple idea, which suggests operating a circuit only when needed. Nevertheless, this is countercurrent when looking the semiconductor industry. Indeed, everything is clocked synchronized, analog-to-digital conversion is clock-sampled. In practice, clock is used as an event generator giving the pace of the circuits generating a large number of events and producing useless activity, computation, storage or communication. The event-based approach tends generating sparse events related to natural events such as a pressure variation or a heartbeat. Therefore, the team works on alternative analog-to-digital converters able to drastically reduce the number of samples and, hence, limit useless activity and energy consumption (see Figure 1).

### Asynchronous Circuits

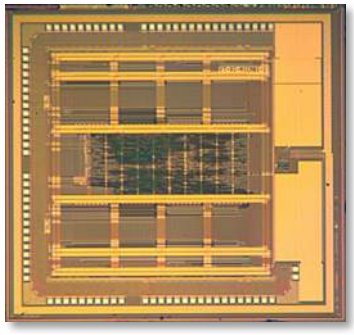


Figure 2: Asynchronous microcontroller with on-chip NFC antenna

Since more than 20 years, the team works on new synchronization paradigms, which are not based on a clock but on handshake signals. Such techniques reveal many opportunities for rethinking the circuit design process and opening new degrees of freedom. The first expected advantage is probably the reusability of existing blocks that can simply be connected together, making the assembly of a system a kind of LEGO build. Indeed, the timing assumptions are locally fulfilled guarantying an easy block association. Moreover, many other advantages are of interest such a lower power consumption, a better robustness, lower electromagnetic emissions, safer and more secured circuits…

## Targeting Ultra-low power

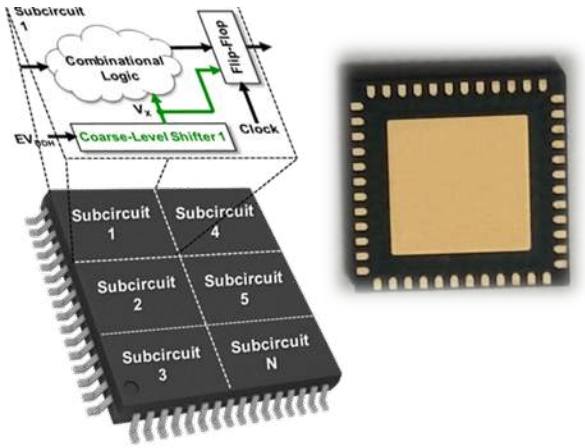



Figure 3: FDSOI 28 nm asynchronous testchip managing several local fine-grain body-bias domains

Today power is a main concern for chip design. The event-based strategy is probably the best technique for reducing power at least by one order of magnitude. Indeed, a sparse sampling scheme produces much less data, which are non-uniformly spaced in time. Each datum is no more than an event that can be sporadically processed by asynchronous circuits. Indeed, these latter are data-driven and consume energy only when computing. Moreover, the intrinsic robustness of asynchronous circuits favors their use at low-voltage, near- or subthreshold. Indeed, lowering the voltage is an efficient and well-known strategy to save power. Its main drawback is the decrease of the circuit speed. The Fully Depleted Silicon on Insulator (FDSOI) technology allows mitigating this speed drop thanks to forward body biasing. As asynchronous circuits use communication protocols indicating circuit activity, the handshake signals are perfectly suited for controlling local body-bias domains ensuring low-energy expenses for body biasing and compensating the speed loss.

All these mechanisms can be implemented for mitigating the energy and helping the adoption of energy harvesting in batteryless systems.

## Security

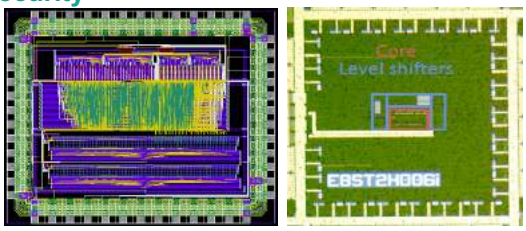



Figure 4: TRNG with entropy monitoring (left) and Ultra-low power TRNG (right) (30 pJ/bit@0.3 V)

Another opportunity offered by the asynchronous circuits is its ability to make more difficult the side-channel analysis and attacks in trusted devices. Indeed, the absence of clock synchronization, the specific encoding and the computation time control makes them of interest for developing trusted platforms. They also offer disruptive strategies for true random number generators (TRNG) and physically unclonable functions (PUF) while consuming a few energy.

## Design flow and proven technology

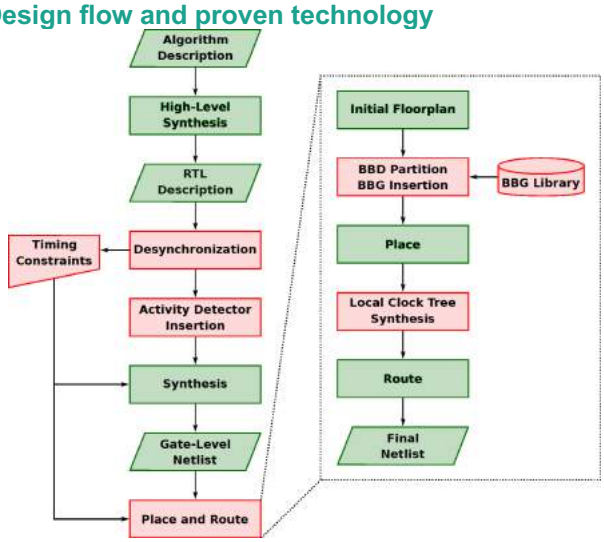



Figure 5: Asynchronous circuit HLS to layout design flow

Developing non-conventionally synchronized circuits is not obvious because of the lack of dedicated CAD tools. Although the first good idea is to implement such tools, there is some overcoming hurdles. The first one is clearly the quasi-absence of trained people with the know-how for designing efficient and performant asynchronous circuits. The second is the impact, the reliability and the engineer confidence into a new design flow. Therefore, for more than 10 years, the team is developing dedicated flows based on the standard commercial tools with a particular emphasis on a proven by construction synthesis.

### Near-sensor computing

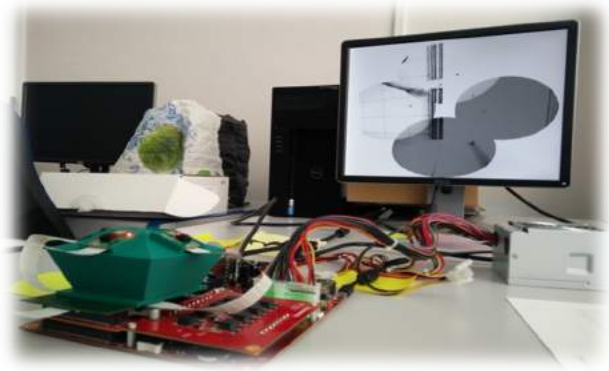


Figure 6: Panoptic camera for laparoscopy

With the dissemination of autonomous and connected objects, it appeared the need to limit the amount of transmitted raw data, especially in RF communications where the problem is more acute. Therefore, developing tiny sensor platforms able to preprocessed data before transmitting information is becoming a challenging topic. Indeed, enhancing the sensing techniques and immediately processing the raw data with a reduced energy budget is the grail in near-sensor computing. The team developed several strategies based on event-based techniques or improving the adequacy between the algorithms and the circuit architecture. This is typically the case for many image-processing applications such as panoptic camera for laparoscopy.

## Smart-sensing technologies

### In-sensor computing

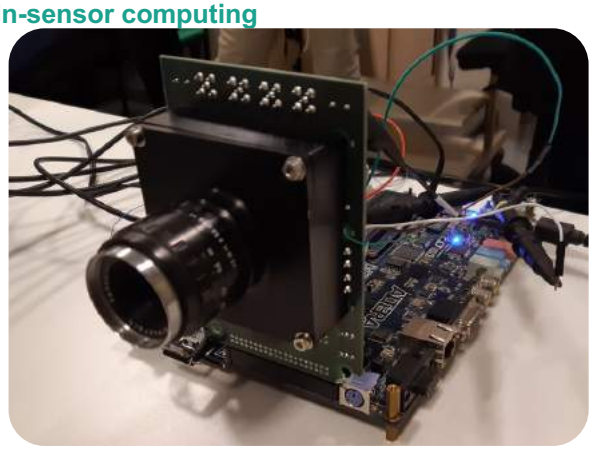


Figure 7: Event-based camera

As previously stated, smart sensing is a key for envisioning systems with advanced features such as detection, pattern recognition or low-power. Beyond the state of art of sensor technology, the enhancement can be obtained thanks to new architectures or in-sensor computing. One of the approach concerns image sensors, which usually permanently read the image. This is a waste of energy and time for acquiring an image. In order to reduce these issues, the image capture can be performed thanks to an event-based readout, which only samples a pixel when this latter fires. In this case, the firing pixel indicates that its value has to be changed in the image memory. Such a strategy is applied for reducing the power consumption and increasing the speed sensor thanks to a dedicated readout canceling the spatial and temporal redundancies.

### Measuring time

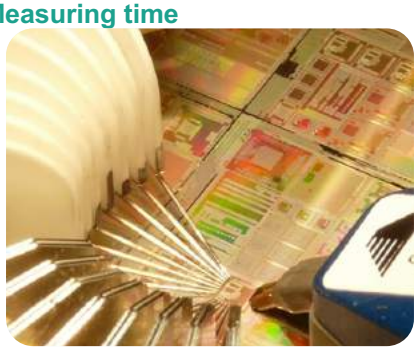


Figure 8: Asynchronous multiphase oscillator (under test) used in TDC

Using an event-based sensing implies a duality with the standard Nyquist analog-to-digital conversion because the quantization is no more applied to the amplitude but to the time elapsed between two successive events. Therefore, designing advanced Time-to-Digital Converters (TDC) is an important block for many sensors or even for some security primitives such as TRNG or PUF.

## Harvesting for ultra-low power systems

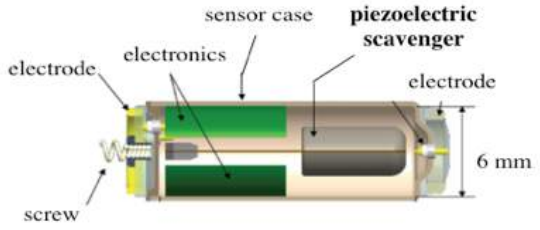



Figure 9: Piezoelectric scavenger for automous pacemaker (Vibration: 10 - 25 Hz, Size: L = 30 mm, Ø= 6 mm, energy: 5 - 10 µJ)

With the advent of the Internet of Things, the system requirements in term of power are extremely demanding, especially for smart sensing and actuating. A typical highlight targets the medical implant such as pacemakers. Indeed, they need today a battery, which lasts less than 10 years. Then the pacemaker has to be explanted because this is not a rechargeable battery. Wireless power transfer may overcome this issue via acoustic wave propagation, using piezoelectric transducers to generate and harvest acoustic power. The MEMS are particularly well-suited for this purpose, for small autonomous and smart objects.

## Security (chaotic approach)

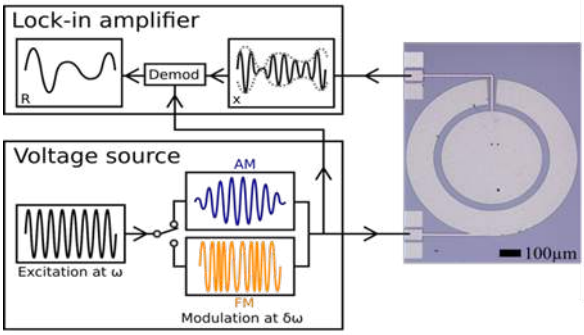



Figure 10: Experimental Setup and modulations in the Duffing's regime. The MEMS (photography) is driven by a voltage modulated voltage source (AM or FM). The Lock-in-Amplifier extracts the displacement magnitude of the MEMS to observe the chaos.

MEMS have opened the doors to intense researches covering most of the technology fields. It is not surprising that they can be of interest for security. They offer original solutions for designing chaotic generators using the dynamical bistability of a Duffing's microresonator. This approach is particularly relevant for generating true random numbers because MEMS already exist on various systems such as mobile phones and are useable for extracting chaos. Moreover, this could be employed for securing communications in various transduction schemes. In acoustics, chaotic MEMS can be used as ultrasonic jammers. In optics, synchronization of chaotic MEMS takes benefit from both high complexity yet controllable chaos and large data rate for secured telecom applications.

## New Sensors and actuators

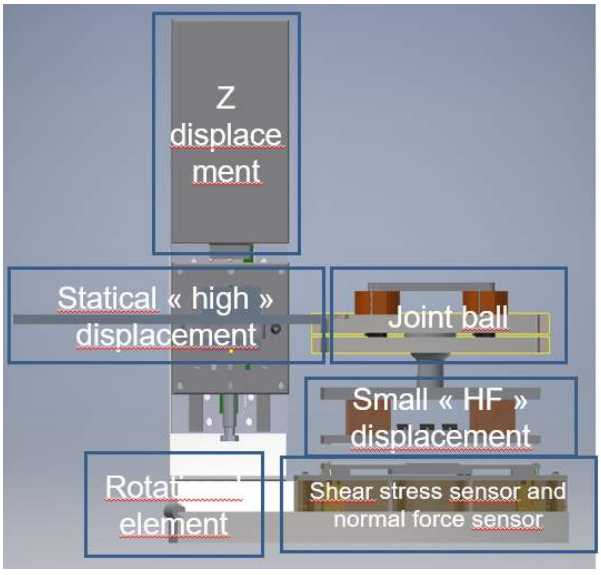



Figure 11: The 3D representation of the new piezo rheometer with description of its functions

The team is also developing a new kind of piezo-based sensors and actuators for applications in rheometry, earphones, or microphones.

The piezorheometer permits to obtain high frequency strain compared to standard equipment. This rheometer combines piezoelectric actuator, slaved by accelerometers to give accurate strain to a media, with piezolectrics ceramics which are the sensors to extract the stress given to this media. With a precise extraction of the imposed strain synchronized with the stress, the shear modulus is calculated. Innovation comes from the slaving of the actuators. Moreover, this kind of rheometer only applied small strain so a linear piezoelectric actuator has been implemented to evaluate the shear modulus from very low to very high strain. Finally, this rheometer will be as precise as classical rheometer but less expensive and with a smaller volume.

Figure 12: ActivMotion earphones concept

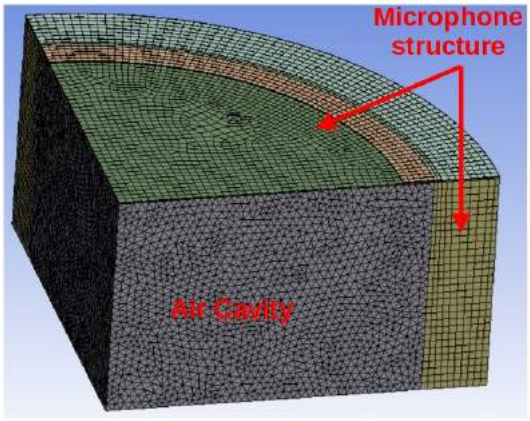



Figure 13: Finite element model for MEMS piezoelectric microphone.

Piezoelectric actuators can also be implemented in earphones to replace the widely used electrodynamic transducers. They offer new possibilities in term of design and integration, which ActivMotion is pushing. In their concept, the user's ears become the emitting surface which allows for new earphone ergonomics. High power density piezoelectric actuators working at low voltages are ideal for this use case. With the resonance control of the actuator, a linear performance over the audible frequency range is obtained.

CDSI team is also part of the project MAMBO aiming at reducing airplanes noises. The knowledge of noise sources in airplanes is crucial and requires specific microphones characteristics to measure them (high pressure, wide dynamic and frequency range, low SNR,…). In this context, the team work is focused on the conception of a MEMS piezoelectric microphone using finite element method and lumped element equivalent circuit to predict the microphone performances for aeroacoustic measurements.

## Recent highlights

### March 31, 2022: FMNT half-day - graduate school@UGA PT-SUMMIT: Alternative approaches for sustainable sensors

The GraduateSchool@UGA PT-SUMMIT and the FMNT of Grenoble are jointly organizing on March 31, 2022 at the amphi Bergès in GreEn-ER an event dedicated to alternative approaches for sustainable sensors. Read more: https://greengrenoble2022.eu/agenda/301/3-demi-journee-fmnt-graduate-school-uga-pt-summit-approches-alternatives-pour-des-capteurs-durables.htm)

### October 27, 2022: Scientific Day: Piezoelectric Microsystems and Transducers

These Scientific Days are meant to present the research topics and to disseminate the recent advances of TIMA researchers. These presentations are open to everybody, whether they are members of TIMA or not.
Program: 2022_10_27_cdsi_piezoelectric_microsystems_and_transducers.pdf

### December 15, 2022: Seminar by Damiano ZUCCALA (PhD student at TIMA Lab)

*"Alan Turing and the Enigma Machine - An historical overview"*
By Damiano ZUCCALA - PhD student at TIMA Laboratory (CDSI team)

## Academic and research members

### Skandar BASROUR

**Position**
Professor at UGA – Polytech school

**Responsibilities**
Researcher in CDSI team

### Martial DEFOORT

**Position**
Researcher at CNRS

**Responsibilities**
Researcher in CDSI team

### Sylvain ENGELS

**Position**
Associate Professor PAST at Grenoble INP - Phelma school

**Responsibilities**
Researcher in CDSI team

### Laurent FESQUET

**Position**
Associate Professor at Grenoble INP - Phelma school

**Responsibilities**
Deputy Director of TIMA Lab. since 01/2021
Leader of CDSI team
Researcher in CDSI team

### Stéphane MANCINI

**Position**
Associate Professor at Grenoble INP - Ensimag school

**Responsibilities**
Researcher in CDSI team

### Katell MORIN-ALLORY

**Position**
Associate Professor at Grenoble INP - Phelma school

**Responsibilities**
Researcher in CDSI team

*CNRS (French National Center for Scientific Research)*
*ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)*
*GRENOBLE INP (Grenoble Institute of Technology)*
*IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)*
*PHELMA school (Physique-Electronique-Matériaux)*
*POLYTECH school (École Polytechnique de l'Université Grenoble Alpes)*
*UGA (Université Grenoble Alpes)*

## Ph. D. candidates

### 1. AKBARI Masoud
Title of thesis: **Open-Air Fabrication of Oxide Based Cantilever Gas Sensors**
Expected date of defense: 2023
Previous degrees: Master of Science in materials science and engineering - Pohang University of Science and Technology (POSTECH) – Pohang, Republic of Korea (2015)

### 2. AKRARAI Mohamed
Title of thesis: **Smart Event-Based Image Sensor for wake-up applications**
Expected date of defense: **2023**
Previous degrees: Engineer - INPT (Institut National des Postes et Télécommunications) - Rabat, Morocco (2018)

### 3. BELOT Jérémy
Title of thesis: **Towards compact, low energy and with adjustable accuracy Bayesian computers**
Completed on: **October 2, 2022**
Previous degrees: Engineer - Grenoble INP – Phelma - Grenoble, France (2018)

### 4. CROZET Florent
Title of thesis: **Extreme Learning Machine for embedded neural networks**
Expected date of defense: **2024**
Previous degrees: Master - Université de Clermont-Ferrand-I – Clermont-Ferrand, France (2019)

### 5. DECOUDU Yoan
Title of thesis: **An asynchronous circuit design flow: From HLS to FDSOI implementation**
Completed on: **September 23, 2022**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

### 6. DE GIOVANNI Adrien
Title of thesis: **Design of a piezoelectric micro-actuator with mechanical amplification for extra-auricular earphones**
Expected date of defense: **2023**
Previous degrees: Engineer – ENSAM (Ecole Nationale Supérieure d'Arts et Métiers) – Paris, France (2020)

### 7. ENGELS Sylvain
Title of thesis: **Energy efficiency technics for advanced CMOS technologies**
Completed on: **July 1, 2022**
Previous degrees: Engineer – Grenoble INP – Phelma, France (1999)

### 8. GASSAB Marwa
Title of thesis: **Physico-chemical and di-electric development and characterization of polymer films based on PVA-Glycerol for humidity sensors**
Expected date of defense: 2023
Previous degrees: Master in microsystem and embedded electronic systems - Institut Supérieur des Sciences Appliquées et de Technologie, Sousse, Tunisie (2018)

### 9. HACHEMI Mohammed-Bilal
Title of thesis: **Contribution to the study of structural and ferroelectric properties of HZO thin films**
Completed on: **September 29, 2022**
Previous degrees: Engineer - ECole Polytechnique de Constantine – Algeria (2017)

### 10.IGA Rodrigo
Title of thesis: **Reliable event-based techniques for ASK demodulation in NFC devices**
Completed on: **February 24, 2022**
Previous degrees: Master – UGA (Université Grenoble Alpes), France (2011)

### 11. KALEL Diana
Title of thesis: **Development of an advanced flow of structural, formal and semi-formal verification of asynchronous paths using appropriate formal verification methods and tools, for high-performance integrated processor-based subsystems**
Expected date of defense: **2024**
Previous degrees: Master – Ain Shams University – Cairo, Egypt (2019)

### 12. LECLAIRE Nicolas
Title of thesis: **Hardware and software architectures for deep learning acceleration on embedded multi-processor**
Completed on: **January 4, 2022**
Previous degrees: Engineer – Grenoble INP – Phelma – Grenoble, France (2017)

### 13. LESAGE Xavier
Title of thesis: **Smart batteryless InfraRed Image Sensor**
Expected date of defense: **2025**
Previous degrees: Master of Science – Karlsruher Institut fuer Technologie (KIT) - Karlsruhe, Germany (2021)

### 14. LIM Olivier
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2023**
Previous degrees: Master UGA (Université Grenoble Alpes) (2020)

### 15. MERIO Cristiano
Title of thesis: **Using artificial intelligence for near field communication and low-energy signal demodulation**
Expected date of defense: **2025**
Previous degrees: Engineer – Grenoble INP (2022)

### 16. MOUSSA Hasan
Title of thesis: **Event-based Smart RF Architectures**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA (Université Grenoble Alpes) (2021)

### 17. NAIMI Ali
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2025**
Previous degrees: Engineer - INPT (Institut National des Postes et Télécommunications) - Rabat, Morocco (2022)

### 18. ROUX Julie
Title of thesis: **Safety Evaluation of Aircraft Systems using Virtual Platforms**
Completed on: **January 7, 2022**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2017)

### 19. TACYNIAK Pierre
Title of thesis: **Study of a secured wireless acoustic power transfer for medical implants**
Expected date of defense: **2024**
Previous degrees: Master ENSAM (Ecole Nationale Supérieure d'Arts et Métiers) – Paris, France (2021)

### 20. TRAN Rosalie
Title of thesis: **Smart Event-Based Image Processing**
Expected date of defense: **2024**
Previous degrees: Engineer – Grenoble INP – Phelma – Grenoble, France (2021)

### 21. ZUCCALA Damiano
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2025**
Previous degrees: Master in Physics - Università degli Studi dell'Insubria – Como, Italy (2021)

## Other members

### Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. BOCCALERO | Gregorio | ITALY | 12 months |
| 2. ESTEVES | Josue | FRANCE | 10 months |
| 3. PASSY KENGANI | Marco Erickson | CONGO | 12 months |
| 4. RICART | Thibault | FRANCE | 8 months |

### Visitors

No positions in 2022.

### Trainees

| NAME | FORENAME | COUNTRY | DURATION |
|---|---|---|---|
| 1. CHAVES LIMEA CANANEA | Leticia | FRANCE | 3 months 15 days |
| 2. DE FRANCA NOBREGA | Vinicius | BRAZIL | 5 months 19 days |
| 3. GONSALVES SANTOS | Jéssica | FRANCE | 2 months 23 days |
| 4. LE GOUSSE | Nathan | FRANCE | 5 months 8 days |
| 5. ORIEUX | Claire | FRANCE | 1 month |
| 6. PISANU | Michele | ITALY | 3 months 29 days |

## Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2022.

### ANRT

**CIFRE Jérémy BELOT (2020 – 2023)**
Scientific manager: Laurent FESQUET
Industrial partner: HawaiTech

**CIFRE Florent CROZET (2022 – 2025)**
Title: Machines d'apprentissage extrême et matrices aléatoires pour les réseaux de neurones embarqués
Scientific manager: Stéphane MANCINI
Industrial partner: STMicroelectronics

**CIFRE Adrien DE GIOVANNI (2020-2023)**
Title: Design of a piezoelectric micro-actuator with mechanical amplification for extra-auricular earphones
Scientific manager: Skandar BASROUR
Industrial partner: ActiveMotion

### CEC-NATIONAL

**OCEAN 12 (2018 – 2022)**
Program: ECSEL
Title: Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node
Scientific manager: Laurent FESQUET

### INTERNATIONAL

**BRAFISAT (2019 – 2022)**
Program: BRAFITEC
Scientific manager: Rodrigo POSSAMAI BASTOS

### MINISTERES-FUI

**EAUDI (2021 – 2025)**
Title: Ecouteur extra AUriculaire Dissimulé
Scientific manager: Skandar BASROUR

**IMSPOC-UV (2018 - 2022)**
Program: PIA Programme d'Investissement d'Avenir
Title: Imaging Spectrometer On Chip
Scientific manager: Skandar BASROUR

### REGION

**FAIR (2018 – 2023)**
Program: Pack Ambition Recherche
Title: Conception et fabrication par Fabrication Additive de produits Intelligents
Scientific manager: Skandar BASROUR

**GRESAM (2019 – 2022)**
Program: Pack Ambition International
Title: Grenoble Sousse Autonomous Microsystems
Scientific manager: Skandar BASROUR

**MucoPiezoRheo (2020 – 2023)**
Program: PSPC
Scientific manager: Skandar BASROUR

### SATT

**EMIR (2021 – 2023)**
Title: Event-based Microbolometer for IR sensors adn ultra low power applications
Scientific manager: Laurent FESQUET

## Organization and participation of international conferences, workshops, forums

**International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS'2022)**
October 16-20, 2022, Lisbon, Portugal
Rank: NC
technical committee: FESQUET Laurent

**Design, Automation and Test in Europe Conference (DATE'2022)**
March 14-23, 2022, Virtual event
Rank: A+
topic chair: MORIN-ALLORY Katell

**Journées Nationales sur la Récupération et le Stockage de l'Energie 2022 (JNRSE'2022)**
July 7-8, 2022, Bordeaux, FRANCE
Rank: NC
organization committee: BASROUR Skandar
program committee: BASROUR Skandar

**7th International Conference on Advances in Signal, Image and Video (SIGNAL'2022)**
May 22-26, 2022, Venice, ITALY
technical program committee: FESQUET Laurent

# Responsibilities

| Role | TIMA member | Starts | Ends | Comments |
|---|---|---|---|---|
| **Faculties / Schools** | | | | |
| **Phelma school<br>PHysique – ELectronique - MAtériaux** | | | | |
| Manager of SEI branch | MORIN-ALLORY Katell | 01/09/2017 | | |
| **Graduate School@UGA** | | | | |
| Coordinator of SUMMIT program | BASROUR Skandar | 01/09/2020 | | |
| **Research structures** | | | | |
| **CIME Nanotech<br>Centre Interuniversitaire de MicroElectronique et Nanotechnologies** | | | | |
| CIME platform relationship | MORIN-ALLORY Katell | 01/09/2022 | | |
| Deputy Director | FESQUET Laurent | 01/09/2017 | | |
| Manager of Communicating objects platform | MANCINI Stéphane | 01/09/2017 | | |
| Manager of Microsystems platform | BASROUR Skandar | 01/10/2006 | 01/09/2022 | |
| **FMNT<br>Fédération des Micro et Nanotechnologies** | | | | |
| Deputy Director | BASROUR Skandar | 01/01/2021 | | |
| **Parent institutions** | | | | |
| **Grenoble INP<br>Grenoble Institute of Technology** | | | | |
| Board of Directors member (elected member) | MANCINI Stéphane | 12/12/2019 | 01/01/2024 | Strategy, jobs, promotion files, invited professors, teaching assistants |

# Scientific production

## International journals (RI)

**RI-11 Defoort Martial, Hentz Sébastien*, Shaw Steven W.**, Shoshani Oriel*****
Amplitude stabilization in a synchronized nonlinear nanomechanical oscillator
Communications Physics, Volume: 5, pp. 1-7, 2022
**Laboratoire d'Electronique de Technologie de l'Information, **Florida Institute of Technology [Melbourne], ***Ben-Gurion University of the Negev*

**RI-12 Lai Szu-Hsueh*, Lai Szu-Hsueh**, Reynaud Adrien***, Zhang Ning-Ning****, Kwak Minjeong*****, Vysotskyi Bogdan***, Dominguez-Medina Sergio*, Fortin Thomas*, Clement Kavya*, Defoort Martial***, Defoort Martial, Lee Tae Geol*****, Liu Kun****, Hentz Sébastien***, Masselon Christophe D.***
Characterizing Nanoparticle Mass Distributions Using Charge-Independent Nanoresonator Mass Spectrometry
Journal of Physical Chemistry C, Volume: 126, pp. 20946–20953, 2022
**Institut de Recherche Interdisciplinaire de Grenoble , **Department of Chemistry - National Cheng Kung University (NCKU) , ***Laboratoire d'Electronique de Technologie de l'Information, ****State Key Laboratory of Supramolecular Structure and Materials (Jilin University), *****Korea Research Institute of Standards and Science [Daejon]*

**RI-13 Lim Olivier*, Lim Olivier, Mancini Stéphane, Dalla Mura Mauro*, Dalla Mura Mauro****
Feasibility of a Real-Time Embedded Hyperspectral Compressive Sensing Imaging System
Sensors, Volume: 22, pp. 9793, 2022
**GIPSA-Lab, **Institut Universitaire de France*

**RI-14 Proto Antonino*, Proto Antonino**, Rufer Libor, Basrour Skandar, Penhaker Marek****
Modeling and Measurement of an Ultrasound Power Delivery System for Charging Implantable Devices Using an AlN-Based pMUT as Receiver
Micromachines , Volume: 13, 2022
** Department of Neuroscience and Rehabilitation Laboratoire (University of Ferrara), **Department of Cybernetics and Biomedical Engineering (Technical University of Ostrava)*

**RI-15 Rendon Hernandez A.*, Basrour Skandar**
On the Design of a Thermo-Magnetically ActivatedPiezoelectric Micro-Energy Generator: Working Principle
Sensors, Volume: 22, pp. 1610, 2022
**University of Florida [Gainesville]*

**RI-16 Guy Sylvain*, Haberbusch Jean-Loup*, Promayon Emmanuel*, Mancini Stéphane, Voros Sandrine***
Qualitative Comparison of Image Stitching Algorithms for Multi-Camera Systems in Laparoscopy
Journal of Imaging, Volume: 8, pp. 52, 2022
**Gestes Medico-chirurgicaux Assistés par Ordinateur*

**RI-17 Gassab Marwa*, Brefuel Nicolas**, Sylvestre Alain**, Dridi Cherif*, Basrour Skandar**
Structural, thermal and dielectric properties of glycerolized hydrogen-bonded polyvinyl alcohol films
Polymers for Advanced Technologies, Volume: 34, pp. 948-959, 2022
**NANOMISENE RD Laboratory [Sousse], **Laboratoire de Génie Electrique de Grenoble*

## Patents (B)

**B-1 Defoort Martial, Basrour Skandar, Fesquet Laurent**
Générateur physique chaotique de nombres aléatoires vrais et procédé associé
Brevet N° FR3112874, delivered on Jan 28, 2022

**B-2 Lauwers Thomas*, Basrour Skandar, Coutard Jean-Guillaume*, Glière Alain*, Laffont Guillaume***
Photoacoustic or photothermal detector comprising an optical transducer
Brevet N° US 2022/0364981 Al, delivered on Nov 17, 2022
**Laboratoire d'Electronique de Technologie de l'Information*

## Invited conferences talks (INV)

**INV-1 Fesquet Laurent**
Designing Event-Based Electronics
8th International Conference on Event-based Control, Communication, and Signal Processing (EBCCSP 2022), 2022

## International conferences (CI)

**CI-26 Lesage Xavier, Tran Rosalie, Mancini Stéphane, Fesquet Laurent**
An improved event-by-event clustering algorithm for noisy acquisition
8th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2022), pp. 1-8, 2022

**CI-27 Iga Rodrigo*, Iga Rodrigo, Engels Sylvain*, Engels Sylvain, Fesquet Laurent**
A Novel Event-Based Method for ASK Demodulation
IEEE 13th Latin America Symposium on Circuits and System (LASCAS 2022), pp. 1-4, 2022
**STMicroelectronics [Crolles]*

**CI-28 Defoort Martial, Rufer Libor, Basrour Skandar**
Chaos in a non-linear non-buckled microresonator
10th European Nonlinear Dynamics Conference (ENOC 2020, repoussé à 2022), 2022

**CI-29 Defoort Martial**
Chaos in micro-mechanics: towards MEMS-based secured communications
COMET Microsystèmes et Composants Électroniques (COMET-MCE 2022), 2022

**CI-30 Gassab Marwa*, Sylvestre Alain**, Basrour Skandar, Dridi Cherif***
Electrical properties modulation of PVA-glycerol based composites for flexible sensors
IEEE International Conference on Design & Test of Integrated Micro & Nano-Systems (DTS 2022), 2022
**NANOMISENE RD Laboratory [Sousse], **Laboratoire de Génie Electrique de Grenoble*

**CI-31 Nastro Alessandro*, Baù Marco*, Ferrari Marco*, Rufer Libor, Basrour Skandar, Ferrari Vittorio***
Flexural Plate Wave Piezoelectric MEMS Transducer for Cell Alignment in Aqueous Solution
Sustainable and Integrated Engineering International Conference (SIE 2022), pp. 122-127, 2022
**Department of Information Engineering [University of Brescia]*

**CI-32 Defoort Martial, Rufer Libor, Basrour Skandar**
Génération d'ultrasons à comportement chaotique par un micro-transducteur piézoélectrique non-linéaire
16ème Congrès Français d'Acoustique (CFA2022), 2022
**CI-33 Alshakoush Ali, Ibrahim Sana, Subias Serge, Podevin Florence, Barragan Manuel, Pino Monroy Dayana Andrea, Bendjeddou Imadeddine, Lauga-Larroze Estelle, Fesquet Laurent, Taris Thierry*, Bourdel Sylvain**
N-Path Mixer with Wide Rejection Including the 7th Harmonic for Low Power Multi-standard Receivers
20th IEEE Interregional NEWCAS Conference (NEWCAS 2022), pp. 256-260, 2022
**Laboratoire de l'Intégration du Matériau au Système (Bordeaux)*
**CI-34 Moussa Hasan, Ibrahim Sana, Lauga-Larroze Estelle, Podevin Florence, Bourdel Sylvain, Fesquet Laurent**
Self-Timed Ring Oscillators for Non-Overlapping and Overlapping Phases Synthesis
20th IEEE International NEWCAS Conference (NEWCAS 2022), 2022

## Book chapters (CH)

**CH-2 Roux Julie, Roux Julie*, Morin-Allory Katell, Beroulle Vincent*, Bossuet Lilian**, Cezilly Frédéric***, Berthoz Frédéric***, Genevrier Gilles***, Cerisier François****, Leveugle Régis**
FMEA on critical systems: A cross-layer approach based on high-level models
VLSI-SoC: Technology Advancement on SoC Design, pp. 113-133, 2022
**Laboratoire de Conception et d'Intégration des Systèmes, **Laboratoire Hubert Curien , ***Thalès Valence, ****AEDVICES CONSULTING*

## National journals (RN)

**RN-3 Lehouque Grégoire*, Costani Antoine*, Portolan Michele, Fesquet Laurent**
L'apprentissage par projet en microélectronique numérique Vers l'acquisition d'un savoir-faire
J3eA – Journal sur l'enseignement des sciences et technologies de l'information et des systèmes, Volume: 21, pp. 7, 2022
**École nationale supérieure de physique, électronique, matériaux (Grenoble INP)*

## National conferences (CN)

**CN-1 Alshakoush Ali, Ibrahim Sana, Subias Serge, Vincent Loïc*, Lauga-Larroze Estelle, Fesquet Laurent, Podevin Florence, Bourdel Sylvain**
Mélangeur N-Path à 5 chemins rejetant jusqu'à l'harmonique 8 inclus pour récepteurs multistandards basse consommation
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Centre Interuniversitaire de Micro-Electronique*

## Others communications (O)

**O-4 Fesquet Laurent**
Innovation and education in microelectronics to face the society needs in semiconductors
7th Forum on Research and Technologies for Society and Industry Innovation: latest developments for a better world (RTSI 2022), Paris, FRANCE
**O-5 Tacyniak Pierre, Defoort Martial, Basrour Skandar**
Numerical simulations of acoustic power transfer
Journées Nationales sur la Récupération et le Stockage de l'Energie (JNRSE 2022), Bordeaux, FRANCE

## Theses (T)

**T-3 Belot Jérémy**
Towards robust, low power and adjustable accuracy Bayesian computers
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Oct 12, 2022
**T-4 Decoudu Yoan**
An asynchronous Design Flow for Event-Based Processing in FDSOI Technologies
These de Doctorat, Université Grenoble Alpes, spécialité "", Sep 23, 2022
**T-5 Engels Sylvain**
Energy Efficiency Technics for advanced CMOS Technologies
These de Doctorat, Université Grenoble Alpes, spécialité "", Jul 01, 2022
**T-6 Hachemi Mohammed-Bilal**
Contribution to the study of structural and ferroelectric properties of HZO thin films
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Sep 29, 2022
**T-7 Iga Rodrigo**
Reliable event-based techniques for ASK demodulation in NFC devices
These de Doctorat, Université Grenoble Alpes, spécialité "", Feb 24, 2022
**T-8 Leclaire Nicolas**
Hardware and Software architectures for deep learning acceleration on embedded multi-processor
These de Doctorat, Université Grenoble Alpes, spécialité "Informatique", Jan 04, 2022
**T-9 Roux Julie**
Safety Evaluation of Aircraft Systems using Virtual Platforms
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Jan 07, 2022

TiMA
CNRS — GRENOBLE INP — UGA

# RMS team

## Reliable RF and Mixed-signal Systems

# Reliable RF and Mixed-signal Systems (RMS team)

## Description

The Reliable RF and Mixed-signal Systems group (**R**MS) is focused on the design, test and control of analog/mixed-signal/RF/mm-Wave integrated circuits and systems. 2021 has been a transition year for the **R**MS team, in preparation for the integration of the researchers in RFIC-Lab within the team in 2022. In this regard, the research axes of the team have evolved to better describe the wider scope of the team activities after the integration. Our research can be declined into the following four main axes:

### Design of AMS-RF integrated circuits and systems

Novel AMS-RF design solutions are required in a wide variety of state-of-the-art applications, including communications, computing, imaging, etc. In this regard, the **R**MS group explores the multiple challenges of state-of-the-art AMS-RF current and emerging design paradigms, especially focusing on low-power and/or low-voltage applications. Our research includes the development of low-power mixed-signal and RF design techniques, state-of-the-art area-efficient high-resolution and ultra-low power data converters for imaging applications, integrated control electronics for quantum computing, and advanced RF design techniques for 5G and beyond-5G applications.

### Integration and miniaturization of RF-mmW circuits

In this research axe our activities are focused on exploring novel integration solutions, including “More Moore” approaches, such as taking advantage of optimized Back-End-Of-Line metal stacks for integrating novel 3D passive structures, and “More-Than-Moore” approaches, where heterogeneous 2.5D and 3D solutions using mmW interposers.

### Design for test and reliability of AMS-RF/mmW circuits and systems

Testing AMS-RF/mmW functions in a complex integrated system represent nowadays a major challenge for the IC industry. Our research in this area is focused on two main research lines: a) the development of AMS-RF-mmW state-of-the-art on-chip test instruments for Built-In Self-Test (BIST) applications and dedicated DfT techniques; and b) the development of novel indirect test methodologies based on the applications of advanced machine learning algorithms.

### Control, optimization and self-healing of AMS/RF and mm-Wave circuits

In parallel with the test challenge, performance calibration and tuning are of key interest in the IC industry. Performance calibration in the production line enables a yield enhancement, while providing tuning capabilities during the lifetime of the circuit opens the door to self-healing applications and enhanced reliability. In this line, we develop optimized, minimally intrusive tuning knobs for performance calibration, together with novel performance control algorithms based on machine learning models.

## Research milestones

- Non-intrusive mm-wave test: we have outlined and experimentally demonstrated a machine learning-based non-intrusive test methodology for mm-Wave circuits.
- Advanced modeling of mm-wave couplers for design enhancement: design-oriented model considering frequency-dependent electrical losses.
- Inversion-based design methodology for low-power LNA design.
- Design-oriented modeling of short-channel MOS transistors: based on the ACM model, we have developed a 7-parameter MOS transistor DC model including the main short-channel effects in advanced nanometric technologies.
- Quantum dot test structures have been fabricated in FD-SOI technology and the characteristic Coulomb blockade diagrams have been successfully measured.
- Ultra low-power and area-efficient high resolution analog to digital converter
- Low noise read-out for integrated quantum random number CMOS sensors
- First-ever OBT technique for mm-wave circuits: we have demonstrated the potential of Oscillation-Based Test techniques for the test and calibration of phased arrays.
- Development of Embedded Test Instruments for the static and dynamic test of state-of-the-art ADCs and for the characterization of clock jitter.
- Development of machine learning-based image quality evaluation and correction techniques.
- Low-cost controller synthesis: we have developed a software platform for automatic generation of logic control codes for a wide variety of low-cost microcontroller targets.
- Scheduling control for lifetime optimization in Wireless Sensor Nodes technologies: we have proposed a novel solution to the Maximum Lifetime Coverage Problem (MLCP) that takes into account the non-zero energy of nodes in sleep mode.

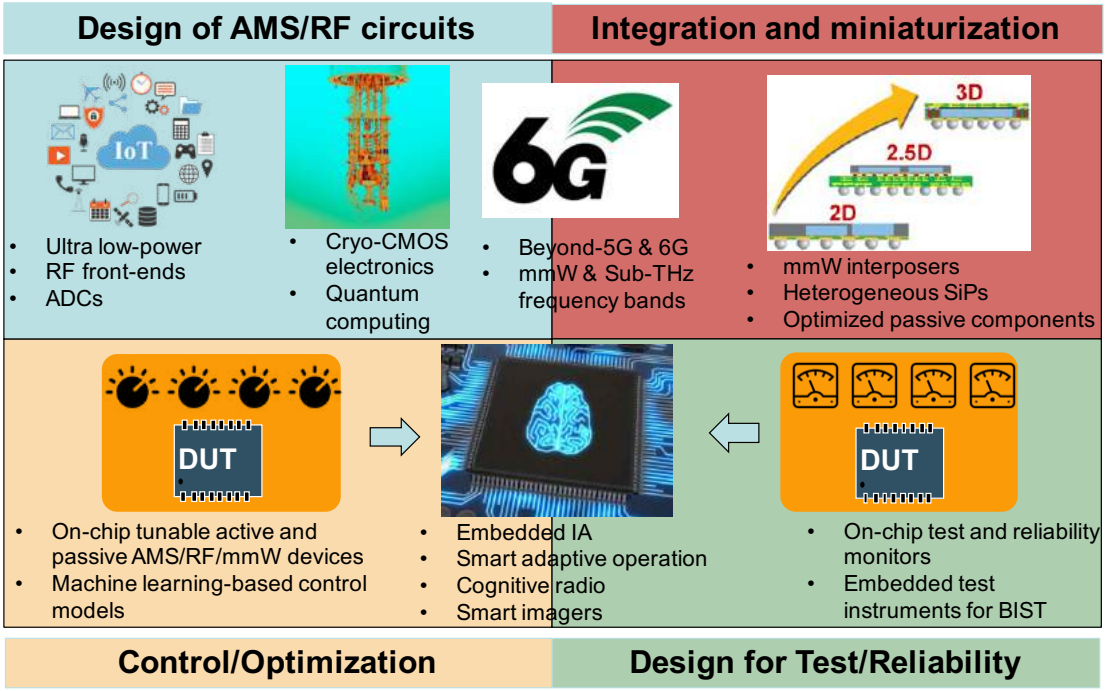



Figure 1: **R**MS research activities at a glance

# Recent highlights

## International Cooperation

**CETIC project : Low cost controller design; Embedded Programmable circuits (FPGA) (Youndé - CAMEROON)**
Scientific Manager: Emmanuel SIMEU
Partners: University of Yaoundé I
City: Yaoundé
Country: CAMEROON
Start the: Jan 01, 2016 until Dec 31, 2022

**Conception de bits quantiques sur silicium**
Scientific Manager: Salvador MIR
Partners: Université de Sherbrooke
City: Sherbrooke
Country: CANADA
Start the: Oct 25, 2018 until Apr 30, 2022

**GISS project (Ghana Instrumentation Sensors and Systems)**
Scientific Manager: Daniel DZAHINI
Partners: Ashesi University
City: Berekuso
Country: GHANA
Start the: May 17, 2022 until May 17, 2024

## May 11, 2022: Best Paper Award at TMREES22 for RMS team

Best Paper Award at TMREES22 for Abdelali AGOUZOUL, Badr CHEGARI, Mohamed TABAA and Emmanuel SIMEU

*“A Neural Network Model-Based Predictive Control Model to improve the energy performance of buildings”*

TMREES22: Technologies and Materials for Renewable Energy, Environment and Sustainability (
Place: Metz (France)

European Academy for Sustainable Development

Best Paper Award

The European Academy for Sustainable Development Best Paper Award for the Best Paper Published in Tmrees22Fr was awarded to

Author/s: Abdelali Agouzoul, Badr Chegari, Mohamed Tabaa and Emmanuel Simeu

Title: A Neural Network Model-Based Predictive Control Model to improve the energy performance of buildings

International Conference on
Technologies and Materials for Renewable Energy, Environment and Sustainability
TMREES22Fr Int'l Conf. Metz-Grand Est - France. 09-10-11 May, 2022.

European Academy for Sustainable Development
EURACA. Decree 618559064

Chafic-Touma Salamé

## December 8, 2022: Seminar by Prof. Abhijit CHATTERJEE (School of ECE, Atlanta - USA)

*"Machine Learning Driven AMS Validation, Test and Tuning: Pre Through Post-Silicon"*
By Abhijit CHATTERJEE, School of ECE, Georgia Institute of Technology, Atlanta, GA
Introduced by Manuel BARRAGAN (RMS team)

## Academic and research members

### Jean-Daniel ARNOULD

**Position**
Associate Professor at Grenoble INP - Phelma school

**Responsibilities**
Researcher in RMS team

### Manuel BARRAGAN

**Position**
Researcher at CNRS

**Responsibilities**
Leader of RMS team
Researcher in RMS team

### Sylvain BOURDEL

**Position**
Full professor at Grenoble INP – Phelma school

**Responsibilities**
Researcher in RMS team

### Daniel DZAHINI

**Position**
Research engineer at CNRS

**Responsibilities**
Researcher in RMS team

### Philippe FERRARI

**Position**
Full professor at UGA – IUT1

**Responsibilities**
Researcher in RMS team

### Estelle LAUGA-LARROZE

**Position**
Associate professor at UGA – IUT1

**Responsibilities**
Researcher in RMS team

### Salvador MIR

**Position**
Research Director at CNRS

**Responsibilities**
Researcher in RMS team

### Emmanuel PISTONO

**Position**
Associate professor at UGA – IUT1

**Responsibilities**
Researcher in RMS team

### Florence PODEVIN

**Position**
Full professor at Grenoble INP – Phelma school

**Responsibilities**
Researcher in RMS team

### Emmanuel SIMEU

**Position**
Associate Professor at UGA – Polytech school

**Responsibilities**
Researcher in RMS team

*CNRS (French National Center for Scientific Research)*
*Grenoble INP (Grenoble Institute of Technology)*
*PHELMA school (Physique-Electronique-Matériaux)*
*POLYTECH school (École Polytechnique de l'Université Grenoble Alpes)*
*UGA (Université Grenoble Alpes)*

## Ph. D. candidates

### 1. AGOUZOUL Abdelali
Title of thesis: **Synthesis of optimized control system of alternative energies for the building**
Expected date of defence: **2024**
Previous degrees: Engineer – EMSI (École Marocaine des Sciences de l'Ingénieur) - Casablanca, Maroc (2021)

### 2. BELKHADRA Oumayma
Title of thesis: **Self-tuning power amplifier in advanced CMOS technology for automotive radar**
Expected date of defence: **2024**
Previous degrees: Engineer – Enseirb-Matmeca - Bordeaux, France (2020)

### 3. BENDJEDDOU Imadeddine
Title of thesis: **Energy-efficient wake-up radio system based on spintronic devices**
Expected date of defense: **2023**
Previous degrees: Master – UGA (Université Grenoble Alpes) – France (2019)

### 4. BONTEMS William Illich
Title of thesis: **Design of a 15-bit analog to digital converter for ultra low power applications**
Expected date of defense: **2023**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

### 5. BOUCHOUCHA Mohamed Khalil
Title of thesis: **Design methodology based on the inversion coefficient for RF and mmW circuits optimization using 28 nm FDSOI technology**
Expected date of defense: **2024**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

### 6. BOUZAR Tarek
Title of thesis: **Contribution to the design of miniature high frequency probes for precision microwave measurements on silicon wafers**
Expected date of defense: **2025**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2022)

### 7. BRITTON OROZCO Giovani Crasby
Title of thesis: **Design of an FD-SOI read / control circuit dedicated to the field of quantum computing under Cryogenic conditions**
Expected date of defense: **2023**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2020)

### 8. CHEGARI Badr
Title of thesis: **Contribution towards integrating optimal energy management systems for intelligent buildings**
Completed on: **July 28, 2022**
Previous degrees: Master - Université Ibn Zohr, Maroc (2017)

### 9. EL CHAAR Mohamad
Title of thesis: **Design Tools for Millimeter Wave Ultra Wideband Distributed Amplifiers**
Completed on: **September 29, 2022**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2019)

### 10. GOMES Leonardo
Title of thesis: **Voltage-controlled oscillator for high-performance mmW beam-steering front-end**
Completed on: **December 13, 2022**
Previous degrees: Master - São Paulo University - São Paulo, Brazil (2019)

### 11. HAI Joycelyn
Title of thesis: **RF Reliability in C065SOI FEM mmW : Device Model and Application to Power Amplifier**
Expected date of defense: **2023**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

### 12. IBRAHIM Sana
Title of thesis: **Clock Generation For Low Power Receiver based on N-Path Mixers**
Expected date of defense: **2023**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2020)

### 13. KRIEKOUKI Ioanna
Title of thesis: **Industrial approach to quantum dots in fully-depleted silicon-on-insulator devices for quantum information applications**
Completed on: **December 14, 2022**
Previous degrees: Master – Université Grenoble Alpes, France (2017)

### 14. MADHVARAJ Manasa
Title of thesis: **IPS for mixed-signal/high speed integrated circuits dependability and control**
Expected date of defense: **2023**
Previous degrees: Master SJCE, Visvesvaraya Technological University – Mysore, India (2015)

### 15. MALBEC Pierre
Title of thesis: **Analysis of the pollutions of a switch mode power supply on a Bluetooth Low Energy type Radio Frequency transmitter embedded on a same System on Chip**
Expected date of defense: **2023**
Previous degrees: Master – Université de Montpellier – France (2020)

### 16. MAMGAIN Ankush
Title of thesis: **On-chip generation of high-frequency sinusoidal signals using harmonic cancellation techniques**
Expected date of defense: **2023**
Previous degrees: Master MTech – IIIT Delhi - New Delhi, India (2018)

### 17. MOHSEN Fadel
Title of thesis: **HRNPM_based low power receivers - Spintronic diodes based wake-up radios**
Expected date of defense: **2023**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2022)

### 18. NAOUI Ayoub
Title of thesis: **Integration of RF switches based on chalcogenide phase change materials: application to millimeter wave imaging**
Expected date of defense: **2024**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2021)

### 19. OCCELLO Olivier
Title of thesis: **Self-learning self-test and self-calibration for integrated millimeter-wave systems**
Expected date of defense: **2023**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2020)

### 20. OUATTARA David
Title of thesis: **Design of phase shifters based on new architectures for mm-wave applications: 5G/6G & automotive radar**
Expected date of defense: **2023**
Previous degrees: Bordeaux INP - ENSEIRB-Matméca Talence - Bordeaux, France (2019)

### 21. PINO MONROY Dayana Andrea
Title of thesis: **RF design methodology based on MOS transistors for circuit / technology optimization**
Expected date of defense: **2023**
Previous degrees: Master WICS UGA – (Université Grenoble Alpes) – France (2019)

### 22. POUPON Julien
Title of thesis: **Study of the Gm/ID design methodology for low-power RF/mmW frequency synthesizers in SOI technology**
Expected date of defense: **2025**
Previous degrees: Engineer – Bordeaux INP - ENSEIRB-Matméca Talence - Bordeaux, France (2022)

### 23. TROUSSIER Chloé
Title of thesis: **Study of ESD/CDM stresses phenomena from elementary charged devices to package discharge**
Completed on: **May 12, 2022**
Previous degrees: Engineer – Télécom Bretagne - Brest, France (2018)

### 24. WEHBI Mohammed
Title of thesis: **Design of patch filters for millimeter-wave applications in BiCMOS 55-nm technology**
Expected date of defense: **2023**
Previous degrees: Master - Arab University of Beyrouth - Lebanon (2017)

## Other members

### Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. CORSI | Jordan | FRANCE | 7,5 months |
| 2. EL CHAAR | Mohamad | LEBANON | 3 months |
| 3. KRIEKOUKI | Ioanna | GREECE | 6 months |
| 4. SUBIAS | Serge | FRANCE | 8 months |

### Visitors

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. GALUP | Carlos | BRAZIL | 1 month |
| 2. LACORTE CANIATO SERRANO | Ariana Maria Da Conceiçao | BRAZIL | 15 days |
| 3. LELLOUCH | Alexandre | FRANCE | 8 months |
| 4. LISBOA DE SOUZA | Antonio Augusto | BRAZIL | 10 months |
| 5. MARGALEF ROVIRA | Marc | SPAIN | 4 months |
| 6. PLAMPLONA REHDER | Gustavo | BRAZIL | 15 days |
| 7. SCHOULTEN | Felipe | BRAZIL | 4 months |

### Trainees

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. AKARRACHI | Widad | FRANCE | 2 months |
| 2. ALSUKOUR | Mohammad | FRANCE | 2 months |
| 3. AYLAR | Mehmet | FRANCE | 1 month |
| 4. BARBOSA DE ALMEIDA CAVALCANTI | Maria Eduarda | BRAZIL | 2 months |
| 5. BOUKHEZAR | Larbi | ALGERIA | 12 months |
| 6. BOUZAR | Tarek | ALGERIA | 3 months |
| 7. CHAHBOUNE | Oussama | FRANCE | 3 months |
| 8. DOBRIN | Catalin Andrei | FRANCE | 2 months |
| 9. FOURCADE | Léandre | FRANCE | 2 months |
| 10.GRANADOS | Irwin | FRANCE | 2 months |
| 11.HASSOUN | Khodor | FRANCE | 1 month |
| 12.HOURDRY | Benjamin | FRANCE | 3 months |
| 13.JEANNIN | Lucie | FRANCE | 3 months |
| 14.KHIBANE | Nouhaila | FRANCE | 2 months |
| 15.KONAN | Serge | COTE D'IVOIRE | 3 months |
| 16.LI | Xiao | FRANCE | 2 months |
| 17.MEDBOUHI | Mohammed | MOROCCO | 2 months |
| 18.MEKHALDI | Amine | FRANCE | 2 months |
| 19.MO | Manqi | CHINA | 3 months |
| 20.MOHSEN | Fadel | FRANCE | 1 month |
| 21.POUZOU | Christopher | FRANCE | 1 month |
| 22.SIMIONATO | ELIGIA | BRAZIL | 15 days |
| 23.SRINIVASSANE | Naveen | FRANCE | 1 month |
| 24.XUAN | Hanwen | FRANCE | 2 months |
| 25.ZIDANE | Hajar | FRANCE | 2 months |

## Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2022.

### ANR

**MASHWaves (2022 – 2024)**
Title: MAchine learning-based Self-Healing of mmW ICs
Scientific manager: Manuel BARRAGAN

**NPATH LOW-POWER (2022 - 2024)**
Scientific manager: Florence PODEVIN

### ANRT

**CIFRE Giovanni BRITTON (2020 – 2023)**
Scientific manager: Salvador MIR
Industrial partner: STMicroelectronics

**CIFRE Ioanna KRIEKOUKI (2018 – 2022)**
Title: Fabrication et caractérisation de bits quantiques avec contrôle embarqué en technologie 28nm UTBB FD-SOI et au-delà à température cryogénique
Scientific manager: Salvador MIR
Industrial partner: STMicroelectronics

### COLLECTIVITES TERRITORIALES

**MESSI (2019 – 2022)**
Programme : nano 2022
Title : Mixed-Signal Self-Test IPs for on-chip testing and technology qualification
Scientific manager: Salvador MIR

### INTERNATIONAL

**SWAN-on-chip (2022 – 2025)**
Scientific manager: Florence PODEVIN

## Organization and participation of international conferences, workshops, forums

**27th IEEE European Test Symposium (ETS'2022)**
May 23-27, 2022, Barcelona, SPAIN
Rank: A
program chair: MIR Salvador
program committee: BARRAGAN Manuel

**28th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2022)**
September 12-14, 2022, Torino, ITALY
Rank: B
program committee: BARRAGAN Manuel, MIR Salvador, SIMEU Emmanuel

**20th IEEE International NEWCAS Conference (NEWCAS'2022)**
June 19-22, 2022, Québec, CANADA
publicity chair: BOURDEL Sylvain

**30th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC'2022)**
October 3-5, 2022, Patras, GREECE
publicity chair: MIR Salvador
steering committee: MIR Salvador

**40th IEEE VLSI Test Symposium (VTS'2022)**
April 25-27, 2022, San Diego (CA), USA
technical committee: BARRAGAN Manuel, MIR Salvador

## Responsibilities

| Role | TIMA member | Starts | Ends | Comments |
|---|---|---|---|---|
| **Faculties / Schools** | | | | |
| **Polytech Grenoble<br>École Polytechnique de l'Université Grenoble Alpes** | | | | |
| Manager of Risks Prevention department | SIMEU Emmanuel | 01/09/2017 | | |
| Restricted council member | SIMEU Emmanuel | 01/09/2017 | | Examine promotion files, invited professors, teaching assistants |
| School council member | SIMEU Emmanuel | 01/09/2017 | | Elected members - School Strategy, relations with industrial partners |
| **Research structures** | | | | |
| **EEATS doctoral school<br>Électronique, Électrotechnique, Automatique, Traitement du Signal** | | | | |
| Council member of EEATS doctoral school | SIMEU Emmanuel | 01/09/2017 | | |
| **S.mart Grenoble Alpes** | | | | |
| Manager of CIM S.mart platform | SIMEU Emmanuel | 01/09/2015 | | |

# Scientific production

## International journals (RI)

**RI-18 El Chaar Mohamad, Vincent Loïc*, Arnould Jean-Daniel, Lisboa de Souza Antonio Augusto**, Bourdel Sylvain, Podevin Florence**
Accurate Design Method for Millimeter Wave Distributed Amplifier Based on Four-Port Chain (ABCD) Matrix Model
IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: Early access, 2022
**Centre Interuniversitaire de Micro-Electronique, **Centro de Energias Alternativas e Renováveis Laboratoire*

**RI-19 Acri Giuseppe*, Corsi Jordan, Podevin Florence, Pistono Emmanuel, Ferrari Philippe, Boccia Luigi****
A Sensitivity Study of Butler Matrices: Application to an SIW Extended Beam Matrix at 28 GHz
IEEE Access, Volume: 10, pp. 101972 - 101987, 2022
**NXP semiconductors (Toulouse, France), **DIMES - Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica*

**RI-20 Agouzoul Abdelali*, Tabaa Mohamed*, Chegari Badr, Mhenni Meryem*, Simeu Emmanuel, Dandache Abbas**, Alami Karim***
Design and Study of a Digital Energy Building: Case of Morocco
Journal of Ubiquitous Systems & Pervasive Networks , Volume: 16, pp. 71-76, 2022
**Laboratoire Pluridisciplinaire de recherche et innovation , **LGIPM - Laboratoire de Génie Informatique, de Production et de Maintenance*

**RI-21 Britton Orozco Giovani Crasby*, Britton Orozco Giovani Crasby, Lauga-Larroze Estelle, Mir Salvador, Galy Philippe***
Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables
Solid-State Electronics , Volume: 194, pp. 108340, 2022
**STMicroelectronics [Crolles]*

**RI-22 Pino Monroy Dayana Andrea*, Pino Monroy Dayana Andrea, Scheer Patrick*, Bouchoucha Mohamed Khalil*, Bouchoucha Mohamed Khalil, Galup-Montoro Carlos**, Barragan Manuel, Cathelin Philippe*, Fournier Jean-Michel, Cathelin Andreia*, Bourdel Sylvain**
Design-Oriented All-Regime All-Region 7-Parameter Short-Channel MOSFET Model Based on Inversion Charge
IEEE Access, Volume: 10, pp. 86270-86285, 2022
**STMicroelectronics [Crolles], **UFSC - Universidade Federal de Santa Catarina = Federal University of Santa Catarina [Florianópolis]*

**RI-23 Zahran Sherif*, Moscato Stefano**, Fonte Alessandro**, Oldoni Matteo***, Traversa Antonio A.**, Tresoldi Dario**, Ferrari Philippe, Amendola Giandomenico*, Boccia Luigi***
Flippable and Hermetic E -Band RWG to GCPW Transition With Substrate Embedded Backshort
IEEE Transactions on Microwave Theory and Techniques, Volume: , pp. 1-12, 2022
**Millimeter-wave Antennas and Integrated Circuits Laboratory , **SIAE Microelettronica [Milan], ***Dipartimento di Elettronica, Informazione e Bioingegneria (POLIMI)*

**RI-24 Saadi Abdelhalim*, Margalef-Rovira Marc**, Amara Youcef, Vincent Loïc***, Lepilliet Sylvie**, Gaquière Christophe**, Ferrari Philippe**
Innovative millimetre-wave resonators based on slow-wave coplanar stripline components
IET Microwaves Antennas and Propagation, Volume: 16, pp. 477-488, 2022
**NXP Semiconductors (Eindhoven, Netherlands), **Institut d'électronique, de microélectronique et de nanotechnologie, ***Centre Interuniversitaire de Micro-Electronique*

**RI-25 El Chaar Mohamad, Podevin Florence, Bourdel Sylvain, Lisboa de Souza Antonio Augusto*, Arnould Jean-Daniel**
Integrated Stacked Parallel Plate Shunt Capacitor for Millimeter-Wave Systems in Low-Cost Highly Integrated CMOS Technologies
IEEE Solid-State Circuits Letters, Volume: 5, pp. 114-117, 2022
**UFPB - Universidade Federal da Paraiba*

**RI-26 Kriekouki Ioanna*, Kriekouki Ioanna, Kriekouki Ioanna**, Beaudoin Félix***, Philippopoulos Pericles***, Zhou Chenyi***, Camirand-Lemyre Julien**, Rochette Sophie**, Mir Salvador, Barragan Manuel, Pioro-Ladrière Michel**, Galy Philippe***
Interpretation of 28 nm FD-SOI quantum dot transport data taken at 1.4 K using 3D quantum TCAD simulations
Solid-State Electronics , Volume: 194, 2022
**STMicroelectronics [Crolles], **Institut Quantique [Sherbrooke], ***Nanoacademic Technologies Inc.*

**RI-27 Corsi Jordan, Plamplona Rehder Gustavo*, Ferrari Philippe, Lacorte Caniato Serrano Ariana Maria Da Conceiçao*, Pistono Emmanuel**
Modeling and Design of a Partially Air-Filled Slow Wave Substrate Integrated Waveguide
IEEE Transactions on Microwave Theory and Techniques, Volume: , pp. 1-13, 2022
**University of Sao Paulo*

**RI-28 Mota Frutuoso Tadeu*, Lé Joao**, Berthoud Yoann***, Mota Pinheiro Julio**, Margalef-Rovira Marc****, Ferrari Philippe, Plamplona Rehder Gustavo**, Lacorte Caniato Serrano Ariana Maria Da Conceiçao****
Nanowire-Based 3-D Transmission-Line Transformer for Millimeter-Wave Applications
IEEE Microwave and Wireless Components Letters, Volume: 32, pp. 1171-1174, 2022
**Laboratoire d'Electronique de Technologie de l'Information, **Escola Politecnica da Universidade de Sao Paulo [Sao Paulo], ***Laboratoire de Génie Electrique de Grenoble, ****Institut d'électronique, de microélectronique et de nanotechnologie*

**RI-29 Agouzoul Abdelali, Chegari Badr, Tabaa Mohamed*, Simeu Emmanuel**
Using neural network in a model-based predictive control loop to enhance energy performance of buildings
Energy Reports, Volume: 8, pp. 1196-1207, 2022
**Laboratoire Pluridisciplinaire de recherche et innovation*

## Invited conference talks (INV)

**INV-2 Mir Salvador**
Advanced Built-In Test for AMS/RF circuits: industrial solutions and future directions
IEEE CASS Rio Grande do Sul Chapter 2022, 2022

**INV-3 Mir Salvador**
Cryogenic CMOS circuis for control and readout of spin qubits
Colloque LN2 2022, 2022

**INV-4 Barragan Manuel, Leger Gildas*, Cilici Florent, Lauga-Larroze Estelle, Mir Salvador, Bourdel Sylvain**
Feature selection techniques for indirect test and statistical calibration of mm-wave integrated circuits
27th European Test Symposium (ETS 2022), 2022
**IMSE - Instituto de Microelectronica de Sevilla*

**INV-5 Mangelsdorf Chris*, Madhvaraj Manasa, Mir Salvador, Barragan Manuel, Limori Daisuke**, Nakatani Takayuki**, Katayama Shogo**, Ogihara Gaku**, Zhao Yujie**, Wei Jianglin**, Kuwana Anna**, Kentaroh Katoh**, Hatayama Kazumi**, Kobayashi Haruo**, Sato Keno***, Ishida Takashi***, Okamoto Toshiyuki***, Ichikawa Tamotsu*****
Innovative Practices Track: Innovative Analog Circuit Testing Technologies
40th IEEE VLSI Test Symposium (VTS 2022), 2022
**--, **Gunma University - Department of Computer Science [Gunma Univ.], *** ROHM Semiconductor*

## International conferences (CI)

**CI-35 Occello Olivier, Boukhezar Larbi, Margalef-Rovira Marc*, Barragan Manuel, Durand Cédric**, Vincent Loïc***, Ferrari Philippe**
A 3D slow-wave transmission line approach for the design of Ka-band CMOS compact filters
52nd European Microwave Conference (EuMC 2022), 2022
**Institut d'électronique, de microélectronique et de nanotechnologie, **STMicroelectronics [Crolles], ***Centre Interuniversitaire de Micro-Electronique*

**CI-36 Ramos Sparrow Oswaldo*, Bourdel Sylvain, Jacquemod Gilles**, Gaubert Jean*****
A 6.3 pJ/b Ultra-low Power Energy Detector for Non-Coherent UWB Impulse Radio Receiver
37th Conference on Design of Circuits and Integrated Circuits (DCIS 2022), 2022
**Qualcomm France RFFE SARL, **Laboratoire de Polytech Nice-Sophia, ***Institut Matériaux Microélectronique Nanosciences de Provence*

**CI-37 Leger Gildas*, Gines Arteaga Antonio Jose*, Gutierrez Valentin*, Barragan Manuel**
A methodology for defect detection in analog circuits based on causal feature selection
29th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2022), 2022
**IMSE - Instituto de Microelectronica de Sevilla*

**CI-38 Corsi Jordan, Acri Giuseppe, Moulin Maxime*, Zerounian Nicolas*, Grimault-Jacquin Anne-Sophie*, Vincent Loïc**, Ducournau Guillaume***, Aniel Frédéric*, Podevin Florence, Ferrari Philippe, Pistono Emmanuel**
A Millimeter-Wave Substrate Integrated Waveguide Filter in Si-BCB Technology
51st European Microwave Conference (EuMC 2022), 2022
**Centre de Nanosciences et de Nanotechnologies, **Centre Interuniversitaire de Micro-Electronique, ***Institut d'électronique, de microélectronique et de nanotechnologie*

**CI-39 Troussier Chloé*, Troussier Chloé, Bourgeat Johan*, Simeu Emmanuel, Arnould Jean-Daniel, Jacquier Blaise***
Analysis of input receiver transistors behavior during a CDM event
44th Annual EOS/ESD Symposium (EOS/ESD 2022), 2022
**STMicroelectronics [Crolles]*

**CI-40 Madhvaraj Manasa, Mir Salvador, Barragan Manuel**
A self-referenced on-chip jitter BIST with sub-picosecond resolution in 28 nm FD-SOI technology
IFIP/IEEE 30th International Conference on Very Large Scale Integration (VLSI-SoC 2022), 2022

**CI-41 Zahran Sherif, Boccia Luigi*, Podevin Florence, Ferrari Philippe**
BiCMOS Rat-Race Coupler Based on Slow-Wave CPS Transmission lines for 120 GHz Applications
Microwave Mediterranean Symposium (MMS 2022), 2022
**DIMES - Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica*

**CI-42 Agouzoul Abdelali, Simeu Emmanuel, Tabaa Mohamed***
Building energy consumption enhancement using a neural network based model predictive control synthesis in FPGA
International Conference on Microelectronics (ICM 2022), 2022
**Laboratoire Pluridisciplinaire de recherche et innovation*

**CI-43 Wehbi Mohammed, Margalef-Rovira Marc*, Durand Cédric**, Ferrari Philippe**
Compact Patch-like Bandpass Filter using grounded CSRR on BiCMOS 55nm technology
17th European Microwave Integrated Circuits Conference (EuMIC 2022), 2022
**Institut d'électronique, de microélectronique et de nanotechnologie, **STMicroelectronics [Crolles]*

**CI-44 Saïd Aïcha*, Bossuet Alice*, Bourdel Sylvain, Hameau Frédéric*, Vauché Rémy****
Conception d'une antenne patch en bande millimétrique pour la détection non-invasive des caractéristiques de la peau
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Laboratoire d'Electronique de Technologie de l'Information, **Institut Matériaux Microélectronique Nanosciences de Provence*

**CI-45 Bontems William, Dzahini Daniel**
Design of a high resolution (15bit) ultra-low power column SAR ADC
Space & Scientific CMOS Image Sensors 2022, 2022

**CI-46 Wehbi Mohammed, Margalef-Rovira Marc*, Durand Cédric**, Lepilliet Sylvie*, Lacorte Caniato Serrano Ariana Maria Da Conceiçao***, Ferrari Philippe**
Dual-Band Patch Filter 180/270 GHz on BiCMOS 55nm
IEEE/MTT-S International Microwave Symposium (IMS 2022), 2022
**Institut d'électronique, de microélectronique et de nanotechnologie, **STMicroelectronics [Crolles], ***Escola Politecnica da Universidade de Sao Paulo [Sao Paulo]*

**CI-47 Malbec Pierre*, Arnould Jean-Daniel, Vollaire Christian**, Duchamp Jean-Marc***, Chesneau David***
Intégration d'une alimentation à découpage et d'un émetteur-récepteur Bluetooth Low Energy dans un même système sur puce
Journées Nationales Microondes (JNM 2022) , 2022
**STMicroelectronics [Grenoble], **Ampère, Département Energie Electrique, ***Laboratoire de Génie Electrique de Grenoble*

**CI-48 Siniscalchi Mariana*, Galup-Montoro Carlos**, Bourdel Sylvain, Silveira Fernando***
Limits for Low Supply Voltage Operation of a 5 GHz VCO to Drive a 4-Path Mixer
35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI 2022), 2022
**IIE - Instituto de Ingenierí a Eléctrica Institution , **UFSC - Universidade Federal de Santa Catarina = Federal University of Santa Catarina [Florianópolis]*
**CI-49 Mota Frutuoso Tadeu*, Garros Xavier*, Batude Perrine*, Brunet Laurent*, Lacord Joris*, Sklenard Benoit*, Lapras Valérie*, Fenouillet-Beranger Claire*, Ribotta Mickael*, Magalhaes-Lucas Alexandre*, Kanyandekwe Joël*, Kies Rabah*, Romano Giovanni*, Catapano Edoardo*, Cassé Mickaël*, Lugo-Alvarez José*, Ferrari Philippe, Gaillard Frédéric***
Methodology for Active Junction Profile Extraction in thin film FD-SOI Enabling performance driver identification in 500°C devices for 3D sequential integration
IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits 2022), 2022
**Laboratoire d'Electronique de Technologie de l'Information*
**CI-50 Alshakoush Ali, Ibrahim Sana, Subias Serge, Podevin Florence, Barragan Manuel, Pino Monroy Dayana Andrea, Bendjeddou Imadeddine, Lauga-Larroze Estelle, Fesquet Laurent, Taris Thierry*, Bourdel Sylvain**
N-Path Mixer with Wide Rejection Including the 7th Harmonic for Low Power Multi-standard Receivers
20th IEEE Interregional NEWCAS Conference (NEWCAS 2022), pp. 256-260, 2022
**Laboratoire de l'Intégration du Matériau au Système (Bordeaux)*
**CI-51 Mamgain Ankush, Mir Salvador, Tripathi Jai Narayan*, Barragan Manuel**
On-chip calibration for high-speed harmonic cancellation-based sinusoidal signal generators
IEEE 31st Asian Test Symposium (ATS 2022), 2022
**Indian Institute of Technology Jodhpur*
**CI-52 Moussa Hasan, Ibrahim Sana, Lauga-Larroze Estelle, Podevin Florence, Bourdel Sylvain, Fesquet Laurent**
Self-Timed Ring Oscillators for Non-Overlapping and Overlapping Phases Synthesis
20th IEEE International NEWCAS Conference (NEWCAS 2022), 2022
**CI-53 Gomes Leonardo*, Wang Dongwei**, Palomino Gustavo*, Lé Joao*, Jakoby Rolf**, Maune Holger***, Ferrari Philippe, Lacorte Caniato Serrano Ariana Maria Da Conceiçao*, Plamplona Rehder Gustavo***
Slow-Wave MEMS phase shifter with Liquid Crystal for Reconfigurable 5G
IEEE/MTT-S International Microwave Symposium (IMS 2022), 2022
**Escola Politecnica da Universidade de Sao Paulo [Sao Paulo], **Institute for Microwave Engineering and Photonics, ***Otto-von-Guericke-Universität Magdeburg = Otto-von-Guericke University [Magdeburg]*
**CI-54 Mota Frutuoso Tadeu*, Garros Xavier*, Lugo-Alvarez José*, Kom Kammeugne Roméo*, Mohgouk Zouknak Louis David*, Viey Abygaël*, Vandendaele William*, Ferrari Philippe, Gaillard Frédéric***
Ultra-fast CV methods (< 10µs) for interface trap spectroscopy and BTI reliability characterization using MOS capacitors
IEEE International Reliability Physics Symposium (IRPS 2022), 2022
**Laboratoire d'Electronique de Technologie de l'Information*
**CI-55 Margalef-Rovira Marc*, Margalef-Rovira Marc, Maye Caroline*, Lepilliet Sylvie*, Gloria Daniel*, Ducournau Guillaume*, Gaquière Christophe***
Wideband mm-Wave Integrated Passive Tuners for Accurate Characterization of BiCMOS Technologies
99th ARFTG Microwave Measurement Conference 2022, colocated with IEEE/MTT-S International Microwave Symposium, IMS 2022, 2022
**Institut d'électronique, de microélectronique et de nanotechnologie*

## Books & Edited Publications (L)

**L-1 Ferrari Philippe, Jakoby Rolf*, Karabey Onur Hamza**, Plamplona Rehder Gustavo***, Maune Holger******
Reconfigurable Circuits and Technologies for Smart Millimeter-Wave Systems
, Cambridge University Press, 2022
**Institute for Microwave Engineering and Photonics, **ALCAN Systems GmbH , ***Escola Politecnica da Universidade de Sao Paulo [Sao Paulo], ****Otto-von-Guericke-Universität Magdeburg = Otto-von-Guericke University [Magdeburg]*

## National journals (RN)

**RN-4 Arnould Jean-Daniel, Podevin Florence, Vincent Loïc***
Mesures et modélisation RF de capacités MIM intégrées
J3eA – Journal sur l'enseignement des sciences et technologies de l'information et des systèmes, Volume: 21, pp. 6 pages, 2022
**Centre Interuniversitaire de Micro-Electronique*

## National conferences (CN)

**CN-2 Zahran Sherif*, Podevin Florence, Boccia Luigi*, Ferrari Philippe**
Déphaseur 3-bits en technologie BiCMOS 55nm à 100 GHz
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Millimeter-wave Antennas and Integrated Circuits Laboratory*
**CN-3 Wehbi Mohammed, Margalef-Rovira Marc*, Margalef-Rovira Marc, Durand Cédric**, Lepilliet Sylvie*, Ferrari Philippe**
Filtre patch à structure de type CSRR en technologie BiCMOS 55 nm
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Institut d'électronique, de microélectronique et de nanotechnologie, **STMicroelectronics [Crolles]*
**CN-4 Wehbi Mohammed, Margalef-Rovira Marc*, Margalef-Rovira Marc, Durand Cédric**, Lepilliet Sylvie*, Ferrari Philippe**
Filtre patch bi-bande 180/270 GHz en technologie BiCMOS 55 nm
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Institut d'électronique, de microélectronique et de nanotechnologie, **STMicroelectronics [Crolles]*
**CN-5 Corsi Jordan, Acri Giuseppe, Moulin Maxime, Zerounian Nicolas*, Grimault-Jacquin Anne-Sophie*, Vincent Loïc**, Ducournau Guillaume***, Podevin Florence, Ferrari Philippe, Pistono Emmanuel**
Filtres millimétriques à guides d'ondes intégrés au substrat en technologie BenzoCycloButene sur silicium
XXIIèmes Journées Nationales Microondes (JNM 2022), 2022
**Centre de Nanosciences et de Nanotechnologies, **Centre Interuniversitaire de Micro-Electronique, ***Institut d'électronique, de microélectronique et de nanotechnologie*

**CN-6 Occello Olivier, Margalef-Rovira Marc*, Barragan Manuel, Durand Cédric**, Ferrari Philippe**
Filtre ultra compact à lignes à ondes lentes 3D en technologie BiCMOS à 29 GHz
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Institut d'électronique, de microélectronique et de nanotechnologie, **STMicroelectronics [Crolles]*
**CN-7 Alshakoush Ali, Ibrahim Sana, Subias Serge, Vincent Loïc*, Lauga-Larroze Estelle, Fesquet Laurent, Podevin Florence, Bourdel Sylvain**
Mélangeur N-Path à 5 chemins rejetant jusqu'à l'harmonique 8 inclus pour récepteurs multistandards basse consommation
22èmes Journées Nationales Microondes (JNM 2022), 2022
**Centre Interuniversitaire de Micro-Electronique*
**CN-8 El Chaar Mohamad, Podevin Florence, Bourdel Sylvain, Lisboa de Souza Antonio Augusto*, Arnould Jean-Daniel**
Méthode de conception d'amplificateurs distribués millimétriques basée sur la matrice chaîne (ABCD) 4 ports
22èmes Journées Nationales Microondes, 2022
**UFPB - Universidade Federal da Paraiba*
**CN-9 Corsi Jordan, Doan Phi-Long*, Podevin Florence, Ferrari Philippe, Pistono Emmanuel**
Optimisation d'un filtre passe-bande en guide d'ondes partiellement rempli d'air à effet d'ondes lentes intégré au substrat
22èmes Journées Nationales Microondes (JNM 2022), 2022
**TE-OX*

## Other communications (O)

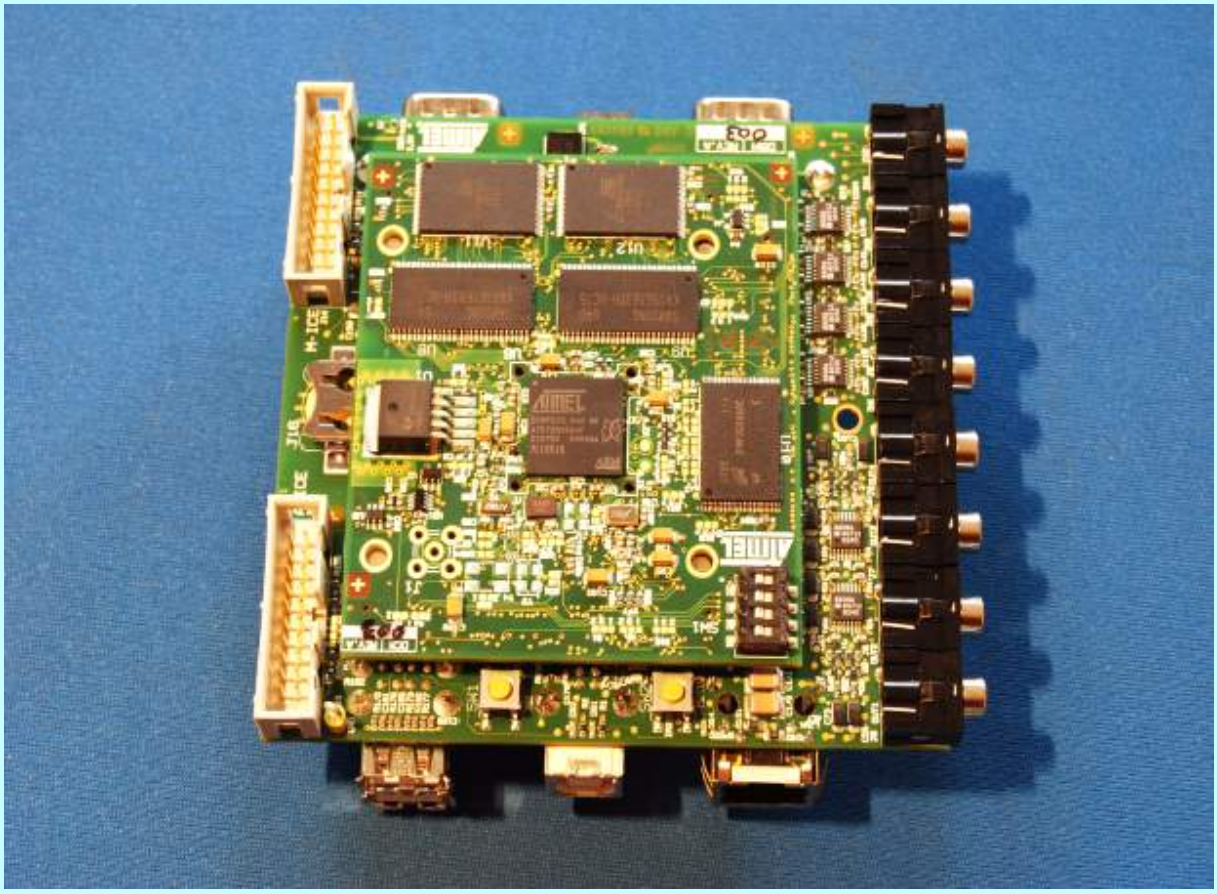
**O-6 Hai Joycelyn, Hai Joycelyn*, Hai Joycelyn**, Cacho Florian*, Divay Alexis*, Lauga-Larroze Estelle, Arnould Jean-Daniel, Forest Jérémie**, Knopik Vincent**, Garros Xavier***
Comprehensive Analysis of RF Hot-Carrier Reliability Sensitivity and Design Explorations for 28GHz Power Amplifier Applications
IEEE International Reliability Physics Symposium (IRPS 2022), Dallas, UNITED STATES, DOI: 10.1109/IRPS48227.2022.9764535
**Laboratoire d'Electronique de Technologie de l'Information, **STMicroelectronics [Crolles]*
**O-7 Britton Orozco Giovani Crasby, Lauga-Larroze Estelle, Mir Salvador, Galy Philippe***
Design methodology of a 28 nm FD-SOI Capacitive Feedback RF LNA based on the ACM Model and Look-up Tables
8th Joint International EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS 2022) , Udine, ITALY
**STMicroelectronics [Crolles]*
**O-8 Kriekouki Ioanna, Beaudoin Félix*, Philippopoulos Pericles*, Zhou Chenyi*, Camirand-Lemyre Julien**, Rochette Sophie**, Mir Salvador, Barragan Manuel, Pioro-Ladrière Michel**, Galy Philippe*****
Interpretation of 28 nm FD-SOI quantum dot transport data taken at 1.4 K using 3D Quantum TCAD simulations
8th Joint International EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS 2022), Udine, ITALY
**Nanoacademic Technologies Inc., **Institut Quantique [Sherbrooke], ***STMicroelectronics [Crolles]*

## Theses (T)

**T-10 Chegari Badr**
Contribution towards integrating optimal energy management systems for intelligent buildings
These de Doctorat, Université Grenoble Alpes, spécialité "", Jul 28, 2022
**T-11 El Chaar Mohamad**
Design Tools for Millimeter Wave Ultra Wideband Distributed Amplifiers
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Sep 29, 2022
**T-12 Gomes Leonardo**
Voltage-controlled oscillator for high-performance mmW beam-steering front-end
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Dec 13, 2022
**T-13 Kriekouki Ioanna**
Industrial approach to quantum dots in fully-depleted silicon-on-insulator devices for quantum information applications
These de Doctorat, Université Grenoble Alpes, spécialité "", Dec 14, 2022
**T-14 Troussier Chloé**
Study of ESD/CDM stresses phenomena from elementary charged devices to package discharge
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", May 12, 2022

TiMA
CNRS — GRENOBLE INP — UGA

# SLS team



## System Level Synthesis

# System Level Synthesis (SLS team)

## Research activities

The SLS team focuses on (a) highly efficient architectures for general purpose computing or AI-dedicated algorithms, (b) system-level modeling and design methodology : specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware. The work of the team is included in the Laboratory themes “Hardware/software codesign” and “Simulation and verification of systems” described below.

### Hardware/software codesign

Our research on high performance general purpose processors explores the use of value prediction in processor design. We have shown that simple value prediction can be implemented by reusing existing pipeline structures, leading to increased performance with reduced overheads. We have also shown that predicting values enables the dynamic "reduction" of some instructions (e g., transforming an add into a nop at runtime), which further improves performance. So far, we have considered value prediction for out-of-order microarchitectures only. In the meantime, through a collaboration with University of Murcia in Spain, we have shown that conservative implementations of atomic read-modify-write instructions (which are used to write higher-level synchronization primitives) in x86 processors incurred significant overhead and proposed a more aggressive implementation to significantly reduce the time spent synchronizing threads.

Multi-core and many-core architectures have evolved towards a set of clusters. Each cluster integrates a set of cores, a cache memory and a local memory shared by all the cores of the cluster. We have worked on hardware methods for distributing memory bank accesses in many-core architectures by experimenting on the MPPA Kalray processor. In addition, we have proposed an innovative hardware support for synchronization locks. This decentralized solution manages dynamic re-homing of locks in a dedicated memory, close to the latest access-granted core.

On the dedicated architecture side, the team is still working on Artificial Intelligence. After our work on high-throughput ternary neural network, we have collaborated with the university of Salerno on the design of a tiny Binary Neural Network for human recognition applications.

Through a collaboration with OVHcloud, we also worked on a dedicated IP used in their mitigation systems to face Distributed Denial-of-Service (DDOS) attacks. In this domain, hard- ware development has to be agile. By introducing the Chisel hardware construction language in the hardware design flow, we showcase how Chisel unleashes the power of agile development methodologies through development iterations. We have also shown through a General Matrix Multiply implementation case study that Chisel can be used to generate highly parametrizable circuits, bringing huge benefits in design exploration, reuse and designer productivity.

### Simulation and verification of systems

Modeling and simulation of cyber-physical devices is challenging because of their heterogeneity: discrete events simulation progresses by discrete timesteps while continuous time simulation does so in a time continuum. The SystemC AMS synchronization strategy is based on fixed timesteps and can generate inaccuracies overcame only at expanse of simulation speed. We have proposed a new continuous time and discrete events synchronization algorithm on top of the SystemC framework and have proven its causality, completeness and liveness. In addition, we have also proposed an adaptive algorithm to adjust the synchronization step to provide near to optimum simulation speed. Results on various cases studies have demonstrated that our algorithm circumvents these challenges, attains high accuracy with respect to established tools, and improves simulation speed. This work aims at enlarging the modeling and simulation capabilities of SystemC as a heterogeneous design tool.

Today’s SoCs require a complex design and verification process. In early design stages, high-level debugging of the SoC functionality is feasible on TLM (Transaction-Level Modeling) descriptions. To ease debugging of such SoC’s models, Assertion-Based Verification (ABV) enables the runtime verification of temporal properties. In the last design stages, RTL (Register Transfer Level) descriptions of hardware blocks expose microarchitectural details. To gain confidence in the validity of system level properties after this TLM-to-RTL synthesis, transaction level assertions must be reverifiable on RTL models. To address that issue, we propose refinement rules for the automatic system level to signal level transformation of PSL assertions (Property Specification Language, IEEE standard 1850).

Many scientific applications require higher accuracy than what can be represented on 64 bits of the floating-point IEEE 754 standard, and to that end make use of dedicated arbitrary precision software libraries such as

MPRF. To reach a good performance/accuracy trade-off, developers use variable precision, requiring e.g. more accuracy as the computation progresses. Hardware accelerators for this kind of computations do not exist yet, and independently of the actual quality of the underlying arithmetic computations, defining the right instruction set architecture, memory representations, etc, for them is a challenging task. We have investigated the support for arbitrary and variable precision arithmetic in a dynamic binary translator (QEMU implementation), to help gain an insight of what such an accelerator could provide as an interface to compilers, and thus programmers. Through collaborations, we also worked on a FP representation supporting both static and dynamically variable precision: by designing its compilation flow to hardware FP instructions or software libraries, and by demonstrating its performance, far better than the Boost programming interface for the MPFR library on the PolyBench suite. Simulations of manycores architectures take a lot of time with gem5 (simulator used for manycores architectures), to improve this point we explore the accuracy of QEMU. QEMU used the DBT (Dynamic Binary Translation) mechanism which transforms instructions from a target ISA to a host ISA. In our experimentations, the target ISA is RISC-V, several of the team works used RISC-V eco-system. To reduce the simulation time of manycores architectures with QEMU, we propose to pin vCPUs (virtual CPUs simulated by QEMU) to physical CPUs on the host,

e.g. forcing vCPU to run on a chosen physical CPU. PARSEC benchmarks are used to obtain results. Unfortunately, pinning vCPUs does not improve the execution time of our programs. Simulators based on the DBT are fast because they focus on instructions and do not modeling architecture. We propose to add the cache representation in QEMU to improve the accuracy.

## Recent highlights

### International Cooperation

**Online learning and prototyping of digital systems**
Scientific Manager: Frédéric ROUSSEAU
Partners: National University Galway
City: Galway
Country: Ireland
Start the: 2017-2024

**Improving performances of general-purpose processors**
Scientific Manager: Arthur PERAIS
Partners: University of Murcia
City: Murcia
Country: Spain
Start the: Oct 2021

### May 18, 2022: Scientific Day: Design Methodologies

These Scientific Days are meant to present the research topics and to disseminate the recent advances of TIMA researchers. These presentations are open to everybody, whether they are members of TIMA or not.
Program: 2022_05_18_sls_design_methodologies.pdf

### November 24, 2022: Talk by Prof. Amro AWAD (NCSU- USA)

"High-Performance and Crash-Recoverable Security Support for Emerging Memory Architectures"
By Prof. Amro AWAD - North Carolina State University (NCSU) – USA
Introduced by Arthur PERAIS (SLS team)

### Reviews in scientific journals

Arthur PERAIS:
- 2 reviews for ACM Transactions on Architecture and Code Optimization (TACO)
- 3 reviews for IEEE Transactions on Computer (TC)

## Academic and research members

### Liliana ANDRADE

**Position**
Associate professor at UGA - Polytech school

**Responsibilities**
Researcher in SLS team

### Julie DUMAS

**Position**
Associate professor at Grenoble INP – Ensimag school

**Responsibilities**
Researcher in SLS team

### Olivier MULLER

**Position**
Associate professor at Grenoble INP – Ensimag school

**Responsibilities**
Leader of SLS team
Researcher in SLS team

### Arthur PERAIS

**Position**
Researcher at CNRS

**Responsibilities**
Researcher in SLS team

### Frédéric PÉTROT

**Position**
Professor at Grenoble INP – Ensimag school

**Responsibilities**
Researcher in SLS team

### Laurence PIERRE

**Position**
Professor at UGA – IM2AG school

**Responsibilities**
Researcher in SLS team

### Frédéric ROUSSEAU

**Position**
Professor at UGA – Polytech school

**Responsibilities**
Researcher in SLS team

*CNRS (French National Center for Scientific Research)*
*ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)*
*Grenoble INP (Grenoble Institute of Technology)*
*IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)*
*POLYTECH (École Polytechnique de l'Université Grenoble Alpes)*
*UGA (Université Grenoble Alpes)*

## Ph. D. candidates

### 1. BADAROUX Marie
Title of thesis: **Fast and accurate simulation of multi/many-core SoCS**
Expected date of defense: **2023**
Previous degrees: Engineer – Grenoble INP – Ensimag - Grenoble, France (2020)

### 2. BAIN Nathan
Title of thesis: **Methods for the learning and adapting formal neural networks to the constraints of hardware accelerators for applications optimized in power and / or throughput**
Expected date of defence: **2023**
Previous degrees: Engineer – Grenoble INP – Phelma - Grenoble, France (2020)

### 3. BONICEL Louis
Title of thesis: **Study of an architectural model for code generation taking into account the real time constraints of an embedded system in the electrical measure and protection domain**
Completed on: **November 23, 2022**
Previous degrees: Engineer – Polytech Montpellier, France (2017)

### 4. BRUANT Jean
Title of thesis: **Abstracting Hardware Architectures for Agile Design of High-performance Applications on FPGA**
Completed on: **December 8, 2022**
Previous degrees: Engineer - Télécom Bretagne – Brest, France (2018)

### 5. CATHELINEAU Benjamin
Title of thesis: **Test and reliability analysis for cyber-physical system models**
Expected date of defense: **2025**
Previous degrees: Master UGA (Université Grenoble Alpes) – Grenoble, France (2022)

### 6. CHRIST Maxime
Title of thesis: **Learning in very low precision**
Expected date of defense: **2023**
Previous degrees: Engineer - INSA Lyon, France (2017)

### 7. DESHPANDE Chandana
Title of thesis: **Building an Efficient 128-bit General Purpose Processor**
Expected date of defense: **2025**
Previous degrees: Master - Visvesvaraya Technological University – Bangalore, India (2014)

### 8. FERRES Bruno
Title of thesis: **Flexible Leveraging Hardware Construction Languages for Design Space Exploration on FPGA**
Completed on: **March 23, 2022**
Previous degrees: Engineer – Grenoble INP - Ensimag, France (2018)

### 9. ISAAC—CHASSANDE Valentin
Title of thesis: **Design of a Memory System for Sparse Data Processing**
Expected date of defense: **2025**
Previous degrees: Master UGA Polytech - Grenoble, France (2022)

### 10. TOMASI RIBEIRO Eduardo
Title of thesis: ***Single address space for massively parallel computers***
Expected date of defense: **2025**
Previous degrees: Engineer – Grenoble INP – Ensimag - Grenoble, France (2019)

### 11. VIANES Arthur
Title of thesis: **Integration of a Manycore Accelerator in a High-Performance Processor**
Expected date of defense: **2023**
Previous degrees: Master UGA Polytech - Grenoble, France (2018)

## Other members

### Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. BAUMELA | Thomas | FRANCE | 12 months |
| 2. PINZARI | Ana | FRANCE | 12 months |
| 3. RAVENEL | Pierre | FRANCE | 15 days |

### Visitors

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. SINGH | Sawan | INDIA | 3 months |

### Trainees

| Name | Forename | Country | Duration |
|---|---|---|---|
| 1. AVDIBEGOVIC | Ugo | FRANCE | 3 months |
| 2. BARBAZA | Valentin | FRANCE | 3 months |
| 3. BESSON | Nicolas | FRANCE | 3 months 8 days |
| 4. BULTINCK | Léonard | FRANCE | 2 months |
| 5. CATHELINEAU | Benjamin | FRANCE | 4,5 months |
| 6. DABADIE | Hugo | FRANCE | 5 months |
| 7. DIDIER | Anthony | FRANCE | 2 months |
| 8. GARCIA DUARTE | Juan Jose | FRANCE | 2,5 months |
| 9. MAGALHAES GOMES DE SOUZA | Gustavo | BRAZIL | 2,5 months |
| 10.MORLIER | Damien | FRANCE | 2,5 months |
| 11.NOIRY | Sylvain | FRANCE | 2,5 months |

## Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2022.

### ANR

**MAPLURINUM (2021 - 2025)**
Title: Machinae pluribus unum - (faire) une seule machine avec plusieurs
Scientific manager: Arthur PERAIS

**RAKES (2019 – 2023)**
Scientific manager: Frédéric PETROT

### ANRT

**CIFRE Nathan BAIN (2020 – 2023)**
Title: Méthodes pour l'apprentissage et l'adaptions des réseaux de neurones formels aux contraintes des accélérateurs matériels pour des applications optimisées en puissance et/ou en débit
Scientific manager: Frédéric PETROT
Industrial partner: STMicroelectronics

**CIFRE Jean BRUANT (2018 – 2022)**
Scientific manager: Olivier MULLER
Industrial partner: OVH

**CIFRE Arthur VIANES (2019 – 2022)**
Scientific manager: Frédéric ROUSSEAU
Industrial partner: Kalray

### CEC-NATIONAL

**AI4DI (2019 – 2022)**
Program: ECSEL
Titre : Artificial Intelligence for Digitizing Industry
Scientific manager: Frédéric PETROT

### EPST

**Digital Hardware AI Architectures (2019 – 2023)**
Program: MIAI (Multidisciplinary Institute in Artificial Intelligence)
Scientific manager: Frédéric PETROT

### INDUSTRY

**Back to the Future (2022 – 2025)**
Partners: Intel Corporation / University of Cyprus
Scientific manager: Arthur PERAIS

## Organization and participation of international conferences, workshops, forums

**Conférence francophone d'informatique en Parallélisme, Architecture et Système (COMPAS'2022)**
July 5-8, 2022, Amiens, FRANCE
reading committee: DUMAS Julie, PERAIS Arthur
Rank: NC

**Design, Automation and Test in Europe Conference (DATE'2022)**
March 14-23, 2022, Virtual event
Rank: A+
topic member: PIERRE Laurence

**25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS'2022)**
April 6-8, 2022, Prague, CZECH REP.
Rank: B
technical committee: PIERRE Laurence

**IEEE International Symposium on High-Performance Computer Architecture (HPCA'2022)**
April 2-6, 2022, Seoul, SOUTH KOREA
Rank: A+
extended technical program committee: PERAIS Arthur
industry technical program committee: PERAIS Arthur

**IEEE International Conference on Computer Design (ICCD'2022)**
October 23-26, 2022, Lake Tahoe, US
Rank: A
technical program committee: PERAIS Arthur

**IEEE/ACM International Symposium on Computer Architecture (ISCA'2022)**
June 18-22, 2022, New York, US
Rank: A+
extended technical program committee: PERAIS Arthur

**IEEE/ACM International Symposium on Microarchitecture (MICRO'2022)**
October 1-5, 2022, Chicago, US
Rank: A+
technical program committee: PERAIS Arthur

**20th Multicore and Multiprocessor SoCs (MPSoCs) Forum**
June 19-24, 2022, Megève, FRANCE
general chair: Frédéric PÉTROT
technical program committee: Frédéric PÉTROT
finance chair: Frédéric ROUSSEAU
local organization: Frédéric ROUSSEAU

**14th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO'2022)**
June 20-22, 2022, Budapest, HUNGARY
technical committee: PETROT Frédéric

**34th International Workshop on Rapid System Prototyping (RSP'2022)**
September 21, 2022, Hamburg, GERMANY
organization committee: MULLER Olivier, ROUSSEAU Frédéric

## Responsibilities

| Role | TIMA member | Starts | Ends | Comments |
|---|---|---|---|---|
| **Faculties / Schools** | | | | |
| **ENSIMAG school<br>École nationale supérieure d'informatique et de mathématiques appliquées de Grenoble** | | | | |
| Deputy Director | PETROT Frédéric | 01/09/2018 | 31/08/2022 | |
| Restricted council member | PETROT Frédéric | 01/09/2017 | | Examine promotion files, invited professors, teaching assistants |
| | MULLER Olivier | 01/09/2017 | | |
| School council member | PETROT Frédéric | 01/09/2017 | | Elected members - School Strategy, relations with industrial partners |
| | MULLER Olivier | 01/09/2017 | | |
| **Polytech Grenoble<br>École Polytechnique de l'Université Grenoble Alpes** | | | | |
| Manager of E2I branch | ANDRADE Liliana | 01/10/2019 | | 5th year - Apprenticeship training |
| Deputy director in charge of education and training | ROUSSEAU Frédéric | 01/09/2018 | | |
| Restricted council member | ROUSSEAU Frédéric | 01/09/2017 | | Examine promotion files, invited professors, teaching assistants |
| School council member | ROUSSEAU Frédéric | 01/09/2017 | | |
| **UFR IM2AG<br>Informatique, Mathématiques et Mathématiques Appliquées** | | | | |
| Research commission member | PIERRE Laurence | 01/09/2017 | | Examine promotion files, invited professors, teaching assistants |
| UFR Council member | PIERRE Laurence | 01/09/2017 | | |
| **TIMA Laboratory** | | | | |
| Scientific animation | ANDRADE Liliana | 01/09/2022 | | |
| Laboratory contact for european projects | ROUSSEAU Frédéric | 01/09/2017 | | |
| **Research structures** | | | | |
| **EEATS doctoral school<br>Électronique, Électrotechnique, Automatique, Traitement du Signal** | | | | |
| HDR commission president | ROUSSEAU Frédéric | 01/01/2020 | | |
| HDR commission member of EEATS doctoral school | ROUSSEAU Frédéric | 01/09/2013 | | |
| **MSTII doctoral school<br>Mathématiques, Sciences et Technologies de l'Information, Informatique** | | | | |
| Council member of MSTII doctoral school | PIERRE Laurence | 01/09/2017 | | |
| HDR commission member of MSTII doctoral school | PETROT Frédéric | 01/09/2017 | | |
| **MSTIC pole<br>Mathématiques, sciences et technologies de l'information et de la communication** | | | | |
| TIMA representative of MSTIC cluster | PETROT Frédéric | 01/09/2016 | | |

# Scientific production

## International conferences (CI)

**CI-56 Singh Sawan*, Perais Arthur, Jimborean Alexandra*, Ros Alberto***
Exploring Instruction Fusion Opportunities in General Purpose Processors
55th IEEE/ACM International Symposium on Microarchitecture (MICRO 2022), 2022
**Universidad de Murcia*

**CI-57 Portas-Pittet Fabien, Pétrot Frédéric**
Fast simulation of future 128-bit architectures
Design, Automation & Test in Europe Conference & Exhibition (DATE 2022), pp. 1131-1134, 2022

**CI-58 Asgharzadeh Ashkan*, Cebrian Juan M.*, Perais Arthur, Kaxiras Stefanos**, Ros Alberto***
Free Atomics: Hardware Atomic Operations Without Fences
International Symposium on Computer Architecture (ISCA 2022), pp. 1-13, 2022
**Universidad de Murcia, **Uppsala University*

**CI-59 Christ Maxime*, Christ Maxime, De Dinechin Florent*, Pétrot Frédéric**
Low-precision logarithmic arithmetic for neural network accelerators
33rd IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2022), 2022
**Systèmes Embarqués audio programmables*

## Book chapters (CH)

**CH-3 Vermesan Ovidiu*, Pétrot Frédéric, Coppola Marcello**, Schneider Mathias***, Höß Alfred*****
Industrial AI Technologies for Next-Generation Autonomous Operations with Sustainable Performance
Industrial AI Technologies for Next-Generation Autonomous Operations with Sustainable Performance, pp. 1-71, 2022
**SINTEF Industry, **STMicroelectronics [Grenoble], ***Ostbayerische Technische Hochschule Amberg-Weiden*

## Theses (T)

**T-15 Bonicel Louis**
Study of an architectural model for code generation taking into account the real-time constraints of an embedded system in the electrical measure and protection domain
These de Doctorat, Université Grenoble Alpes, spécialité "Informatique", Nov 23, 2022

**T-16 Bruant Jean**
Abstracting Hardware Architectures for Agile Design of High-performance Applications on FPGA
These de Doctorat, Université Grenoble Alpes, spécialité "", Dec 08, 2022

**T-17 Ferres Bruno**
Leveraging Hardware Construction Languages for Flexible Design Space Exploration on FPGA
These de Doctorat, Université Grenoble Alpes, spécialité "", Mar 23, 2022

TiMA
CNRS — GRENOBLE INP — UGA

# Laboratory life

# Gender equality committee

TIMA is committed to a policy of gender equality.

Our Parity referent is Elena-Ioana VATAJELU.

All of our job offers start with the following diversity statement:

*“Our laboratory welcomes applicants with diverse backgrounds and experiences.*

*We regard gender equality and diversity as a strength and an asset.”*

# Sustainable development committee

Article 55 of the French law n°2009-967 of August 3, 2009 on the implementation of the Grenelle de l'environnement, known as "Grenelle 1", requires all higher education establishments to implement a sustainable development approach. Our parent institutions are committed to this approach, and have set up initiatives aimed at fighting global warming, respecting the environment, training staff and raising their awareness of social and environmental issues, etc. The laboratory's Sustainable Development Commission extends and adapts these actions at the laboratory level. It proposes measures to the Laboratory Council to minimize our greenhouse gas emissions, raises staff awareness of climate issues, relays information from parent institutions, etc.

The laboratory's Sustainable Development Commission has worked hard to reduce the laboratory's environmental impact in the digital environment (extending the life of equipment, pooling server rooms and equipment, managing the end-of-life of equipment, etc.). From now on, it will be carrying out Greenhouse Gas Emission Assessments, in order to provide the Laboratory Council precise indicators enabling it to steer a policy of reducing our environmental impact. This includes reducing the carbon footprint of our professional trips.

# Communication

## New logo …

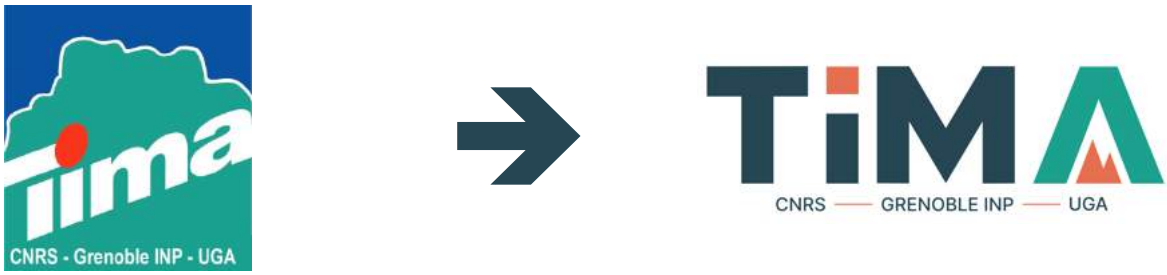
TIMA changed its logo in 2022 !

A first poll was held to decide whether we change our logo or not.

Then, TIMA researchers and support teams had to choose the one they liked the most among 19 different logos. Some were made by UGA Communication Department, or TIMA members.

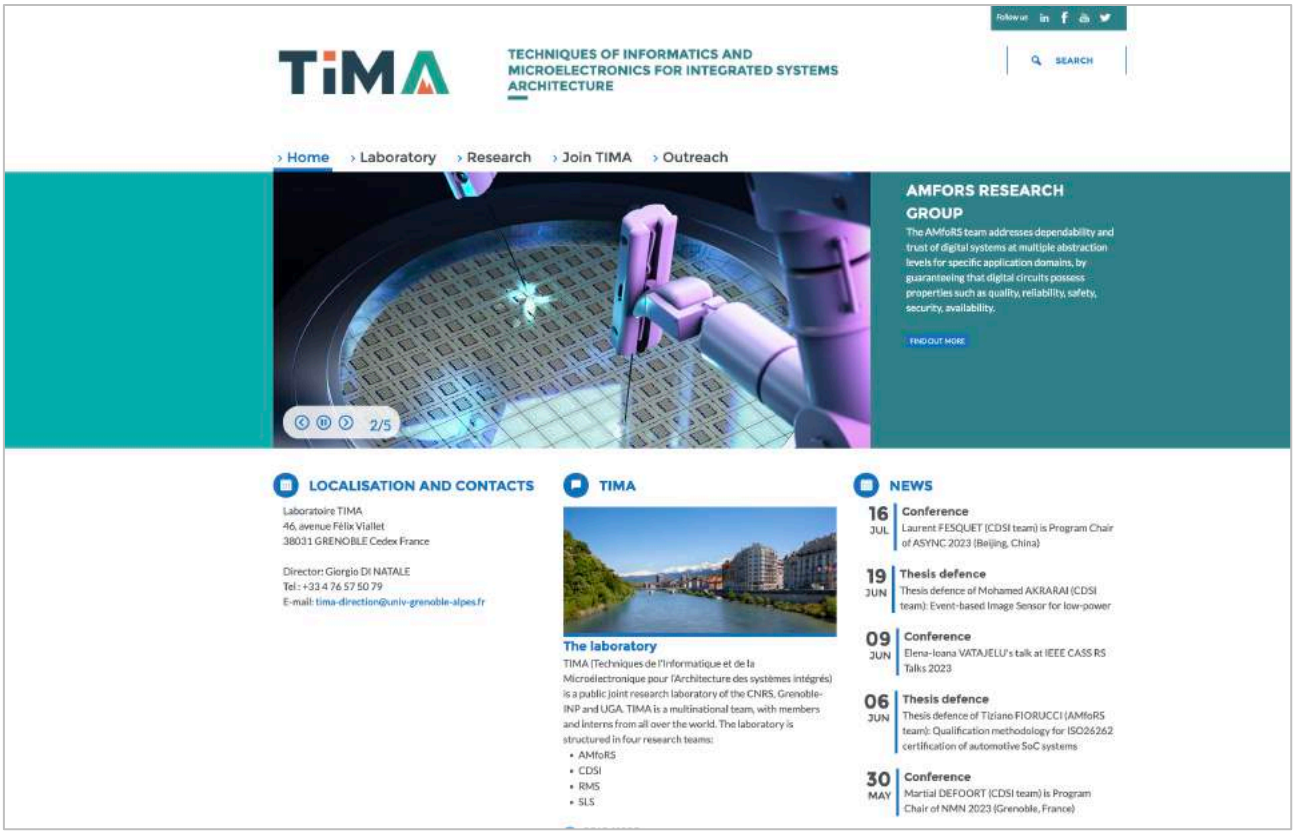
The logo with the highest number of votes was created by one of our doctoral students: Sergio VINAGRERO GUTIERREZ.

Thanks and congratulations to him !




## And new website !

TIMA Laboratory has now a new website that reflects the university's corporate identity.




Visit the new TIMA website !
https://tima.univ-grenoble-alpes.fr/

# Scientific events

## Welcome of newcomers and general assembly

**March 11, 2022**

The welcome of newcomers and general assembly has taken place in Barbillion amphitheater (Grenoble INP).

Morning: presentation of the laboratory and short presentations from newcomers

Afternoon: General Assembly (scientific animation and results, …

## Tribute to François Anceau

**June 14, 2022**

The tribute to François Anceau has taken place in Barbillion amphitheater (Grenoble INP) and also on-line.

This event was organised by IFIP WG10.5 “Design and Engineering of Electronic Systems”, Synopsys, CMP, TIMA, Grenoble INP-UGA and IEEE.

It was called: “Trends on Computing Systems” Day

François Anceau was a pioneer in the design and automation of silicon processors and embedded computing systems. Professor of the ENSIMAG/Grenoble INP Engineering School in the first part of his academic career, he contributed to the creation of a “Grenoble school” on computer architecture in the 70s and early 80s, building a world-wide reputation that has endured until today. Responsible of the Computer Architecture Group of the former Jean Kuntzmann’s LA7 Laboratory until the early 80s, he was the founder of the CMP Service in 1981. His group evolved as part of the TIM3 Laboratory later in the 80s and next formed TIMA Laboratory in the early 90s. In the mid 80s, he joined Bull enterprise in Clayes Sous-Bois where he lead pioneering industrial work on embedded computing systems. Outstanding teacher and prolific researcher, he completed his academic career in the Ecole Polytechnique in Paris from the 90s to the late 00s. Extremely enthusiast and passionate of his field, he collaborated with the CNAM in Paris until his very last days.

This event is a tribute in memory of François Anceau. It includes talks on the past, present and future of embedded computing systems. These talks are given by internationally well-known personalities in the field, complemented with testimonials from François Anceau’s relatives, colleagues and former students.

François Anceau
1940-2020

## TIMA PhD day

**November 25, 2022**

TIMA PhD day has taken place in amphitheater C (Grenoble INP).

TIMA doctoral students had the opportunity to present themselves (studies / past work experience, thesis subject, presentation of their native country).

# Social life / Quality of life at work (QWL)

## Conviviality Day at Château de Vizille

**May 30, 2022**

A conviviality day has been organized on May 30th, 2022.

The laboratory has invited all staff members to discover (or rediscover) the Château de Vizille / Museum of the French Revolution : https://musees.isere.fr/musee/domaine-de-vizille-musee-de-la-revolution-francaise

We have visited the Museum and gardens, and had lunch at the museum's restaurant.





# A step ahead of 2023 …

Here are some news of early 2023 we can't wait to announce in the next annual report !

## Congratulations to Emmanuel SIMEU: appointed Full Professor

**January 19, 2023**
Emmanuel SIMEU was appointed Full Professor at Polytech Grenoble, now part of Grenoble Institute of Engineering and Management of Grenoble INP (part of Grenoble Alpes University).

## Congratulations to Ioana VATAJELU and Mounir BENABDENBI for their HDR theses

Ioana VATAJELU and Mounir BENABDENBI (AMfoRS team) both defended their HDR theses (habilitation to conduct research).

**January 24, 2023**
Ioana VATAJELU - AMfoRS team:
***"Emerging Memories for Dependable Computing"***
https://tima.univ-grenoble-alpes.fr/actualites/hdr-thesis-defence-ioana-vatajelu-amfors-team-emerging-memories-dependable-computing

**February 07, 2023**
Mounir BENABDENBI - AMfoRS team:
***"Contributions to the Test, Fault Tolerance and Approximate Computing of System on a Chip"***
https://tima.univ-grenoble-alpes.fr/actualites/hdr-thesis-defence-mounir-benabdenbi-amfors-team-contributions-test-fault-tolerance-and-approximate

## TIMA Laboratory

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