TIMA Laboratory

2020

Annual report

Contents

TIMA's staff

TIMA's Direction

From 01/01/2015 to 31/12/2020

Salvador MIR
Director

Skandar BASROUR
Deputy Director

Frédéric PÉTROT
Deputy Director

Since 01/01/2021

Giorgio DI NATALE
Director

Laurent FESQUET
Deputy Director

Administrative and Financial pole

Anne-Laure FOURNERET-ITIE
Manager - Human resources - Special events - Communication

Laurence BEN TITO
Executive & laboratory assistant - Publications

Mathilde GARÇON
Budgets, contracts

Aurore GAYRAUD
Teams finance administrator

Youness RAJAB
Teams finance administrator - Common expenses administrator

Computer Service

Frédéric CHEVROT
Manager - Systems, networks and park manager

Nicolas GARNIER
Systems, networks and park manager

Ahmed KHALID
Computer park manager

Development Service

Alice DE BIGNICOURT
Development engineer, webmaster

Mamadou DIALLO
Development engineer

Foreword

TIMA Laboratory is a joint research laboratory between the Centre National de la Recherche Scientifique (CNRS), the Grenoble Institute of Technology (Grenoble INP) and the Université Grenoble Alpes (UGA).

TIMA addresses some of the most urgent and ambitious challenges related to the design of integrated circuits and Systems-on-chip (SoC). The research activities cover the specification, design, verification, test, CAD tools and design methods for integrated systems, including analog and digital components, smart sensors and actuators, up to multiprocessor SoCs together with their operating system. More in particular, researchers at TIMA cover the following topics:

- Low power design
- Asynchronous design
- New sampling and data processing techniques
- MEMS, Smart Sensors and Actuators
- Design of AMS/RF/mmW devices, circuits and systems
- Modeling, control and calibration of AMS/RF devices, circuits and systems
- Robustness, reliability and test
- Hardware security and embedded trust
- New hardware computing and digital design
- Hardware/Software co-design
- Simulation and verification
- Embedded AI

The laboratory is structured in the following four research teams:

Architectures and Methods for Resilient Systems (AMfoRS): Robustness and dependability evaluations of embedded systems; Hardened and robust architecture; Design for reliability with respect to variability, aging, and soft errors; Modeling, analysis and testing at the system level; Hardware security and embedded trust; New computational approaches and technologies

Circuits, Devices and System Integration (CDSI): Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

Reliable RF and Mixed-signal Systems (RMS): Design for test of analog, mixed-signal and RF circuits; Estimation of test metrics; Calibration of RF devices; Embedded control for efficient energy management; Prediction and control of quality and energy management; High-level modeling of heterogeneous and multi-physic systems

System Level Synthesis (SLS): Highly efficient architectures for general purpose computing or AI-dedicated algorithms; system-level modeling and design methodology (specification, simulation and verification of hardware/software systems on chip); design exploration and synthesis of hardware

TIMA takes an active part in the organization of the Grenoble Alpes research community, being linked to the poles "Mathematics, Informatics and Communication" (MSTIC) and "Physics, Engineering and Materials" (PEM). TIMA is also a member of the Carnot Institute LSI, the Laboratory of Excellence Persyval and the local federation of micro and nanoelectronics laboratories FMNT.

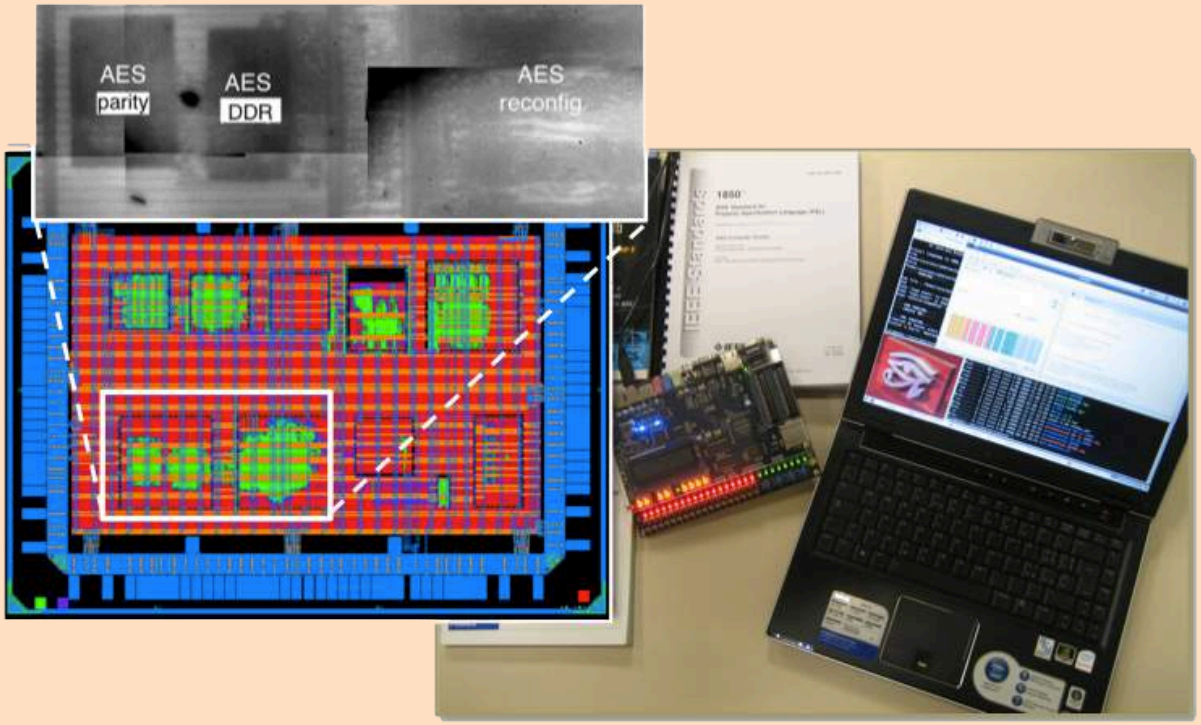
The 2020 edition of the TIMA annual report presents a brief and synthetic presentation of the scientific achievements of each research team.

Salvador MIR
Director from 01/01/2015 to 31/12/2020

Giorgio DI NATALE
Director since 01/01/2021

CNRS - Grenoble INP - UGA

AMfoRS team



Architectures and Methods for Resilient Systems

Architectures and Methods for Resilient Systems (AMfoRS team)

http://tima.univ-grenoble-alpes.fr/tima/fr/amfors/amforsoverview.html

The **AMfoRS** team addresses dependability and trust of digital systems at multiple abstraction levels for specific application domains (e.g., automotive, avionics, smartcards, IoT), by guaranteeing that digital circuits possess properties such as quality, reliability, safety, security, availability. The work of the team is focused on design and analysis methods, techniques and tools to assess and improve circuits dependability and trust, for the above-mentioned domains.

Research activities

Robustness and dependability

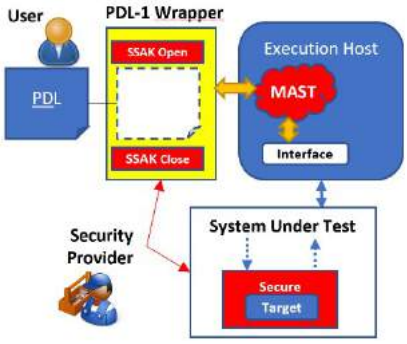
Many domains have functional safety among the classical list of design constraints, e.g. ISO 26262 standard in automotive. Our work aims at improving **early evaluations of dependability** w.r.t. errors induced by environmental disturbances. The goal, to reduce development and production costs, is to be able to evaluate accurately and at an early stage of the design the potential functional effects of soft and permanent errors. We have recently proposed a **cross-layer fault simulation method** to perform the robustness evaluation of RTL architectures used in critical embedded systems, based on both fault simulation in RTL and Transaction Level Model (TLM) descriptions to make a trade-off between simulation time and realism of the simulated high level faulty behaviors, with application to an airborne case study. In the context of **radiation** testing, we have evaluated the vulnerability of hardware-implemented machine learning algorithms, which are finding their way in various domains, including safety-critical applications. Thus, these algorithms have to perform correctly even in harsh environmental conditions, such as in avionics altitudes. Support Vector Machine (SVM) is an important Machine Learning that has been target of hardware implementation in recent years. We have presented the first evaluation of SVMs under thermal neutron radiation along with the first assessment of radiation effects on Multiclass SVMs, proving that Multiclass SVM present an overall higher reliability when compared to a Binary SVM.

We have recently worked on **memory system reliability**, which is a serious concern today and is becoming more worrisome as technology scales, system size grows and the demand of aggressive voltage reduction becomes more stringent. In this context, Error Correcting Codes (ECC)-based repair techniques were proposed and offer aggressive reduction of the repair cost for high defect densities, but this approach suffers from the fact that, single particles induce Single-Event Upsets (SEUs) may lead to Multi-Cell Upsets (MCUs) and Multi-Bit Upsets (MBUs) in the same memory word. Standard mitigating approaches based on interleaving exist, but the impact of MBUs on the repairing circuitry needs also to be mitigated, through a repair Content Addressable Memory (CAM) having interleaving at its data-words, or else an Offset CAM. We have presented and evaluated a novel repair approach based on the Offset CAM in ECC-based Memory Repair and hence permits the mitigation of the MBUs affecting it.

Due to technology scaling and transistor size getting smaller and closer to atomic size, the last generation of CMOS technologies presents more variability in various physical parameters. Moreover, circuit wear-out degradation leads to additional temporal variations, potentially resulting in timing and functional failures. To handle such problems, one conventional method consists in providing more safety margins (also called guard bands) at design-time. Therefore, the usage of delay violation **monitors** becomes a must. Placing the monitors is a critical task as the designer has to carefully select the place that will age the most and may become a potential point of failure in a given design.

We have explored the use of **Machine Learning techniques** in order to drive the automated selection of potential insertion points of such monitors. Digital delay analysis of basic gates using multiple linear regression has been modeled, predicted, and validated against original data using spice simulation. We have compared multiple linear regression algorithms and used them to study the aging mechanism of CMOS basic gates using supervised learning algorithms. We have showed how it is possible to reliably estimate activity-related path aging and tune the prediction framework by extracting activity profiles from simulations on a synthesized design, which allows a finer grain estimation by obtaining activity profiles at both the path and gate-level.

System-level test and standards



The IEEE 1687-2014 standard proposes solutions for the access and usage of Embedded Instruments, but Electronic Design Automation (EDA) is still limited to only a small subset of the new features. In this context, in the frame of the Eureka European project HADES, we improved our innovative Test Flow and Environment called **"Manager for SoC Test" (MAST)**, a software backend able to provide features and performance superior to the industrial legacy solutions. We have proposed an innovative solution that exploits the dynamic nature of the standard to obtain an Authentication-based Secure Access framework able to provide a trusted, configurable, efficient, and transparent interface to the test infrastructure depending on user-defined security levels. Our framework extends MAST with a novel solution developed within the team, the **"*Segment Set Authorization Keys*" (SSAK)** protocol. Security-wise, secret sharing is limited to a minimum; from a performance point of view, the tool fully leverages its strength in terms of topology resolution and concurrent execution. Last but not least, user experience is also optimal, as security is handled automatically and transparently.

Hardware security and trust

The team works on the design of cryptographic/secure primitives, and the analysis of security and trust threats, by proposing effective countermeasures. We work on algorithms, schemes, and protocols, such as the **SSAK protocol** for secure test access (see System- level Test), post-quantum cryptography, homomorphic encryption, and non-linear codes for protecting circuits against fault attacks. Concerning the security threats, we work regularly on implementation attacks. In 2020, we have set up a platform for **side channel attacks** on embedded systems. The environment allows the designer to perform power and EM analysis, and clock and voltage glitch attacks on ARM microcontrollers and FPGA boards. Near-Field EM probes complete the setup, in the LF and RF bandwidths. The platform is going to be extended by supporting EM Fault Injection (EMFI) equipment in the next year. This platform has been partially supported by IRT Nanoelec and by the CNRS (INS2I). In the context of **Control Flow Hardening**, we have proposed the use of nonlinear codes. Hardware-based control flow monitoring techniques enable to detect both errors in the control flow and the instruction stream being executed on a processor. However, these techniques may fail to detect malicious carefully tuned manipulation of the instruction stream in a basic block. We have shown how using a non-linear encoder and checker can cope with this weakness. Concerning the secure primitives, we are currently working on secure elements such as Physically Unclonable Functions to cope with reliability issues, and True Random Number Generators with memristive and spintronic devices. In this context, we have set up an experimental platform, financed by the CNRS/INS2I, for the evaluation of **SRAM-based PUFs**. Concerning the trust issues, we are working on methods to detect and possibly avoid the presence of hardware Trojan horses.

New hardware computing approaches

Today's computing systems are facing several issues related to architectural and technological limitations. To mitigate these issues, novel computing paradigms, such as **Computing-in-Memory**, **Neuromorphic Computing** and **Approximate Computing**, are being researched, in conjunction with novel emerging technologies such as memristive and spintronic devices. Concerning these devices, our research aims at using enhanced compact models to perform failure analysis, and define pertinent fault models to establish design-for-test and design-for-reliability methodologies. Concerning the Computing-in-Memory paradigm, we are investigating feasible design solutions, with a special focus on applications for security. Concerning Neuromorphic Computing, we are focusing on the reliability analysis and test of spiking neural networks. Concerning the Approximate Computing paradigm, which has been gaining momentum both in the industry and in academia, we are studying the trade-offs between selective approximation (or occasional violation of specifications) and power consumption. We are also working on an extension of a tool initially developed for dependability evaluation (EARS) in order to identify from RTL descriptions and a given application the operators that are the less sensitive to approximations.

Recent highlights

New recruitment

- Brice Colombier, Assistant Professor

Dissemination

- Book: **Di Natale G.**, Gizopoulos D., Di Carlo S., Bosio A., Canal R. (Eds.) *Cross-Layer Reliability of Computing Systems*, Ed. IET - The Institution of Engineering and Technology, 2020
- Invited talk: Regazzoni F., […], **Di Natale G.**, […], **Vatajelu I.**, et al., *Machine Learning and Hardware security: Challenges and Opportunities*, International Conference on Computer-Aided Design (ICCAD 2020)
- Keynote: **I. Vatajelu**, *Versatility of Emergent Memory Technologies: Friend or Foe?,*
- The 17th Biennial Baltic Electronics Conference, Tallin 2020

Involvement in research activities

- Participation to the IEEE P1687.1 Working Group
- Participation to the Grenoble Alpes CyberSecurity Institute for post-quantum cryptography

Platforms and demonstrators

- A comprehensive platform for hardware/software co-design based on the RISC-V processor architecture. The platform supports several RISC-V implementations (such as the Rocket Chip or CVA6) and it features high modularity and tuning capabilities (https://tima-amfors.gricad-pages.univ-grenoble-alpes.fr/learnv/)
- Hardware demonstrator for Secure Access to 1687 Test Infrastructure
- Experimental platforms for Side Channel Analysis and PUF evaluation
- Open-source fault injection tool for SNNs

Academic and research members

Lorena ANGHEL

Position
Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team until 31/05/2020

Mounir BENABDENBI

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Brice COLOMBIER

Position
Associate Professor at Grenoble INP - PHELMA school since 01/09/2020

Responsibilities
Researcher in AMfoRS team since 01/09/2020

Giorgio DI NATALE

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team
Director of TIMA Lab. Since 01/01/2021

Régis LEVEUGLE

Position
Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Paolo MAISTRI

Position
Researcher at CNRS

Responsibilities
Leader of AMfoRS team
Researcher in AMfoRS team

Mihail NICOLAIDIS

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team

Michele PORTOLAN

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Rodrigo POSSAMAI BASTOS

Position
Associate Professor at UGA - IM2AG school

Responsibilities
Researcher in AMfoRS team since 01/07/2020

Elena-Ioana VATAJELU

Position
Researcher at CNRS

Responsibilities
Researcher in AMfoRS team

Raoul VELAZCO

Position
Professor Emeritus at CNRS

Responsibilities
Researcher in AMfoRS team since 01/01/2020

Nacer-Eddine ZERGAINOH

Position
Associate Professor at UGA - POLYTECH school

Responsibilities
Researcher in AMfoRS team since 01/01/2020

CNRS (French National Center for Scientific Research)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AIT SAID Noureddine
Title of thesis: **Self adaptive precision in SoCs: design and verification techniques**
Expected date of defense: **2021**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

2. ALI POUR Amir
Title of thesis: **PUF based Secure Computing for Constraint Cyber Physical Object**
Expected date of defense: **2022/2023**
Previous degrees: Engineer (2020)

3. ALSHAER Ihab
Title of thesis: **Cross-Layer Fault Analysis for Microprocessor Architectures (CLAM)**
Expected date of defense: **2023**
Previous degrees: Engineer

4. CINÇON Valérian
Title of thesis: **Ultra low power integration of neuro-morphic systems on FD-SOI**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

5. DADDINOUNOU Salah
Title of thesis: **Test and reliability of spiking neural networks**
Expected date of defense: **2023**
Previous degrees: Engineer (2019)

6. FIORUCCI Tiziano
Title of thesis: **Qualification methodology for ISO26262 certification of automotive SoC systems**
Expected date of defense: **2023**
Previous degrees: Engineer

7. GARAY TRINDADE Matheus
Title of thesis: **Optimization and Qualification of Hardware Machine-Learning Systems under Radiation-Induced Effects**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidade Federal de Santa Maria, Rio Grande do Sul, Brazil (2017)

8. GERBAUD Merlin
Title of thesis: **Hardware Security Techniques for Cryptographic Algorithms taking advantage of In-Memory Computing**
Expected date of defense: **2023**
Previous degrees: Engineer

9. INGLESE Pietro
Title of thesis: **Exploration of security threats in In-Memory Computing Paradigms**
Expected date of defense: **2023**
Previous degrees: Engineer – Politecnico di Torino, Italy (2019)

10. JAAMOUN Amine
Title of thesis: **Strategies for securing a memory hierarchy against software side channel attacks**
Expected date of defense: **2022/2023**
Previous degrees: Master 2 Systèmes électroniques et systèmes informatiques – Université Pierre et Marie Curie Paris 6 (2020)

11. KRAEMER SARZI SARTORI Tarso
Title of thesis: **Mitigation of Space-to-Ground Radiation Effects on Attitude Estimation Algorithms for Inertial Navigation Systems**
Expected date of defense: **2023**
Previous degrees: Engineer – Aerospace engineering – Federal University of Santa Maria, Brazil (2020)

12. LINARES Antoine
Title of thesis: **Flexible Hardware for Intrinsic Secure computing**
Expected date of defense: **2023**
Previous degrees: Engineer

13. MARTINOLI Valentin
Title of thesis: **Secure Processors with respect to Micro Architectural Attacks**
Expected date of defense: **2023**
Previous degrees: Engineer

14. REYNAUD Vincent
Title of thesis: **Secured access to IEEE 1687 test resources and lightweight crypto-processors in the IoT context**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2017)

15. SENTHAMARAI KANNAN Kalpana
Title of thesis: **Performance and Safety/Security Management in automotive and IoT applications**
Expected date of defense: **2021**
Previous degrees: Engineer - Pondichery University, India (2013)

16. SHAH Riddhi
Title of thesis: **HiRel Product Demonstration by Dynamic Wearout Management**
Completed on: **October 5th, 2020**
Previous degrees: Engineer – Nirma University, India (2016)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

No positions in 2020

Visitors

Name	Forename	Country	Duration
1. GUPTA	Vishal	INDIA	3 months
2. HONORIO	Martin	SPAIN	3 months
3. IANNICELLI	Pierpaolo	ITALY	5 months

Trainees

Name	Forename	Country	Duration
1. AFLIHAOU	Houdeifa	ALGERIA	3 months
2. AMANS	Annabel	FRANCE	2 months
3. BOUDIAF	Imene Milissa	ALGERIA	2 months
4. GUIRONNET	Solenn	FRANCE	2 months 14 days
5. HO	Duc Nhan	VIET NAM	5 months
6. JABRANE	Kenza	MOROCCO	3 months
7. LIN	Jiaru	-	2 months
8. LUO	Zhifei	CHINA	2 months
9. MAILLEFERT	Antoine	FRANCE	2 months 8 days
10.MALDANER	LiÃ¨ge	BRAZIL	2 months
11.MESNAGER	Victor	FRANCE	2 months 13 days
12.OLIVEIRA	Alexandre	FRANCE	2 months 13 days
13.PASCAL-VALETTE	Djeson Franck	FRANCE	2 months 13 days
14.VARADARAJULU	Swetha	INDIA	6 months
15.VINAGRERO GUTIERREZ	Sergio	SPAIN	2 months 13 days
16.ZECH	Guillaume	FRANCE	2 months

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANR

EMINENT
Responsable scientifique : VATAJELU Ioana
Durée : 2019 - 2023

ANRT

CIFRE Antoine LINARES
Titre : Flexible Hardware for Intrinsic Secure Computing
Responsable scientifique : DI NATALE Giorgio
Durée : 2020 - 2023

CIFRE Valérian CINCON
Titre : "Etude et intégration de systèmes neuro-morphiques ultra basse consommation en technologie FD-SOI"
Responsable scientifique : ANGHEL Lorena
Durée : 2018 - 2021

CIFRE Riddhi J. SHAH
Titre : "Etude et réalisation de démonstrateurs ayant une gestion dynamique du vieillissement pour les applications exigeant une haute fiabilité"
Responsable scientifique : ANGHEL Lorena
Durée : 2017 - 2020

CEC

QUOG-DP
Programme : ATTRACT Project
Titre : Quantum Optimization of Worldwide LHC Computing Grid data placement
Responsable scientifique : ZERGAINOH Alain Nasserdine
Durée : 2019 - 2020

EPST

CLAM
Programme : Equipe-Action Labex Persyval
Titre : Cross-Layer Fault Analysis for Microprocessor Architectures
Responsable scientifique : MAISTRI Paolo
Durée : 2020 - 2023

AVOCAM
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Analyse de durée de Vie pour l'Optimisation de Calcul Approché Matériel
Responsable scientifique : LEVEUGLE Régis
Durée : 2020 - 2021

State
Responsable scientifique : POSSAMAI BASTOS Rodrigo
Durée : 2020 - 2023

IRT Vision embarquée
Programme : IRT
Responsable scientifique : BENABDENBI Mounir
Durée : 2020 - 2020

EPST (suite)

IRT Cybersécurité
Programme : IRT
Responsable scientifique : MAISTRI Paolo
Durée : 2020 - 2020

IRT Intelligence Artificielle et sécurité matérielle
Programme : IRT
Responsable scientifique : ANGHEL Lorena
Durée : 2020 - 2020

Hardware for spike-coded neural networks exploiting hybrid CMOS non-volatile technologies
Programme : MIAI (Multidisciplinary Institute in Artificial Intelligence)
Responsable scientifique : ANGHEL Lorena
Durée : 2019 - 2020

CADI
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Calcul Approché et Distribué dans les systèmes Intégrés
Responsable scientifique : BENABDENBI Mounir
Durée : 2019 - 2020

CROCHET
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Low Cost Control Flow Checking for Secure Applications Based on Nonlinear Codes
Responsable scientifique : DI NATALE Giorgio
Durée : 2019 - 2020

Cyber@Alpes
Programme : Grenoble Alpes CyberSecurity Institute
Responsable scientifique : MAISTRI Paolo
Co-partage d'équipes (AMfoRS, CDSI)
Durée : 2018 – 2021

EUREKA

HADES
Programme : PENTA
Titre : Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems
Responsable scientifique : MIR Salvador
Co-partage d'équipes (AMfoRS, RMS)
Durée : 2017 - 2020

INDUSTRIE

Processeurs Sécurisés et Attaques de micro architectures
Responsable scientifique : LEVEUGLE Régis
Durée : 2020 - 2023

REGION

MULTIRAD
Programme : Pack Ambition International
Responsable scientifique : POSSAMAI BASTOS Rodrigo
Durée : 2020 - 2021

OVNIPROM
Programme : SCUSI
Titre : "Ordinateur de vol d'un nanosatellite implémenté dans un processeur many-core"
Responsable scientifique : VELAZCO Raoul
Durée : 2017 - 2020

SAFE-AIR
Programme : Pack Ambition Recherche
Titre : Safety Evaluation of Aircraft Systems using Virtual Platforms
Responsable scientifique : LEVEUGLE Régis
Durée : 2017 - 2022

SATT

Ovnipromsat / OVSAT
Responsable scientifique : PANCHER Fabrice
Durée : 2019 - 2020

Organization and participation of international conferences, workshops, forums

16th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA'2020)
December 1-4, 2020, Virtual event from Porto Alegre (Brazil), BRAZIL
Rang : NC
general chair: VELAZCO R.

IEEE International Test Conference (ITC'2020)
November 3-5, 2020, Washington DC, USA
Rang : A+
steering committee member: DI NATALE G.
technical program committee: VATAJELU E.I.

33rd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'2020)
October 19-21, 2020, Frascati (Roma), ITALY
Rang : A
technical program committee: DI NATALE G.

26th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2020)
July 13-15, 2020, Virtual event from Naples (Italy), ITALY
Rang : B
general chair: NICOLAIDIS M.
technical program committee: DI NATALE G., LEVEUGLE R., NICOLAIDIS M., BENABDENBI M
steering committee member: NICOLAIDIS M.

8th Prague Embedded Systems Workshop (PESW'2020)
June 25-27, 2020, Roztoky u Prahy, CZECH REP.
Rang : NC
technical program committee: VATAJELU E.I., DI NATALE G.

25th IEEE European Test Symposium (ETS'2020)
May 25-29, 2020, Tallinn, ESTONIA
Rang : A
program co-chair: VATAJELU E.I.
technical program committee: DI NATALE G., VATAJELU E.I., ANGHEL L.
steering committee member: ANGHEL L., DI NATALE G., VATAJELU E.I.
topic chair: LEVEUGLE R., VATAJELU E.I.
embedded tutorial chair: ANGHEL L.
publication chair: DI NATALE G.

Test Spring School (TSS'2020)
May 22-25, 2020, Tallinn, ESTONIA
Rang : NC
technical program committee: VATAJELU E.I.

23rd Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS'2020)
April 22-24, 2020, Novi Sad, SERBIA
Rang : B
technical program committee: LEVEUGLE R., MAISTRI P., PORTOLAN M., VATAJELU E.I.

38th IEEE VLSI Test Symposium (VTS'2020)
April 5-8, 2020, San Diego, USA
Rang : A
general chair: ANGHEL L.
publication chair: VATAJELU E.I.
technical program committee: DI NATALE G.

15th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS'2020)
April 1-3, 2020, Marrakesh, MOROCCO
Rang : NC
track chair: VATAJELU E.I.
technical program committee: BENABDENBI M., VATAJELU E.I.

21st IEEE Latin-American Test Symposium (LATS'2020)
March 30-April 2, 2020, Jatiúca (Maceió), BRAZIL
Rang : NC
steering committee member: VELAZCO R.
technical program committee: LEVEUGLE R., VELAZCO R.

Design, Automation & Test in Europe (DATE'2020)
March 9-13, 2020, Grenoble, FRANCE
Rang : A+
general chair: DI NATALE G.
publication chair: VATAJELU E.I.
technical program committee: ANGHEL L., PORTOLAN M.
local organization: ANGHEL L.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
PHELMA school PHysique, ÉLectronique, Matériaux				
Board of Directors member	ANGHEL L.	01/09/2017	31/05/2020	Strategy, jobs, promotion files, invited professors, teaching assistants
Co-responsible of SEI branch	BENABDENBI M.	01/09/2017		
Manager of SEOC/PHELMA branch	PORTOLAN M.	01/09/2017		
School council member	ANGHEL L.	01/09/2016	31/05/2020	Elected members - School Strategy, relations with industrial partners
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Manager of Office Automation and Informatics	POSSAMAI BASTOS R.	01/09/2017		Formation à tous les parcours du Département Licence Sciences et Technologies de l'UGA
Research structures				
CIME Nanotech Centre Interuniversitaire de MicroElectronique et Nanotechnologies				
Manager of Design platform	BENABDENBI M.	01/09/2017		
CSUG Centre Spatial Universitaire de Grenoble				
Technical manager	PANCHER F.	02/05/2018		
FMNT Fédération des Micro et Nanotechnologies				
Manager of Microelectronics Axis	ANGHEL L.	01/09/2017	31/05/2020	
MSTIC pole Mathématiques, sciences et technologies de l'Information et de la communication				
Council member of MSTIC cluster	LEVEUGLE R.	01/09/2015		Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC
Parent institutions				
Grenoble INP				
Deputy vice-president for Industry relations	ANGHEL L.	01/09/2017	31/05/2020	

Scientific production

International journals

1 **Morgül M.C., Frontini L., Tunali O., Anghel L., Ciriani V., Vatajelu I., Moritz C.A., Stan M., Alexandrescu D., Altun M.,** Circuit Design Steps for Nano-Crossbar Arrays: Area-Delay-Power Optimization with Fault Tolerance, IEEE transactions on Nanotechnology, Ed. IEEE, Vol. , DOI: 10.1109/TNANO.2020.3044017, décembre 2020
2 **Skaf A., Ezzadeen M., Benabdenbi M., Fesquet L.,** Clocked and event-driven redundant adjustable precision computing, Microelectronics Reliability, Ed. Elsevier, Vol. 111, pp. 113729, DOI: 10.1016/j.microrel.2020.113729, août 2020
3 **Anghel L., Bernasconi A., Ciriani V., Frontini L., Trucco G., Vatajelu I.,** Stuck-At Fault Mitigation of Emerging Technologies Based Switching Lattices, Journal of Electronic Testing: Theory and Applications, Ed. Springer , Vol. , pp. 313–326, DOI: 10.1007/s10836-020-05885-2, juin 2020
4 **Di Natale G., Bolchini C.,** Holding Conferences Online due to COVID-19: The DATE Experience, IEEE Design & Test, Ed. IEEE, Vol. 37, No. 3, pp. 116-118, DOI: 10.1109/MDAT.2020.2995140, juin 2020
5 **Fabero J.C., Mecha H., Franco F., Clemente J.A., Korkian G., Rey S., Cheymol B., Baylac M., Hubert G., Velazco R.,** Single Event Upsets Under 14-MeV Neutrons in a 28-nm SRAM-Based FPGA in Static Mode, IEEE Transactions on Nuclear Science, Ed. IEEE, Vol. 67, No. 7, pp. 1461-1469, DOI: 10.1109/TNS.2020.2977874, mars 2020

Invited conferences talks

1 **Regazzoni F., Bhasin S., Ali Pour A., Alshaer I., Aydin F., Aysu A., Beroulle V., Di Natale G., Franzon P., Hély D., Homma N., Ito A., Jap D., Kashyap P., Polian I., Potluri S., Ueno R., Vatajelu I., Yli-Mäyry V.,** Machine Learning and Hardware security: Challenges and Opportunities, Invited talk (Special Session), International Conference on Computer-Aided Design (ICCAD 2020), San Diego, UNITED STATES, 2 au 5 novembre 2020
2 **Pétrot F., Anghel L., Andrade Porras L.L.,** State of the art in hardware-accelerated neural networks, Invited Talk, Applied Machine Learning Days (AMLD 2020), Lausanne, SWITZERLAND, 27 au 29 janvier 2020

International conferences

1 **Garay Trindade M., Garibotti R.F., Ost L., Letiche M., Beaucour J., Possamai Bastos R.,** Assessment of Machine Learning Algorithms for Near-Sensor Computing Under Radiation Soft Errors, 16th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA 2020), Porto Alegre (Virtual edition), BRAZIL, 1 au 4 décembre 2020
2 **Garay Trindade M., Garibotti R.F., Ost L., Letiche M., Beaucour J., Possamai Bastos R.,** Assessment of Machine Learning Algorithms for Near-Sensor Computing Under Radiation Soft Errors, IEEE International conference on electronics, circuits & systems (ICECS 2020), Glasgow, SCOTLAND, UNITED KINGDOM, 23 au 25 novembre 2020
3 **Roux J., Beroulle V., Morin-Allory K., Leveugle R., Bossuet L., Cezilly F., Berthoz F., Genevrier G., Cerisier F.,** High Level Fault Injection Method for Evaluating Critical System Parameter Ranges, 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2020), pp. 1-4, Glasgow, UNITED KINGDOM, DOI: 10.1109/ICECS49266.2020.9294821, 23 au 25 novembre 2020
4 **Laisne M., Crouch A., Portolan M., Keim M., Von Staudt H.M, Abdalwahab M., Van Treuren B., Rearick J.,** Modeling Novel Non-JTAG IEEE 1687-Like Architectures, International Test Conference (ITC 2020), Washington DC, UNITED STATES, 3 au 5 novembre 2020
5 **Anghel L., Cantoro R., Foti D., Portolan M., Sartoni S., Sonza Reorda M.,** New Perspectives on Core In-field Path Delay Test, International Test Conference (ITC 2020), Washington DC, UNITED STATES, 3 au 5 novembre 2020
6 **Di Natale G., Regazzoni F., Albanese V., Lhermet F., Loisel Y., Sensaoui A., Pagliarini S.,** Latest Trends in Hardware Security and Privacy, IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2020), Rome, ITALY, 19 au 21 octobre 2020
7 **Cinçon V., Vatajelu I., Anghel L., Galy P.,** From 1.8V to 0.19V voltage bias on analog spiking neuron in 28nm UTBB FD-SOI technology, EUROSOI-ULIS 2020, Caen, FRANCE, 1 au 30 septembre 2020
8 **Portolan M., Silveira Feitoza R., Takam Tchendjou G., Reynaud V., Senthamarai Kannan K., Barragan M., Simeu E., Maistri P., Anghel L., Leveugle R., Mir S.,** A Comprehensive End-to-end Solution for a Secure and Dynamic Mixed-signal 1687 System, 2020 International Symposium on On-Line Testing and Robust System Design (IOLTS 2020), Naples (Napoli), ITALY, DOI: 10.1109/IOLTS50870.2020.9159721, 13 au 15 juillet 2020
9 **Papavramidou P., Nicolaidis M., Girard P.,** An ECC-Based Repair Approach with an Offset-Repair CAM for Mitigating the MBUs Affecting Repair CAM, IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS 2020), pp. 1-6, Napoli, ITALY, DOI: 10.1109/IOLTS50870.2020.9159731, 13 au 15 juillet 2020
10 **Portolan M., Reynaud V., Maistri P., Leveugle R.,** Dynamic Authentication-Based Secure Access to Test Infrastructure, European Test Symposium (ETS 2020), Tallin, ESTONIA, 25 mai au 1 juin 2020
11 **Elshamy M., Di Natale G., Pavlidis A., Louërat M.-M., Stratigopoulos H.,** Hardware Trojan Attacks in Analog/Mixed-Signal ICs via the Test Access Mechanism, IEEE European Test Symposium (ETS 2020), Tallinn, ESTONIA, 25 mai au 1 juin 2020
12 **Portolan M., Rearick J., Keim M.,** Linking Chip, Board, and System Test via Standards, European Test Symposium (ETS 2020), Tallinn, ESTONIA, 25 mai au 1 juin 2020
13 **Di Natale G., Keren O.,** Nonlinear Codes for Control Flow Checking, IEEE European Test Symposium (ETS 2020), pp. 1-6, Tallinn, ESTONIA, DOI: 10.1109/ETS48528.2020.9131592, 25 au 29 mai 2020
14 **Ali Pour A., Beroulle V., Cambou B., Danger J.-L., Di Natale G., Hély D., Guilley S., Karimi N.,** PUF Enrollment and Life Cycle Management: Solutions and Perspectives for the Test Community, IEEE European Test Symposium (ETS 2020), Tallinn, ESTONIA, 25 mai au 1 juin 2020
15 **Roux J., Beroulle V., Morin-Allory K., Leveugle R., Bossuet L., Cezilly F., Berthoz F., Genevrier G., Cerisier F.,** Cross Layer Fault Simulations for Analyzing the Robustness of RTL Designs in Airborne Systems, 23rd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS 2020), pp. 1-4, Novi Sad, SERBIE, DOI: 10.1109/DDECS50862.2020.9095559, 22 au 24 avril 2020

Book chapters

1 **Anghel L., Nicolaidis M.,** Design techniques to improve the resilience of computing systems: logic layer, Cross-Layer Reliability of Computing Systems, Giorgio DI NATALE, Dimitris GIZOPOULOS, Stefano DI CARLO, Alberto BOSIO, Ramon CANAL (Eds.) , Ed. IET - The Institution of Engineering and Technology, pp. 23-42, 2020

2 **Bosio A., Di Carlo S., Di Natale G., Sonza Reorda M., Rodriguez Condia J.E.,** Design techniques to improve the resilience of computing systems: software layer, Cross-Layer Reliability of Computing Systems, Giorgio DI NATALE, Dimitris GIZOPOULOS, Stefano DI CARLO, Alberto BOSIO, Ramon CANAL (Eds.) , Ed. IET - The Institution of Engineering and Technology, pp. 95-112, 2020

Books & edited publications

1 **Di Natale G., Gizopoulos D., Di Carlo S., Bosio A., Canal R. (Eds.)** Cross-Layer Reliability of Computing Systems, pp. 1-328, Ed. IET - The Institution of Engineering and Technology, 2020

Other communications

1 **Alipour A., Hély D., Beroulle V., Di Natale G.,** Power of Prediction: Advantages of Deep Learning Modeling as Replacement for Traditional PUF CRP Enrollment, TrueDevice Workshop 2020, Grenoble, FRANCE, 2020

Theses

1 **Shah R.,** Reliability Improvement by Dynamic Wearout Management using In-Situ Monitors, These de Doctorat, 5 octobre 2020

CNRS - Grenoble INP - UGA

CDSI team

Circuits, Devices and System Integration

Circuits, Devices and System Integration (CDSI team)

Keywords: Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

The CDSI team

The team activity covers a broad spectrum of activities from MEMS to systems. Indeed, the team postulates high performances are achieved thanks to disruptive technologies, which are at the frontiers of different fields of applications. Nevertheless, the team is built on two key pillars, sensing and event processing.

Event-based techniques are key for enhancing integrated circuits and systems because they offer a unique opportunity to rethink circuit design, which does not take well into account most of the non-functional specifications, such as power, security, safety or electromagnetic emissions. This paves the way to ultra-low power systems, enhanced secured systems, proven design methods but also near sensor computing.

Sensing is the second key. Taking advantage of smart sensors and actuators requires globally envisioning systems, favors a smart sensing approach limiting useless information and pushes new experiments and usage.

Event-based technologies

Event-based approach

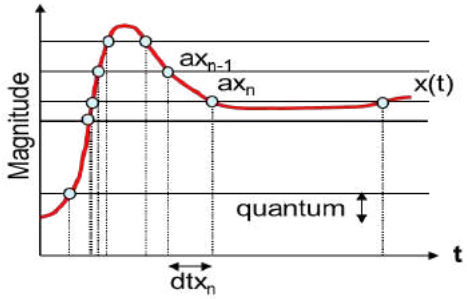


Figure 1: Level Crossing Sampling Scheme

Event-based is a quite simple idea, which suggests operating a circuit only when needed. Nevertheless, this is countercurrent when looking the semiconductor industry. Indeed, everything is clocked synchronized, analog-to-digital conversion is clock-sampled. In practice, clock is used as an event generator giving the pace of the circuits generating a large number of events and producing useless activity, computation, storage or communication. The event-based approach tends generating sparse events related to natural events such as a pressure variation or a heartbeat. Therefore, the team works on alternative analog-to-digital converters able to drastically reduce the number of samples and, hence, limit useless activity and energy consumption.

Asynchronous Circuits

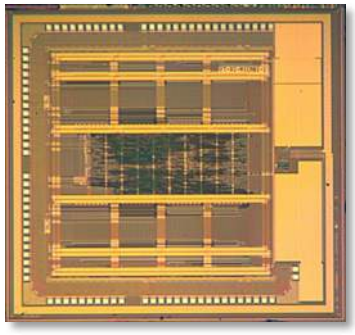


Figure 2: Asynchronous microcontroller with on-chip NFC antenna

Since more than 20 years, the team works on new synchronization paradigms, which are not based on a clock but on handshake signals. Such techniques reveal many opportunities for rethinking the circuit design process and opening new degrees of freedom. The first expected advantage is probably the reusability of existing blocks that can simply be connected together, making the assembly of a system a kind of LEGO build. Indeed, the timing assumptions are locally fulfilled guarantying an easy block association. Moreover, many other advantages are of interest such a lower power consumption, a better robustness, lower electromagnetic emissions, safer and more secured circuits…

Targeting Ultra-low power

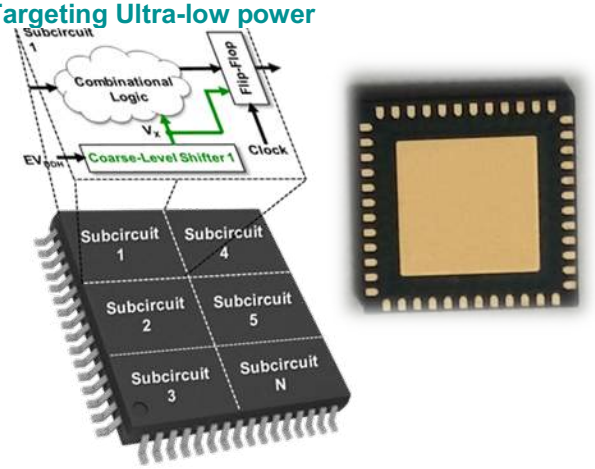


Figure 3: FDSOI 28 nm asynchronous testchip managing several local fine-grain body-bias domains

Today power is a main concern for chip design. The event-based strategy is probably the best technique for reducing power at least by one order of magnitude. Indeed, a sparse sampling scheme produces much less data, which are non-uniformly spaced in time. Each datum is no more than an event that can be sporadically processed by asynchronous circuits. Indeed, these latter are data-driven and consume energy only when computing. Moreover, the intrinsic robustness of asynchronous circuits favors their use at low-voltage, near- or subthreshold. Indeed, lowering the voltage is an efficient and well-known strategy to save power. Its main drawback is the decrease of the circuit speed. The Fully Depleted Silicon on Insulator (FDSOI) technology allows mitigating this speed drop thanks to forward body biasing.

As asynchronous circuits use communication protocols indicating circuit activity, the handshake signals are perfectly suited for controlling local body-bias domains ensuring low-energy expenses for body biasing and compensating the speed loss. All these mechanisms can be implemented for mitigating the energy and helping the adoption of energy harvesting in batteryless systems.

Security

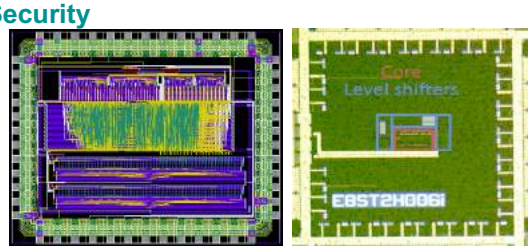


Figure 4: TRNG with entropy monitoring (left) and Ultra-low power TRNG (right) (30 pJ/bit@0.3 V)

Another opportunity offered by the asynchronous circuits is its ability to make more difficult the side-channel analysis and attacks in trusted devices. Indeed, the absence of clock synchronization, the specific encoding and the computation time control makes them of interest for developing trusted platforms. They also offer disruptive strategies for true random number generators (TRNG) and physically unclonable functions (PUF) while consuming a few energy.

Design flow and proven technology

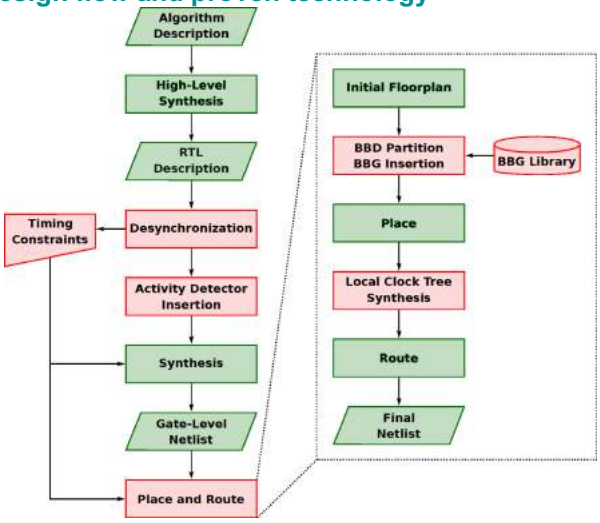


Figure 5: Asynchronous circuit HLS to layout design flow

Developing non-conventionally synchronized circuits is not obvious because of the lack of dedicated CAD tools. Although the first good idea is to implement such tools, there is some overcoming hurdles. The first one is clearly the quasi-absence of trained people with the know-how for designing efficient and performant asynchronous circuits. The second is the impact, the reliability and the engineer confidence into a new design flow. Therefore, for more than 10 years, the team is developing dedicated flows based on the standard commercial tools with a particular emphasis on a proven by construction synthesis.

Near-sensor computing

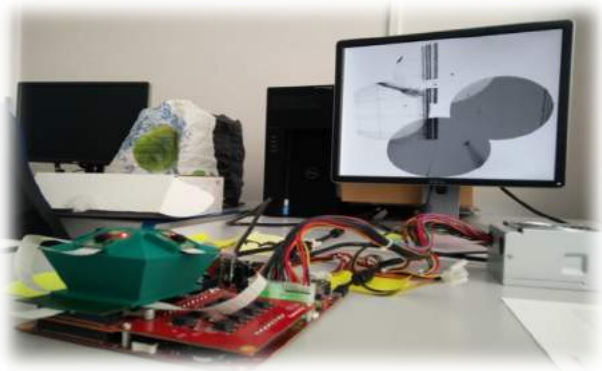


Figure 6: Panoptic camera for laparoscopy

With the dissemination of autonomous and connected objects, it appeared the need to limit the amount of transmitted raw data, especially in RF communications where the problem is more acute. Therefore, developing tiny sensor platforms able to preprocessed data before transmitting information is becoming a challenging topic. Indeed, enhancing the sensing techniques and immediately processing the raw data with a reduced energy budget is the grail in near-sensor computing. The team developed several strategies based on event-based techniques or improving the adequacy between the algorithms and the circuit architecture. This is typically the case for many image-processing applications such as panoptic camera for laparoscopy.

Smart-sensing technologies

In-sensor computing

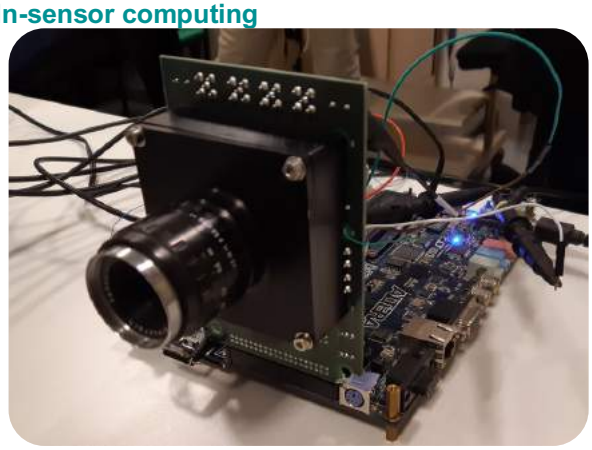


Figure 7: Event-based camera

As previously stated, smart sensing is a key for envisioning systems with advanced features such as detection, pattern recognition or low-power. Beyond the state of art of sensor technology, the enhancement can be obtained thanks to new architectures or in-sensor computing. One of the approach concerns image sensors, which usually permanently read the image. This is a waste of energy and time for acquiring an image. In order to reduce these issues, the image capture can be performed thanks to an event-based readout, which only samples a pixel when this latter fires. In this case, the firing pixel indicates that its value has to be changed in the image memory. Such a strategy is applied for reducing the power consumption and increasing the speed sensor thanks to a dedicated readout canceling the spatial and temporal redundancies.

Measuring time

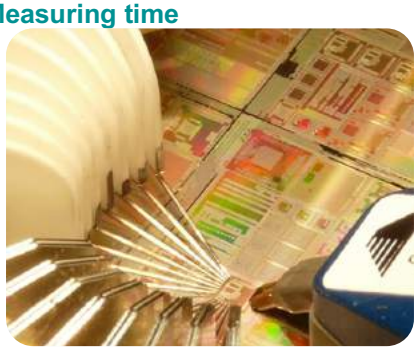


Figure 8: Asynchronous multiphase oscillator (under test) used in TDC

Using an event-based sensing implies a duality with the standard Nyquist analog-to-digital conversion because the quantization is no more applied to the amplitude but to the time elapsed between two successive events. Therefore, designing advanced Time-to-Digital Converters (TDC) is an important block for many sensors or even for some security primitives such as TRNG or PUF.

Harvesting for ultra-low power systems

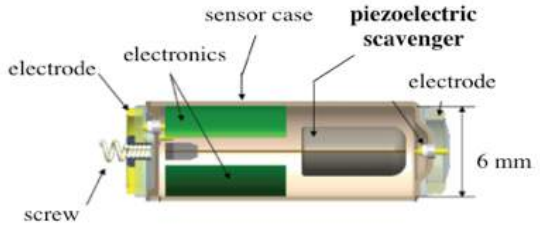


Figure 9: Piezoelectric scavenger for automous pacemaker (Vibration: 10 - 25 Hz, Size: L = 30 mm, Ø= 6 mm, energy: 5 - 10 µJ)

With the advent of the Internet of Things, the system requirements in term of power are extremely demanding, especially for smart sensing and actuating. A typical highlight targets the medical implant such as pacemakers. Indeed, they need today a battery, which lasts less than 10 years. Then the pacemaker has to be explanted because this is not a rechargeable battery. In order to overcome this issue, a strategy is to harvest the heart mechanic power thanks to a piezoelectric harvester. The MEMS are particularly well-suited for extracting energy from different sources (thermal, mechanical, electrical…) for small autonomous and smart objects.

Security (chaotic approach)

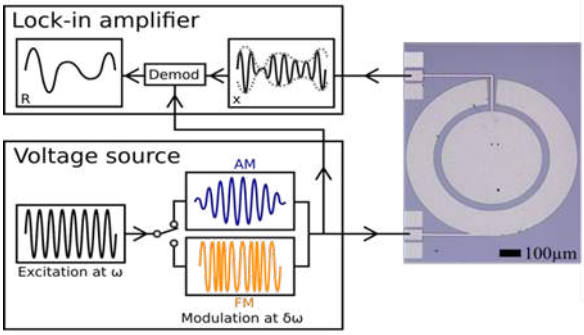


Figure 10: Experimental Setup and modulations in the Duffing's regime. The MEMS (photography) is driven by a voltage modulated voltage source (AM or FM). The Lock-in-Amplifier extracts the displacement magnitude of the MEMS to observe the chaos.

MEMS have opened the doors to intense researches covering most of the technology fields. It is not surprising that they can be of interest for security. They offer original solutions for designing chaotic generators using the dynamical bistability of a Duffing's microresonator. This approach is particularly relevant for generating true random numbers because MEMS already exist on various systems such as mobile phones and are useable for extracting chaos. Moreover, this could be employed for securing communications thanks to a couple of twin chaotic MEMS, using various transduction schemes such as electrical, acoustic or optical signals.

New Sensors and actuators

Figure 11: Haptic screen, the modulation of stationary waves gives different feeling when touching the surface

The team is also developing original micro-acoustic systems (Piezo Micromachined Ultrasonic Transducers) used as microphones, non-contact gesture recognitions, proximity sensors, fingerprint sensors or aeroacoustic measurements.

Piezo-MEMS devices have been developed in order to give a haptic rendering by friction modulation. They are key components for the future haptic touch screen, which will be used in many applications (automotive, smartphones, …).

Highlights of 2020 and of the recent years

- Asynchronous circuit High Level Synthesis for fine-grain body-biasing in FDSOI (tetschips in 65 nm and 28 nm from STMicroelectronics)
- New event-based image sensor cancelling spatial and temporal redundancies in FDSOI 28 nm from STMicroelectronics
- Physically Unclonable Function based on self-timed ring and TDC (testchip in 65 nm from STMicroelectronics)
- First DFT technique for asynchronous bundled-data circuits based on commercial tools
- Static Timing Analysis of asynchronous bundled-Data Circuits
- Local clock set methodology for implementing asynchronous circuits with commercial tools
- Event-based demodulation for NFC applications
- EM shaping with bundled-data circuits
- First demonstration of MEMS-based TRNG achieving NIST requirements
- Generation and reception of chaotic ultrasonic waves

Academic and research members

Skandar BASROUR

Position
Professor at UGA – POLYTECH school

Responsibilities
Deputy Director of TIMA Lab. since 01/2015
Co-leader of CDSI team
Researcher in CDSI team

Agnès BONVILAIN

Position
Associate Professor at UGA – POLYTECH school

Responsibilities
Researcher in CDSI team

Martial DEFOORT

Position
Researcher at CNRS

Responsibilities
Researcher in CDSI team

Sylvain ENGELS

Position
Associate Professor PAST at Grenoble INP - PHELMA school

Responsibilities
Researcher in CDSI team

Laurent FESQUET

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Co-leader of CDSI team
Researcher in CDSI team

Stéphane MANCINI

Position
Associate Professor at Grenoble INP - ENSIMAG school

Responsibilities
Researcher in CDSI team

Katell MORIN-ALLORY

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in CDSI team

Rodrigo POSSAMAI BASTOS

Position
Associate Professor at UGA - IM2AG school

Responsibilities
Researcher in CDSI team until 30/06/2020

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
GRENOBLE INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AKRARAI Mohamed
Title of thesis: **Smart Event-Based Image Sensor for wake-up applications**
Expected date of defense: **2022**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

2. AQUINO GUAZZELLI Ricardo
Title of thesis: **Exploring a Non-conventional Testing Technique for Asynchronous Circuits**
Completed on: **December 3rd, 2020**
Previous degrees: Engineer – Pontifícia Universidade Católica do Rio Grande do Sul – Porto Alegre, Brazil (2017)

3. BELOT Jérémy
Title of thesis: **Towards robust, low power and adjustable accuracy Bayesian computers**
Expected date of defense: **2022**
Previous degrees: Engineer Grenoble INP – Phelma, France (2018)

4. CROZET Florent
Title of thesis: **Extreme Learning Machine for embedded neural networks**
Expected date of defense: **2024**
Previous degrees: Engineer (2019)

5. DECOUDU Yoan
Title of thesis: **An asynchronous Design Flow for Event-Based Processing in FDSOI Technologies**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

6. DE GIOVANNI Adrien
Title of thesis: **Design of a piezoelectric micro-actuator with mechanical amplification for extra-auricular earphones**
Expected date of defense: **2023**
Previous degrees: Engineer (2020)

7. FERNANDEZ BRILLET Lucas
Title of thesis: **Convolutional Neural Networks for embedded vision**
Completed on: **September 28th, 2020**
Previous degrees: Engineer – ENSEIRB / MATMECA - Bordeaux INP, France (2016)

8. GARAY TRINDADE Matheus
Title of thesis: **Optimization and Qualification of Hardware Machine-Learning Systems under Radiation-Induced Effects**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidade Federal de Santa Maria, Rio Grande do Sul, Brazil (2017)

9. GASSAB Marwa
Title of thesis: **New electroactive nanostructured materials for flexible sensors**
Expected date of defense: **2021**
Previous degrees: Engineer – Higher Institute of Applied Sciences and Technology of Sousse (2018)

10. GIMENEZ Grégoire
Title of thesis: **Design of secure and very low power circuits : an asynchronous alternative**
Completed on: **February, 12th, 2020**
Previous degrees: Engineer – Grenoble INP, France (2009)

11. HACHEMI Mohammed-Bilal
Title of thesis: **Study of HZO films for MEMS applications**
Expected date of defense: **2022**
Previous degrees: Engineer - ECole Polytechnique de Constantine – Algeria (2017)

12. IGA Rodrigo
Title of thesis: **EM compliant Low-Energy Sugnal Demodulation for NFC applications**
Expected date of defense: **2021**
Previous degrees: Engineer – Université Grenoble Alpes, France (2010)

13. LAUWERS Thomas

Title of thesis: **Resonant optical transduction for photoacoustic detection**
Completed on: **March 22nd, 2020**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2016)

14. LECLAIRE Nicolas

Title of thesis: **Hardware and software architectures for deep learning acceleration on embedded multi-processor**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2017)

15. LIM Olivier

Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defense: **2023**
Previous degrees: Master (2020)

16. ROUX Julie

Title of thesis: **Safety Evaluation of Aircraft Systems using Virtual Platforms**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2017)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. ABDALI	El Mehdi	MOROCCO	9 months 12 days
2. MARGOTAT	Nils	FRANCE	12 months
3. RICART	Thibault	FRANCE	3 months

Visitors

Name	Forename	Country	Duration
1. FRAGA GARIBOTTI	Rafael	BRAZIL	5 months
2. RUFER	Libor	CZECH REP.	12 months

Trainees

Name	Forename	Country	Duration
1. HAI	Joycelyn	MALAYSIA	1 month
2. HOLANDA BATISTA	Madson Ivens	BRAZIL	1 month
3. MAAMER	Bilel	TUNISIA	12 months
4. MALDANER	Liege	BRAZIL	1 month
5. MATIASSO PORTELLA	Kenedy	BRAZIL	12 days

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANRT

CIFRE Jérémy BELOT
Responsable scientifique : FESQUET Laurent
Durée : 2020 - 2023

CIFRE Alexis Rodrigo IGA RADUE
Titre : "Démodulation NFC Basse Consommation et Respectueuse de la Compatibilité Electromagnétique"
Responsable scientifique : FESQUET Laurent
Durée : 2018 - 2021

CIFRE Nicolas LECLAIRE
Titre : "Architectures matérielles et logicielles pour l'accélération du "deep learning" sur multiprocesseur évolutif embarqué"
Responsable scientifique : MANCINI Stéphane
Durée : 2018 - 2021

CARNOT

EBIS
Titre : Event Based Image Sensor
Responsable scientifique : FESQUET Laurent
Durée : 2019 - 2020

CEC-NATIONAL

OCEAN 12
Programme : ECSEL
Titre : Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node
Responsable scientifique : FESQUET Laurent
Durée : 2018 - 2021

EPST

Chameleon
Programme : IRS (Initiative de Recherche Stratégique)
Responsable scientifique : BASROUR Skandar
Durée : 2020 - 2021

Cyber@Alpes
Programme : Grenoble Alpes CyberSecurity Institute
Responsable scientifique : MAISTRI Paolo
Co-partage d'équipes (AMfoRS, CDSI)
Durée : 2018 – 2021

INDUSTRIE

ICALPS - G.GIMENEZ
Titre : Conception de circuits d'identification sécurisé basse consommation
Responsable scientifique : FESQUET Laurent
Durée : 2018 - 2021

Thèse Grégoire GIMENEZ
Titre : "Etude et conception de puces sécurisées basse consommation pour plateforme IoT"
Responsable scientifique : FESQUET Laurent
Durée : 2016 - 2020

INTERNATIONAL

BRAFISAT
Programme : BRAFITEC
Responsable scientifique : POSSAMAI BASTOS Rodrigo
Durée : 2019 - 2022

MINISTERES-FUI

IMSPOC-UV
Programme : PIA Programme d'Investissemeent d'Avenir
Titre : Imaging Spectrometer On Chip
Responsable scientifique : BASROUR Skandar
Durée : 2018 – 2022

REGION

MucoPiezoRheo
Programme : PSPC
Responsable scientifique : BASROUR Skandar
Durée : 2020 - 2023

GRESAM
Programme : Pack Ambition International
Titre : Grenoble Sousse Autonomous Microsystems
Responsable scientifique : BASROUR Skandar
Durée : 2019 - 2021

FAIR
Programme : Pack Ambition Recherche
Titre : Conception et fabrication par Fabrication Additive de produits Intelligents
Responsable scientifique : BASROUR Skandar
Durée : 2018 - 2023

Convertisseur temps numérique
Programme : SCUSI
Titre : Dispositif microélectronique ultra-précis de mesure de temps basé sur l'oscillateur en anneau auto-séquencé
Responsable scientifique : FESQUET Laurent
Durée : 2017 - 2020

Organization and participation of international conferences, workshops, forums

13th International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS'2020)
November 21-25, 2020, Valencia, SPAIN
Rang : NC
technical program committee: FESQUET L.

6th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP'2020)
June 3-5, 2020, Grenoble, FRANCE
Rang : NC
general chair: FESQUET L.

10èmes Journées Nationales sur la Récupération et le Stockage de l'Energie (reportées à 2021) (JNRSE'2020)
May 27-28, 2020, Grenoble, FRANCE
Rang : NC
technical program committee: BASROUR S.

5th International Conference on Advances in Signal, Image and Video Processing (SIGNAL'2020)
May 24-29, 2020, Venice, ITALY
Rang : NC
industry liaison: FESQUET L.
technical program committee: FESQUET L.

International Symposium on Asynchronous Circuits and Systems (ASYNC '2020)
May 17-20, 2020, Snowbird (Utah), USA
Rang : A+
technical program committee: FESQUET L.

21st IEEE Latin-American Test Symposium (LATS'2020)
March 30-April 2, 2020, Jatiúca (Maceió), BRAZIL
Rang : NC
technical program committee: POSSAMAI BASTOS R.

21st International Symposium on Quality Electronic Design (ISQED'2020)
March 25-26, 2020, Santa Clara, USA
Rang : A
track chair: RUFER L.

Design, Automation & Test in Europe (DATE'2020)
March 9-13, 2020, Grenoble, FRANCE
Rang : A+
technical program committee: MORIN-ALLORY K.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
PHELMA school PHysique, ÉLectronique, Matériaux				
Manager of SEI branch	MORIN-ALLORY K.	01/09/2017		
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Manager of Office Automation and Informatics	POSSAMAI BASTOS R.	01/09/2017		Formation à tous les parcours du Département Licence Sciences et Technologies de l'UGA
Research structures				
CIME Nanotech Centre Interuniversitaire de MicroElectronique et Nanotechnologies				
Deputy Director	FESQUET L.	01/09/2017		
Manager of Communicating objects platform	MANCINI S.	01/09/2017		
Manager of Microsystems platform	BASROUR S.	01/10/2006		
PEM pole Physique, ingénierie, matériaux				
TIMA representative of PEM cluster	BASROUR S.	01/09/2016		
Parents institutions				
Grenoble INP				
Board of Directors member (elected member)	MANCINI M.	12/12/2019	01/01/2024	Strategy, jobs, promotion files, invited professors, teaching assistants

Scientific production

International journals

Possamai Bastos R., **Dutertre J.M.**, **Garay Trindade M.**, **Andreoni Camponogara Viera R.**, **Potin O.**, **Letiche M.**, **Cheymol B.**, **Beaucour J.**, Assessment of On-Chip Current Sensor for Detection of Thermal-Neutron Induced Transients, IEEE Transactions on Nuclear Science, Ed. IEEE, Vol. 67, No. 7, pp. 1404-1411, DOI: 10.1109/tns.2020.2975923, 2020

Hadj Salem K., **Jost V.**, **Kieffer Y.**, **Libralesso L.**, **Mancini S.**, Minimizing makespan under data prefetching constraints for embedded vision systems: a study of optimization methods and their performance, ORIJ - Operational Research - An International Journal, Ed. Springer , Vol. , 2020

Skaf A., **Ezzadeen M.**, **Benabdenbi M.**, **Fesquet L.**, Clocked and event-driven redundant adjustable precision computing, Microelectronics Reliability, Ed. Elsevier, Vol. 111, pp. 113729, DOI: 10.1016/j.microrel.2020.113729, août 2020

Sansa M., **Defoort M.**, **Brenac A.**, **Hermouet M.**, **Banniard L.**, **Fafin A.**, **Gely M.**, **Masselon C.D.**, **Favero I.**, **Jourdan G.**, **Hentz S.**, Optomechanical mass spectrometry, Nature Communications, Ed. Nature Publishing Group, Vol. 11, No. 1, pp. 3781, DOI: 10.1038/s41467-020-17592-9, juillet 2020

Popescu A., **Besancon G.**, **Voda A.**, **Basrour S.**, Observer-Based 3-D Control Enhancement for Topographic Imaging--Validation With an STM Prototype, IEEE Transactions on Control Systems Technology, Ed. IEEE, Vol. , pp. 1-12, DOI: 10.1109/TCST.2020.2991871, mai 2020

Aquino Guazzelli R., **Garay Trindade M.**, **Acunha Guimaraes L.**, **Ferreira De Paiva Leite T.**, **Fesquet L.**, **Possamai Bastos R.**, Trojan Detection Test for Clockless Circuits, Journal of Electronic Testing: Theory and Applications, Ed. Springer , Vol. , février 2020

Patents

Engels S., **Fesquet L.**, **Germain S.**, System and Method for Managing Requests in an Asynchronous Pipeline, No. US2020184110 (A1), 11 juin 2020

Fesquet L., **Cherkaoui A.**, **Frisch R.**, Circuit and Method for Protecting Asynchronous Circuits, No. WO/2020/008229, 9 janvier 2020

Invited conferences talks

Fesquet L., **Decoudu Y.**, **Iga R.**, **Ferreira De Paiva Leite T.**, **Rolloff O.**, **Diallo M.**, **Possamai Bastos R.**, **Morin-Allory K.**, **Engels S.**, Body-Bias Micro-Generators for Activity-Driven Power Management, Invited Talk, FDSOI workshop at DATE Conference 2020, Grenoble, FRANCE, 9 mars 2020

International conferences

Roux J., **Beroulle V.**, **Morin-Allory K.**, **Leveugle R.**, **Bossuet L.**, **Cezilly F.**, **Berthoz F.**, **Genevrier G.**, **Cerisier F.**, High Level Fault Injection Method for Evaluating Critical System Parameter Ranges, 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2020), pp. 1-4, Glasgow, UNITED KINGDOM, DOI: 10.1109/ICECS49266.2020.9294821, 23 au 25 novembre 2020

Leclaire N., **Mancini S.**, **Delnondedieu C.**, **Henriques J.P.**, Efficient Implementation of Convolution and Winograd on ASMP Embedded Multicore Vector Processor, IEEE International Workshop on Signal Processing Systems (SIPS 2020), Coimbra (Virtual event), PORTUGAL, 20 au 22 octobre 2020

Mian Qaisar S., **Fesquet L.**, An Effective QRS Selection Based on the Level-Crossing Sampling and Activity Selection, 6th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2020), Krakow, POLAND, DOI: 10.1109/EBCCSP51266.2020.9291365, 23 au 25 septembre 2020

Akrarai M., **Margotat N.**, **Sicard G.**, **Fesquet L.**, Arbiterless Event-Based Imager Architecture with temporal and spatial redundancies suppression, 6th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2020), Krakow, POLAND, DOI: 10.1109/EBCCSP51266.2020.9291345, 23 au 25 septembre 2020

Decoudu Y., **Simatic J.**, **Morin-Allory K.**, **Fesquet L.**, From High-Level Synthesis to Bundled-Data Circuits, International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2020), Samos, GREECE, 6 au 9 juillet 2020

Akrarai M., **Margotat N.**, **Sicard G.**, **Fesquet L.**, A Novel Event Based Image Sensor with Spatial and Temporal Redundancy Suppression, 18th IEEE International NEWCAS Conference (NEWCAS 2020), Montreal, CANADA, DOI: 10.1109/NEWCAS49341.2020.9159847, 16 au 19 juin 2020

Alshakoush A., **Lauga-Larroze E.**, **Podevin F.**, **Ibrahim S.**, **Fesquet L.**, **Bourdel S.**, Improved Pi-Delayed Harmonic Rejection N-Path Mixer for Low Power Consumption and Multistandard Receiver, 18th IEEE International NEWCAS Conference (NEWCAS 2020), Montreal, CANADA, DOI: 10.1109/NEWCAS49341.2020.9159792, 16 au 19 juin 2020

Gimenez G., **Cherkaoui A.**, **Fesquet L.**, A Self-Timed Ring based PUF, 26th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2020), pp. 69-77, Snowbird, UNITED STATES, DOI: 10.1109/ASYNC49171.2020.00019, 18 au 20 mai 2020

Roux J., **Beroulle V.**, **Morin-Allory K.**, **Leveugle R.**, **Bossuet L.**, **Cezilly F.**, **Berthoz F.**, **Genevrier G.**, **Cerisier F.**, Cross Layer Fault Simulations for Analyzing the Robustness of RTL Designs in Airborne Systems, 23rd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS 2020), pp. 1-4, Novi Sad, SERBIE, DOI: 10.1109/DDECS50862.2020.9095559, 22 au 24 avril 2020

Lauwers T., **Glière A.**, **Basrour S.**, Resonant optical transduction for photoacoustic detection, SPIE Photonics West 2020 - Optoelectronics, photonic materials and devices, San Francisco, UNITED STATES, 1 au 6 février 2020

Others communications

Garraud A., **Basrour S.**, **Peyrade D.**, Fabrication of a Multiple Heater-Sensor Platform for Cell Temperature Monitoring, Symposium on Design, Test, Integration & Packaging of MEMS and MOEMS (DTIP 2020), Virtual event, FRANCE, 2020

Theses

Fernandez-Brillet L., Convolutional Neural Networks for embedded vision, These de Doctorat, 28 septembre 2020

CNRS - Grenoble INP - UGA

RMS team

Reliable RF and Mixed-signal Systems

Reliable RF and Mixed-signal Systems (RMS team)

Description

The Reliable RF and Mixed-signal Systems group (**R**MS) is focused on the design, test and control of analog/mixed-signal/RF/mm-Wave integrated circuits and systems. The work of the team is included in the Laboratory themes of "Robustness, reliability and test", "Design of AMS/RF devices, circuits and systems" and "Machine learning-based modeling of AMS/RF circuits and systems".

Robustness, reliability and test

The test, control and calibration of AMS-RF-mmW functions in a complex integrated system represent nowadays a major challenge for the IC industry. Our research in this area is focused on two main research lines: a) the development of AMS-RF-mmW state-of-the-art on-chip test instruments for Built-In Self-Test (BIST) applications and dedicated DfT techniques; and b) the development of embedded solutions for performance control, optimization and self-calibration.

Design of AMS/RF devices, circuits and systems

Novel AMS/RF/mmW design solutions are required in a wide variety of state-of-the-art applications, including communications, computing, imaging, etc. In this regard, the **R**MS group explores the multiple challenges of state-of-the-art AMS/RF/mmW current and emerging design paradigms. Our research includes the development of low-power mixed-signal and RF design techniques, state-of-the-art data converters for imaging applications, integrated control electronics for quantum computing, and advanced RF and mmW design techniques for beyond- 5G and 6G applications.

Machine learning-based modeling of AMS/RF circuits and systems

The basis for using machine learning for AMS/RF circuits is to find rich statistical performance models which allow predicting the circuit performance from simple observational data. In this research line, the **R**MS group explores the use of machine learning techniques for reducing test complexity and cost, simplifying the control of complex systems and enabling efficient statistical calibration methods.

Research milestones

- Non-intrusive mm-wave test: we have outlined and experimentally demonstrated a machine learning-based non-intrusive test methodology for mm-Wave circuits
- Advanced modeling of mm-wave couplers for design enhancement: design-oriented model considering frequency-dependent electrical losses
- First-ever OBT technique for mm-wave circuits: we have demonstrated the potential of Oscillation-Based Test techniques for the test and calibration of phased arrays
- Development of Embedded Test Instruments for the static and dynamic test of state-of- the-art ADCs
- Development of machine learning-based image quality evaluation and correction techniques
- Low cost controller synthesis: we have developed a software platform for automatic generation of logic control codes for a wide variety of low-cost microcontroller targets
- Scheduling control for lifetime optimization in Wireless Sensor Nodes technologies: we have proposed a novel solution to the Maximum Lifetime Coverage Problem (MLCP) that takes into account the non-zero energy of nodes in sleep mode

Highlights

- Best Reading Paper in the December 2020 issue of IEEE Trans. on Microwave Theory and Techniques.
- Best Paper Award from the IEEE European Test Symposium 2018
- Best Poster Award from the Journées Nationales de Réseau Doctoral en Micro-nanoélectronique 2017
- Best Paper Award at the 20th IEEE European Test Symposium (ETS 2015)
- Selected Best in Test: Top Papers from the 2015 International Test Conference, by IEEE Design & Test
- Best Special Session Award in IEEE VLSI Test Symposium 2015 (VTS'15)
- Selected Best Paper Candidate in VTS 2018, DATE 2017, ETS 2016, ITC 2015
- Creation of a Joint Research Laboratory with the startup company XDIGIT

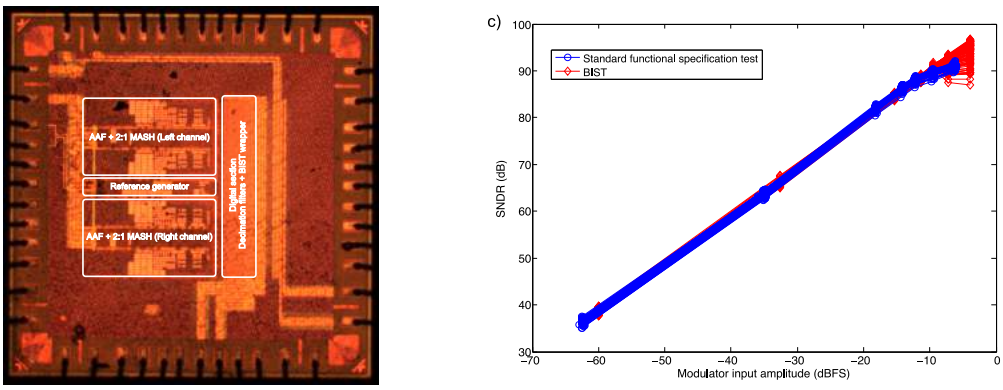


Figure 1: Sigma-Delta ADC with dynamic BIST

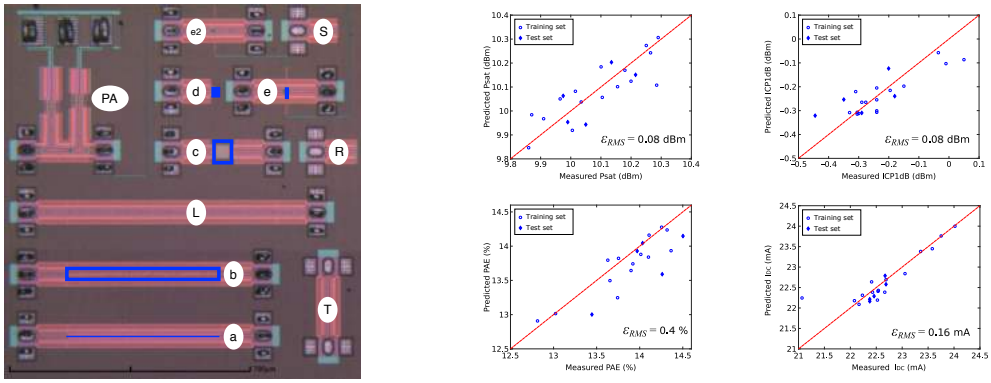


Figure 2: 60 GHz PA with non-intrusive machine learning-based test

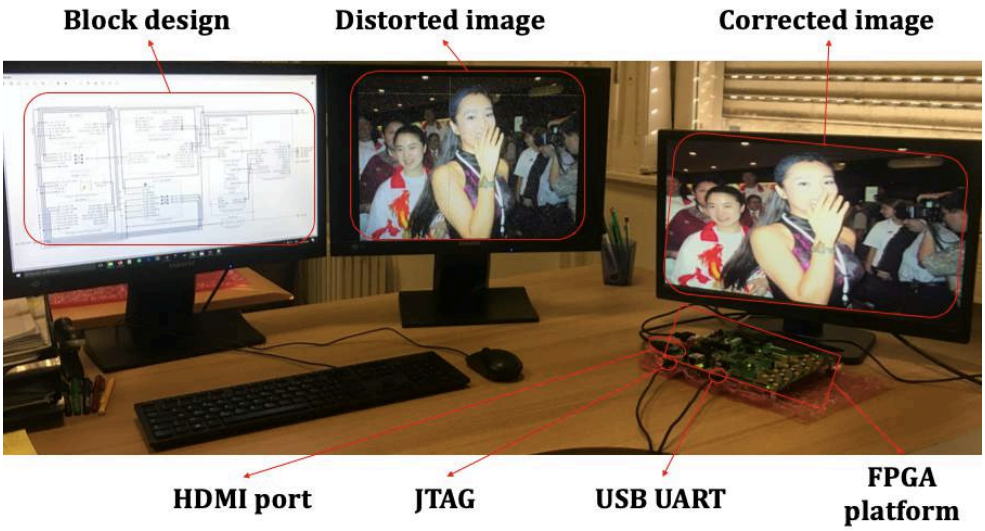


Figure 3: Image quality evaluation and correction

Academic and research members

Manuel BARRAGAN

Position
Researcher at CNRS

Responsibilities
Reseacher in RMS team

Daniel DZAHINI

Position
Research engineer at CNRS

Responsibilities
Researcher in RMS team

MIR Salvador

Position
Research Director at CNRS

Responsibilities
Director of TIMA Laboratory from 01/01/2015 to 31/12/2020
Reseacher in RMS team

Emmanuel SIMEU

Position
Associate Professor at UGA – POLYTECH school

Responsibilities
Leader of RMS team
Reseacher in RMS team

CNRS (French National Center for Scientific Research)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. BONTEMS William Illich

Title of thesis: **Design of a 15-bit analog to digital converter for ultra low power applications**
Expected date of defense: **2023**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

2. BRITTON OROZCO Giovani Crasby

Title of thesis: **Design of an FD-SOI read / control circuit dedicated to the field of quantum computing under Cryogenic conditions**
Expected date of defense: **2023**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2020)

3. KRIEKOUKI Ioanna

Title of thesis: **Fabrication and characterization of spin-based quantum bits with embedded control in 28 nm UTBB FD-SOI technology and at very low temperatures**
Expected date of defense: **2022**
Previous degrees: Engineer – Université Grenoble Alpes, France (2017)

4. MADHVARAJ Manasa

Title of thesis: **IPS for mixed-signal/high speed integrated circuits dependability and control**
Expected date of defense: **2023**
Previous degrees: Master of technology “VLSI design and embedded systems” – Bangalore, India (2015)

5. MAMGAIN Ankush

Title of thesis: **Design of embedded test instrument for mixed signal application**
Expected date of defense: **2023**
Previous degrees: Master of technology “Electronic and communication engineering” – New Delhi, India (2014)

6. MARGALEF ROVIRA Marc

Title of thesis: **Design of mm-wave Reflection-Type Phase Shifters with Oscillation-BasedTest capabilities**
Completed on: **September 11th, 2020**
Previous degrees: Engineer – Université Grenoble Alpes, France (2017)

7. MELIS Tommaso

Title of thesis: **Diagnosis tool developement for failure analysis of analog an mixed signal devices**
Expected date of defense: **2022**
Previous degrees: Engineer - Università degli Studi di Cagliari, Italy (2018)

8. SILVEIRA FEITOZA Renato

Title of thesis: **Desigh-for-test strategies for built-in static test of high-performance SAR ADCs**
Expected date of defense: **2021**
Previous degrees: Engineer – Pontifícia Universidade Católica do Rio de Janeiro, Brazil (2017)

9. TROUSSIER Chloé

Title of thesis: **Study of ESD/CDM stresses phenomena from elementary charged devices to package discharge: failure mechanism, protection strategy and predictive tools**
Expected date of defense: **2021**
Previous degrees: Engineer – IMT Atlantique Bretagne Pays de Loire, France (2018)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. BEN AZIZA	Sassi	TUNISIA	1 month, 10 days
2. TAKAM TCHENDJOU	Ghislain	CAMEROON	12 months

Visitors

No visitors in 2020.

Trainees

Name	Forename	Country	Duration
1. BERLINGARD	Quentin	FRANCE	7 months, 9 days
2. MONGUILO MANTOVANI	Javier Alejandro	ITALY	1 month

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANRT

CIFRE Giovanni BRITTON
Responsable scientifique : MIR Salvador
Co-partage d'équipes (RFIC Lab, RMS)
Durée : 2020 - 2023

CIFRE Chloé TROUSSIER
Titre : "Etude des phénomènes de décharge électrostatique (ESD/CDM) : du composant au circuit intégré"
Responsable scientifique : SIMEU Emmanuel
Durée : 2018 - 2021

CIFRE Tommaso MELIS
Titre : "Développement d'outils de diagnostic pour l'analyse des défaillances des circuits intégrés analogiques et mixtes"
Responsable scientifique : SIMEU Emmanuel
Durée : 2018 - 2021

CIFRE Ioanna KRIEKOUKI
Titre : "Fabrication et caractérisation de bits quantiques avec contrôle embarqué en technologie 28nm UTBB FD-SOI et au delà à température cryogénique"
Responsable scientifique : MIR Salvador
Durée : 2018 - 2021

COLLECTIVITES TERRITORIALES

MESSI
Programme : nano 2022
Titre : Mixed-Signal Self-Test IPs for on-chip testing and technology qualification
Responsable scientifique : MIR Salvador
Durée : 2019 - 2022

EPST

Conception Analogique
Responsable scientifique : BARRAGAN ASIAN Manuel
Durée : 2019 - 2020

EUREKA

HADES
Programme : PENTA
Titre : Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems
Responsable scientifique : MIR Salvador
Co-partage d'équipes (AMfoRS, RMS)
Durée : 2017 - 2020

INDUSTRIE

XDIGIT -Easytech 2020
Programme : PYXCAD/EASYTECH
Titre : "Développement microélectronique pour la technologie MASSAR"
Responsable scientifique : MIR Salvador
Durée : 2020 - 2021

Organization and participation of international conferences, workshops, forums

4th International Conference on Control, Automation and Diagnosis (ICCAD (Control Automation and Diagnosis)'2020)
October 7-9, 2020, Paris, FRANCE
Rang : NC
technical program committee: SIMEU E.
industry liaison: SIMEU E.

28th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC'2020)
October 5-7, 2020, Salt Lake City, USA
Rang : A
steering committee member: MIR S.
topic chair : MIR S.

26th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2020)
July 13-15, 2020, Virtual event from Naples (Italy), ITALY
Rang : B
technical program committee: BARRAGAN M., MIR S

18th IEEE International NEWCAS Conference (NEWCAS'2020)
June 16-19, 2020, Montréal, CANADA
Rang : B
program chair: BARRAGAN M.

25th IEEE European Test Symposium (ETS'2020)
May 25-29, 2020, Tallinn, ESTONIA
Rang : A
technical program committee: BARRAGAN M., MIR S

IEEE International Symposium on Circuits and Systems (ISCAS'2020)
May 17-20, 2020, Seville, SPAIN
Rang : A
technical program committee: BARRAGAN M.

23rd Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS'2020)
April 22-24, 2020, Novi Sad, SERBIA
Rang : B
technical program committee: BARRAGAN M.

38th IEEE VLSI Test Symposium (VTS'2020)
April 5-8, 2020, San Diego, USA
Rang : A
technical program committee: MIR S., BARRAGAN M.

21st IEEE Latin-American Test Symposium (LATS'2020)
March 30-April 2, 2020, Jatiúca (Maceió), BRAZIL
Rang : NC
technical program committee: MIR S, SIMEU E.

Design, Automation & Test in Europe (DATE'2020)
March 9-13, 2020, Grenoble, FRANCE
Rang : A+
track chair: BARRAGAN M.

11th IEEE Latin American Symposium on Circuits and Systems (LASCAS'2020)
February, 25-28, 2020, San José, COSTA RICA
Rang : B
technical program committee: MIR S.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
POLYTECH Grenoble				
Manager of Risks Prevention department	SIMEU E.	01/09/2017		
Restricted council member	SIMEU E.	01/09/2017		Examine promotion files, invited professors, teaching assistants
School council member	SIMEU E.	01/09/2017		Elected members - School Strategy, relations with industrial partners
Research structures				
AIP PRIMECA **Productique et ressources informatiques pour la mécanique**				
Manager of CIM AIP PRIMECA platform	SIMEU E.	01/09/2017		
Carnot LSI **Logiciel et Systèmes Intelligents**				
TIMA representative	MIR S.	01/09/2009		
École doctorale EEATS **Électronique Électrotechnique Automatique & Traitement du signal**				
Council member of EEATS doctoral school	SIMEU E.	01/09/2017		
FMNT **Fédération des Micro et Nanotechnologies**				
Manager of Telecommunications Axis	BARRAGAN M.	01/09/2017		

Scientific production

International journals

Margalef-Rovira M., Lugo-Alvarez J., Bautista A., Vincent L., Lepilliet S., Saadi A., Podevin F., Barragan M., Pistono E., Bourdel S., Gaquière C., Ferrari P., Design of mm-Wave Slow-wave Coupled Coplanar Waveguides, IEEE Transactions on Microwave Theory and Techniques, Ed. IEEE, Vol. , DOI: 10.1109/TMTT.2020.3015974, 2020

Melis T., Simeu E., Auvray E., Armagnat P., Analog and mixed-signal circuits simulation for product level EMMI analysis, Microelectronics Reliability, Ed. Elsevier, Vol. 114, DOI: 10.1016/j.microrel.2020.113881, novembre 2020

Margalef-Rovira M., Saadi A., Vincent L., Lepilliet S., Gaquière C., Gloria D., Durand C., Barragan M., Pistono E., Bourdel S., Ferrari P., Highly Tunable High-Q Inversion-Mode MOS Varactor in the 1–325-GHz Band, IEEE Transactions on Electron Devices, Ed. IEEE, Vol. 67, No. 6, pp. 2263-2269, DOI: 10.1109/TED.2020.2989726, juin 2020

Cilici F., Barragan M., Lauga-Larroze E., Bourdel S., Leger G., Vincent L., Mir S., A Nonintrusive Machine Learning-Based Test Methodology for Millimeter-Wave Integrated Circuits, IEEE Transactions on Microwave Theory and Techniques, Ed. IEEE, Vol. , pp. 1-1, DOI: 10.1109/TMTT.2020.2991412, mai 2020

Chegari B., Tabaa M., Moutaouakkil F., Simeu E., Medromi H., Local energy self-sufficiency for passive buildings: Case study of a typical Moroccan building, Journal of Building Engineering, Ed. Elsevier, Vol. 29, No. 101164, DOI: 10.1016/j.jobe.2019.101164, mai 2020

Takam Tchendjou G., Simeu E., Detection, Location and Concealment of Defective Pixels in Image Sensors, IEEE Transactions on Emerging Topics in Computing, Ed. IEEE, Vol. , DOI: 10.1109/TETC.2020.2976807, février 2020

International conferences

Melis T., Simeu E., Auvray E., Analog and Mixed Signal Diagnosis Flow Using Fault Isolation Techniques and Simulation, 46th International Symposium for Testing and Failure Analysis (ISTFA 2020), Virtual event, UNITED STATES, 7 au 9 décembre 2020

El-Chaar M., Lisboa de Souza A.A., Barragan M., Podevin F., Bourdel S., A Non-Closed-Form Mathematical Model for Uniform and Non-Uniform Distributed Amplifiers, IEEE MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM 2020), Linz, AUSTRIA, DOI: 10.1109/ICMIM48759.2020.9299099, 23 novembre 2020

Melis T., Simeu E., Auvray E., Armagnat P., Analog and mixed-signal circuits simulation for product level EMMI analysis, 31st European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF 2020), Virtual event, GREECE, 4 au 8 octobre 2020

Portolan M., Silveira Feitoza R., Takam Tchendjou G., Reynaud V., Senthamarai Kannan K., Barragan M., Simeu E., Maistri P., Anghel L., Leveugle R., Mir S., A Comprehensive End-to-end Solution for a Secure and Dynamic Mixed-signal 1687 System, 2020 International Symposium on On-Line Testing and Robust System Design (IOLTS 2020), Naples (Napoli), ITALY, DOI: 10.1109/IOLTS50870.2020.9159721, 13 au 15 juillet 2020

Melis T., Simeu E., Auvray E., Automatic Fault Simulators for Diagnosis of Analog Systems, 26th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS 2020), Virtual event, ITALY, 13 au 15 juillet 2020

Margalef-Rovira M., Saadi A., Bourdel S., Barragan M., Pistono E., Gaquière C., Ferrari P., mm-Wave Through-Load Switch for in-situ Vector Network Analyzer on a 55-nm BiCMOS Technology, 18th IEEE International NEWCAS Conference (NEWCAS 2020), Montreal, CANADA, 16 au 19 juin 2020

Silveira Feitoza R., Barragan M., Gines A., Mir S., Static linearity BIST for Vcm-based switching SAR ADCs using a reduced-code measurement technique, 18th IEEE International NEWCAS Conference (NEWCAS 2020), Montreal, CANADA, DOI: 10.1109/NEWCAS49341.2020.9159839, 16 au 19 juin 2020

Silveira Feitoza R., Barragan M., Gines A., Mir S., On-chip reduced-code static linearity test of Vcm -based switching SAR ADCs using an incremental analog-to-digital converter, IEEE European Test Symposium (ETS 2020), Tallinn, ESTONIA, DOI: 10.1109/ETS48528.2020.9131588, 25 mai au 1 juin 2020

Takam Tchendjou G., Simeu E., Parametric faults detection and concealment on imager with FPGA implementation, IEEE Latin-American Test Symposium (LATS 2020), pp. 1-6, Maceio, BRAZIL, DOI: 10.1109/LATS49555.2020.9093671, 30 mars au 2 avril 2020

Other communications

Aouimeur W., Margalef-Rovira M., Lauga-Larroze E., Gloria D., Gaquière C., Arnould J.D., A Fully-Integrated High-Isolation Transfer Switch for G-band in-situ Reflectometer applications, IEEE MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM 2020), Linz, AUSTRIA, 2020

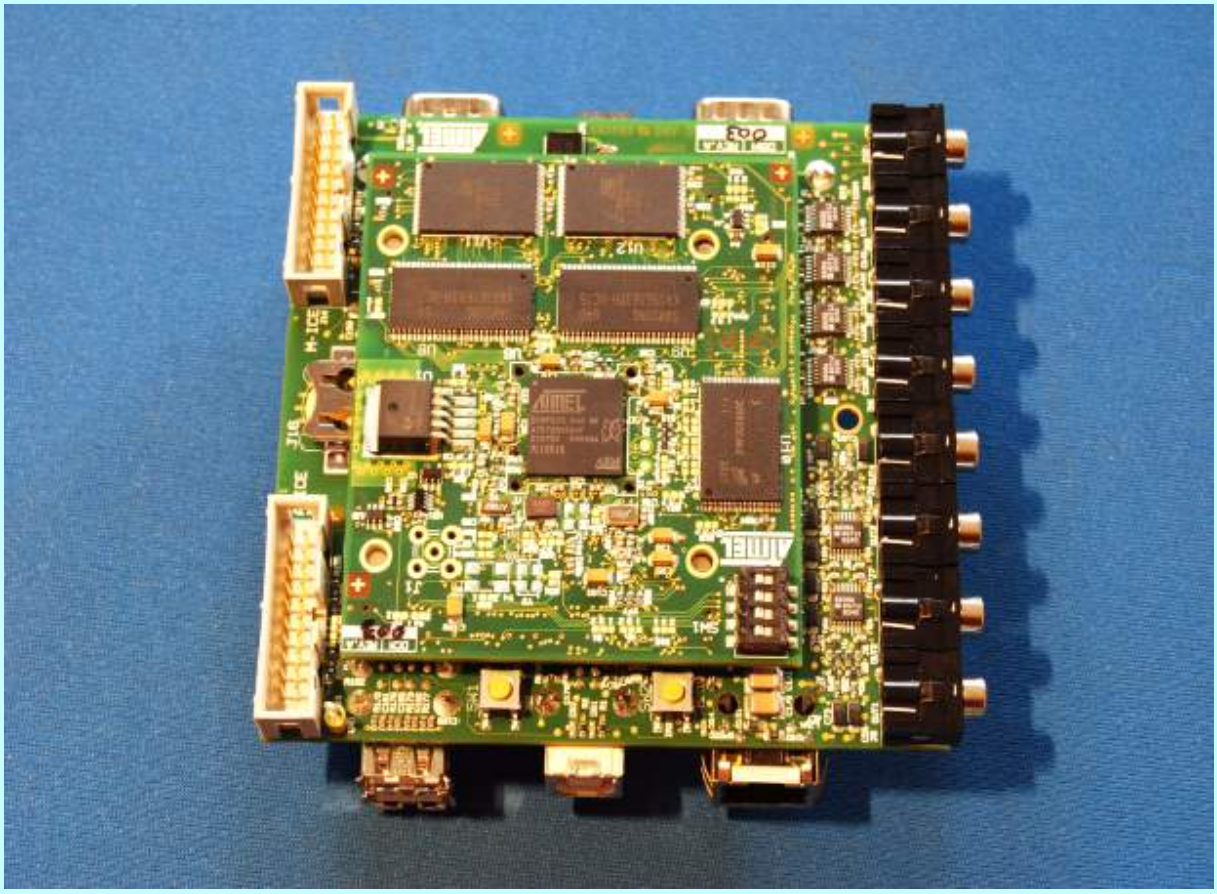
Troussier C., Bourgeat J., Simeu E., Arnould J.D., Jimenez J., Jacquier B., Study of Inter-Power Domain Failures during a CDM Event, IEEE 42nd EOS/ESD symposium (ESDA 2020), Virginia St, Reno, UNITED STATES, 2020

Theses

Margalef-Rovira M., Design of mm-wave Reflection-Type Phase Shifters with Oscillation-Based Test capabilities, These de Doctorat, 11 septembre 2020

CNRS - Grenoble INP - UGA

SLS team



System Level Synthesis

System Level Synthesis (SLS team)

Research activities

The SLS team focuses on (a) highly efficient architectures for general purpose computing or AI-dedicated algorithms, (b) system-level modeling and design methodology : specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware. The work of the team is included in the Laboratory themes “Hardware/software codesign” and “Simulation and verification of systems” described below.

Hardware/software codesign

Our research on high performance general purpose processors explores the use of value prediction in processor design. We have shown that simple value prediction can be implemented by reusing existing pipeline structures, leading to increased performance with reduced overheads. We have also shown that predicting values enables the dynamic "reduction" of some instructions (e.g., transforming an add into a nop at runtime), which further improves performance. So far, we have considered value prediction for out-of-order microarchitectures only.

Multi-core and many-core architectures have evolved towards a set of clusters. Each cluster integrates a set of cores, a cache memory and a local memory shared by all the cores of the cluster. We have worked on hardware methods for distributing memory bank accesses in many-core architectures by experimenting on the MPPA Kalray processor. In addition, we have proposed an innovative hardware support for synchronization locks. This decentralized solution manages dynamic re-homing of locks in a dedicated memory, close to the latest access-granted core.

On the dedicated architecture side, the team is still working on Artificial Intelligence. After our work on high-throughput ternary neural network, we have collaborated with the university of Salerno on the design of a tiny Binary Neural Network for human recognition applications.

Through a collaboration with OVHcloud, we also worked on a dedidated IP used in their mitigation systems to face Distributed Denial-of-Service (DDOS) attacks. In this domain, hard- ware developement has to be agile. By introducing the Chisel hardware construction language in the hardware design flow, we showcase how Chisel unleashes the power of agile development methodologies through development iterations. We have also shown through a General Matrix Multiply implementation case study that Chisel can be used to generate highly parametrizable circuits, bringing huge benefits in design exploration, reuse and designer productivity.

Along with the ever-increasing hardware IP development pace, System-on-Chips (SoCs) now integrate a tremendous amount of IPs, each of them specifying more and more interface registers. This exacerbates the already difficult hardware/software integration challenge, which remains a challenge despite the decades that separate us from the first days of computers. We have proposed a generic interface to devices, using message conduit instead of registers and interrupt, taking inspiration from USB and virtualization strategies. This strategy has the benefit of partitioning the driver in a front-end, which is device and operating system dependent, meaning that few distinct front-ends will be required in practice, and a backend that is the responsibility of the device maker. Our prototypes demonstrate that it is suitable for small systems with low latency and low throughput devices (FPGA IP integration), such as high-performance devices in the Linux kernel or in hypervised systems.

Simulation and verification of systems

Modeling and simulation of cyber-physical devices is challenging because of their heterogeneity: discrete events simulation progresses by discrete timesteps while continuous time simulation does so in a time continuum. The SystemC AMS synchronization strategy is based on fixed timesteps and can generate inaccuracies overcame only at expanse of simulation speed. We have proposed a new continuous time and discrete events synchronization algorithm on top of the SystemC framework and have proven its causality, completeness and liveness. In addition, we have also proposed an adaptive algorithm to adjust the synchronization step to provide near to optimum simulation speed. Results on various cases studies have demonstrated that our algorithm circumvents these challenges, attains high accuracy with respect to established tools, and improves simulation speed. This work aims at enlarging the modeling and simulation capabilities of SystemC as a heterogeneous design tool.

Today’s SoCs require a complex design and verification process. In early design stages, high-level debugging of the SoC functionality is feasible on TLM (Transaction-Level Modeling) descriptions. To ease

debugging of such SoC's models, Assertion-Based Verification (ABV) en- ables the runtime verification of temporal properties. In the last design stages, RTL (Register Transfer Level) descriptions of hardware blocks expose microarchitectural details. To gain confi- dence in the validity of system level properties after this TLM-to-RTL synthesis, transaction level assertions must be reverifiable on RTL models. To address that issue, we propose refinement rules for the automatic system level to signal level transformation of PSL assertions (Property Specification Language, IEEE standard 1850).

Many scientific applications require higher accuracy than what can be represented on 64 bits of the floating-point IEEE 754 standard, and to that end make use of dedicated arbitrary precision software libraries such as MPRF. To reach a good performance/accuracy trade-off, developers use variable precision, requiring e.g. more accuracy as the computation progresses. Hardware accelerators for this kind of computations do not exist yet, and independently of the actual quality of the underlying arithmetic computations, defining the right instruction set ar- chitecture, memory representations, etc, for them is a challenging task. We have investigated the support for arbitrary and variable precision arithmetic in a dynamic binary translator (QEMU implementation), to help gain an insight of what such an accelerator could provide as an interface to compilers, and thus programmers. Through collaborations, we also worked on a FP represen- tation supporting both static and dynamically variable precision : by designing its compilation flow to hardware FP instructions or software libraries, and by demonstrating its performance, far better than the Boost programming interface for the MPFR library on the PolyBench suite.

Publications

http://tima.univ-grenoble-alpes.fr/tima/fr/sls/slspublications.html

Academic and research members

Liliana ANDRADE

Position
Associate professor at UGA

Responsibilities
Researcher in SLS team

Arthur PERAIS

Position
Researcher at CNRS

Responsibilities
Researcher in SLS team since 01/10/2020

Laurence PIERRE

Position
Professor at UGA – IM2AG school

Responsibilities
Researcher in SLS team

Olivier MULLER

Position
Associate professor at Grenoble INP – ENSIMAG school

Responsibilities
Leader of SLS team since 01/01/2020
Researcher in SLS team

Frédéric PÉTROT

Position
Professor at Grenoble INP – ENSIMAG school

Responsibilities
Deputy Director of TIMA Lab. since 01/2015
Researcher in SLS team

Frédéric ROUSSEAU

Position
Professor at UGA – POLYTECH school

Responsibilities
Researcher in SLS team

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. BADAROUX Marie
Title of thesis: **Fast and accurate simulation of multi/many-core SoCS**
Expected date of defense: **2023**
Previous degrees: Master – Grenoble INP – ENSIMAG, France (2020)

2. BAUMELA Thomas
Title of thesis: **Externalisation of device drivers from embedded processors to devices**
Expected date of defense: **2021**
Previous degrees: Engineer – Université Grenoble Alpes, France (2016)

3. BONICEL Louis
Title of thesis: **Study of an architectural model for code generation taking into account the real time constraints of an embedded system in the electrical measure and protection domain**
Expected date of defense: **2022**
Previous degrees: Engineer – Polytech Montpellier, France (2017)

4. BRUANT Jean
Title of thesis: **Abstracting FPGA development flow as a modern software development flow**
Expected date of defense: **2021**
Previous degrees: Engineer - Télécom Bretagne, France (2018)

5. CHRIST Maxime
Title of thesis: **Learning in very low precision**
Expected date of defense: **2022**
Previous degrees: Engineer - INSA Lyon, France (2017)

6. FERNANDEZ-MESA Breytner Joseph
Title of thesis: **Exploration of Direct Synchronization Approaches for a High-Level and Unified Simulation of Discrete-Event/Continuous-Time Systems**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidad de Los Andes – Mérida, Venezuela (2017)

7. FERRES Bruno
Title of thesis: **Task migration software/hardware in an heterogeneous and reconfigurable system**
Expected date of defense: **2022**
Previous degrees: Engineer – Grenoble INP - Ensimag, France (2018)

8. MILICI Giulio
Title of thesis: **Strategy of crosspoint non-volatile memory integration in cache hierarchy of a multicore architecture**
Expected date of defense: **2021**
Previous degrees: Engineer – Politecnico di Torino, Italy (2018)

9. TREVISAN JOST Tiago
Title of thesis: **Compiler-Hardware interface of emerging UNUM number formats**
Expected date of defense: **2022**
Previous degrees: Master – Federal University of Rio Grande do Sul, Brazil (2017)

10. VIANES Arthur
Title of thesis: **Integration of a Manycore Accelerator in a High-Performance Processor**
Expected date of defense: **2022**
Previous degrees: Engineer Polytech Grenoble, France (2018)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

No positions in 2020.

Visitors

Name	Forename	Country	Duration
1. DE VITA	Antonio		

Trainees

Name	Forename	Country	Duration
1. DJEAFEA SONWA	Medric Bruel	CAMEROON	
2. HAMAIN	Thomas Frederic Robert	RUSSIAN FED	
3. LAGAROSSE	Paul	FRANCE	
4. ROBE	Guillaume	FRANCE	
5. YADAV	Archit	INDIA	
6. ZHANG	Shuo	CHINA	
7. KEMEH	Marck-Edward	GHANA	

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANR

RAKES
Responsable scientifique : PETROT Frédéric
Durée : 2019 - 2023

ANRT

CIFRE Arthur VIANNES
Responsable scientifique : ROUSSEAU Frédéric
Durée : 2019 - 2022

CIFRE Jean BRUANT
Responsable scientifique : MULLER Olivier
Durée : 2018 - 2022

CIFRE Louis BONICEL
Titre : "Etude d'un modèle architectural pour la génération de code intégrant les contraintes d'un système temps réel embarqué dans le domaine de la mesure et la protection électrique"
Responsable scientifique : PETROT Frédéric
Durée : 2018 - 2021

CIFRE Lucas FERNANDEZ-BRILLET
Titre : "Architectures intégrrées 3D de réseaux de neurones CNN pour la vision embarquée"
Responsable scientifique : MANCINI Stéphane
Durée : 2017 - 2020

CEC-NATIONAL

AI4DI
Programme : ECSEL
Titre : Artificial Intelligence for Digitizing Industry
Responsable scientifique : PETROT Frédéric
Durée : 2019 - 2022

EPST

ARTE
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Architectures de Réseaux de neurones Ternaires dédiées pour l'Embarqué
Responsable scientifique : ANDRADE PORRAS Liliana Lilibeth
Durée : 2019 - 2020

Digital Hardware AI Architectures
Programme : MIAI (Multidisciplinary Institute in Artificial Intelligence)
Type : EPST
Responsable scientifique : PETROT Frédéric
Durée : 2019 - 2023

Organization and participation of international conferences, workshops, forums

31st International Workshop on Rapid System Prototyping (RSP'2020)
September 24-25, 2020, Virtual event, FRANCE
Rang : B
steering committee member: PETROT F., ROUSSEAU F.
technical program committee: MULLER O., PETROT F., ROUSSEAU F.
program chair: ROUSSEAU F.
publication chair: MULLER O.

Conférence francophone d'informatique en Parallélisme, Architecture et Système (COMPAS'2020)
June 30-July 03, 2020, Lyon, FRANCE
Rang : NC
technical program committee: PETROT F.
20th International Forum on MPSoC for Software-Defined Hardware (MPSoC'2020)
June 28-July 3, 2020, Megève, FRANCE
Rang : NC
general chair: PETROT F.
technical program committee: PETROT F.
finance chair: ROUSSEAU F.
local organization: MULLER O., ROUSSEAU F.

23rd Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS'2020)
April 22-24, 2020, Novi Sad, SERBIA
Rang : B
technical program committee: PIERRE L.

Design, Automation & Test in Europe (DATE'2020)
March 9-13, 2020, Grenoble, FRANCE
Rang : A+
University Booth Co-Chair: PETROT F.

12th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO'2020)
January 21, 2020, Bologna, ITALY
Rang : NC
technical program committee: PETROT F.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
ENSIMAG school École nationale supérieure d'informatique et de mathématiques appliquées				
Deputy Director	PETROT F.	01/09/2018	31/08/2022	
Restricted council member	MULLER O.	01/09/2017		Examine promotion files, invited professors, teaching assistants
	PETROT F.	01/09/2017		
School council member	MULLER O.	01/09/2017		Elected members - School Strategy, relations with industrial partners
	PETROT F.	01/09/2017		
POLYTECH Grenoble				
Manager of E2I branch	ANDRADE L.L.	01/10/2019		5th year - Apprenticeship training
Deputy director in charge of education and training	ROUSSEAU F.	01/09/2018		
Restricted council member	ROUSSEAU F.	01/09/2017		Examine promotion files, invited professors, teaching assistants
School council member	ROUSSEAU F.	01/09/2017		Elected members - School Strategy, relations with industrial partners
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Research commission member	PIERRE L.	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR Council member	PIERRE L.	01/09/2017		
TIMA laboratory				
Laboratory contact for european projects	ROUSSEAU F.	01/09/2017		
Research structures				
École doctorale EEATS Électronique Électrotechnique Automatique & Traitement du signal				
HDR commission member of EEATS doctoral school	ROUSSEAU F.	01/09/2017		
École doctorale MSTII Mathématiques, Sciences et Technologies de l'Information, Informatique				
Council member of MSTII doctoral school	PIERRE L.	01/09/2017		
HDR commission member of MSTII doctoral school	PETROT F.	01/09/2017		
LABEX PERSYVAL Pervasive Systems and Algorithms				
Education Board Member	PIERRE L.	01/06/2015		Training activities
Pôle MSTIC Mathématiques, sciences et technologies de l'information et de la communication				
TIMA representative of MSTIC cluster	PETROT F.	01/09/2016		
Parent institutions				
UGA Université Grenoble Alpes				
Manager of Informatics Master M1-M2 UGA – G-INP	PIERRE L.	01/09/2017		In charge for UGA

Scientific production

International journals

Fernandez-Mesa B.J., **Andrade Porras L.L.**, **Pétrot F.**, Synchronization of Continuous Time and Discrete Events Simulation in SystemC, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Ed. IEEE, Vol. , DOI: 10.1109/TCAD.2020.3019204, 2020

Invited conferences talks

1 **Pétrot F.**, **Anghel L.**, **Andrade Porras L.L.**, State of the art in hardware-accelerated neural networks, Invited Talk, Applied Machine Learning Days (AMLD 2020), Lausanne, SWITZERLAND, 27 au 29 janvier 2020

International conferences

Leclaire N., **Mancini S.**, **Delnondedieu C.**, **Henriques J.P.**, Efficient Implementation of Convolution and Winograd on ASMP Embedded Multicore Vector Processor, IEEE International Workshop on Signal Processing Systems (SIPS 2020), Coimbra (Virtual event), PORTUGAL, 20 au 22 octobre 2020

Trevisan Jost T., **Durand Y.**, **Fabre Ch.**, **Cohen A.**, **Pétrot F.**, VP Float: First Class Treatment for Variable Precision Floating Point Arithmetic, International Conference on Parallel Architectures and Compilation Techniques (PACT 2020), pp. 355-356, Atlanta, UNITED STATES, 5 au 7 octobre 2020

Pêcheux F., **Andrade Porras L.L.**, **Louërat M.-M.**, **Bournias I.**, **Chotin-Avot R.**, **Genius D.**, Virtual Prototyping of Open Source Heterogeneous Systems with an Open Source Framework Featuring SystemC MDVP Extensions, Forum for Specification and Design Languages (FDL 2020), pp. 1-8, Kiel, GERMANY, DOI: 10.1109/FDL50818.2020.9232947, 15 au 17 septembre 2020

De Vita A., **Pau D.**, **Di Benedetto L.**, **Rubino A.**, **Pétrot F.**, **Licciardo G.D.**, Low Power Tiny Binary Neural Network with improved accuracy in Human Recognition Systems, Euromicro Conference on Digital System Design (DSD 2020), pp. 309-315, Kranj, SLOVENIA, DOI: DOI 10.1109/DSD51259.2020.00057, 26 au 28 août 2020

France-Pillois M., **Martin J.**, **Rousseau F.**, Implementation and Evaluation of a Hardware Decentralized Synchronization Lock for MPSoCs, International Parallel and Distributed Processing Symposium (IPDPS 2020), pp. 1112-1121, New Orleans, UNITED STATES, DOI: 10.1109/IPDPS47924.2020.00117, 18 au 22 mai 2020

Fernandez-Mesa B.J., **Andrade Porras L.L.**, **Pétrot F.**, Accurate and Efficient Continuous Time and Discrete Events Simulation in SystemC, Design, Automation and Test in Europe (DATE 2020), Grenoble, FRANCE, 9 au 13 mars 2020

Other communications

Ferres Bruno, **Muller O.**, **Rousseau F.**, Chisel Usecase: Designing General Matrix Multiply for FPGA, Applied Reconfigurable Computing. Architectures, Tools, and Applications (ARC 2020), pp. 61-72, Toledo, SPAIN, DOI: 10.1007/978-3-030-44534-8_5, 2020

Christ M., **Forget L.**, **De Dinechin F.**, Lossless Differential Table Compression for Hardware Function Evaluation / Compression de table sans perte pour l'évaluation matérielle de fonctions, , Grenoble, FRANCE, 2020

Bruant J., **Horrein P.H.**, **Muller O.**, **Groleat T.**, **Pétrot F.**, (System)Verilog to Chisel Translation for Faster Hardware Design, 31th International Symposium on Rapid System Prototyping (RSP 2020), Virtual Conference, FRANCE, 2020

TIMA Laboratory

46 avenue Félix Viallet
38031 GRENOBLE Cedex 1
FRANCE

Tel: +33 (0)4 76 57 50 79
E-mail: tima-direction@univ-grenoble-alpes.fr

http://tima.univ-grenoble-alpes.fr

follow us

https://www.linkedin.com/company/tima-laboratory

https://www.youtube.com/results?search_query=tima+laboratory