TIMA Laboratory

Scientific report

2019

Summary

Foreword 4

AMfoRS team (Architectures and Methods for Resilient Systems) 5

CDSI team (Circuits, Devices and System Integration) 9

RIS team (Robust Integrated Systems) 14

RMS team (Reliable Mixed-Signal circuits and Systems) 16

SLS team (Systems Level Synthesis) 20

Academic and research members 23

Staff members 28

Ph.D. candidates 30

Other members of TIMA 34

Contracts 36

International activities 46

Educational tasks 54

Roles of TIMA members on University faculties and research structures 55

Scientific production 57

Press review 67

Foreword

TIMA is a public research laboratory sponsored by Centre National de la Recherche Scientifique (CNRS), Grenoble Institute of Technology (Grenoble INP) and Université Grenoble Alpes (UGA). TIMA addresses some of the most urgent and ambitious challenges related to the design of circuits and Systems-on-chip (SoC). The research topics cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor SoCs together with their basic operating system on the other end.

In 2019, a total of 158 persons have worked in the Laboratory including 37 permanent members (24 research staff and 13 administrative and technical staff) and 121 temporary members (45 PhD students, 12 post-doc/expert-collaborator/associate researchers, 6 other temporary support and research staff, 47 trainees and 11 visitors).

The laboratory is structured in the following five research teams:

- ***Architectures and Methods for Resilient Systems (AMfoRS):*** multi-level specification and verification of hardware/software on-chip architectures; system-level modeling, analysis and testing; dependability of integrated systems; secured integrated architectures; multi-level dependability evaluations.
- ***Circuits, Devices and System Integration (CDSI):*** MEMS: microgenerators, acoustic sensors, pressure microsensors; BIOMEMS microsystems; asynchronous circuits and systems (asynchronous IP's, NoCs, GALS, etc.); non-uniform sampling and signal processing (algorithms, architectures, circuits); reconfigurable asynchronous logic; safe and secure robust asynchronous circuits; smart CMOS vision sensors.
- ***Robust Integrated Systems (RIS):*** robust massively parallel single-chip architectures; power management from the OS down to silicon; fault tolerant and self-adaptive architectures; 3D NOC robust architectures; design-for-reliability due to aging; process variation and soft errors; evaluation of robustness and qualification: radiation tests, fault injection; architectures for nanotechnologies.
- ***Reliable Mixed-Signal circuits and systems (RMS):*** mixed-signal/RF integrated devices; test and control techniques; design-for-test; diagnosis; embedded control; behavioral and statistical modeling methods; CAD tools for test and control.
- ***System Level Synthesis (SLS):*** HW/SW architectures and CAD software for multiprocessor systems on chip; specification, modeling, simulation and implementation of embedded systems on chip; reconfigurable systems and rapid prototyping.

The 2019 edition of the TIMA annual report presents a brief and synthetic presentation of the scientific achievements of each research team, followed by a description of the personnel, on-going research contracts, international activities, major educational roles and tasks, and a complete list of this scientific production, classified by team and category. The scientific production of 2019 includes 124 results: 22 articles in international journals, 55 articles in international conferences, 13 PhD theses, 15 invited talks, 3 books, 3 book chapters, 1 journal edition, 11 other communications and 1 protected software.

A large part of the research is financed by research grants and contracts. Some are large cooperative projects with industrial and academic partners, at the national, European or world level; others are bilateral industrial collaborations linked to a CIFRE doctoral co-tutorship or academic collaborations funded by our parent institutions. Most contracts run from 3 to 4 years. In 2019, 47 contracts were in operation, out of which 18 new contracts started during the year. The report gives an overview of the contractual activity.

Members of TIMA were active in the organization of 45 international conferences and workshops. The details of these contributions to the scientific community are listed in the report.

Finally, TIMA takes an active part in the organization of the Grenoble Alpes research community, being linked to the poles "Mathematics, Informatics and Communication" (MSTIC) and "Physics, Engineering and Materials" (PEM). TIMA is also a member of the Carnot Institute LSI, the Laboratory of Excellence Persyval and the local federation of micro and nanoelectronics laboratories FMNT.

Salvador MIR

Further information may be obtained from:
Salvador MIR – TIMA Laboratory - 46 avenue Félix Viallet - 38031 GRENOBLE Cedex, FRANCE
Tel : (+33) 4 76 57 45 86 - E-mail : directeur-tima@univ-grenoble-alpes.fr
http://tima.univ-grenoble-alpes.fr/

Architectures and Methods for Resilient Systems (AMfoRS)

Permanent Personnel
Lorena ANGHEL[(1)] (PR1 Grenoble INP, Section 61)
Mounir BENABDENBI (MCFCN Grenoble INP, Section 61)
Giorgio DI NATALE (DR2 CNRS, Section 7)
Régis LEVEUGLE (PREX Grenoble INP, Section 27)
Paolo MAISTRI[(2)] (CR1 CNRS, Section 7)
Michele PORTOLAN[(3)] (MCFCN Grenoble INP, Section 27)
Ioana VATAJELU (CRCN CNRS, Section 8)

(1) Team co-leader
(2) Team co-leader
(3) Mobility for academic collaboration to Politécnico de Torino until end 08/2019

Temporary personnel		
PhD Students	8	Noureddine AIT SAID Xavier AUBERT Valérian CINÇON Geoffrey DELAHAYE Pietro INGLESE Vincent REYNAUD Kalpana SENTHAMARAI KANNAN Riddhi SHAH
ATER, PAST, Emeritus	1	Dominique BORRIONE
Trainees	7	Ali BAWAB Ali Sohaib CHAFIK Mona EZZADEEN Alessandro FICI Victor MESNAGER Muhammad Talha QURESHI Lucas SANTANDER

Research Activities

The AMfoRS team addresses trust and dependability of digital systems at multiple abstraction levels. This can be achieved by guaranteeing that digital circuits possess a number of different properties, possibly depending on the specific application domain, such as reliability, safety, security, availability, specification compliance. The work is focused on design and analysis methods, techniques and tools applying to above-mentioned domains.

System-level test and standards

The IEEE 1687-2014 standard proposes solutions for the access and usage of Embedded Instruments. Even though the standard has already been published and industrial acceptance is high, Electronic Design Automation (EDA) is still limited to only a small subset of the new features, and the real novelties are not considered. In this context, in the frame of the Eureka European project HADES, we carry on developing an innovative Test Flow and Environment called “Manager for SoC Test” (MAST), a software backend able to provide features and performance superior to the industrial legacy solutions [RI-8]. We are using MAST as the basis for new experimentations and abstractions, and we have a strict interaction with the IEEE P1687.1 Working Group, which is evaluating our proposals for inclusion in the upcoming release of the standard.

Aging Induced Reliability evaluation and Robustness improvement

Process, voltage, temperature and other environmental variations in current CMOS nanometric digital designs cause performance degradations and may lead to functional failures, which can be serious issues in critical and mixed-critical systems (such as automotive, health-care, avionic and space applications). Usually timing errors can manifest on critical propagation paths and are detectable by timing-violation monitors. The usage of monitors for error and pre-error detection allow decreasing margins imposed on the overall design. They can be implemented together with Adaptive Voltage Scaling (AVS) or Dynamic Voltage Frequency Scaling (DVFS) techniques which are triggered by the pre-errors of in-situ timing monitors while adapting dynamically the frequency and the voltage according to the operating conditions and the application needs. In the framework of the European Eureka project HADES, we have continued the design of different pre-error monitor

techniques. They are based on Replica Path principle, but the design has been optimized to allow sensing local and global variability and aging degradations. We also explore a new research direction consisting in finding a near-optimal monitor placement strategy based on predictive aging modeling. Therefore, we prioritize data-driven automated learning approaches to model the specific near-unpredictable behavior of transistor aging using ML-friendly models. This allowed us to couple a lightweight Machine Learning prediction framework with traditional, computationally intensive circuit simulations as validation. This Proof-of-Concept was presented in the past and given as a keynote talk in [INV-7], where we demonstrated its capability to accurately model path aging. The activity is progressing on two fronts: on the one hand port the model to the FDSOI 28nm technology, more prone to aging, and on the other hand, to apply the ML framework to the identification of an optimal set of monitor insertion points. Since 2018, we have worked on the design of a novel in-situ delay monitor adapted to detect delay faults, including hidden delay faults (i.e., a delay fault, which is smaller than the slack of the propagation path). Compared to existing solutions, the proposed monitor has a polymorphic behavior and can be used (i) during testing to perform user-defined hidden-delay-fault test, (ii) for reliability degradation estimation due to process, environmental variations and aging, and (iii) in security to detect the insertion of Trojan horses that alter the path delay [CI-9].

Safety and security evaluation

In the recent years, many domains have added functional safety to the classical list of design constraints, e.g. ISO 26262 standard in automotive towards autonomous vehicles. Similar standard evolutions occurred in other areas. Our work aimed at improving early evaluations of dependability w.r.t. errors induced by environmental disturbances. The goal, in order to reduce development and production costs, is to be able to evaluate accurately and at an early stage of the design the potential functional effects of (soft) errors. Classical fault-injection approaches at RT-level (where registers can be identified), known for a long time in the team, are not efficient enough even with emulation-based support. A software developed in the team called "EARS" has been leveraged to allow an accurate analysis of data lifetime in registers, in the context of approximate computing [CI-5] and also led, associated to other works, to an embedded tutorial at ETS19 [CI-4]. Following these works, we are working towards a more accurate evaluation of error consequences with respect to the global system, since all circuit output errors are not critical from a system point of view. This is done in the context of the Aura Region project Safe-Air, with contributions from both classical dependability analysis and formal verification techniques.

When considering the different hardware components, the memory components are more susceptible to soft errors, thus they have significant impact on the overall system reliability. We have presented an analytical methodology to measure the vulnerability of the memory components of a microprocessor-based computing system [RI-2]. It is based on the data and the instruction lifetime and residence [RI-5]. The proposed approach considers only the software-layer of the system, which makes it usable at early design stage when the hardware architecture is not fully defined. Then, to consider the hardware memory hierarchy (i.e., RAM, Caches, Register Files) at software level, we have developed a memory subsystem emulator that can be easily configured to support different features. The methodology can be used to perform a fast, easy and not costly cache-aware Design Space Exploration (DSE) to accurately evaluate the vulnerability of the RAM and the caches. We have validated the approach on small benchmarks (Mibench) and proven the efficiency of the proposed approach on a real industrial test case (i.e., a Flight Management System for avionic application). The results show that the proposed methodology gives precise results compared to a classical fault injection tool, and it scales well with the complexity of the application.

Robustness of emerging computing technologies

Today’s computing systems are facing a plethora of issues related to architectural and technological limitations. From a technology perspective, the main issues are related to CMOS technology scaling, i.e., diminished returns in performance and increased leakage power. To mitigate these issues, novel emerging technologies are being researched, such as memristive and spintronic devices, in conjunction with novel computing paradigms, such as computing in memory - CIM, or neuromorphic computing. Our current research and collaborations in relation with this topic are threefold: (i) to use enhanced compact models of emerging devices to perform failure analysis and define pertinent fault models [INV-2], (ii) to investigate meaningful reliability threats affecting the computing modules and architectures (CIM and neuromorphic), and derive solutions for their mitigation (Design-for-Reliability) [INV-6] ; and (iii) to establish design and test methodologies for these devices and architectures. This work has been presented as an ‘invited talk’ at the national Workshop GDR BioComp 2019. We have developed an in-house tool for training, inferring and evaluating the performance under faults of a spiking neural network (HW ready). To the best of our knowledge, this is the first tool containing a platform for fault injection in SNNs.

Security primitives and hardware trust

The implementation of security primitives has been enriched with the use of high-level synthesis tools and methodologies. In the IoT context, innovative ways have to be explored to achieve low cost and security: we have proposed some approaches to improve the global security at low cost. In particular, we proposed an improved approach to provide secure authenticated access to test structures [CI-1]. On a second front, our research activities covered the design and evaluation of True Random Number Generators (TRNG) and Physically Unclonable Functions (PUF). True Random Number Generators (TRNGs) are used to generate random numbers from a physical process. We have proposed a solution exploiting the intrinsic stochastic properties characterizing the write operation in magnetic devices [RI-4]. Indeed, the write operation has a stochastic behavior, which can be manipulated to set the write probability to 50%, thus generating random numbers. The design is straightforward and the quality of the random numbers is guaranteed from the first generated bit. Physically Unclonable Functions (PUFs), on the other hand, exploit intrinsic manufacturing variability introduced in a device during the fabrication process to generate a signature, unique to each single device and robust w.r.t. aging and environmental variations. In this context, our research is focused on the hardware implementation of reliable and attack-resistant PUFs. We have proposed solutions to identify and mask unreliable PUF responses; we then exploited this information to design a PUF scheme able to generate Zero Bit-Error-Rate response. In addition, we are presenting a novel approach for building Strong PUFs that are inherently resistant to modeling attacks in IOLTS'19 and a solution to analyze and improve the reliability of PUFs [CI-11]. These results have been also presented in a keynote talk in PESW'19 |INV-5].

New hardware computing approaches

In the last few years, a promising solution known as "Approximate Computing" (AC), has been gaining more and more interest in the scientific community both in the industry and in academia. AC is based on the intuitive observation that, while performing exact computation requires a high amount of resources, allowing selective approximation or occasional violation of the specification can provide significant gains in power consumption. Or, for the same amount of consumption, performances can be enhanced. Various applications of AC were surveyed by the scientific community such as data analytics, scientific computing, multimedia, signal processing, machine learning and so forth. We are collaborating with the LIRMM Laboratory on this topic. At circuit level, we developed, in collaboration with the CDSI team, adders, multipliers and MACs using redundant arithmetic [CI-10]. At system level, we are developing a precision evaluation platform based on Berkeley's Rocket Chip HW/SW environment (RISC V based).

Nano-crossbar arrays have emerged as area- and power-efficient structures with an aim of achieving high performance computing beyond the limits of current CMOS. Due to the stochastic nature of nano-fabrication, nano arrays show different properties both in structural and physical device levels compared to conventional technologies. A competent logic synthesis methodology must consider basic technology characteristics for switching elements, defect or fault rates of the given nano switching element and the variation values, as well as their effects on performance metrics including power, delay, and area. Our current interests are leading towards development of a complete synthesis and optimization methodology for switching nano-crossbar arrays to enable design and construction of emerging nanocomputer. This work has been done in collaboration with U of Milano. Moreover, we have investigated the possible defects and faults that can occur in these types of structures and related technologies and proposed defect tolerance techniques which can be employed during logic synthesis. The impact of the crossbar sensitivity on the algorithm is leading to a lot of challenges [INV-7]. Our current and future research and collaborations are related to logic synthesis-dependent defect/fault tolerance techniques, and variation-area-power-delay performance optimization of logic and arithmetic operations mapped on crossbars.

Highlights

- Interaction with the IEEE P1687.1 Working Group
- Keynote talk in LATS 2019 in test and security embedded monitors
- Open-source fault injection tool for SNNs
- Participation to the Grenoble Alpes CyberSecurity Institute for post-quantum cryptography
- Keynote talk at PESW 2019

Indicators

Scientific production	2019
International journals	9
International conferences	18
Book chapters	1
National journals	1
National conferences	2
Other communications	4

Scientific recognition	2019
Prizes and distinctions	1
Invited conferences	8
Conference/workshop Committees	27
Journal Edition Committees	3

Contracts 2019		
ANR	1	Eminent (2019-2023)
ANRT	3	STMicroelectronics (2) / Dolphin (1)
CEC	1	NanoxComp (2016-2019)
EPST	4	IDEX Grenoble IRS (2), MIAI Institute (1), IRT Nanoelec (1)
EUREKA	1	Hades (2017-2020)
Région	1	Safe-air (2017-2022)

Circuits, Devices and System Integration (CDSI)

Permanent Personnel
Skandar BASROUR[1] (PREX UGA, Section 63)
Agnès BONVILAIN (MCFHC UGA, Section 63)
Laurent FESQUET[2] (MCFHC Grenoble INP, Section 61)
Stéphane MANCINI (MCFCN Grenoble INP, Section 61)
Katell MORIN-ALLORY (MCFCN Grenoble INP, Section 27)
Rodrigo POSSAMAI BASTOS (MCFCN UGA, Section 61)

[1] Team co-leader and TIMA vice-director
[2] Team co-leader, CNRS mobility from 01/09/2017 to 28/2/2019 and CIME Nanotech vice-director

Temporary personnel			
PhD Students	20	Mohamed AKRARAI Ricardo AQUINO GUAZZELLI Jérémy BELOT François BERTRAND Yoan DECOUDU Assia EL HADBI Lucas FERNANDEZ BRILLET Thiago FERREIRA DE PAIVA LEITE Raphael FRISCH Matheus GARAY TRINDADE	Sophie GERMAIN Grégoire GIMENEZ Mohammed-Bilal HACHEMI Rodrigo IGA JODUE Arthur KALSING Thomas LAUWERS Nicolas LECLAIRE Andrei POPESCU Otto Aureliano ROLLOFF Julie ROUX
ATER, PAST, Emeritus	1	PAST : Sylvain ENGELS	
Postdocs, engineers, expert collaborators	5	Post-docs : Antonino PROTO Engineers : Nils MARGOTAT Experts : Martial DEFOORT Thibault RICART Ali SKAF	
Trainees	20	Oubaid AKRMI Suresh ALASATRI Ahmed BAAZAOUI Oualid BACHIR-ELEZAAR Carlos Augusto BERLITZ Oussama BOUGHZALA Ismail EL KHAMSI Badri GHANEM Joycelyn HAI Madson Ivens HOLANDA BATISTA	Bara JANOSCOVA Nejmeddine LAKHAL Olivier LIM Bilel MAAMER Liege MALDANER Kenedy MATIASSO PORTELLA Tarik MOUHOUB Dinh-Duy-Kha NGUYEN Baptiste POLLIEN Mohamed YAKHLEF
Visitors	5	Luciano COPELLO OST Rafael FRAGA GARIBOTTI Fernanda GUSMAO DE LIMA KASTENSMIDT Kattan RAFIC Libor RUFER	

Research Activities

Event-driven strategies are fashionable techniques because they offer design flexibility in many field of applications. Indeed, event-driven circuits are known for a long time but they spark interest in really recent challenges such as reliable, safe and secure circuits, low-EM emissions or ultra-low power. Intel announced last year a 130.000 neuron chip based on an asynchronous Spiking Neural Network (SNN) and, very recently, aiCTX presents a 1 million neuron chip based on a Dynamic Neurormorphic Asynchronous Processor (DYNAP). These examples illustrate the today interest in event-driven technology. This latter is studied since 20 years at TIMA and has been applied to several domains. Event-driven strategies are deployed in the CDSI team through different activities covering ultra-low-power circuits, safe and secure circuits, low-EM circuits, reliable, advanced sampling techniques for near-sensor computing.

Nowadays the More than Moore approach is spread in a huge number of devices and systems. In this framework the CDSI team is involved in the design and fabrication of low power smart transducers for IoT and MedTech applications. To reach this target these transducers combines new electroactive materials, ultra-low power read-out circuits and near sensor processing (computing). For instance, the design of low power CMOS vision sensors is explored combining conventional pixels, asynchronous read-out circuit and near sensor processing. Another strong insight concerns the development and integration of new piezoelectric materials for MEMS devices used in acoustics applications, in energy harvesting generators for autonomous systems or for haptic rendering devices.

Probabilistic Machines for Low level Sensor Interpretation

The development of modern computers is principally devoted to increasing performance and decreasing size and energy consumption, without any modification of the principles of computation. In particular, all the components must always perform deterministic and exact operations on sets of binary signals. These constraints impede further progress in terms of speed, miniaturization and power consumption. In cooperation with LIG, Grenoble, we investigated a radically different approach using stochastic bit streams to perform calculation. Our goal has been to show that stochastic architectures can outperform standard computer when solving complex inference problems such as source localization [T4 – Thesis of R. Frisch] and separation both in terms of execution speed and power consumption. The project has been supported by the Persyval Labex and implies LIG, Gipsa and IF laboratories. One of the project results is the creation of the HawAI startup company.

Asynchronous Low-Power Systems (ALPS)

This work targets very ambitious objectives because we expect developing several design tools in a unique framework called ALPS. ALPS stands for Asynchronous Low-Power Systems but integrates different tools able to provide a wide range of asynchronous solutions to designers. On one hand, designers face today problems in implementing circuits while the specifications cover not only the design functionalities but also requirements such as power, security, EMC or safety. On the other hand, the asynchronous strategy based on synchronizing circuits thanks to local handshakes offers a wide range of solutions for targeting at design time the non-functional circuit requirements. All these solutions share the asynchronous and event-based approach but also models and theory. Therefore, a complete framework has been setup in order to integrate several tools that could be connected together. Notice that these tools are complementary to those included in the commercial design flows.

Smart non-uniform sampling schemes

Reducing the power consumption in integrated systems has been the starting point. Indeed, the theoretical and practical researches, pushed in our team since 2000, has highlighted that the Nyquist-Shannon theory tends to capture useless samples. Therefore, Level-crossing sampling schemes (LCSS) have been devised and an Asynchronous Analog-to-Digital Converter (A-ADC) has been designed, fabricated and tested.

Our sampling techniques produce fewer samples than with the traditional Nyquist-Shannon techniques but the samples are not anymore captured thanks to a sampling clock! The consequence of these non-uniform sampling schemes is the non-regular arrival of the data. Nevertheless, this is absolutely not an issue if considering event-driven (asynchronous) circuits. Indeed, thanks to this parsimonious sampling, fewer data are produced and, thus lower activity and power consumption.

ALPS framework

The ALPS framework targets the automated synthesis of integrated systems based on a LCSS analog-to-digital conversion and an event-driven circuit able to process the data captured by the A-ADC. The framework offers the opportunity to evaluate the sampling scheme and the appropriate processing thanks to the SPASS library written in Matlab. Once the sampling scheme and the associate signal processing are fixed, the tools ALPS-HLS and ALPS-ADCGen respectively generate a netlist of the processing unit and another one for the A-ADC. As the designs are specified at an algorithmic level, an automated High-Level Synthesis (HLS, adapted version of AUGH from SLS team) has been targeted.

Shaping EM emissions

Electromagnetic Compatibility (EMC) specifications have always been a hard task for integrated circuit designers. Indeed, the unwanted generation, propagation and reception of electromagnetic energy in integrated circuits may cause unwanted effects such as electromagnetic interference (EMI) or, even worst, physical damage. This work only targets the mitigation of the EM field emitted by a circuit aggressor and tends to respond to this issue for the first time by a design strategy, which could easily be automated. With such an approach, fitting within a spectral mask should become a specific step in the integrated circuit design flow. This is ensured by a specific tool ALPS-EMShaper producing event-based asynchronous micropipeline circuits. Once the event-driven circuit is designed, the method determines the switching instants of the logic thanks to specific delays accordingly chosen with the specified spectral mask [RI10 - JLPEA'2019]. We obtained significant reductions of the electromagnetic spectral peaks with this strategy compared to the spectrum of its synchronous counterpart. A test chip in 40 nm from ST Microelectronics has been designed, fabricated and tested for validating the approach. This works have been done with academic collaborations, the GIPSA and LJK laboratories in Grenoble, and industrial partners such as STMicroelectronics and the Swatch Group in Switzerland.

Low-Power Event-Driven Image Sensors

As the power has become a leitmotiv for all the embedded applications including systems with embedded cameras such as smartphones, the power efficiency of the CMOS image sensors has been enhanced during the last two decades. Nevertheless, the standard reading architecture of image sensors requires an analog to digital converter (ADC), which is currently the most consuming part. Therefore, many studies have been provided in order to reduce the impact of the analog-to-digital converter. Furthermore, the classical reading method of the image sensor consists in reading the entire image for each frame, which induces extra power consumption and useless data. Therefore, the asynchronous event-based image sensors are becoming promising alternatives. The CDSI team proposed an event-driven sensor performing spatial redundancies suppression and thus a data flow reduction in still image and video streaming by only reading pixels with relevant information. In addition, we removed the analog-to-digital converter, and used instead a time-to-digital conversion to encode the pixel information. In order to demonstrate the potential of our approach, two test chips have been designed. The first one is a test chip designed fabricated and tested for characterizing the pixel behavior and comparing two pixel architectures. The second, a fully operational event-based image sensor has been taped-out in February 2019.

This image sensor principle is able to cover different kind of usages. Indeed, the architecture seems to be useful for Time-of-Flight (ToF) measurements and providing 3D vision. For such a purpose, the approach could be coupled to SPAD (Single Photon Avalanche Diodes) or low-noise photodiodes. These kinds of techniques are of interest for 3D vision but also for dust, smoke and fog vision. Moreover, the potentials of this image sensor architecture is large. It could be used as a low-power wake-up imager, High Dynamic Range vision (night and day), low-data rate imager or as high speed image sensor. This work has been supported by the Persyval LabEx and made in cooperation with iCube (Strasbourg), EPFL (Switzerland) and CEA-LETI (Grenoble).

Near Sensor Computing

Several imaging systems have been under investigations in order to develop advanced imaging systems such as adaptive imaging in nuclear medical imaging, video stitching, hyperspectral camera or near sensor deep learning. For instance, video stitching aims at gathering images from several video sources to build a larger image. This implies to implement on an FPGA algorithms performing non-linear mapping from several video sources to a final geometric space. This is typically used in surgery for per-operatory laparoscopy. Another example is the design of Convolutional Neural Network (CNN) targeting a CNN compression, which allows to precisely controlling the trade-off between detection quality, memory occupancy and computing power. All these studies are made in cooperation with Partners including STMicroelectronics, CEA, Gipsa and TIMC.

Event-driven circuit design techniques

Event-driven circuits appear today as an attractive solution for designing robust and low-power chips dedicated to smart sensing and IoT platforms. However, a massive adoption of this technology by the industry requires industrial-grade tools for the design flow. In order to facilitate its dissemination, we targeted asynchronous bundled-data circuits. Indeed, the gap between asynchronous bundled-data and synchronous circuits is sufficiently tight to exploit the existing commercial tools without impacting the design flow and time-to-market. As such an approach requires formal models, formal verification has also been used for checking liveliness and detecting deadlocks. Therefore, practical methods have been developed for specifying, verifying, optimizing and physically implementing asynchronous bundle-data circuits. The results show that asynchronous bundle-data circuits provide lower power consumption than its gated clock counterpart. Finally, this work has been done with several industrial partners among then STMicroelectronics, Dolphin Design, Starchip, IC'Alps, Swatch Group and academic partners IM2NP and EPFL.

Asynchronous Circuits for FDSOI technology

Low-voltage operation is an efficient and well-known strategy to save power at the price of a reduced speed. The Fully Depleted Silicon on Insulator (FDSOI) technology allows mitigating this speed loss thanks to body biasing. In addition, asynchronous circuits use communication protocols which indicate circuit activity. This is used to locally activate/deactivate body biasing when blocks are unused. The research works target the sizing of an optimal granularity for biasing asynchronous circuits in 28-nm FDSOI technology when operating in low-voltage mode. In order to bias small blocks, an analog standard cell - controlled by the asynchronous handshaking signals and dedicated to bias a small area - has been designed. Level shifter architectures were studied for this purpose. A complete asynchronous QDI design flow, dedicated to FDSOI technology, has been proposed and evaluated through this study. The FD-SOI 28-nm standard-cell design flow was developed with Synopsys, Cadence, Mentor and Tiempo CAD tools. This work has been successful thanks to a tight cooperation between STMicroelectronics, Tiempo and TIMA during the Things2Do ENIAC project.

Reliable and trusted systems

Among the design strategies for detecting transient faults caused by radiation or intentional sources, Bulk Built-In Current Sensors (BBICS) offer a promising solution that is perfectly suitable for system design flows based on CMOS standard cells of commercial libraries. BBICS combine the high detection efficiency of costly fault-tolerance schemes (e.g. duplication) with low area and power overheads. Several BBICS architectures have recently been proposed by our team to monitor transient faults induced by radiation or malicious sources. The technique has also been employed for tracking fabrication defects and hardware Trojans. This work has been made in cooperation with EMSE, Gardanne and LIRMM Montpellier.

Time-to-Digital Converters

Accurate time measurements between two events are required in many fields such as high-energy physics, time-of-flight measurement, satellite positioning and instrumentation. A new compact TDC architecture based on STR with sub-gate delay resolution has been devised. The STR allows generating evenly-spaced transitions that can be made arbitrarily close by simply increasing the number of stages. Thanks to these unique STR features, our TDC can virtually achieve a time resolution as fine as desired. The concept has been implemented and tested on an FPGA and on an ASIC in AMS CMOS 350. The work is supported by SCUSI contract from AuRA Région and is made in cooperation with INPT, Morocco.

Micro Power Generators for Autonomous Microsystems

Energy harvesting has been the subject of intense research over the last decades. Various transduction principles have been presented as potential ways of scavenging the ambient energy and transforming it into usable electrical energy. Among these principles, the piezoelectric transduction is probably the most studied one. Most of the approaches that we have studied so far were based on resonant piezoelectric devices with working frequencies above 200 Hz. However, our current work is focused on the development of energy harvesters designed to scavenge energy from real vibrational sources like the heartbeat. Such a design must consider a wideband spectral content of an acceleration source centered in a frequency band not exceeding 30 Hz. The dimensional aspects as the geometry and the volume as well as the energy requirements are critical constraints and play important role in the design strategy

Design and Technologies for Integrated Micro and Nano Systems

The design of new smart Micro and Nano Systems can be achieved in different way. For instance, we have used extensively a CMOS (AMS 0.35µm) compatible process for the design of acoustic transducers for airborne signals. The ultimate goal was the monolithic integration of a device working both as a source and a sensor with electronics, thus facilitating signal routing, suppressing parasitic effects, and improving the signal-to-noise ratio. More recently in the collaboration with the CityU, we presented an aluminum nitride (AlN) CMOS-compatible piezoelectric micromachined ultrasonic transducer (PMUT) capable of an extended detection range of up to 140 cm for touchless sensing applications. AlN-PMUTs have been of increasing interest for range-finding applications over PZT and ZnO films owing to their CMOS-compatibility and maturity of deposition techniques, but are limited to a detection range below 1 m. This technology was also used in collaboration with Univ. of Brescia for the design of new microfluidic components.

In the framework of the project NEED (Cross Disciplinary Project – UGA – Grenoble) we have started the study of thick films of hafnium zirconium oxide HZO. This oxide is a sustainable material and presents promising piezoelectric, pyroelectric, ferroelectric and electrocaloric properties. This material can pave the route of new piezoMEMS devices.

Finally, in the framework of the FMNT (Federation des Micro Nano Technologies), we are developing in collaboration with G2ELab and LMGP laboratories new Piezoelectret polymers using a PDMS matrix. This approach allows us to tailor the electromechanical properties (Young modulus, and piezoelectric coefficients) of stretchable and conformal thick films for soft autonomous sensors embedded in wearable devices.

Highlights

- Bayesian asynchronous computers (LIG, StartUp HawAI.Tech)

Indicators

Scientific production	2019
International journals	7
International conferences	24
Books & Edited Books	1
Softwares	1
PhD thesis	8

Scientific recognition	2019
Prizes and distinctions	1
Invited conferences	4
Conference/workshop Committees	13

Contracts 2019		
ANRT	4	STMicroelectronics (3) / StarChip (1)
Carnot	1	EBIS (2019-2020)
CEC National	2	Ocean 12 (2018-2021) / Things2Do (2014-2019)
EPST	1	Microbayes (2016-2019)
Industrie	2	Icalps (2018-2020) / Thesis of Grégoire GIMENEZ (2016-2020)
International	1	Brafisat (2019-2022)
Ministères-FUI	2	Imspoc-UV (2018-2021) / LISA (2014-2019)
Région	3	Gresam (2019-2020) / Fair (2018-2023) / Convertisseur temps numérique (2017-2020)

Robust Integrated Systems (RIS)

Permanent Personnel
Michael NICOLAIDIS (DR1 CNRS, Section 7) Raoul VELAZCO[(1)] (DR1 CNRS, Section 7) Alain Nasserdine ZERGAINOH (MCFHC UGA, Section 61)

(1) Team leader / Emeritus from 09/2019

Temporary personnel		
PhD Students	1	Alexandre DA PENHA COELHO
ATER, PAST, Emeritus	1	Raoul VELAZCO (Emeritus from 09/2019)
Postdocs, engineers, expert collaborators	3	Postdoc: David César ARDILES SARAVIA Expert : David César ARDILES SARAVIA, Panagiota PAPAVRAMIDOU
Trainees	2	Mohamed BENOMAR Enric GIL
Visitors	2	Said KAROUI Carlos SILVA CARDENAS

Research Activities

RIS team researches deal with the main reliability challenges issued from the advances in integrated circuits manufacturing technologies: high density of defects dues to the variabilities (power supply, temperature …) of manufacturing process, integrated circuits accelerated ageing and soft-errors dues to the impact of energetic particles present in the environment where ICs operate. Moreover it is also considered the impact on reliability of very low power supplies.

Fault-tolerance and reliability of many-core processors and NoCs

The continuous advances in semiconductor technologies make it possible to integrate billions of gates into a single chip. In this context, Multiprocessor System-on-Chips (MPSoCs) design interconnected by Networks-on-Chip (NoCs) is moving towards the integration of tens or hundreds of Processing Elements blocks on a single chip. However, while aggressive technology scaling has its benefits in terms of delay, area, and power consumption, it is known to pose some serious concerns about reliability, suggesting the need for fault-tolerant designs for both MPSoCs and NoCs. The emergence of 3D integration circuit can significantly benefit future MPSoCs by enabling low-latency three-dimensional Networks-On-Chip (3D-NoC) topologies. However, due to the high cost, low yield, and frequent failures of vertical connections, 3D-NoCs are most likely to include only a few vertical connections. Fault-tolerance in NoCs is directly tied to the degree of flexibility of the routing algorithm. High routing flexibility is also required in some irregular topologies, as is the case for TSV-based 3D Network-on-Chips, wherein only a subset of the routers are connected using vertical connections. Unfortunately, routing freedom is often limited by the deadlock-avoidance method, which statically restricts the set of virtual channels that can be acquired by each packet.

SEE sensitivity evaluation of advanced circuits and systems

The continuous shrinking of transistor geometry and the increasing complexity of these devices dramatically affect their sensitivity to natural radiation, and thus diminish their reliability. Single Event Effects (SEEs) are a major concern in Nanoscale technologies, especially for high-density integrated devices.

Methods, tools and platforms for fault injection and simulation

Throughout our research, we have study several new Network-on-Chip designs that need to be tested and validated prior to hardware implementation. At an early stage, novel Network-on-Chip (NoC) designs are usually evaluated and validated by means of cycle accurate simulation. While simulating NoCs at the RTL (Register Transfer Level) can produce very accurate results, popular cycle-accurate simulators are often preferred due to their shorter simulation run times and easier programmability. However, with the tremendous increase in the number of processing nodes in modern and emerging chips, new proposals will have to be validated against increasingly large NoCs, which can take impractical simulation times, even when simulating at a high level of abstraction. GPGPUs (General-Purpose Graphics Processing Units) have been gaining in popularity in various domains, including cycle-accurate simulation. Unfortunately, prior attempts at simulating NoCs on GPU assume an overly simplified NoC architecture and propose a static parallelization method that is very hard to extend and generalize. To the best of our knowledge, no general and scalable method for performing realistic NoC simulations on GPU has yet been proposed.

Highlights

- NASA satellite (see picture below)

The experimental FPGA-based board called COTS-2, devised and designed at TIMA, has been included in the SET payload (https://lws-set.gsfc.nasa.gov/) on the AFRL/NASA DSX satellite, successfully launched June 25, 2019 at NASA's Kennedy Space Center (Florida, USA) and will be in operation until August 2021. The DSX (Demonstration and Science Experiments) satellite is part of the LWS (Living With a Star) NASA program and includes Space Environment Testbeds (SET) that aim at getting experimental data to study how to better protect satellites against effects of energetic radiation particles present at Medium Earth Orbit (MEO) of space, operating around Earth between 6000 km and 12000 km above sea level. The COTS-2 (Commercial Off-The-Shelf) board includes an SRAM-based FPGA in which the implemented digital design has been protected by using a classical state-of-the-art fault-tolerance scheme based on Triple Modular Redundancy (TMR). First experimental results provide clear evidences of the risks of using TMR-based schemes in COTS FPGAs operating within MEO. In fact, since the beginning of the SET mission, COTS-2 board has already reported 21 radiation-induced failures that have not been mitigated by the TMR-based scheme, new results are expected to be obtained until August 2021.

Indicators

Scientific production	2019
International journals	2
Book chapters	2
Books & Edited Books	3
PhD thesis	1

Scientific recognition	2019
Conference/workshop Committees	7
Journal Edition Committees	1

Contracts 2019		
CEC	1	Quog-DP (2019-2020)
Région	1	Ovniprom (2017-2020)
SATT	1	Ovnipromsat / OVSAT (2019-2020)

Reliable Mixed-signal Systems (RMS)

Permanent Personnel
Manuel BARRAGAN (CRCN CNRS, Section 7) Salvador MIR[(1)] (DR1 CNRS, Section 7) Emmanuel SIMEU[(2)] (MCFHC UGA, Section 61)

(1) TIMA director
(2) Team leader

Temporary personnel		
PhD Students	7	Florent CILICI Ioanna KRIEKOUKI Marc MARGALEF ROVIRA Tommaso MELIS Renato SILVEIRA FEITOZA Diane TCHUANI TCHAKONTE Chloé TROUSSIER
ATER, PAST, Emeritus	2	ATER : Mouhamad CHEHAITLY Ghislain TAKAM TCHENDJOU
Postdocs, engineers, expert collaborators	3	Postdocs : Sassi BEN AZIZA Hani MALLOUG Ghislain TAKAM TCHENDJOU
Trainees	3	Giovani Crasby BRITTON OROZCO Imen MIGHRI Javier Alejandro MONGUILO MANTOVANI
Visitors	3	Gildas LEGER Antonio Jose LOPEZ ANGULO Hoang Nam NGUYEN

Research Activities

Since its creation in 2002, the RMS group has addressed the integrated design, test and control of analog/mixed-signal/RF circuits and systems.

Design-for-test of AMS/RF circuits and systems

Testing the AMS-RF functions in a complex integrated system represents nowadays the largest fraction of the test cost. Therefore, simplifying the test of AMS-RF circuits is an area of innovation that may have a significant impact for the IC industry. In this line, Design-for-Test (DfT) solutions are aimed at reducing test cost and complexity by taking into consideration the testability of the circuit at the design stage. Our research in this area has focused on the development of AMS-RF state-of-the-art on-chip test instruments for Built-In Self-Test (BIST) applications and dedicated DfT techniques for reducing test time, complexity and cost. This research has been supported by EUREKA-PENTA European project HADES, and ECSEL European project TARANTO. The major results are described next.

Test solutions for the static linearity test of ADCs. Accurate static linearity test of high-resolution ADCs is one of the most challenging and time-consuming tasks in the production test of a mixed-signal system. Our group has developed two complementary strategies for reducing the cost of static test and relaxing its stringent requirements. Firstly, we have developed reduced-code static linearity test algorithms for pipeline and SAR ADCs. These test algorithms take advantage of the repetitive architecture and/or operation of certain ADC topologies for inferring the complete static linearity characteristics of an ADC from the measurement of a reduced subset of its output codes. Compared to standard histogram testing, we have demonstrated test time reductions in the order of 90% SAR ADCs [RI22], with accuracy better than one LSB. Secondly, we have developed a high-linearity on-chip step-wise ramp stimulus generator for enabling static linearity BIST applications. Our proposed solution is based on a discrete-time integrator whose input stage has been modified to produce a very small gain. A prototype has been designed in ST 65nm CMOS technology. Experimental results from 15 fabricated samples show an average static ENOB of 14.5 bits in a ±2 V differential output range [RI21], well ahead the state-of-the-art. Moreover, the proposed generator can be used for moving reduced-code techniques to a BIST scheme.

Embedded test instruments for the dynamic test of high-speed ADCs. One of the main key points to enable mixed-signal BIST solutions is the development of accurate on-chip analog signal generators that can provide appropriate test stimuli and replace costly external signal generators in standard analog and mixed-signal functional test protocols. In this line, the on-chip generation of sinusoidal stimuli is an unavoidable first step for moving many standard functional tests to a full-BIST solution. In the evaluated period, we have developed novel calibrated harmonic cancellation algorithms that can be employed for designing efficient on-chip sinusoidal signal generators with a high spectral quality using mostly-digital resources. A proof-of-concept demonstrator of the proposed sinusoidal signal generator has been designed in ST 28nm FDSOI technology. Experimental results from fabricated samples show a 10 dB THD and SFDR improvement with respect to the uncalibrated generator, for an output frequency range from 1.7 MHz to 333 MHz [CI43].

Control and optimization of performances for AMS/RF circuits

Our research in this domain has been partially funded by means of a collaboration with the University of Yaoundé, Cameroon, as part of the CETIC project (African Centre of Excellence in Information and Communication Technologies) funded by the World Bank.

Self-Healing of Image Sensors. We have developed a set of methods for monitoring and improving image quality based on the detection and correction of defective pixels, by concealing defective pixels present in the image sensors or introduced during transmission or decoding (VTS'19). The proposed error detection and correction process is based on scanning the image file, and isolating outlier pixel values and correcting them with a local median filtering that does not disturb healthy pixels. The results we are obtaining on the detection and correction of defective pixels now allow us to push the investigations further towards the diagnosis of image sensors, with the aim of identifying the sources of the defects detected and monitoring the ageing of these sensors.

Scheduling control for lifetime optimization in WSN. Limited energy autonomy is a significant barrier to the low-cost deployment of Wireless Sensor Nodes (WSN) technologies. As part of our collaboration with the University of Yaoundé within the CETIC research program, we have addressed the Maximum Lifetime Coverage Problem (MLCP) that aims at controlling a sleep/active schedule for sensors nodes in order to maximize the time span when all the targets are continuously covered by the network. Contrary to previous work that assumed that energy consumed in sleep mode is negligible, a non-zero sleeping energy of sensor nodes is considered in our proposal. The consideration of non-zero energy consumption of sensor nodes in sleep mode is more realistic but significantly increases the complexity of the problem. We address this question by proposing a greedy algorithm that gives priority to sensors with lowest energy, and uses a blacklist to limit the number of sensors covering critical targets. Simulations show that this algorithm outperforms the previously published solutions. Another contribution of this work is a formal framework, based on graph automorphisms and linear algebra, for ring connected networks that generalize a well-known tricky example of the literature. We have proposed for regular arrays, an analytical approach which shows that, for any optimal solution, all sensors' remaining energies are zero. This theoretical approach sheds new light on ring connected arrays of odd size that are known to be rather tricky when non-disjoint cover sets are considered [T12 – Thesis of D. Tchuani].

Design of AMS/RF circuits and systems

The development of advanced AMS/RF circuits has been carried out through the joint research laboratory PYXCAD created in 2018 with the start-up company XDIGIT (currently running for the period 2018-2020) and a doctoral contract (2016-2019).

High performance ADCs for industrial imaging applications. The goal of the joint laboratory PYXCAD is the development of very high performance analog/mixed-signal measurement interfaces and software solutions for the treatment of the generated data. The work in 2019 has continued with the optimized layout of switched-capacitor ADCs for image sensors, using customized capacitances rather than the usual pcells that are made available with the technological design kits. In parallel, an advanced characterization test bench has been developed, using an Applicos test equipment that is very flexible for testing converters.

Design of embedded sensors and tuning knobs for yield enhancement of RF and mmW circuits. In collaboration with the Laboratory RFICLab, we have designed tuning knobs based on variable decoupling cells which have been implemented for calibration purposes of a 60 GHz Power Amplifier designed in STMicroelectronics 55nm CMOS technology. A one-shot calibration procedure reads the output of embedded process monitors and then relies on a machine learning regression model to find the best configuration of the tuning knobs for optimizing the performance of the circuit and enhance fabrication yield [CI53].

Machine learning-based modeling of AMF/RF circuits and systems

This research has been partially supported by CNRS PICS project IndieTEST (PICS07703).

Feature selection and feature design in the context of machine learning-based test. The definition of the input space of signatures is one of the key aspects that limit the adoption of machine learning-based test as a methodology. Together with the Instituto de Microelectrónica de Sevilla (IMSE-CNM, CSIC-Universidad de Sevilla), Spain, we have explored efficient methodologies for feature selection and feature design in the context of machine learning-based test applications of analog, mixed-signal, and RF integrated circuits [CI48]. Feature selection techniques considered include filters based on the Brownian distance correlation metric, wrapper algorithms for feature selection, and we proposed a novel correlation-guided wrapper. Finally, we devised a novel algorithm to automate the design of features and assist in the physical implementation of machine learning-based test. Our proposal was demonstrated on a 60 GHz PA case study [CI53] showing the potential of indirect test techniques in the emerging field of mmW built-in test.

Estimation of analog/RF parametric test metrics. Analog/RF built-in test (BIT) techniques are essential for reducing the very high costs of specification-based tests and for high-safety applications. The adoption of a BIT technique needs to be decided at the design stage, and this can be facilitated by estimating the test quality in terms of errors such as Test Escapes (TE) and Yield Loss (YL). Test quality estimation at the design stage has been traditionally very difficult for analog/RF circuits due to the lack of fault models that properly cover parametric faulty behavior. The RMS group has developed several statistical modeling techniques for the estimation of these metrics with part-per-million (ppm) precision without the need to consider parametric fault models. The most recent work has considered a fast statistical simulation exploiting machine-learning techniques, providing the data required for using rigorous Extreme Value Theory (EVT) models for test metrics estimation. This modeling technique has demonstrated ppm precision for the evaluation of a RF LNA BIT technique using a large date set of 1 million simulated circuits [RI20].

Machine learning based image quality assessment. We proposed a set of new objective methods for Image Quality Assessment (IQA) based on machine learning. In order to cover the variety of applications for which knowledge of image quality is required, we have proposed two classes of objective perception quality assessment methods depending on whether or not a reference image is available. Objective image quality is computed by pooling several image features extracted from different concepts: the natural scene statistic in spatial domain, the gradient magnitude, the Laplacian of Gaussian, as well as the spectral and spatial entropies. The extracted features are used as the entries of regression machine learning techniques, to construct the models that can be used to estimate the quality of an image. The experimental results demonstrate that the proposed models produce the best image quality prediction, compared to the other state-of-art objective no-reference image quality assessment models. We proposed an implementation of the proposed models on an FPGA platform. The implementation has been tested using Xilinx Virtex 7 FPGA board, implemented with C/C++ code on Xilinx Vivado HLS [CI45 - VTS'2019].

Highlights

- Silicon demonstration of the indirect test of mmW circuits, with two invited talks in this domain (SMACD'19).
- Demonstration of new machine-learning based algorithms and techniques for image quality enhancement for video and CMOS imager applications.
- New research project in collaboration with STMicroelectronics on embedded integrated jitter measurement and analog test signal generation, in the frame of the Nano2022 program.

Indicators

Scientific production	2019
International journals	4
International conferences	11
Books & Edited Books	1
National conferences	2
Other communications	1
PhD thesis	3

Scientific recognition	2019
Invited conferences	3
Conference/workshop Committees	12
Journal Edition Committees	2

Contracts 2019		
ANR	1	Falcon (2017-2019)
ANRT	3	STMicroelectronics
Collectivités territoriales	1	Messi (2019-2022)
EPST	2	Conception analogique (2019-2020) / PICS – Indie TEST (2017-2019)
EUREKA	1	Hades (2017-2020)
Industrie	1	Pyxcad 2019 (2019)

System Level Synthesis (SLS)

Permanent Personnel
Liliana ANDRADE (MCFCN UGA, section 27)
Olivier MULLER (MCFCN Grenoble INP, section 27)
Frédéric PETROT[(1)] (PREX Grenoble INP, section 27)
Laurence PIERRE (PR1 UGA, section 27)
Frédéric ROUSSEAU (PR1 UGA, section 27)

(1) Team leader and TIMA vice-director

Temporary personnel		
PhD Students	9	Thomas BAUMELA Louis BONICEL Jean BRUANT Maxime CHRIST Georgios CHRISTODOULIS Breytner Joseph FERNANDEZ MESA Bruno FERRES Giulio MILICI Arthur VIANES
Postdocs, engineers, expert collaborators	3	Engineers : Enzo BRIGNON Arthur VIANES Robin STIEGLITZ
Trainees	8	Matheus ALCÂNTARA SOUZA Nadia BENMOUSSA Enzo BRIGNON Amaury BUTAUX Gabriel JOB ANTUNES GRABHER Loic JOVANOVIC Marius LEBLANC Shuo ZHANG
Visitors	1	Manuel SELVA

Research Activities

The SLS team focuses on (a) hardware/software architectures, (b) specification, modeling, simulation and verification of embedded systems on chip and (c) reconfigurable and prototyping for cloud and ad-hoc digital circuits. The work of the team is included in the Laboratory themes “Hardware/software codesign” and “Simulation and verification of systems” described below.

Hardware/Software Codesign

Although the integration techniques have evolved drastically in the last decade, the definition of the frontier between peripheral devices and the kernel of the operating system, structuring how input/output operations occur at runtime, has remained mostly unchanged since the very first days of computers, even though the number of IPs and IPs in SoCs have risen tremendously, has had the number of registers per IP. We have worked on two paths around this topic. The first one deals with generating drivers from abstract descriptions. In practice, it appears to be somewhat contrived, and makes the handling of timing constraints cumbersome and hardly independent of the host OS. So we decided to try a second approach which consists of proposing a generic interface to devices, using channels instead of registers, taking inspiration from USB and virtualization strategies. This strategy has the benefit of partitioning the driver in a front-end, class and operating system dependent, but thus very limited in number, and a backend that is the responsibility of the device maker. We did a first experiment focusing on FPGA IPs, as they are particularly sensitive to version changes. We plan to apply this approach also to hard IPs, taking benefit from the fact that most IPs embed a processor or micro-controller of some sort that can run the backend part of the driver.

Providing high-performance synchronization mechanisms is a key issue to leverage hardware parallelism offered by MPSoCs. We studied the synchronization barrier mechanism and the impact of hardware contention for shared memory clustered MPSoC. Based on the implementation of the TSAR platform on the Veloce2 Quattro emulator, we have designed a non-intrusive approach to observe certain internal signals. We implemented a spy module in the platform to extract at runtime, by this side channel, useful signals like processors program counters and registers. Thanks to that, we have identified hardware modules restrictions and Linux kernel sub-optimal services both in active and passive wait processes. We show how the introduction of delays in the thread awakening process improves the overall synchronization mechanism. We have provided a combined HW/SW optimization. For the passive wait, our proposal provides a 60 % gain for 64 threads running on a 64-core architecture, and about 85 % gain for active wait on 16 and 32-core architecture.

Another work concerns hardware support for synchronization locks. We have confirmed a fundamental hypothesis for the optimization of the lock mechanism: although during the run time a lock may be used by various cores belonging to different clusters, it is often reused by the last core which has released it. Based on this observation, we propose an innovative decentralized solution to manage dynamic re-homing of locks in memory close to the last access-granted core, thus reducing overall access latency and network traffic in case of reuse of the lock by the same cluster.

Field-Programmable Gate Arrays (FPGAs) have been gaining popularity as hardware accelerators in heterogeneous architectures thanks to their high performance and low energy consumption. This argument has been supported by the recent integration of FPGA devices in cloud services and data centers. The potential offered by the reconfigurable architectures can still be optimized by treating FPGAs as virtualizable resources and offering them multitasking capability. The idea to preempt a hardware task on an FPGA with the objective of context switching it has been in research for many years. We nevertheless proposed a new strategy based on flow control analysis to extract the context of a running task from the FPGA to provide the possibility of its resumption at a later time. This strategy minimizes the context size and has the great interest of being applicable to IP generated using high-level synthesis.

Heterogeneity in High Performance Computing HPC nodes appears as a promising solution to improve the execution of a wide range of scientific applications, regarding both performance and energy consumption. Unlike CPUs and GPUs, FPGAs can be configured to fit the application needs, making them an appealing target to extend traditional heterogeneous HPC architectures. However, exploiting them requires an in-depth knowledge of low-level hardware and high expertise on vendor-provided tools, which should not be the primary concern of HPC application programmers. We proposed a framework, which requires the minimum knowledge of the underlying architecture, as well as fewer changes to the existing code. To fulfill these requirements, we extend the StarPU task programming library that initially targets heterogeneous architectures to also support FPGA.

Embedded vision systems are typical of high performance and energy efficiency requirement. As circuit integration is now extremely high, allowing to use hundreds to thousands hardware units in a single die, video stream data movement and parallelisation schemes are the higher level enablers. We focused on a methodology to speed up the design space exploration by rapidly estimating the performance of video analytics application on the STx-ASMP multiprocessor system. This led to tools: Parana rapidly estimates the performance of an application through an analytical approach taking as input application-independent metrics of the platform and some timings of the sequential version of the application. The estimates accuracy are below 5% of a real execution. From the same characterization data, the Tilana tool computes the optimal tile size to parallelize an image processing algorithm.

Artificial intelligence is a very hot topic, but digital hardware acceleration mainly focuses on the use of DSP and ad-hoc MAC acceleration. We have worked on the implementation of fully “unrolled” convolutional networks on FPGA using ternary weights and activations. Thanks to the high amount of resources available in modern FPGA, we have designed and implemented a versatile high-throughput accelerator with high accuracy and low power consumption.

On the general purpose computing side, we have worked on new protocols for ensuring cache coherency in multicore systems. Our main concern is the growing size of the meta-data as a function of the number of cores. A way to limit this is to use multicast, but it is hard to implement on NoCs, or broadcast, but this is highly inefficient in term of throughput and latency. A first approach we worked on consists of introducing virtualization support in NoC so that several virtual NoCs could share a single HW NoC at low HW cost. We were able to demonstrate broadcasting on a subpart of the NoC at lower cost than multicasting. A second approach is to represent the sharing set more efficiently. We propose the use of a rectangular shape to cover most of the sharers, and of a list allocated in a shared heap for the outliers. Using this approach leads to several interesting problems, such as how to find the best covering rectangle, how to implement efficiently the rectangle covering algorithm in hardware, what should be the size of the list and heap, etc.

Simulation and Verification of Systems

The discrepancy between computing and storage motivates the design of memory hierarchies trying to prefetch the data ahead of the computing unit. Both static and dynamic strategies have been explored in the context of image processing. During this period, we focused on dynamic strategies to guess the next data reference through statistical characterization of the past references. The proposed algorithm guesses the next references by online computing of the Kolmogorov-Smirnov hypothesis test and updates some internal parameter thanks to a metric of the prediction quality.

High-level performance estimation of software codes requires abstract models to represent processors behaviors, in terms of instruction throughput and execution latency. To that aim, we have worked on annotating the intermediate representation of a compiler with target specific information while generating code for the host simulation machine. We have discovered that some constructs, loops to be precise, are particularly hard to annotate when aggressive optimization such as loop unrolling, loop folding, loop pipelining are used. Indeed, the mapping between the control flow graph of the target binary and the one of the host binary differ, and therefore the annotation are not accounted for correctly. We worked on host control flow graph reorganization to take into account the machine level optimization and reached a high-level of accuracy at high speed for timing estimation of sequential programs.

Accelerating hardware/software simulation is an historical topic of the group. During the period, we have on the one hand worked on “native simulation” taking into account non-functional properties, applied to many-core platforms and VLIW processors. Even though we obtained interesting and publishable results, we plan not to go further in that direction. Indeed, modeling constraints make native simulation usable only for bare metal software or require very heavy paravirtualization developments. On the other hand, we kept on working on dynamic binary translation, with first a prototype proving that it can be used to execute VLIW codes, and second a strategy which bypasses the logical to physical address translation, that accounts for 10% to 60% of simulation times, depending on the benchmarks. We have mainly focused on speed of simulation, but performance estimation is also important, and to that aim we have modeled micro-architectural properties, such as caches or branch predictors, by annotating generated code. Overall, accuracy in the range 20%/50% can be achieved, but at a high overhead in terms of simulation speed.

Given its importance in modern design, we started an activity aiming at the verification of intrinsic properties of C or C++ embedded software. To that goal, we advocate the use of runtime Assertion-Based Verification (ABV) which aims at checking whether applications obey properties, usually expressed as *formal temporal formulas* that capture the design intent. They can be used for debugging purposes; they can also be useful for the online monitoring of fault-tolerance, security, or performance properties. These properties are automatically transformed into *assertion checkers, triggered upon specific events during execution*. These events can be updatings and readings of program variables (both global and local), and function calls or returns. A specific binary instrumentation mechanism has been defined to implement such an event-driven activation of temporal assertion checkers [CI54].

Highlights

- …
-

Indicators

Scientific production	2019
International journals	2
International conferences	6
National conferences	2
PhD thesis	1

Scientific recognition	2019
Conference/workshop Committees	8

Contracts 2019		
ANR	1	Rakes (2019-2023)
ANRT	4	Kalray (1) / OVH (1) / Schneider Electric (1) / STMicroelectronics (1)
CEC National	1	AI4DI (2019-2022)
EPST	2	Arte (2019-2020) / Digital Hardware AI Architectures (2019-2023)

Academic and research members

Liliana ANDRADE

Position
Associate Professor at Université Grenoble Alpes
POLYTECH school

Current responsibilities
Researcher in SLS team
(System Level Synthesis)

Lorena ANGHEL

Position
Professor at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities
Co-leader of AMfoRS team
(Architectures and Methods for Resilient Systems)

Manuel BARRAGAN

Position
Researcher at CNRS
(French National Center for Scientific Research)

Current responsibilities
Researcher in RMS team
(Reliable Mixed-signal Systems)

Skandar BASROUR

Position
Professor at Université Grenoble Alpes
POLYTECH school *(Electrical Engineering Department - 3I)*

Current responsibilities
Deputy Director of TIMA Lab. since 01/2015
Co-leader of CDSI team
(Circuits, Devices and System Integration)

Mounir BENABDENBI

Position
Associate Professor at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities
Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)

Agnès BONVILAIN

Position
Associate Professor at Université Grenoble Alpes
POLYTECH school

Current responsibilities
Researcher in CDSI team
(Circuits, Devices and System Integration)

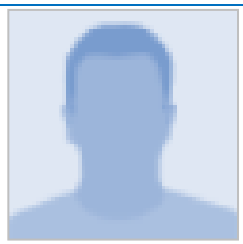
Dominique BORRIONE

Position

Professor Emerita at Université Grenoble Alpes until 31/08/2019

Current responsibilities

Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)



Mouhamad CHEHAITLY

Position

Teaching assistant ATER at Université Grenoble Alpes until 31/08/2019

Current responsibilities

Researcher in RMS team
(Reliable Mixed-signal Systems)

Giorgio DI NATALE

Position

Research Director at CNRS
(French National Center for Scientific Research)

Current responsibilities

Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)

Sylvain ENGELS

Position

Associate Professor PAST at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities

Researcher in CDSI team
(Circuits, Devices and System Integration)

Laurent FESQUET

Position

Associate Professor at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities

Co-leader of CDSI team
(Circuits, Devices and System Integration)

Régis LEVEUGLE

Position

Professor at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities

Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)

Paolo MAISTRI

Position

Researcher at CNRS
(French National Center for Scientific Research)

Current responsibilities

Co-leader of AMfoRS team
(Architectures and Methods for Resilient Systems)

Stéphane MANCINI

Position

Associate Professor at GRENOBLE INP
(Grenoble Institute of Technology)
ENSIMAG school *(Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)*

Current responsibilities

Researcher in CDSI team
(System Level Synthesis)

Salvador MIR

Position

Research Director at CNRS
(French National Center for Scientific Research)

Current responsibilities

Director of TIMA Lab. since 01/2015
Researcher in RMS team
(Reliable Mixed-signal Systems)

Katell MORIN-ALLORY

Position

Associate Professor at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities

Researcher in CDSI team
(Architectures and Methods for Resilient Systems)

Olivier MULLER

Position

Associate Professor at GRENOBLE INP
(Grenoble Institute of Technology)
ENSIMAG school *(Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)*

Current responsibilities

Researcher in SLS team
(System Level Synthesis)

Mihail NICOLAIDIS

Position

Research Director at CNRS
(French National Center for Scientific Research)

Current responsibilities

Researcher in RIS team
(Robust Integrated Systems)

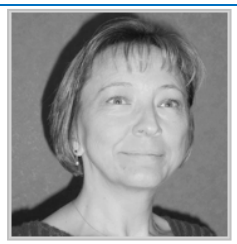
Frédéric PÉTROT

Position

Professor at GRENOBLE INP
(Grenoble Institute of Technology)
ENSIMAG school *(Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)*

Current responsibilities

Deputy Director of TIMA Lab. since 01/2015
Leader of SLS team
(System Level Synthesis)



Laurence PIERRE

Position

Professor at Université Grenoble Alpes
IM2AG school *(Informatique, Mathématiques et Mathématiques Appliquées)*

Current responsibilities

Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)

Michele PORTOLAN

Position

Associate Professor at GRENOBLE INP
(Grenoble Institute of Technology)
PHELMA school *(Physique-Electronique-Matériaux)*

Current responsibilities

Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)

Rodrigo POSSAMAI BASTOS

Position

Associate Professor at Université Grenoble Alpes
IM2AG school *(Informatique, Mathématiques et Mathématiques Appliquées)*

Current responsibilities

Researcher in CDSI team
(Circuits, Devices and System Integration)

Frédéric ROUSSEAU

Position

Professor at Université Grenoble Alpes
POLYTECH school

Current responsibilities

Researcher in SLS team
(System Level Synthesis)

Libor RUFER

Position

Researcher at Université Grenoble Alpes
POLYTECH school

Current responsibilities

Researcher in CDSI team
(Circuits, Devices and System Integration)
Acoustic and ultrasonic micro-devices
Energy harvesting

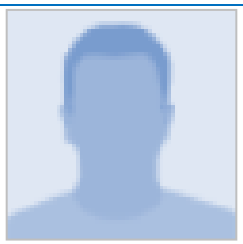
Emmanuel SIMEU

Position

Associate Professor at Université Grenoble Alpes
POLYTECH school

Current responsibilities

Leader of RMS team
(Reliable Mixed-signal Systems)



Elena-Ioana VATAJELU

Position

Researcher at CNRS
(French National Center for Scientific Research)

Current responsibilities

Researcher in AMfoRS team
(Architectures and Methods for Resilient Systems)

Raoul VELAZCO

Position

Research Director at CNRS
(French National Center for Scientific Research)

Current responsibilities

Leader of RIS team
(Robust Integrated Systems)

Nacer-Eddine ZERGAINOH

Position

Associate Professor at Université Grenoble Alpes
POLYTECH school

Current responsibilities

Researcher in RIS team
(Robust Integrated Systems)

Staff members

Laurence BEN TITO

Position
Engineer assistant at TIMA Lab. since 03/2010
Employer: GRENOBLE INP (Grenoble Institute of Technology)

Current responsibilities
Executive Secretary

Frédéric CHEVROT

Position
Engineer assistant at TIMA Lab. since 03/2003
Employer: GRENOBLE INP (Grenoble Institute of Technology)

Current responsibilities
Computer Service Manager

Alice DE BIGNICOURT

Position
Engineer at TIMA Lab. since 05/2011
Employer: CNRS (French National Center for Scientific Research)

Current responsibilities
Software development engineer – Webmaster

Mamadou DIALLO

Position
Engineer at TIMA Lab. since 12/2014
Employer: CNRS (French National Center for Scientific Research)

Current responsibilities
Integrated Circuits Designer

Anne-Laure FOURNERET-ITIE

Position
Engineer at TIMA Lab. since 09/2003
Employer: ADR (Research Development Association)

Current responsibilities
Administrative Service Manager
Personnel officer, special event manager

Nicolas GARNIER

Position
Engineer at TIMA Lab. since 02/2006
Employer: CNRS (French National Center for Scientific Research)

Current responsibilities
System Engineer

Aurore GAYRAUD

Position

Engineer assistant at TIMA Lab. since 03/2013
Employer: CNRS (French National Center for Scientific Research)

Current responsibilities

Research contracts justification (until 03/2016)
Teams finance administrator (since 12/2016)

Mathilde GARÇON (JOUANNON)

Position

Engineer assistant at TIMA Lab. since 12/2018
Employer: UGA (Université Grenoble Alpes)

Current responsibilities

Financial Service Deputy Manager
Accounting of budgets, contracts

Ahmed KHALID

Position

Technical assistant at TIMA Lab. since 01/2007
Employer: GRENOBLE INP (Grenoble Institute of Technology)

Current responsibilities

System technician

Fabrice PANCHER

Position

Research engineer at TIMA Lab. since 06/2010
Employer: CNRS (French National Center for Scientific Research)

Current responsibilities

Development Service Manager
Software developments for TIMA's research groups

Youness RAJAB

Position

Technician at TIMA Lab. since 09/2008
Employer: CNRS (French National Center for Scientific Research)

Current responsibilities

Teams finance administrator
Common expenses administrator

Marie-Christine SALIZZONI

Position

Engineer at TIMA Lab. since 01/2000
Employer: ADR (Research Development Association)

Current responsibilities

Financial Service Manager
Accounting of budgets, contracts

Ph. D. candidates

1. AIT SAID Noureddine
Title of thesis: **Self adaptive precision in SoCs: design and verification techniques**
Expected date of defense: **2021**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

2. AKRARAI Mohamed
Title of thesis: **Smart Event-Based Image Sensor for wake-up applications**
Expected date of defense: **2022**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

3. AQUINO GUAZZELLI Ricardo
Title of thesis: **Testing of Asynchronous Circuits for Security Systems in Advanced Technologies**
Expected date of defense: **2020**
Previous degrees: Engineer – Pontifícia Universidade Católica do Rio Grande do Sul – Porto Alegre, Brazil (2017)

4. AUBERT Xavier
Title of thesis: **Adaptive low-power techniques for Systems-on-a-chip based on Fully Depleted Silicon-On-Insulator technology**
Expected date of defense: **thesis stopped (June 2019)**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2017)

5. BAUMELA Thomas
Title of thesis: **Externalisation of device drivers from embedded processors to devices**
Expected date of defense: **2020**
Previous degrees: Engineer – Université Grenoble Alpes, France (2016)

6. BELOT Jérémy
Title of thesis: **Towards robust, low power and adjustable accuracy Bayesian computers**
Expected date of defense: **2022**
Previous degrees: Engineer Grenoble INP – Phelma, France (2018)

7. BERTRAND François
Title of thesis: **Design flow and formal models for desynchronization of synchronous circuits**
Completed on: **July 2, 2019**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2015)

8. BONICEL Louis
Title of thesis: **Study of an architectural model for code generation taking into account the real time constraints of an embedded system in the electrical measure and protection domain**
Expected date of defense: **2022**
Previous degrees: Engineer – Polytech Montpellier, France (2017)

9. BRUANT Jean
Title of thesis: **Abstracting FPGA development flow as a modern software development flow**
Expected date of defense: **2021**
Previous degrees: Engineer - Télécom Bretagne, France (2018)

10. CHRIST Maxime
Title of thesis: **Learning in very low precision**
Expected date of defense: **2022**
Previous degrees: Engineer - INSA Lyon, France (2017)

11. CHRISTODOULIS Georgios
Title of thesis: **Adaptation of a HPC runtime system to FPGA**
Completed on: **December 5, 2019**
Previous degrees: Engineer diploma from NTUA, Greece (2015)

12. CILICI Florent
Title of thesis: **Development of Built-In Self-Test solutions for RF/mmW integrated circuits**
Completed on: **December 17, 2019**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2016)

13. CINÇON Valérian
Title of thesis: **Ultra low power integration of neuro-morphic systems on FD-SOI**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

14. DA PENHA COELHO Alexandre
Title of thesis: **Fault Tolerance and Reliability for Partially Connected 3D Networks-on-Chip**
Completed on: **October 25, 2019**
Previous degrees: Engineer (2010)

15. DECOUDU Yoan
Title of thesis: **An asynchronous Design Flow for Event-Based Processing in FDSOI Technologies**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

16. DELAHAYE Geoffrey
Title of thesis: **Protection against Electrostatic Discharge (ESD) in a harsh environment advanced silicon-on-insulator technology (FD-SOI)**
Expected date of defense: **thesis stopped (January 2020)**
Previous degrees: Engineer – ISEN Lille-Brest-Toulon, France (2018)

17. EL HADBI Assia
Title of thesis: **Time-to-digital Conversion based on a Self-Timed Ring Oscillator**
Completed on: **November 20, 2019**
Previous degrees: Engineer - Telecommunication Engineering, Morocco (2011)

18. FERNANDEZ BRILLET Lucas
Title of thesis: **3D integrated circuit implementation of convolutional neural networks for embedded vision**
Expected date of defense: **2020**
Previous degrees: Engineer – ENSEIRB / MATMECA - Bordeaux INP, France (2016)

19. FERNANDEZ-MESA Breytner Joseph
Title of thesis: **Exploration of Direct Synchronization Approaches for a High-Level and Unified Simulation of Discrete-Event/Continuous-Time Systems**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidad de Los Andes – Mérida, Venezuela (2017)

20. FERREIRA DE PAIVA LEITE Thiago
Title of thesis: **FD-SOI technology opportunities for more energy efficient asynchronous circuits**
Completed on: **January 21, 2019**
Previous degrees: Engineer - Universidade Federal de Campina Grande - Paraiba, Brazil (2015)

21. FERRES Bruno
Title of thesis: **Task migration software/hardware in an heterogeneous and reconfigurable system**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP - Ensimag, France (2018)

22. FRISCH Raphael
Title of thesis: **Stochastic machines dedicated to Bayesian inference for source localization and separation**
Completed on: **November 14, 2019**
Previous degrees: Engineer – Université Grenoble Alpes - 2R MOSIG, France (2016)

23. GARAY TRINDADE Matheus
Title of thesis: **Optimization and Qualification of Hardware Machine-Learning Systems under Radiation-Induced Effects**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidade Federal de Santa Maria, Rio Grande do Sul, Brazil (2017)

24. GERMAIN Sophie
Title of thesis: **Electromagnetic spectrum control of asynchronous digital circuits**
Completed on: **November 25, 2019**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2016)

25. GIMENEZ Grégoire
Title of thesis: **Studies and design of secure and low-power chips for IoT**
Expected date of defense: **2020**
Previous degrees: Engineer – Grenoble INP, France (2009)

26. HACHEMI Mohammed-Bilal
Title of thesis: **Study of HZO films for MEMS applications**
Expected date of defense: **2022**
Previous degrees: Engineer - ECole Polytechnique de Constantine – Algeria (2017)

27. IGA Rodrigo
Title of thesis: **EM compliant Low-Energy Sugnal Demodulation for NFC applications**
Expected date of defense: **2021**
Previous degrees: Engineer – Université Grenoble Alpes, France (2010)

28. INGLESE Pietro
Title of thesis: **Exploration of security threats in In-Memory Computing Paradigms**
Expected date of defense: **2022**
Previous degrees: Engineer – Politecnico di Torino, Italy (2019)

29. KALSING Arthur
Title of thesis: **Power-Intent Management During RTL Optimizations**
Completed on: **July 11, 2019**
Previous degrees: Engineer - Grenoble INP - Ensimag, France (2014)

30. KRIEKOUKI Ioanna
Title of thesis: **Fabrication and characterization of spin-based quantum bits with embedded control in 28 nm UTBB FD-SOI technology and at very low temperatures**
Expected date of defense: **2022**
Previous degrees: Engineer – Université Grenoble Alpes, France (2017)

31. LAUWERS Thomas
Title of thesis: **Resonant sensors for the photoacoustic detection of gaz**
Expected date of defense: **2020**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2016)

32. LECLAIRE Nicolas
Title of thesis: **Hardware and software architectures for deep learning acceleration on embedded multi-processor**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2017)

33. MARGALEF ROVIRA Marc
Title of thesis: **Design of passive and active circuits in BiCMOS 55nm technology for mm-wave frequencies**
Expected date of defense: **2020**
Previous degrees: Engineer – Université Grenoble Alpes, France (2017)

34. MELIS Tommaso
Title of thesis: **Diagnosis tool developement for failure analysis of analog an mixed signal devices**
Expected date of defense: **2022**
Previous degrees: Engineer - Università degli Studi di Cagliari, Italy (2018)

35. MILICI Giulio
Title of thesis: **Strategy of crosspoint non-volatile memory integration in cache hierarchy of a multicore architecture**
Expected date of defense: **2021**
Previous degrees: Engineer – Politecnico di Torino, Italy (2018)

36. POPESCU Andrei
Title of thesis: **On control approaches for estimation purposes - Application to tunneling current and magnetic levitation processes**
Completed on: **November 25, 2019**
Previous degrees: Engineer - Polytechnique Bucarest, Romania (2016)

37. REYNAUD Vincent
Title of thesis: **Secured access to IEEE 1687 test resources and lightweight crypto-processors in the IoT context**
Expected date of defense: **2020**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2017)

38. ROLLOFF Otto Aureliano
Title of thesis: **Distributed Body-Bias Micro-Generators for an activity-driven power management in FD-SOI Technologies**
Completed on: **December 3, 2019**
Previous degrees: Engineer – Télécom Bretagne, France (2014)

39. ROUX Julie
Title of thesis: **Safety Evaluation of Aircraft Systems using Virtual Platforms**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2017)

40. SENTHAMARAI KANNAN Kalpana
Title of thesis: **Performance and Safety/Security Management in automotive and IoT applications**
Expected date of defense: **2020**
Previous degrees: Engineer – Pondichery University, India (2013)

41. SHAH Riddhi
Title of thesis: **HiRel Product Demonstration by Dynamic Wearout Management**
Expected date of defense: **2020**
Previous degrees: Engineer – Nirma University, India (2016)

42. SILVEIRA FEITOZA Renato
Title of thesis: **Desigh-for-test strategies for built-in static test of high-performance SAR ADCs**
Expected date of defense: **2020**
Previous degrees: Engineer – Pontifícia Universidade Católica do Rio de Janeiro, Brazil (2017)

43. TCHUANI TCHAKONTE Diane
Title of thesis: **Minimization of energy consumption of sensor networks in target coverage applications**
Completed on: **July 19, 2019**
Previous degrees: Engineer (2011) (Cameroon)

44. TROUSSIER Chloé
Title of thesis: **Study of ESD/CDM stresses phenomena from elementary charged devices to package discharge: failure mechanism, protection strategy and predictive tools**
Expected date of defense: **2021**
Previous degrees: Engineer – IMT Atlantique Bretagne Pays de Loire, France (2018)

45. VIANES Arthur
Title of thesis: **Integration of a Manycore Accelerator in a High-Performance Processor**
Expected date of defense: **2022**
Previous degrees: Engineer Polytech Grenoble, France (2018)

Other members of TIMA

Post-doctoral position – Engineers – Experts – Teaching Assistants

Name	Forename	Position	Team
1. ARDILES SARAVIA	David César	Postdoc	RIS
2. ARDILES SARAVIA	David César	Expert	RIS
3. BEN AZIZA	Sassi	Postdoc	RMS
4. BRIGNON	Enzo	Contracted Engineer	SLS
5. CHEHAITLY	Mouhamad	Teaching assistant	RMS
6. DEFOORT	Martial	Expert	CDSI
7. MALLOUG	Hani	Postdoc	RMS
8. MARGOTAT	Nils	Contracted Engineer	CDSI
9. PAPAVRAMIDOU	Panagiota	Expert	RIS
10. PROTO	Antonino	Postdoc	CDSI
11. RICART	Thibaut	Expert	CDSI
12. SKAF	Ali	Expert	CDSI
13. STIEGLITZ	Robin	Contracted Engineer	SLS
14. TAKAM TCHENDJOU	Ghislain	Teaching assistant	RMS
15. TAKAM TCHENDJOU	Ghislain	Postdoc	RMS
16. VIANES	Arthur	Contracted Engineer	SLS

Visitors

Name	Forename	Country	Duration
1. COPELLO OST	Luciano	BRAZIL	1 month 1 day
2. FRAGA GARIBOTTI	Rafael	BRAZIL	5 months 29 days
3. GUSMAO DE LIMA KASTENSMIDT	Fernanda	BRAZIL	1 month 2 days
4. KAROUI	Said	ALGERIA	7 days
5. LEGER	Gildas	FRANCE	9 days
6. LOPEZ ANGULO	Antonio Jose	SPAIN	14 days
7. NGUYEN	Hoang Nam	VIET NAM	23 days
8. RAFIC	Kattan	LEBANON	10 days
9. RUFER	Libor	CZECH REP.	11 months 29 days
10. SELVA	Manuel	FRANCE	1 year 7 months
11. SILVA CARDENAS	Carlos	PERU	4 days

Trainees

Name	Forename	Country	Duration	Team
1. AKRMI	Oubaid	TUNISIA	2 months 19 days	CDSI
2. ALASATRI	Suresh	INDIA	4 months 4 days	CDSI
3. ALCÂNTARA SOUZA	Matheus	BRAZIL	5 months	SLS
4. BAAZAOUI	Ahmed	TUNISIA	4 months 27 days	CDSI
5. BACHIR-ELEZAAR	Oualid	FRANCE	4 months 20 days	CDSI
6. BAWAB	Ali	LEBANON	4 months 22 days	AMfoRS
7. BENMOUSSA	Nadia	ALGERIA	4 months 6 days	SLS
8. BENOMAR	Mohamed	SPAIN	4 months 15 days	RIS
9. BERLITZ	Carlos Augusto	BRAZIL	3 months 15 days	CDSI
10. BOUGHZALA	Oussama	TUNISIA	3 months 21 days	CDSI
11. BRIGNON	Enzo	FRANCE	10 months	SLS
12. BRITTON OROZCO	Giovani Crasby	COLOMBIA	4 months 21 days	RMS
13. BUTAUX	Amaury	FRANCE	2 months 19 days	SLS
14. CHAFIK	Sohaib	MOROCCO	4 months 29 days	AMfoRS
15. EL FIDALI	Ouissal	MOROCCO	3 months 16 days	TIMA
16. EL KHAMSI	Ismail	MOROCCO	2 months 19 days	CDSI
17. EZZADEEN	Mona	FRANCE	5 months 1 day	AMfoRS
18. FICI	Alessandro	ITALY	4 months 15 days	AMfoRS
19. GHANEM	Badri	ALGERIA	4 months 17 days	CDSI
20. GIL	Enric	SPAIN	4 months 15 days	RIS
21. HAI	Joycelyn	MALAYSIA	3 months 17 days	CDSI
22. HOLANDA BATISTA	Madson Ivens	BRAZIL	3 months 13 days	CDSI
23. IGUEBLALENE	Shana	FRANCE	4 days	TIMA
24. JANOSCOVA	Bara	CZECH REP.	4 months 27 days	CDSI
25. JOB ANTUNES GRABHER	Gabriel	BRAZIL	2 months 18 days	SLS
26. JOVANOVIC	Loic	FRANCE	1 month 28 days	SLS
27. JRAD	Moatez	TUNISIA	2 months 27 days	TIMA
28. LAKHAL	Nejmeddine	TUNISIA	4 months 27 days	CDSI
29. LEBLANC	Marius	FRANCE	2 months 19 days	SLS
30. LIM	Olivier	France	5 months 6 days	CDSI
31. MAAMER	Bilel	TUNISIA	4 months	CDSI
32. MALDANER	Liege	BRAZIL	3 months 13 days	CDSI
33. MATIASSO PORTELLA	Kenedy	BRAZIL	2 months 12 days	CDSI
34. MESNAGER	Victor	FRANCE	3 months 15 days	AMfoRS
35. MIGHRI	Imen	TUNISIA	9 months 22 days	RMS
36. MONGUILO MANTOVANI	Javier Alejandro	ITALY	3 months 20 days	RMS
37. MOUHOUB	Tarik	ALGERIA	2 months 19 days	CDSI
38. NGUYEN	Dinh-Duy-Kha	VIET NAM	2 months 19 days	CDSI
39. POLLIEN	Baptiste	FRANCE	3 months 23 days	CDSI
40. PRANDO DAVANZO	Renan	BRAZIL	2 months 20 days	TIMA
41. QURESHI	Muhammad Talha	PAKISTAN	4 months 22 days	AMfoRS
42. RAMZI	Jinane	MOROCCO	3 months 16 days	TIMA
43. SANTANDER	Lucas	FRANCE	2 months 6 days	AMfoRS
44. YAKHLEF	Mohamed	MOROCCO	3 months 21 days	CDSI
45. ZHANG	Shuo	CHINA	2 months 20 days	SLS

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2019 (13).

ANR

ANR / EMINENT project (Oct 01, 2019 - Apr 30, 2023)

EMINENT est axé sur les domaines de recherche suivants : (i) technologies émergentes de mémoire (résistives et dispositifs spintroniques) utilisées dans un contexte non-Von Neumann, (ii) implémentations matérielles de réseaux de neurones bio-inspirés (réseaux de neurones impulsionnels), (iii) fiabilité du matériel (robustesse, vieillissement et test) et conception en vue de la fiabilité. Le projet EMINENT a pour but de fournir une architecture de réseau de neurones impulsionnels reposant sur des mémoires émergentes. Cet objectif sera atteint à travers la réalisation des tâches suivantes : (i) étude des principales menaces visant la fiabilité des architectures SNN, (ii) estimation du vieillissement des architectures SNN, (iii) définition de stratégies de test post-fabrication et solutions de conception en vue du test, (iv) définition de stratégies d'amélioration de la fiabilité de l'architecture.

ANR / RAKES project (Jun 01, 2019 - May 31, 2023)

Partners: - INRIA Centre Rennes - Bretagne Atlantique - CNRS : Délégation Régionale Bretagne et Pays de la Loire

ANR / FALCON project (Sep 01, 2017 - Mar 30, 2019)

Réseaux de caméras ultrarapides par assemblage nanotechnologique

Partners: Université de Strasbourg, CEA Laboratoire Electronique Technologies Information, Dolphin Integration

La vidéo rapide est une activité en plein essor tout en étant un terrain d'application idéal des imageurs à technologie CMOS. Elle trouve des applications dans l'analyse des mouvements, la balistique, les explosions, la biomécanique, les crashs test, la dynamique des fluides, les chocs et les vibrations etc. La vidéo rapide conventionnelle est actuellement pilotée par l'industriel avec des sociétés comme Photron, Redlake ou Drs Hadland qui produisent leurs propres capteurs. La meilleure caméra du marché offre 22000 images par seconde (ips) pour une résolution spatiale de 1280x800 pixels, c'est-à-dire un taux d'échantillonnage de 22 Giga pixel/s. Cette vitesse n'est pas restreinte par l'électronique du pixel, mais par celle des entrées sortie qui permettent d'extraire l'image du capteur. L'objectif du projet FALCON est de franchir cette barrière technologique en repoussant la vitesse d'acquisition de 3 ordres de grandeurs en proposant un capteur capable de prendre jusqu'à 100 millions d'ips en montant le taux d'échantillonnage à 10 Petabits/s. Pour y parvenir, l'approche classique d'extraction des images en continu doit être abandonnée pour s'affranchir du goulet d'étranglement des entrées/sorties au profit de l'approche de capteur d'image par rafale (BIS pour Burst Image Sensor). Puisqu'il n'est pas possible de sortir les images au fur et à mesure qu'elles sont prises, il suffit de les laisser sur le capteur. Ainsi, l'ensemble des BIS précédemment réalisés intègrent une mémoire analogique embarquée sur un capteur monolithique. Le pitch du pixel est généralement de l'ordre de 50 µm, la vitesse d'acquisition d'environ 10 Mega ips et la profondeur mémoire, c'est-à-dire le nombre d'images stockées, tourne aux alentours d'une centaine. Ce dernier nombre, principalement limité par l'espace occupé par la mémoire en relation avec le pitch du pixel, est bien insuffisant dans bon nombre d'applications et spécifiquement celles ou la durée de l'événement à mesurer est longue ou bien ou la synchronisation de l'événement et le déclenchement de la caméra est incertain. Cela peut conduire à une expérience manquée. Par ailleurs, les travaux n'évoquent que très peu le rapport signal à bruit (SNR) mais sa valeur diminue lorsque le temps de lecture augmente, c'est-à-dire lorsque le nombre d'images à lire grandit, car les courants de fuites dégradent l'information stockée dans une capacité. Cette contrainte joue également en défaveur d'une grande profondeur de mémoire et en pratique, le SNR ne dépasse pas les 45 dB. Le dispositif proposé dans le cadre du projet FALCON repose sur un concept en totale rupture avec les précédents BIS en mettant en œuvre les possibilités offertes par les technologies microélectroniques 3D émergentes. Une thèse démarrée en 2012 en collaboration entre ICube et le L3i du CEA Leti a permis de déterminer une nouvelle architecture qui tire parti de la structure 3D de manière optimale. Une approche numérique audacieuse permet d'augmenter les performances de ce type de capteur, et également d'y apporter de nouvelles fonctionnalités. La particularité de l'architecture réside dans son mode d'acquisition avec conversion analogique vers numérique a haute cadence et stockage des images sous format numérique qui améliore à la fois la qualité du signal et qui augmente d'un ordre de grandeur la profondeur mémoire. L'objectif final étant d'obtenir une caméra haute définition (1200x1200), fonctionnant à 10 Mega ips avec une mémoire de plus de 1000 images. Ce projet repousse les performances de chacun des sous éléments du système à l'état de l'art afin de proposer un capteur unique. Une méthodologie originale de conception conjointe architecture/partitionnement et électrothermique est également au cœur du projet. En effet, de nouvelles méthodes et de nouveaux outils sont nécessaires pour mener à bien la conception de tels systèmes intégrés hétérogènes.

ANRT

ANRT / CIFRE Xavier AUBERT (Nov 01, 2017 - Oct 30, 2021)
"Techniques adaptatives de réduction de la consommation des systèmes sur puce en technologie silicium sur isolant complètement déplété"
Partners: Dolphin Integration, Laboratoire TIMA

ANRT / CIFRE Arthur VIANNES project (May 01, 2019 - Apr 30, 2022)
Il s'agit du contrat CIFRE d'Arthur VIANNES dans le cadre de la thèse. : Intégration d'un accélérateur pluri-coeurs dans un processeur à hautes performances.

ANRT / CIFRE Louis BONICEL project (Mar 01, 2018 - Feb 28, 2021)
"Etude d'un modèle architectural pour la génération de code intégrant les contraintes d'un système temps réel embarqué dans le domaine de la mesure et la protection électrique"
Partners: Schneider Electric Industries SAS

ANRT / CIFRE Jean BRUANT project (Oct 01, 2018 - Jan 31, 2022)
Il s'agit du contrat d'accompagnement de la thèse de Jean Bruant intitulé « Abstraction du développement sur FPGA pour l'intégrer dans un flot de développement logiciel moderne »

ANRT / CIFRE François BERTRAND project (Apr 14, 2016 - Apr 13, 2019)
"Conception asynchrone robuste pour la très faible consommation dans les cartes à puces."
Partners: STARCHIP
"conception asynchrone robuste pour la très faible consommation dans les cartes à puces." L'avènement des cartes à puces sans contact sur le marché est en train de conduire à une révolution dans la conception de ces dernières. pour avoir des cartes à puces performantes en mode sans contact, il faudra être capable de consommer moins et de récupérer mieux l'énergie. L'étude vise deux angle d'approche. Le premier consiste en une approche asynchrone qui présente l'avantage de n'activer que les parties effectuant réellement un calcul. Le second angle d'attaque est d'abaisser la tension d'alimentation près du seuil ce qui permet de baisser considérablement la consommation. Le sujet de la thèse se concentrera sur le développement d'une méthode de conception de circuits asynchrones capables de fonctionner près du seuil.

ANRT / CIFRE Alexis Rodrigo IGA RADUE project (Sep 17, 2018 - Sep 16, 2021)
"Démodulation NFC Basse Consommation et Respectueuse de la Compatibilité Electromagnétique"
Partners: ST

ANRT / CIFRE Chloé TROUSSIER project (Nov 19, 2018 - Nov 18, 2021)
"Etude des phénomènes de décharge électrostatique (ESD/CDM) : du composant au circuit intégré"

ANRT / CIFRE Ioanna KRIEKOUKI project (Oct 25, 2018 - Oct 24, 2021)
"Fabrication et caractérisation de bits quantiques avec contrôle embarqué en technologie 28nm UTBB FD-SOI et au delà à température cryogénique"

ANRT / CIFRE Tommaso MELIS project (Nov 05, 2018 - Nov 04, 2021)
"Développement d'outils de diagnostic pour l'analyse des défaillances des circuits intégrés analogiques et mixtes"
Partners: ST Microelectronics Grenoble, TIMA / INP

ANRT / CIFRE Valérian CINCON project (Nov 05, 2018 - Nov 04, 2021)
"Etude et intégration de systèmes neuro-morphiques ultra basse consommation en technologie FD-SOI"

ANRT / CIFRE Lucas FERNANDEZ-BRILLET (Mar 13, 2017 - Mar 12, 2020)
"Architectures intégrrées 3D de réseaux de neurones CNN pour la vision embarquée"
Partners: STMicroélectronics (Grenoble 2) SAS
Architectures intégrrées 3D de réseaux de neurones CNN pour la vision embarquée

ANRT / CIFRE Riddhi J. SHAH project (May 11, 2017 - May 10, 2020)
"Etude et réalisation de démonstrateurs ayant une gestion dynamique du vieillissement pour les applications exigeant une haute fiabilité"
Partners: STMicroélectronics SAS
Etude et réalisation de démonstrateurs ayant une gestion dynamique du vieillissement pour les applications exigeant une haute fiabilité.

ANRT / CIFRE Sophie GERMAIN project (Nov 02, 2016 - Oct 31, 2019)
"EM spectrum control based on micropipeline circuits for NFC applications"
Partners: STMicroelectronics SA
EM spectrum control based on micropipeline circuits for NFC applications

ANRT / CIFRE Mohammed TMIMI project (Sep 25, 2017 - Sep 25, 2020)

"Nouvelle approche pour lien série en technologie FD-SOI 28nm CMOS avancée et au-delà"
Partners: ST Microelectronics, Laboratoire TIMA

ANRT / CIFRE Nicolas LECLAIRE project (Jan 02, 2018 - Jan 01, 2021)

"Architectures matérielles et logicielles pour l'accélération du "deep learning" sur multiprocesseur évolutif embarqué"
Partners: ST Microélectronics (Grenoble 2) SAS

CARNOT

CARNOT / EBIS project (May 01, 2019 - Dec 31, 2020)

Event Based Image Sensor
La consommation électrique des composants électroniques est, depuis quelques années, devenu un critère capital lors de la conception des systèmes intégrés électroniques (puces). Notre équipe de recherche (CDSI) à TIMA s'intéressent à la thématique de la faible et de l'ultra-faible consommation depuis de nombreuses années. Par ailleurs, elle possède aussi une expertise dans le domaine des capteurs d'images CMOS qui sont à l'heure actuelle des composants qui n'ont jamais réellement été pensés pour être peu gourmands en énergie. Cette double compétence nous a poussés à investiguer le développement de capteurs d'images CMOS peu énergivores. Afin de parvenir à un imageur peu consommant, nous avons développé un capteur doté d'un protocole de lecture événementiel (on ne lit pas en permanence la totalité de l'image) et d'un échantillonnage non uniforme de l'image. Cette approche originale présente un intérêt pour la faible consommation électrique mais aussi pour des applications tels que l'imagerie 3D, la vision dans le brouillard, l'image rapide et certains traitements de l'image comme la segmentation.

CEC

CEC / NANOxCOMP project (Dec 01, 2016 - Nov 30, 2019)

Synthesis and performance Optimization of Switching Nano-crossbar Computer
Partners: ITU (istanbul Teknik Universitesi), UMIL (Universita degli studi di Milano, IROC TECHNOLOGIE SA, KIT(Karlsruher Institut Fuer Technoligie) Germany, Grenoble-INP
The main goal of this project is developing a complete synthesis and optimization methodology for switching nanocrossbar arrays that leads to the design and construction of an emerging nanocomputer. New computing models for diode, FET, and four-terminal switch based nanoarrays are developed. The proposed methodology implements both arithmetic and memory elements, necessitated by achieving a computer, by considering performance parameters such as area, delay, power dissipation, and reliability. With combination of arithmetic and memory elements a synchronous state machine (SSM), representation of a computer, is realized. The proposed methodology targets variety of emerging technologies including nanowire/nanotube crossbar arrays, magnetic switch-based structures, and crossbar memories. The results of this project will be a foundation of nano-crossbar based circuit design techniques and greatly contribute to the construction of emerging computers beyond CMOS.

CEC / QUOG-DP project (Sep 01, 2019 - Aug 31, 2020)

Quantum Optimization of Worldwide LHC Computing Grid data placement
Partners: European Laboratory for Nuclear Research (CERN), Suisse ; TIMA/Grenoble INP ; University Politehnica of Bucharest, Roumanie
Starting from the specific case of the ALICE Collaboration at LHC, this project will try to determine the optimal storage, movement and access of the data produced by the ALICE experiment in quasi real-time, in order to improve resource allocation and usage and to increase the efficiency of data handling workflow. The work will be done in collaboration with Google, which has extensive experience in distributed computing and is developing one of the most advanced hardware and software QC programmes. TIMA will provide its expertise in optimisation and statistical analysis techniques.

CEC-NATIONAL

CEC-NATIONAL (May 01, 2019 - May 31, 2022)

AI4DI project Artificial Intelligence for Digitizing Industry

Partners: Infineon Technologies Ag, Audi Aktiengesellschaft, Fraunhofer Gesellschaft Zur Foerderung Der Angewandten Forschung E.v., Technische Universitaet Dresden, Technische Universitaet Muenchen, Avl List Gmbh, Infineon Technologies Austria Ag, Technische Universitaet Graz, Kompetenzzentrum - Das Virtuelle Fahrzeug, Forschungsgesellschaft mbh, Vysoke Uceni Technicke V Brne, Institut Mikroelektronickych Aplikaci S.r.o., Stmicroelectronics Srl, Dpcontrol Srl, Consorzio Nazionale Interuniversitario Per La, Nanoelettronica, Scm Group Spa, Tttech Computertechnik Ag, Sintef As, Elektronikas Un Datorzinatnu Instituts, Industrial Technology Research Institute Incorporated, Interuniversitair Micro-Electronica Centrum, Uab Teraglobus, Vilniaus Gedimino Technikos Universitetas, Stmicroelectronics Grenoble 2 Sas, Commissariat A L Energie Atomique Et Aux Energies Alternatives, Technext, Universite De Reims Champagne-Ardenne, Institut Polytechnique De Grenoble, Denofa As, Iglobaltracking As, Nxtech As, Intrasoft International Sa, Information Technology For Market Leadership, Know-Center Gmbh Research Center For Data-Driven, Business & Big Data Analytics, Murata Electronics Oy, Teknologian Tutkimuskeskus Vtt Oy, Linkker Oy, Vranken-Pommery Monopole, Ostbayerische Technische Hochschule - Amberg Weiden, Vaisto Solutions Ltd., Cognition Factory Gmbh, Symate Gmbh.

CEC-NATIONAL / OCEAN 12 project (Apr 01, 2018 - Dec 31, 2021)

Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node

Partners: TIMA, RFICLAB, IMEP

OCEAN12 is a major “Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node" and leverage Europe leadership on Automotive and aeronautics applications. OCEAN12 aims to bring concrete technological solutions and corresponding demonstrators to the key societal challenge of Smart mobility. Since the last few years, electronic components become more and more prevalent in the automotive industry. Today they create a superior value for the final customer and represent an important vector of differentiation in this industry. The share economy model, which drives innovation strategies in Smart mobility, will further increase the need for safe, cost efficient, secure, reliable and un-hackable operations, raising logically the proportion of electronics and software as a percentage of the total cost of a vehicle. Based on the innovative FDSOI technology, OCEAN12 will develop new processors and applications designs that leverage Fully Depleted Silicon On Insulator (FD-SOI) technology to offer the industry’s lowest power consuming processor and components, especially for automotive and aeronautic applications.

CEC-NATIONAL (Jan 01, 2014 - Mar 31, 2019)

THINGS2DO project Conception et développement de produits exploitant la technologie FDSO

Partners: Union européenne, État, collectivités locales, autres personnes publiques...

The program THINGS2DO is focused on building the Design & Development Ecosystem for FD-SOI-technology. This technology is uniquely positioned to take advantage of some very distinct strengths of the European Semiconductor Industry. The baseline 28nm FD-SOItechnology is available at an inflection point in the semiconductor progression path and offers unique features at this particular point in time. 14nm-FD-SOI will then take the technology’s integration potential to unprecedented levels, utilizing the design/development ecosystem developed here.

COLLECTIVITES TERRITORIALES

COLLECTIVITES TERRITORIALES / MESSI project Mixed-Signal Self-Test IPs for on-chip testing and technology qualification (Jan 01, 2019 - Dec 31, 2022)

Partners:

Le programme Nano 2022 décline et prolonge en France l’IPCEI Microelectronics de l'UE. Il vise à promouvoir la recherche, le développement et la première industrialisation de composants électroniques innovants, et à favoriser leur intégration dans le processus d’innovation des filières situées en aval. Il a défini cinq champs technologiques : composants numériques basse consommation, composants de puissance, capteurs intelligents, équipements optiques, semi-conducteurs composites. Le Laboratoire TIMA va développer des IPs de test embarqué pour des circuits analogiques et mixtes numérique-analogique en collaboration avec STMicroelectronics.

EPST

EPST / Digital Hardware AI Architectures project (May 01, 2019 - Mar 31, 2023)

Partners: Google France Kalray STMicroelectronics Upmem

According to a recent Facebook analysis, AI tasks need a 100x power reduction in the coming years to be sustainable. This chair focuses on highly energy efficient hardware/software architectures integration of AI and deep-learning to take up this challenge.

EPST / Hardware for spike-coded neural networks exploiting hybrid CMOS non-volatile technologies project (Jun 01, 2019 - May 31, 2023)

Partners: CEA LETI - Alexandre VALERIAN

Spiking Neural Networks are seen as a Key building block for strongly improving the energy efficiency of current AI applications and opening up new possibilities (in terms of unsupervised learning, recurrent networks, probabilistic inference, etc.). In that respect, the Grenoble R&D ecosystem has key strengths, especially its capability to design and manufacture embedded systems in advanced hybrid CMOS-Non Volatile Memory (NVM) technology. The scientific challenges to be tackled are the following. The first one is to define power-constrained learning and inference algorithms (online, supervised, unsupervised, probabilistic, etc.). The second one is to design a scalable and flexible SNN architecture, adaptable to the different above-mentioned algorithms, and fabricate that circuit in hybrid nanoscale CMOS and NVM technology, enabling very dense synaptic density. The last objective is to derive a principled toolchain for the algorithm, design, development, and integration of spiking neural networks for future adoption in industrial health and automotive embedded applications.

EPST / Conception Analogique project (Feb 15, 2019 - Feb 14, 2020)

Partners: CMP

CMP a recueilli ces dernières années de nombreuses demandes pour mettre à disposition des IP fonctionnelles en exemple et pouvant être utilisées par sa communauté d'utilisateurs. Avec le support et l'expertise du laboratoire TIMA, ce projet développe des fonctions microélectroniques analogiques de base, incluant des views schématiques et layout, en technologie FDSOI 28nm.

EPST / PICS - Indie TEST project Indirect test solutions for analog, mixed-signal, and RF integrated systems (Jan 01, 2017 - Dec 31, 2019)

The combination of indirect test and Built-In Self-Test (BIST) is a promising solution to mitigate the increasing cost of testing complex mixed-signal integrated systems. Indirect test replaces complex specification measurements by simpler signatures, and then uses modern data analysis algorithms to map these signatures onto the specification space. Signatures can be efficiently monitored by simple on-chip test instruments that can be integrated together with the system under test. Indirect test is then an interesting path to enable cost-effective BIST for mixed-signal systems. This PICS project has the goal of developing reliable and accurate built-in indirect test methods for complex mixed-signal systems. The project is structured into two interconnected research lines: a) Combining causal inference techniques with feature selection and feature extraction algorithms for indirect test, and b) Developing a feature-driven strategy for the definition of on-chip test instruments

EPST / Microbayes - Probabilistic Machines for Low-level Sensor Interpretation project (Jun 01, 2016 - Nov 30, 2019)

Partners: LIG, GIPSA-lab, IF, TIMA

The development of modern computers is mainly based on increase of performances and decrease of size and energy consumption. This incremental evolution is notable, but it involves no notable modification of the basic principles of computation. In particular, all the components perform deterministic and exact operations on sets of binary signals. These constraints obviously impede further sizable progresses in terms of speed, miniaturization and power consumption. As detailed below, the goal of the MicroBayes project is twofold: (1) to investigate a radically different approach to perform computations, namely stochastic computing using stochastic bit streams. And (2) to show that stochastic architectures can outperform standard computers to solve complex inference problems both in terms of execution speed and of power consumption. We will evaluate stochastic machines on difficult Bayesian inference problems. Moreover we will demonstrate the interest and feasibility of stochastic computing on two applications involving low-level information processing from sensor signals.

EPST / ARTE project Architectures de Réseaux de neurones Ternaires dédiées pour l'Embarqué (May 01, 2019 - Dec 31, 2020)

EPST / CADI project Calcul Approché et Distribué dans les systèmes Intégrés (May 01, 2019 - Dec 31, 2020)

Le projet CADI a pour but de mieux comprendre les problématiques (et proposer des solutions) liées à l'extension du paradigme "Approximate Computing" à des applications multitâches devant s'exécuter sur des systèmes intégrés multi cœurs. Le spectre de recherche étant très large, nous nous proposons d'axer dans un premier temps notre champ d'investigation essentiellement aux aspects logiciels (application et système d'exploitation) avec en vue une exécution sur une plateforme matérielle adéquate. Cela passera par une redéfinition de l'usage des métriques de précision dans ce contexte et par une gestion intelligente des ressources matérielles et logicielles en fonction de ces métriques.

EPST / CROCHET project Low Cost Control Flow Checking for Secure Applications Based on Nonlinear Codes (May 01, 2019 - Dec 31, 2020)

EPST / IRT 40 project "IRT 40 conception de systèmes sur puce pour la vision embarquée" (Jan 01, 2019 - Dec 31, 2019)

EUREKA

EUREKA / HADES project (Apr 01, 2017 - Mar 31, 2020)

Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems

Partners: IROC TECHNOLOGIES; CNRS/Délégation Languedoc Roussillon; TEMENTO SYSTEMS; ISSM; THALES COMMUNICATIONS ET SECURITYS SAS; CEA Commissariat à l'Energie Atomique et aux Energies Alternantives; STMICROELECTRONICS (GRENOBLE 2) SAS; UNIVERSITE PARIS VI; NXP SEMICONDUCTORS FRANCE

The objective of the project is to create a hierarchical on-line test infrastructure that allows reutilization of the same test programs though out all levels of hierarchy in an electronic equipment. This test infrastructure will be based on standards like IEEE 1687 for larger systems and on SPI or I2C for smaller SoC devices. At the same time a number of test instruments will be developed to be embedded in the chips to facilitate on line testing and data collections to allow early fault detection, diagnose and repair. These test instruments could indicate also circuit degradation even before a fault really occurs, and could be use to tune the circuit performance to save power.

INDUSTRIE

INDUSTRIE / Thèse Grégoire GIMENEZ project (Oct 10, 2016 - Oct 10, 2020)

"Etude et conception de puces sécurisées basse consommation pour plateforme IoT"

Partners: Dolphin Intégration, IC'Alps

INDUSTRIE / ICALPS - G.GIMENEZ project (Sep 03, 2018 - Sep 02, 2020)

Conception de circuits d'identification sécurisé basse consommation

Néant

INDUSTRIE / Pyxcad 2019 project (Jan 01, 2019 - Dec 31, 2019)

"Développement microélectronique pour des interfaces de mesure "

Partners: XDIGIT

Deux tâches sont réalisés dans ce projet : (1) développement microélectronique et réalisation de tests pour le projet MASSAR, (2) développement d’interfaces microélectroniques de mesure pour le comptage de photons.

INTERNATIONAL

INTERNATIONAL / BRAFISAT project (Jan 01, 2019 - Dec 31, 2022)

Partners: Institut Polytechnique de Grenoble (Grenoble INP), Université Grenoble Alpes, Université de Montpellier, Institut Polytechnique de Bordeaux (Bordeaux INP), Institut Mines-Télécom (IMT), Universidade Federal de Santa Maria (UFSM), Instituto Tecnologico de Aeronautica (ITA), Universidade Federal do Ceara (UFC)

Ce projet baptisé BRAFISAT : « Coopération BRA sil- F rance pour la formation d'ingén I eurs dans les domaines d'exploration de micro et nano SAT ellites » vise à établir un nouveau réseau d'universités françaises et brésiliennes qui explorent et développent les thématiques relatives à la conception, fabrication et qualification de nano-satellites. L'objectif principal du projet est la formation d'ingénieurs ayant les capacités à résoudre les défis associés à la microélectronique , à l' électronique en général , à la télécommunication et aux systèmes embarqués de ces engins spatiaux à petite taille et faible poids ainsi que toutes les thématiques d'autres applications exigeant aussi la connaissance de différents domaines de l'électronique. Les établissements d'enseignement supérieur participants du projet sont l'Institut Polytechnique de Grenoble (PHELMA), l'Université Grenoble Alpes (Polytech Grenoble), l'Université de Montpellier (Polytech Montpellier), l'Institut Polytechnique de Bordeaux (ENSEIRB-MATMECA), l'Institut Mines-Télécom (Mines St-Etienne), l'Universidade Federal de Santa Maria (UFSM), l'Instituto Tecnológico de Aeronáutica (ITA) et l'Universidade Federal do Ceará (UFC). Dans le contexte de l'appel BRAFITEC, les équipes d'enseignants-chercheurs du projet BRAFISAT composeront un consortium inédit qui permettra ainsi la réalisation de nouvelles coopérations entre les universités françaises et brésiliennes participantes. L'UFSM et l'ITA n'ont jamais eu des projets BRAFITEC avec les universités françaises participantes de ce projet. Par ailleurs, celui-ci est le premier projet BRAFITEC auquel l'UFSM participe, ce qui permettra de créer de nouveaux liens entre cette excellente université brésilienne et cinq universités françaises renommées.

MINISTERES-FUI

MINISTERES-FUI / LISA project (Mar 26, 2014 - Jun 30, 2019)

"Ultra low power Integrated circuit for Secure RF"

Partners: DOLPHIN INTEGRATION SMART PACKAGING SOLUTIONS UNIVERSITE D'AIX MARSEILLE MORPHO STARCHIP

Le marché sans contact /dual interface est en pleine croissance dans les 3 principaux domaines : le transport, l'identité et le bancaire. C'est l'industrie de la carte à puce des années 90 qui est à l'origine des produits sans contact actuels (Puce, Module, Antenne, Inlay). Le projet LISA propose de finaliser ce processus et de développer des objets sans contact, basée sur un nouveau module RF (13,56 Mhz/10 cm de portée) dual interface intégrée (puce & antenne) compatible avec les infrastructures existantes (mêmes lecteur), sans alimentation extérieure et compatible avec moyens actuels de production. Son objectif majeur est de diviser par 10 le besoin énergétique des solutions actuelles à performances égales. A cette fin les partenaires se fixeront comme sous objectifs de diviser par 5 la consommation de la puce et multiplier par 2 l'énergie récupérée par l'antenne.

MINISTERES-FUI / IMSPOC-UV project (Oct 01, 2018 - Sep 30, 2021)

Imaging Spectrometer On Chip

Partners: Gipsa / IPAG / CSUG / IGE

Imaging Spectrometer On Chip ou ImSPOC-UV est le nom du projet et celui d'un dispositif très intégré qui permet d'augmenter notre vision du monde qui nous entoure. Si l'oeil humain se satisfait de 3 couleurs, un appareil qui multiplie par 100 le nombre de couleurs intelligibles permet alors de comprendre la vraie nature de chaque point de l'image au point de mesurer sa composition chimique, la présence de cellules tumorales etc … Cette technique va permettre de mieux appréhender l'évolution du climat et de la pollution depuis l'espace, et c'est l'objet du projet ImSPOC-UV de construire le module compact de spectro-imagerie applicable au spatial et également approprié pour certaines applications industrielles ou médicales et dont le principe pourra sans doute, à terme, être étendu à des appareils grand-public.

REGION

REGION / SAFE-AIR project (Apr 10, 2017 - Sep 29, 2022)

Safety Evaluation of Aircraft Systems using Virtual Platforms

Partners: LCIS, Valence

Confrontées à des exigences de certification de plus en plus contraignantes en termes de sûreté de fonctionnement, les entreprises notamment dans le domaine des transports recherchent de nouvelles méthodes pour évaluer la robustesse des systèmes intégrés numériques complexes. En particulier nos partenaires industriels dans ce projet, THALES Valence et AEDvices consulting, s'intéressent à la robustesse des systèmes de vol utilisés en aéronautique. En effet, ces systèmes intégrés, du fait de l'évolution des technologies, sont de plus en plus sensibles aux perturbations causées par exemple par les particules atmosphériques ou d'autres phénomènes environnementaux. Plusieurs méthodes sont bien établies pour évaluer la sûreté des systèmes électroniques. Les analyses d'arbres de fautes (« Fault Tree Analysis » FTA) et les analyses des modes de défaillances (« Failure Mode Effect Analysis » FMEA) en sont deux exemples. Cependant, les organismes de certification imposent aux constructeurs de garantir par des méthodes de plus en plus rigoureuses (et déterministes) la robustesse de leurs systèmes. De nombreux standards imposent aujourd'hui une évaluation de sûreté fonctionnelle, en fonction du domaine d'application. On peut citer le IEC 61508 pour les équipements électroniques industriels, le DO-254 pour l'avionique, l'ISO 26262 pour l'automobile, l'ISO 60601 pour le médical, … Ainsi, notre projet vise une évaluation plus précise du niveau de robustesse réel des systèmes numériques complexes, très tôt dans le développement. Réaliser une évaluation précise très tôt dans le développement permet d'éviter des corrections tardives coûteuses et d'améliorer très sensiblement le temps de mise sur le marché, conduisant à augmenter considérablement la productivité. Elle permet aussi de concevoir des protections au « juste coût » ni « sur » ni « sous » dimensionnées. Au-delà des systèmes aéronautiques et des systèmes de transport en général (automobile ferroviaire), les résultats de ce projet intéressent TOUS les systèmes intégrés utilisés dans les applications critiques : systèmes de générations d'énergie (centrale nucléaire), implants médicaux ou encore systèmes pour l'internet (routeurs)… Tous les acteurs ayant besoin de respecter l'un de ces standards pourront bénéficier de l'approche que nous proposons pour anticiper leurs certifications. Le projet proposé s'appuie sur une méthode d'analyse multi-niveau, c'est-à-dire prenant à la fois en compte l'effet des perturbations sur les composants matériels et également la propagation des erreurs dans le système, que ce soit à l'intérieur du composant lui-même ou au niveau plus général de l'équipement. Les méthodes et outils développés permettront de mieux cibler la mise en place de solutions ou contremesures efficaces (soit au niveau équipement, soit au niveau composant) pour garantir la robustesse de l'intégralité d'un équipement dès la phase de conception des composants matériels. Notre proposition vise à réduire le fossé qui existe aujourd'hui entre le niveau composant (circuit ou système intégré) et le niveau équipement (produit global). La première contribution du projet est l'utilisation d'une modélisation de l'équipement sous la forme d'une plateforme dite "virtuelle", permettant de créer un modèle exécutable du système complet, incluant le composant en cours de développement. Cette modélisation de haut niveau du système (modélisation conjointe du logiciel et du matériel) permettra de prendre en compte la propagation des erreurs en sortie du composant dans tout le système. Elle s'appuiera sur plusieurs approches complémentaires, en exploitant les compétences et connaissances antérieures du LCIS et de TIMA. La seconde contribution du projet est la génération de nouveaux modèles de fautes au niveau système à partir des simulations des composants. Ces modèles de fautes seront plus réalistes que des modèles générés directement au niveau système. Le fait de s'affranchir des simulations des composants matériels lors de la simulation du système permettra d'augmenter la vitesse des simulations. La dernière contribution que nous proposons est l'utilisation d'un nouveau modèle de fautes. Récemment dans le cadre du projet ANR LIESSE (dans lequel le LCIS et le TIMA étaient partenaires) a été proposé un modèle de fautes spécifique permettant de modéliser l'effet des attaques laser sur les composants matériels. Ce modèle de fautes qui prend en compte les propriétés de localité des attaques laser peut être réutilisé pour modéliser plusieurs types de perturbations, dont l'effet des particules atmosphériques sur les composants matériels. Ce projet est pour nos entreprises partenaires une opportunité de valorisation de ces résultats de l'ANR LIESSE. Ce projet s'inscrit dans les domaines d'excellence « NUMERIQUE » et « MOBILITE, SYSTEMES DE TRANSPORT INTELLIGENTS » de la région. Il s'inscrit aussi dans le pôle de compétitivité MINALOGIC. Finalement, les outils et méthodes développés dans le cadre de ce projet contribueront à développer les techniques utilisées par THALES Valence et à ouvrir un nouveau champ connexe (l'analyse de la tolérance aux fautes) à l'offre d'AEDvices consulting.

REGION / Convertisseur temps numérique project (Jan 01, 2017 - Dec 31, 2020)

Dispositif microélectronique ultra-précis de mesure de temps basé sur l'oscillateur en anneau auto-séquencé

Partners: Institut National des Postes et Télécommunications (Marroc)

This project is a continuation of the work previously initiated within the framework of the COOPERA project n ° 1500546501 started in 2015. A new fully digital high resolution time-to-digital converter (TDC) based on a self-timed ring oscillator (STR) is presented. The proposed TDC can virtually achieve as fine as desired time resolution by simply increasing its number of stages thanks to the STR unique features. Moreover, the proposed technique allows on-the-fly time measurement on fast non-periodic signals. The TDC has been designed using 28 nm FDSOI CMOS technology to provide a proof of concept of the proposed method. Simulation results point out the advantages of this TDC in terms of compactness and measurement accuracy. The principle of this innovative system and the obtained results have been published in two international conferences EFTF-IFCS 2017 [1] and NEWCAS 2017 [2]. Another journal publication is in preparation. The goal of this project is the hardware validation of the proposed architecture, already validated theoretically and by simulation. Firstly, by its implementation on an FPGA device, which will allow a relatively fast and modular hardware validation of the principle. Then, by designing and manufacturing of a testchip in CMOS technology to completely validate this innovative concept. We also wish to study the use of this device in specific applications in order to target possible industrial transfer. We have already contacts with companies in the region interested such a system, in particular by the very precise measurement of the time of flight of a radiofrequency wave for geolocation application or for high-performance analog-digital conversions. [1] A. El-Hadbi, A. Cherkaoui, O. Elissati, and L. Fesquet, High Precision Time Measurement using a Self-timed Ring Oscillator based TDC, 2017 Joint 31st European Frequency and Time Forum & 71st IEEE International Frequency Control Symposium (EFTF/IFCS), Besançon, France, 2017. (Accepted) [2] A. El-Hadbi, A. Cherkaoui, O. Elissati, J. Simatec, and L. Fesquet, On-the-fly and Sub-Gate-Delay Resolution TDC based on Self-Timed Ring: A Proof of Concept, in 2017 12th IEEE International New Circuits and Systems Conference (NEWCAS) , Strasbourg, France, 2017.

REGION / OVNIPROM project (Nov 01, 2017 - Dec 31, 2020)

"Ordinateur de vol d'un nanosatellite implémenté dans un processeur many-core"

Partners: Université Concordia (Canada)

Le but principal de ce projet est l'implémentation de l'ordinateur de bord d'un nano-satellite dans un processeur ayant des nombreux cores de calcul ce qui permettra atteindre la performance et la fiabilité requises. Le processeur choisi comme cible a été le MPPA, dont la version appelée Bostan a 256 cores, circuit fabriqué par l'entreprise grenobloise KALRAY. Ce processeur étant au coeur des activités du projet CAPACITES (Calcul Parallèle pour Applications Critiques en Temps et Sûreté) financé dans le cadre de LEOC (Logiel Embarqué et Objets Connectés) dans lequel TIMA est partenaire, a déjà fait l'objet de campagnes de test sous radiations qu'ont mis en évidence sa sensibilité intrinsèque et l'efficacité des techniques de tolérance aux fautes implémentées dans le cadre des deux dernières thèses soutenues à TIMA et dirigées par Dr. Raoul Velazco. La contribution significative et l'objectif principal du projet OVNIPROM sera le développement de l'ordinateur de bord d'un nanosatellite dans le MPPA. Les diverses applications nécessaires pour les activités à bord du nanosatellites (contrôle d'attitude, télécommunication, traitement d'images, contrôle de l'énergie, etc...) pourront être implémentées dans le MPPA, bénéficiant de la mutliplicité de cores. Bien entendu deux paramètres significatifs seront considérés lors de l'implémentation: la performance requise pour certaines des applications mentionnées, et la tolérance aux fautes de celles en relation étroite avec la fiabilité, ceci pour garantir les objectifs du nanosat et assurer une durée de vie la plus longue possible.

REGION / GRESAM project (Jul 01, 2019 - Dec 31, 2020)

Grenoble Sousse Autonomous Microsystems

Partners: Université de Sousse, Tunisie

Dans le cadre d'une collaboration entre l'équipe CDSI de TIMA et NANOMISEN du CRMN à Souuse, on souhaite développer des piézoélectrets en utilisant le PVA, polymère biocompatible de plus en plus étudié dans la communauté travaillant sur les MEMS. En s’appuyant sur le savoir-faire acquis entre 2013 et 2017 sur la première génération de piézoélectrets en PDMS nous souhaitons : - optimiser les méthodes de microfabrication (création de microcavités, manipulation de films très souples, assemblage de matériau par collage plasma, effet de la température de réticulation, de l’agent rétuculant, etc) pour obtenir des échantillons de plusieurs centaines de cm2 , - optimiser le dépôt électrodes métalliques à base de nano-fils d’argent qui permettent des déformations très importantes, - analyser l’effet des paramètres physiques (pression dans les microcavités, température, nature et durée d’application du champ électrique, etc.) jouant sur la densité de charges engendrée dans les cavités, - caractériser les propriétés piézoélectriques (effets direct et inverse), - étudier le vieillissement de ces matériaux sans sollicitation (auto-décharge) puis lors de sollicitations mécaniques en grandes déformations.

REGION / FAIR project (Mar 20, 2018 - Jun 15, 2023)

Conception et fabrication par Fabrication Additive de produits Intelligents

Partners: GSCOP et TIMA

Les produits intelligents sont des composants essentiels de l'industrie 4.0. Ces produits sont capables de fournir des informations relatives à leur état ou à leur environnement voir permettre une interaction entre l'entreprise et le produit. Quelles technologies de fabrication sont capables de réaliser de tels produits, en intégrant les contraintes de réduction des coûts et des délais de fabrication ? Les nouvelles technologies de fabrication comme la Fabrication Additive (FA) permettent d'envisager la réalisation de produits intelligents. Le principe généralement retenu consiste à placer des capteurs et/ou des actionneurs (appelés devices) au sein du produit afin de suivre et/ou contrôler son comportement durant la phase d'utilisation L'objectif à l'issu du projet est de proposer un pré-démonstrateur permettant d'évaluer les possibilités techniques d'utiliser les technologies de Fabrication Additive afin de réaliser des produits métalliques intelligents d'une part et le déploiement potentiel dans le monde industriel d'autre part. Pour cela, une démarche permettant d'intégrer dès la conception des capteurs et/ou actionneurs au sein d'un produit fabriqué par une technologie WAAM (Wire and Arc Additive Manufacturing) sera proposée. Les procédés de fabrication WAAM utilisent un arc électrique pour fusionner un métal d'apport sous forme de fil. La pièce 3D est ainsi générée par empilement de cordons de soudure à partir de tout type de matériau soudable. Les procédés WAAM présentent l'avantage d'être plus productifs et moins onéreux que les autres technologies de FA. En utilisant ces procédés, l'insertion des devices dans la pièce en cours de construction est également facilitée. Le partenariat est composé des laboratoires grenoblois G-SCOP et TIMA (CNRS, Grenoble INP, Université Grenoble Alpes). G-SCOP possède des compétences en fabrication additive métallique, des activités de recherche sur cette thématique y sont menées depuis 2012. En 2017, des travaux plus spécifiques aux procédés WAAM ont démarré avec l'acquisition par le pôle S.MART Dauphiné Savoie d'une cellule de soudage robotisée sur laquelle s'appuierons les essais réalisés au cours de ce projet. Un des axes de recherche de TIMA concerne la conception, la fabrication et le test de dispositifs, circuits et systèmes intégrés et l'activité principale se concentre sur la minimisation de l'énergie et la miniaturisation de composants et systèmes. 2 Les principaux verrous scientifiques liés à cette intégration et qui restent à lever sont : rendre compatible une technologie de fabrication additive avec l'insertion de devices dans un produit au cours de sa réalisation, préparer le/les devices pour permettre leur intégration dans le produit avec la technologie retenue (opérations de packaging) et conserver les performances des devices après leur intégration. Ce projet répond à des interrogations d'industriels de la région Auvergne Rhône-Alpes qui soutiennent le projet : Caterpillar veut tester la technologie pour la réalisation de crochets de levage intelligents; ART est une PME spécialiste du rechargement métallique qui envisage d'étendre ses activités vers la fabrication additive de pièces métalliques intelligentes.

SATT

SATT / Ovnipromsat / OVSAT project (Nov 16, 2019 - May 15, 2021)

L'objectif d'OVSAT est de développer et valider un ordinateur de bord pour nano satellites, utilisant un processeur 256 cœurs, qui offrira des performances et une fiabilité sans précédent. La multiplicité des nœuds de calcul et la haute performance du processeur permettra d'une part l'implémentation de l'ensemble des applications requises dans un seul OBC et d'autre part l'adaptation de techniques logicielles de tolérance aux fautes. Dans ce contexte, l'ordinateur de bord OVSAT est un candidat idéal pour les applications nécessitant des hautes performances et une fiabilité élevée.

International activities

This section gives an overview of international activities in which the members of the Laboratory participated.

International collaborations in 2019

The Laboratory is engaged or has been recently engaged in a number of cooperations. They are listed below. These cooperations took various forms, e.g. extended visits of researchers at the cooperative location, organization of joint research, organization of workshops, etc.

International collaborations that are carried in the frame of a formal contract are listed in the Contracts section.

AMfoRS team (Architectures and Methods for Resilient Systems)

Invited Professor at Politecnico di Torino
Team: AMfoRS
Scientific Manager: PORTOLAN M.
Partners: Politecnico di Torino
City: Torino
Country: ITALY
Start the: Dec 18, 2018 until Jun 17, 2019

Beyond Von-Neumann Computing
Team: AMfoRS
Scientific Manager: VATAJELU E.I.
Partners: Nokia
City: Antwerp
Country: BELGIUM
Start the: Nov 05, 2019 until Nov 05, 2019

CDSI team (Circuits, Devices and System Integration)

Modeling, design and characterization of electroacoustic micro-machined transducers
Team: CDSI
Scientific Manager: RUFER L.
Partners: Czech Technical University, Faculty of Electrical Engineering
City: Prague
Country: CZECH REP.
Start the: Jan 01, 2003 until Dec 31, 2019

High Frequency MEMS Sensor for Aeroacoustics Measurements
Team: CDSI
Scientific Manager: RUFER L.
Partners: Hong Kong University of Science & Technology (HKUST)
City: Hong Kong
Country: CHINA
Start the: Jan 05, 2004 until Dec 31, 2019

MEMS Technology for Acoustic Devices
Team: CDSI
Scientific Manager: RUFER L.
Partners: HKUST (Hong Kong University of Science & Technology)
City: Hong Kong
Country: CHINA
Start the: Jan 05, 2004 until Dec 31, 2019

Limits to thermal actuation in high frequency micromechanical resonators for sensing and timing applications (NATRES)
Team: CDSI
Scientific Manager: RUFER L.
Partners: CityU (University of Hong Kong) - Dept. of El. Eng
City: Hong Kong
Country: CHINA
Start the: Mar 01, 2005 until Dec 31, 2019

MEMS resonators and ultrasonic transducers
Team: CDSI
Scientific Manager: RUFER L.
Partners: City University of Hong Kong (CityU)
City: Hong Kong
Country: CHINA
Start the: Mar 01, 2005 until Dec 31, 2019

Acoustic Microdevices for Hearing Aids
Team: CDSI
Scientific Manager: RUFER L.
Partners: Politecnico di Torino
City: Torino
Country: ITALY
Start the: Jan 01, 2013 until Dec 31, 2019

Microstructures Integration to Sensors for Telemedicine Networks (MISETEN)
Team: CDSI
Scientific Manager: RUFER L.
Partners: Politecnico di Torino
City: Torino
Country: ITALY
Start the: Jan 01, 2013 until Dec 31, 2019

MEMS-based micro-speaker in polymer technology
Team: CDSI
Scientific Manager: RUFER L.
Partners: University of Electronic Science and Technology of China
City: Chengdu
Country: CHINA
Start the: Jan 01, 2016 until Dec 31, 2019

MEMS for Mechanobiology
Team: CDSI
Scientific Manager: RUFER L.
Partners: University of Brescia
City: Brescia
Country: ITALY
Start the: Jan 01, 2017 until Dec 31, 2019

Secure and Self-Aware Multi-core Systems (SSAMS) International Cooperation Project
Team: CDSI
Scientific Manager: POSSAMAI BASTOS R.
Partners: PUCRS (Pontifícia Universidade Católica do Rio Grande do Sul)
City: Porto Allegre
Country: BRAZIL
Start the: Jan 01, 2018 until Dec 31, 2020

Applications and Algorithms in Artificial Intelligence on Self-Driving Cars and Fault-Tolerance Techniques to Detect and Correct Errors and Attacks
Team: CDSI
Scientific Manager: POSSAMAI BASTOS R.
Partners: UFRGS (Universidade Federal do Rio Grande do Sul)
City: Porto Allegre
Country: BRAZIL
Start the: Apr 01, 2018 until Dec 31, 2019

Built-in Sensors for Reliable, Secure, and Low-Power Integrated Circuits
Team: CDSI
Scientific Manager: POSSAMAI BASTOS R.
Partners: DFKI (German Research Center for Artificial Intelligence)
City: Bremen
Country: GERMANY
Start the: Apr 01, 2018 until Dec 31, 2019

Evaluation of Multicore Systems Soft Error Reliability
Team: CDSI
Scientific Manager: POSSAMAI BASTOS R.
Partners: Loughborough University
City: LOUGHBOROUGH
Country: UNITED KINGDOM
Start the: Apr 01, 2018 until Dec 31, 2019

Infrastructure for Secure, Reliable, and Low-Power Computing Systems
Team: CDSI
Scientific Manager: POSSAMAI BASTOS R.
Partners: PUCRS (Pontifícia Universidade Católica do Rio Grande do Sul)
City: Porto Allegre
Country: BRAZIL
Start the: Nov 01, 2018 until Oct 31, 2022

SLS team (System Level Synthesis)

NUSANTARA Project - Efficiency of Reconfigurable Devices in Cryptography
Team: SLS
Scientific Manager: ROUSSEAU F.
Partners: Arif SASONGKO - Electronics Research Group, SEEI ITB
City: Bandung
Country: INDONESIA
Start the: Feb 01, 2018 until Dec 31, 2019

Organisation and participation of International Conferences, Workshops, Forums in 2019

In the following table, TIMA's researchers were involved in the organization of the listed events.

Acronym	Title	Location	Role	Name
AsianHOST	*Asian Hardware Oriented Security and Trust Symposium (AsianHOST'2019)*	Xi'an, CHINA	technical program committee	DI NATALE Giorgio
ASYNC	*25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC '2019)*	Hirosaki, JAPAN	technical program committee	FESQUET L.
ATS	*28th IEEE Asian Test Symposium (ATS'2019)*	The LaLiT Great Eastern Kolkata, INDIA	technical program committee	ANGHEL L.
			technical program committee	BARRAGAN M.
CENICS	*12th International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS'2019)*	Nice, FRANCE	industry/research committee	FESQUET L.
			technical program committee	FESQUET L.
COMPAS	*Conférence d'informatique en Parallélisme, Architecture et Système (COMPAS'2019)*	Anglet, FRANCE	technical program committee	ANDRADE L.L.
			technical program committee	LEVEUGLE R.
			technical program committee	MORIN-ALLORY K.
CS2	*6th Workshop on Cryptography and Security in Computing Systems (CS2'2019)*	Valencia, SPAIN	technical program committee	DI NATALE Giorgio
			technical program committee	MAISTRI P.
DATE	*Design, Automation & Test in Europe (DATE'2019)*	Firenze, ITALY	interactive presentations chair	PETROT F.
			publication chair	DI NATALE Giorgio
			technical program committee	BARRAGAN M.
			technical program committee	MORIN-ALLORY K.
			technical program committee	VATAJELU E.I.
			University Booth Co-Chair	VATAJELU E.I.
			vice general chair	DI NATALE Giorgio
DDECS	*22nd IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS'2019)*	Cluj-Napoca, ROMANIA	technical program committee	BARRAGAN M.
			technical program committee	LEVEUGLE R.
			technical program committee	MAISTRI P.
			technical program committee	PIERRE L.
			technical program committee	PORTOLAN M.
			topic chair	DI NATALE Giorgio
			topic chair	VATAJELU E.I.
DFT	*32nd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'2019)*	Delft, NETHERLANDS	technical program committee	ANGHEL L.
DSD	*22nd Euromicro Conference on Digital System Design (DSD'2019)*	Kallithea, Chalkidiki, GREECE	technical program committee	DI NATALE Giorgio
DTIS	*14th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS'2019)*	Mykonos, GREECE	program chair	VATAJELU E.I.
			technical program committee	DI NATALE Giorgio
ETS	*24th IEEE European Test Symposium (ETS'2019)*	Baden-Baden, GERMANY	embedded tutorial chair	ANGHEL L.
			publication chair	DI NATALE Giorgio
			review chair	DI NATALE Giorgio
			steering committee member	ANGHEL L.
			technical program committee	BARRAGAN M.
			technical program committee	MIR S.
			technical program committee	PAPAVRAMIDOU P.
			topic chair	LEVEUGLE R.
			topic chair	VATAJELU E.I.
FDL	*Forum on specification & Design Languages (FDL'2019)*	Southampton, UNITED KINGDOM	technical program committee	PIERRE L.

Acronym	Title	Location	Role	Name
FEDfRo	*4th IEEE Federative Event on Design for Robustness (FEDfRo'2019)*	Rhodes Island, GREECE	general chair	NICOLAIDIS M.
GDR SOC 2	*13ème Colloque National du GDR SOC2 (GDR SOC 2'2019)*	Montpellier, FRANCE	technical program committee	ANGHEL L.
GLSVLSI	*29th Great Lakes Symposium on VLSI (GLSVLSI'2019)*	Washington DC, USA	technical program committee	VATAJELU E.I.
ICCAD (Control Automation and Diagnosis)	*2nd International Conference on Control, Automation and Diagnosis (ICCAD (Control Automation and Diagnosis)'2019)*	Grenoble, FRANCE	technical program committee	SIMEU E.
ICCD	*37th IEEE International Conference on Computer Design (ICCD'2019)*	Abu Dhabi, UNITED ARABIAN EMIRATES	technical program committee	VATAJELU E.I.
IOLTS	*25th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2019)*	Rhodes Island, GREECE	finance chair	ANGHEL L.
			finance chair	VELAZCO R.
			general chair	NICOLAIDIS M.
			local organization	FOURNERET-ITIÉ A.-L.
			local organization	SIMEU E.
			local organization	ZERGAINOH N. - E.
			publication chair	PAPAVRAMIDOU P.
			steering committee member	NICOLAIDIS M.
			technical program committee	ANGHEL L.
			technical program committee	BARRAGAN M.
			technical program committee	BENABDENBI M.
			technical program committee	DI NATALE Giorgio
			technical program committee	LEVEUGLE R.
			technical program committee	MIR S.
			technical program committee	NICOLAIDIS M.
			technical program committee	PAPAVRAMIDOU P.
			technical program committee	SIMEU E.
			technical program committee	VATAJELU E.I.
ISCAS	*IEEE International Symposium on Circuits and Systems (ISCAS'2019)*	Sapporo, JAPAN	technical program committee	BARRAGAN M.
ISVLSI	*IEEE Computer Society Annual Symposium on VLSI (ISVLSI'2019)*	Miami, USA	technical program committee	DI NATALE Giorgio
			technical program committee	PORTOLAN M.
			technical program committee	VATAJELU E.I.
ITC	*IEEE International Test Conference (ITC'2019)*	Washington DC, USA	technical program committee	ANGHEL L.
			technical program committee	VATAJELU E.I.
			track chair	ANGHEL L.
IVSW	*4th International Verification and Security Workshop (IVSW'2019)*	Rhodes Island, GREECE	local organization	NICOLAIDIS M.
			program co-chair	DI NATALE Giorgio
			publicity chair	VATAJELU E.I.
			steering committee member	NICOLAIDIS M.
			technical program committee	DI NATALE Giorgio
			technical program committee	LEVEUGLE R.
			technical program committee	MAISTRI P.
			technical program committee	PIERRE L.
			technical program committee	VATAJELU E.I.
			vice-program chair	DI NATALE Giorgio
			website chair	DE BIGNICOURT A.
IWASI	*8th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI'2019)*	Otranto, ITALY	technical program committee	RUFER L.

Acronym	Title	Location	Role	Name
JNRSE	*9èmes Journées Nationales sur la Récupération et le Stockage de l'Energie (JNRSE'2019)*	Blois, FRANCE	technical program committee	BASROUR S.
LASCAS	*10th IEEE Latin American Symposium on Circuits and Systems (LASCAS'2019)*	Armenia, Quindío, COLOMBIA	technical program committee	MIR S.
			technical program committee	POSSAMAI BASTOS R.
LATS	*20th IEEE Latin American Test Symposium (LATS'2019)*	Santiago, CHILI	co-general chair	VELAZCO R.
			finance chair	FOURNERET-ITIÉ A.-L.
			publication chair	SIMEU E.
			technical program committee	ANGHEL L.
			technical program committee	DI NATALE Giorgio
			technical program committee	LEVEUGLE R.
			technical program committee	MIR S.
			technical program committee	POSSAMAI BASTOS R.
			technical program committee	SIMEU E.
MEMOCODE	*17th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE'2019)*	San Diego, USA	technical program committee	MORIN-ALLORY K.
MPSoC	*19th International Forum on MPSoC for Software - defined Hardware (MPSoC'2019)*	Hakone, Kanagawa, JAPAN	finance chair	ROUSSEAU F.
			technical program committee	PETROT F.
NANOARCH	*15th IEEE / ACM International Symposium on Nanoscale Architectures (NANOARCH'2019)*	Qingdao, CHINA	publicity chair	ANGHEL L.
			technical program committee	ANGHEL L.
			technical program committee	VATAJELU E.I.
PESW	*7th Prague Embedded Systems Workshop (PESW'2019)*	Prague, CZECH REP.	technical program committee	DI NATALE Giorgio
			technical program committee	VATAJELU E.I.
POWERMEMS	*The 19th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (POWERMEMS'2019)*	Krakow, POLAND	steering committee member	BASROUR S.
PROOFS	*8th International Workshop on Security Proofs for Embedded Systems (PROOFS'2019)*	Atlanta, USA	technical program committee	DI NATALE Giorgio
RAPIDO	*11th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO'2019)*	Valencia, SPAIN	technical program committee	PETROT F.
RSP	*30th International Workshop on Rapid System Prototyping (RSP'2019)*	New York, USA	general chair	ROUSSEAU F.
			publication chair	MULLER O.
			steering committee member	PETROT F.
			steering committee member	ROUSSEAU F.
			technical program committee	MULLER O.
			technical program committee	PETROT F.
			technical program committee	ROUSSEAU F.
SBCCI	*32nd Symposium on Integrated Circuits and Systems Design (SBCCI'2019)*	Sao Paulo, BRAZIL	technical program committee	POSSAMAI BASTOS R.
			track chair	POSSAMAI BASTOS R.
SecHard	*1st Workshop on Cybersecurity on Hardware (SecHard'2019)*	Canary Islands, SPAIN	technical program committee	DI NATALE Giorgio
			technical program committee	MAISTRI P.
			technical program committee	VATAJELU E.I.
SERESSA	*15th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA'2019)*	Seville, SPAIN	general chair	VELAZCO R.

Acronym	Title	Location	Role	Name
SIGNAL	*4th International Conference on Advances in Signal, Image and Video Processing (SIGNAL'2019)*	Athens, GREECE	steering committee member	FESQUET L.
			technical program committee	FESQUET L.
SMACD	*International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD'2019)*	Lausanne, SWITZERLAND	technical program committee	BARRAGAN M.
TESTA	*4th International Test Standards Application Workshop (TESTA'2019)*	Baden-Baden, GERMANY	workshop chair	PORTOLAN M.
TRUDEVICE	*8th Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE'2019)*	Baden-Baden, GERMANY	finance chair	DI NATALE Giorgio
TSS	*Test Spring School (TSS'2019)*	Baden-Baden, GERMANY	general chair	ANGHEL L.
VLSI-SoC	*27th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC'2019)*	Cuzco, PERU	publicity chair	MIR S.
			steering committee member	MIR S.
			technical program committee	BARRAGAN M.
			technical program committee	DI NATALE Giorgio
			technical program committee	MORIN-ALLORY K.
			technical program committee	VATAJELU E.I.
			track chair	MIR S.
VTS	*37th IEEE VLSI Test Symposium (VTS'2019)*	Monterey (CA), USA	publication chair	DI NATALE Giorgio
			publication chair	VATAJELU E.I.
			steering committee member	NICOLAIDIS M.
			technical program committee	BARRAGAN M.
			technical program committee	MIR S.
			vice-general co-chair	ANGHEL L.

Participation to Societies and Working Groups in 2019

2019

- Manuel BARRAGAN: IEEE member since 2014
- Manuel BARRAGAN: CEDA member
- Manuel BARRAGAN: TTTC member
- Giorgio DI NATALE: TTTC electronic media chair
- Giorgio DI NATALE: TTTC vice-chair
- Laurent FESQUET: Vice-Chapter Chair of the French IEEE Solid-State Circuits chapter
- Michael NICOLAIDIS: TTTC past chair
- Michele PORTOLAN: Core member of the IEEE P1687.1 Standardization Working Group
- Michele PORTOLAN: External member of the IEEE P2654 Standardization Working Group
- Ioana VATAJELU: Member of IEEE Test Technology Technical Council (TTTC)
- Ioana VATAJELU: Program Chair of TTTC Educational Programme

Awards and distinctions in 2019

AMfoRS team (Architectures and Methods for Resilient Systems)

April 26, 2019 - Best Paper Award at DDECS'2019 (Cluj Napoca, ROMANIA)
Best Paper Award at DDECS'2019 (22nd International Symposium on Design and Diagnostics of Electronics Circuits and Systems)
Date: April 24-26, 2019
Place: Cluj Napoca (ROMANIA)
Title: Encryption-Based Secure JTAG
Authors:

- Emanuele VALEA (LIRMM, Montpellier)
- Mathieu DA SILVA (LIRMM, Montpellier)
- Marie-Lise FLOTTES (LIRMM, Montpellier)
- Giorgio DI NATALE (TIMA, AMfoRS team, Grenoble)
- Bruno ROUZEYRE (LIRMM, Montpellier) CDSI team (Circuits, Devices and System Integration)

CDSI team (Circuits, Devices and System Integration)

October 9, 2019 - Winner of PhD Forum at VLSI-SoC'2019 (Cuzco, PERU)
Winner of PhD Forum at VLSI-SoC'2019 (27th IFIP/IEEE International Conference on Very Large Scale Integration)
Date: October 6-9, 2019
Place: Cuzco (PERU)
Title: A Digital Event-Based Strategy for ASK demodulation
Authors:

- Rodrigo IGA JADUE (TIMA - CDSI team)
- Sylvain ENGELS (TIMA - CDSI team)
- Laurent FESQUET (TIMA - CDSI team)

Educational tasks

Dealing with problems risen by advanced technologies and proposing advanced design and test methodologies, TIMA's members are, as a matter of fact, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people.

Open Seminars at TIMA in 2019

In addition to internal seminars, the Laboratory regularly publicises talks given by our visiting researchers. Grenoble academic and industrial researchers had the opportunity to listen to the following speakers:

Speaker	Institution	Date	Theme
Sungjoo YOO	Seoul National University (Full professor)	Jan 07, 2019	Low precision in neural network training and inference
Dr. Luciano OST	Loughborough University, UK	Oct 01, 2019	Evaluation of Multicore Platforms Soft Error Reliability Using Virtual Platforms

Seminars given by TIMA's members in 2019 excluding conferences

Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions:

Institution	Location	Date	Speaker	Title or content
IMT Atlantique	Nantes (France)	Dec 17, 2018 (2019 session)	Laurent FESQUET	Thinking and Designing Differently: the Asynchronous Alternative
FETCH 2019	Louvain-la-Neuve (Belgium)	Jan 28-30, 2019	Laurence PIERRE	Runtime assertion-based verification for correctness and reliability analysis

Roles of TIMA members on University faculties and research structures

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
ENSIMAG school				
Deputy Director	PETROT F.	01/09/2018	31/08/2022	
Restricted council member	MULLER O.	01/09/2017		Examine promotion files, invited professors, teaching assistants
	PETROT F.	01/09/2017		
School council member	MULLER O.	01/09/2017		Elected members - School Strategy, relations with industrial partners
	PETROT F.	01/09/2017		
PHELMA school				
Board of directors member	ANGHEL L.	01/09/2017		Strategy, jobs, promotion files, invited professors, teaching assistants
Co-responsible of SEI branch	BENABDENBI M.	01/09/2017		
Manager of SEI branch	MORIN-ALLORY K.	01/09/2017		
Manager of SEOC/PHELMA branch	PORTOLAN M.	01/09/2017		
School Council member	ANGHEL L.	01/09/2016		Elected members - School Strategy, relations with industrial partners
Polytech Grenoble				
Deputy director in charge of education and training	ROUSSEAU F.	01/09/2018		
Manager of Risks Prevention department	SIMEU E.	01/09/2017		
Responsible of E2I branch	ANDRADE L.	01/10/2019		5th year - Apprenticeship training
Restricted council member	ROUSSEAU F.	01/09/2017		Examine promotion files, invited professors, teaching assistants
	SIMEU E.	01/09/2017		
School council member	ROUSSEAU F.	01/09/2017		Elected members - School Strategy, relations with industrial partners
	SIMEU E.	01/09/2017		
IM2AG UFR				
Manager of Office Automation and Informatics	POSSAMAI BASTOS R.	01/09/2017		All trainings at Sciences and Technologies Licence Department (UGA)
Research commission member	PIERRE L.	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR Council member	PIERRE L.	01/09/2017		
TIMA Laboratory				
TIMA Laboratory				
Laboratory contact for european projects	ROUSSEAU F.	01/09/2017		

Research structures				
AIP PRIMECA				
Manager of CIM AIP PRIMECA platform	SIMEU E.	01/09/2017		
Carnot LSI				
TIMA representative	MIR S.	01/09/2009		
CIME				
Manager of Microsystems platform	BASROUR S.	01/10/2006		
Deputy Director	FESQUET L.	01/09/2017		
Manager of Communicating objects platform	MANCINI S.	01/09/2017		
Manager of Design platform	BENABDENBI M.	01/09/2017		
CSUG				
Technical manager	PANCHER F.	02/05/2018		
EEATS doctoral school				
Council member of EEATS doctoral school	SIMEU E.	01/09/2017		
HDR commission member of EEATS doctoral school	ROUSSEAU F.	01/09/2017		
MSTII doctoral school				
Council member of MSTII doctoral school	PIERRE L.	01/09/2017		
HDR Commission member of MSTII doctoral school	PETROT F.	01/09/2017		
FMNT				
Manager of Microelectronics Axis	ANGHEL L.	01/09/2017		
Manager of Telecommunications Axis	BARRAGAN M.	01/09/2017		
MSTIC cluster				
TIMA representative of MSTIC cluster	PETROT F.	01/09/2016		
Council member of MSTIC cluster	LEVEUGLE R.	01/09/2015		Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC
PEM cluster				
Council member of PEM cluster	BONVILAIN A.	26/11/2018	01/10/2019	Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC
TIMA representative of PEM cluster	BASROUR S.	01/09/2016		
PERSYVAL LabEx				
Education board member	PIERRE L.	01/01/2015		Training activities
Parent institutions				
Grenoble Institute of technology				
Board of Directors member	MANCINI S.	12/12/2019	01/01/2024	
Deputy vice-president for Industry relations	ANGHEL L.	01/09/2017		
Grenoble Alpes University				
Manager of Informatics Master M1-M2 UGA – G-INP	PIERRE L.	01/09/2017		In charge for UGA

Scientific production

International journals (RI)

AMfoRS

RI-1 Valea E.*, Da Silva M.*, Di Natale G., Flottes M.-L.*, Rouzeyre B.*
A Survey on Security Threats and Countermeasures in IEEE Test Standards
IEEE Design & Test, Volume: 36, pp. 95-116, 2019
**LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*

RI-2 Portolan M.
Automated Testing Flow: the Present and the Future
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: , 2019

RI-3 Vallero A.*, Savino A.*, Chatzidimitriou A., Kaliorakis M.**, Kooli M.***, Riera V.****, Di Natale G., Bosio A.*****, Canal R.****, Gizopoulos D.**, Di Carlo S.***
Early System Reliability Analysis for Cross-layer Soft Errors Resilience in Memory Arrays of Microprocessor Systems
IEEE Transactions on Computers, Volume: 68, pp. 765-783, 2019
**Politecnico di Torino, **University of Athens, ***CEA-LETI - Laboratoire d'Electronique de Technologie de l'Information, ****Universitat Politècnica de Catalunya, *****Institut des nanotechnologies de Lyon*

RI-4 Martin H.*, Peris-Lopez P.*, Di Natale G., Taouil M., Hamdioui S.****
Enhancing PUF Based Challenge-Response Sets by Exploiting Various Background Noise Configurations
MDPI Electronics, Volume: 8, 2019
**Universidad Carlos III of Madrid - Electronics Technology Department, **Delft University of Technology*

RI-5 Vatajelu I., Di Natale G.
High-Entropy STT-MTJ-based TRNG
IEEE Transactions on Very Large Scale Integration (VLSI) Systems , Volume: , 2019

RI-6 Kooli M.*, Di Natale G., Bosio A.**
Memory-Aware Design Space Exploration for Reliability Evaluation in Computing Systems
Journal of Electronic Testing: Theory and Applications, Volume: , 2019
**CEA-LETI - Laboratoire d'Electronique de Technologie de l'Information, **Institut des nanotechnologies de Lyon*

RI-7 Plassan G., Morin-Allory K., Borrione D.
Mining Missing Assumptions from Counter-Examples
Transactions on Embedded Computing Systems (TECS), Volume: 18, 2019

RI-8 Valea E.*, Da Silva M.*, Flottes M.-L.*, Di Natale G., Rouzeyre B.*
Stream vs block ciphers for scan encryption
Microelectronics journal, Volume: 86, pp. 65-76, 2019
**LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*

RI-9 Galy P.*, De Conti L.*, Delahaye G., Anghel L.
Topology and design investigation on thin film silicon BIMOS device for ESD protection in FD-SOI technology
Microelectronics Reliability, Volume: , 2019
**STMicroelectronics*

CDSI

RI-10 Germain S.*, Germain S., Engels S.*, Engels S., Fesquet L.
A High Level Current Modeling for Shaping Electromagnetic Emissions in Micropipeline Circuits
Journal of Low Power Electronics and Applications (JLPEA) - Open access, Volume: 9, 2019
**STMicroelectronics*

RI-11 Garay Trindade M., Coelho A., Valadares C.*, Andreoni Camponogara Viera R., Rey S., Cheymol B.**, Baylac M.**, Velazco R., Possamai Bastos R.**
Assessment of a Hardware-Implemented Machine Learning Technique under Neutron Irradiation
IEEE Transactions on Nuclear Science, Volume: , 2019
**Instituto Federal de Educacao, Ciencia e Tecnologia do Ceara , **LPSC - Laboratoire de Physique Subatomique et de Cosmologie*

RI-12 Rendon Hernandez A., Ferrari M.*, Basrour S., Ferrari V.*
Electrical modelling and characterization of a Thermo-Magnetically Activated Piezoelectric Generator (TMAPG)
Journal of Physics: Conference Series, Volume: 1407, 2019
**University of Brescia*

RI-13 Aquino Guazzelli R., Garay Trindade M., Fesquet L., Possamai Bastos R.
Learning-Based Reliability Assessment Method for Detection of Permanent Faults in Clockless Circuits
Microelectronics Reliability, Volume: , 2019

RI-14 Plassan G., Morin-Allory K., Borrione D.
Mining Missing Assumptions from Counter-Examples
Transactions on Embedded Computing Systems (TECS), Volume: 18, 2019

RI-15 Andreoni Camponogara Viera R., Maurine P.*, Dutertre J.M., Possamai Bastos R.**
Simulation and Experimental Demonstration of the Importance of IR-Drops During Laser Fault-Injection
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: , 2019
**LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier, **Ecole Nationale Supérieure des Mines de Saint-Etienne*

RI-16 Ayres A.*, Ayres A., Rozeau O., Borot B.*, Fesquet L., Batude P.**, Vinet M.****
Variance Analysis in 3D Integration: A Statistically Unified Model with Distance Correlations
IEEE Transactions on Electron Devices, Volume: 66, pp. 633-640, 2019
**STMicroelectronics, **CEA-LETI - Laboratoire d'Electronique de Technologie de l'Information*

RIS

RI-17 Garay Trindade M., Coelho A., Valadares C.*, Andreoni Camponogara Viera R., Rey S., Cheymol B.**, Baylac M.**, Velazco R., Possamai Bastos R.**
Assessment of a Hardware-Implemented Machine Learning Technique under Neutron Irradiation
IEEE Transactions on Nuclear Science, Volume: , 2019
**Instituto Federal de Educacao, Ciencia e Tecnologia do Ceara , **LPSC - Laboratoire de Physique Subatomique et de Cosmologie*
RI-18 Coelho A., Charif A.*, Zergainoh N.-E., Velazco R.
FL-RuNS: A High Performance and Runtime Reconfigurable Fault-Tolerant Routing Schemes for Partially-Connected 3D Networks-on-Chip
IEEE transactions on Nanotechnology, Volume: 18, pp. 806-818, 2019
**CEA-LETI - Laboratoire d'Electronique de Technologie de l'Information*

RMS

RI-19 Sharma E.*, Saadi A., Barragan M., Pistono E.**, Margalef-Rovira M., Lisboa de Souza A.A.**, Ferrari P.**, Bourdel S.****
Design of a 77-GHz LC-VCO With a Slow-Wave Coplanar Stripline-Based Inductor
IEEE Transactions on Circuits and Systems, Volume: , pp. 1-11, 2019
**HUAWEI Technologies France, **RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits*
RI-20 Bounceur A.*, Mir S., Euler R.*, Beznia K.*
Estimation of Analog/RF Parametric Test Metrics Based on a Multivariate Extreme Value Model (Early Access)
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: , 2019
**Université de Bretagne Occidentale*
RI-21 Renaud G., Diallo M., Barragan M., Mir S.
Fully-differential 4 V-output range 14.5-ENOB step-wise ramp stimulus generator for on-chip static linearity test of ADCs
IEEE Transactions on Very Large Scale Integration (VLSI) Systems , Volume: 27, pp. 281-293, 2019
RI-22 Silveira Feitoza R., Barragan M., Dzahini D., Mir S.
Reduced-code static linearity test of split-capacitor SAR ADCs using an embedded incremental Sigma-Delta converter
IEEE Transactions on Device and Materials Reliability, Volume: 19, pp. 37-45, 2019

SLS

RI-23 Muller O., Prost-Boucle A., Bourge A., Pétrot F.
Efficient Decompression of Binary Encoded Balanced Ternary Sequences (Early Access)
Transactions on Very Large Scale Integration (VLSI) Systems, Volume: , 2019
RI-24 Matoussi O., Pétrot F.
Loop aware CFG matching strategy for accurate performance estimation in IR-level native simulation
Integration, the VLSI Journal, Volume: , 2019

Invited conference talks (INV)

AMfoRS

INV-1 Anghel L.
Embedded Hardware Architectures for AI
From Brain and Cognition to Artificial Intelligence Workshop, 2019
INV-2 Vatajelu I.
Fault Modeling of Spiking Neural Networks with STDP
BioComp 2019, 2019
INV-3 Vatajelu I.
Fiabilité des architectures neuromorphiques
GDR SoC2 Journée Thématique: Sécurité, fiabilité et test des SoC 2 : challenges et opportunités dans l'ère de l'IA, 2019
INV-4 Anghel L.
Managing Aging Induced Reliability at Run-time
7th Workshop on Cross-layer Resiliency (IWCR'2019), 2019
INV-5 Vatajelu I.
Randomness in emerging technologies: Functional robustness vs. security
7th Prague Embedded Systems Workshop (PESW'2019), 2019
INV-6 Vatajelu I.
Reliability of neuromorphic computing
GDR BioComp & SoC2: Quantum and Neuromorphic Technologies Meet, 2019

INV-7 Anghel L.
Run-time Age Induced Reliability Prediction for SOC
IEEE Latin America Test Symposium (LATS 2019), 2019
INV-8 Maistri P.
Secure Test Architectures in IoT
European Nanoelectronics Applications, Design & Technology Conference (ADTC 2019), 2019

CDSI

INV-9 Fesquet L., Frisch R.*, Frisch R., Faix M.*, Belot J.*, Simatic J., Cherkaoui A.**, Mazer E.***
Asynchronous circuits for new computation paradigms
IEEE International Nanodevices & Computing Conference (INC 2019), 2019
**LIG - Laboratoire d'Informatique de Grenoble, **HawAI.Tech*
INV-10 Fesquet L., Akrarai M., Sicard G.*, Diallo M.
Event-Based Image Sensors
5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2019), 2019
**CEA-LETI - Laboratoire d'Electronique de Technologie de l'Information*
INV-11 Basrour S.
Piezoelectric devices for energy harvesting and actuators
International Workshop on Piezoelectric Materials and Applications in Actuators & ENHANCE Workshop (IWPMA 2019), 2019
INV-12 Basrour S.
Piezoelectric transducers for medical and biological applications
IEEE International Conference on Design & Test of integrated micro & nano-Systems (DTS 2019), 2019

RMS

INV-13 Mir S., Barragan M., Mammasse M.*
BIST Solutions for Industrial Mixed-signal Circuits
25th International On-Line Testing Symposium (IOLTS 2019), 2019
**STMicroelectronics*
INV-14 Cilici F., Leger G.*, Barragan M., Mir S., Lauga-Larroze E., Bourdel S.****
Efficient generation of data sets for one-shot statistical calibration of RF/mm-wave circuits
International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2019), pp. 17-20, 2019
**IMSE, Instituto de Microelectronica de Sevilla , **RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits*
INV-15 Barragan M., Leger G.*
Feature selection and feature design for machine learning indirect test: a tutorial review
International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2019), 2019
**IMSE, Instituto de Microelectronica de Sevilla*

International conferences (CI)

AMfoRS

CI-1 Merandat M.*, Reynaud V., Valea E., Quévremont J.***, Maistri P., Leveugle R., Flottes M.-L.**, Dupuis S.**, Rouzeyre B.**, Di Natale G.**
A Comprehensive Approach to a Trusted Test Infrastructure
4th International Verification and Security Workshop (IVSW 2019), 2019
**INVIA, **LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier, ***Thalès Communications, Colombes, France*
CI-2 Skaf A., Ezzadeen M., Benabdenbi M., Fesquet L.
Adjustable Precision Computing Using Redundant Arithmetic
Workshop on Approximate Computing (AxC'2019), 2019
CI-3 Shah A., Cacho F.*, Anghel L.
Aging Investigation of Digital Circuits using In-Situ Monitors
IEEE International Integrated Reliability Workshop (IIRW 2019), 2019
**STMicroelectronics*
CI-4 Portolan M., Savino A.*, Leveugle R., Di Carlo S.*, Bosio A., Di Natale G.**
Alternatives to fault injections for early safety/security evaluations
24th IEEE European Test Symposium (ETS 2019), 2019
**Politecnico di Torino, **Ecole Centrale de Lyon*
CI-5 Savino A.*, Portolan M., Leveugle R., Di Carlo S.*
Approximate computing design exploration through data lifetime metrics
24th IEEE European Test Symposium (ETS 2019), 2019
**Politecnico di Torino*

CI-6 Valea E.*, Da Silva M.*, Flottes M.-L.*, Di Natale G., Rouzeyre B.*
Encryption-Based Secure JTAG
IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2019), 2019
**LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*
CI-7 Mosanu S.*, Guo X.*, Anghel L., Stan M.*
Flexi-AES: A Highly-Parameterizable Cipher for a Wide Range of Design Constraints
IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM'2019), 2019
**University of Virginia*
CI-8 Bolchini C.*, Cassano L.*, Montalbano I.*, Reppole G.*, Zanetti A.*, Di Natale G.
HATE: a HArdware Trojan Emulation Environment for Microprocessor-based Systems
IEEE 25th International Symposium on On-Line Testing And Robust System Design (IOLTS'2019), 2019
**Politecnico di Milano*
CI-9 Di Natale G., Vatajelu I., Senthamarai Kannan K., Anghel L.
Hidden-Delay-Fault Sensor for Test, Reliability and Security
IEEE Design Automation and Test Conference in Europe (DATE 2019), 2019
CI-10 Skaf A., Ezzadeen M., Benabdenbi M., Fesquet L.
On-Line Adjustable Precision Computing
Design & Technologies of Integrated Systems (DTIS 2019), 2019
CI-11 Vatajelu I., Di Natale G., Keren O.*, Martin H.**
On the Reliability of the Ring Oscillator Physically Unclonable Functions
IEEE 4th International Verification and Security Workshop (IVSW'2019), pp. 25-30, 2019
**Bar-Ilan University - Faculty of Engineering, **Universidad Carlos III of Madrid - Electronics Technology Department*
CI-12 Valea E.*, Da Silva M.*, Flottes M.-L.*, Di Natale G., Rouzeyre B.*, Dupuis S.*
Providing Confidentiality and Integrity in Ultra Low Power IoT Devices
14th International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS 2019), 2019
**LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*
CI-13 Bosio A.*, Hamdioui S., O'Connor I.*, Rodrigues G.***, Lima F.***, Vatajelu I., Di Natale G., Anghel L., Nagarajan S.***, Fieback M.R.*****
Rebooting Computing: The Challenges for Test and Reliability
IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'2019), pp. 8138-8143, 2019
**Ecole Centrale de Lyon, **Delft University of Technology, ***UFRGS*
CI-14 Damljanovic A.*, Jutman A., Portolan M., Sanchez E.*, Squillero G.*, Tsertov A.****
Simulation-based Equivalence Checking between IEEE 1687 ICL and RTL
International Test Conference (ITC 2019), 2019
**Politecnico di Torino, **Testonica Labs*
CI-15 Vatajelu I., Di Natale G., Anghel L.
Special Session: Reliability of Hardware-Implemented Spiking Neural Networks (SNN)
IEEE VLSI Test Symposium (VTS 2019), 2019
CI-16 Savino A.*, Portolan M., Di Carlo S.*, Leveugle R.
Targeting approximation through data lifetime: a quest for optimization metrics
4th Approximate Computing Workshop (AxC 2019), 2019
**Politecnico di Torino*
CI-17 Ait Said N., Benabdenbi M.
Teaching Hardware/Software co-design using Rocket Chip
RISC V Workshop 2019, 2019
CI-18 Galy P.*, De Conti L.*, Vinet M., Cristoloveanu S.***, Delahaye G., Anghel L.**
Topology and design investigation on thin film silicon BIMOS device for ESD protection in FD-SOI technology
30th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF'2019), 2019
**STMicroelectronics, **CEA-LETI - Laboratoire d'Electronique de Technologie de l'Information, ***IMEP-LAHC*

CDSI

CI-19 Fesquet L., Decoudu Y., Iga R., Ferreira De Paiva Leite T., Rolloff O., Diallo M., Possamai Bastos R., Morin-Allory K., Engels S.*, Engels S.
A Distributed Body-Biasing Strategy for Asynchronous Circuits
27th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2019), 2019
**STMicroelectronics*
CI-20 Skaf A., Ezzadeen M., Benabdenbi M., Fesquet L.
Adjustable Precision Computing Using Redundant Arithmetic
Workshop on Approximate Computing (AxC'2019), 2019
CI-21 Iga R.*, Iga R., Engels S.*, Engels S., Fesquet L.
An Event-Based Strategy for ASK demodulation
5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2019), 2019
**STMicroelectronics*

CI-22 Bidegaray-Fesquet B.*, Fesquet L.
A new synthesis approach for non-uniform filters in the log-scale: proof of concept
5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2019), 2019
**Laboratoire Jean Kuntzmann*

CI-23 El Hadbi A.*, El Hadbi A., Elissati O.*, Fesquet L.
An FPGA Implementation of High-Precision STR-based Time-to-Digital Converter
25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2019), 2019
**STRS Laboratory*

CI-24 Possamai Bastos R., Dutertre J.M.*, Garay Trindade M., Andreoni Camponogara Viera R., Potin O.*, Rey S., Cheymol B.**, Baylac M.****
Assessment of Current Sensor on Chip for Detecting Neutron-Induced Transients via Body Terminals
Conference on Radiation Effects on Components and Systems (RADECS 2019), 2019
**Ecole Nationale Supérieure des Mines de Saint-Etienne , **LPSC - Laboratoire de Physique Subatomique et de Cosmologie*

CI-25 Decoudu Y., Simatic J.*, Alexandre P., Morin-Allory K., Fesquet L.
Comparison of Synchronous and Asynchronous FIR Filter Architecture
5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2019), 2019
**HawAI.Tech*

CI-26 Nastro A.*, Rufer L., Ferrari M.*, Basrour S., Ferrari V.*
Electrical Tuning of the Resonant Frequency of a Piezoelectric Micromachined Acoustic Transducer
Associazione Italiana Sensori e Microsistemi (AISEM 2019), 2019
**University of Brescia*

CI-27 Gassab M., Chebil A., Dridi C., Basrour S.
Electrochemical performance of interdigitated electrodes supercapacitors for embedded systems: simulation and experimental aspects
12th International Workshop on Impedance Spectroscopy (IWIS 2019), 2019

CI-28 Gimenez G.*, Gimenez G., Simatic J., Fesquet L.**
From Signal Transition Graphs to Timing Closure – Application to Bundle-Data Circuits
25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2019), 2019
**IC'ALPS, **HawAI.Tech*

CI-29 Maamer B., Basrour S., Tounsi F.*
Investigation on a Low Frequency Electrostatic Harvester with High Out-of-plane Translation
9th National Days on Energy Harvesting and Storage (JNRSE 2019), 2019
**Ecole Nationale d'Ingenieurs de Sfax (ENIS)*

CI-30 Aquino Guazzelli R., Garay Trindade M., Fesquet L., Possamai Bastos R.
Learning-Based Reliability Assessment Method for Detection of Permanent Faults in Clockless Circuits
30th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2019), 2019

CI-31 Demori M.*, Baù M.*, Ferrari M.*, Basrour S., Rufer L., Ferrari V.*
Mems Device with Piezoelectric Actuators for Driving Mechanical Vortexes in Aqueous Solution Drop
20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII), pp. 2318-2321, 2019
**University of Brescia*

CI-32 Bonnaud O.*, Fesquet L.
Microelectronics at the heart of the digital society: technological and training challenges
34th SBMicro – Symposium on Microelectronics and Devices, 2019
**Institut d'Electronique et de Télécommunications de Rennes, Université de Rennes 1 – Institut National des Sciences Appliquées (INSA Rennes) – SUPELEC, France*

CI-33 Garraud A.*, Debontride G., Blachier D.*, Basrour S., Peyrade D.***
Multiple heater-sensor microsystems on a single glass slide to monitor cell culture temperature
7ème Journées Nationales des Technologies Emergentes Autonomes (JNTE 2019), 2019
**LTM | Laboratoire des technologies de la Microélectronique, **CIME, INPG, Grenoble*

CI-34 Skaf A., Ezzadeen M., Benabdenbi M., Fesquet L.
On-Line Adjustable Precision Computing
Design & Technologies of Integrated Systems (DTIS 2019), 2019

CI-35 Nastro A.*, Rufer L., Ferrari M.*, Basrour S., Ferrari V.*
Piezoelectric Micromachined Acoustic Transducer with Electrically-Tunable Resonant Frequency
20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII), pp. 1905-1908, 2019
**University of Brescia*

CI-36 Bonnaud O.*, Fesquet L., Bsiesy Ah.**
Skilled manpower shortage in microelectronics A challenge for the french education microelectronics network
18th International Conference on Information Technology Based Higher Education and Training (ITHET'2019), pp. 8937384, 2019
**Institut d'Electronique et de Télécommunications de Rennes, Université de Rennes 1 – Institut National des Sciences Appliquées (INSA Rennes) – SUPELEC, France, **LTM | Laboratoire des technologies de la Microélectronique*

CI-37 Sylvestre A.*, Jean-Mistral C., Basrour S., Bellet D.***, Bai J.******
Soft Dielectric Generators for energy harvesting and sensors
Advanced Materials Sciences and Engineering (AMSE 2019), 2019
**Laboratoire de Génie Electrique de Grenoble, **LAMCOS - Laboratoire de Mécanique des Contacts et des Structures, ***LMGP - Laboratoire des Matériaux et du Génie Physique, ****MSSMat - Laboratoire de mécanique des sols, structures et matériaux*

CI-38 Sylvestre A.*, Jean-Mistral C., Basrour S.**
Soft Electroactive Polymers for Energy Harvesting
5th Annual World Congress of Smart Materials (BIT's 2019), 2019
**Laboratoire de Génie Electrique de Grenoble, **LAMCOS - Laboratoire de Mécanique des Contacts et des Structures*

CI-39 Fernandez-Brillet L., Leclaire N., Mancini S., Cleyet-Merle S.*, Nicolas M.*, Henriques J.P.*, Delnondedieu C.*
Speeding-up CNN inference through dimensionality reduction
Design and Architectures for Signal and Image Processing (DASIP 2019), 2019
**STMicroelectronics*

CI-40 Frisch R.*, Frisch R., Faix M.*, Belot J.*, Fesquet L., Mazer E.*
Stochastic sampling machine for Bayesian inference
IEEE International Nanodevices & Computing Conference (INC 2019), 2019
**LIG - Laboratoire d'Informatique de Grenoble*

CI-41 El Hadbi A.*, El Hadbi A., Elissati O.*, Fesquet L.
Time-to-Digital Converters: A Literature Review and New Perspectives
3rd International Nordic-Mediterranean Workshop on Time-to-Digital Converters and Applications (NoMe–TDC 2019), 2019
**STRS Laboratory*

CI-42 Fernandez-Brillet L., Mancini S., Cleyet-Merle S.*, Nicolas M.*
Tunable CNN Compression Through Dimensionality Reduction
IEEE International Conference on Image Processing (ICIP 2019), 2019
**STMicroelectronics*

RMS

CI-43 Malloug H., Barragan M., Mir S.
A 52 dB-SFDR 166 MHz sinusoidal signal generator for mixed-signal BIST applications in 28 nm FDSOI technology
European Test Symposium (ETS 2019), 2019

CI-44 Takam Tchendjou G., Simeu E.
Control Loop of Image Correction based on Detection and Self-Healing of Defective Pixels
25th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS 2019), 2019

CI-45 Takam Tchendjou G., Simeu E.
Defective pixel analysis for Image sensor online diagnostic and self-healing
37th IEEE VLSI Test Symposium (VTS 2019), 2019

CI-46 Chegari B., Tabaa M.*, Moutaouakkil F., Simeu E., Medromi H.*****
Energy savings and thermal comfort benefits of shading devices: case study of a typical moroccan building
4th International Conference on Smart City Applications (ACM 2019), pp. 63, 2019
**LPRI - Laboratoire Pluridisciplinaire de recherche et innovation , **ENSEM - École nationale supérieure d'électricité et mécanique de Casablanca, ***UH2MC - Université Hassan II de Casablanca*

CI-47 Nzebop Ndenoka G.*, Tchuente M.*, Simeu E.
Langage et sémantique des expressions pour la synthèse de modèle Grafcet dans un environnement IDM
Conférence de Recherche en Informatique (CRI 2019), 2019
**Université de Yaoundé I*

CI-48 Barragan M., Leger G.*, Cilici F., Lauga-Larroze E., Bourdel S.**, Mir S.**
On the use of causal feature selection in the context of machine-learning indirect test
Design, Automation & Test in Europe Conference & Exhibition (DATE 2019), pp. 276-279, 2019
**IMSE, Instituto de Microelectronica de Sevilla , **RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits*

CI-49 Tchuani Tchakonte D.*, Simeu E., Tchuente M.*
Optimization of wireless sensor network lifetime for target coverage applications
Conférence de Recherche en Informatique 2019 (CRI 2019), 2019
**Université de Yaoundé I*

CI-50 Silveira Feitoza R., Barragan M., Mir S.
Reduced-Code Techniques for On-Chip Static Linearity Test of SAR ADCs
27th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pp. 263-268, 2019

CI-51 Takam Tchendjou G., Simeu E.
Self-Healing Image Sensor Using Defective Pixel Correction Loop
International Conference on Control, Automation and Diagnosis (ICCAD 2019), 2019

CI-52 Chegari B., Tabaa M.*, Moutaouakkil F., Simeu E., Medromi H.*****
The impact of the thermos-physical parameters of insulation on the energy performance of a building in Morocco
International Conference of Computer Science and Renewable Energies (ICCSRE 2019), pp. 1-6, 2019
**LPRI - Laboratoire Pluridisciplinaire de recherche et innovation , **ENSEM - École nationale supérieure d'électricité et mécanique de Casablanca, ***UH2MC - Université Hassan II de Casablanca*

CI-53 Cilici F., Barragan M., Mir S., Lauga-Larroze E.*, Bourdel S.*, Leger G.**
Yield Recovery of mm-Wave Power Amplifiers using Variable Decoupling Cells and One-Shot Statistical Calibration
IEEE International Symposium on Circuits and Systems (ISCAS 2019), pp. 1-5, 2019
**RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits, **IMSE, Instituto de Microelectronica de Sevilla*

SLS
CI-54 Brignon E., Pierre L.
Assertion-Based Verification through Binary Instrumentation
Design, Automation and Test in Europe (DATE'2019), 2019
CI-55 Alcantara Souza M.*, Cota Freitas H.*, Pétrot F.
Coherence State Awareness in Way-Replacement Algorithms for Multicore Processors
Anais do XX Simpósio em Sistemas Computacionais de Alto Desempenho (WSCAD 2019), pp. 240-251, 2019
**UFMG - Universidade Federal de Minas Gerais*
CI-56 Fernandez-Mesa B.J., Andrade Porras L.-L., Pétrot F.
Electronic System Level Design of Heterogeneous Systems: a Motor Speed Control System Case Study
IEEE International New Circuits and Systems Conference (NEWCAS 2019), 2019
CI-57 Bonicel L., Bohrer R.*, Leprettre B.*, Rousseau F., Pétrot F.
Multi-Triggered Embedded Software Code Generation for Electrical Metering and Protection Applications
Workshop on Rapid System Prototyping (RSP 2019), 2019
**Schneider Electric Industries*
CI-58 Fernandez-Brillet L., Leclaire N., Mancini S., Cleyet-Merle S.*, Nicolas M.*, Henriques J.P.*, Delnondedieu C.*
Speeding-up CNN inference through dimensionality reduction
Design and Architectures for Signal and Image Processing (DASIP 2019), 2019
**STMicroelectronics*
CI-59 Fernandez-Brillet L., Mancini S., Cleyet-Merle S.*, Nicolas M.*
Tunable CNN Compression Through Dimensionality Reduction
IEEE International Conference on Image Processing (ICIP 2019), 2019
**STMicroelectronics*

Book chapters (CH)

AMfoRS
CH-1 Anghel L., Shah R., Cacho F.*
On-Chip Ageing Monitoring and System Adaptation
Ageing of Integrated Circuits: Causes, Effects and Mitigation TechniquesOn-Chip Ageing Monitoring and System Adaptation, pp. 149-180, 2019
**STMicroelectronics*

RIS
CH-2 Ramos P.*, Vargas V.*, Velazco R., Zergainoh N.-E.
Error Rate Prediction of Applications Implemented in Multi-Core and Many-Core Processors
Radiation Effects on Integrated Circuits and Systems for Space Applications, Nature, pp. 145-173, 2019
**Universidad de las Fuerzas Armadas*
CH-3 Vargas V., Ramos P., Méhaut J-F.*, Velazco R.
Improving Reliability of Multi-/Many-Core Processors by Using NMR-MPar Approach
Radiation Effects on Integrated Circuits and Systems for Space Applications, pp. 175-203, 2019
**LIG - Laboratoire d'Informatique de Grenoble*

Books & Edited Publications (L)

CDSI
L-1 Possamai Bastos R., Torres F.S.*
On-Chip Current Sensors for Reliable, Secure, and Low-Power Integrated Circuits
, Springer , 2019
**DFKI - Deutsches Forschungszentrum für Künstliche Intelligenz GmbH*

RIS
L-2 Gizopoulos D.*, Alexandrescu D., Nicolaidis M.**
Guest Editorial: Robust System Design - IEEE International On-Line Testing and Robust System Design Symposium (IOLTS) 2018
IEEE Transactions on Device and Materials Reliability, IEEE, 2019
**DIT, Department of Informatics & Telecommunications , **iROc Technologies*

L-3 Simeu E., Jurimagi L.*, Velazco R.
Proceedings of the 20th Latin-American Test Symposium (LATS 2019)
, IEEE, 2019
**TALTECH - Tallinn University of Technology*
L-4 Velazco R., Mcmorrow D.*, Estela J.**
Radiation Effects on Integrated Circuits and Systems for Space Applications
, Springer , 2019
**Naval Research Laboratory, **Spectrum Aeropace Group*

RMS
L-5 Simeu E., Jurimagi L.*, Velazco R.
Proceedings of the 20th Latin-American Test Symposium (LATS 2019)
, IEEE, 2019
**TALTECH - Tallinn University of Technology*

National journals (RN)

AMfoRS
RN-1 Ait Said N., Benabdenbi M., Villanova Novaes Magalhaes G.
Prototypage Matériel-Logiciel de Systèmes Intégrés avec l'architecture RISC-V
J3eA – Journal sur l'enseignement des sciences et technologies de l'information et des systèmes, Volume: 18, 2019

National conferences (CN)

AMfoRS
CN-1 Ait Said N., Benabdenbi M.
LearnV: A Hardware/Software RISC V Based platform for Research and Education
Colloque National du GDR SoC2 2019, 2019
CN-2 Andrade Porras L.-L., Benabdenbi M., Muller O., Rousseau F., Pétrot F.
Teaching basic computer architecture, assembly language programming, and operating system design using RISC-V
RISC V week 2019, 2019

CDSI
CN-3 Fernandez-Brillet L., Mancini S., Cleyet-Merle S.*, Nicolas M.*
Compression adaptative des CNNs par réduction de la dimensionnalité
XXVIIème Colloque francophone de traitement du signal et des images (GRETSI 2019), 2019
**STMicroelectronics*

RMS
CN-4 Margalef-Rovira M., Barragan M., Pistono E.*, Bourdel S.*, Ferrari P.*
Conception de déphaseurs RTPS faible consommation en bande millimétrique
21èmes Journées Nationales Micro-ondes (JNM 2019), 2019
**RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits*
CN-5 Silveira Feitoza R., Barragan M., Dzahini D., Mir S.
Static linearity test of SAR ADCs using an embedded incremental ΣΔ converter
Journées Nationales du Réseau Doctoral en Micro-nanoélectronique (JNRDM 2019), 2019

SLS
CN-6 Fernandez-Brillet L., Mancini S., Cleyet-Merle S.*, Nicolas M.*
Compression adaptative des CNNs par réduction de la dimensionnalité
XXVIIème Colloque francophone de traitement du signal et des images (GRETSI 2019), 2019
**STMicroelectronics*
CN-7 Andrade Porras L.-L., Benabdenbi M., Muller O., Rousseau F., Pétrot F.
Teaching basic computer architecture, assembly language programming, and operating system design using RISC-V
RISC V week 2019, 2019

Other communications (O)

AMfoRS

O-1 Portolan M., Cantoro R.*, Sanchez E.*
A Functional Approach to Test and Debug of IEEE 1687 Reconfigurable Networks
European Test Symposium (ETS 2019), Baden Baden, GERMANY
**Politecnico di Torino*

O-2 Vatajelu I., Di Natale G.
High-Entropy STT-MTJ-based TRNG
8th Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE'2019), Baden Baden, GERMANY

O-3 Eggersglüß S.*, Hamdioui S., Jutman A.***, Michael M.K.****, Raik J.*****, Sonza Reorda M.******, Tahoori M.*******, Vatajelu I.**
IEEE European Test Symposium (ETS)
IEEE International Test Conference (ITC'2019), Washington DC, UNITED STATES, DOI: 10.1109/ITC44170.2019.9000148
**Mentor Graphics Corp., **Delft University of Technology, ***Testonica Labs, ****University of Cyprus, *****TALTECH - Tallinn University of Technology, ******Politecnico di Torino, *******Karlsruhe Institute of Technology*

O-4 Valea E.*, Flottes M.-L.*, Di Natale G., Rouzeyre B.*
Stream Cipher Based Encryption in IEEE Test Standards
8th Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE 2019), Baden Baden, GERMANY
**LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*

RMS

O-5 Kriekouki I., Camirand Lemyre J.*, Rochette S.*, Rohrbacher C.*, Drouin D.*, Barragan M., Mir S., Galy P., Pioro-Ladrière M.***
UTBB FD-SOI Technology for Silicon-based Quantum Dots and Cryo-CMOS Electronics
Silicon Quantum Electronics Workshop (SIQEW'2019), San Sebastian, SPAIN
**Université de Sherbrooke, **STMicroelectronics*

Softwares (S)

CDSI

1 Gimenez G., Simatic J., Fesquet L.
Static Timing Analysis of Bundled-Data Circuits, Mar 11, 2019

Theses (T)

CDSI

T-1 Bertrand Fra.
Design flow and formal models for desynchronization of synchronous circuits (confidential thesis - unavailable online)
These de Doctorat, Université Grenoble Alpes, spécialité "Microélectronique", Jul 02, 2019

T-2 El Hadbi A.
Time-to-digital Conversion based on a Self-Timed Ring Oscillator
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Nov 20, 2019

T-3 Ferreira De Paiva Leite T.
FD-SOI technology opportunities for more energy efficient asynchronous circuits
These de Doctorat, Université de Grenoble, spécialité "Nanoélectronique et Nanotechnologies", Jan 21, 2019

T-4 Frisch R.
Stochastic machines dedicated to Bayesian inference for source localization and separation
These de Doctorat, Université Grenoble Alpes, spécialité "Informatique", Nov 14, 2019

T-5 Germain S.
Electromagnetic spectrum control of asynchronous digital circuits
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Nov 25, 2019

T-6 Kalsing A.
Power-Intent Management During RTL Optimizations (confidential thesis - unavavaible online)
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Jul 11, 2019

T-7 Popescu A.
On control approaches for estimation purposes - Application to tunneling current and magnetic levitation processes
These de Doctorat, Université Grenoble Alpes, spécialité " Systèmes Automatiques et Microélectroniques", Nov 25, 2019

T-8 Rolloff O.
Distributed Body-Bias Micro-Generators for an activity-driven power management in FD-SOI Technologies
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Dec 03, 2019

RIS

T-9 Coelho A.
Fault Tolerance and Reliability for Partially Connected 3D Networks-on-Chip
These de Doctorat, Université Grenoble Alpes, spécialité "Electronique, électrotechnique, automatique", Oct 25, 2019

RMS

T-10 Barragan M.
Built-In Self-Test solutions for high-performance and reliable analog, mixed-signal, and RF integrated circuits
HDR, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Jul 09, 2019
T-11 Cilici F.
Development of Built-In Self-Test solutions for RF/mm-wave integrated circuits
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Dec 17, 2019
T-12 Tchuani Tchakonte D.
Minimization of energy consumption of sensor networks in target coverage applications
These de Doctorat, Université Grenoble Alpes, spécialité "", Jul 19, 2019

SLS

T-13 Christodoulis G.
Adapting a HPC runtime system to FPGAs
These de Doctorat, Université Grenoble Alpes, spécialité "", Dec 05, 2019

Press review

Interview of Laurent FESQUET (Associate Professor at TIMA Laboratory)

(from Mina-News magazine – February 2019)

ENTRETIEN

LAURENT FESQUET,
chercheur à TIMA

"Rebooting Computing remet en cause tous les principes des ordinateurs"

MINA-NEWS : Avec la conférence ICRC* d'avril à Grenoble *(lire ci-contre)*, les participants vont découvrir l'initiative *Rebooting Computing* lancée aux Etats-Unis en 2016. De quoi s'agit-il ?

Laurent Fesquet : Nous voulons repenser la façon de concevoir les ordinateurs. Aujourd'hui, la plupart des machines sont basées sur une architecture Von Neumann. Cette dernière a été inventée en 1945 pour effectuer du calcul exact, ce qui est très énergivore. Aujourd'hui d'autres approches plus économes voient le jour : réseaux de neurones, calcul approché, architecture probabiliste ou quantique…

MINA-NEWS : Et la technologie ouvre de nouvelles pistes…

LF : Exactement. Intel a présenté en 2018 sa puce neuromorphique Loihi, qui compte 130 000 neurones, un chiffre jamais atteint. Les avancées de la micro-électronique permettent la réalisation de réseaux de neurones très denses. On peut aussi évoquer les premiers ordinateurs quantiques, ou l'avènement des nanocomposants : ils ouvrent des perspectives pour le calcul au plus près des mémoires, ou la manipulation de distributions statistiques pour le calcul probabiliste.

MINA-NEWS: Sur quel sujet travaillez-vous à TIMA ?

LF : Nous développons des circuits sans horloge, dits asynchrones. Par exemple, un réseau de neurones asynchrone consomme moins que son homologue synchrone, car seuls les neurones utiles au calcul sont activés. La puce d'Intel fonctionne sur ce principe. À ICRC, je présenterai des travaux qui marient technologie asynchrone et calcul probabiliste afin de concevoir un ordinateur probabiliste. Ils sont le fruit d'une collaboration avec des collègues du LIG (Laboratoire d'informatique de Grenoble). ■

**International Conference on Rebooting Computing*

laurent.fesquet@univ-grenoble-alpes.fr

TIMA Laboratory

46 avenue Félix Viallet
38031 GRENOBLE Cedex 1
FRANCE

Tel: +33 (0)4 76 57 45 86
E-mail: directeur-tima@univ-grenoble-alpes.fr

http://tima.univ-grenoble-alpes.fr

→ https://www.linkedin.com/company/tima-laboratory/**follow us**