TIMA Laboratory

2021

Annual report

Contents

TIMA's staff

Since 01/01/2021

Giorgio DI NATALE
Director

Laurent FESQUET
Deputy Director

Administrative and Financial pole

Anne-Laure FOURNERET
Manager - Human resources - Special events - Communication

Laurence BEN TITO
Executive & laboratory assistant - Publications

Mathilde GARÇON
Budgets, contracts

Aurore GAYRAUD
Teams finance administrator

Youness RAJAB
Teams finance administrator - Common expenses administrator

Computer Service

Frédéric CHEVROT
Manager - Systems, networks and park manager

Nicolas GARNIER
Systems, networks and park manager

Ahmed KHALID
Computer park manager

Development Service

Alice DE BIGNICOURT
Development engineer, webmaster

Mamadou DIALLO
Development engineer

Foreword

TIMA Laboratory is a joint research laboratory between the Centre National de la Recherche Scientifique (CNRS), the Grenoble Institute of Technology (Grenoble INP) and the Université Grenoble Alpes (UGA).

TIMA addresses some of the most urgent and ambitious challenges related to the design of integrated circuits and Systems-on-chip (SoC). The research activities cover the specification, design, verification, test, CAD tools and design methods for integrated systems, including analog and digital components, smart sensors and actuators, up to multiprocessor SoCs together with their operating system. More in particular, researchers at TIMA cover the following topics:

- Low power design
- Asynchronous design
- New sampling and data processing techniques
- MEMS, Smart Sensors and Actuators
- Design of AMS/RF/mmW devices, circuits and systems
- Modeling, control and calibration of AMS/RF devices, circuits and systems
- Robustness, reliability and test
- Hardware security and embedded trust
- New hardware computing and digital design
- Hardware/Software co-design
- Simulation and verification
- Embedded AI

The laboratory is structured in the following four research teams:

Architectures and Methods for Resilient Systems (AMfoRS): Robustness and dependability evaluations of embedded systems; Hardened and robust architecture; Design for reliability with respect to variability, aging, and soft errors; Modeling, analysis and testing at the system level; Hardware security and embedded trust; New computational approaches and technologies

Circuits, Devices and System Integration (CDSI): Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

Reliable RF and Mixed-signal Systems (RMS): Design for test of analog, mixed-signal and RF circuits; Estimation of test metrics; Calibration of RF devices; Embedded control for efficient energy management; Prediction and control of quality and energy management; High-level modeling of heterogeneous and multi-physic systems

System Level Synthesis (SLS): Highly efficient architectures for general purpose computing or AI-dedicated algorithms; system-level modeling and design methodology (specification, simulation and verification of hardware/software systems on chip); design exploration and synthesis of hardware

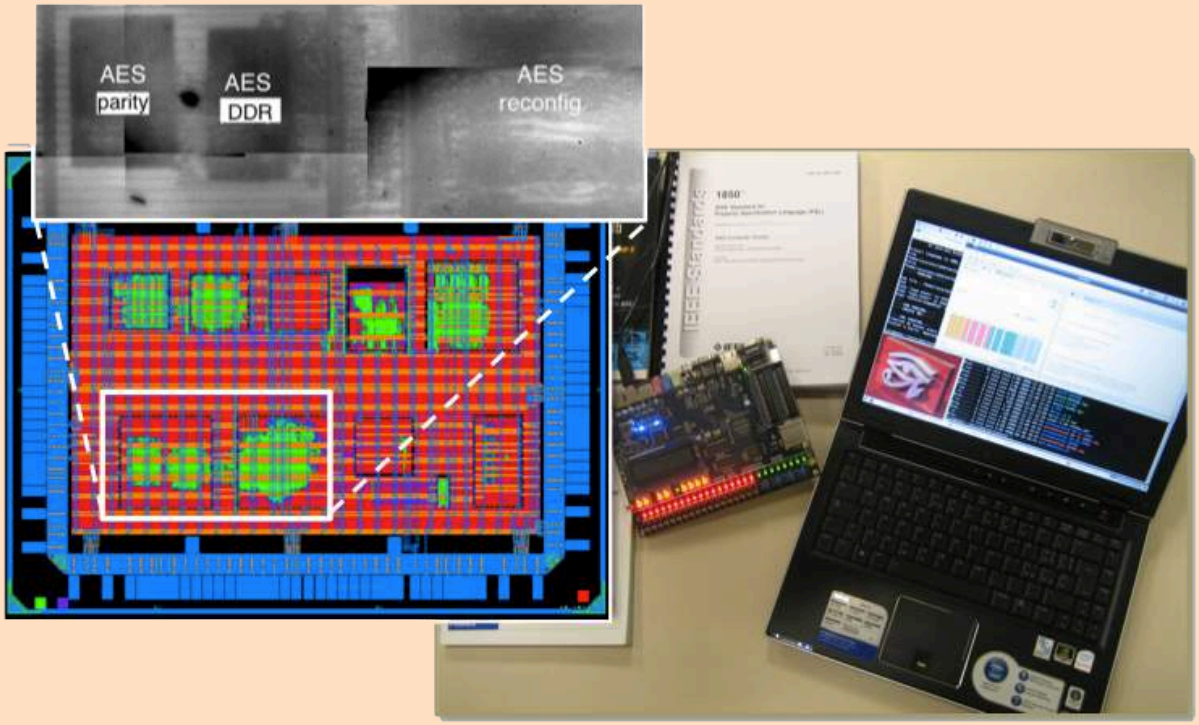
TIMA takes an active part in the organization of the Grenoble Alpes research community, being linked to the poles "Mathematics, Informatics and Communication" (MSTIC) and "Physics, Engineering and Materials" (PEM). TIMA is also a member of the Carnot Institute LSI, the Laboratory of Excellence Persyval and the local federation of micro and nanoelectronics laboratories FMNT.

The 2021 edition of the TIMA annual report presents a brief and synthetic presentation of the scientific achievements of each research team.

Giorgio DI NATALE
Director

CNRS - Grenoble INP - UGA

AMfoRS team



Architectures and Methods for Resilient Systems

Architectures and Methods for Resilient Systems (AMfoRS team)

http://tima.univ-grenoble-alpes.fr/tima/fr/amfors/amforsoverview.html

The **AMfoRS** team addresses dependability and trust of digital systems at multiple abstraction levels for specific application domains (e.g., automotive, avionics, smartcards, IoT), by guaranteeing that digital circuits possess properties such as quality, reliability, safety, security, availability. The work of the team is focused on design and analysis methods, techniques and tools to assess and improve circuits dependability and trust, for the above-mentioned domains.

Research activities

Robustness and dependability

Many domains have functional safety among the classical list of design constraints e.g., ISO 26262 standard in automotive. Our work aims at improving **early evaluations of dependability** w.r.t. errors induced by environmental disturbances. The goal, to reduce development and production costs, is to be able to evaluate accurately and at an early stage of the design the potential functional effects of soft and permanent errors. We have recently proposed a **cross-layer fault simulation method** to perform the robustness evaluation of critical embedded systems, based on fault injections in both Transaction Level Model (TLM) and Register Transfer Level (RTL) descriptions to make a trade-off between simulation time and realism of the simulated high level faulty behaviors, Another important characteristic of the approach is taking into account the global system specifications in order to discriminate actually critical faults from faults leading to effects with no real consequences on the system behavior. The approach has been applied to an airborne case study. In 2021, the approach has been improved with an iterative flow allowing both the global reduction of the fault injection durations and the improvement of the TLM models along the iterations in order to achieve a good correlation between the consequences of faults injected at TLM and RTL levels.

Another study started in 2021 aims at better evaluating (and predicting) the impact of the software workload on the dependability of complex digital components such as microcontrollers and SoCs. Ultimately, one goal is to define a set of representative benchmarks, allowing a dependability evaluation on critical systems before the actual application program is available. The first step was to develop a versatile profiling tool based on a virtual platform adapted to many processors, coresponding to a modified version of QEMU. This analysis flow has been applied on the RISC-V target and Mibench softwares, allowing us to better understand the impact of software load on SoC fault tolerance. Our proposed metric called “Likelihood Percentage” demonstrated that a high level evaluation with our tool can be very efficient to obtain significant information on program behaviour, coherent with results obtained from both a reference instruction set simulator and a hardware architecture. We have also shown that our profiling tool allows us to compare the behaviour of several programs and exhibits specific characteristics. This data helps in understanding how the processor architecture will be used for each application and therefore what level of fault tolerance can be expected depending on the software load. We formulated three hypotheses that will have to be confirmed with more program examples, the use of several hardware platforms and finally actual tests under particle beams.

In the field of automatic quality or safety assurance level evaluation, we have proposed the first approach towards the automation of the extraction processes of both the valid and faulty state machines within a System-on-a-Chip. The data automatically extracted by this method is a relevant input for behavioural modelization and FMEA (Failure Modes and Effects Analysis) analysis. The method is based on a semi-automated approach for the systematic extraction of failure modes of a digital design in the hypothesis of a single-event upset (SEU) or stuck-at in flip-flops. This procedure aims to enhance human driven failure analysis and provide inputs for RAMS (Reliability, Availability, Maintainability, and Safety) frameworks in the process of quality assurance of complex devices. The main objective is to transport and apply RAMS methods and tools in the area of SoCs design. Experimental results have been conducted on an I2C - AHB system, laying the base for a complete and more complex analysis on an entire SoC [CI3]

Due to technology scaling and transistor size getting smaller and closer to atomic size, the last generation of CMOS technologies presents more variability in various physical parameters. Moreover, circuit wear-out degradation leads to additional temporal variations, potentially resulting in timing and functional failures. To handle such problems, one conventional method consists in providing more safety margins (also called guard bands) at design-time. Therefore, the usage of delay violation **monitors** becomes a must. Placing the monitors is a critical task as the designer has to carefully select the place that will age the most and may become a potential point of failure in a given design.

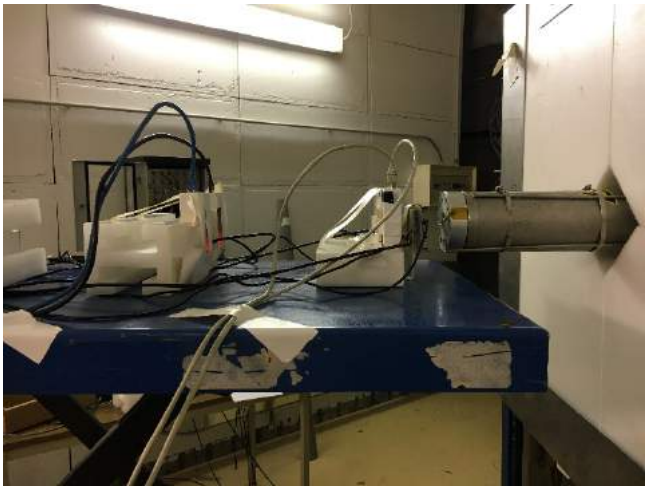
We have explored the use of **Machine Learning techniques** in order to drive the automated selection of potential insertion points of such monitors. Digital delay analysis of basic gates using multiple linear regression has been modeled, predicted, and validated against original data using spice simulation. We have compared multiple linear regression algorithms and used them to study the aging mechanism of CMOS basic gates using supervised learning algorithms. We have showed how it is possible to reliably estimate activity-related path aging and tune the prediction framework by extracting activity profiles from simulations on a synthesized design, which allows a finer grain estimation by obtaining activity profiles at both the path and gate-level.

High-energy particle radiation effects in computing systems

In space environments, aviation altitudes, and ground levels, computing systems' components are liable to high-energy particle radiation-induced transient, accumulative, permanent, and destructive effects. At atmospheric altitudes, for example, neutron environment is primarily responsible for inducing radiation-induced transient effects in avionics and their computing systems. Moreover, the advent of artificial intelligence (AI) systems further extends the computing system applications with self-driving cars, climate-smart agriculture technologies, intelligent medical devices, autonomous monitoring robots/drones, nanosatellites, and spacecraft, making them even more ubiquitous. Within the new era of autonomous things, AI computing solutions are being developed also for the edge of applications, close to sensors, in order to minimize data transfer to/from the cloud and reduce related risks in case of unavailable connections. On the other hand, edge computing is normally resource-constrained in terms of latency, power, and memory, demanding the development of tiny and also reliable machine learning (ML) systems.

In this context, our recent works have assessed and compared the effectiveness of three prominent ML algorithms for tiny ML computing systems in tolerating neutron-induced soft errors. Radiation test-based results suggest that the case-study ML algorithms retain a certain intrinsic level of effectiveness in tolerating neutron effects even thought without any mitigation technique. Notably, random forest algorithm has performed no misclassification during different radiation testing campaigns carried out with 14-MeV and thermal neutron beams.

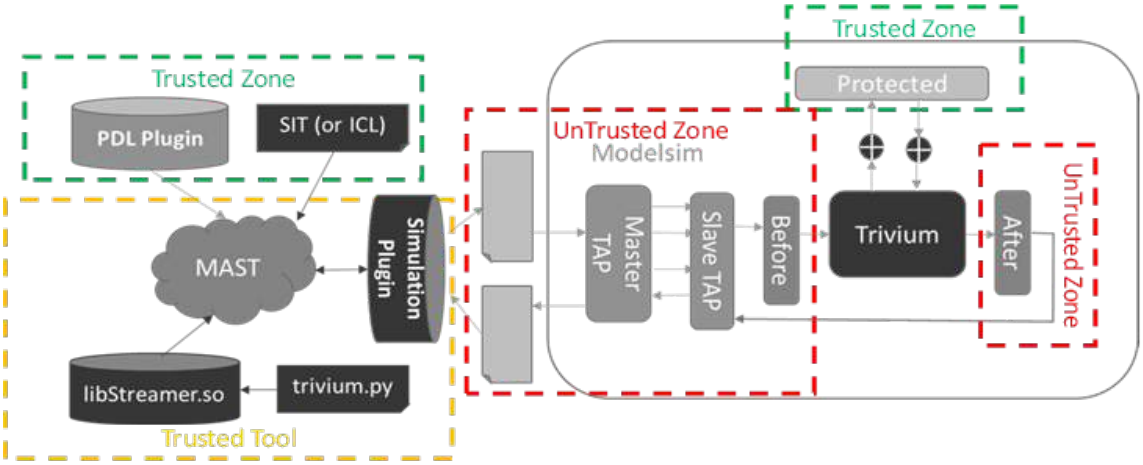
Furthermore, we have also recently assessed neutron radiation effects on the attitude estimation (AE) processing typically embedded in inertial navigation systems (INS) and modern autonomous things. Findings highlight the importance of radiation-induced critical failures that are able to upset INS embedding AE processing modules. Radiation tests were conducted running three strategies for computing different advanced AE algorithms on a case-study processing module exposed to 14-MeV neutron and thermal neutron radiation. Results and analysis suggest that the contribution of radiation-induced soft errors to be mitigated on the AE processing modules is essentially related to single event functional interrupts that can lead inertial navigation to critical failures.



TIMA is also participating of NASA/GFSC's SET program (https://lws-set.gsfc.nasa.gov/) since 2005. The experimental FPGA-based board called COTS-2, devised and designed at TIMA, was included in the NASA/GFSC's SET payload, embedded in the AFRL's DSX spacecraft that was successfully launched on June 25, 2019 at the NASA's Kennedy Space Center (Florida, USA). The DSX spacecraft was in operation until May 31, 2021, weekly providing data to TIMA researchers since June 2019. The NASA/GFSC's SET payload aimed at getting experimental data to study how to better protect satellites/spacecraft against effects of energetic radiation particles present at a medium Earth orbit (MEO) of space, operating around Earth between 6000 km and 12000 km above sea level. The TIMA's COTS-2 board includes an SRAM-based FPGA in which the implemented computing system design was protected by using a classical state-of-the-art fault-tolerance scheme based on Triple Modular Redundancy (TMR). First spaceflight results provide experimental evidences of the risks of using TMR-based schemes in COTS FPGAs operating within MEO.

System-level test and standards

The IEEE 1687-2014 standard and its evolutions like the IEEE P1687.1 (under development) propose solutions for the access and usage of Embedded Instruments, but Electronic Design Automation (EDA) is still limited to only a small subset of the new features. In this context we have improved our innovative Test Flow and Environment called **"Manager for SoC Test" (MAST)**, a software backend able to provide features and performance superior to the industrial legacy solutions. We have proposed innovative solutions that exploits the dynamic nature of the standard to integrate Security features directly into the flow. Our framework extends MAST with novel solutions developed within the team, namely Stream cyphers and Dynamic authentication. We were notably able to integrate Scan Encryption directly inside the EDA tool, allowing Encryption to be natively integrated as a P1687.1 element and be freely mixed inside the Design-of-Test (DfT) infrastructure while retaining full interactive capabilities, while legacy solutions are limited to top-level encryption with offline processing. We then merged this new feature with the ongoing work on Scan Authentication, obtaining the Encryption SIB (eSIB, see Hardware Security and Trust), an Authentication-based Secure Access framework able to provide a trusted, configurable, efficient, and transparent interface to the test infrastructure depending on user-defined security levels. Security-wise, secret sharing is limited to a minimum; from a performance point of view, the tool fully leverages its strength in terms of topology resolution and concurrent execution. Last but not least, we are able to clearly separate the system in Trusted and Untrusted areas, providing an optimal user experience, as se curity is handled automatically and transparently.



Hardware security

The team works on the design of cryptographic/secure primitives, and the analysis of security threats, by proposing effective countermeasures. We work on algorithms, schemes, and protocols. We have improved our Authenticated and Secure access to the test infrastructure by presenting the **Encryption SIB**, which provides segment-level confidentiality thanks to the dynamic topology supported by our MAST tool (see System-Level test). Our framework not only supports secure procedures such as user authentication or data encryption, but provides these functionalities with a flexible approach that is totally transparent to the user. We also evaluate the resistance of post-quantum cryptography algorithms against physical attacks, which is necessary besides their theoretical evaluation by cryptanalysis. We highlighted a weakness in the Classic McEliece cryptosystem, which can be attacked by laser fault injection. We are working right now on extending this attack to rely only on side-channel analysis, which incurs a much less restrictive attacker model.

Concerning the security threats, we work regularly on implementation attacks. In 2021, we have improved our experimental platform for **physical attacks** on embedded systems. We have acquired the equipment for active EM fault injection and we are currently building a motorized stage to perform extensive experimental campaigns, thanks to the partial support by CNRS (INS2I) and UGA. We have also worked on an emulation platform on FPGA, aimed at evaluating the effects of EM Fault Injection (EMFI) early in the design flow without the need of either EMFI equipment, nor the final ASIC implementation. In an effort to generalize the characterization of fault attacks on complex systems such as CPUs and microcontrollers, we have started working on a **Cross-Layer Methodology** aiming

at understanding and modelling the fault occurrence mechanisms within the microarchitecture of modern processors, and map this model to upper levels with the final goal of designing optimal countermeasures.
We have addressed the problem of cache timing attacks, which have become very popular in recent years. Eviction set construction is a common step for many such attacks, and algorithms for building them are evolving rapidly. On the other hand, countermeasures are also being actively researched and developed. However, most countermeasures have been designed to secure last-level caches and few of them actually protect the entire memory hierarchy. Cache randomization is a well-known mitigation technique against cache attacks that has a low-performance overhead. We have proposed solutions to determine whether address randomization on first-level caches is worth considering from a security perspective. The work included the implementation of a noise-free cache simulation framework that enables the analysis of the behavior of eviction set construction algorithms. We show that randomization at the first level of caches (L1) brings about improvements in security but is not sufficient to mitigate all known algorithms, such as the recently developed Prime–Prune–Probe technique [CI-14]
In the same context, a study has first shown that Intel mitigations to avoid attacks against secure enclaves (SGX) can be efficient, but not sufficient in all attack scenarios. We have also evaluated the feasibility of the Prime&Probe attack on a system with the CVA6 RISC-V processor. With a bare-metal implementation, it has been shown that the attack works, although a noticeable effort was necessary in terms of reverse engineering of the cache accesses and analysis of the behavior. An attack considered as “turnkey” is not so easy to implement, even without mitigations. Adding additional processes as perturbators, the attack is more complex but still succeeds after analysis of the cache behavior. Currently, work is on-going with the attack implemented under Linux.
In the context of **Control Flow Hardening**, we have proposed the use of nonlinear codes. Hardware-based control flow monitoring techniques enable to detect both errors in the control flow and the instruction stream being executed on a processor. However, these techniques may fail to detect malicious carefully tuned manipulation of the instruction stream in a basic block. We have shown how using a non-linear encoder and checker can cope with this weakness [RI-8]

Hardware trust

The quest of low production cost and short time-to- market, as well as the complexity of modern integrated circuits pushed towards a globalization of the supply chain of silicon devices. Such production paradigm raised a number of trust threats. We are actively working on the proposition of novel solutions to address this problem. In particular, we are proposing novel methods, architectures and protocols for the identification and authentication of hardware devices based on Physically Unclonable Functions (PUFs), as well as mitigation techniques for Hardware Trojans.

Concerning the PUFs, we have proposed: (i) an experimental platform for the evaluation of SRAM-based PUFs; (ii) a theoretical method for the assessment of the reliability of PUFs; (iii) the use of emerging technologies (resistive and magnetic memories) as building block for new PUF architectures; (iv) a novel concept for the enrollment of strong PUF based on machine learning; (v) a new protocol for key exchange which does not require cryptographic primitives [CI-8] [O-1]
In the context of Hardware Trojans (HTs), we worked on the use of software obfuscation to protect systems against HTs that aim at stealing information from the microprocessor while it is executing a program. The method is enhanced by a Genetic Algorithm-based approach to optimize the obfuscation level while minimizing the introduced overhead. We proved the effectiveness and efficiency of the proposed methodology on the Ariane 64bit RISC-V microprocessor running a set of MiBench benchmarks and cryptographic programs.
We also proposed an HT attack for analog circuits, in the context of Systems-on-Chip (SoCs) comprising both digital and analog Intellectual Property (IP) blocks. The HT trigger is placed inside a dense digital IP block where it can be effectively hidden, whereas the HT payload is in the form of a digital pattern transported via the test bus or generated within the test bus, reaching the Design-for-Test (DfT) or programmability interface of the victim analog IP with the test bus. The HT payload unexpectedly activates the DfT and sets the victim analog IP into some possibly partial and undocumented test mode or changes the nominal programmability [RI-3].

New hardware computing approaches

Today's computing systems are facing several issues related to architectural and technological limitations. To mitigate these issues, novel computing paradigms, such as **Computing-in-Memory**, **Neuromorphic Computing** and **Approximate Computing**, are being researched, in conjunction with novel emerging technologies such as memristive and spintronic devices. Concerning these devices, our research aims at using enhanced compact models to perform failure analysis, and define pertinent fault models to establish design-for-test and design-for-reliability methodologies. Concerning the Computing-in-Memory paradigm, we are investigating feasible design solutions, with a special focus on applications for security [CI-10] [CI-13]. Concerning Neuromorphic Computing, we are focusing on the design of efficient Spiking Neural Networks with on-line unsupervised learning and the reliability analysis and test of such networks. Concerning the Approximate Computing paradigm, which has been gaining momentum both in the industry and in academia, we are studying the trade-offs between selective approximation (or occasional violation of specifications) and power consumption. We have focused on Floating Point dynamic approximation, with an impact evaluated i) at algorithm and application level and ii) at hardware level with the design of a configurable FPU ([RI-2] and [RI-9]) . We are also working on an extension of a tool initially developed for dependability evaluation (EARS) in order to identify from RTL descriptions the operators that are the less sensitive to approximations for a given application. In 2021, EARS has been modified to include new metrics and also to better link the multi-bit elements in the RTL description (e.g., operators) to the analysis results. Several benchmarks have also been prepared; the next step is to compare the results of EARS with the results of the manual benchmarks analyses.

Involvement in research activities:

- Participation to the IEEE P1687.1 Working Group
- Participation to the Grenoble Alpes CyberSecurity Institute
- Chair of TTTC – IEEE Computer Society
- Chair of TTEP Educational Program of TTTC
- In charge of Microelectronics within FMNT

Platforms and demonstrators:

- A comprehensive platform for hardware/software co-design based on the RISC-V processor architecture. The platform supports several RISC-V implementations (such as the Rocket Chip or CVA6) and it features high modularity and tuning capabilities (https://tima-amfors.gricad-pages.univ-grenoble-alpes.fr/learnv/).
- Hardware demonstrator for Secure Access to 1687 Test Infrastructure
- Experimental platforms for Physical Attacks and PUF evaluation
- Emulation platform for EM Fault Injection
- Accelerated radiation testing platform for assessing computing systems under high-energy neutron radiation effects

Recent highlights

International Cooperations

MultiRad: Evaluation of Space-to-Ground Radiation Effects in Multicore Computing Systems for Safety-Critical Applications
Scientific Manager: POSSAMAI BASTOS
Partners: Loughborough University (LU), Universidad de Alicante (UA, Spain), Pontifícia Universidade Católica do Rio Grande do Sul (PUCRS), Universidade Federal do Rio Grande do Sul (UFRGS), Universidade Federal de Santa Maria (UFSM)
City: Loughborough, Alicante, Porto Alegre, Santa Maria
Country: UNITED KINGDOM, SPAIN, and BRAZIL
Start the: Jul 01, 2020 until Dec 31, 2023

Physically Unclonable Functions and Identification of Hardware Devices based on Sensors and Switching Activity
Scientific Manager: DI NATALE Giorgio
Partners: University of Madrid
City: Madrid
Country: SPAIN
Start the: Jan 01, 2015 until Dec 31, 2021

Low-cost Zero-latency AMD-based Control Flow Checker for 32/64-bit Architectures
Scientific Manager: DI NATALE Giorgio
Partners: Bar-Ilan University
City: Tel-Aviv
Country: ISRAEL
Start the: Jan 01, 2018 until Dec 31, 2021

Hardware Trojan Horses detection in microprocessors through software Obfuscation
Scientific Manager: DI NATALE Giorgio
Partners: Politecnico di Milano
City: Milano
Country: ITALY
Start the: Jan 01, 2019 until Dec 31, 2021

Physical attacks on Error-Correcting Codes-based Cryptosystems
Scientific Manager: COLOMBIER Brice
Partners: Aurel Vlaicu University
City: Arad
Country: ROMANIA
Start the: Sep 01, 2020 until Dec 31, 2021

Awards and distinctions

May 17, 2021: Outstanding service to the EDA community as General Chair (DATE 2020)
IEEE Council on EDA Outstanding Service Recognition to Giorgio DI NATALE for outstanding service to the EDA community as DATE General Chair in 2020

Academic and research members

Mounir BENABDENBI

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Brice COLOMBIER

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Giorgio DI NATALE

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team
Director of TIMA Lab. Since 01/01/2021

Régis LEVEUGLE

Position
Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Paolo MAISTRI

Position
Researcher at CNRS

Responsibilities
Leader of AMfoRS team
Researcher in AMfoRS team

Mihail NICOLAIDIS

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team

Michele PORTOLAN

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Rodrigo POSSAMAI BASTOS

Position
Associate Professor at UGA - IM2AG school

Responsibilities
Researcher in AMfoRS team

Elena-Ioana VATAJELU

Position
Researcher at CNRS

Responsibilities
Researcher in AMfoRS team

Raoul VELAZCO

Position
Professor Emeritus at CNRS

Responsibilities
Emeritus Research Director in AMfoRS team

Nacer-Eddine ZERGAINOH

Position
Associate Professor at UGA - POLYTECH school

Responsibilities
Researcher in AMfoRS team

CNRS (French National Center for Scientific Research)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AIT SAID Noureddine
Title of thesis: **Toward Floating-Point Run-time Variable Precision in CPU-based Architectures**
Completed on: **November 24th, 2021**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

2. ALI POUR Amir
Title of thesis: **PUF based Secure Computing for Constraint Cyber Physical Object**
Expected date of defence: **2022/2023**
Previous degrees: Engineer (2020)

3. ALSHAER Ihab
Title of thesis: **Cross-Layer Fault Analysis for Microprocessor Architectures (CLAM)**
Expected date of defence: **2023**
Previous degrees: Engineer

4. BORDES Nicolas
Title of thesis: **Security of symmetric primitives and their implementations**
Completed on: **December 9th, 2021**
Previous degrees: Engineer

5. CINÇON Valérian
Title of thesis: **Ultra low power integration of neuro-morphic systems on FD-SOI**
Thesis stopped on: **October 25th, 2021**
Previous degrees: Engineer – Grenoble INP - Phelma, Grenoble - France (2018)

6. DADDINOUNOU Salah
Title of thesis: **Test and reliability of emerging memory-based spiking neural networks**
Expected date of defence: **2023**
Previous degrees: Engineer - Université Paris-Sud Orsay Paris FRANCE (2019)

7. FIORUCCI Tiziano
Title of thesis: **Qualification methodology for ISO26262 certification of automotive SoC systems**
Expected date of defence: **2023**
Previous degrees: Engineer - Università degli Studi di Roma Tor Vergata, Roma – Italy (2019)

8. GARAY TRINDADE Matheus
Title of thesis: **Assessment of Edge Machine-Learning Systems under Radiation-Induced Effects**
Completed on: **September 30th, 2021**
Previous degrees: Engineer – Universidade Federal de Santa Maria, Rio Grande do Sul, Brazil (2017)

9. GERBAUD Merlin
Title of thesis: **Hardware Security Techniques for Cryptographic Algorithms taking advantage of In-Memory Computing**
Expected date of defence: **2023**
Previous degrees: Engineer - Grenoble INP - Esisar, Valence - France

10.INGLESE Pietro
Title of thesis: **Exploration of security threats in In-Memory Computing Paradigms**
Expected date of defence: **2023**
Previous degrees: Engineer – Politecnico di Torino, Italy (2019)

11. JAAMOUN Amine
Title of thesis: **Strategies for securing a memory hierarchy against software side channel attacks**
Expected date of defence: **2022/2023**
Previous degrees: Master 2 Systèmes électroniques et systèmes informatiques – Université Pierre et Marie Curie Paris 6 (2020)

12. KRAEMER SARZI SARTORI Tarso
Title of thesis: **Mitigation of radiation effects on the attitude estimation processing of autonomous things**
Expected date of defence: **2023**
Previous degrees: Engineer – Aerospace engineering – Federal University of Santa Maria, Brazil (2020)

13. LINARES Antoine
Title of thesis: **Flexible Hardware for Intrinsic Secure computing**
Thesis stopped on: **December 15th, 2021**
Previous degrees: Engineer

14. MARTINOLI Valentin
Title of thesis: **Secure Processors with respect to Micro Architectural Attacks**
Expected date of defence: **2023**
Previous degrees: Engineer – Ecole des Mines – Saint-Etienne / Gardanne - France

15.NOIZETTE Luc
Title of thesis: **Predictive fault tolerance analysis methodology for complex components with consideration of the application**
Expected date of defence: **2024**
Previous degrees: Engineer - Grenoble INP - Phelma, Grenoble - France (2020)

16. REYNAUD Vincent
Title of thesis: **Secured access to IEEE 1687 test resources and lightweight crypto-processors in the IoT context**
Completed on: **March 9th, 2021**
Previous degrees: Engineer – Grenoble INP - Phelma, Grenoble - France (2017)

17. SENTHAMARAI KANNAN Kalpana
Title of thesis: **Performance and Safety/Security Management in automotive and IoT applications**
Completed on: **July 19th, 2021**
Previous degrees: Engineer - Pondichery University, India (2013)

18.TALY Emilien
Title of thesis: **Design of a very low power Artificial Intelligence system (Tensor Processing Unit - TPU) based on memory computation**
Expected date of defence: **2024**
Previous degrees: Engineer – Université de Montpellier – France (2020)

19. VINAGRERO GUTIERREZ Sergio
Title of thesis: **Design and Evaluation of Resistive-based Security Primitives (Physically Unclonable Function & True Random Number Generator)**
Expected date of defence: **2024**
Previous degrees: Engineer – Université Grenoble Alpes – France (2021)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. SHIMOU	Yasser	MOROCCO	3 months
2. TALY	Emilien	FRANCE	2 months

Visitors

No positions in 2021

Interns and trainees

Name	Forename	Country	Duration
1. AFLIHAOU	Houdeifa	ALGERIA	7 months
2. AMANS	Annabel	FRANCE	1 month 15 days
3. BOUCHEX-BELLOMIÉ	Guillaume	FRANCE	4 months 29 days
4. BOUDIAF	Imene Milissa	ALGERIA	2 months 11 days
5. CORREA CUETO	Marcelo	BRAZIL	4 months 30 days
6. FRATINI CHEM	Pedro	BRAZIL	3 months 25 days
7. GORCHS PICAS	Marti	SPAIN	8 months 1 day
8. JAMAL	Meriam	MOROCCO	4 months 8 days
9. KACI CHAOUCHE	Mohand	FRANCE	3 months 12 days
10.KHALLOUKI	Hamza	MOROCCO	3 months
11.LIN	Jiaru	CHINA	5 months 5 days
12.LUO	Zhifei	CHINA	2 months 11 days
13.MAILLEFERT	Antoine	FRANCE	5 months
14.MALDANER	Liège	BRAZIL	2 months 11 days
15.MEJRI	Mohamed Ali	TUNISIA	6 months
16.NAKHLE	Robert	FRANCE	3 months
17.OLIVEIRA	Alexandre	FRANCE	3 months 6 days
18.PASCAL-VALETTE	Djeson Franck	FRANCE	2 months 11 days
19.PO	Jia Yun	MALAYSIA	6 months
20.PONCET	Mehdy	FRANCE	3 months 3 days
21.SALES BRUM	Joao Paulo	BRAZIL	5 months
22.VINAGRERO GUTIERREZ	Sergio	SPAIN	10 months

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2021.

ANR

CAD4RMD (2021 – 2022)
Title: CAD Tool and Design Space Exploration for Resistive-based Memory Devices Integration in non-Von Neuman Architectures

EMINENT (2019 – 2023)
Scientific manager: VATAJELU Ioana

EM2G (2021 – 2022)
Title: EMulation de fautes EM par Glitch d'horloge locaux

EPOQAP (2021 – 2022)
Title: Évaluation des algorithmes de cryptographie post-quantique contre les attaques physiques

POP (2021 – 2025)
Title: Attaque laser de primitives de sécurité non alimentées
Partners: Ecole Nationale Supérieure des Mines Saint-Etienne (ENSMSE) Institut Polytechnique de Grenoble (Grenoble INP) Université Jean-Monnet Saint-Etienne

ANRT

CIFRE Antoine LINARES (2020 – 2023)
Title: Flexible Hardware for Intrinsic Secure Computing
Scientific manager: DI NATALE Giorgio

CIFRE Valérian CINCON (2018 – 2021)
Title: "Etude et intégration de systèmes neuro-morphiques ultra basse consommation en technologie FD-SOI"
Scientific manager: ANGHEL Lorena

EPST

CLAM (2020 – 2023)
Program: Equipe-Action Labex Persyval
Title: Cross-Layer Fault Analysis for Microprocessor Architectures
Scientific manager: MAISTRI Paolo

AVOCAM (2020 – 2021)
Program: IRS (Initiative de Recherche Stratégique)
Title: Analyse de Duration de Vie pour l'Optimisation de Calcul Approché Matériel
Scientific manager: LEVEUGLE Régis

stAte (2020 – 2023)
Program: PhD Thesis Program Labex Persyval
Scientific manager: POSSAMAI BASTOS Rodrigo
Title: stAte: Mitigation of Radiation Effects on the Attitude Estimation Processing of Autonomous Things

Cyber@Alpes (2018 – 2021)
Program: Grenoble Alpes CyberSecurity Institute
Scientific manager: MAISTRI Paolo
Team sharing (AMfoRS, CDSI)

INDUSTRIE

Processeurs Sécurisés et Attaques de micro architectures (2020 – 2023)
Scientific manager: LEVEUGLE Régis

REGION

MultiRad (2020 – 2023)
Program: Pack Ambition International
Title: MultiRad: Evaluation of Space-to-Ground Radiation Effects in Multicore Computing Systems for Safety-Critical Applications
Scientific manager: POSSAMAI BASTOS Rodrigo

SAFE-AIR (2017 – 2022)
Program: Pack Ambition Recherche
Title: Safety Evaluation of Aircraft Systems using Virtual Platforms
Scientific manager: LEVEUGLE Régis

Organization and participation of international conferences, workshops, forums

Design, Automation & Test in Europe (DATE'2021)
February 1-5, 2021, Virtual event, GERMANY
Rang : A+
local organization: DI NATALE G.
publication chair: VATAJELU E.I.
technical program committee: DI NATALE G.

24th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS'2021)
April 7-9, 2021, Vienna (virtual event), AUSTRIA
Rang : B
technical program committee: LEVEUGLE R., MAISTRI P., PORTOLAN M., VATAJELU E.I.

Dependability, Testing and Fault Tolerance in Digital Systems (DTFT'2021)
September 1-3, 2021, Palermo, ITALY
Rang : B
steering committee member: DI NATALE G.

IEEE 16th International Conference on Design & Technology of Integrated System in Nanoscale Era (DTIS'2021)
June 28-30th, 2021, Apulia, ITALY
Rang : NC
technical program committee: BENABDENBI M., VATAJELU E.I.

26th IEEE European Test Symposium (ETS'2021)
May 24-28, 2021, Virtual event, BELGIUM
Rang : A
local organization: INGLESE P.
program chair: VATAJELU E.I.
steering committee member: DI NATALE G.
technical program committee: VATAJELU E.I.
topic chair: LEVEUGLE R., VATAJELU E.I.

27th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2021)
June 28-30th, 2021, Virtual event, ITALY
Rang : B
general chair: NICOLAIDIS M.
steering committee member: NICOLAIDIS M.
technical program committee: ANGHEL L., BENABDENBI M., DI NATALE G., LEVEUGLE R., NICOLAIDIS M., PAPAVRAMIDOU P., PORTOLAN M.

22nd IEEE Symposium on Integrated Circuits and System Design (SBCCI'2021)
August 23-27, 2021, Virtual event
Rang : B
technical program committee: POSSAMAI BASTOS, Rodrigo

22nd IEEE Latin-American Test Symposium (LATS'2021)
October 27-29, 2021, Virtual event
Rang : NC
co-general chair: VELAZCO R.
technical program committee: POSSAMAI BASTOS Rodrigo, LEVEUGLE Régis

9th Prague Embedded Systems Workshop (PESW'2021)
July 1-3, 2021, Horomerice, CZECH REP.
Rang : NC
technical program committee: DI NATALE G.

Test Spring School (TSS'2021)
May 17-23, 2021, Virtual event
Rang : NC
technical program committee: VATAJELU E.I.

39th VLSI Test Symposium (VTS'2021)
April 25-28, 2021, Virtual event, FRANCE
Rang : A
steering committee member: NICOLAIDIS M.
technical program committee: DI NATALE G.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
PHELMA school PHysique, ÉLectronique, Matériaux				
Co-responsible of SEI branch	BENABDENBI M.	01/09/2017		
Manager of SEOC/PHELMA branch	PORTOLAN M.	01/09/2017		
DLST Département Licence Sciences et Technologies				
Manager of Training in Computer and Internet Basics	POSSAMAI BASTOS R.	01/09/2017		Training targeting around 1300 UGA/DLST's students
Research structures				
CIME Nanotech Centre Interuniversitaire de MicroElectronique et Nanotechnologies				
Manager of Design platform	BENABDENBI M.	01/09/2017		
MSTIC pole Mathématiques, sciences et technologies de l'information et de la communication				
Council member of MSTIC cluster	LEVEUGLE R.	01/09/2015		Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC

Scientific production

International journals (RI)

RI-1 Senthamarai Kannan K., Portolan M., Anghel L.*
Activity-aware prediction of Critical Paths Aging in FDSOI technologies
Microelectronics Reliability, Volume: 124, 2021
**Spintec*

RI-2 Ait Said N., Benabdenbi M., Morin-Allory K.
Arbitrary Reduced Precision for Fine-grained Accuracy and Energy Trade-offs
Microelectronics Reliability, Volume: 120, 2021

RI-3 Elshamy M.*, Di Natale G., Sayed Alhassan*, Pavlidis Antonios*, Louërat M.M.*, Aboushady Hassan*, Stratigopoulos H.*
Digital-to-Analog Hardware Trojan Attacks
IEEE Transactions on Circuits and Systems, Volume: , pp. 1-14, 2021
**LIP6 - Laboratoire d'Informatique de Paris 6*

RI-4 Garay Trindade M., Benevenuti F.*, Letiche M., Beaucour J.**, Kastensmidt F.*, Possamai Bastos R.**
Effects of thermal neutron radiation on a hardware-implemented machine learning algorithm
Microelectronics Reliability, Volume: 116, 2021
**UFRGS - Université fédérale du Rio Grande do Sul, **ILL - Institut Laue-Langevin*

RI-5 Portolan M., Valea E.*, Maistri P., Di Natale G.
Flexible and Portable Management of Secure Scan Implementations Exploiting P1687.1 Extensions
IEEE Design & Test, Volume: , 2021
**LIRMM - Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*

RI-6 Roux J.*, Roux J., Beroulle V.*, Morin-Allory K., Leveugle R., Bossuet L., Cezilly F.***, Berthoz F.***, Genevrier G.***, Cerisier F.****
High-level fault injection to assess FMEA on critical systems
Microelectronics Reliability, Volume: 122, pp. 114135, 2021
**Laboratoire de Conception et d'Intégration des Systèmes, **LHC - Laboratoire Hubert Curien , ***Thalès Valence, ****AEDVICES CONSULTING*

RI-7 Bandeira Vitor*, Sampford Jack, Garibotti R.F.***, Garay Trindade M., Possamai Bastos R., Reis R.*, Ost L.****
Impact of radiation-induced soft error on embedded cryptography algorithms
Microelectronics Reliability, Volume: , 2021
**UFRGS - Université fédérale du Rio Grande do Sul, **Phixos, ***PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ****Loughborough University*

RI-8 Dar G.*, Di Natale G., Keren O.*
Nonlinear Code-based Low-Overhead Fine-Grained Control Flow Checking
IEEE Transactions on Computers, Volume: , 2021
**BIU - Bar-Ilan University*

RI-9 Ait Said N., Benabdenbi M., Morin-Allory K.
Self-Adaptive Run-Time Variable Floating-Point Precision for Iterative Algorithms: A Joint HW/SW Approach
MDPI Electronics, Volume: 10, pp. 2209, 2021

RI-10 Martin H.*, Dupuis S., Di Natale G., Entrena L.***
Using Approximate Circuits Against Hardware Trojans
IEEE Design & Test, Volume: , 2021
**Universidad Carlos III de Madrid, **LIRMM - Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*

Invited conferences talks (INV)

INV-1 Di Natale G.
Hardware Security and Machine Learning: Hero or Hoax?
22nd IEEE Latin-American Test Symposium (LATS 2021), 2021

INV-2 Possamai Bastos R.
Radiation effects in tiny machine learning systems and attitude estimation processing modules for autonomous things
17th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA 2021), 2021

INV-3 Maistri P., Reynaud V., Portolan M., Leveugle R.
Secure Test with RSNs: Seamless Authenticated Extended Confidentiality
19th IEEE International New Circuits and Systems Conference (NEWCAS 2021), 2021

INV-4 Di Natale G., Vatajelu I.
Security Primitives with Emerging Memories
Design Automation Conference (DAC 2021), 2021

International conferences (CI)

CI-1 Kraemer Sarzi Sartori Tarso, Fourati H.*, Garay Trindade M., Possamai Bastos R.
Assessment of Attitude Estimation Processing System under Neutron Radiation Effects
Conference on Radiation Effects on Components and Systems (RADECS 2021), 2021
**INRIA Grenoble - Rhône-Alpes*

CI-2 Garay Trindade M.*, Garay Trindade M., Sales Brum Joao Paolo, Sales Brum Joao Paolo, Maldaner Liége, Maldaner Liége**, Garibotti R.F.***, Ost L.****, Possamai Bastos R.**
Assessment of Machine Learning Models in Computing System under Neutron Radiation
Conference on Radiation Effects on Components and Systems (RADECS 2021), 2021
**INRIA Grenoble - Rhône-Alpes, **Universidade Federal de Santa Maria, ***PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ****Loughborough University*

CI-3 Fiorucci T.*, Fiorucci T., Daveau J.M.*, Di Natale G., Roche P.*
Automated Dysfunctional Model Extraction for Model Based Safety Assessment of Digital Systems
IEEE 27th International Symposium on On-Line Testing and Robust System Design (IOLTS 2021), 2021
**STMicroelectronics [Crolles]*

CI-4 Linarès A.*, Hély D., Lhermet F.*, Di Natale G.**
Design Space Exploration Applied to Security
16th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS 2021), 2021
**SiFive France, **Laboratoire de Conception et d'Intégration des Systèmes*

CI-5 Sales Brum Joao Paolo, Sales Brum Joao Paolo*, Kraemer Sarzi Sartori Tarso, Lin Jiaru, Garay Trindade M., Fourati H., Velazco R., Possamai Bastos R.**
Evaluation of Attitude Estimation Algorithm under Soft Error Effects
IEEE Latin-American Test Symposium (LATS 2021), 2021
**Universidade Federal de Santa Maria, **INRIA Grenoble - Rhône-Alpes*
CI-6 Von Staudt H.M*, Van Treuren B., Rearick J.***, Portolan M., Keim M.****
Exploring and Comparing IEEE P1687.1 and IEEE 1687 Modeling of Non-TAP Interfaces
IEEE European Test Symposium (ETS 2021), 2021
**Dialog Semiconductor, **VT Enterprises, ***Advanced Micro Devices Inc., USA, ****Siemens Digital Industries Software*
CI-7 Ait Said N., Benabdenbi M., Morin-Allory K.
FPU Reduced Variable Precision in Time: Application to the Jacobi Iterative Method
IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2021), 2021
CI-8 Martin H.*, Vatajelu I., Di Natale G.
Identification of Hardware Devices based on Sensors and Switching Activity: a Preliminary Study
Design, Automation & Test in Europe Conference & Exhibition (DATE 2021), 2021
**Universidad Carlos III de Madrid*
CI-9 Bandeira Vitor*, Sampford Jack, Garibotti R.F.***, Garay Trindade M., Possamai Bastos R., Reis R.*, Ost L.****
Impact of radiation-induced soft error on embedded cryptography algorithms
European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2021), 2021
**UFRGS - Université fédérale du Rio Grande do Sul, **Phixos, ***PUCRS - Pontificia Universidade Catolica do Rio Grande do Sul, ****Loughborough University*
CI-10 Inglese P., Vatajelu I., Di Natale G.
Memristive Logic-in-Memory Implementations: A Comparison
16th International Conference on PRIME, 2021
CI-11 Alshaer I.*, Colombier B., Deleuze C.*, Beroulle V.*, Maistri P.
Microarchitecture-aware Fault Models: Experimental Evidence and Cross-Layer Inference Methodology
International Conference on Design & Technology of Integrated System in Nanoscale Era (DTIS 2021), 2021
**Laboratoire de Conception et d'Intégration des Systèmes*
CI-12 Pancher F.*, Vargas V., Ramos P.**, Possamai Bastos R., Ardiles Saravia David César, Velazco R.**
Nanosatellite On-Board Computer including a Many-Core Processor
IEEE Latin-American Test Symposium (LATS 2021), 2021
**Institut de Planétologie et d'Astrophysique de Grenoble, **Universidad de las Fuerzas Armadas*
CI-13 Inglese P., Vatajelu I., Di Natale G.
On the Limitations of Concatenating Boolean Operations in Memristive-Based Logic-In-Memory Solutions
16th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS 2021), 2021
CI-14 Jaamoun A., Hiscock T.*, Di Natale G.
Scramble Cache: An Efficient Cache Architecture for Randomized Set Permutation
Design, Automation & Test in Europe Conference & Exhibition (DATE 2021), 2021
**Laboratoire d'Electronique de Technologie de l'Information*
CI-15 Portolan M., Reynaud V., Maistri P., Leveugle R., Di Natale G.
Security EDA Extension through P1687.1 and 1687 Callbacks
IEEE International Test Conference (ITC 2021), pp. 344-353, 2021

Book chapters (CH)

CH-1 Cayrel P.L.*, Colombier B., Dragoi V.F., Menu A.***, Bossuet L.***
Message-Recovery Laser Fault Injection Attack on the Classic McEliece Cryptosystem
Eurocrypt 2021, pp. 438-467, 2021
**LHC - Laboratoire Hubert Curien , **UAV - Aurel Vlaicu University of Arad, ***Ecole Nationale Supérieure des Mines de Saint-Etienne*

National journals (RN)

RN-1 Benabdenbi M., Leveugle R.
Test des circuits intégrés numériques - Notions de base et évolutions
Techniques de l'Ingénieur, Volume: TIP350WEB, 2021

Other communications (O)

O-1 Noizette Luc, Leveugle R., Miller Florent*, Colladant Thierry, Helen Youri*****
Comparaison des données disponibles sur trois plateformes d'analyses différentes RISC-V en vue d'une étude sur la propagation de fautes
15ème Colloque National du GDR SOC2, Rennes, FRANCE
**Nucletudes, **Direction générale de l'Armement , ***DGA Maîtrise de l'information (Bruz)*
O-2 Martinoli Valentin, Teglia Y.*, Leveugle R.
How SGX security claims meet real life scenarios
IEEE European Test Conference, PhD Forum (ETS 2021), Virtual event, BELGIUM
**Thalès DIS*
O-3 Martinoli Valentin, Teglia Y.*, Leveugle R.
SGX face aux menaces micro architecturales : efficacité et limitations
15ème Colloque National du GDR SOC2, Rennes, FRANCE
**Thalès DIS*
O-4 Vinagrero Gutierrez Sergio, Martin H.*, Vatajelu I., Di Natale G.
SRAM-PUF: Platform for Acquisition of Sram-Based Pufs from Micro-Controllers
University Booth - IEEE Design Automation and Test Conference in Europe (DATE 2021), Grenoble, FRANCE
**Universidad Carlos III de Madrid*

Theses (T)

T-1 Ait Said N.
Toward Floating-Point Run-time Variable Precision in CPU-based Architectures
These de Doctorat, Université Grenoble Alpes, spécialité "", Nov 24, 2021
T-2 Bordes N.
Security of symmetric primitives and their implementations
These de Doctorat, Université Grenoble Alpes, spécialité "Mathématiques et Informatique", Dec 09, 2021
T-3 Garay Trindade M.
Assessment of Edge Machine-Learning Systems under Radiation-Induced Effects
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Sep 30, 2021
T-4 Reynaud V.
Secured access to IEEE 1687 test resources and lightweight crypto-processors in the IoT context
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Mar 09, 2021
T-5 Senthamarai Kannan K.
Performance and Safety/Security Management in automotive and IoT applications
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Jul 19, 2021

CNRS - Grenoble INP - UGA

CDSI team

Circuits, Devices and System Integration

Circuits, Devices and System Integration (CDSI team)

Keywords: Asynchronous circuits, design methods and tools, design for ultra-low power, FDSOI technology, MEMS, Smart sensors and actuators

The CDSI team

The team activity covers a broad spectrum of activities from MEMS to systems. Indeed, the team postulates high performances are achieved thanks to disruptive technologies, which are at the frontiers of different fields of applications. Nevertheless, the team is built on two key pillars, sensing and event processing.

Event-based techniques are key for enhancing integrated circuits and systems because they offer a unique opportunity to rethink circuit design, which does not take well into account most of the non-functional specifications, such as power, security, safety or electromagnetic emissions. This paves the way to ultra-low power systems, enhanced secured systems, proven design methods but also near sensor computing.

Sensing is the second key. Taking advantage of smart sensors and actuators requires globally envisioning systems, favors a smart sensing approach limiting useless information and pushes new experiments and usage.

Event-based technologies

Event-based approach

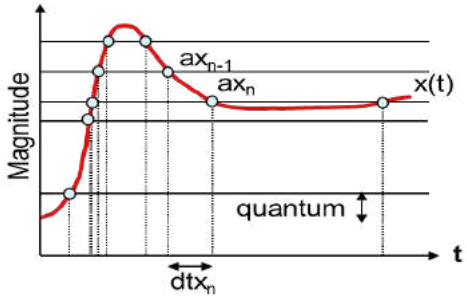


Figure 1: Level Crossing Sampling Scheme

Event-based is a quite simple idea, which suggests operating a circuit only when needed. Nevertheless, this is countercurrent when looking the semiconductor industry. Indeed, everything is clocked synchronized, analog-to-digital conversion is clock-sampled. In practice, clock is used as an event generator giving the pace of the circuits generating a large number of events and producing useless activity, computation, storage or communication. The event-based approach tends generating sparse events related to natural events such as a pressure variation or a heartbeat. Therefore, the team works on alternative analog-to-digital converters able to drastically reduce the number of samples and, hence, limit useless activity and energy consumption (see Figure 1).

Asynchronous Circuits

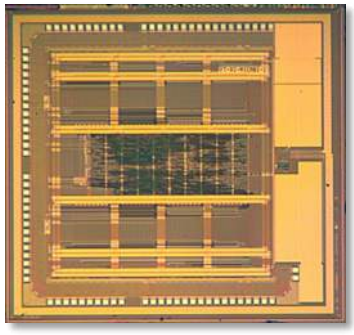


Figure 2: Asynchronous microcontroller with on-chip NFC antenna

Since more than 20 years, the team works on new synchronization paradigms, which are not based on a clock but on handshake signals. Such techniques reveal many opportunities for rethinking the circuit design process and opening new degrees of freedom. The first expected advantage is probably the reusability of existing blocks that can simply be connected together, making the assembly of a system a kind of LEGO build. Indeed, the timing assumptions are locally fulfilled guarantying an easy block association. Moreover, many other advantages are of interest such a lower power consumption, a better robustness, lower electromagnetic emissions, safer and more secured circuits…

Targeting Ultra-low power

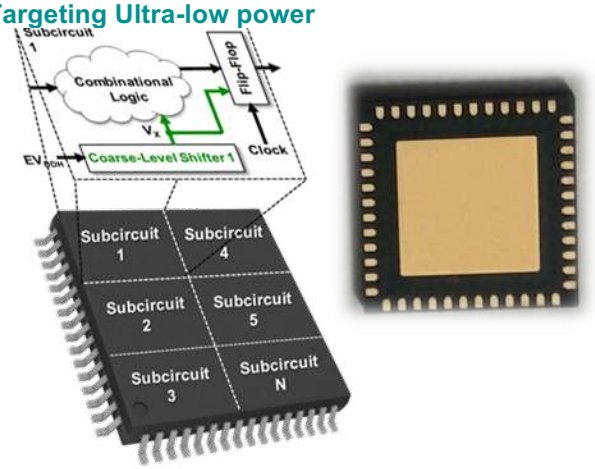


Figure 3: FDSOI 28 nm asynchronous testchip managing several local fine-grain body-bias domains

Today power is a main concern for chip design. The event-based strategy is probably the best technique for reducing power at least by one order of magnitude. Indeed, a sparse sampling scheme produces much less data, which are non-uniformly spaced in time. Each datum is no more than an event that can be sporadically processed by asynchronous circuits. Indeed, these latter are data-driven and consume energy only when computing. Moreover, the intrinsic robustness of asynchronous circuits favors their use at low-voltage, near- or subthreshold. Indeed, lowering the voltage is an efficient and well-known strategy to save power. Its main drawback is the decrease of the circuit speed. The Fully Depleted Silicon on Insulator (FDSOI) technology allows mitigating this speed drop thanks to forward body biasing. As asynchronous circuits use communication protocols indicating circuit activity, the handshake signals are perfectly suited for controlling local body-bias domains ensuring low-energy expenses for body biasing and compensating the speed loss.

All these mechanisms can be implemented for mitigating the energy and helping the adoption of energy harvesting in batteryless systems.

Security

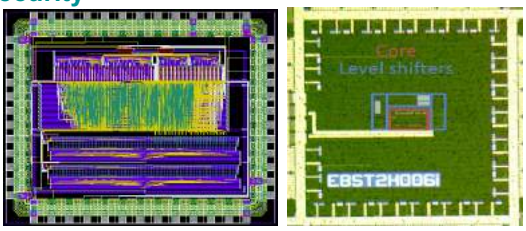


Figure 4: TRNG with entropy monitoring (left) and Ultra-low power TRNG (right) (30 pJ/bit@0.3 V)

Another opportunity offered by the asynchronous circuits is its ability to make more difficult the side-channel analysis and attacks in trusted devices. Indeed, the absence of clock synchronization, the specific encoding and the computation time control makes them of interest for developing trusted platforms. They also offer disruptive strategies for true random number generators (TRNG) and physically unclonable functions (PUF) while consuming a few energy.

Design flow and proven technology

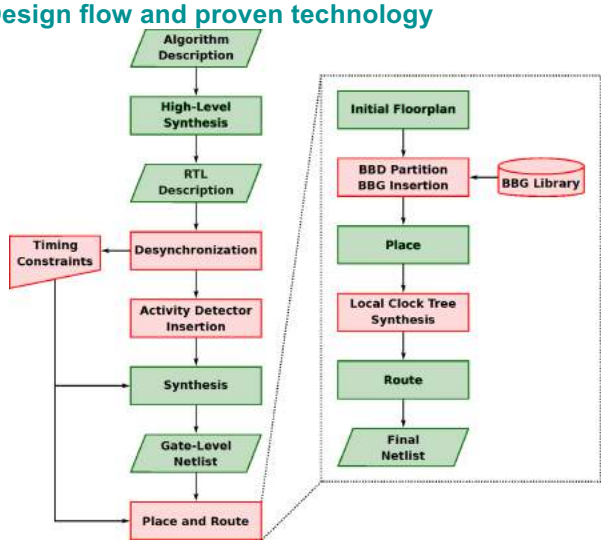


Figure 5: Asynchronous circuit HLS to layout design flow

Developing non-conventionally synchronized circuits is not obvious because of the lack of dedicated CAD tools. Although the first good idea is to implement such tools, there is some overcoming hurdles. The first one is clearly the quasi-absence of trained people with the know-how for designing efficient and performant asynchronous circuits. The second is the impact, the reliability and the engineer confidence into a new design flow. Therefore, for more than 10 years, the team is developing dedicated flows based on the standard commercial tools with a particular emphasis on a proven by construction synthesis.

Near-sensor computing

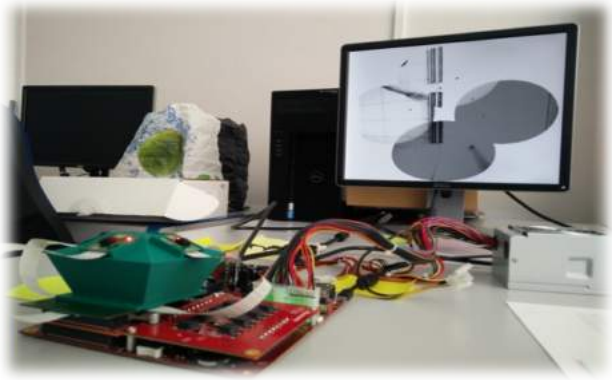


Figure 6: Panoptic camera for laparoscopy

With the dissemination of autonomous and connected objects, it appeared the need to limit the amount of transmitted raw data, especially in RF communications where the problem is more acute. Therefore, developing tiny sensor platforms able to preprocessed data before transmitting information is becoming a challenging topic. Indeed, enhancing the sensing techniques and immediately processing the raw data with a reduced energy budget is the grail in near-sensor computing. The team developed several strategies based on event-based techniques or improving the adequacy between the algorithms and the circuit architecture. This is typically the case for many image-processing applications such as panoptic camera for laparoscopy.

Smart-sensing technologies

In-sensor computing

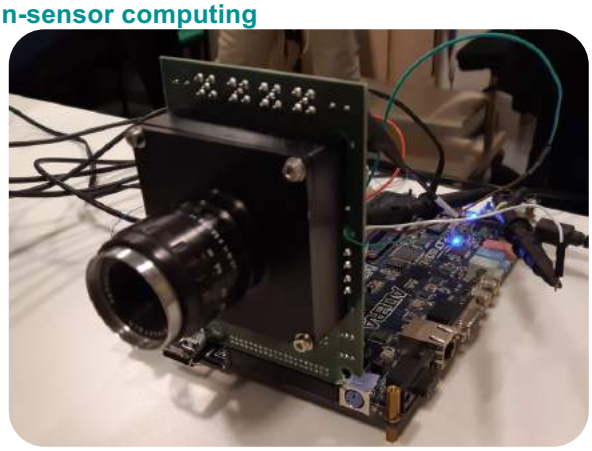


Figure 7: Event-based camera

As previously stated, smart sensing is a key for envisioning systems with advanced features such as detection, pattern recognition or low-power. Beyond the state of art of sensor technology, the enhancement can be obtained thanks to new architectures or in-sensor computing. One of the approach concerns image sensors, which usually permanently read the image. This is a waste of energy and time for acquiring an image. In order to reduce these issues, the image capture can be performed thanks to an event-based readout, which only samples a pixel when this latter fires. In this case, the firing pixel indicates that its value has to be changed in the image memory. Such a strategy is applied for reducing the power consumption and increasing the speed sensor thanks to a dedicated readout canceling the spatial and temporal redundancies.

Measuring time

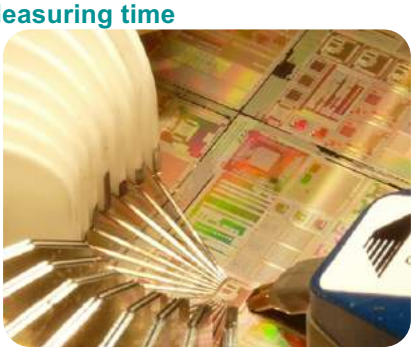


Figure 8: Asynchronous multiphase oscillator (under test) used in TDC

Using an event-based sensing implies a duality with the standard Nyquist analog-to-digital conversion because the quantization is no more applied to the amplitude but to the time elapsed between two successive events. Therefore, designing advanced Time-to-Digital Converters (TDC) is an important block for many sensors or even for some security primitives such as TRNG or PUF.

Harvesting for ultra-low power systems

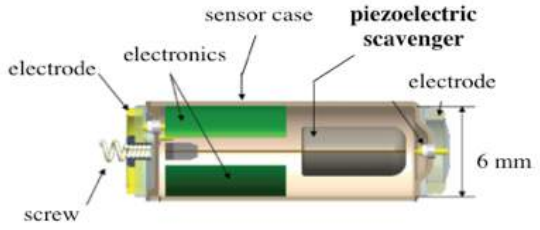


Figure 9: Piezoelectric scavenger for automous pacemaker (Vibration: 10 - 25 Hz, Size: L = 30 mm, Ø= 6 mm, energy: 5 - 10 µJ)

With the advent of the Internet of Things, the system requirements in term of power are extremely demanding, especially for smart sensing and actuating. A typical highlight targets the medical implant such as pacemakers. Indeed, they need today a battery, which lasts less than 10 years. Then the pacemaker has to be explanted because this is not a rechargeable battery. Wireless power transfer may overcome this issue via acoustic wave propagation, using piezoelectric transducers to generate and harvest acoustic power. The MEMS are particularly well-suited for this purpose, for small autonomous and smart objects.

Security (chaotic approach)

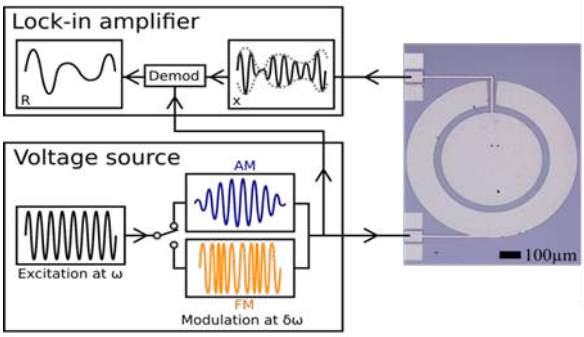


Figure 10: Experimental Setup and modulations in the Duffing's regime. The MEMS (photography) is driven by a voltage modulated voltage source (AM or FM). The Lock-in-Amplifier extracts the displacement magnitude of the MEMS to observe the chaos.

MEMS have opened the doors to intense researches covering most of the technology fields. It is not surprising that they can be of interest for security. They offer original solutions for designing chaotic generators using the dynamical bistability of a Duffing's microresonator. This approach is particularly relevant for generating true random numbers because MEMS already exist on various systems such as mobile phones and are useable for extracting chaos. Moreover, this could be employed for securing communications in various transduction schemes. In acoustics, chaotic MEMS can be used as ultrasonic jammers. In optics, synchronization of chaotic MEMS takes benefit from both high complexity yet controllable chaos and large data rate for secured telecom applications.

New Sensors and actuators

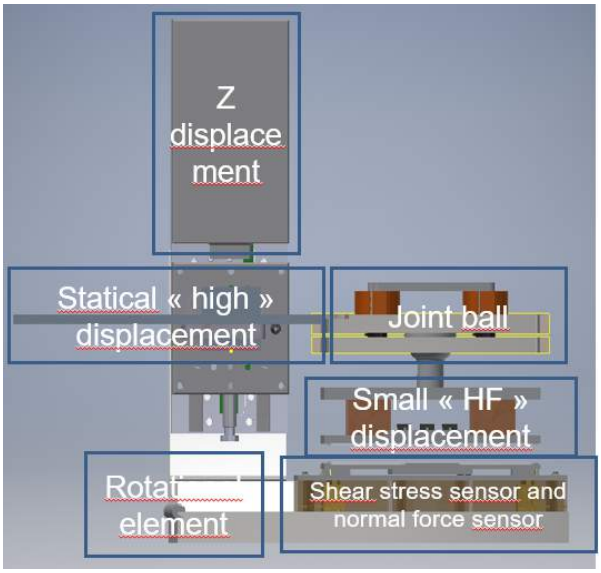


Figure 11: The 3D representation of the new piezo rheometer with description of its functions

The team is also developing a new kind of piezo-based sensors and actuators for applications in rheometry, earphones, or microphones.

The piezorheometer permits to obtain high frequency strain compared to standard equipment. This rheometer combines piezoelectric actuator, slaved by accelerometers to give accurate strain to a media, with piezolectrics ceramics which are the sensors to extract the stress given to this media. With a precise extraction of the imposed strain synchronized with the stress, the shear modulus is calculated. Innovation comes from the slaving of the actuators. Moreover, this kind of rheometer only applied small strain so a linear piezoelectric actuator has been implemented to evaluate the shear modulus from very low to very high strain. Finally, this rheometer will be as precise as classical rheometer but less expensive and with a smaller volume.

Figure 12: ActivMotion earphones concept

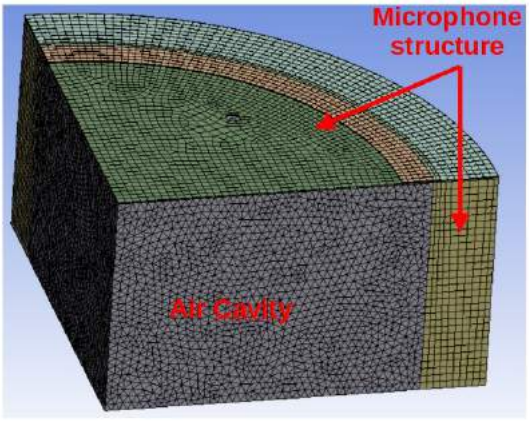


Figure 13: Finite element model for MEMS piezoelectric microphone.

Piezoelectric actuators can also be implemented in earphones to replace the widely used electrodynamic transducers. They offer new possibilities in term of design and integration, which ActivMotion is pushing. In their concept, the user's ears become the emitting surface which allows for new earphone ergonomics. High power density piezoelectric actuators working at low voltages are ideal for this use case. With the resonance control of the actuator, a linear performance over the audible frequency range is obtained.

CDSI team is also part of the project MAMBO aiming at reducing airplanes noises. The knowledge of noise sources in airplanes is crucial and requires specific microphones characteristics to measure them (high pressure, wide dynamic and frequency range, low SNR,…). In this context, the team work is focused on the conception of a MEMS piezoelectric microphone using finite element method and lumped element equivalent circuit to predict the microphone performances for aeroacoustic measurements.

Highlights of 2021 and of the recent years

International Cooperation

Design of MEMS for acoustic applications and Energy harvesting
Scientific Manager: DE GIOVANNI Adrien
Partners: Universita di Brescia
City: Brescia
Country: ITALY
Start the: Jan 01, 2016 until Dec 31, 2021

Développement de TDC FPGA et ASIC à très haute résolution et faible latence
Scientific Manager: FESQUET L.
Partners: INPT (Institut National des Postes et Télécommunications)
City: Rabat
Country: MOROCCO
Start the: Jan 01, 2018 until Dec 31, 2021

Infrastructure for Secure, Reliable, and Low-Power Computing Systems
Scientific Manager: POSSAMAI BASTOS R.
Partners: PUCRS (Pontifícia Universidade Católica do Rio Grande do Sul)
City: Porto Alegre
Country: BRAZIL
Start the: Nov 01, 2018 until Oct 31, 2022

Accueil de Marwa GASSAB en co-tutelle
Scientific Manager: FESQUET L.
Partners: Université de Sousse
City: Sousse
Country: TUNISIA
Start the: Jan 01, 2019 until Dec 31, 2021

Organisation and participation of National Conferences, Workshops, Forums in 2021

JNRSE - 10èmes Journées Nationales sur la Récupération et le Stockage de l'Energie
June 2-3, 2021, Online edition, FRANCE
technical program committee: BASROUR S.

- Asynchronous circuit High Level Synthesis for fine-grain body-biasing in FDSOI (tetschips in 65 nm and 28 nm from STMicroelectronics)
- New event-based image sensor cancelling spatial and temporal redundancies in FDSOI 28 nm from STMicroelectronics
- Physically Unclonable Function based on self-timed ring and TDC (testchip in 65 nm from STMicroelectronics)
- First DFT technique for asynchronous bundled-data circuits based on commercial tools
- Static Timing Analysis of asynchronous bundled-Data Circuits
- Local clock set methodology for implementing asynchronous circuits with commercial tools
- Event-based demodulation for NFC applications
- EM shaping with bundled-data circuits
- First demonstration of MEMS-based TRNG achieving NIST requirements
- Generation and reception of chaotic ultrasonic waves
- Synchronization of two chaotic MEMS
- Acoustic power transfer through a Tungsten layer

Academic and research members

Skandar BASROUR

Position
Professor at UGA – POLYTECH school

Responsibilities
Researcher in CDSI team

Martial DEFOORT

Position
Researcher at CNRS

Responsibilities
Researcher in CDSI team

Sylvain ENGELS

Position
Associate Professor PAST at Grenoble INP - PHELMA school

Responsibilities
Researcher in CDSI team

Laurent FESQUET

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Leader of CDSI team
Researcher in CDSI team

Stéphane MANCINI

Position
Associate Professor at Grenoble INP - ENSIMAG school

Responsibilities
Researcher in CDSI team

Katell MORIN-ALLORY

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in CDSI team

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
GRENOBLE INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AKBARI Masoud
Title of thesis: **Open-air fabrication of oxide based cantilever gas sensors**
Expected date of defence: **2023**
Previous degrees: Engineer - Pohang University of Science and Technology, Korea (2015)

2. AKRARAI Mohamed
Title of thesis: **Smart Event-Based Image Sensor for wake-up applications**
Expected date of defence: **2022**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

3. BELOT Jérémy
Title of thesis: **Towards robust, low power and adjustable accuracy Bayesian computers**
Expected date of defence: **2022**
Previous degrees: Engineer Grenoble INP – Phelma, France (2018)

4. CROZET Florent
Title of thesis: **Extreme Learning Machine for embedded neural networks**
Expected date of defence: **2024**
Previous degrees: Engineer (2019)

5. DECOUDU Yoan
Title of thesis: **An asynchronous Design Flow for Event-Based Processing in FDSOI Technologies**
Expected date of defence: **2022**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

6. DE GIOVANNI Adrien
Title of thesis: **Design of a piezoelectric micro-actuator with mechanical amplification for extra-auricular earphones**
Expected date of defence: **2023**
Previous degrees: Engineer (2020)

7. GASSAB Marwa
Title of thesis: **New electroactive nanostructured materials for flexible sensors**
Expected date of defence: **2022**
Previous degrees: Engineer – Higher Institute of Applied Sciences and Technology of Sousse (2018)

8. GIMENEZ Grégoire
Title of thesis: **Design of secure and very low power circuits : an asynchronous alternative**
Completed on: February 12th, 2021
Previous degrees: Engineer – Grenoble INP - Phelma, France (2009)

9. HACHEMI Mohammed-Bilal
Title of thesis: **Study of HZO films for MEMS applications**
Expected date of defence: **2022**
Previous degrees: Engineer - ECole Polytechnique de Constantine – Algeria (2017)

10. IGA Rodrigo
Title of thesis: **EM compliant Low-Energy Sugnal Demodulation for NFC applications**
Expected date of defence: **2022**
Previous degrees: Engineer – Université Grenoble Alpes, France (2010)

11. KALEL Diana
Title of thesis: **Development of an advanced flow of structural, formal and semi-formal verification of asynchronous paths using appropriate formal verification methods and tools, for high-performance integrated processor-based subsystems**
Expected date of defence: **2024**
Previous degrees: Master 15.173 - Université Grenoble Alpes, France (2020)

12. LAUWERS Thomas
Title of thesis: **Resonant optical transduction for photoacoustic detection**
Completed on: March 22nd, 2021
Previous degrees: Engineer –Grenoble INP –Phelma, France (2016)

13. LECLAIRE Nicolas
Title of thesis: **Hardware and software architectures for deep learning acceleration on embedded multi-processor**
Expected date of defence: **2022**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2017)

14. LIM Olivier
Title of thesis: **Real-Time unconventional adaptive cameras for multimodal acquisition**
Expected date of defence: **2023**
Previous degrees: Master (2020)

15. MOUSSA Hasan
Title of thesis: **Event-based Smart RF Architectures**
Expected date of defence: **2024**
Previous degrees: Master WICS - Université Grenoble Alpes (2021)

16. ROUX Julie
Title of thesis: **Safety Evaluation of Aircraft Systems using Virtual Platforms**
Expected date of defence: **2022**
Previous degrees: Engineer – Grenoble INP - Phelma, France (2017)

17. TACYNIAK Pierre
Title of thesis: **Study of a secured wireless piezoelectric power transmitter for medical implants.**
Expected date of defence: **2024**
Previous degrees: Engineer - Arts et Métiers ParisTech, France (2021)

18. TRAN Rosalie
Title of thesis: **Smart Event-Based Image Processing**
Expected date of defence: **2024**
Previous degrees: Engineer - Grenoble INP - Phelma, France (2021)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
1. ABDALI	El Mehdi	MOROCCO	9 months
2. BOCCALERO	Gregorio	ITALY	1 month
3. PASSY KENGANI	Marco Erickson	CONGO	2 months 10 days
4. RICART	Thibault	FRANCE	12 months
5. RUFER	Libor	CZECH REP	12 months

Visitors

No positions in 2021

Interns and trainees

Name	Forename	Country	Duration
1. AZZOUZ	Yosra	TUNISIA	2 months 15 days
2. DECOUDU	Clovis	FRANCE	2 days
3. KERDOUSSI	Ilyes	FRANCE	2 months 12 days
4. LOUWERS	Erin	FRANCE	2 months 18 days
5. MERIO	Cristiano	BRAZIL	3 months 29 days

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2021.

ANRT

CIFRE Jérémy BELOT (2020 – 2023)
Scientific manager: FESQUET Laurent

CIFRE Alexis Rodrigo IGA JADUE (2018 – 2021)
Title: "Démodulation NFC Basse Consommation et Respectueuse de la Compatibilité Electromagnétique"
Scientific manager: FESQUET Laurent

CIFRE Nicolas LECLAIRE (2018 – 2021)
Title: "Architectures matérielles et logicielles pour l'accélération du "deep learning" sur multiprocesseur évolutif embarqué"
Scientific manager: MANCINI Stéphane

CEC-NATIONAL

OCEAN 12 (2018 – 2021)
Program: ECSEL
Title: Opportunity to Carry European Autonomous driviNg further with FDSOI technology up to 12nm node
Scientific manager: FESQUET Laurent

EPST

Chameleon (2020 – 2021)
Program: IRS (Initiative de Recherche Stratégique)
Scientific manager: BASROUR Skandar

Cyber@Alpes (2018 – 2021)
Program: Grenoble Alpes CyberSecurity Institute
Scientific manager: MAISTRI Paolo
Team sharing (AMfoRS, CDSI)

INDUSTRIE

ICALPS - G.GIMENEZ (2018 – 2021)
Title: Conception de circuits d'identification sécurisé basse consommation
Scientific manager: FESQUET Laurent

INTERNATIONAL

BRAFISAT (2019 – 2022)
Program: BRAFITEC
Scientific manager: POSSAMAI BASTOS Rodrigo

MINISTERES-FUI

EAUDI (2021 – 2025)
Title: Ecouteur extra AUriculaire Dissimulé

IMSPOC-UV (2018 – 2022)
Program: PIA Programme d'Investissemeent d'Avenir
Title: Imaging Spectrometer On Chip
Scientific manager: BASROUR Skandar

REGION

MucoPiezoRheo (2020 – 2023)
Program: PSPC
Scientific manager: BASROUR Skandar

GRESAM (2019 – 2021)
Program: Pack Ambition International
Title: Grenoble Sousse Autonomous Microsystems
Scientific manager: BASROUR Skandar

FAIR (2018 – 2023)
Program: Pack Ambition Recherche
Title: Conception et fabrication par Fabrication Additive de produits Intelligents
Scientific manager: BASROUR Skandar

SATT

EMIR (2021 – 2023)
Title: Event-based Microbolometer for IR sensors adn ultra low power applications

Organization and participation of international conferences, workshops, forums

14th International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS'2021)
November 14-18, 2021, Athens, GREECE
Rang : NC
technical program committee: FESQUET L.

Design, Automation & Test in Europe (DATE'2021)
February 1-5, 2021, Virtual event, GERMANY
Rang : A+
technical program committee: MORIN-ALLORY K.

IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC'2021)
December 20-23, 2021, Singapore, SINGAPORE
Rang : NC
technical program committee: MORIN-ALLORY K.

6th International Conference on Advances in Signal, Image and Video Processing (SIGNAL'2021)
May 30-June 03, 2021, Valencia, SPAIN
Rang : NC
industry/research committee: FESQUET L.
technical program committee: FESQUET L.

21st International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS'2021)
June 20-25, 2021, Virtual event
Rang : NC
technical program committee: BASROUR S.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
PHELMA school PHysique, ÉLectronique, Matériaux				
Manager of SEI branch	MORIN-ALLORY K.	01/09/2017		
Research structures				
CIME Nanotech Centre Interuniversitaire de MicroElectronique et Nanotechnologies				
Deputy Director	FESQUET L.	01/09/2017		
Manager of Communicating objects platform	MANCINI S.	01/09/2017		
Manager of Microsystems platform	BASROUR S.	01/10/2006		
FMNT Fédération des Micro et Nanotechnologies				
Deputy Director	BASROUR S.	01/01/2021		
PEM pole Physique, ingénierie, matériaux				
TIMA representative of PEM cluster	BASROUR S.	01/09/2016		
Parent institutions				
Grenoble INP Grenoble Institute of Technology				
Board of Directors member (elected member)	MANCINI M.	12/12/2019	01/01/2024	Strategy, jobs, promotion files, invited professors, teaching assistants

Scientific production

International journals (RI)

RI-11 Defoort M., Rufer L., Fesquet L., Basrour S.
A dynamical approach to generate chaos in a micromechanical resonator
Microsystems & Nanoengineering, Volume: 7, 2021
RI-12 Belot Jérémy*, Belot Jérémy, Cherkaoui A.*, Laurent Raphaël*, Fesquet L.
An Area and Power Efficient Stochastic Number Generator for Bayesian Sensor Fusion Circuits
IEEE Design & Test, Volume: 38, pp. 69-77, 2021
**HawAI.Tech*
RI-13 Fortin Thomas*, Vysotskyi Bogdan, Defoort M., Reynaud Adrien***, Lai Szu-Hsueh****, Lai Szu-Hsueh*****, Dominguez-Medina Sergio******, Clement Kavya*, Çumaku Vaitson*, Hentz Sébastien***, Masselon C.***
A Nonlinear Model for Nano-Electro Mechanical Mass Sensing Signals Processing
Sensors Journal , Volume: 21, 2021
**Institut de Recherche Interdisciplinaire de Grenoble , **Institut de micro-électronique et composants, ***Laboratoire d'Electronique de Technologie de l'Information, ****Bijvoet Center for Biomolecular Research [Utrecht], *****Utrecht Institute for Pharmaceutical Sciences , ******Folio Photonics Inc.*
RI-14 Ait Said N., Benabdenbi M., Morin-Allory K.
Arbitrary Reduced Precision for Fine-grained Accuracy and Energy Trade-offs
Microelectronics Reliability, Volume: 120, 2021
RI-15 Panayanthatta Namanu*, Clementi Giacomo, Ouhabaz Merieme**, Costanza Mario**, Margueron Samuel**, Bartasyte Ausrine**, Basrour S., Bano Edwige*, Montes Laurent*, Dehollain Catherine***, La Rosa Roberto***, La Rosa Roberto****
A Self-Powered and Battery-Free Vibrational Energy to Time Converter for Wireless Vibration Monitoring
Sensors, Volume: 21, pp. 7503, 2021
**IMEP-LAHC - Institut de Microélectronique, Electromagnétisme et Photonique - Laboratoire d'Hyperfréquences et Caractérisation, **FEMTO-ST (Franche-Comté Électronique Mécanique, Thermique et Optique - Sciences et Technologies), ***EPFL, ****STMicroelectronics [Catania]*
RI-16 Defoort M., Rufer L., Basrour S.
Chaotic ultrasound generation using a nonlinear piezoelectric microtransducer
Journal of Micromechanics and Microengineering, Volume: 31, 2021
RI-17 Fernandez-Brillet L.*, Fernandez-Brillet L., Leclaire N.*, Leclaire N., Mancini S., Nicolas M.*, Cleyet-Merle S.*, Henriques J.P.*, Delnondedieu C.*
Compression and Speed-up of Convolutional Neural Networks Through Dimensionality Reduction for Efficient Inference on Embedded Multiprocessor
Journal of Signal Processing Systems, Volume: , 2021
**STMicroelectronics [Grenoble]*
RI-18 Aguenounon E.*, Razavinejad S., Schell J.B.*, Dolatpoor Lakeh M.*, Khaddour W.*, Dadouche F.*, Kammerer Jean-Baptiste*, Fesquet L., Uhring Wifried***
Design and Characterization of an Asynchronous Fixed Priority Tree Arbiter for SPAD Array Readout
Sensors, Volume: 21, pp. 3949, 2021
**ICube - Laboratoire des sciences de l'ingénieur, de l'informatique et de l'imagerie , **Guilan University*
RI-19 Roux J.*, Roux J., Beroulle V.*, Morin-Allory K., Leveugle R., Bossuet L., Cezilly F.***, Berthoz F.***, Genevrier G.***, Cerisier F.******
High-level fault injection to assess FMEA on critical systems
Microelectronics Reliability, Volume: 122, pp. 114135, 2021
**Laboratoire de Conception et d'Intégration des Systèmes, **LHC - Laboratoire Hubert Curien , ***Thalès Valence, ****AEDVICES CONSULTING*
RI-20 Hadj Salem K.*, Jost V., Kieffer Y.***, Libralesso L.**, Mancini S.**
Minimizing makespan under data prefetching constraints for embedded vision systems: a study of optimization methods and their performance
ORIJ - Operational Research - An International Journal, Volume: , 2021
**LIFAT - Laboratoire d'Informatique Fondamentale et Appliquée de Tours, **G-SCOP - Laboratoire des sciences pour la conception, l'Optimisation et la Production, ***Laboratoire de Conception et d'Intégration des Systèmes*
RI-21 Popescu A.*, Besancon G.*, Voda A.*, Basrour S.
Observer-Based 3-D Control Enhancement for Topographic Imaging--Validation With an STM Prototype
IEEE Transactions on Control Systems Technology, Volume: , pp. 1-12, 2021
**GIPSA-Lab*
RI-22 Zeidi Najeh*, Kaziz S.*, Hadj Said M., Hadj Said M.*, Rufer L., Cavallini Andrea***, Tounsi F.***
Partial discharge detection with on-chip spiral inductor as a loop antenna
Review of Scientific Instruments, Volume: 92, 2021
**Ecole Nationale d'Ingenieurs de Sfax (ENIS) , **Center for Research on Microelectronics and Nanotechnology, ***School of Engineering and Architecture - Bologna University*
RI-23 Clement Kavya*, Reynaud Adrien, Defoort M., Vysotskyi Bogdan***, Fortin Thomas*, Lai Szu-Hsueh****, Lai Szu-Hsueh*****, Çumaku Vaitson*, Dominguez-Medina Sergio******, Hentz Sébastien**, Hentz Sébastien*******, Masselon C.***
Requirements and Attributes of Nano-Resonator Mass Spectrometry for the Analysis of Intact Viral Particles
Analytical and Bioanalytical Chemistry, Volume: 413, pp. 7147–7156, 2021
**Etude de la dynamique des protéomes, **Laboratoire d'Electronique de Technologie de l'Information, ***Institut de micro-électronique et composants, ****Bijvoet Center for Biomolecular Research [Utrecht], *****Utrecht Institute for Pharmaceutical Sciences , ******Folio Photonics Inc., *******Université Grenoble Alpes*
RI-24 Ait Said N., Benabdenbi M., Morin-Allory K.
Self-Adaptive Run-Time Variable Floating-Point Precision for Iterative Algorithms: A Joint HW/SW Approach
MDPI Electronics, Volume: 10, pp. 2209, 2021
RI-25 Lauwers T.*, Glière A.*, Verdot Thierry*, Basrour S.
πFBG resonator used as a transducer for trace gas photothermal detection
Optics Express, Volume: 29, pp. 31796-31811, 2021
**Laboratoire d'Electronique de Technologie de l'Information*

International conferences (CI)

CI-16 Decoudu Y., Morin-Allory K., Fesquet L.
A High-Level Design Flow for Locally Body-Biased Asynchronous Circuits
29th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2021), 2021
CI-17 Akrarai M., Margotat Nils, Sicard Gilles*, Fesquet L.
A hybrid event-based pixel for low-power image Sensing
28th IEEE International Conference on Electronics Circuits and Systems (ICECS 2021), 2021
**Laboratoire d'Electronique de Technologie de l'Information*
CI-18 Akrarai M., Margotat Nils, Sicard Gilles*, Fesquet L.
An asynchronous hybrid pixel image sensor
27th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2021), 2021
**Laboratoire d'Electronique de Technologie de l'Information*
CI-19 Belot Jérémy*, Belot Jérémy, Cherkaoui A.*, Laurent Raphaël*, Fesquet L.
An Energy Efficient Multi-Rail Architecture for Stochastic Computing: A Bayesian Sensor Fusion Case Study
28th IEEE International Conference on Electronics Circuits and Systems (ICECS 2021), 2021
**HawAI.Tech*
CI-20 Iga R., Engels S.*, Engels S., Fesquet L.
Comparison between an ASK Event-Based Demodulation and a Digital IQ Demodulation
7th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP 2021), 2021
**STMicroelectronics [Crolles]*
CI-21 Bonnaud O.*, Fesquet L.
Distance learning is not an online face-to-face – Observations in microelectronic education
13th annual International Conference on Education and New Learning Technologies (EduLearn 2021), 2021
**Institut d'Electronique et de Télécommunications de Rennes, Université de Rennes 1 – Institut National des Sciences Appliquées (INSA Rennes) – SUPELEC, France*
CI-22 Ait Said N., Benabdenbi M., Morin-Allory K.
FPU Reduced Variable Precision in Time: Application to the Jacobi Iterative Method
IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2021), 2021
CI-23 El Hadbi A., El Issati O.*, Fesquet L.
Self-Timed Ring Oscillator Based Time-to-Digital Converter: a 0.35µm CMOS Proof-of-Concept Prototype
IEEE International Instrumentation & Measurement Technology Conference (I2MTC 2021), 2021
**STRS Laboratory*

Other communications (O)

O-5 Iga R., Iga R.*, Engels S., Engels S.*, Fesquet L.
A Novel Continuous TDC Measurement Technique
27th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2021), Portland, UNITED STATES
**STMicroelectronics [Crolles]*

Theses (T)

T-6 Gimenez G.
Design of secure and very low power circuits : an asynchronous alternative
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Feb 12, 2021
T-7 Lauwers T.
Optical transduction methods for the photoacoustic and photothermal detection of trace gas
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Mar 22, 2021

CNRS - Grenoble INP - UGA

RMS team

Reliable RF and Mixed-signal Systems

Reliable RF and Mixed-signal Systems (RMS team)

Description

The Reliable RF and Mixed-signal Systems group (**R**MS) is focused on the design, test and control of analog/mixed-signal/RF/mm-Wave integrated circuits and systems. 2021 has been a transition year for the **R**MS team, in preparation for the integration of the researchers in RFIC-Lab within the team in 2022. In this regard, the research axes of the team have evolved to better describe the wider scope of the team activities after the integration. Our research can be declined into the following four main axes:

Design of AMS-RF integrated circuits and systems

Novel AMS-RF design solutions are required in a wide variety of state-of-the-art applications, including communications, computing, imaging, etc. In this regard, the **R**MS group explores the multiple challenges of state-of-the-art AMS-RF current and emerging design paradigms, especially focusing on low-power and/or low-voltage applications. Our research includes the development of low-power mixed-signal and RF design techniques, state-of-the-art area-efficient high-resolution and ultra-low power data converters for imaging applications, integrated control electronics for quantum computing, and advanced RF design techniques for 5G and beyond-5G applications.

Integration and miniaturization of RF-mmW circuits

In this research axe our activities are focused on exploring novel integration solutions, including “More Moore” approaches, such as taking advantage of optimized Back-End-Of-Line metal stacks for integrating novel 3D passive structures, and “More-Than-Moore” approaches, where heterogeneous 2.5D and 3D solutions using mmW interposers.

Design for test and reliability of AMS-RF/mmW circuits and systems

Testing AMS-RF/mmW functions in a complex integrated system represent nowadays a major challenge for the IC industry. Our research in this area is focused on two main research lines: a) the development of AMS-RF-mmW state-of-the-art on-chip test instruments for Built-In Self-Test (BIST) applications and dedicated DfT techniques; and b) the development of novel indirect test methodologies based on the applications of advanced machine learning algorithms.

Control, optimization and self-healing of AMS/RF and mm-Wave circuits

In parallel with the test challenge, performance calibration and tuning are of key interest in the IC industry. Performance calibration in the production line enables a yield enhancement, while providing tuning capabilities during the lifetime of the circuit opens the door to self-healing applications and enhanced reliability. In this line, we develop optimized, minimally intrusive tuning knobs for performance calibration, together with novel performance control algorithms based on machine learning models.

Research milestones

- Non-intrusive mm-wave test: we have outlined and experimentally demonstrated a machine learning-based non-intrusive test methodology for mm-Wave circuits.
- Advanced modeling of mm-wave couplers for design enhancement: design-oriented model considering frequency-dependent electrical losses.
- Inversion-based design methodology for low-power LNA design.
- Design-oriented modeling of short-channel MOS transistors: based on the ACM model, we have developed a 7-parameter MOS transistor DC model including the main short-channel effects in advanced nanometric technologies.
- Quantum dot test structures have been fabricated in FD-SOI technology and the characteristic Coulomb blockade diagrams have been successfully measured.
- Ultra low-power and area-efficient high resolution analog to digital converter
- Low noise read-out for integrated quantum random number CMOS sensors
- First-ever OBT technique for mm-wave circuits: we have demonstrated the potential of Oscillation-Based Test techniques for the test and calibration of phased arrays.
- Development of Embedded Test Instruments for the static and dynamic test of state-of-the-art ADCs and for the characterization of clock jitter.
- Development of machine learning-based image quality evaluation and correction techniques.
- Low-cost controller synthesis: we have developed a software platform for automatic generation of logic control codes for a wide variety of low-cost microcontroller targets.
- Scheduling control for lifetime optimization in Wireless Sensor Nodes technologies: we have proposed a novel solution to the Maximum Lifetime Coverage Problem (MLCP) that takes into account the non-zero energy of nodes in sleep mode.

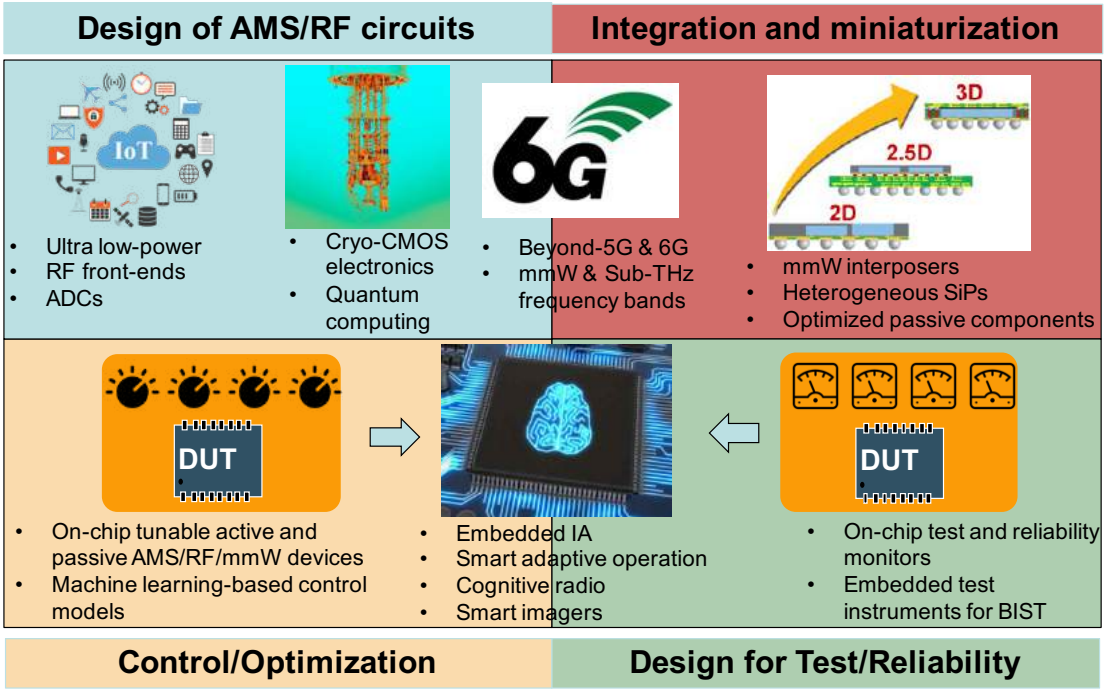


Figure 1: **R**MS research activities at a glance

Highlights of 2021 and of the recent years

International Cooperation

CETIC project : Low cost controller design; Embedded Programmable circuits (FPGA)
Scientific Manager: SIMEU E.
Partners: University of Yaoundé I
City: Yaoundé
Country: CAMEROON
Start the: Jan 01, 2016 until Dec 31, 2022

Conception de bits quantiques sur silicium
Scientific Manager: MIR S.
Partners: Université de Sherbrooke
City: Sherbrooke
Country: CANADA
Start the: Oct 25, 2018 until Dec 31, 2022

Machine learning-based test of AMS-RF-mmW circuits
Scientific Manager: BARRAGAN M.
Partners: Instituto de Microelectrónica de Sevilla
City: Sevilla
Country: Spain
Start: oct 1 2014 –

Memorandum of Understanding for Academic Collaboration with IIT Jodhpur
Scientific Manager: MIR S. and BARRAGAN M.
Partners: IIT Jodhpur
City: Jodhpur
Country: India
Start: may 1 2021

Invited Professor : Embedded systems in process control and monitoring applications
Scientific Manager: SIMEU E.
Partners: Université des Montagnes
City: Bangangte
Country: CAMEROON
Start the: November 2021

Invited Professor : Embedded systems
Scientific Manager: SIMEU E.
Partners: Ecole Centrale de Casablanca
City: Casablanca
Country: Morocco
Start the: November 2021

Invited professor: Instrumentation and signal processing for high energy physics and particle colliders
Partners: ESIPAP (European School of Instrumentation in Particle & Astroparticle Physics)
Scientific Manager: Daniel Dzahini
City: Geneva & Archamps
Country: world wide
Start: 2012

Awards

IFIP Silver Core Award for Salvador MIR
The IFIP Silver Core distinction is awarded by the IFIP General Assembly in every other year, in recognition of significant achievements of the recipient that are important from the point of view of the mission and goals of IFIP. Eligible are past and current members of any IFIP body (e.g. members of the General Assembly, members of Technical Committees, Committee officers, member of Working Groups) and people involved in organization of IFIP events, like chairs of Organization Committees, Chairs of Program Committees, etc.
Awardees 2021: P. Campos, M. Glesner, S. Mir, H. Petrie, G. Weber

Editorial work

Since 01/01/2020 : Daniel DZAHINI is part of the editorial board - Section Circuits and signal processing at MDPI (Publisher of Open Access Journals)
https://www.mdpi.com/

Academic and research members

Manuel BARRAGAN

Position
Researcher at CNRS

Responsibilities
Leader of RMS team
Reseacher in RMS team

Daniel DZAHINI

Position
Research engineer at CNRS

Responsibilities
Researcher in RMS team

MIR Salvador

Position
Research Director at CNRS

Responsibilities
Reseacher in RMS team

Emmanuel SIMEU

Position
Associate Professor at UGA – POLYTECH school

Responsibilities
Reseacher in RMS team

CNRS (French National Center for Scientific Research)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AGOUZOUL Abdelali
Title of thesis: **Modeling,Control/command,AI,Embedded electronics,Renewable energies,Optimization**
Expected date of defence: **2024**
Previous degrees: Engineer - EMSI, Maroc (2021)

2. BELKHADRA Oumayma
Title of thesis: **Self-tuning power amplifier in advanced CMOS technology for automotive radar**
Expected date of defence: **2024**
Previous degrees: Engineer – Enseirb-Matmeca (Toulouse), France (2020)

3. BONTEMS William Illich
Title of thesis: **Design of a 15-bit analog to digital converter for ultra low power applications**
Expected date of defence: **2023**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2020)

4. BRITTON OROZCO Giovani Crasby
Title of thesis: **Design of an FD-SOI read / control circuit dedicated to the field of quantum computing under Cryogenic conditions**
Expected date of defence: **2023**
Previous degrees: Engineer - Grenoble INP – Phelma, France (2020)

5. CHEGARI Badr
Title of thesis: **Contribution** towards **integrating optimal energy management systems for intelligent buildings**
Expected date of defence: **2022**
Previous degrees: Engineer - Université Ibn Zohr, Maroc (2017)

6. KRIEKOUKI Ioanna
Title of thesis: **Realization of quantum dot devices with embedded control in FD-SOI technology**
Expected date of defence: **2022**
Previous degrees: Engineer – Université Grenoble Alpes, France (2017)

7. MADHVARAJ Manasa
Title of thesis: **IPS for mixed-signal/high speed integrated circuits dependability and control**
Expected date of defence: **2023**
Previous degrees: Master of technology “VLSI design and embedded systems” – Bangalore, India (2015)

8. MAMGAIN Ankush
Title of thesis: **On-chip** generation **of high-frequency sinusoidal signals using harmonic cancellation techniques**
Expected date of defence: **2023**
Previous degrees: Master of technology “Electronic and communication engineering” – New Delhi, India (2014)

9. MELIS Tommaso
Title of thesis: **Diagnosis tool developement for failure analysis of analog and mixed signal devices**
Completed on: **December 14th, 2021**
Previous degrees: Engineer - Università degli Studi di Cagliari, Italy (2018)

10. SILVEIRA FEITOZA Renato
Title of thesis: **Strategies for Reduced-code Static Testing of SAR ADCs**
Completed on: **July 20th, 2021**
Previous degrees: Engineer – Pontifícia Universidade Católica do Rio de Janeiro, Brazil (2017)

11. TROUSSIER Chloé
Title of thesis: **Study of ESD/CDM stresses phenomena from elementary charged devices to package discharge: failure mechanism, protection strategy and predictive tools**
Expected date of defence: **2022**
Previous degrees: Engineer – IMT Atlantique Bretagne Pays de Loire, France (2018)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

No positions in 2021.

Visitors

No positions in 2021.

Interns and trainees

Name	Forename	Country	Duration
1. AYLAR	Mehmet	FRANCE	1 month 15 days
2. BERLINGARD	Quentin	FRANCE	3 months 6 days
3. HASSOUN	Khodor	FRANCE	3 months 12 days
4. MEDBOUHI	Mohammed	MOROCCO	2 months 11 days
5. PIROT	Yann	France	2 months 6 days

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2021.

ANRT

CIFRE Giovanni BRITTON (2020 – 2023)
Scientific manager: MIR Salvador
Team sharing (RFIC Lab, RMS)

CIFRE Chloé TROUSSIER (2018 – 2021)
Title: "Etude des phénomènes de décharge électrostatique (ESD/CDM) : du composant au circuit intégré"
Scientific manager: SIMEU Emmanuel

CIFRE Tommaso MELIS (2018 – 2021)
Title: "Développement d'outils de diagnostic pour l'analyse des défaillances des circuits intégrés analogiques et mixtes"
Scientific manager: SIMEU Emmanuel

CIFRE Ioanna KRIEKOUKI (2018 – 2021)
Title: "Fabrication et caractérisation de bits quantiques avec contrôle embarqué en technologie 28nm UTBB FD-SOI et au delà à température cryogénique"
Scientific manager: MIR Salvador

COLLECTIVITES TERRITORIALES

MESSI (2019 – 2022)
Program: nano 2022
Title: Mixed-Signal Self-Test IPs for on-chip testing and technology qualification
Scientific manager: MIR Salvador

INDUSTRIE

XDIGIT -Easytech 2020 (2020 – 2021)
Program: PYXCAD/EASYTECH
Title: "Développement microélectronique pour la technologie MASSAR"
Scientific manager: MIR Salvador

Organization and participation of international conferences, workshops, forums

Design, Automation & Test in Europe (DATE'2021)
February 1-5, 2021, Virtual event, GERMANY
Rang : A+
Topic chair: BARRAGAN M.

26th IEEE European Test Symposium (ETS'2021)
May 24-28, 2021, Virtual event, BELGIUM
Rang : A
program vice-chair: MIR S.
technical program committee: BARRAGAN M., MIR S.

5th International Conference on Control, Automation and Diagnosis (Control Automation and Diagnosis) (ICCAD'2021)
November 3-5, 2021, Grenoble, FRANCE
Rang : NC
industry/research committee: SIMEU E.
technical program committee: SIMEU E.

27th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2021)
June 28-30th, 2021, Virtual event, ITALY
Rang : B
general chair: NICOLAIDIS M.
technical program committee: BARRAGAN M., MIR S., SIMEU E.

22nd IEEE Latin-American Test Symposium (LATS'2021)
October 27-29, 2021, Virtual event
Rang : NC
publication chair: SIMEU E.
technical program committee: MIR S.

19th IEEE Interregional NEWCAS Conference (NEWCAS'2021)
June 13-16, 2021, Virtual event
Rang : B
finance chair: FOURNERET-ITIÉ A.-L.
technical program chair: BARRAGAN M.

Test Spring School (TSS'2021)
May 17-23, 2021, Virtual event
Rang : NC
technical program committee: MIR S.

29th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC'2021)
October 4-8, 2021, Singapore, SINGAPORE
Rang : A
steering committee member: MIR S.
Topic chair: MIR S.

39th VLSI Test Symposium (VTS'2021)
April 25-28, 2021, Virtual event, FRANCE
Rang : A
technical program committee: BARRAGAN M., MIR S.

12th Latin American Symposium on Circuits and Systems (LASCAS'2021)
February 21, 2021 to February 25, 2021, virtual, Peru
Rang B
Technical program committee: MIR S.

IEEE International Symposium on Circuits and Systems (ISCAS'2021)
May 22-28, virtual, Korea
Rang A
Technical program committee: BARRAGAN, M.

IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD 2021)
Jul 19, 2021 - Jul 22, 2021, Virtual event
Rang: B
Technical program committee: BARRAGAN M.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
POLYTECH GRENOBLE				
Manager of Risks Prevention Management department	SIMEU E.	01/09/2017		
Restricted council member	SIMEU E.	01/09/2017		Examine promotion files, invited professors, teaching assistants
School council member	SIMEU E.	01/09/2017		Elected members - School Strategy, relations with industrial partners
Research structures				
S.mart Grenoble Alpes **Pôle d'équipements et d'expertises pour vos projets d'industrialisation**				
Manager of CIM S.mart Grenoble Alpes	SIMEU E.	01/09/2015		
EEATS doctoral school **Électronique Électrotechnique Automatique & Traitement du signal**				
Council member of EEATS doctoral school	SIMEU E.	01/09/2017		

Scientific production

International journals (RI)

RI-26 Takam Tchendjou G., Simeu E.
Detection, Location and Concealment of Defective Pixels in Image Sensors
IEEE Transactions on Emerging Topics in Computing, Volume: 9, pp. 664-679, 2021
RI-27 Margalef-Rovira M.*, Pelletier Géraldine, Avramovic V.*, Lepilliet S.*, Bourgeat J.***, Duchamp J.M.****, Barragan M., Pistono E.**, Bourdel S.**, Gaquière C.*, Ferrari Philippe****
ESD mm-Wave-Circuit Protection: 3-dB Couplers
IEEE Transactions on Electron Devices, Volume: , pp. 1-6, 2021
**IEMN - Institut d'électronique, de microélectronique et de nanotechnologie, **RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits, ***STMicroelectronics [Crolles], ****Laboratoire de Génie Electrique de Grenoble*
RI-28 David Jean-Pierre*, Barragan M.
Guest Editorial Special Issue on the IEEE International NEWCAS Conference 2020
IEEE Transactions on Circuits and Systems, Volume: 68, pp. 1-2, 2021
**Ecole Polytechnique de Montréal*
RI-29 Nzebop Ndenoka Gérard*, Tchuente Maurice, Simeu E.**
Langage et sémantique des expressions pour la synthèse de modèle Grafcet dans un environnement IDM Language and semantics of expressions for Grafcet model synthesis in a MDE environment
ARIMA - Revue Africaine de la Recherche en Informatique et Mathématiques Appliquées, Volume: 33, 2021
**Université de Yaoundé I, ** Laboratoire International de Recherche en Informatique et Mathématiques Appliquées*
RI-30 Margalef-Rovira M.*, Occello O., Saadi A.***, Avramovic V.*, Lepilliet S.*, Vincent Loïc****, Barragan M., Pistono E.**, Bourdel S.**, Gaquière C.*, Ferrari Philippe****
Mm-wave through-load element for on-wafer measurement applications
IEEE Transactions on Circuits and Systems, Volume: , pp. 1-14, 2021
**IEMN - Institut d'électronique, de microélectronique et de nanotechnologie, **RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits, ***NXP Semiconductors (Eindhoven, Netherlands), ****CIME Nanotech - Centre Interuniversitaire de Micro-Electronique*
RI-31 Chegari B., Tabaa M.*, Simeu E., Moutaouakkil F., Moutaouakkil F.***, Medromi H.**, Medromi H.*****
Multi-objective optimization of building energy performance and indoor thermal comfort by combining artificial neural networks and metaheuristic algorithms
Energy and Buildings, Volume: 239, pp. 110839, 2021
**EMSI - Ecole Marocaine des Sciences de l'Ingénieur, **ENSEM - École nationale supérieure d'électricité et mécanique de Casablanca, ***UH2MC - Université Hassan II de Casablanca*
RI-32 Agouzoul Abdelali*, Tabaa M.*, Chegari B., Simeu E., Dandache A., Alami Karim***
Towards a Digital Twin model for Building Energy Management: Case of Morocco
Procedia Computer Science, Volume: 184, pp. 404-410, 2021
**LPRI - Laboratoire Pluridisciplinaire de recherche et innovation , **LGIPM - Laboratoire de Génie Informatique, de Production et de Maintenance*
RI-33 Takam Tchendjou G., Simeu E.
Visual Perceptual Quality Assessment Based on Blind Machine Learning Techniques
Sensors, Volume: 22, pp. 175, 2021

Invited conference talks (INV)

INV-5 Melis T.
Automated Analog Fault Simulators: Application to Failure Analysis
26th IEEE European Test Symposium (ETS 2021), 2021

International conferences (CI)

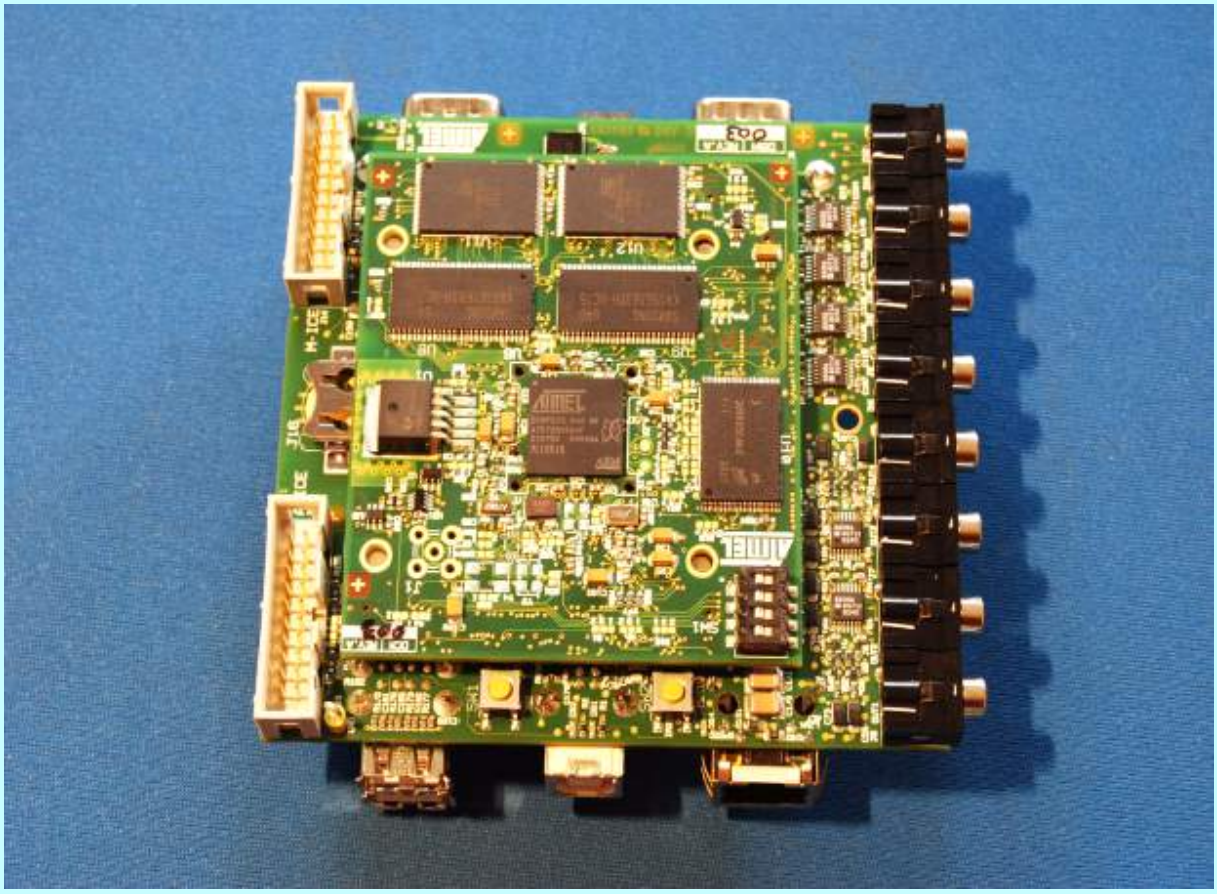
CI-24 Bourdel S.*, Subias S.*, Bouchoucha Mohamed Khalil*, Barragan M., Cathelin Andreia, Galup Carlos*****
A gm/ID Design Methodology for 28 nm FD-SOI CMOS Resistive Feedback LNAs
28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2021), pp. 1-4, 2021
**RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits, **STMicroelectronics [Crolles], ***UFSC - Universidade Federal de Santa Catarina = Federal University of Santa Catarina [Florianópolis]*
CI-25 Mamgain Ankush, Barragan M., Mir S.
Analysis and mitigation of timing inaccuracies in high-frequency on-chip sinusoidal signal generators based on harmonic cancellation
IEEE European Test Symposium (ETS 2021), pp. 1-6, 2021
CI-26 Troussier C., Bourgeat J.*, Jacquier B.*, Simeu E., Arnould J.D.**
Estimation of Oxide Breakdown Voltage During a CDM Event Using Very Fast Transmission Line Pulse and Transmission Line Pulse Measurements
IEEE International Reliability Physics Symposium (IRPS 2021), 2021
**STMicroelectronics [Crolles], **RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits*
CI-27 El-Chaar M.*, Lisboa de Souza A.A., Barragan M., Podevin F.*, Bourdel S.*, Arnould J.D.***
Integrated Wideband Millimeter-Wave Bias-Tee – Application to Distributed Amplifier Biasing
19th IEEE International New Circuits and Systems Conference (NEWCAS 2021), pp. 1-4, 2021
**RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits, **UFPB - Universidade Federal da Paraiba*
CI-28 Margalef-Rovira M.*, Gaquière C.*, Lisboa de Souza A.A., Vincent Loïc***, Barragan M., Pistono E.****, Podevin F.****, Ferrari Philippe******
Mm-wave single-pole double-throw switches: HBT-vs MOSFET-based designs
19th IEEE International New Circuits and Systems Conference (NEWCAS 2021), 2021
**IEMN - Institut d'électronique, de microélectronique et de nanotechnologie, **UFPB - Universidade Federal da Paraiba, ***CIME Nanotech - Centre Interuniversitaire de Micro-Electronique, ****RFIC-Lab - Laboratoire de Radio-Fréquences et d'Intégration de Circuits*

Theses (T)

T-8 Melis T.
Diagnosis tool development for failure analysis of analog and mixed signal devices
These de Doctorat, Université Grenoble Alpes, spécialité "Nanoélectronique et Nanotechnologies", Dec 14, 2021
T-9 Silveira Feitoza R.
Strategies for Reduced-code Static Testing of SAR ADCs Strategies
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Jul 20, 2021

CNRS - Grenoble INP - UGA

SLS team



System Level Synthesis

System Level Synthesis (SLS team)

Research activities

The SLS team focuses on (a) highly efficient architectures for general purpose computing or AI-dedicated algorithms, (b) system-level modeling and design methodology: specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware. The work of the team is included in the Laboratory themes “Hardware/software codesign” and “Simulation and verification of systems” described below.

Hardware/software codesign

Our research on high performance general purpose processors explores the use of value prediction in processor design. We have shown that simple value prediction can be implemented by reusing existing pipeline structures, leading to increased performance with reduced overheads. We have also shown that predicting values enables the dynamic "reduction" of some instructions (e g., transforming an add into a nop at runtime), which further improves performance. So far, we have considered value prediction for out-of-order microarchitectures only. In the meantime, through a collaboration with University of Murcia in Spain, we have shown that conservative implementations of atomic read-modify-write instructions (which are used to write higher-level synchronization primitives) in x86 processors incurred significant overhead and proposed a more aggressive implementation to significantly reduce the time spent synchronizing threads.

Multi-core and many-core architectures have evolved towards a set of clusters. Each cluster integrates a set of cores, a cache memory and a local memory shared by all the cores of the cluster. We have worked on hardware methods for distributing memory bank accesses in many-core architectures by experimenting on the MPPA Kalray processor. In addition, we have proposed an innovative hardware support for synchronization locks. This decentralized solution manages dynamic re-homing of locks in a dedicated memory, close to the latest access-granted core.

On the dedicated architecture side, the team is still working on Artificial Intelligence. After our work on high-throughput ternary neural network, we have collaborated with the university of Salerno on the design of a tiny Binary Neural Network for human recognition applications.

Through a collaboration with OVHcloud, we also worked on a dedicated IP used in their mitigation systems to face Distributed Denial-of-Service (DDOS) attacks. In this domain, hard- ware development has to be agile. By introducing the Chisel hardware construction language in the hardware design flow, we showcase how Chisel unleashes the power of agile development methodologies through development iterations. We have also shown through a General Matrix Multiply implementation case study that Chisel can be used to generate highly parametrizable circuits, bringing huge benefits in design exploration, reuse and designer productivity.

Simulation and verification of systems

Modeling and simulation of cyber-physical devices is challenging because of their heterogeneity: discrete events simulation progresses by discrete timesteps while continuous time simulation does so in a time continuum. The SystemC AMS synchronization strategy is based on fixed timesteps and can generate inaccuracies overcame only at expanse of simulation speed. We have proposed a new continuous time and discrete events synchronization algorithm on top of the SystemC framework and have proven its causality, completeness and liveness. In addition, we have also proposed an adaptive algorithm to adjust the synchronization step to provide near to optimum simulation speed. Results on various cases studies have demonstrated that our algorithm circumvents these challenges, attains high accuracy with respect to established tools, and improves simulation speed. This work aims at enlarging the modeling and simulation capabilities of SystemC as a heterogeneous design tool.

Today’s SoCs require a complex design and verification process. In early design stages, high-level debugging of the SoC functionality is feasible on TLM (Transaction-Level Modeling) descriptions. To ease debugging of such SoC’s models, Assertion-Based Verification (ABV) enables the runtime verification of temporal properties. In the last design stages, RTL (Register Transfer Level) descriptions of hardware blocks expose microarchitectural details. To gain confidence in the validity of system level properties after this TLM-to-RTL synthesis, transaction level assertions must be reverifiable on RTL models. To address that issue, we propose refinement rules for the automatic system level to signal level transformation of PSL assertions (Property Specification Language, IEEE standard 1850).

Many scientific applications require higher accuracy than what can be represented on 64 bits of the floating-point IEEE 754 standard, and to that end make use of dedicated arbitrary precision software libraries such as MPRF. To reach a good performance/accuracy trade-off, developers use variable precision, requiring e.g. more accuracy as the computation progresses. Hardware accelerators for this kind of computations do not exist yet, and independently of the actual quality of the underlying arithmetic computations, defining the right instruction set architecture, memory representations, etc, for them is a challenging task. We have investigated the support for arbitrary and variable precision arithmetic in a dynamic binary translator (QEMU implementation), to help gain an insight of what such an accelerator could provide as an interface to compilers, and thus programmers. Through collaborations, we also worked on a FP representation supporting both static and dynamically variable precision: by designing its compilation flow to hardware FP instructions or software libraries, and by demonstrating its performance, far better than the Boost programming interface for the MPFR library on the PolyBench suite. Simulations of manycores architectures take a lot of time with gem5 (simulator used for manycores architectures), to improve this point we explore the accuracy of QEMU. QEMU used the DBT (Dynamic Binary Translation) mechanism which transforms instructions from a target ISA to a host ISA. In our experimentations, the target ISA is RISC-V, several of the team works used RISC-V eco-system. To reduce the simulation time of manycores architectures with QEMU, we propose to pin vCPUs (virtual CPUs simulated by QEMU) to physical CPUs on the host,

e.g. forcing vCPU to run on a chosen physical CPU. PARSEC benchmarks are used to obtain results. Unfortunately, pinning vCPUs does not improve the execution time of our programs. Simulators based on the DBT are fast because they focus on instructions and do not modeling architecture. We propose to add the cache representation in QEMU to improve the accuracy.

Highlights of 2021 and of the recent years

International Cooperation

Academic and research members

Liliana ANDRADE

Position
Associate professor at UGA

Responsibilities
Researcher in SLS team

Julie DUMAS

Position
Associate professor at Grenoble INP – ENSIMAG school

Responsibilities
Researcher in SLS team since 01/09/2021

Olivier MULLER

Position
Associate professor at Grenoble INP – ENSIMAG school

Responsibilities
Leader of SLS team
Researcher in SLS team

Arthur PERAIS

Position
Researcher at CNRS

Responsibilities
Researcher in SLS team

Frédéric PÉTROT

Position
Professor at Grenoble INP – ENSIMAG school

Responsibilities
Researcher in SLS team

Laurence PIERRE

Position
Professor at UGA – IM2AG school

Responsibilities
Researcher in SLS team

Frédéric ROUSSEAU

Position
Professor at UGA – POLYTECH school

Responsibilities
Researcher in SLS team

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. BADAROUX Marie
Title of thesis: **Fast and accurate simulation of multi/many-core SoCS**
Expected date of defence: **2023**
Previous degrees: Master – Grenoble INP – Ensimag, France (2020)

2. BAIN Nathan
Title of thesis: **Methods for the learning and adapting formal neural networks to the constraints of hardware accelerators for applications optimized in power and / or throughput**
Expected date of defence: **2023**
Previous degrees: Master – Grenoble INP – Phelma, France (2020)

3. BAUMELA Thomas
Title of thesis: **Integrating devices in FPGA using an end-to-end hardware/software co-designed message-based approach**
Completed on: **February 24th, 2021**
Previous degrees: Engineer – Université Grenoble Alpes, France (2016)

4. BONICEL Louis
Title of thesis: **Study of an architectural model for code generation taking into account the real time constraints of an embedded system in the electrical measure and protection domain**
Expected date of defence: **2022**
Previous degrees: Engineer – Polytech Montpellier, France (2017)

5. BRUANT Jean
Title of thesis: **Abstracting FPGA development flow as a modern software development flow**
Expected date of defence: **2022**
Previous degrees: Engineer - Télécom Bretagne, France (2018)

6. CHRIST Maxime
Title of thesis: **Learning in very low precision**
Expected date of defence: **2022**
Previous degrees: Engineer - INSA Lyon, France (2017)

7. FERNANDEZ-MESA Breytner Joseph
Title of thesis: **Exploration of Direct Synchronization Approaches for a High-Level and Unified Simulation of Discrete-Event/Continuous-Time Systems**
Completed on: **October 14th, 2021**
Previous degrees: Engineer – Universidad de Los Andes – Mérida, Venezuela (2017)

8. FERRES Bruno
Title of thesis: **Flexible Leveraging** Hardware **Construction Languages for Design Space Exploration on FPGA**
Expected date of defence: **2022**
Previous degrees: Engineer – Grenoble INP - Ensimag, France (2018)

9. TREVISAN JOST Tiago
Title of thesis: **Compilation and optimizations for variable precision floating-Point arithmetic: from language and libraries to code generation**
Completed on: **July 2nd, 2021**
Previous degrees: Master – Federal University of Rio Grande do Sul, Brazil (2017)

10. VIANES Arthur
Title of thesis: **Integration of a Manycore Accelerator in a High-Performance Processor**
Expected date of defence: **2022**
Previous degrees: Engineer Polytech Grenoble, France (2018)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

Name	Forename	Country	Duration
BAUMELA	Thomas	FRANCE	9 months
PINZARI	Ana	FRANCE	4 months
TREVISAN JOST	Tiago	BRAZIL	23 days

Visitors

No positions in 2021.

Interns and trainees

Name	Forename	Country	Duration
1. DJEAFEA SONWA	Medric Bruel	CAMEROON	
2. HAMAIN	Thomas Frederic Robert	RUSSIAN FED	
3. LAGAROSSE	Paul	FRANCE	
4. ROBE	Guillaume	FRANCE	
5. YADAV	Archit	INDIA	
6. ZHANG	Shuo	CHINA	
7. KEMEH	Marck-Edward	GHANA	

Name	Forename	Country	Duration
CANTORI	Thibaut	FRANCE	2 months 3 days
DEVRIESERE	Aymeric	FRANCE	2 months 9 days
LIANG	Jichen	CHINA	5 months 26 days
MARTIN	Maxime	FRANCE	2 months 20 days
NOELLE	Léo	FRANCE	3 months 17 days
PORTAS-PITTET	Fabien	FRANCE	2 months 22 days
RAVENEL	Pierre	FRANCE	2 months 20 days
SHIMOU	Yasser	MOROCCO	5 months 16 days
VIOLET	Florian	FRANCE	3 months 17 days

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANR

MAPLURINUM (2021 – 2025)
Title: Machinae pluribus unum - (faire) une seule machine avec plusieurs
Partners: Telecom SudParis Evry - Institut National de Recherche en Informatique et en Automatique (INRIA) - Centre Rennes-Bretagne Atlantique – CEA Saclay

RAKES (2019 – 2023)
Scientific manager: PETROT Frédéric

ANRT

CIFRE Arthur VIANES (2019 – 2022)
Scientific manager: ROUSSEAU Frédéric

CIFRE Jean BRUANT (2018 – 2022)
Scientific manager: MULLER Olivier

CIFRE Louis BONICEL (2018 – 2021)
Title: "Etude d'un modèle architectural pour la génération de code intégrant les contraintes d'un système temps réel embarqué dans le domaine de la mesure et la protection électrique"
Scientific manager: PETROT Frédéric

CEC-NATIONAL

AI4DI (2019 – 2022)
Program: ECSEL
Title: Artificial Intelligence for Digitizing Industry
Scientific manager: PETROT Frédéric

EPST

Digital Hardware AI Architectures (2019 – 2023)
Program: MIAI (Multidisciplinary Institute in Artificial Intelligence)
Scientific manager: PETROT Frédéric

Organization and participation of international conferences, workshops, forums

Design, Automation & Test in Europe (DATE'2021)
February 1-5, 2021, Virtual event, GERMANY
Rank: A+
University Booth Co-Chair: PETROT F.

24th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS'2021)
April 7-9, 2021, Vienna (virtual event), AUSTRIA
Rank: B
technical program committee: PIERRE L.

13th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO'2021)
January 20, 2021, Budapest, HUNGARY
Rank: NC
technical program committee: PETROT F.

32nd International Workshop on Rapid System Prototyping (RSP'2021)
October 14, 2021, Virtual event
Rank: B
program co-chair: ROUSSEAU F.
publication chair: MULLER J.D.
steering committee member: PETROT F.
steering committee member: ROUSSEAU F.
technical program committee: MULLER O.
technical program committee: PETROT F.
technical program committee: ROUSSEAU F.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
ENSIMAG school École nationale supérieured'informatique et de mathématiques appliquées				
Deputy Director	PETROT F.	01/09/2018	31/08/2022	
	MULLER O.	01/09/2017		
Restricted council member	PETROT F.	01/09/2017		Examine promotion files, invited professors, teaching assistants
	MULLER O.	01/09/2017		
School council member	PETROT F.	01/09/2017		Elected members - School Strategy, relations with industrial partners
POLYTECH GRENOBLE				
Manager of E2I branch	ANDRADE L.L.	01/10/2019		5th year - Apprenticeship training
Deputy director in charge of education and training	ROUSSEAU F.	01/09/2018		
Manager of Risks Prevention department	ROUSSEAU F.	01/09/2017		
Restricted council member	ROUSSEAU F.	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Research commission member	PIERRE L.	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR Council member	PIERRE L.	01/09/2017		
TIMA Laboratory				
Laboratory contact for european projects	ROUSSEAU F.	01/09/2017		
Research structures				
EEATS doctoral school Électronique Électrotechnique Automatique & Traitement du signal				
HDR commission member of EEATS doctoral school	ROUSSEAU F.	01/09/2017		
MSTII doctoral school Mathématiques, Sciences et Technologies de l'Information, Informatique				
Council member of MSTII doctoral school	PIERRE L.	01/09/2017		
HDR commission member of MSTII doctoral school	PETROT F.	01/09/2017		
LABEX PERSYVAL Pervasive Systems and Algorithms				
Education Board Member	PIERRE L.	01/06/2015		Training activities
MSTIC pole Mathématiques, sciences et technologies de l'information et de la communication				
TIMA representative of MSTIC cluster	PETROT F.	01/09/2016		
Parent institutions				
UGA Université Grenoble Alpes				
Manager of Informatics Master M1-M2 UGA – G-INP	PIERRE L.	01/09/2017		In charge for UGA

Scientific production

International journals (RI)

RI-34 Perais A.
A Case for Speculative Strength Reduction
IEEE Computer Architecture Letters, Volume: 20, pp. 22-25, 2021
RI-35 France-Pillois M.*, Martin J.*, Rousseau F.
A Non-intrusive Tool Chain to Optimize MPSoC End-to-end Systems
ACM Transactions on Architecture and Code Optimization , Volume: 18, 2021
**Laboratoire d'Electronique de Technologie de l'Information*
RI-36 Sasongko A.*, Kumara I.M. Narendra*, Wicaksana A., Rousseau F., Muller O.
Hardware Context Switch-based Cryptographic Accelerator for Handling Multiple Streams
ACM Transactions on Reconfigurable Technology and Systems (TRETS) , Volume: 14, 2021
**Institut Teknologi Bandung*
RI-37 Christ M.*, Christ M., Forget L.*, De Dinechin F.*
Lossless Differential Table Compression for Hardware Function Evaluation
IEEE Transactions on Circuits and Systems II: Express Briefs, Volume: , pp. 1642 - 1646, 2021
**CITI-INSA Lyon-Centre of Innovation in Telecommunications and Integration of services*
RI-38 Pierre L.
Refinement rules for the automatic TLM-to-RTL conversion of temporal assertions
Integration, the VLSI Journal, Volume: 76, pp. 190-204, 2021
RI-39 Fernandez-Mesa B.J., Andrade Porras L.L., Pétrot F.
Synchronization of Continuous Time and Discrete Events Simulation in SystemC
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 40, pp. 1450 - 1463, 2021
RI-40 Bruant J.*, Bruant J., Horrein P.H.*, Muller O., Groleat T.*, Pétrot F.
Towards Agile Hardware Designs with Chisel: a Network Use-case
IEEE Design & Test, Volume: , 2021
**OVH*

Invited conferences talks (INV)

INV-6 Andrade Porras L.L., Baumela T., Pétrot F., Briand David*, Bichler Olivier*, Coppola M.**
Efficient Deep Learning Approach for Fault Detection in the Semiconductor Industry
European Nanoelectronics Applications Design & Technology Conference (ADTC 2021), 2021
**Laboratoire Intelligence Artificielle Embarquée , **STMicroelectronics [Crolles]*
INV-7 Pétrot F., Prost-Boucle A.*, Bourge A., Andrade Porras L.L., Baumela T., Pinzari Ana**
Hardware-friendly AI algorithms: Ternary Neural Networks
HiPEAC Computing Systems Week (HiPEAC 2021), 2021
**Synopsys Inc. (Montbonnot), **Atos Bull*

International conferences (CI)

CI-29 Badaroux M., Pétrot F.
Arbitrary and Variable Precision Floating-Point Arithmetic Support in Dynamic Binary Translation
26th Asia and South Pacific Design Automation Conference (ASP-DAC 2021), 2021
CI-30 Bonicel L.*, Bohrer R.*, Leprettre B.*, Pétrot F., Rousseau F.
Component Based Framework for Designing and Validating Asynchronous Algorithms for Electrical Measurement and Protection
4th IEEE International Conference on Industrial Cyber-Physical Systems (ICPS 2021), 2021
**Schneider Electric Industries*
CI-31 Perais A.
Leveraging Targeted Value Prediction to Unlock New Hardware Strength Reduction Potential
IEEE/ACM International Symposium on Microarchitecture (MICRO 2021), 2021
CI-32 Morgan F.*, Beretta A.*, Gallivan I.*, Clancy J.*, Rousseau F., Callaly F.*
RISC-V Online Tutor and Lab
International Conference on Remote Engineering and Virtual Instrumentation (REV 2021), 2021
**NUI - National University of Ireland [Galway]*
CI-33 Trevisan Jost T.*, Trevisan Jost T., Durand Y.*, Fabre Ch.*, Cohen A., Pétrot F.**
Seamless Compiler Integration of Variable Precision Floating-Point Arithmetic
International Symposium on Code Generation and Optimization (CGO 2021), 2021
**Laboratoire d'Electronique de Technologie de l'Information, **Google Inc [Mountain View]*
CI-34 Fernandez-Mesa B.J., Andrade Porras L.L., Pétrot F.
Simulation of Ideally Switched Circuits in SystemC
Asia and South Pacific Design Automation Conference (ASP-DAC 2021), 2021
CI-35 Badaroux M., Miroddi Saverio*, Pétrot F.
To Pin or Not to Pin: Asserting the Scalability of QEMU Parallel Implementation
24th Euromicro Conference on Digital System Design (Euromicro DSD/SEAA 2021), pp. 238-245, 2021
**Ticketsolve*

Book chapters (CH)

CH-2 De Luca Cristina*, Lippmann Bernhard*, Schober Wolfgang, Al-Baddai Saad**, Pelz Georg*, Rojko Andreja***, Pétrot F., Coppola M.****, John Rainer*****
AI in Semiconductor Industry
Artificial Intelligence for Digitising Industry, pp. 105-112, 2021
**Infineon Technologies AG [Munich - Germany], **Infineon Technologies AG [Regensburg - Germany], ***Infineon Technologies AG [Villach - Austria], ****STMicroelectronics [Grenoble], *****AVL List GmbH*
CH-3 Wicaksana A., Muller O., Rousseau F., Sasongko A.*
Maintaining Communication Consistency during Task Migrations in Heterogeneous Reconfigurable Devices
Multi-Processor System-on-Chip 1: Architectures, 1, pp. 255-285, 2021
**Institut Teknologi Bandung*
CH-4 Faravelon A., Gruber O.*, Pétrot F.
Removing Load/Store Helpers in Dynamic Binary Translation
Multi-Processor System-on-Chip, Electronics Engineering, pp. 133-160, 2021
**LIG - Laboratoire d'Informatique de Grenoble*
CH-5 Vianes A., Vianes A.*, Rousseau F.
Study and Comparison of Hardware Methods for Distributing Memory Bank Accesses in Many-core Architectures
Multi-Processor System-on-Chip 1: Architectures, 1, pp. 161-194, 2021
**Kalray*

Books and edited publications (L)

L-1 Andrade Porras L.L., Rousseau F.
Multi-Processor System-on-Chip 1: Architectures
, Wiley, Chichester, UK, 2021
L-2 Andrade Porras L.L., Rousseau F.
Multi-Processor System-on-Chip 2: Applications
, Wiley, Chichester, UK, 2021

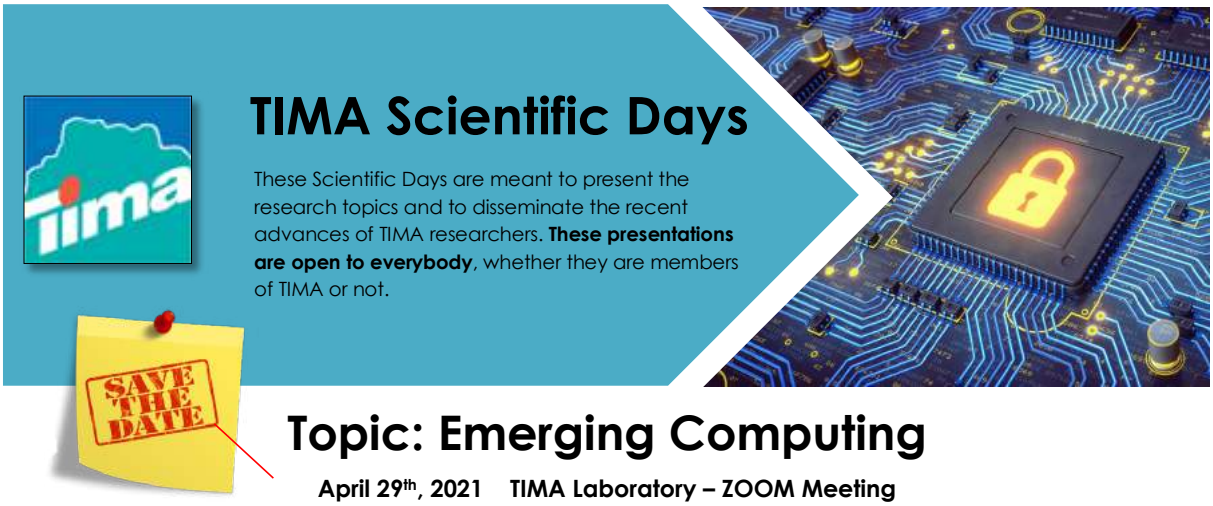
Theses (T)

T-10 Baumela T.
Externalisation of device drivers from embedded processors to devices
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Feb 24, 2021
T-11 Fernandez-Mesa B.J.
Exploration of Direct Synchronization Approaches for a High-Level and Unified Simulation of Discrete-Event/Continuous-Time Systems
These de Doctorat, Université Grenoble Alpes, spécialité "Informatique", Oct 14, 2021
T-12 Trevisan Jost T.
Compilation and optimizations for variable precision floating-Point arithmetic: from language and libraries to code generation
These de Doctorat, Université Grenoble Alpes, spécialité "Micro et Nano Electronique", Jul 02, 2021

Scientific animation

Scientific Days 2021

Scientific Days are meant to present the research topics and to disseminate the recent advances of researchers. These presentations are open to everybody, whether they are members of TIMA or not.



	Program
14h00 – 14h10	Ioana Vatajelu – **Emerging Topics in Computing** – Brief introduction
14h10 – 14h30	*Approximate Computing – Noureddine Ait-Said*
14h30 – 14h50	*Bayesian Systems – Jeremy Belot*
14h50 – 15h10	Quantum Computing – Ioanna Kriekouki
15h10 – 15h30	*Break*
15h30 – 15h50	*In-Memory Computing – Merlin Gerbaud*
15h50 – 16h10	*In-Memory Computing – Pietro Inglese*
16h10 – 16h30	*Spiking Neural Networks – Salah Daddinounou*

For more information, please contact: Ioana Vatajelu <ioana.vatajelu@univ-grenoble-alpes.fr>

TIMA Scientific Days

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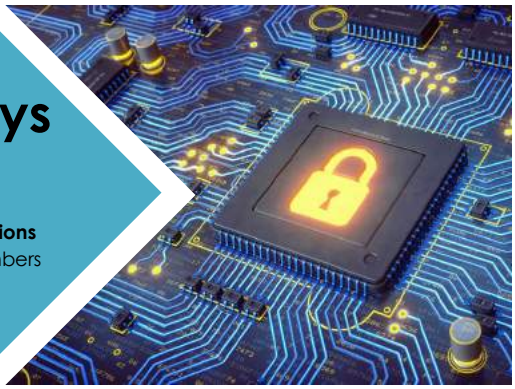

RISC-V in Research and Education

– TIMA / LCIS / VERIMAG Laboratories –

July 9th, 2021 – ZOOM Meeting

Hardware Security | Robustness, Reliability, Test | Emerging Computing | **Hardware/ software codesign** | Simulation and verification | Async design, non-uniform sampling | AMS/RF circuits and systems | Sensors and Actuators

	Program
9h00 – 9h10	Brief introduction
9h10 – 9h40	*RISC-V: An Opportunity for Research and Education – Noureddine Ait-Said*
9h40 – 10h10	*An In-Depth Vulnerability Analysis of RISC-V Micro-architecture Against Fault Injection Attack – Zahra Kazemi*
10h10 – 10h40	Microarchitecture-aware Fault Models: Experimental Evidence and Cross-Layer Inference Methodology – Ihab Alshaer
10h40 – 11h00	*Break*
11h00 – 11h30	*Introducing Scheduling Optimizations in CompCert with a posteriori verification – Cyril Six*
11h30 – 12h00	*Formally-verified Compiler Optimizations for Simple Embedded Cores* – Léo Gourdin

For more information, please contact: Liliana Andrade – liliana.andrade@univ-grenoble-alpes.fr

Join Zoom Meeting
https://univ-grenoble-alpes-fr.zoom.us/j/92323210689?pwd=OUZlOXB0NExtekE2aHprcDcrRS8xZz09

Meeting ID: 923 2321 0689

Passcode: 563130

TIMA Laboratory
46 avenue Félix Viallet - 38031 GRENOBLE – FRANCE
http://tima.univ-grenoble-alpes.fr/tima/fr/index.html

TIMA Scientific Days

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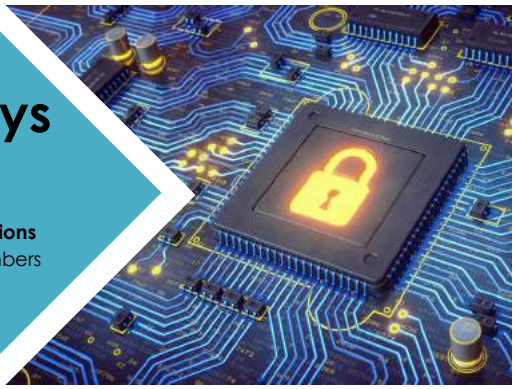

RISC-V in Research and Education

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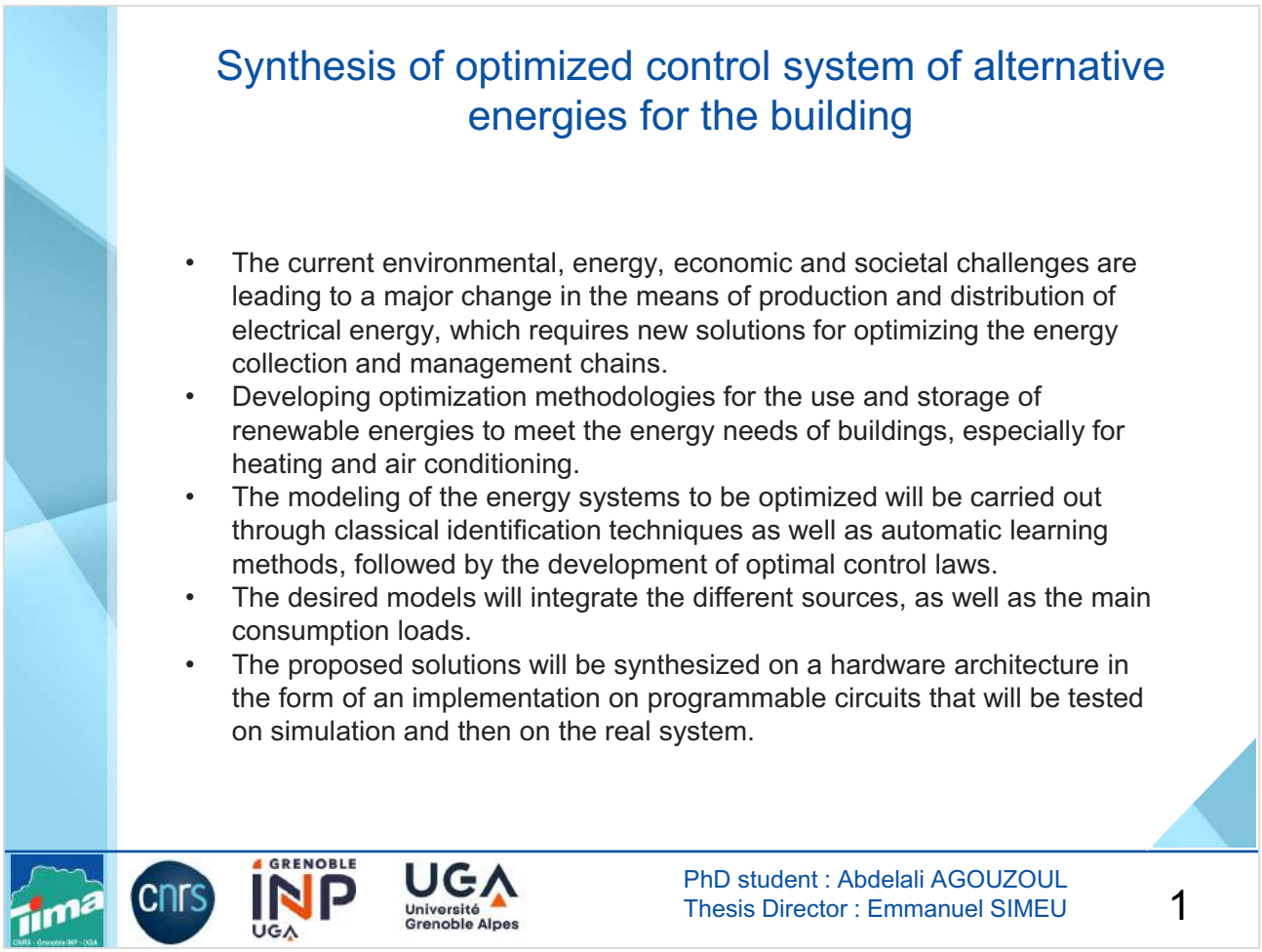
PhD day – Nov. 18th, 2021

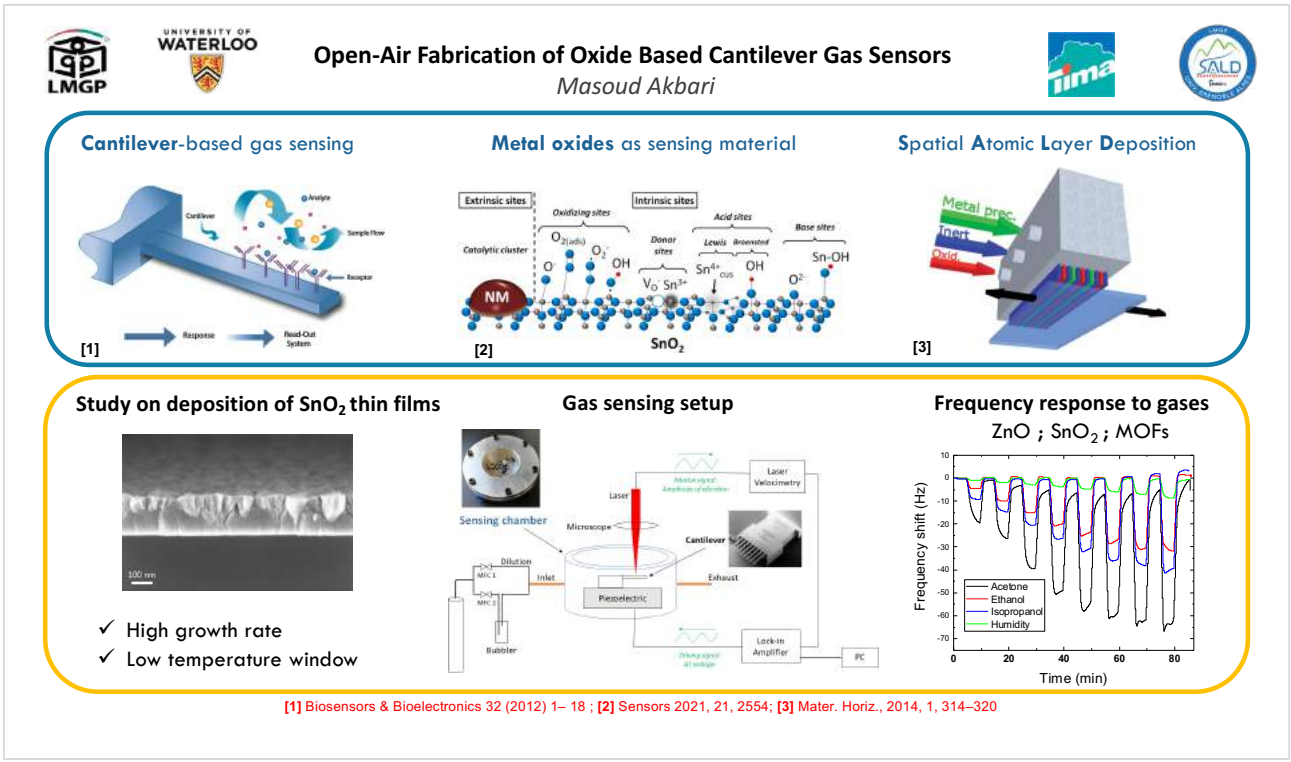
TIMA has organized the “PhD Day” on November 18th, 2021. Current PhD students of TIMA and RFIC-Lab (included in RMS team on Jan. 1st, 2022) have presented their work in one single slide and 180 seconds. Here are their slides and abstracts.

Abdelali AGOUZOUL – RMS team



This thesis aims at developing optimization methodologies for the use and storage of renewable energies to meet the energy needs of buildings, especially for air conditioning and heating. The modeling of the energy systems to be optimized will be carried out through classical identification techniques as well as automatic learning methods, followed by the development of optimal control laws. The proposed solutions will be synthesized on a hardware architecture in the form of an implementation on programmable circuits that will be tested on simulation and then on the real system.

Masoud AKBARI – CDSI team

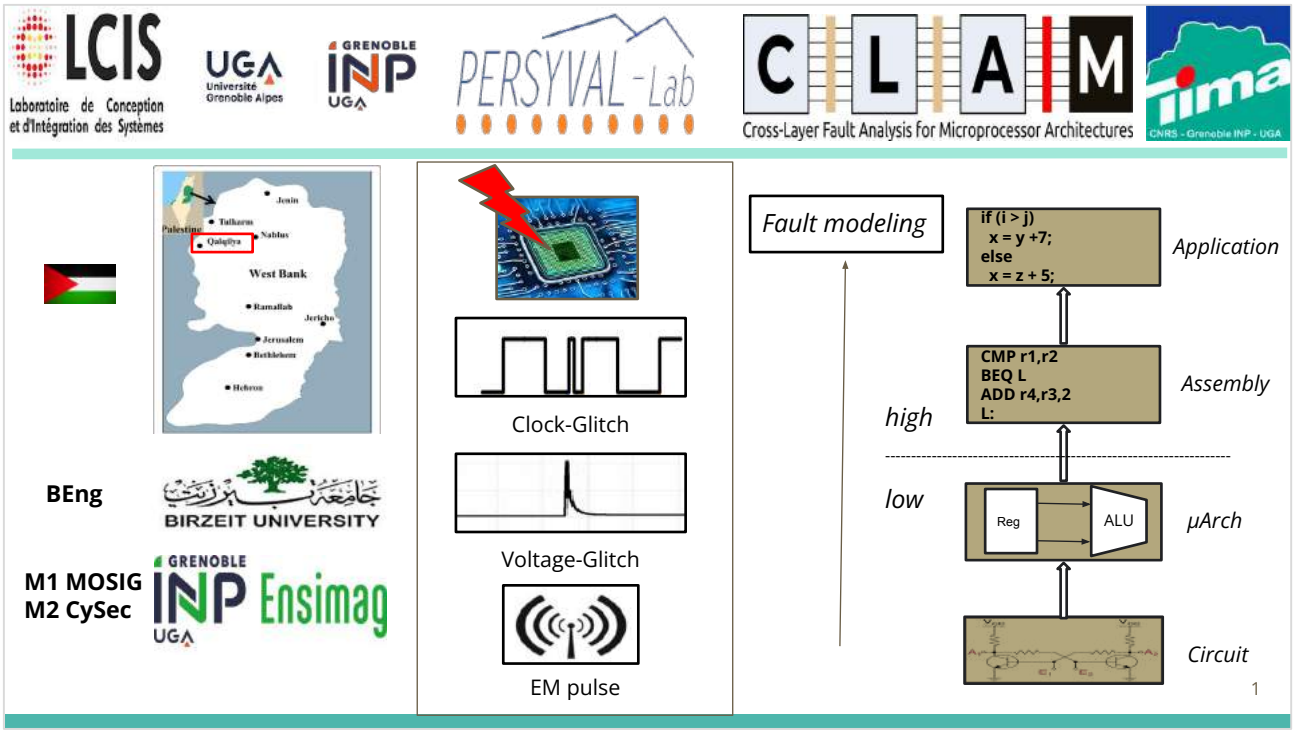


[1] Biosensors & Bioelectronics 32 (2012) 1– 18 ; [2] Sensors 2021, 21, 2554; [3] Mater. Horiz., 2014, 1, 314–320

Metal oxides are commonly used as sensing material for gas detection applications. The surface of the metal oxide is covered with oxygen ions (ion adsorbed) in presence of air, and these ions act as electron acceptors. Metal oxides have mostly been used in resistive or conductive gas sensors, where electronic events in the material generate a detection signal. However, they are also promising as sensing layer in gravimetric micro-electromechanical systems (MEMS). MEMS-based gravimetric sensors, such as cantilevers, are ultra-fast and highly sensitive and the sensing mechanism is related to mass change. Upon exposure of the metal oxide-coated sensor to a gas, the surface oxygen ions react with the gas molecules, which results in lowering or increasing the sensor mass. The sensing performance of the sensor is highly dependent on the chemical and structural properties of the sensing layer. Recently, Atmospheric-Pressure Spatial Atomic Layer Deposition (AP-SALD) has proven to be an excellent deposition technique that is capable of producing high quality metal oxide thin films with precision control, while being up to 2 orders of magnitude faster than conventional ALD, and working at atmospheric pressure.

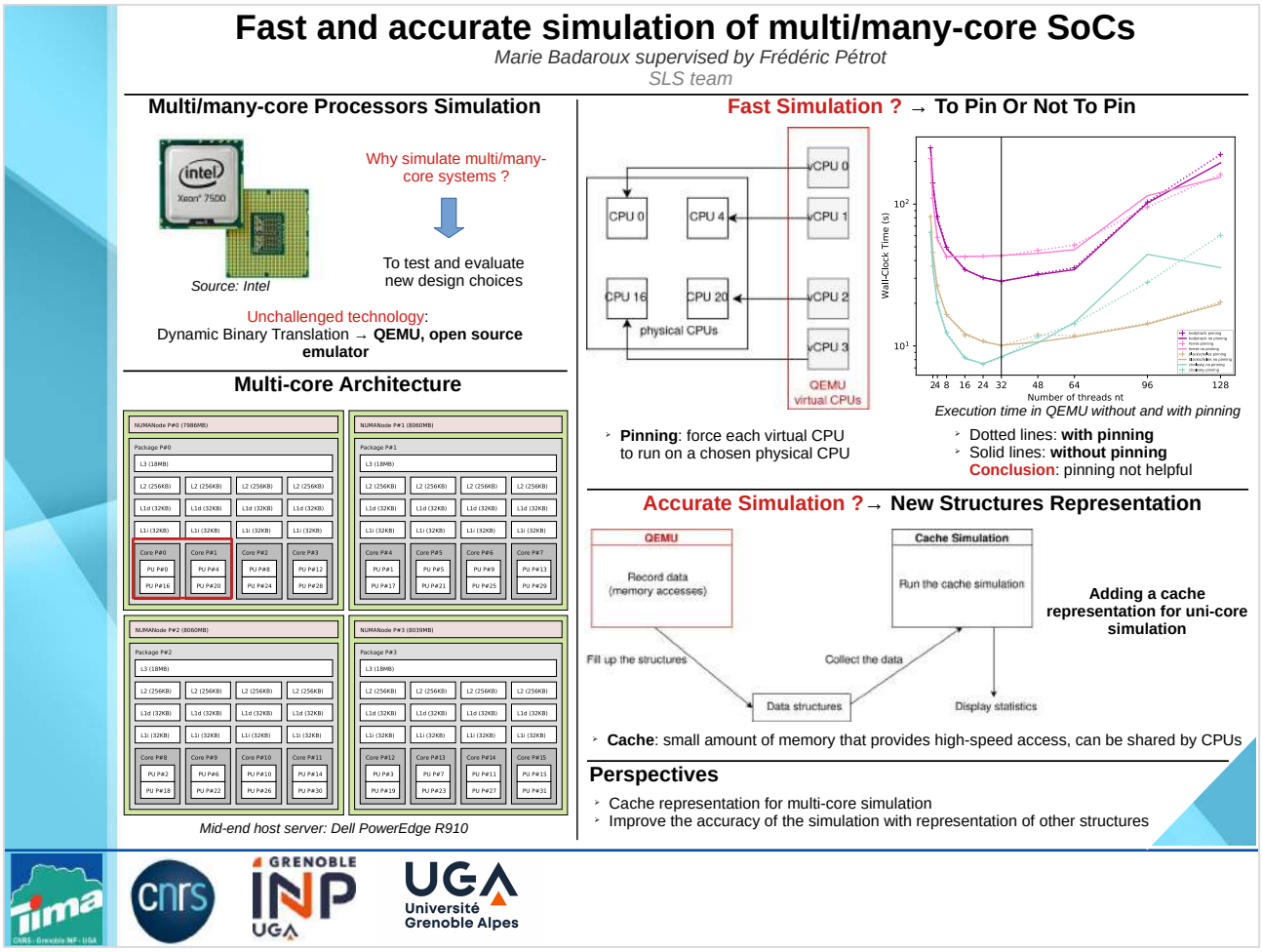
Recently, we developed ZnO-based transparent conductive films deposited with our home-made AP-SALD for resistive gas sensing. In this research, we employed AP-SALD for deposition of different metal oxides for gravimetric gas sensing. We present a complete study on deposition of tin oxide (SnO2), as a common sensing material, and structural, optical, chemical and electrical properties of the SnO2 thin films will be shown. Gas sensing properties of SnO2, ZnO, etc. deposited by AP-SALD will be investigated and discussed in detail. The gas sensors functionalized by metal oxides showed fast response and high sensitivity toward humidity, ethanol and acetone.

Ihab ALSHAER – AMfoRS team



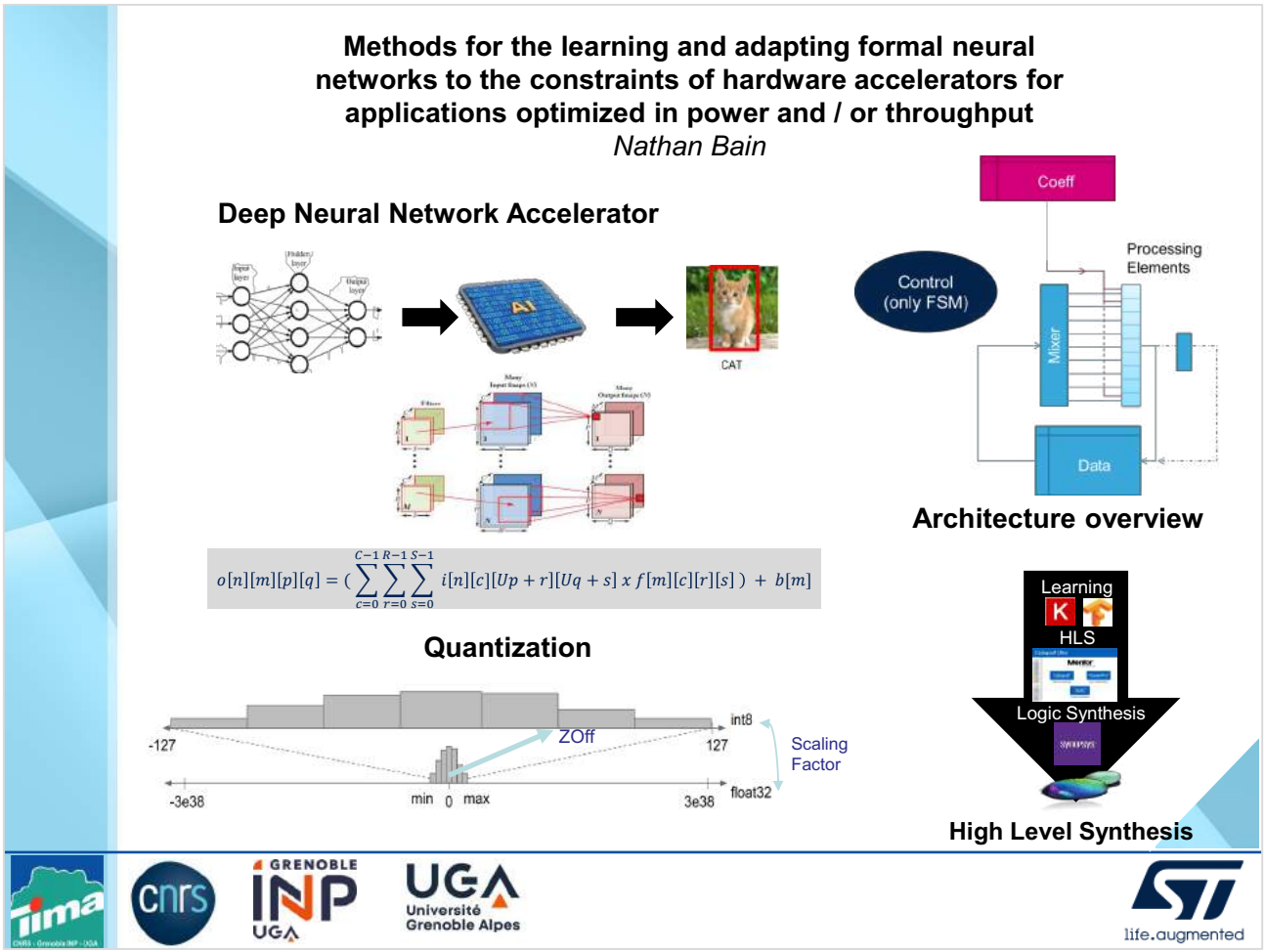
Securing components, such as microprocessors and microcontrollers, against fault attacks, requires a thorough understanding of faults: on the one hand, this means characterizing, studying, and analyzing the faults that could lead to exploitable code vulnerabilities. On the other hand, it also requires designing countermeasures at different levels, hardware, and software, with an acceptable cost. To build appropriate countermeasures, designers need realistic fault models that provide a proper characterization of the fault effects. However, with the increasing complexity of microprocessors, fault effect characterization based on a single level of analysis, such as assembly level or Register-Transfer level (RTL), is difficult and limits the understanding of the fault. As a consequence, the fault model development becomes a complex task: the models are a high-level approximation, sometimes unrealistic, and the development and evaluation of the countermeasures are not optimized. In this project, we propose a methodology to address the issues of faults effects characterization and bridge the gap between previous studies by providing a cross-layer analysis of code and microarchitectural vulnerabilities while performing fault injections at three distinct levels: physical, RTL, and software levels. We aim at providing a full picture of fault characterization at multiple description levels, by taking into consideration microarchitectural specifications. This will help in assessing the realism of already existing fault models, eliminate unrealistic models, and possibly propose new ones. Such methodology will also help in designing countermeasures at an appropriate cost. Regarding the main tasks that I have done in my first year, they were as the following: First of all, I focused on studying different types of ARM processors, in particular: Cortex-M processors. Then, reading articles and analyzing them critically besides performing some experiments to prove the need for our work.

Marie BADAROUX – SLS team



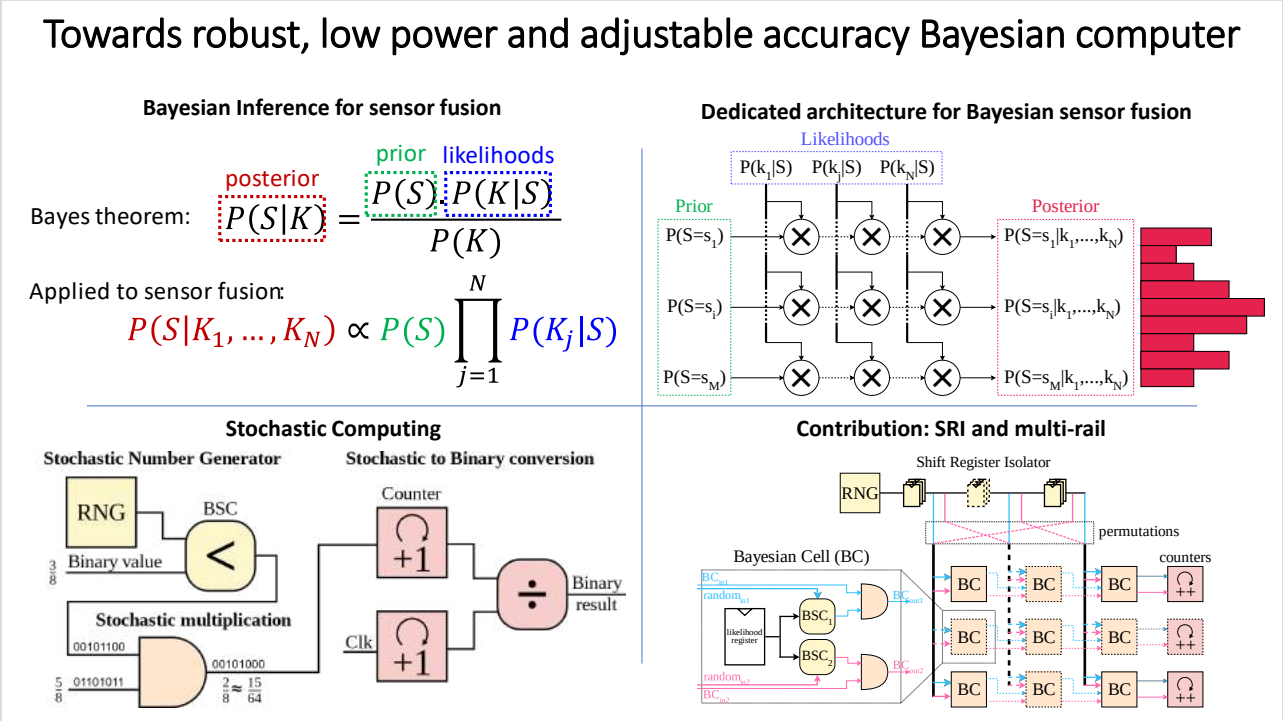
Due to the popularity of multi and many-core systems (1024 cores or more) over the last few years, simulation technologies are employed to test and evaluate new Instruction Set Architecture design choices. There exist lots of different types of simulators based on their levels of abstraction. The dynamic binary translation mechanism appears to be the solution for simulating full system level while remaining fast. Our desire to have a fast cross-simulation without representing all the hardware components in detail leads us to QEMU, a popular open-source translator using the dynamic binary translation mechanism. QEMU is the reference for cross-ISA emulation and has a very lively community around it. Fast and accurate simulation of multi/many-core architectures is an active topic and becomes more and more popular so the goal of this thesis is to investigate simulation strategies at system level for multi-core architectures so that it remains fast while increasing the accuracy of the simulation by adding new representations of structures (caches or TLB for example). Before increasing the accuracy of the simulation, my work for the first year of this thesis was to analyze the scalability of QEMU parallel implementation by adding the possibility to pin virtual CPUs (i.e. assign each virtual CPU to run on a chosen physical CPU of the host machine). QEMU provides support for lots of different architectures but we decided to focus on the RISC-V Instruction Set Architecture that is now mainly adopted by academical researchers and industrials. Surprisingly, forcing virtual CPUs to run on designated host cores does not improve the simulation performance in our case. To increase the accuracy of the simulation, we started to implement a cache model by capturing memory accesses in QEMU RISC-V. For the moment, we are able to run our cache simulator with QEMU uni-core with only one level of cache memory but we aim this year at adapting it to QEMU multi-core respecting memory coherence.

Nathan BAIN – SLS team



In our technological world, Artificial Intelligence (AI) is indivisible of the civilization and its importance become bigger and bigger with the passage of time. So, an hardware named Tensor Processing Unit (TPU) has been developed to make AI faster and reduce its power consumption. Here we will discuss about one part of AI, AI one the edge. It is concerning AI for embedded systems which have limited resources. In this context, ST opened a project about an innovative TPU architecture design. This architecture was intended for AI on the edge and was developed with High Level Synthesis (HLS) tool to make the reconfiguration of the TPU easier for future usage. The main target for this kind of IP is to minimize the area and the power consumption and keep a high throughput without changing the accuracy of the results. The detail of the architecture is confidential and cannot be explained here but I will attempt to bring out the main axes of the implementation. Concerning the power consumption, the memory is one of the most energy intensive so, in this concern, the reusing of data is maximized to reduce the number of memory access. A second important point is the way of parallelization of the Processing Elements (PEs) which can greatly reduce the latency of the TPU, depending on the choice and the neural network targeted. During the first year of my CIFRE thesis, my work consisted of the implementation of the TPU with the HLS tool. First, I had to understand how to use HLS and how Catapult (the synthesis tool) work to implement all the requirement of the IP and still minimizing the area. During the implementation I challenged the already thought architecture to improve it. I changed the scheduling of the data accumulation to reduce the loading of data. Then I compared different type of memory abstraction, some that were already existing and some that I realize myself, to choose the more efficient one. Now that the IP is almost finished, I will focus on the activation and the weights bit-width to reduce the TPU and the memory area without decreasing the accuracy of the results.

Jérémy BELOT – CDSI team



Depuis l'essor de l'internet des objets ou Internet of Things (IoT), des milliards d'appareils captent, collectent, traitent et distribuent des quantités de données de plus en plus importantes. Ainsi, il existe aujourd'hui une forte demande pour un matériel dédié capable d'analyser, à faible coût, de tels volumes de données, alors que les dispositifs sont de plus en plus contraints en énergie et que la puissance de calcul requise ne fait qu'augmenter.

Dans ce contexte, la fusion de capteur Bayésienne semble alors une piste particulièrement intéressante pour effectuer à faible coût et avec peu d'énergie des calculs à partir d'une information a priori et d'observations. Ces calculs réalisés au plus près du capteur permettent de limiter la quantité d'informations envoyées au cloud.

En réduisant les multiplications à une simple porte ET logique, l'arithmétique stochastique permet de réduire significativement la taille des opérateurs ainsi que leur consommation, en contrepartie d'une vitesse de calcul plus faible, ce qui la rend particulièrement adaptée aux calculs d'inférences Bayésiennes.

Les premiers résultats des projets BAMBI et MicroBayes dont cette thèse s'inscrit dans la continuité, montrent l'efficacité énergétique de cette approche stochastique lorsque la taille du problème à traiter est réduite et lorsque la précision requise est faible.

Ces résultats soulèvent néanmoins deux principaux goulots d'étranglement lorsque la taille du problème augmente : l'espace mémoire nécessaire pour le stockage des distributions de probabilité et le coût énergétique pour générer les nombres aléatoires.

Le but de cette thèse est de concevoir des architectures de machines bayésiennes efficaces dans les faibles et fortes précisions, et avec une faible consommation énergétique. Pour ce faire, il est nécessaire, d'une part, de contourner les limites définies précédemment en repensant les méthodes de stockage des distributions et de génération de nombres aléatoires nécessaires au calcul stochastique. Et d'autre part, d'exploiter les spécificités de ces calculateurs, en proposant des architectures moins gourmandes en énergie.

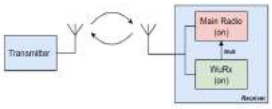
Imadeddine BENDJEDDOU – RFIC-Lab → RMS team

Wake-up Radio Receivers based on Spin-Torque Diodes and N-Path Passive Mixer-First

Imadeddine BENDJEDDOU, CFR CEA-Leti/RFIC-Lab/GIPSA-lab 10/2019 - 02/2023

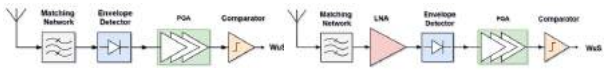
• WHY?

- Most of the **IoT devices** transmit and receive very small amounts of data, moreover **very rarely**
- To preserve battery life, **IoT device needs to wake-up** only when transmission is necessary
- A specific **ultra-low power consumption wake-up radio (WuRX)** interface has to be designed

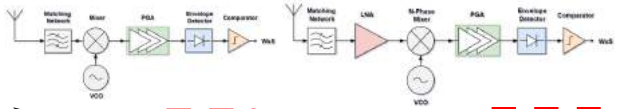


• HOW?

1. RF Envelope Detector
2. LNA + RF Envelope Detector



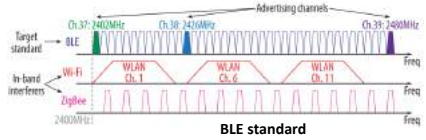
3. Mixer-First
4. LNA-First



Characteristics / Architecture	RF ED	RF ED + LNA	Mixer-First	LNA-First
Power consumption	nW	uW	uW	uW – mW
Sensitivity	-60 dBm ≤	-70 dBm ≤	-95 dBm ≤	-120 dBm ≤
Multiple standard	No	No	Yes	Yes
Selectivity	Low	Low	High	High
False Alarms	High	High	Low	Low

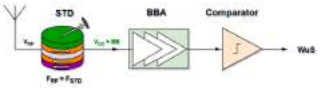
• WHAT?

Application

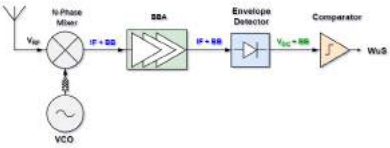


BLE standard

RF Envelope Detector architecture



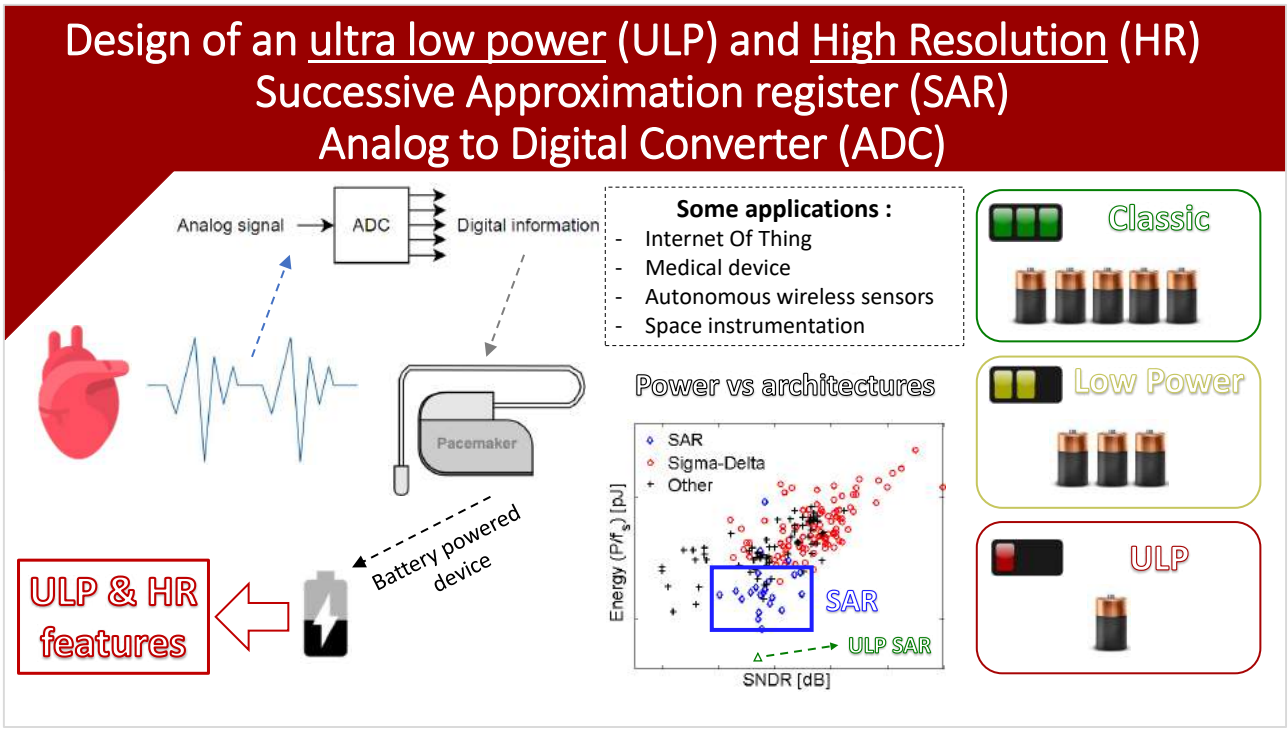
N-Path Mixer-First architecture



My research study focuses on an energy-efficient WuRx system based on spintronic devices. This work will allow acquiring the intellectual property on multi-band spintronic WuRx and better control of spintronic technology and related rectification properties to adapt them to the needs of wireless sensor networks. This is a multidisciplinary thesis that will rely on the expertise of a CEA laboratory (INAC / Spintec for the realization and characterization of spintronic devices) and two laboratories of the University Grenoble Alpes / Grenoble INP (the RFIC laboratory for the design of RF circuits and the GIPSA-lab for the development of new radiocommunication techniques). my work in 2020 focused on :

- The development of an electrical model of the nano-spintronic device.
- Electrical model of the device network
- Development of the radio communication technique and the wake-up protocol, modeling including the nanodevice model, prediction of the performances in different types of radio channels
- Choice of the receiver architecture
- Design of the circuit

William BONTEMS – RMS team



Following the Internet of Things expansion, the need of ultra-low power analog to digital converters (ADCs) is growing. Autonomous applications, such as medical devices, wireless sensors, and space instrumentations must deal with the power dissipation as a major issue. To achieve this goal, reducing the power consumption of the ADC stage is very challenging. Thanks to their simple structure and their capability to take full advantage of process scaling, successive approximation register (SAR) ADCs are suitable to fit this need.

However, to reach a high resolution in SAR ADCs, one must carefully consider the comparator design as a first step limitation. Then one may focus on some other limitations coming with the large capacitive DAC mismatches, the power-hungry reference voltages as well as charge injection issues.

This work consists first in designing a low power comparator respecting the speed and precision needs. It is then necessary to set up a calibration and Dynamic Element Matching (DEM) algorithm top compensate mismatch effect and improve the Integral Non-Linearity (INL). Finally, the reference voltage buffers must be studied to be robust while respecting a reasonable consumption budget.

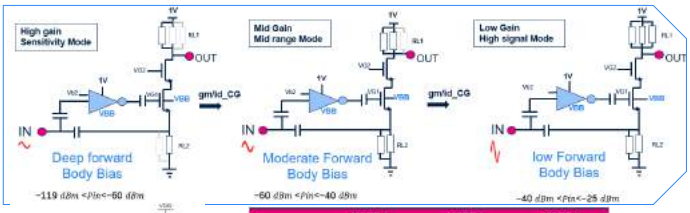
Mohamed Khalil BOUCHOUCHA – RFIC-Lab → RMS team

BOUCHOUCHA Mohamed Khalil, Cifre ST/RFIC Lab , 12/2020 –12/2023

Design Methodology based on the inversion coefficient for RF and mmW circuits optimization using 28 nm FDSOI Technology

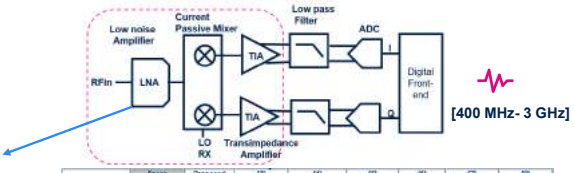
- **WHY?**
  - Expand IoT applications with sustainable power consumption
  - Demonstration through design of key RF building blocks
- **HOW?**

+ gm/ID efficiency factor and the inversion coefficient: main design variables
+ 28 nm FDSOI technology for power efficient design
+ Tunable design for large design space and more applications: study of LNA and RX chain



	MODE 1		MODE 2		MODE 3	
S21 (dB)	34	30.8	28.9	22	19.7	14.1
NF (dB)	1.47	2.1	3	7	5	8.5
IIP2 (dBm)	71.9	66.4	55.3	48.1	41.5	55.3
BW (GHz)	0.1-3		0.1 - 5.5		0.1 - 6.4	
Power (mW)	3	2.6	2.6	0.44	1.9	0.3

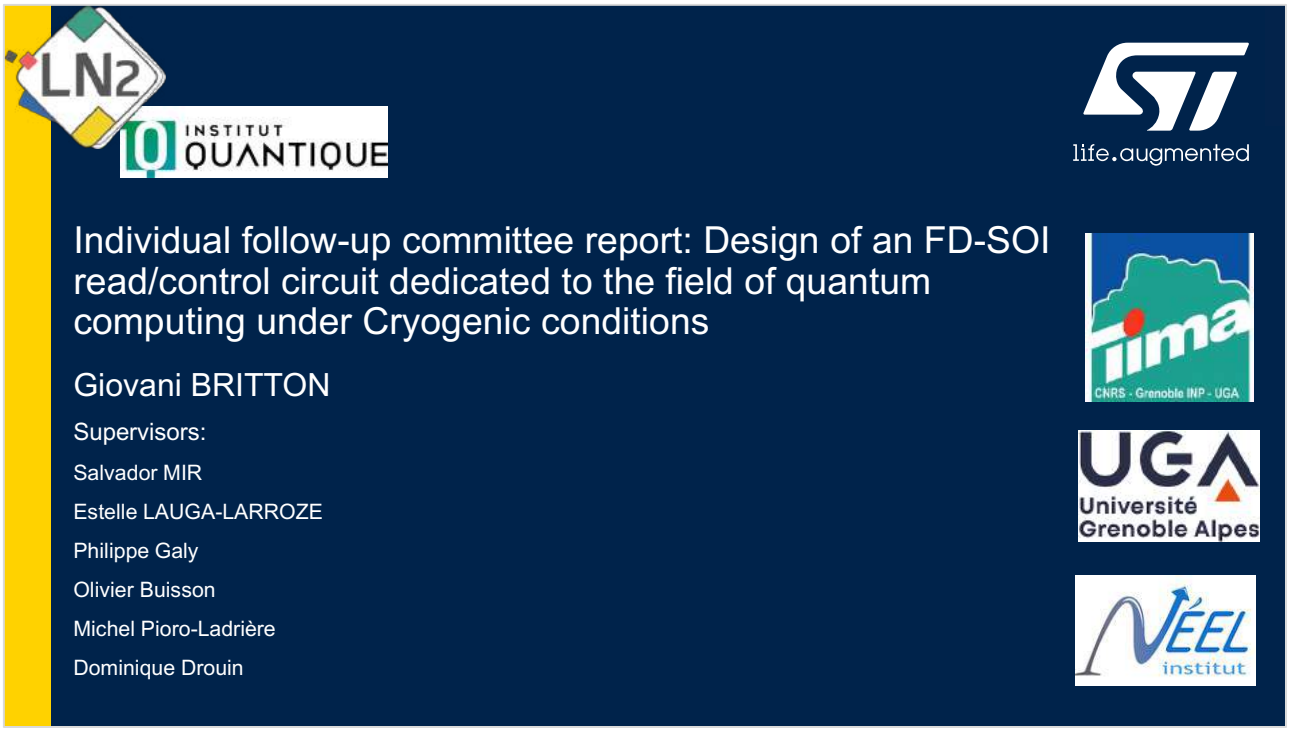
- **WHAT?** UWB Receiver Front-End chain for LTE-M IoT



	Specs	Proposed (Simulation)	[3]	[4]	[5]	[6]	[7]	[8]
Topology		Gm-boost CG	Inductive degeneration source	Complementary CS Inductive degeneration	Cascode CS with inductive degeneration	Capacitive cross coupled CG	RF-feedback complementary CS	Gm-boost CG
Technology(nm)	28 FDSOI	28 FDSOI	180	180	250	90	90	28 FDSOI
Operation frequency band (GHz)	0.4-1.2 1.35-3	0.1 - 3.4	0.7-1.7	0.75-1.1	1.2-1.35	0.1-1.77	0.1-2.3	0.1- 4.5
NF (dB)	1	1.5	0.3-0.6	1	0.8	1.8-2.3	1.7	3.6
Power (mW)	2	2.9	50	16.2	9	5.6	18	2
S21 (dB)	>20	33.6	17	12	20	23	21	22.9
IIP3 (dBm)	-10	-8		7.7	-11	-2.85	-1.5	-17.2
IIP2 (dBm)	35	>60						-
Inductor	0	0	5	3	3	0	0	0
Fully integrated	Y	Y	No		Y	Y	Y	Y

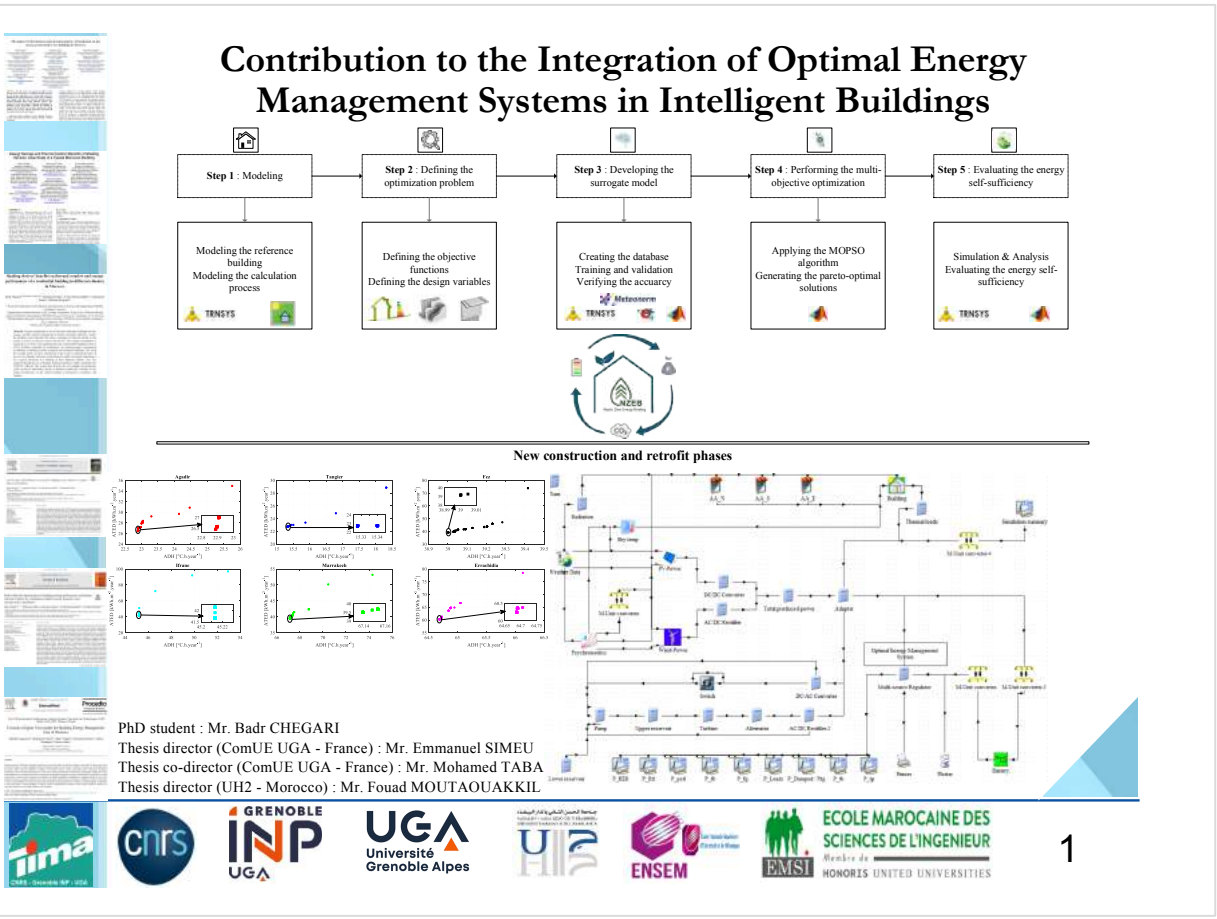
Facing tight commercial specifications, the design time and the performances of RF blocks can be optimized using advanced technology nodes such as the STMicroelectronics 28-nm fully depleted silicon on insulator (FD-SOI) as well as fast design methodologies. Through this work we highlight the efficiency of such methods since they are applied to complex architectures and different blocks and together with the additional tuning knob of the technology which is the body biasing, they allow to migrate continuously within a large design space to satisfy different sets of specifications and target multiple applications. This design strategy is applied on a RX chain targeting different standards composed of an ultra wideband LNTA, a passive mixer and a transimpedance amplifier TIA.

Giovani Crasby BRITTON OROZCO – RMS team



Le domaine du calcul quantique est un champ de recherche qui a suscité beaucoup d'intérêts et d'investissement ces dernières années. Le principal enjeu pour aboutir à l'intégration d'un ordinateur quantique est l'interconnexion de plusieurs Qubit. Néanmoins, le défi principal est lié à la liaison de plusieurs Qubit et ses répercussions sur le bruit. L'intégration de plusieurs étapes a pour conséquence l'apparition de bruit et d'interférences entre les composants. Sous les contraints et limitations actuelles, le but principal de la thèse est la conception d'une étape de lecture en technologie FD-SOI à temperatures cryogéniques. Le circuit à concevoir est un amplificateur de bas bruit (LNA), qui est fait dans le but de minimiser le bruit ajouté au système et d'amplifier la sortie vue depuis la sortie du Qubit. L'utilisation de la techno FD-SOI est liée au fait de ses performances à une temperature cryogénique est la facilité de régler la tension deVt avec l'aide du backbiasing.

Badr CHEGARI – RMS team

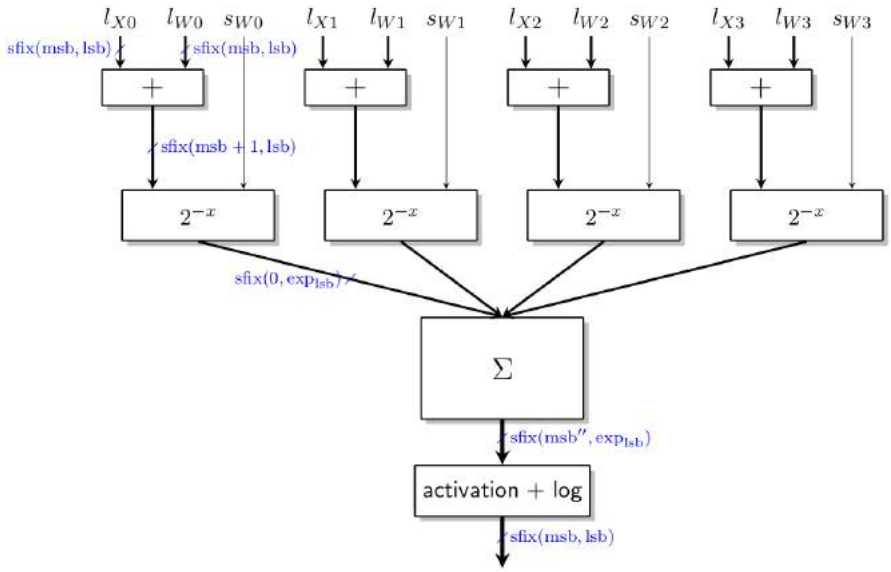


Today, the building sector is one of the largest energy consumers in the world. The transition from conventional buildings to nearly zero energy buildings is becoming one of the major contemporary challenges. The energy performance indicator of buildings is strongly considered by stakeholders. However, there are other indicators that constitute a key factor for sustainable development, namely those related to energy self-sufficiency and thermal comfort. The present thesis project aims to overcome this challenge, which still has shortcomings in the existing technical state of the art. It consists in developing a functional system, both in theory and in practice, which allows to optimize as much as possible the passive and active part of the building in order to achieve a better energy performance, a comfortable indoor environment and a suitable energy self-sufficiency. The work of this thesis project is divided into 3steps, firstly the development of an optimal energy management system for the passive part of the building. This step has already been developed by setting up a numerical platform in the TRNSYS environment associated with Matlab, in order to optimize the various thermo-physical parameters of the building envelope so as to minimize as much as possible the energy needs and the hours of thermal discomfort. This platform is based on the most recent techniques that have proven their performance and reliability in the state of the art. These techniques concern artificial intelligence, in particular artificial neural networks, and metaheuristic algorithms, in particular NSGA-II and PSO. Second, the development of an optimal energy management system for the active part of the building. This step has already been developed by setting up a numerical platform in the TRNSYS environment, which will optimize the energy flow between 3 energy resources including PV, wind and hydro with energy storage battery, with respect to the thermal loads of the building in order to achieve a complete energy self-sufficiency. Finally, the implementation of the two optimal energy management systems at the hardware level, notably in FPGA, in order to make the functionalities of the developed systems more realistic.

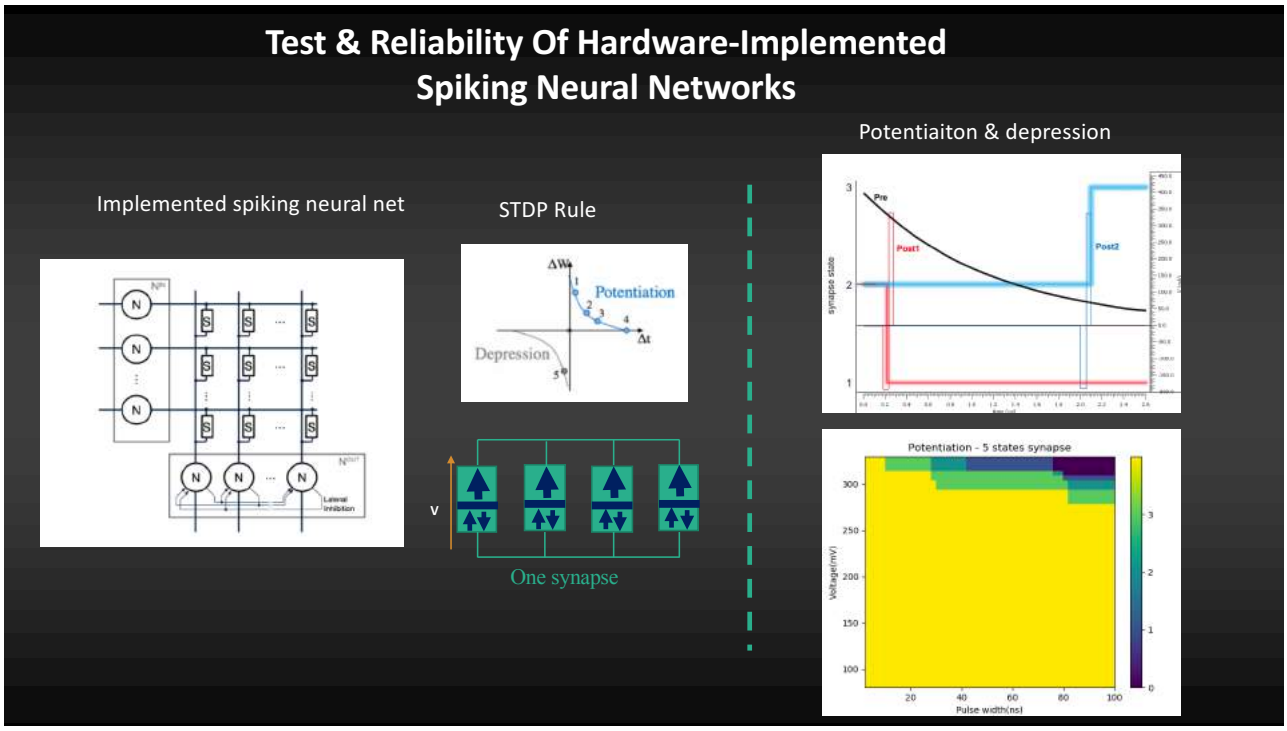
Learning in very low precision

- Embedded DNN
- Issues: memory bandwidth and number of PEs

$$f(Ws, Xs) = act\left(\sum_{i=0}^{n} W_i \times X_i\right)$$

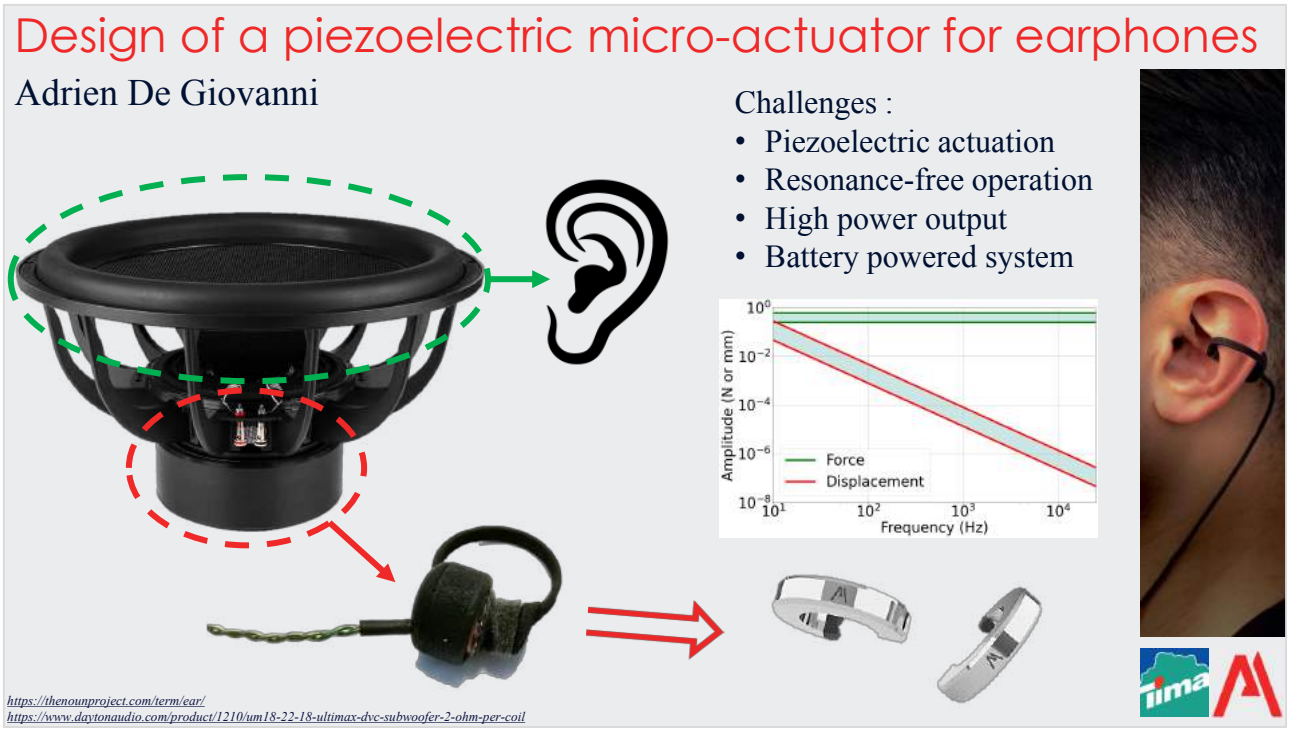


Salah DADDINOUNOU – AMfoRS team



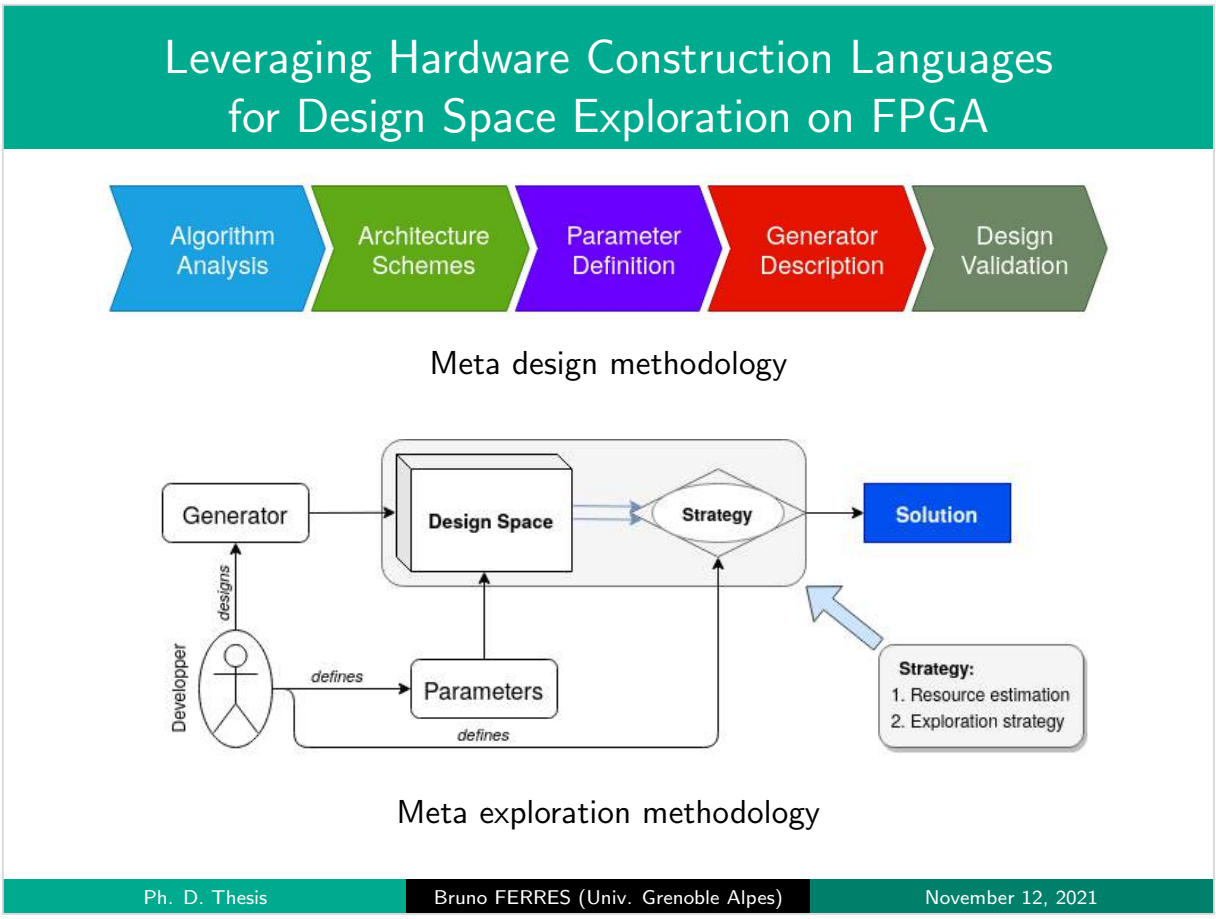
Spiking neural networks (SNN) is one type of artificial neural networks (ANN) in which the structure and the algorithm of learning and inference are inspired from their biological counterparts. Researchers in this topic aim to find the adapted hardware to implement this type of neural network to make it fast and energy-efficient, this is achieved by physically implementing the neurons and the synapses. The weights of the network are stored in physical synapses made of a device called a magnetic tunnel junction (MTJ). Communication between neurons is based on spikes, the timing of neurons' spikes is very crucial for training where the weights of synapses linking the neurons are tuned following a learning rule called spike timing dependent plasticity. The synapse tuning takes its benefit from the intrinsic stochasticity of MTJs when put in a compound to form a single synapse. The goal of my thesis is first to demonstrate by simulation a functional model of a small network. secondly, to understand the effect of stochasticity and study the reliability of SNNs by considering their variability due to the tiny imperfections during fabrication process. third, investigate the robustness of SNNs against environmental conditions, this complete study will culminate in a test protocol.

Adrien DE GIOVANNI – CDSI team



This PhD supported by the AnRT through the CIFRE structure is a collaboration between TIMA laboratory and ActivMotion. XtraSound are extra-auricular earphones unlocking a new enhanced hearing experience offering clear benefits over existing mobile audio and communication solutions. It is a hands-free, discreet solution that aims to be forgotten by its user. Without altering the perception of the surrounding sounds, the desired audio content can be superimposed to it. These earphones work the same way a loudspeaker works. There are two parts, the suspended diaphragm and the electrodynamic motor. The users ear play the role of the suspended diaphragm and the XtraSound earphones are the electrodynamic motors. They make the ear vibrate which will emit sound in the air but also propagate mechanical waves through the cartilaginous structure of the ear to the cochlea.The next level is to reduce the size of this actuator and to integrate the actuation part in the structure of the earphone. Using piezoelectric materials, thin layers can be deposited on it to make it vibrate. More then just opening new opportunities in regards of design, we are also looking foward to get a better yield.In these first 10 months of the PhD, I was able to analyze the electrodynamic earphones toevaluate their performance and set the specification to meet with the newer version. Then, after learning how piezoelectric materials work, I compared different amplifiers to choose the power source the new earphones will have to use. With all the developpement context set up, I could take a first simple piezoelectric actuator and evaluate its performance using a bench setup I putin place. This helped me see how far we are from the specifications established before and to learn how to caracterize an actuator by looking at the correct measurements. Finally, to get into the core part of the project, I learned how to use Ansys to be able to simulate new designs and test them with finite elements to predict their performance. This saves up a lot of time and effort and should get us closer to the wanted result quicker.

Bruno FERRES – SLS team



In a world where required computational capacities grow exponentially, FPGA based hardware accelerators are imposing themselves as energy efficient alternatives to general purpose CPU.

However, while software development methodologies can rely from new paradigms and techniques to improve productivity, designing a digital circuit remains a daunting task here both expertise and time are primordial.

In order to increase hardware developers productivity, we explore the possibility of using a novel design paradigm called Hardware Construction Languages, which enables building parameterized design generators — increasing both code reusability and parametrization — and exploiting high level features such as object-oriented or functional programming.

The first contribution of this project aims at easing accelerator comparison by exposing different estimation metrics and methodologies, in order to provide designers and tools with interesting feedbacks.

We then consider leveraging this new paradigm to generate and compare accelerators — introducing two complementary methodologies: meta design and meta exploration.

Meta design is based on prior analysis of a given algorithm to provide a parameterized design generator, where every generated design belongs to a design space to be explored.

Meta exploration is then used to leverage user expertise on both application domain and target board for efficient exploration of so defined design space.

We choose Chisel as an HCL candidate, and introduce QECE — Quick Exploration using Chisel Estimators — as a demonstrator for both contributions — as Chisel is built on top of Scala, we hence bring high level features from software development to the hardware world.

We finally leverage the introduced methodologies by developing various representative FPGA applicative kernels, and expose various scenarii of estimation and exploration.

Tiziano FIORUCCI – AMfoRS team

The use of deep sub-micron technologies (65 nm, 45nm, and 32nm) has led to an increased sensitivity to errors caused by ionizing particles (heavy ions, protons, neutrons, ? particles). The main effect on such systems is the temporary, non-destructive, flipping of a memory element (latch, flip-flop, memory bit), which may alter the normal system behavior. This can later evolve to several outcomes, from fault masking (silent fault) to a complete system crash (critical fault).

The strong integration capabilities offered by these technologies allows implementing complete systems on a single chip (Systems on a Chip, SoC), embedding processor(s), memories, and peripherals in the same package. The use of SoCs in automotive systems for autonomous cars driving makes necessary to develop and adapt flows and certification procedures to comply with the ISO26262 standard, which is related to functional safety of road vehicles.

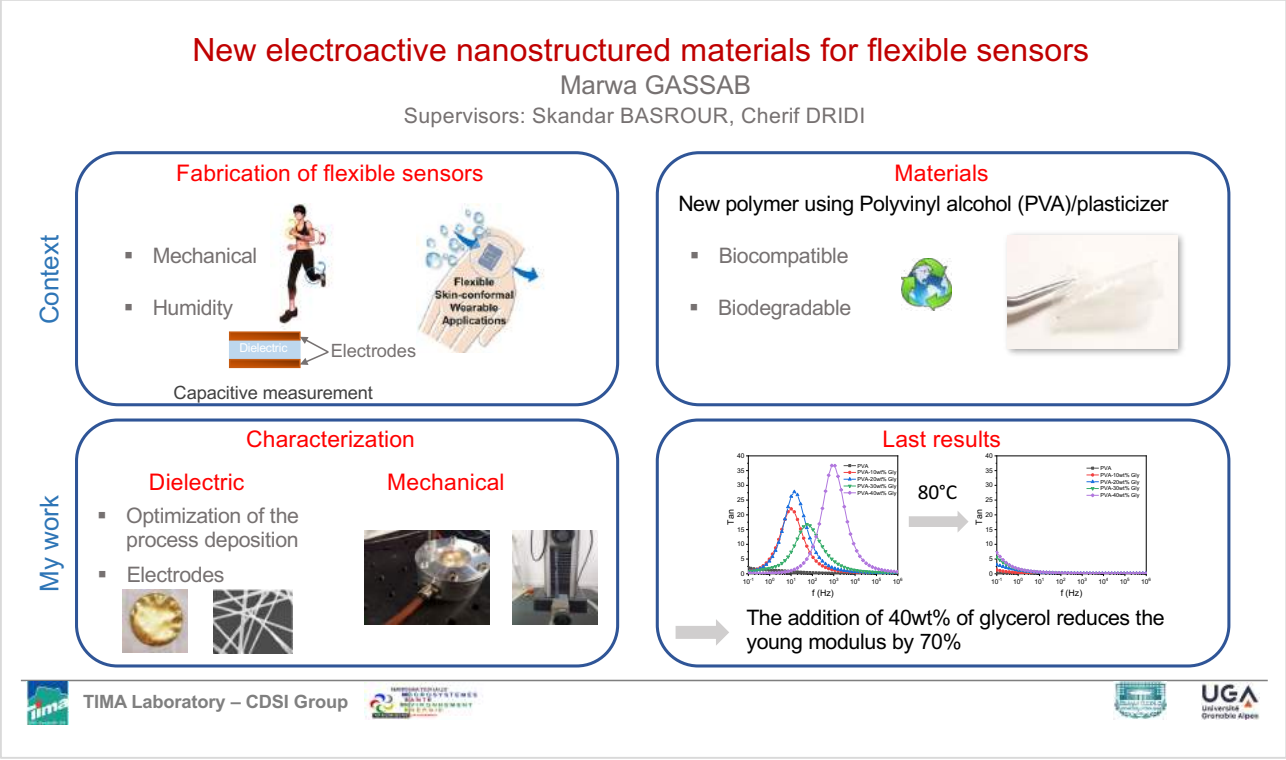
This norm makes mandatory to study and classify the failure modes according to well-defined but generic criteria, which need to be tailored to the specific context of SoCs.

This thesis aims at defining a specific flow and methodology for ISO26262 certification, based on fault injections. The methodology will be in particular based on the extraction of several reliability metrics required in the context of a digital automotive SoC system.

The analysis of the fault outcome at system level will require crossing the fault abstraction levels from combinatorial logic to system level and to the software application. This step is still heavily user guided and requires an expert.

The complexity of the task depends on the fact that the metrics and flows for failure mode identification and analysis of fault outcomes, mandated by the ISO26262 norm, are abstract and hard to map to complex systems, where the propagation of a fault may be difficult to trace. The goal is to develop the techniques allowing to automatically extract the information needed for the certification process, and instantiate the identification/verification flows required by the standard.

Marwa GASSAB – CDSI team



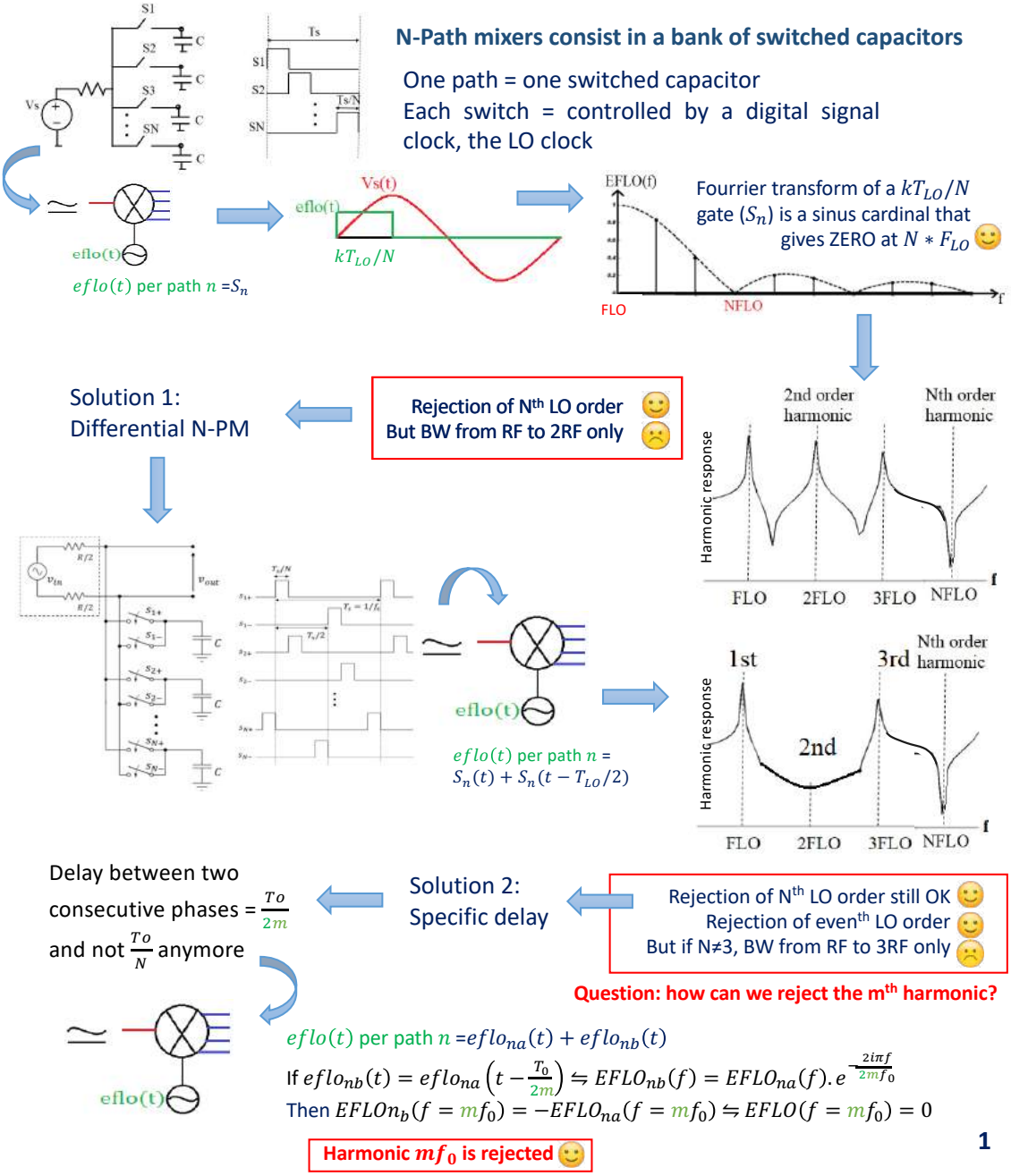
This PhD thesis is supported by the Region Auvergne-Rhône-Alpes as a part of the GRESAM project in collaboration between NANOMISENE Lab in Sousse and TIMA CDSI in Grenoble. Over the previous few years, lot of interest has been devoted towards developing stretchable, soft and harmless sensors for different applications such as wearable sensors, electronic skin, and healthcare devices. Biocompatible and biodegradable polymers are a classification of biomaterials that have received a considerable attention for these sorts of applications. Among these materials, polyvinyl alcohol (PVA) showing versatile advantages like non-toxicity, environmental friendliness, low electrical conductivity and interesting mechanical and dielectric properties. All these characteristics lead this polymer to be easily integrated into different flexible devices. The choice of the electrodes type is also important in this kind of application. Flexible and stretchable electrodes are essential components in flexible devices, which possess durability against repeated mechanical deformations. The aim of this year of my thesis is to modulate the dielectric properties of PVA with the addition of adjuvants and using different electrode materials and structures in order to change the typical and non-flexible electrodes as gold and silver with the use of stretchable Silver nanowire (AgNW)electrodes. The first part of the work was to investigate the impact of the addition of glycerol as a plasticizer agent on the dielectric properties of PVA polymer using classic type of electrodes. The second part was to study the dielectric properties of the different PVA/glycerol films using AgNW as a new candidate for MIM structure. AgNW networks constitute one of the most promising alternatives for classical and non-flexible electrodes. They possess high conductivity, transparency and flexibility and can provide an enhanced dielectric response in comparison to traditional Au or Ag thin film electrodes made by evaporation or sputtering techniques. The third part was to the study the effect of glycerol in the mechanical properties of PVA using two techniques of measurements: Tensile test and Bulge test as a homemade setup. This year of study allowed as choosing the type of electrodes and the concentration of glycerol to host afterward electroactive molecules for the aim of constructing flexible mechanical sensors.

Sana IBRAHIM – RFIC-Lab → RMS team

Sana Ibrahim, phD student 2nd year

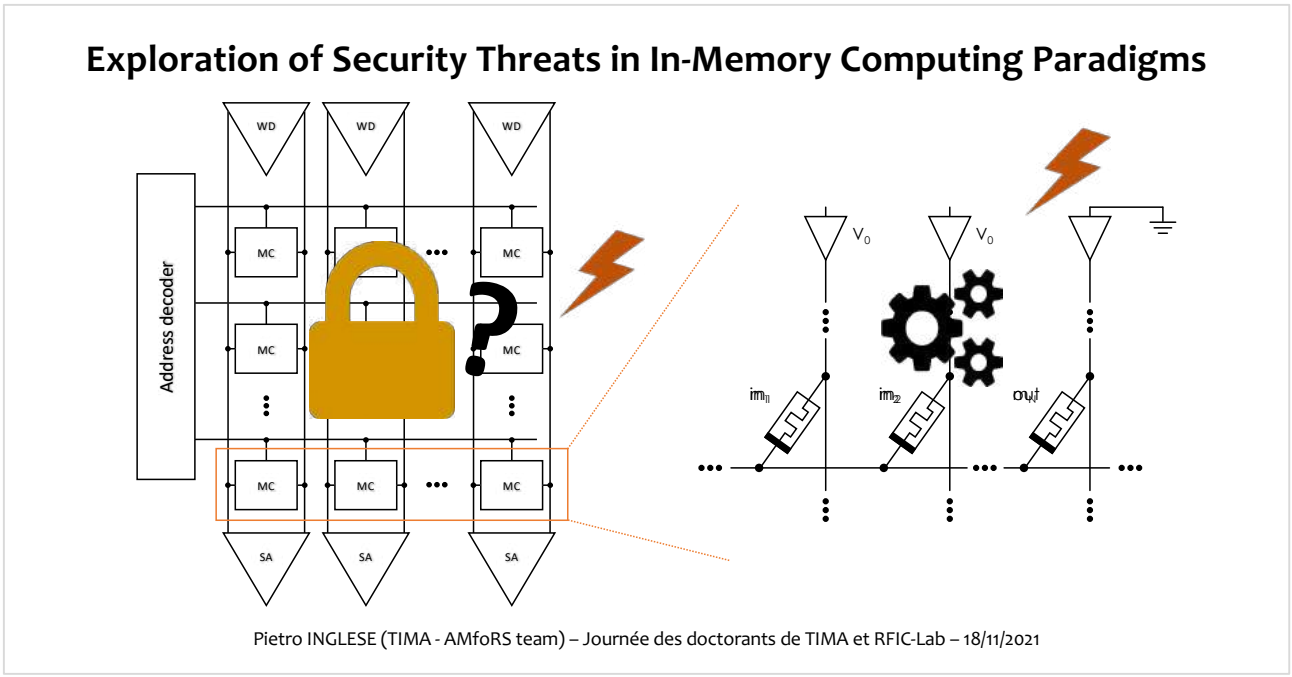
Thesis director/ co-director: Florence Podevin/ Laurent Fesquet

Subject: Clock Generation and Harmonic Rejection N-path Mixers for Low Power Receivers



Following the advance in mobile communications and wireless applications and due to the increasing number of connected devices, more and more frequencies are allocated in the RF spectrum so there is a need for a multi-standard receiver. Accordingly, harmonic rejection N-path mixer based architecture is a good candidate to manage a wideband of frequencies using a single receiver, which requires wideband LNA and wideband VCO (typically based on tunable ring oscillators). This doctoral work allows exploring innovative architectures for N-path mixers that reduces power consumption, complexity and time constraints on the clock generators and capable of resisting the mismatches, including well balanced clock phases to control the mixer. As we are seeking for low power systems, FD-SOI 28nm technology is used for implementing our design.

Pietro INGLESE – AMfoRS team



Security is critical today for information and communication technologies. It is the basis for obtaining confidentiality, authentication, and integrity of data. Improving the attack resilience of secure devices is a major challenge today due, in part, to the accelerated race among the developers and the attackers, and also to the heterogeneity of new systems and their ever-increasing numbers. The vulnerabilities of electronic devices that implement cryptography functions have been well studied in the last decade for von Neumann computing architectures, designed with CMOS technology. However, there is little evidence that these studies hold true for novel computing paradigms with new technologies.

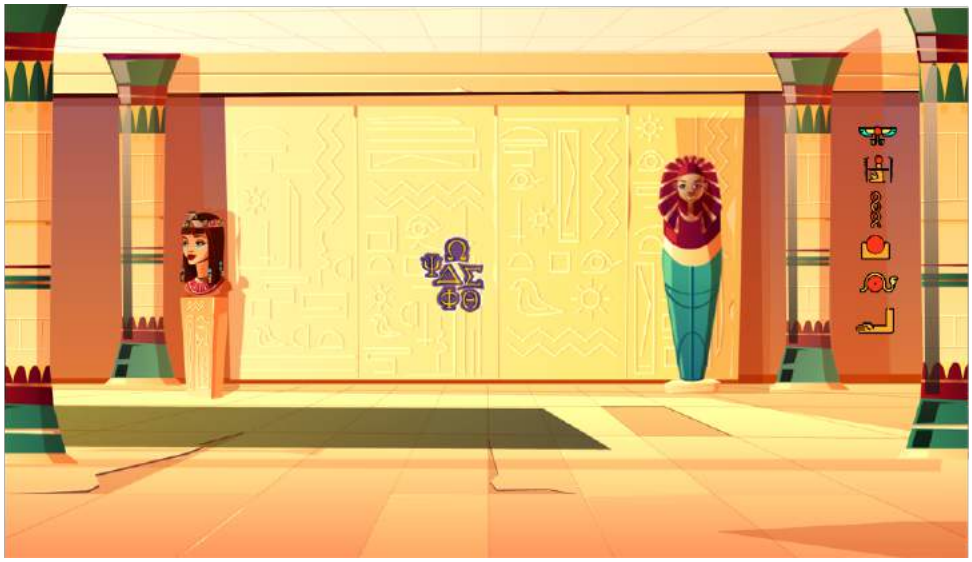
In-memory computing paradigm is an emerging concept based on the tight integration of traditionally separated memory elements and combinational circuitry. It allows the minimization of the time and the energy needed to move data across the processor. The most promising solutions for in-memory computing architectures are based on the use of emerging technologies (Spin Transfer Torque Magnetic RAM and Redox RAM) that are able to act as both storage and information processing unit. Despite the promising nature of the in-memory computing-based architectures many issues related to the devices themselves and to their double usage (storage and computing unit) still need to be solved. In particular, a correct evaluation of security threats targeting systems based on in-memory computing is still missing.

The objectives of the thesis are to compare the in-memory mapping techniques and to establish a taxonomy of the attacks. In fact, several methods exist in literature allowing mapping of any logic function on in-memory computing structures. Our objective is to map a crypto-processor algorithm in the corresponding in-memory architecture by using different mapping approaches, thus obtaining several in-memory crypto-processor versions with different characteristics. With the identification and classification of possible attacks that can lead to exploitable errors or leak of information in an in-memory crypto-processor architecture we will establish a taxonomy of the attacks, and we will compare the resilience of the studied circuits to these attacks.

Amine JAAMOUN - AMfoRS team

The objective of this thesis is to develop new ways of securing a memory hierarchy. A first primary focus of work will be to understand all current attacks on the memory hierarchy and possibly identify potential new vulnerabilities. This analysis will then make it possible to derive a set of quantitative criteria for the security of the hierarchy. We will, therefore, have the appropriate tools to compare the architecture proposed to secure the memory hierarchy in the state-of-the-art and identify their limits. From this, we can build countermeasures that are thought out globally and that target the entire memory hierarchy. Finally, the innovations proposed in this thesis are intended to be integrated into the secure RISC-V processor developed in the Nanoelect Nanotrust IRT project.

Diana KALEL – CDSI team



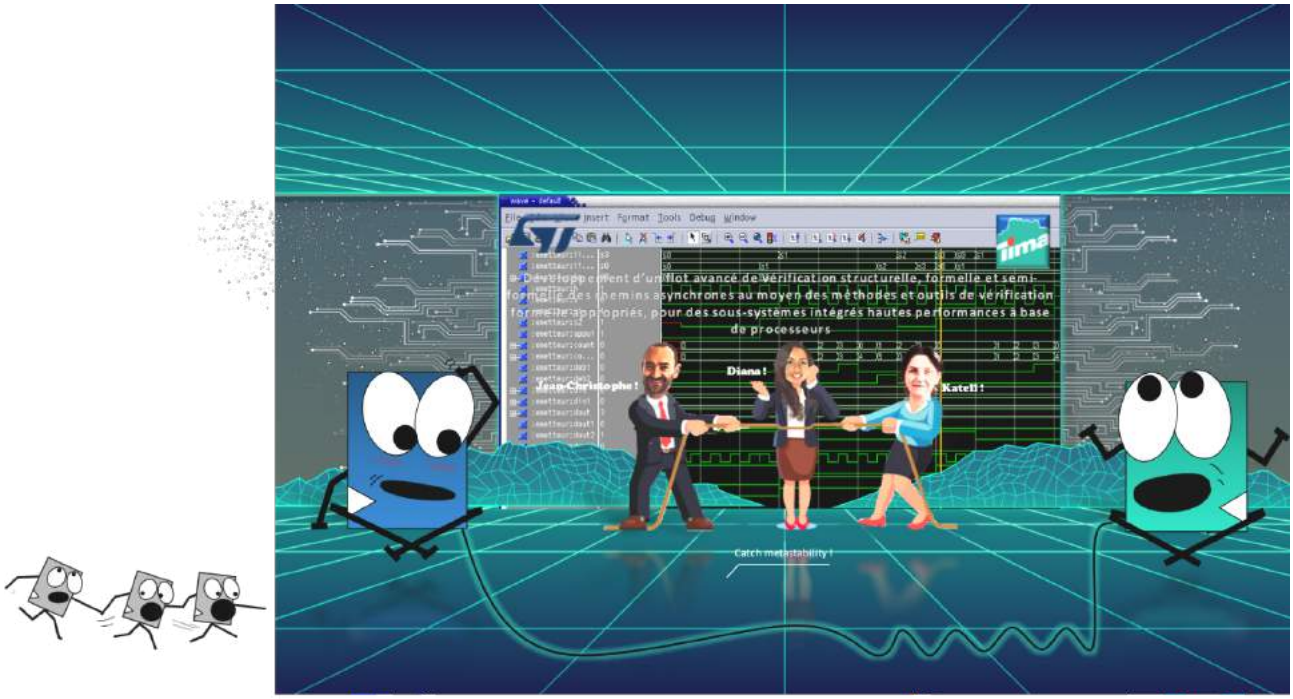
Il y a quelques milliers d'années, les anciens égyptiens utilisaient des symboles mystérieux pour écrire leur langue. Horizontalement ou verticalement, ces symboles pouvaient exprimer des noms, des mots, des phrases et même toute l'histoire de l'ancienne Egypte. Cette histoire qui est restée un grand mystère jusqu'aux années 1800…

Quand le Grenoblois Jean Francois Champollion a pu cracker le code à travers la pierre Rosette où un même texte a été écrit en hiéroglyphes, en démotique et en grec.

Et puisque Champollion connaissait très bien la langue grecque, et à travers la comparaison des noms propres qui existaient dans le texte entre la version grecque et la version hiéroglyphe. Et finalement pour la première fois, on a pu comprendre et "écouter" les symboles des hiéroglyphes.

La langue grecque ici a joué pour lui le rôle d'un ‘'translateur" ou un médiateur.

Entre les hyéroglyphes et toutes les langues parlées aujourd'hui, de même dans l'électronique.



Sur un chip, afin d'optimiser la consommation d'énergie, il est parfois nécéssaire de clocker les différents bloc avec différents domaines d'horloge. Ces domaines d'horloges communiquent entre eux comme s'ils parlaient des langages différents, ce qui peut causer de petites misunderstandings qu'on appelle "la métastabilité". Ce qui veut dire que la data arrive au niveau de la destination avec une certaine incertitude sur sa valeur.

Une métastabilité peut être aussi produite à cause de la communication entre différents domaines de reset.

Il faut donc toujours s'assurer de la présence d'un "translateur" ou "médiateur" entre ces différents domaines pour garantir une transmission safe de data et d'éviter tout genre de misunderstanding ou de métastabilité.

Mon travail de thèse consiste de s'assurer de la présence et de la fonctionnalité de ces structures translateurs.

Je m'appuie bien sûr sur le travail qu'ont effectué Mejid et Guillaume, qui consistait à :

- extraire les propriétés sur la base des structures détectées durant la vérification structurelle,
- déterminer un cône d'influence suffisant pour cette propriété
- vérifier avec une approche formelle. Mais durant cette thèse, on va se focaliser plus sur le semi formel.
- extraire les propriétés et de les lancer dans un environnement de simulation … ce qui peut être moins précis que le formel mais beaucoup plus rapide.

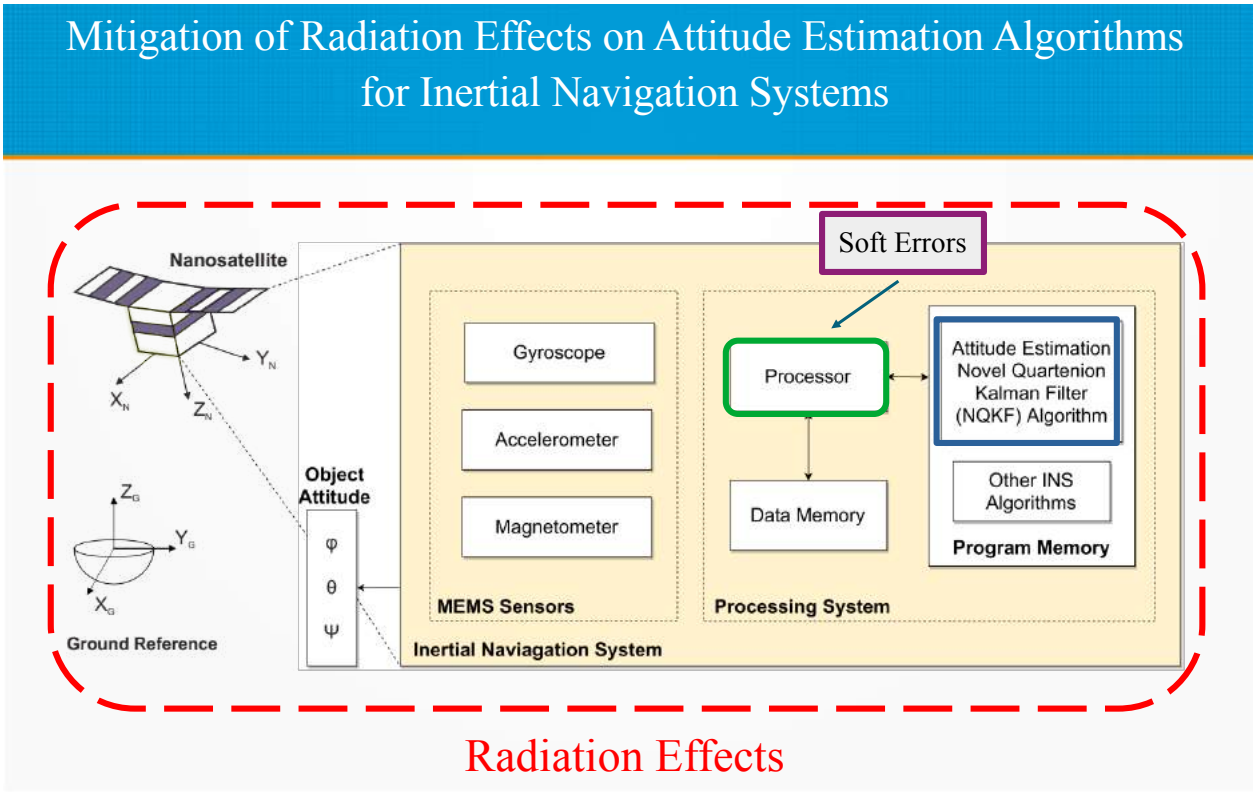
Donc si on parle précision vs temps, le semi-formel est plus favorable.

Je m'appelle Diana, je suis égyptienne et je fais ma thèse à Grenoble, ville de Champollion et de l'électronique. C'est une thèse CIFRE avec deux encadrants :

- Jean-Christophe Brignone, senior engineer chez STMicroelectronics
- Katell Morin-Allory, maître de conférence et ma directrice de thèse du Labo TIMA

Le but est de développer un flot de vérification structurelle et fonctionnelle - formel et semi-formel – des chemins asynchrones pour des sous-systèmes intégrés hautes-performances à base de processeurs.

Tarso KRAEMER SARZI SARTORI - AMfoRS team

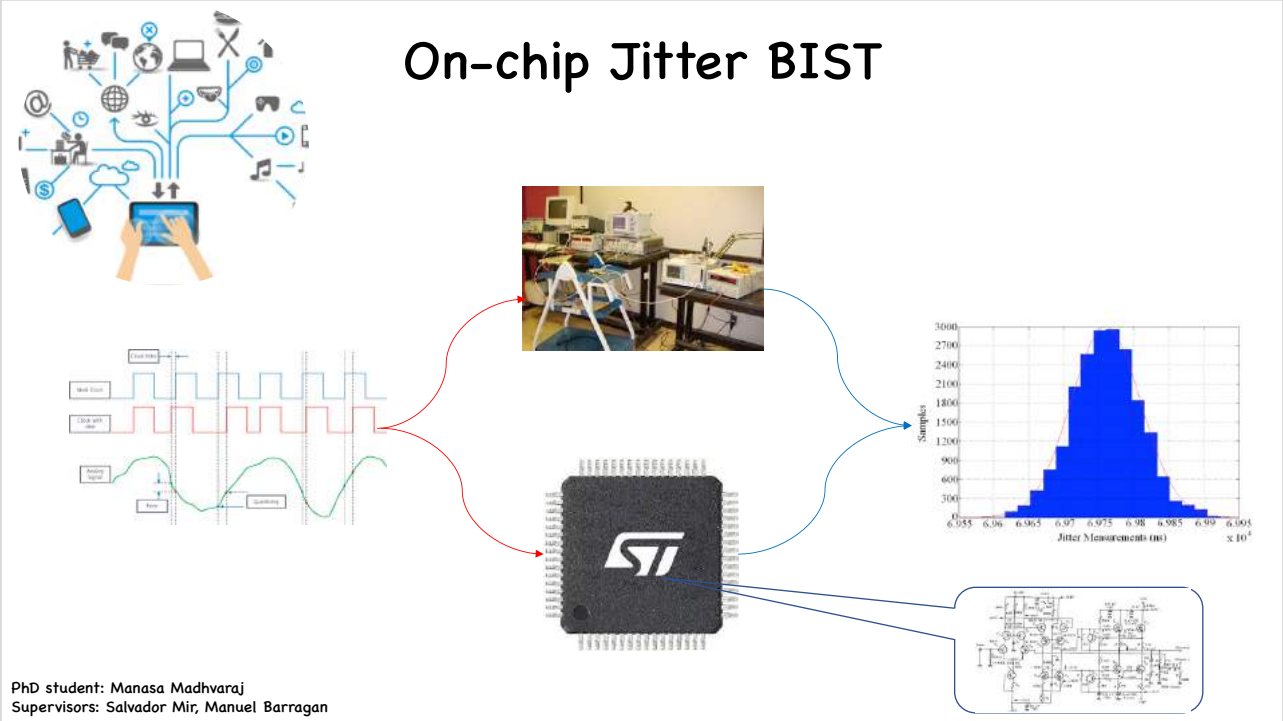


Modern inertial navigation systems (INS) based on microelectro-mechanical systems (MEMS) have been progressively integrated into unmanned vehicles and satellites for essentially determining and controlling their attitude (spatial orientation). MEMS-based INS has become thus more and more popular with low-cost drones and nanosatellites. INS components are liable to radiation effects in space environments, aviation altitudes, and also at ground levels. In addition to radiation-induced destructive effects, MEMS sensors are sensitive to accumulative radiation doses that provoke permanent effects on their physical structures, whereas other INS components can also be upset by radiation particles that create transient faults able to invert memory bit contents of their circuits (soft errors).

Attitude Estimation (AE) algorithms are responsible for estimating the objects' orientation taking into account measurements provided by the sensors and defined reference observations, moreover AE algorithms also ensure the filtering of noisy measurements. Gyroscopes suffer indeed from drift errors as well as accelerometers that can accumulate and interfere in AE algorithms. In addition to the inherent measurement errors, INS components also have to deal with radiation effects that can lead their embedded algorithms to failing in properly estimating the object attitude, and thus in controlling safety-critical functions of INS applications such as autonomous drones, nanosatellites, and self-driving cars.

This doctoral thesis project aims to investigate space-to-ground radiation effects that can upset attitude estimation algorithms of inertial navigation systems for safety-critical applications, devising new software-level solutions for mitigation of radiation-induced errors and related failures.

Manasa MADHVARAJ – RMS team

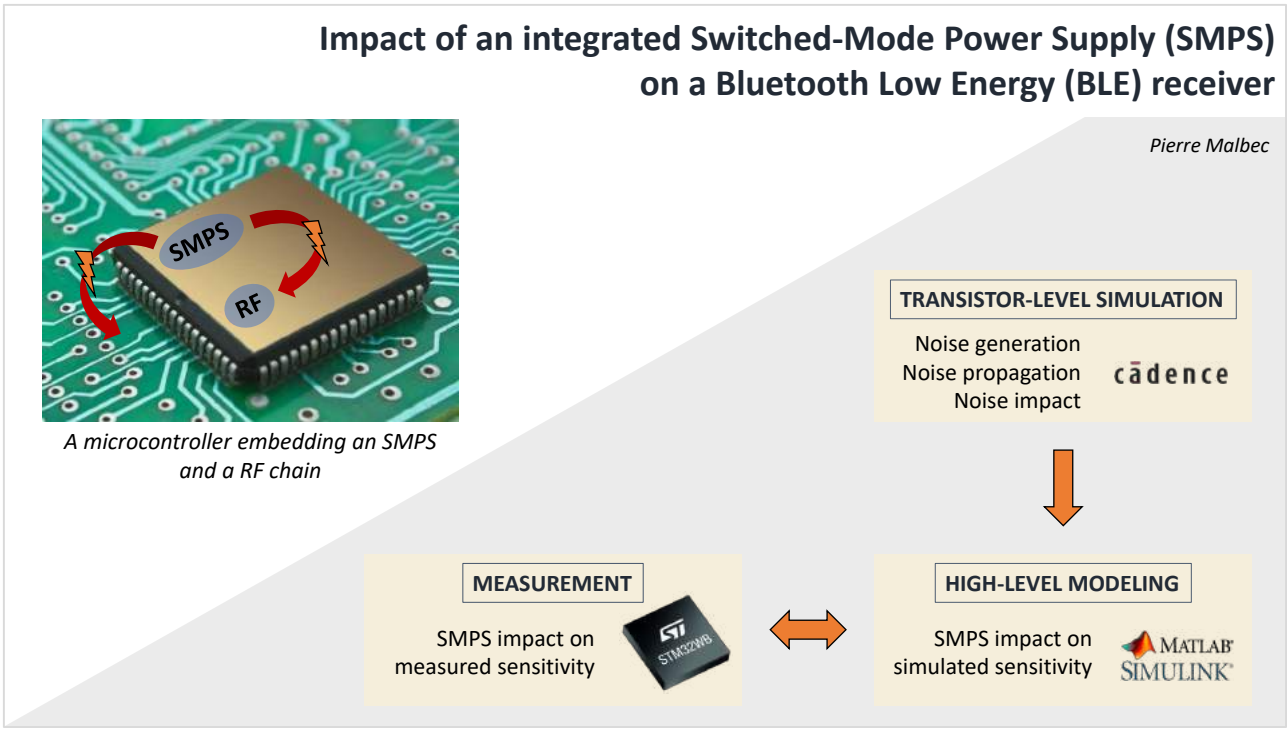


In the current day and age, testability of integrated circuits have become more important, especially in analysis and characterization of performance of high speed mixed signal circuitry. An important parameter that defines the performance of high speed circuits is clock jitter. Clock jitter is the irregularities in the periodic occurrence of a desired clock edge. Towards this direction, my research work involves the development of an on-chip jitter BIST for clocks in the Giga Hertz range, with a sub-picosecond resolution. In the framework of the Nano 2022 program, this research is being carried out in collaboration with ST Microelectronics.

The jitter estimation involves sampling the clock of interest in the vicinity of its rising edges, generating a histogram. Jitter content of the clock is then calculated from the histogram. The BIST uses a self-referenced architecture, where a delayed version of the clock is used for sampling. The delay of the sampling clock is varied using a vernier delay line, whose delay is tuned by varying it's gate and body bias. This possibility of having an additional knob for delay tuning using back bias is thanks to the FDSOI technology in 28nm from ST Microelectronics. It's to be noted that this procedure of jitter estimation leads to the calculation of random jitter content of the signal.

Preliminary electrical simulations of the BIST have resulted in a jitter estimate of a 1GHz clock with a sub picosecond resolution. At present, layout of the BIST along with post-layout simulations is being carried out.

Pierre MALBEC – RFIC-Lab → RMS team



The growing market for Internet of Things (IoT) products creates the need for Integrated Circuits (ICs) allowing always more functions. In terms of miniaturization and cost, it is advantageous to integrate as much components as possible inside one IC, called a System on a Chip (SoC). Theses SoCs integrate components such as Central Processing Units (CPUs), memories, Input and Outputs ports (IOs), or radio modems.

We are interested here in the cohabitation of a Radio Frequency (RF) transceiver and a Switched-Mode Power Supply (SMPS) inside a same SoC. The SMPS allows to significantly reduce the current consumption, thanks to its high conversion efficiency. Low power consumption is a key feature for products designed for the IoT market, especially wireless consumer electronics that often needs to be autonomous in energy and powered by small batteries. Successfully integrating a high efficiency DC/DC converter within a SoC for IoT products is essential.

By its way of functioning (switching techniques), the SMPS is noisy. The switching causes fast current variation on the power supply. These fast current variations occur through the IC package and Printed Circuit Board (PCB) parasitic inductances, generating variation of tension on the common power supply. These electrical pollutions on the power supply can be propagated, by different manner, to sensitive components inside the SoC.

The work for this thesis is based on an existing product designed by STMicroelectronics: a microcontroller that integrate a SMPS as well as a Bluetooth Low Energy (BLE) RF chain. Degradation of the performances of the BLE chain have been observed when the SMPS is activated (degradation of the sensitivity of the BLE chain).

The aim of the thesis is to establish tools allowing to quantify the impact of pollutions generated by a SMPS over the performances of an BLE transceiver, determine which part of the BLE chain is sensitive to the pollutions, and propose solutions to reduce the impact of the SMPS.

Ankush MAMGAIN – RMS team

Title of the Thesis: On-chip generation of high-frequency sinusoidal signals using harmonic cancellation techniques.

Directors: Manuel J. Barragán, Salvador Mir

Presenter: Ankush Mamgain

Summary: The advancement in the CMOS technology has given a great push for integrating more and more complex systems onto a single chip. However, these advanced CMOS manufacturing processes are prone to imperfections, which can lead to degrading the performance of the IC and sometimes malfunctions. After production, it requires a great deal of testing of these ICs to separate the defective ones. Integrating blocks of distinct nature (for example analog-mixed signal blocks, RF, etc.) and limited access to the internal nodes, make the test of these devices more challenging and cost-inefficient. Testing these blocks in these ICs can result in up to 50% of the overall manufacturing cost and this cost is expected to increase in the future as we move to smaller technology nodes. Because, the smaller the technology node is, the more the process variations and defect density will be. Therefore, reducing the cost of the testing for analog-mixed signal circuits and RF circuits is an interesting area of focus and innovation for the semiconductor industry.

A built-in test solution is used to test these circuits. These built-in test solutions facilitate and speed up the testing. A built-in test consists of an on-chip stimuli generator, performing and processing some measurements inside the chip. A built-in test can help in diagnosing the source of the failure and thereby can help in enhancing the production yield through appropriate actions. It also enables an on-field test of the ICs to monitor their health in safety-critical and mission-critical applications.

The goal of this thesis is to develop an efficient built-in test instrument for the characterization of the dynamic parameters of the design under test (DUT). The dynamic characterization requires the generation of appropriate test stimuli (usually a highly linear sine wave) to excite the DUT along with the spectral analysis of the response. The resolution and operating frequency of current mixed-signal systems are increasing, and the fulfillment of these constraints has become extremely challenging for built-in approaches.

In this thesis, our goal shall be to explore the implementation of on-chip generators by exploring novel design techniques based on polyphase oscillators and harmonic cancellation techniques. The combination of these two techniques may enable the generation of high-speed (>1GHz) analog sine waves with high spectral quality while reducing the complexity of the necessary circuitry. The spectral quality of the generated signal is defined by the metric THD (Total Harmonic distortion) which is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental

Hasan MOUSSA – CDSI team

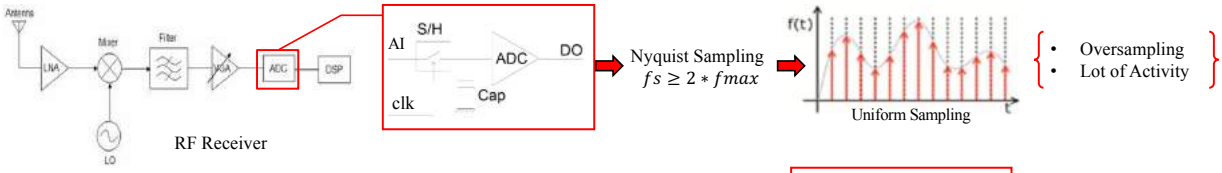
Hasan MOUSSA; PhD Student; 1st year

Thesis Directors: Laurent FESQUET; Estelle LAUGA LARROZE

Subject: **EVENT BASED SMART RF ARCHITECTURES**

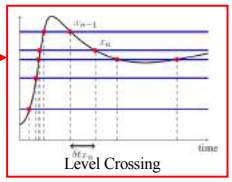
CONTEXT

❖ As the number of connected devices over the internet is increasing, wide band receivers, having low computation and low power consumption are required



❖ Solution: Digitalize the data as soon as possible, taking only the most relevant information

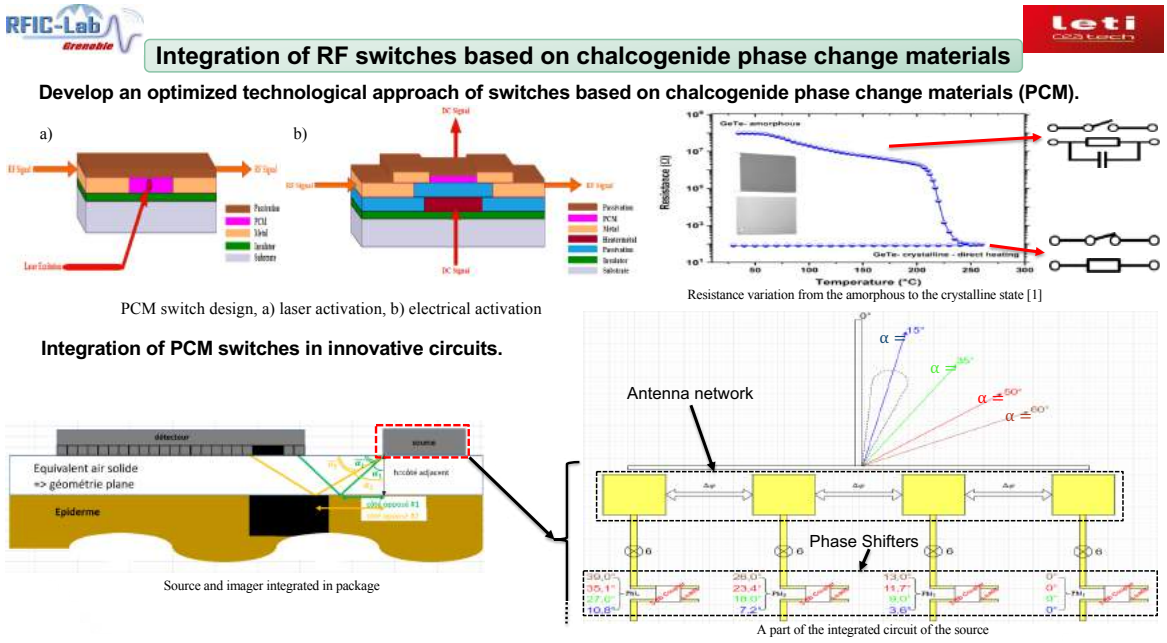
➡ Non-Uniform Sampling:
- Level Crossing
- Peak Detection
- Level and Peak
- Slope



❖ Previous Work: Event-Based Amplitude Shift Keying Demodulator (R.IGA)

❖ OUR WORK: For a Software Defined Radio, design a specific and dedicated Analog to Digital Converter (ADC) which is able to reduce the number of data produced, for specific signals which are RF modulated signals

Ayoub NAOUI – RFIC-Lab → RMS team



[1] A. Ghalem, et al, "Reversible, Fast Optical Switching of Phase Change Materials for Active Control of High-Frequency Functions," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, Jun. 2018

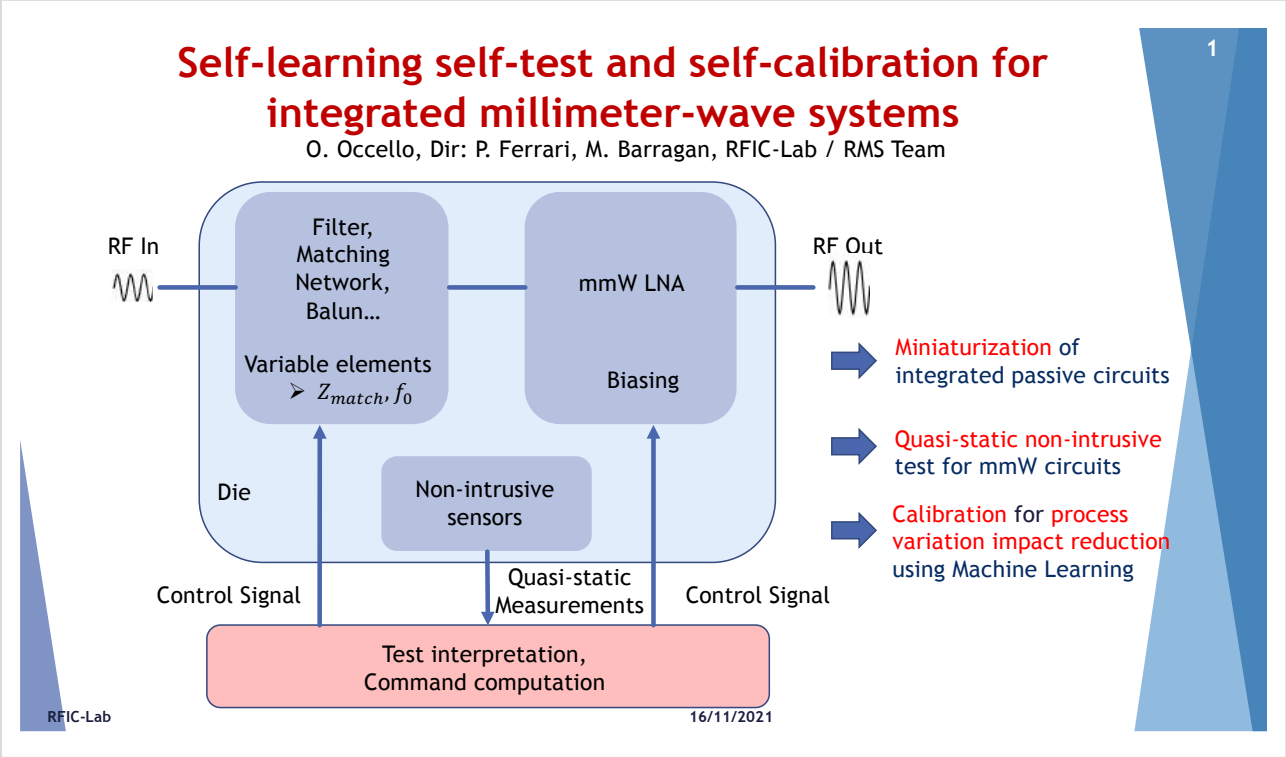
In order to satisfy the requirements of a millimeter (30-300GHz) or sub-THz (300GHz-1THz) medical imaging, it is necessary to develop more efficient millimeter systems, whose electrical properties can be modified according to the need. Millimeter switches, or RF switches, are one of the essential components of these systems and are used, for example, for filter switching, for the reconfiguration of multi-mode and multi-band antenna beams, or for the realization of switching matrices, allowing complex routing of the transmitted or received signal. Beyond millimeter or sub-THz imaging, radar, and 5G-6G telecom applications are also envisaged.

For almost a decade, RF switches based on chalcogenide phase change materials (PCM RF switches) have attracted considerable attention because they have the potential to achieve figures of merit (FoM) in the order of 10fs, which is a factor of 10 improvements over today's best solid-state switches.

Recently, CEA-LETI has produced an RF switch based on a PCM alloy, GeTe, with state-of-the-art performance. Preliminary design laws have been defined, demonstrating the very high potential of these switches. However, a great work must be done before obtaining a component that provides the necessary performance for the targeted applications. In particular, the resistive transition of the PCM material enabling switching is achieved thermally via Joule heating. Thus, the energy efficiency of the switch, as well as its performance, reliability, and endurance, will strongly depend on the phase change material used, the technological stacking achieved, the geometry of the switch, and the means of applying the thermal pulse.

The proposed thesis work will define the main specifications of the switches for the targeted applications and identify the key properties required of the phase change material. The aim is to evaluate different chalcogenide material alloys and to develop a technological integration path for switches that will optimize the reliability, electrical and energy performance of the component.

Olivier OCCELLO – RFIC-Lab → RMS team



David OUATTARA – RFIC-Lab → RMS team

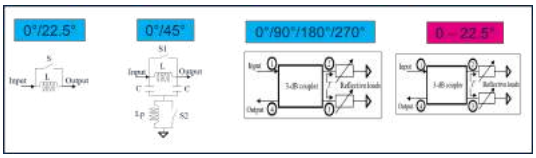
OUATTARA David, 2nd Dec. 2019 – 1st Dec. 2022

Design of phase shifters based on new architectures for mm-wave applications: 5G/6G & automotive radars

Supervisors : Philippe FERRARI & Sylvain BOURDEL (**RFIC-Lab**); Cédric DURAND & Frédéric PAILLARDET (**STMicroelectronics**)

- **Why?** : Challenge beamforming performance at mmW frequencies (>80GHz) → Phase shifters losses bottleneck (Technology, devices, design, CAD)

- **Objective** : Design a full 0 – 360° continuous passive phase shifter at 120GHz in BiCMOS 55nm
- **Solution** : Use a mixed digital/continuous phase shifters to take advantage of both
- **Proposes architecture** : 3 digital (4 bits → 16 states) & 1 continuous phase shifter



- **Executive Summary (Simulation results)** :

Blocks	0°/22.5°	0°/45°	0°/90°/180°/270°	0-22.5°
Topology	MOS or PIN diode based Switched-line	MOS based Switched-filter	Digital RTPS	Continuous RTPS
ILmax (dB) @ 120GHz	0.8	1.2	2.4	4.2
Overall	Maximum Loss estimated ≈ 8.6dB → FoM ≈ 41.9°/dB			

- **Conclusion** : **All key blocks designed** and sent to fabrication. Wafer are waited for measurements
- **Future works** :
  - Building blocks version improvement (Reducing losses)
  - **Full hybrid phase shifter assembly**

Systems operating in millimeter bands are now an evidence to satisfy the need for data rates for mobile communications. To take full advantage of the bandwidth offered in millimeter bands, it is essential on the one hand to have local oscillators allowing to scan a wide range of frequencies, and to change the way in which the terminals and relays operate to meet the energy requirements.

In the case of local broadband oscillators, this involves the production of VCOs with a wide frequency tunability, while in the case of energy problems, the solution is to focus the beam to achieve low-energy point-to-point communications. To have a dynamic point-to-point communication required for mobile applications, it is necessary to be able to modify the orientation of the beams by electronic control. This involves the use of phased arrays that require phase shifters to modify the phase of the signals to be transmitted or received at each antenna.

Overall, a phase shifter is expected to be accurate at the phase level and to have the highest possible factor of merit (the ratio between phase shift and the insertion loss). In the literature, there are active and passive phase shifters.

Active phase shifters are the most widely used due to the simplicity of the architecture and their compact and inexpensive geometry on the silicon surface. However, they suffer from a high DC consumption, because of the “active circuit” approach. The drawback of this approach is that it also deteriorates linearity, limiting transmission power.

Passive phase shifters address DC consumption and linearity issues. On the other hand, they have high insertion loss and use a large silicon area.

The objective of the thesis is to work on passive phasers, despite the disadvantages mentioned above. Also, to value passive phase shifters compared to active phase shifters, we decided to work at 120 GHz where active components begin to show their limits at the level of consumption (due to lower yield) and linearity.

Dayana PINO MONROY – RFIC-Lab → RMS team

Dayana PINO, Cifre ST/RFIC Lab, Oct/19 – Jan/23

RF design methodology based on MOS transistors for circuit/technology co-optimization

WHY?

Co-optimization between technology and application by changing the design method to bring designers closer to the physics of the MOS transistor in a simple way

HOW?

Provide a MOS model:

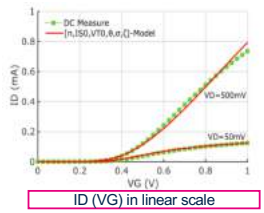
- *Few parameters*
- *All operation regions*
- *Including short channel effects*
- *Non-linearities*

Develop a design methodology

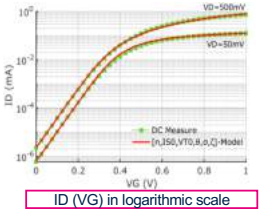
WHAT?

Revisit Advance Compact MOSFET (ACM) model (3 Parameters)

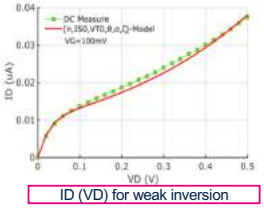
- *Propose 7-Parameter model based on 28FDSOI measurements*
- *Demonstrate the capacity of the model with a design methodology for an Low Noise Amplifier (LNA)*



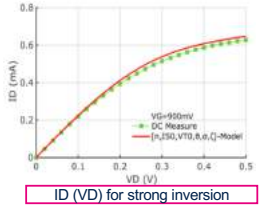
ID (VG) in linear scale



ID (VG) in logarithmic scale



ID (VD) for weak inversion



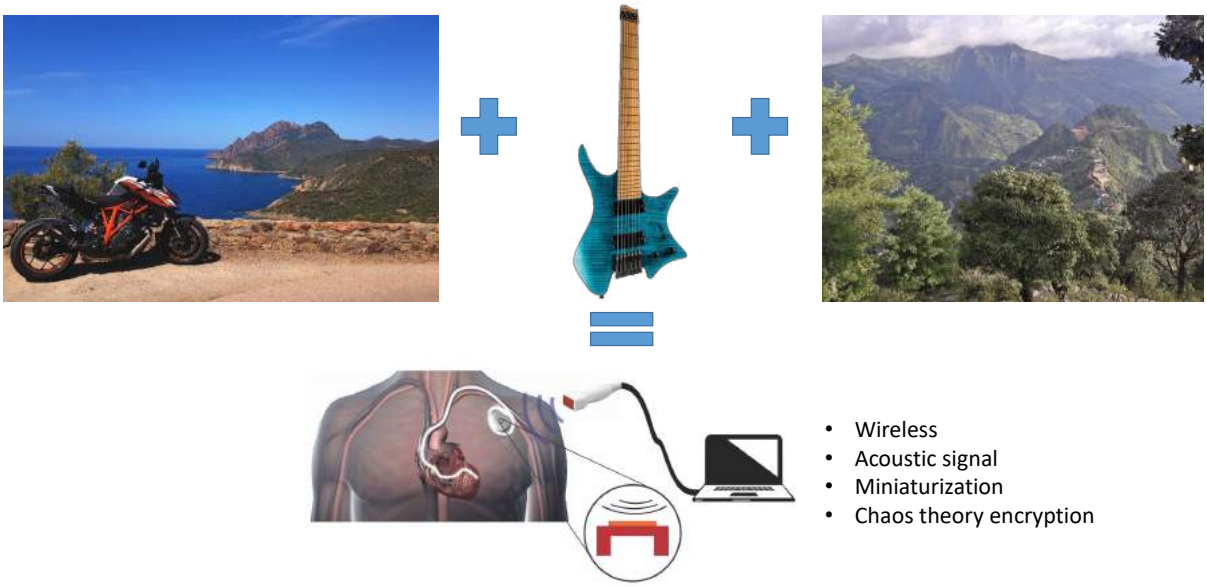
ID (VD) for strong inversion

The main objective of this work is to develop a design methodology that allows the designer to have a tool relating the technology and the performances of a certain circuit. To achieve this, we propose a model for a MOS transistor based on 7 parameters allowing to preserve the link with the main physical effects of the MOS. The model is accurate, simple and practical so that it can be used in the circuit design, in our case, an LNA Noise Canceling Balun based on the specifications of gain, figure noise and 3rd order intercept-point (non-linearities) in 28nm FDSOI technology. Finally, it is expected that by knowing the wanted performances for a certain circuit, it will be possible to determine which will be the most adapted technology or which technological aspects are the most important to achieve these performances for a given application.

Pierre TACYNIAK – CDSI team

Secured wireless piezoelectric power transmitter for medical implants

Pierre Tacyniak
Supervisors : Skandar Basrour, Martial Defoort



- Wireless
- Acoustic signal
- Miniaturization
- Chaos theory encryption

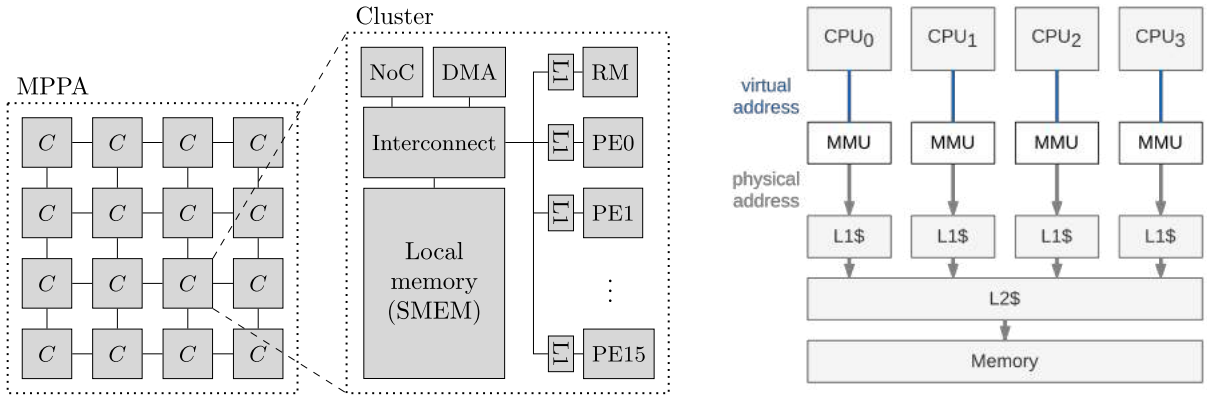
Emilien TALY – AMfoRS team

My work during these six months of thesis revolves around two axes: The state of the art of In Memory Computing (IMC) based on SRAM and more precisely for Multiplications-ACcumulation(MAC) operations for the inference of Convolutional Neural Networks (CNN). And part of the time has been spent on implementing an IP from STMicroelectronics, an accelerator for CNN inference called Tensor Processing Unit (TPU). The thesis goal is to keep the same paradigms in which the calculations are carried out, in order to carry them directly in memory. Indeed, if we bring together computation and memory, we increase the bandwidth and also energy with an energy cost more than 50 times for SRAM read and6000 for DRAM read, compared to 8 bits multiplication. On the state-of-the-art part, a classification was made with on the one hand, the computation techniques in SRAM and on the other hand, the different ways to map a convolution in SRAM. The computation can be entirely digital with the addition of logic in the periphery after the sense amplifier or with a custom bitcell, but also mixed analog-digital with a relationship between the bitline voltage, and activated wordline number. Much of the architecture relies on bitline-level computation by activating multiple wordlines at the same time. The bit-per-bit computations can be done between two operands in two different cells, this is the case for digital architectures, or with an operand in the bitcell and the second modulated through the wordline (voltage, pulse width or pule count) for the case of mixed architectures. On the IP implementation, I worked on the quantization part in order to be bit accurate with the Tensorflow framework, on optimizations of data placements in memory and since two months, on the realization of a testchip including our IP made in HLS (in C ++), a wrapper to manage the different accesses to data/weights SRAM and as well as an APB for the connexion with the top of the testchip including a RISC-V.

Arthur VIANES – SLS team

Integration of a Manycore Accelerator in a High-Performance Processor

Software Cache coherence for Kalray MPPA Processors



Supervisors: Frederic ROUSSEAU - Frederic PETROT

TIMA PhD Day - November 18th, 2021 Arthur VIANES SLS

Modern High-Performance Processors consist of general-purpose cores and dedicated accelerators for various applications. Common examples of dedicated accelerators are GPU or Neural Processing Units (NPU).

This industrial Ph.D, conducted as a collaboration between the TIMA laboratory and Kalray company, investigates the integration of the Kalray MPPA accelerator into a High-Performance Processor environment. This work is also part of the European MontBlanc2020 project, a European High-Performance Processor that features a Kalray accelerator.

During the previous years we worked on a hardware emulation platform for our accelerator and on software layers to offload a workload from a general purpose processor to the Kalray accelerator. Following this work, we are investigating how to make this platform more suitable for conventional programming models, focusing on the memory system and the cache coherence of our accelerator.

The Kalray accelerator is partially cache coherent, it only features local cache coherence within clusters, each cluster is described as an isolated coherence domain. Therefore, we are currently working on the definition of a global cache coherence protocol in software that allows to combine all the coherence domains into a single global coherence domain.

By the term "cache coherence protocol" we do not mean a software emulated cache but rather a software based cache coherence maintenance of hardware caches. This protocol guarantees by software that the memory is always coherent, whether or not a hardware cache is present. The particularity of this protocol is to provide coherence between several coherence domains and can allow, in the context of an accelerator, to provide global cache coherence between the host and the accelerator without adding hardware.

Sergio VINAGRERO GUTIERREZ - AMfoRS team

Design and Evaluation of Resistive-based Security Primitives

Physically Unclonable Functions & True Random Number Generators

Memristors

- Resistance controlled with voltage.
- Cycle to cycle & Device to Device variability

Physical Unclonable Functions

- Exploit random variability to generate secrets or identification

True Random Number Generators

- Exploit stochasticity to generate random numbers

servinagrero

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