Mixed-Mode Stress in Silicon-Germanium Heterostructure Bipolar Transistors: Insights from Experiments and Simulations

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***Abstract*— Recently, a wide class of market segments (e.g., health, material science, security, and communications) is tackled by circuits fabricated in BiCMOS technology integrating silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) and passives. Currently, the reliability of SiGe HBT devices is a major concern, and much attention is given to self-heating (SH), that limits device performance and regulates their degradation during stress. Moreover, its relevance is supposed to increase with the device scaling. In this work we explore the reliability issues of SiGe HBTs by combining dedicated experiments and TCAD simulations. We develop and calibrate a TCAD model that is then used to investigate SH effects in both operating and stress conditions. Results show the important role played by the back-end-of-line (BEOL) and by the substrate thermal resistance in dissipating the heat generated by impact ionization. The location at which defects are generated during stress and the microscopic properties of the defects are determined experimentally by means of dedicated noise measurements. Including defects in the TCAD model allows reproducing the degradation observed in stress experiments. Simulations of the SH effects on a stressed device in measurement conditions revealed the presence of a hole hot spot that suggests a possible physical mechanism involved in the degradation slowdown at long stress times reported in the literature.**

***Index Terms*— SiGe, Heterostructure Bipolar Transistor (HBT), Self-Heating, TCAD Simulation, Random Telegraph Noise, Defects, Traps, Stress.**

I. Introduction

THE strong need for innovative solutions in many vital sectors of the global economy such as smart personal health, next-generation communications, smart cities, security, and the Internet of Things, resulted in a markedly increased interest in the mm- and sub-mm-wave portions of the electromagnetic spectrum [1-3]. From the technological standpoint, this trend fostered the growth of the BiCMOS technology as an attractive and scalable solution that allows a cost-effective on-chip integration of high-performance silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) (that outperform their best-in-class Si-based CMOS counterpart in terms of cutoff frequency) with passive components that greatly helps in lowering the cost of chip fabrication for the targeted market. Due to their unique properties, BiCMOS devices are widely employed in high-speed circuits such as amplifiers for next- generation 5G networks and THz industrial sensors, responding to the demand of a large market that cannot be currently tackled by CMOS technology [1-3]. Nowadays, the BiCMOS process has reached a significant level of complexity, and with scaling SiGe HBT devices get more subjected to self-heating (SH) that can have a detrimental impact on the device reliability [4-5]. Moreover, these devices are frequently driven close to the Safe-Operating-Area (SOA) limits, which makes it important to investigate the reliability issues in conditions that are close to the operating ones. In this paper, we extend our previously published conference paper [6], in which we investigated the reliability of state-of-the-art SiGe HBTs, by combining stress experiments and TCAD simulations with a dedicated statistical noise analysis aimed at identifying the location at which defects are generated during stress.

First, we develop a 2D TCAD model of SiGe HBTs that can be used to investigate the reliability issues of these devices. The model is calibrated against experimental data measured

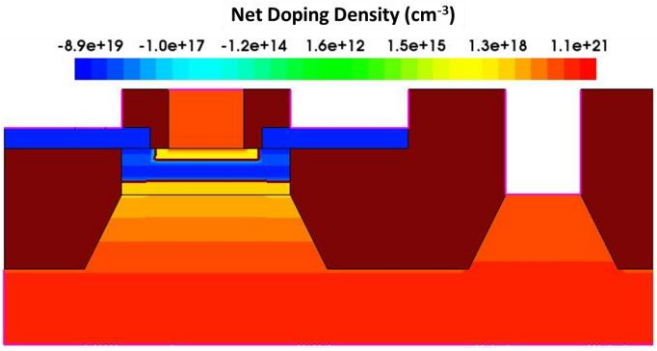

Fig. 1 – Schematic representation of the simulated HBT SiGe device. Color-code reflects the net doping density in the different regions of the device. Positive doping density means n-type doping while negative doping density means p-type doping.

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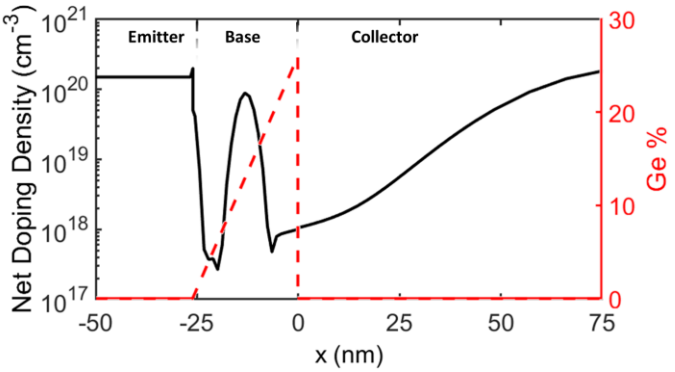

Fig. 2 – Doping (black solid line, left y-axis) and Ge % (red dashed line, right y-axis) vertical profiles. The emitter, base, and collector regions are evidenced.

Parameter	Value
Emitter Doping	$1.5 \cdot 10^{20}$ cm^{-3}
Base Peak Doping	$9.9 \cdot 10^{19}$ cm^{-3}
Coll. Doping (min/max)	$2 \cdot 10^{18}/10^{21}$ cm^{-3}
Peak Ge %	26 %
R_{TH} Emitter	2 cm^2·mK/W
R_{TH} Base	0.1 cm^2·mK/W
R_{TH} Collector	0.2 cm^2·mK/W
R_{TH} Substrate	3.5 cm^2·mK/W *

Tab. I – Calibrated process parameters (doping levels, peak Ge % in the base, and thermal resistance at both the electrical contacts and the substrate). * The R_{TH} value of the substrate thermode is taken from [9].

on 55-nm BiCMOS SiGe HBT devices. This model is then used to investigate both the SH effects and the role played by SH in the degradation dynamics observed experimentally in mixed-mode stress conditions. The comparative analysis of the SH effects in operating conditions and during stress is carried out by using thermal maps obtained from the TCAD, which allows gaining further insights into the physical mechanisms determining the device degradation. The results allow understanding the different roles played by the impact ionization, and the carriers' and lattice heating in the degradation dynamics observed in these devices and associated with defects generation at a specific device location. The preferential locations for defect creation are identified experimentally by means of the analysis of Random Telegraph Noise (RTN) that appears in the base current of SiGe HBTs as a result of the applied stress. The statistical characterization of RTN are used together with the outcomes of the TCAD thermal maps to gain deeper insights into the microscopic properties of the defects generated during stress.

II. Devices, Experiments, and Simulations

The devices analyzed in this study are state of the art SiGe HBTs fabricated in 55-nm BiCMOS technology, Fig. 1. Devices, in the CBEBC configuration, have an emitter window of 5.56 x 0.42 µm^2. Forward Gummel (I_B - V_{BE} and I_C - V_{BE}) and output curves (I_C -V_{CE}) are collected at different stages of cumulative stress (from fresh to full stressed) in mixed-mode stress conditions. Stress is performed by forcing an emitter current density, J_E = 1 mA/µm^2, which corresponds

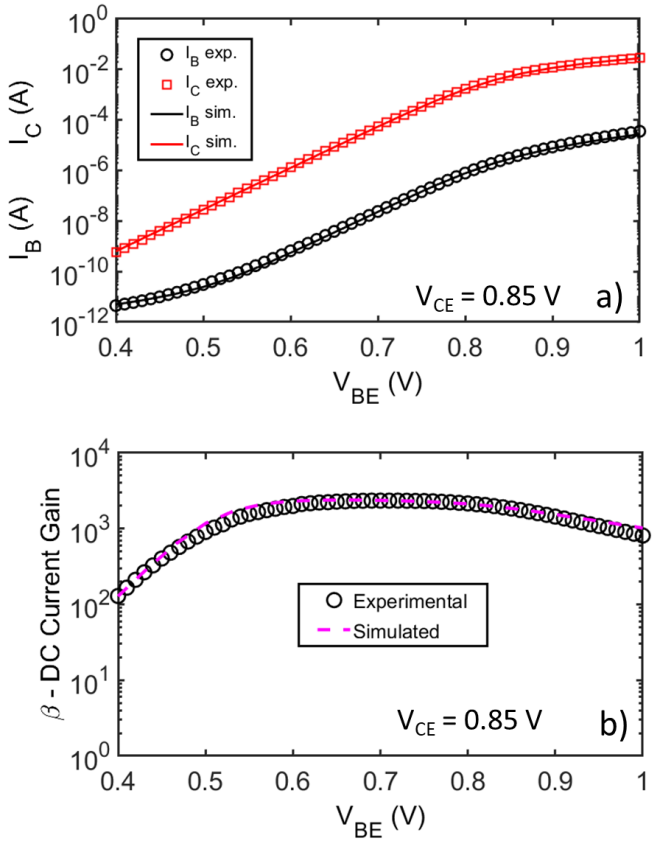

Fig. 3 – Comparison between experimental data (symbols) and 2D TCAD simulations (lines). (a) I_C vs V_{BE} (red) and I_B vs V_{BE} (black) at V_{CE} = 0.85V. (b) DC current gain ($\beta = I_C / I_B$) vs. V_{BE} at V_{CE} = 0.85V.

to a V_{BE} value in the typical operating range (i.e., V_{BE} close to 0.85 V) where the peak f_T is obtained [1]. The voltage at the collector-base junction is V_{CB} = 3 V as a reasonable trade-off between keeping stress conditions close to the operating ones and getting a non-negligible degradation in a reasonable amount of time, with the total stress time set to 5000 s. In order to gain additional knowledge on the defects generation process during stress, RTN measurements are performed before and after stress by applying a DC bias on the base (0.8 V ≤ V_{BE} ≤ 0.92 V) and collector terminals (0.85 V ≤ V_{CE} ≤ 1.2 V) while sampling both the base (I_B) and the collector (I_C) current simultaneously with a sampling time t_s = 34 µs and a total measurement time t_{meas} = 2 s. All measurements are performed at room temperature.

The structure of the device implemented in SDevice™ is shown in Fig. 1. Both the structure and the mesh were derived by refining an existing model in SDevice™ for the HBT device. The mesh refinement process was executed by trying to optimize the trade-off among computation time, simulation accuracy, and reproducibility. The doping profiles and the thickness of the different layers were set in agreement with the specifications of the device provider. The vertical doping and Ge content profiles are reported in Fig. 2. In agreement with results in the literature, the shape of the doping profile in the emitter region is assumed flat, while a Gaussian doping profile is adopted in the base region [1]. The shape of the doping profile in the collector and sub-collector regions and, in general, the overall doping profile in Fig. 2, agrees with the one suggested by a TCAD- based roadmap developed recently

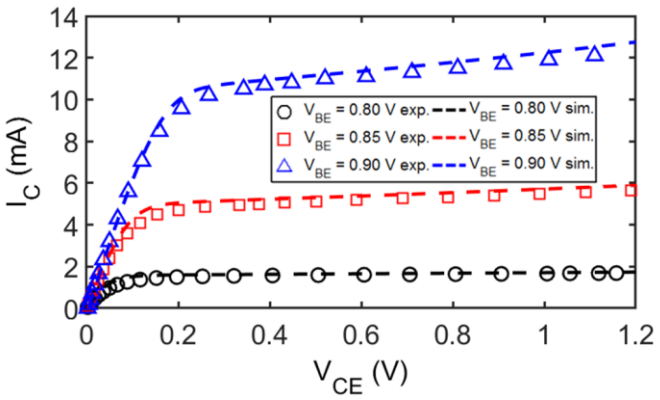

Fig. 4 – Experimental (symbols) and simulated (dashed lines) output curves at different V_{BE} in the range 0.8 V to 0.9 V typically used in circuits (different symbols and colors).

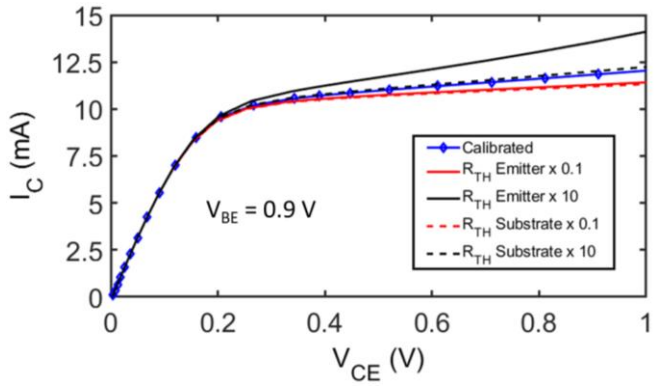

Fig. 5 – Output curves (at V_{BE} = 0.9 V) sensitivity to the substrate (dashed lines) and emitter (solid lines) thermal resistance values. Red (black) curves correspond to a 10 times lower (higher) thermal resistance than the nominal one. Blue line with diamonds corresponds to the calibrated output curve (nominal thermal resistance values) at V_{BE} = 0.9V.

in the framework of the successful DOTSEVEN project [1]. The Ge content profile in the SiGe base, shown in Fig. 2, is assumed linear for simplicity, starting at zero at the interface with the emitter and reaching its peak at the interface with the collector. The peak doping values in all regions and the peak Ge relative content in the base are summarized in Tab. I. In order to carefully reproduce the device static characteristics (i.e., the forward Gummel and output curves) shown in Figs. 3 and 4, a hydrodynamic transport model is used in the TCAD simulations [7], which allows also calculating the lattice and carriers' (both electrons and holes) temperature 2D profiles, together with calibrated models for carriers' recombination (Shockley-Read-Hall with trap-assisted contribution), impact ionization (Okuto model), and field-, material-, and doping-dependent mobility [7-9]. In this respect, calibrating the parameters of such models for SiGe required only a slight tuning of few parameters [9], while default values for Si and polysilicon were used which consolidates the soundness of the proposed TCAD model. Series resistances were included at all contacts, and their values were calibrated to capture the behavior of the output curves in the saturation region. The emitter contact non-idealities are modeled by including a finite recombination velocity for holes, as reported in the literature [8]. To capture the behavior of the output curves in the active region where the thermal effects are supposed to play a major role, i.e., at relatively high V_{CE}, Fig. 4, thermal resistance for all the *thermodes* (thermal interfaces located at the emitter, base, and collector contacts and at the bottom of the substrate) needs to be included. Since their values dictate the SH dynamics at high V_{CE}, they strongly affect the output curve slope in the active region [9], as shown in Fig. 5. The value of thermal resistance at the device electrical contacts (emitter, base, and collector) experience strong variations with process schemes and conditions. Particularly, the materials and structure of the metal lines of the back-end of line (BEOL) strongly influence the local thermal dissipation as shown in Fig. 5. As such, the thermal resistance values of the *thermodes* at the device electrical contacts were calibrated to obtain the best possible fit of the output curves, Figs. 4 and 5. The thermal resistance of the substrate *thermode* is set in agreement with previous results reported in the literature [9-13]. The calibrated values for all thermal resistances are reported in Tab. I. Finally, reproducing the non-ideal excess base current at low V_{BE} (noticeable in Fig. 3a as a deviation from a pure exponential) required including mechanisms for auger recombination, band to band tunneling, and trap-assisted tunneling at defects at the emitter-base (E-B) spacer interface, that are included with a density of $6 \cdot 10^{10}$ cm^{-2}.

III. Self-Heating in Operating Conditions

The developed TCAD model is now used to predict the reliability of SiGe HBT devices in both operating and stress conditions. Particularly, we explore the detrimental effects of hot-carrier degradation (HCD) on i) the device self-heating (SH) and ii) the formation of interface (or near-interface) defects at the E-B spacer that cause an excess base current due to trap-assisted recombination. Figure 6 shows the 2D maps of the impact ionization rate, and of electrons (e^-), holes (h^+), and lattice temperature in operating conditions. Hot-carriers (e^- and h^+) accelerated by the collector-base electric field determine impact ionization in the space charge region of the collector-base junction. This process results in i) the generation of e^-/h^+ pairs and ii) localized power dissipation. This mechanism is fully consistent with the features of the 2D maps in Fig. 6(a-f), where it is evident that the impact ionization rate increases significantly with the electric field in the space charge region of the collector-base junction (i.e., on the V_{CB}). Moreover, both the e^- and h^+ temperature maps well correlate with the impact ionization rate map. It is widely accepted that the carriers generated upon impact ionization are then accelerated by the electric field toward the E-B spacer where they are supposed to dissociate Si-H bonds at the Si/SiO_2 interface that results in the generation of new interface (or near-interface) defects [14]. On the other hand, the heat that is locally generated by impact ionization is transferred to the lattice by phonon exchange and then dissipated via the low thermal resistance paths in the device (i.e., the substrate and the BEOL over the electrical contacts that behave as heat sinks).

For the technology under study, it is evident from the 2D thermal map of lattice temperature that the self-heating peaks in the collector region, as the substrate behaves as the main thermal dissipation pathway, while the temperature increase near the electrical contacts is almost negligible. This asymmetry in the thermal dissipation explains why the lattice

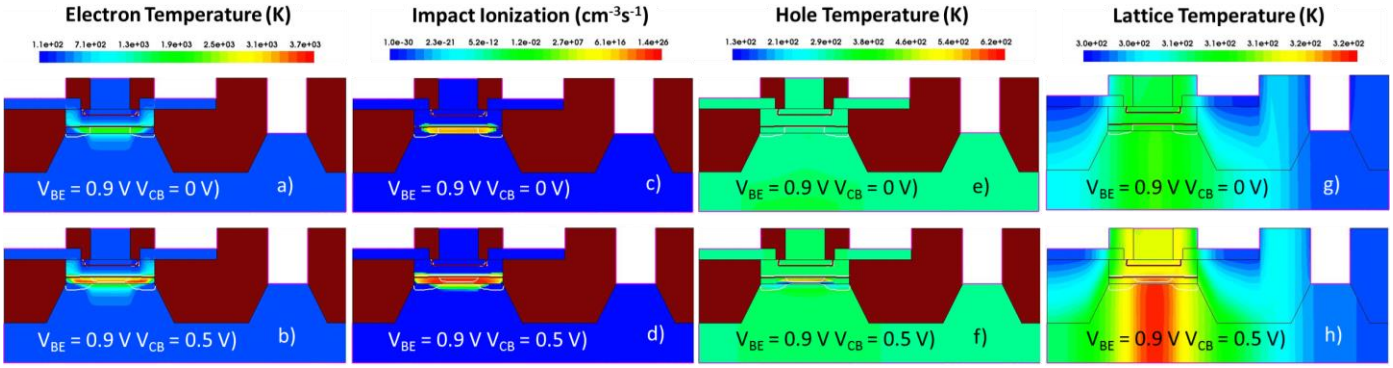

Fig. 6 – Simulated 2D maps of (a-b) e^- temperature, (c-d) impact ionization rate, (e-f) h^+ temperature, and (g-h) lattice temperature at V_{BE} = 0.9V and (a, c, e, g) V_{CB} = 0V, (b, d, f, h) V_{CB} = 0.5V. The bottleneck for heat dissipation is the substrate due to its larger thermal resistance as compared to the one given by the BEOL over the contacts.

temperature map badly correlates with the carriers' temperature maps. As such, decreasing the effective thermal resistance at the substrate interface could be effective for the thermal engineering of the device. Nevertheless, SH in operating conditions seems not to be critical for the technology under study, as the lattice temperature increase is limited to few tens of degrees in typical operating conditions (~20 K increase from 300 K at V_{BE} = 0.9 V and V_{CB} = 0.5 V, Fig. 6). However, this is not the case when the device is driven in stress conditions, as the increase in the lattice temperature will be more marked, possibly accelerating the degradation dynamics and facilitating the generation of new defects

IV. Random Telegraph Noise Analysis

In order to shed light on the effects of the electrical stress on the device in both nominal and harsher operating conditions (e.g., close to the safe operating area limits as typically done in power amplifier circuits for high-frequency communications [15]) we perform a detailed time-domain noise analysis. Specifically, we investigate the features of Random Telegraph Noise (RTN) appearing in the base (I_B) and in the collector (I_C) currents. For this purpose, we bias the device using V_{BE} and V_{CE} values that are in the range of the nominal operating conditions of the device and simultaneously sample I_B and I_C over time. For devices in pristine conditions (i.e., before the application of any electrical stress), no clear RTN could be detected neither in I_B nor in I_C, which highlights the good quality and low defect density of the pristine samples. This was confirmed by analyzing many devices and by applying different V_{BE} and V_{CE} values. However, clear RTN fluctuations were detected in I_B and I_C currents after delivering electrical stress to the device. Of course, due to the transistor effect, the RTN detected in I_B and I_C currents showed a high degree of correlation, with the I_C traces being noisier than the I_B traces. For this reason, we analyzed the RTN appearing in the base current. RTN is investigated at different V_{BE} (keeping V_{CE} fixed) and different V_{CE} (keeping V_{BE} fixed) to help in understanding the nature and location of the defects generated during stress.

Analyzing RTN traces can be a challenging task and for this reason it is only rarely performed [16] and the simpler although less informative low-frequency noise spectral analysis is performed [17-19]. Indeed, in their simplest form,

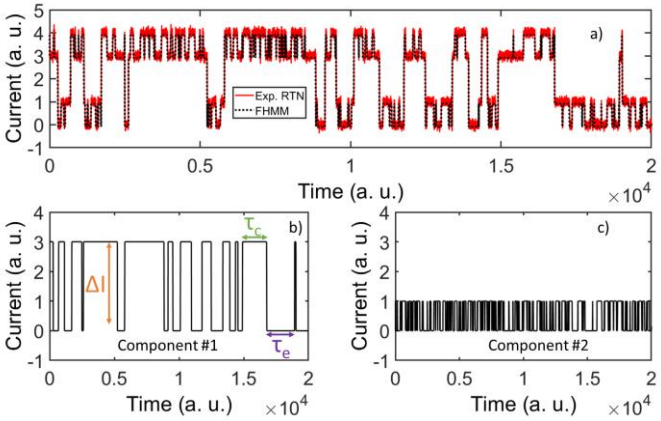

Fig. 7 – a) Example of a multilevel RTN signal (red line) with four discrete levels along with its FHMM fitting (dashed black line). The FHMM analysis allows separating the multilevel RTN signal into its components (two, in this case) that are separately shown in b) and c). In b), the statistical properties of a two-level RTN signal (ΔI, τ_c, and τ_e) are evidenced.

RTN signals are characterized by two discrete levels and are associated with charge carriers capture/emission into/from an individual defect [20-21]. Such signals are relatively easy to be processed with the aim of extracting their statistical properties, i.e. the amplitude of the current fluctuation (ΔI), and the average capture (τ_c) and emission (τ_e) times – see Fig. 7b. Typical tools used to perform the extraction include histograms (see Fig. 8b), time-lag plots, and statistical techniques [20-21]. Nevertheless, in the case under study, we detect multilevel RTN (see Fig. 8a), exhibiting more than two discrete levels and associated with capture and emission processes happening at more than one defect site [20-22]. These signals are more complex to be analyzed, and many conventional analysis tools result ineffective since they only give partial information (e.g., the number and values of discrete levels – L1, L2, and L3 in Fig. 8a), failing at retrieving correctly the capture and emission times [20-22]. However, such signals can be seen as a superposition of many two level RTN signals, each associated with trapping and de-trapping at an individual defect, called *components*. In order to quantitatively determine the statistical features (ΔI, τ_c, and τ_e) of the different components (and of the associated defects) we analyze the multilevel RTN signals using the Factorial Hidden Markov Model (FHMM), which allows separating the

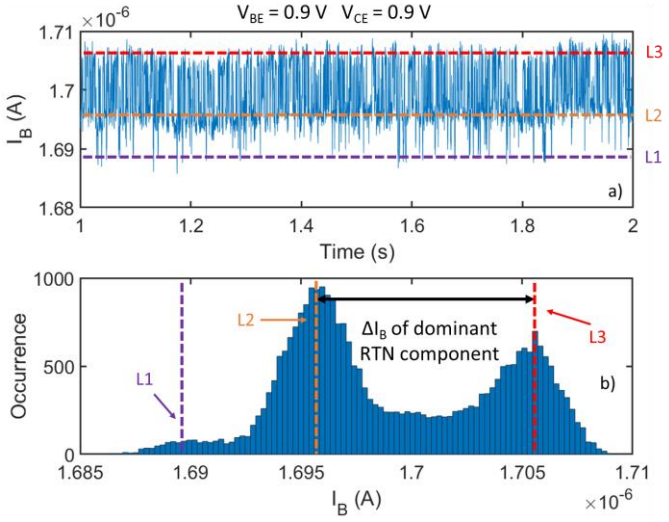

Fig. 8 – a) Multilevel RTN signal experimentally detected in the base current measured at V_{BE} = V_{CE} = 0.9V, exhibiting three discrete levels, L1, L2, and L3. b) The histogram of the signal in a), showing the three discrete levels. The dominant two-level component is identified with the widest fluctuation that switches between L2 and L3 (so that ΔI_B = L3 - L2).

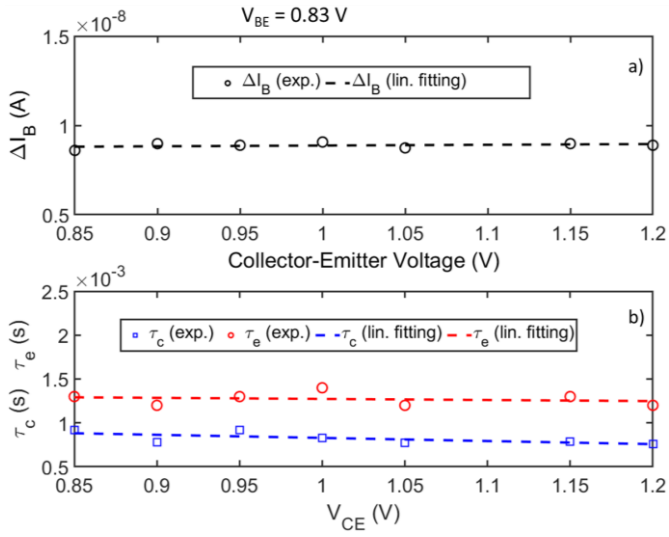

Fig. 9 – Dependence of the statistical properties of the dominant RTN component on V_{CE} keeping V_{BE} fixed at V_{BE} = 0.83 V. ΔI_B (black circles) is reported in a) while τ_c (blue squares) and τ_e (red circles) are reported in b). Linear fittings are also reported (dashed lines). All statistical properties are insensitive to the base-collector biasing.

multilevel RTN (light blue line in Fig. 8a) into its components (Fig. 8b and 8c) [22]. Particularly, we use the FHMM analysis to retrieve the properties of the dominant RTN component (the one with the largest amplitude – component # 1 in the example reported in Fig. 7) at different biasing conditions.

In order to better understand the location of the defect responsible for the observed RTN, we first record the RTN fluctuation at different V_{CE}, keeping V_{BE} fixed, and analyze the statistical properties of the dominant RTN component vs. V_{CE}. In such conditions, only the collector-base junction bias changes. Results are reported in Fig. 9, and clearly demonstrate that the RTN statistical parameters are insensitive to the collector-base junction biasing conditions, which suggests that the defect is not located in device regions that are sensitive to the collector voltage. On the opposite, the analysis

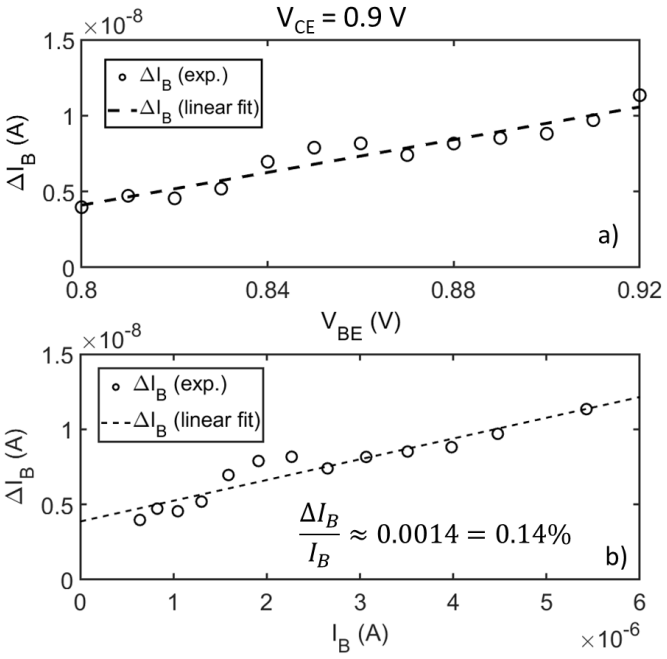

Fig. 10 – Dependence of ΔI_B (empty symbols) of the dominant RTN component on V_{BE} (a) and I_B (b) keeping V_{CE} fixed at V_{CE} = 0.9 V. Linear fittings (dashed lines) are also reported.

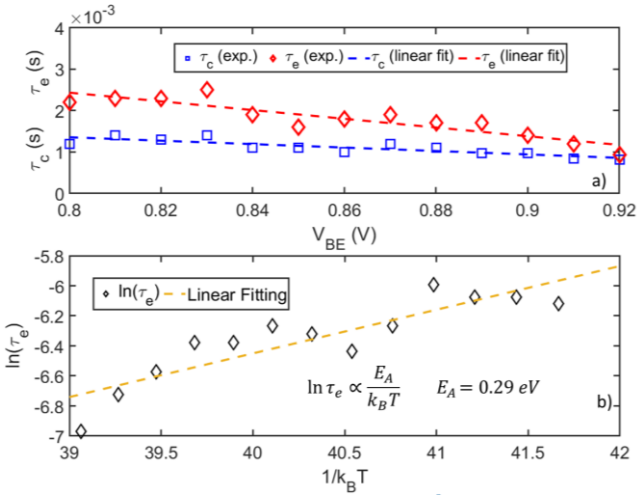

Fig. 11 – a) Dependence of τ_c (blue squares) and τ_e (red diamonds) of the dominant RTN component on V_{BE} keeping V_{CE} fixed at V_{CE} = 0.9 V. Linear fittings are also reported (dashed lines). b) The natural logarithm of the emission time, $\ln(\tau_e)$, is plotted against $1/k_B.T$ (black diamonds). A linear fitting (orange dashed line) is used to extract the slope of the curve that corresponds to the activation energy of the defect, E_A = 0.29 eV.

of the same RTN signal recorded at different V_{BE}, keeping V_{CE} fixed, shows that the defect statistical properties are sensitive to the base-emitter junction biasing. This provides an independent confirmation that the defects generated during stress are likely to be close to the E-B spacer interface, far from the base-collector junction and from the shallow trench isolation sidewalls. Specifically, the fluctuation amplitude ΔI_B increases with V_{BE}, as shown in Fig. 10a. The forward Gummel curves can be used to convert V_{BE} to the corresponding I_B, which allows plotting ΔI_B as a function of I_B, Fig. 10b. Moreover, both capture and emission times decrease with increasing V_{BE}., as reported in Fig. 11a. These findings are in agreement with what reported in the literature.

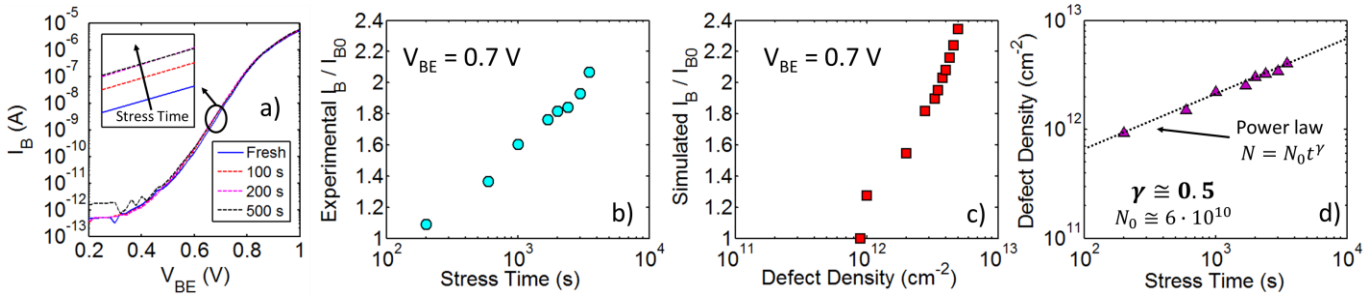

Fig. 12 – (a) Experimental I_B vs. V_{BE} curves at different levels of cumulative stress. (b) Experimental I_B degradation as in (a) measured at V_{BE} = 0.7 V vs. cumulative stress time. (c) Simulated I_B degradation at V_{BE} = 0.7 V at different defect density values. (d) Extracted defect density vs. cumulative stress time along with a power-law fitting.

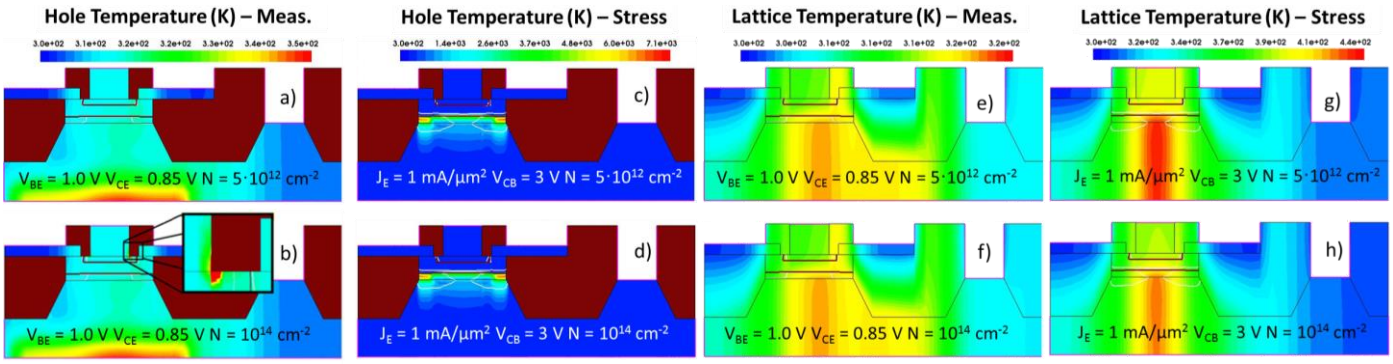

Fig. 13 – Simulated 2D maps of (a-b-c-d) h^+ temperature, and (e-f-g-h) lattice temperature in (a, b, e, f) measurement conditions, i.e., V_{BE} = 1.0 V and V_{CE} = 0.85 V, and (c, d, g, h) stress conditions – J_E = 1 mA/μm², V_{CB} = 3 V – at defect density of (a, c, e, g) $5 \cdot 10^{12}$ cm^{-2}, and (b, d, f, h) 10^{14} cm^{-2}. In (b) a zoom-in shows a hot hole spot close to the region where defects are located.

In the analysis reported in [23], different trends of the RTN parameters vs. applied V_{BE} were observed. Particularly, RTN traps were detected that showed a small (<1%) $\Delta I_B/I_B$ and both capture and emission times weakly decreasing with the applied V_{BE}, like the one found in this study (for which $\Delta I_B/I_B$ ≈0.14%). In [23], the authors attributed such behavior to trapped electrons in SiO_2 that can change the recombination rate in the space charge region to a lower level, and thus lower the recombination current. It is hence likely that the RTN signals detected in this study arise from a non-radiative multi-phonon trap-assisted tunneling (TAT) of electrons into traps generated during stress in the E-B spacer or at its interface. According to the TAT formalism [24], charge carriers' emission is highly likely to happen from the ground state of the trap, which results in a bias-independent emission time. Specifically, we recall from [24]:

$$\tau_e \propto e^{\frac{E_{REL}}{4k_BT}} = e^{\frac{E_A}{k_BT}} \; with \; E_{REL} = 4 \cdot E_A \qquad (1)$$

where k_B is the Boltzmann constant, T the absolute temperature, E_A the activation energy for the emission process, and E_{REL} the relaxation energy that is a physical parameter of the defect related to the energy exchanged between the defect and the lattice when a charge carrier tunnels into/out of a defect as a result of the spatial rearrangement of the atoms in the vicinity of the defect [24].

The observed decrease of τ_e with V_{BE} can be attributed to the localized lattice temperature increase resulting from self-heating, as emphasized in Section III. Such local lattice temperature variations with V_{BE} can be extracted from the simulations in Section III: using the lattice temperature maps calculated at different V_{BE} keeping V_{CE} fixed, i.e. in the range in which RTN measurements have been performed, we extract the average temperature increase with V_{BE} along the E-B spacer interface. It is then possible to plot the natural logarithm of the emission time vs. the inverse local lattice temperature, Fig. 11b. This allows estimating the activation energy for the emission process, E_A, of the defect involved in the RTN by evaluating the slope of the linear fitting in Fig. 11b. The extracted value of E_A = 0.29 eV perfectly matches the value reported in [23] for defects in the SiO_2 E-B spacer, further confirming the validity of the proposed TCAD model and providing a verification for the location of the defects generated during stress. This also allows roughly estimating the relaxation energy of the defect as $E_{REL} = 4 \cdot E_A$ = 1.16 eV.

V. The Role of Self-Heating during Stress

As emphasized in Section III, besides being involved in the device SH, HCD is the mechanism that eventually determines the creation of defects at the E-B spacer and/or at its interface during stress, as confirmed by the RTN analysis in Section IV. The generation of such defects is associated with an increased recombination current component that results in the measured

I_B degradation shown in Fig. 12(a-b). The I_B degradation measured at different stages of cumulative stress is correctly reproduced in TCAD simulations by increasing the defect density at the E-B spacer interface in the range $10^{12} – 5 \cdot 10^{12}$ cm^{-2}, Fig. 12c, consistently with values previously reported in the literature [5]. This allows estimating the defect density increase over time during stress, Fig. 12d, that is well reproduced by a power-law (t^{γ}) with $\gamma = 0.5$, in agreement with results reported in the literature [5] for SiGe HBT devices stressed in both similar and different conditions. Moreover, for the stress time range used in this study, this value also agrees with the predictions of a new compact ageing model [14], which further validates the proposed TCAD model. However, at very long cumulative stress times (i.e. on the order of 1000 hours, depending on the stress condition) the degradation trend tends to change showing a reduction in γ, as reported in the literature [5, 14].

The model is now used to gain insights into this phenomenon, by analyzing the role of temperature during the stress and measurement phases that alternate during a typical stress experiment. It is indeed worth pointing out that while defect generation occurs during the stress phase (typically performed by biasing the device at larger voltages than the nominal ones), the effects of stress are typically evaluated by detecting changes in the forward Gummel curve, the latter being measured in much milder conditions, close to the nominal ones. As a result, investigating this phenomenon requires analyzing the possible change in the device behavior in both measurement and stress conditions considering different defect density values. In Fig. 13 we compare the results of simulations at medium (i.e., $5 \cdot 10^{12}$ cm^{-2}) and very high (i.e., 10^{14} cm^{-2}) defect density, both in stress and in measurement conditions. Notice that the two defect density values chosen for this analysis correspond to a cumulative stress time of few thousands of seconds (where no γ reduction is observed and corresponding to a medium defect density) and ~800 hours (where the γ reduction is typically detected and corresponding to a very high defect density) in the stress conditions used in this work. In stress conditions neither the lattice nor the carriers' temperature profiles show appreciable changes with defect density, which excludes that the observed reduction in γ could be caused by a change in the stress dynamics caused by alterations of the local temperature profile due to the very high defect density. Nevertheless, in measurement conditions, while the lattice temperature is unaffected by the defect density (as expected), the hole temperature profile shows a hot spot at the defects' location only when considering a high defect density, suggesting that hot holes could be involved in the observed γ reduction. The hot spot indicates a loss of trapped holes due to electron injection, which is accompanied by a reduction of interface traps [25], contributing to the slowdown of the degradation dynamics. Another mechanism that could be involved in the observed γ reduction is the saturation of the available Si-H bonds [14], which however deserves further investigation.

While the thorough investigation of this phenomenon requires a more comprehensive study, the results obtained in this paper demonstrate the effectiveness of the proposed model in exploring the reliability issues of SiGe HBT devices and the advantages deriving from the combination of dedicated noise [26] and stress experiments [5] with physics-based simulations [4-9].

VI. Conclusions

In this work, we explored the reliability issues of state-of-the-art SiGe HBT devices by combining dedicated stress and noise experiments with TCAD simulations. The proposed TCAD model, carefully calibrated on experimental data, was used to investigate the SH effects in both stress and measurement conditions by means of 2D thermal maps. Simulations in typical operating conditions show that the lattice temperature increase reaches at most 20 K, which can be further reduced by optimizing the substrate and emitter thermal resistance. The location of the defects generated during stress was experimentally determined by RTN measurements that reveal that, in the stress conditions used in this study, defects tend to form at the E-B spacer and/or its interface. Moreover, the results of mixed-mode stress experiments combined with TCAD simulations allowed estimating the defect generation rate, which was found in agreement with results in the literature. Simulations of the SH effects in stressed devices in stress conditions excluded annealing as the possible reason for the slowdown of the degradation dynamics reported in the literature at long stress times. On the other hand, simulations of a strongly stressed device (with a very high defect density at the E-B spacer interface) in measurement conditions revealed the presence of a hole hot spot possibly involved in the γ reduction observed at very long stress times.

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