Published in: IEEE Transactions on Microwave Theory and Techniques (Vol. 67, no. 9, Sept. 2019)

Millimeter-Wave Noise Source Development on SiGe BiCMOS 55 nm Technology for Applications up to 260 GHz

João Carlos Azevedo Gonçalves[1], Haitham Ghanem[2], Simon Bouvot[1], Daniel Gloria[1], Sylvie Lépilliet[2], Guillaume Ducournau[2], Christophe Gaquière[2] and François Danneville[2]

***Abstract*— This paper describes the development and characterization of a millimeter-wave (mmW) integrated noise source development on silicon technology for applications up to 260 GHz. The developed integrated noise source is based on PN and Schottky junction in series, realized on the SiGe BiCMOS 55 nm technology from STMicroelectronics. Biased in the avalanche regime This integrated diode noise source achieves a tunable Excess Noise Ratio (ENR) ranged between 0 dB and 15 dB mA, in the 130 GHz to 260 GHz frequency range. In order to highlight the usefulness of the integrated noise source, the noise figure of two amplifiers was measured: the first one, is an integrated low noise amplifier (LNA) operating in D-band (130 GHz – 170 GHz) while the second one is packaged and operates from 220 GHz to 260 GHz. Due to its ability to be naturally integrated on silicon, this noise source features a strong interest to carry out high frequency in-situ noise characterization of advanced Si CMOS or BiCMOS technologies in the mmW range.**

***Index Terms*—Integrated noise source, in-situ noise characterization, millimeter-wave.**

I. Introduction

NOWADAYS, advances in the industry of micro and nano technologies lead to the possibility of manufacturing high data rate communication systems with large operational bandwidth. In the meantime, a strong interest to integrate such systems has emerged over the past years. The operating frequency of transistors in circuits has increased due to their outstanding maximum oscillation frequency (f_{max}), now higher than 370 GHz [1]-[2]. This allows the design of systems having high bandwidth and thus able to address applications with better performance such as high resolution in the context of imaging and radar systems, and high data rate wireless communications. The design of such complex systems requires accurate and reliable electrical models of active devices like MOS or bipolar transistors. These linear/nonlinear models are extracted and validated through high frequency (HF) measurements, performed when the device operates under small or large signal conditions. HF noise characterizations are obviously required to extract the device noise model.

Usually, these models are based on measurements below 110 GHz and are extrapolated beyond. Thus, HF measurement above 110 GHz are of utmost importance for the validation of such models used to design circuit in the millimeter-wave (mmW) frequency range and to extract the performance of these circuits. In this context, when noise characterization is performed for frequencies higher than 110 GHz, several critical points have to be taken into account.

First, the maximum reflection coefficient (Γ_S) provided by the impedance tuner should surround the noise optimal source reflection coefficient impedance (Γ_{opt}) of the transistor, allowing an extraction of its four noise parameters by the resolution of Lan algorithm. Beyond 75 GHz, a commercial external impedance tuner is available, but the waveguide and the HF probe allowing to connect the external tuner to the on-wafer device under test (DUT) feature important losses, which significantly limits the maximum reflection coefficient value. This constraint motivated the development of in-situ tuners in the B9MW, B5T and B55 SiGe STMicroelectronics technology, integrated closer to the DUT. In W-band [3], an active impedance tuner was used to extract the noise parameters of a heterojunction bipolar transistor (HBT) using Y-factor measurement. In D-band, investigations were done using passive impedance tuners [4], [5] and the cold method [6]. An active tuner designed in the BiCMOS 55 nm technology was also developed to increase measurement accuracy [7].

The second critical point for HF noise characterization above 110 GHz concerns the minimum detectable signal (MDS) condition, related to the noise figure of the noise receiver (RCV), adding a margin of 3 dB. As a result, there is enough sensitivity when the noise power injected at the input of the RCV is greater than the MDS level. The noise performance of the receiver is directly limited by the commercial availability of its constituent elements, including HF isolator and down frequency mixer. In this paper, two receivers were used; the first

Manuscript received August 20, 2018; revised November 12, 2018 and January 14, 2019; accepted February 11, 2019.

This work was supported by ECSEL TARANTO project toward advanced BiCMOS nanotechnology platforms for RF and THz application and EURAMET ADVENT project "16ENG06 advanced: Metrology for advanced energy-saving technology in next generation electronics applications"

João Carlos Azevedo Gonçalves (e-mail: joao.azevedogoncalves1@st.com), Simon Bouvot and Daniel Gloria are with STMicroelectronics, Crolles 38926.

Haitham Ghanem, Sylvie Lépilliet, Guillaume Ducournau, Christophe Gaquière and François Danneville are with IEMN laboratory, villeneuve d'ascq, 59650.

one operates in the 130 GHz - 170 GHz frequency range. While the second one, recently developed, addresses the 170 GHz to 260 GHz frequency range. These receivers feature a noise figure around 8 and 11 dB, respectively.

The last critical point is the non-availability of a commercial noise source above 220 GHz. HF noise source with an adequate output noise power level is thus required to perform such characterization. III-V Schottky diodes [8] and uni-travelling carrier photodiodes (UTC-PD) [9] have already been used as noise sources to carry out reliable characterizations in the mmW range, but these devices are not compatible with silicon integration processes. Other works have been carried out on silicon integrated noise source in centimeter wave range [10]-[11]; the related applications for these works were radiometer integrated on system-on-chip (SoC) and built-in self-test (BIST). In order to overcome this constraint, an original test structure based on an integrated diode noise source using the STMicroelectronics BiCMOS 55 nm technology has been developed, which constitutes the main motivation of this work.

The BiCMOS 55 nm diode based integrated noise test structure is presented in the next section. Then, the noise characterization of the noise receivers used for noise measurement up to 260 GHz is presented in section III. The on-wafer excess noise ratio extraction is presented and discussed in section IV. And finally, the use of developed integrated noise source is validated by the integrated low noise amplifier (LNA) characterization in D-band and packaged amplifier characterization in 220 GHz to 260 GHz frequency range, in section V and VI, respectively.

II. Integrated Noise Source

Two points strongly motivated the on-wafer noise source design. Firstly, as earlier stated, the unavailability of commercial solid-state noise sources above 220 GHz, and secondly the measurement and extraction accuracy. Consequently, in the case of on-wafer noise characterization, on-wafer noise sources offer real advantage over external solid-state noise sources: their effective ENR is directly known in the on-wafer device input plane, therefore, noise de-embedding of elements between the bench-top noise source and the on-wafer device input is not necessary thus subsequent inaccuracies are avoided [12]. Literature relates several on-wafer noise source solutions using an IMPATT diode [13] or a Schottky diode [8]. Such solid-state noise sources generate high noise power levels when operating in their avalanche regime (biased at their breakdown voltage) [14]. Thus, an integrated silicon diode provides a convenient solution to HF noise generation.

A. Integrated Diode on BiCMOS 55 nm Technology

A cross-section of the diode used as an integrated noise source is shown in Fig. 1. The device is a PN junction diode in series with a Schottky contact on the anode side. This Schottky contact is formed by silicidation (Co-Si) of exposed silicon (P-type) surface between the two shallow trench isolation (STI) regions. The PN junction is formed between a P-type silicon region and high doped N type silicon region (Nsinker and N+). This high doping access allows a low-resistance link to the cathode from the silicide contact on the silicon surface. The STI prevents electrical shorts between cathode and anode contacts, and a deep trench isolation provides perimeter isolation from the substrate and between the devices. A P-type ground guard ring (P+ plug) is surrounding the device in order to delimitate the substrate area.

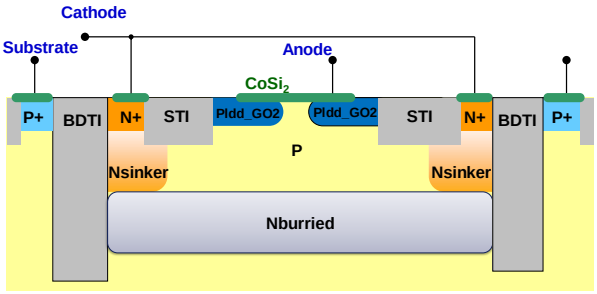

Fig. 1. Cross section Layout of the diode.

A top view of the diode layout is shown in Fig. 2. The diode design is performed by interdigitated cathode and anode fingers. The used diode (L10 N2) is composed of two anode fingers and three cathode fingers, the length and width of each finger are 9 µm and 0.38 µm, respectively.

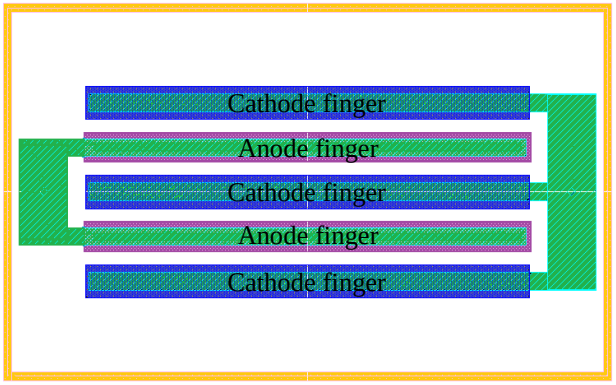

Fig. 2. Top view of the diode layout.

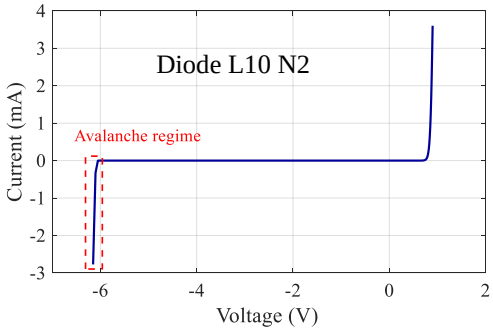

Fig. 3 I-V characteristic of the used diode.

Due to its low junction capacitance, this diode can be used as a HF noise source when it is reverse biased in avalanche regime. The noise generated by the diode has the form of a white noise signal covering a wide frequency bandwidth. The diode is reverse biased using a DC current source and the corresponding voltage is checked. The I-V curve in Fig. 3 shows the reverse voltage with an avalanche region close to -6 V.

III. Millimeter Wave Noise Receiver

A. *Noise Receiver Topology*

The noise receiver is an important block in a HF noise measurement system. The typical block diagram of a noise receiver structure is depicted in Fig. 4. The receiver is used as a frequency down converter from a high frequency band (RF) to an intermediate (IF) frequency band, corresponding to the input frequency range of the noise figure meter (NFM), between 10 MHz and 1.6 GHz. The down converted noise power is measured by a HP 8970 NFM. Usually the RCV performs a double sideband (DSB) down conversion. Thus, the upper and lower side band (USB and LSB) are converted to the same intermediate frequency.

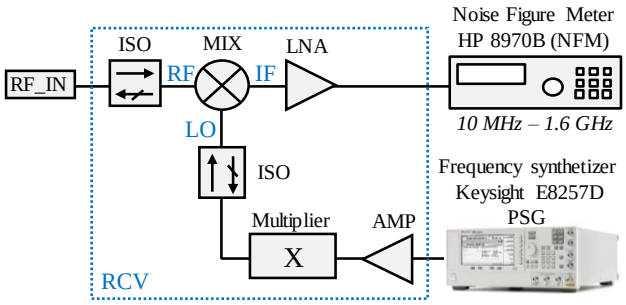

Fig. 4. Typical block diagram of a noise receiver structure.

The noise receiver consists of a sub-harmonic mixer (SHM) used as a down converter. The local oscillator (LO) chain drives the conversion at half of the RF frequency and is composed of an amplifier followed by a frequency multiplier to increase the frequency up to the LO frequency range and an isolator to match the LO port and maintain its performances. The input of the RF mixer is isolated from the previous stage using an isolator, which is important to minimize any reflected signal from flowing back to the circuit, therefore enhancing the impedance matching between the mixer and the previous stage. The IF output signal is followed by an LNA to mask losses between IF output and the NFM input and suppress the noise contribution of the NFM. The manual of the NFM specifies the measurement bandwidth as 4 MHz around the NFM operating frequency.

In this study, the noise measurements were carried out over a 130 GHz bandwidth (130 GHz to 260 GHz), which justifies the use of two noise receivers. Fig. 5 shows photographs of the two receivers used for the noise measurements. Frequency properties of both receivers are reported in Table I.

TABLE I
Frequency Properties of the Noise Receivers

Receiver	F_{RF} (GHz)	F_{LO} (GHz)	F_{IF} (GHz)	F_{PSG} (GHz)	LO multiplier chain factor
WR06	130-170	65-85	0.03	32.5-42.5	2
WR04	170-260	85-130	1	28.3-43.3	3

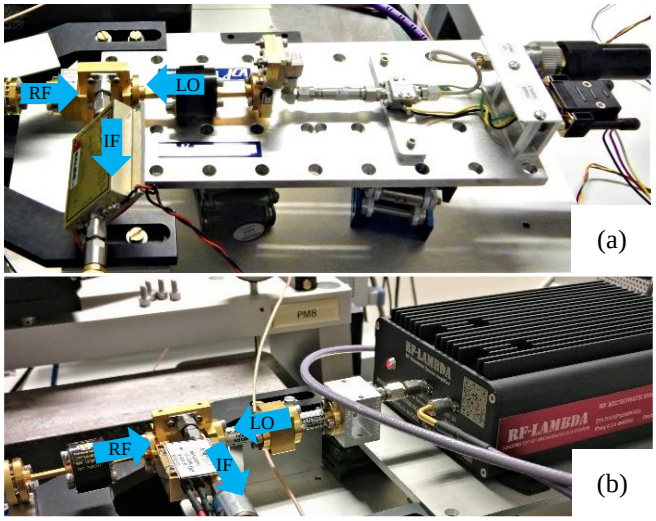

Fig. 5. Photographs of noise receiver structures in (a) D-band (130 GHz to 170 GHz), and (b) WR04 (170 GHz to 260 GHz) frequency ranges.

B. *"Hot/Cold" Noise Calibration*

As stated earlier, the MDS condition is directly related to the noise figure of the receiver (NF_{RCV}). In order to calibrate the noise receiver, measurements were carried out using the hot/cold method. To our best knowledge, there are no commercially available active noise sources above 220 GHz. Fig. 6 shows the block diagram of the setup used in order to perform the hot/cold noise measurement method.

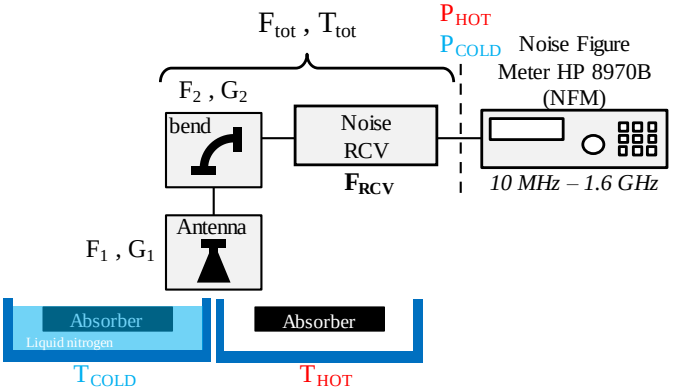

Fig. 6. Block diagram of the setup used in order to perform the hot/cold measurement method.

The measurement procedure is carried out using the NFM, measuring the (down-converted) noise power at the noise receiver output, and is composed of two steps: first, the measurement of the hot noise power (P_{HOT}) and second, the measurement of the cold noise power (P_{COLD}). The noise power P_{HOT} and P_{COLD} (in NFM planes, see Fig. 3) are measured using an absorber in front of a horn antenna successively held at two physical temperatures, T_{HOT} and T_{COLD}, respectively. In our case, T_{COLD} corresponds to the physical temperature of the absorber when held at 77 K using liquid nitrogen, and T_{HOT} corresponds to the physical temperature of the absorber at ambient temperature. For all measurement configurations, the temperature of the absorber is measured using a thermo-resistor.

First, the equivalent noise temperature (T_{tot}) and the noise factor (F_{tot}) for all elements between the noise source and the NFM are extracted using the Y-factor method (1-3). The Y-factor is determined as the ratio of the two measured noise powers (P_{HOT} and P_{COLD}) using (1). After F_{tot} calculation using (2) and (3) the F_{RCV} is determined, knowing the noise factors ($F_1$and F_2) and gains ($G_1$and G_2) of each passive device located between the source and the NFM. The noise factor of the receiver is extracted using FRIIS formula expressed by (4).

$$Y = \frac{P_{HOT}}{P_{COLD}} \tag{1}$$

$$T_{tot} = \frac{T_{HOT} - Y.T_{COLD}}{Y - 1} \tag{2}$$

$$F_{tot} = 1 + \frac{T_{tot}}{T_{\emptyset}} \tag{3}$$

$$F_{RCV} = \left(F_{tot} - F_1 - \frac{F_2 - 1}{G_1}\right).G_1.G_2 + 1 \tag{4}$$

C. Receiver Noise Figure Extraction

The noise calibration procedure was applied to the two noise receivers (WR06 & WR04).

WR04-band receiver has been recently developed to address noise measurement above 170 GHz. Before measurement, the noise figure has been estimated, based on the block diagram of Fig.4. Using the data provided in the datasheets, the noise figure of the receiver can be calculated, using FRIIS formula, expressed by (5).

$$F_{RCV} = F_{ISO} + \frac{F_{MIX} - 1}{G_{ISO}} + \frac{F_{LNA} - 1}{G_{ISO}.G_{MIX}} \tag{5}$$

Where F_{ISO}, F_{MIX} and F_{LNA} are the noise factors of the RF-isolator, mixer and LNA, respectively. G_{ISO} is the gain of the RF-isolator and G_{MIX} is the conversion gain of the mixer.

Fig. 7 shows the extracted noise figure of the WR06 receiver between 130 GHz and 170 GHz, featuring around 8 dB up to 165 GHz. The extracted noise figure of the WR04 receiver is compared to the calculated value in Fig. 8, between 170 GHz and 260 GHz. The extracted results are close to the calculated values. In the NFM datasheet, the measured noise power accuracy is specified as 0.02 dB. Thus, the noise figure uncertainty for both receivers was evaluated using this value. Error-bars were extracted and plotted on the extracted noise figure of the receiver. This uncertainty is more important for high values of the noise figure, corresponding to the lowest measured power values. The power measurements at the output of the LO chain suffered lack of sufficient pumping power to drive the mixer at some frequency points, which is due to the response of the frequency tripler, for these particular frequencies. It induced the impossibility to use these points in the measurements, unless to exceed the maximum input power allowed to drive the amplifier.

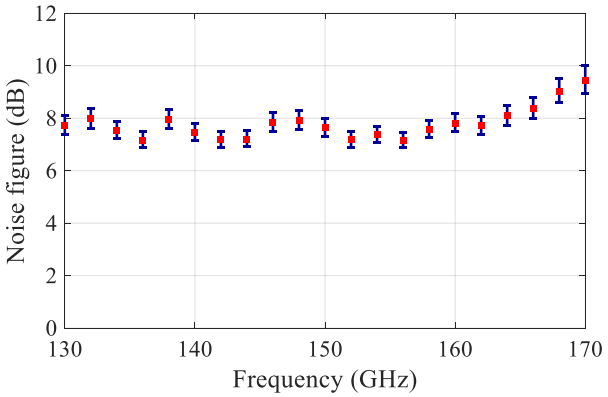

Fig. 7. Measured noise figure of the receiver WR06 on 130 GHz to 170 GHz frequency range.

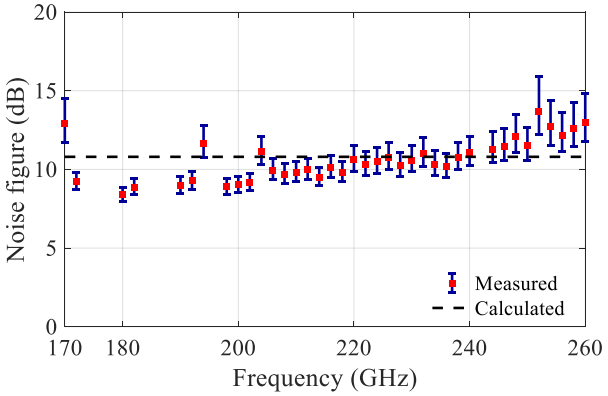

Fig. 8. Measured and calculated noise figure of the receiver WR04 on 170 GHz to 260 GHz frequency range.

IV. On-wafer Excess Noise Ratio Extraction Methodology

A. Methodology

The diode noise source is often specified in terms of effective noise temperature leading to an effective Excess Noise Ratio (ENR_{eff}) [15]–[17] corresponding to the delivered power specified load. However, it is more convenient to extract the available Excess Noise Ratio (ENR_{av}), and then choose whether to calculate the effective value or not. We assume the following equalities, T_{COLD} = T_A = $T_{\emptyset}$ = 290 K, where T_{COLD} is the noise source temperature in the OFF state, T_A is the physical ambient temperature and $T_{\emptyset}$ as a standard temperature. Fig. 9 shows the block diagram of the setup used to perform on- and off-wafer ENR extractions. The test structure characterized in this part is a diode with its anode shunted to ground and its cathode connected to a RF-pad. In this test configuration the diode was biased through the bias tee of the RF probe by a positive current for the ON state and un-biased for the OFF state. The available noise temperature at the on-wafer reference plane A may be obtained with the calibrated noise receiver previously defined. In our case, the diode is unmatched. Thus, the available gain cannot be directly used, and the mismatch factor (M) defined by (6) is used to determine the available values. The noise power is expressed by (7). To reduce the transformations between noise power and noise temperature,

we will combine the mismatch factor and gain with the noise temperature calculation.

$$M = \frac{1 - \left|\Gamma_{OUT}^{probe} . \Gamma_{IN}^{RCV}\right|^2}{\left(1 - \left|\Gamma_{OUT}^{probe}\right|^2\right).(1 - |\Gamma_{IN}^{RCV}|^2)} \quad (6)$$

$$P = k.T_{noise}.\Delta f \quad (7)$$

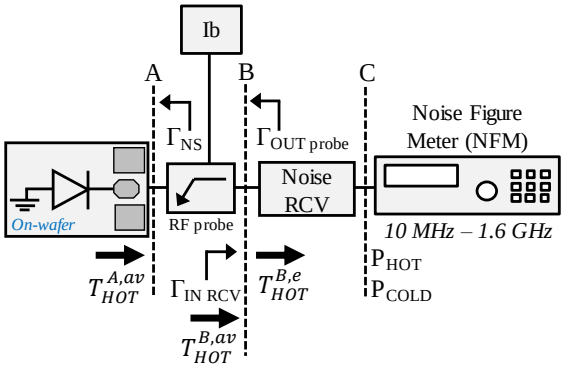

Fig. 9. Block diagram of the setup used to perform the Excess Noise Ratio extraction at on-wafer plane (A) and off-wafer plane (B).

The ENR was extracted using the Y-factor method. Where P_{HOT} correspond to the ON state, when the diode is biased in its avalanche regime and P_{COLD} correspond to the OFF state when the diode is un-biased.

The extraction of the ENR can be decomposed in four steps.

First, the effective hot noise temperature ($T_{HOT}^{B,e}$) is determined at the waveguide plane B using (8) and the Y-factor measurement.

$$T_{HOT}^{B,e} = T_{RCV}.(Y - 1) + Y.\frac{T_{COLD}}{M} \quad (8)$$

Secondly, the available hot noise temperature is determined by the use of the mismatch factor at plane B by the use of (9).

$$T_{HOT}^{B,av} = T_{HOT}^{B,e}.M \quad (9)$$

The third step corresponds to the transposition of the hot noise temperature at plane B to the plane A. Knowing the available gain of the probe, the hot noise temperature at plane B may be transferred to the available hot noise temperature $T_{HOT}^{A,av}$ at the on-wafer plane A by the use of (10)

$$T_{HOT}^{A,av} = \frac{T_{HOT}^{B,av} - T_A\left(1 - G_{probe}^{av}\right)}{G_{probe}^{av}} \quad (10)$$

Where G_{probe}^{av} is the available gain of the probe defined by (11). The calculation of the mismatch factor and the available gain are possible knowing the S-parameters of the probe, the reflection coefficient of the noise receiver Γ_{IN}^{RCV} and the reflection coefficient of the diode noise source ($\Gamma_{NS(i)}$) for each bias current condition.

$$G_{probe}^{av} = \left|S_{21}^{probe}\right|^2 \frac{\left(1 - \left|\Gamma_{NS(i)}\right|^2\right)}{\left|1 - S_{11}^{probe}\Gamma_{NS(i)}\right|^2.\left(1 - \left|\Gamma_{OUT}^{probe}\right|^2\right)} \quad (11)$$

Finally, the available excess noise ratio at plane A ($ENR_{A,av}$) can be determined by the use of (12).

$$ENR_{A,av} = \frac{T_{HOT}^{A,av} - T_{COLD}}{T_{\emptyset}} \quad (12)$$

The measured S parameters of the test structure in G (130 GHz – 220 GHz) and J (220 GHz – 320 GHz) band for OFF and ON (7 mA) states are shown on Fig. 10. A change in the reflection coefficient phase is obviously observed between ON and OFF states. Nevertheless, the change in the magnitude of the reflection coefficient is limited to 6%; as a result, it does (almost) not impact the extraction.

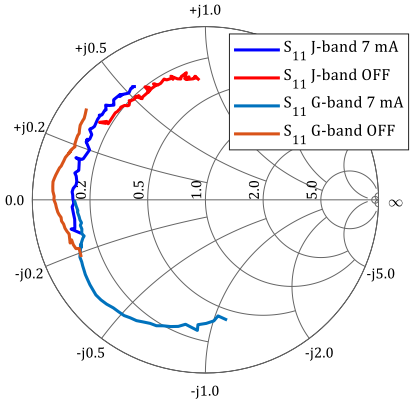

Fig. 10 Measured S parameters of the test structure on contact pad plane on G (130 GHz – 220 GHz) and J (220 GHz – 320 GHz) bands for OFF state and 7 mA of bias current condition.

B. *On-Wafer Excess Noise Ratio extraction*

The extracted $ENR_{A,av}$ of the diode noise source versus frequency is shown on Fig. 11. We notice that the level of ENR varies according to the reversed biasing current of the diode source. The diode features an ENR varying from 5 dB to 20 dB in the D-band and from 0 dB to 15 dB in the 200 GHz-260 GHz frequency range. Between 170 GHz and 200 GHz, the ENR value constantly decreases for all bias currents. This ENR shape was reported in the literature [12]-[18] and corresponds to the diode avalanche noise model.

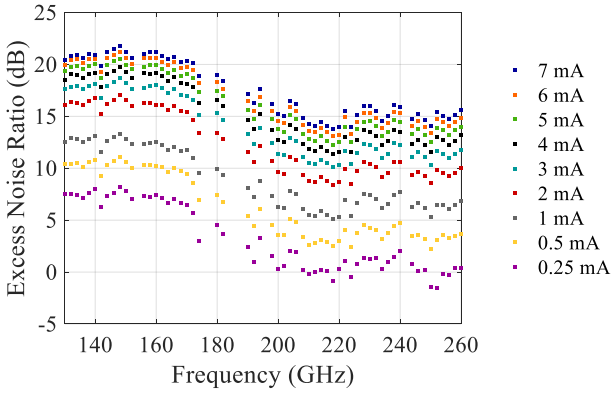

Fig. 11. Available Excess Noise Ratio extracted at on-wafer plane A.

As for the noise receiver calibration, the ENR has been extracted considering 0.02 dB of accuracy on the measured noise power (P_{HOT} and P_{COLD}) by the NFM. The error bars have been plotted in Fig. 12 (for one test structure), featuring the impact of the NFM measurement accuracy on ENR extraction. Moreover, in order to investigate the repeatability of the noise source characteristic, the ENR curves of six different test structures (same diodes located at different places on the wafer) are plotted in Fig. 12.

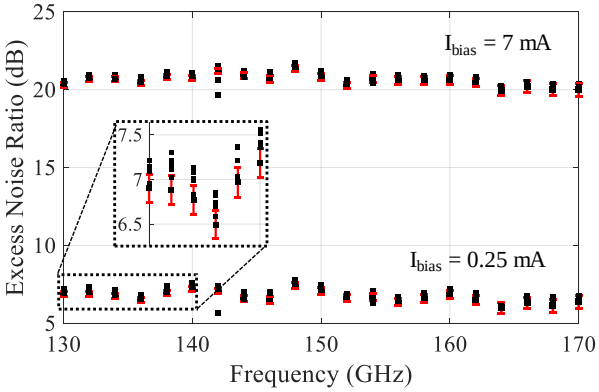

Fig. 12. Available Excess Noise Ratio extracted at on-wafer plane A, on six different reticules and corresponding error bars considering 0.02 dB of accuracy on the noise power measured by the NFM.

The error bars show that the NFM power measurement accuracy does not have critical impact on the ENR extraction. Moreover, the ENR extracted for the six test structures shows a very good repeatability with a variation lower than 0.5 dB (in the same range values that those of the error bars).

V. Integrated Low Noise Amplifier Characterization

A. *Integrated Noise Source Based Extraction*

The LNA is a key device in mmW frequency range for datacom, detection and characterization. For these purposes and in order to validate the use of an integrated noise source for in-situ noise characterization, we took benefit of a LNA available on BiCMOS 55 nm [7] as well as our developed diode noise source. For the in-situ noise characterization, the diode noise source is directly connected on-wafer to the input of the amplifier, as shown on Fig. 13.

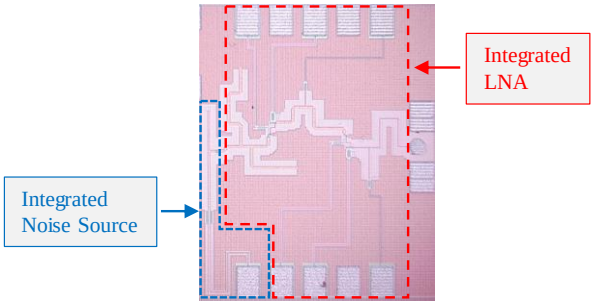

Fig. 13. Chip photograph of the BiCMOS 55 nm test structure, composed of the integrated noise source and the LNA.

In this configuration, the noise source cannot be biased through the bias tee of the RF probe. Thus, an integrated bias tee was designed on the cathode side. The diode noise source was biased in its avalanche regime through the integrated bias tee and the dc-pad on the lower side by a dc-probe. To perform on-wafer noise characterization with an integrated noise source, two test structures are needed.

The first structure is composed of the noise source for the extraction of its ENR using the setup shown in Fig. 14(a).

The second structure is composed of the noise source directly connected to the input of the device for noise characterization of the device using the setup shown in Fig. 14(b).

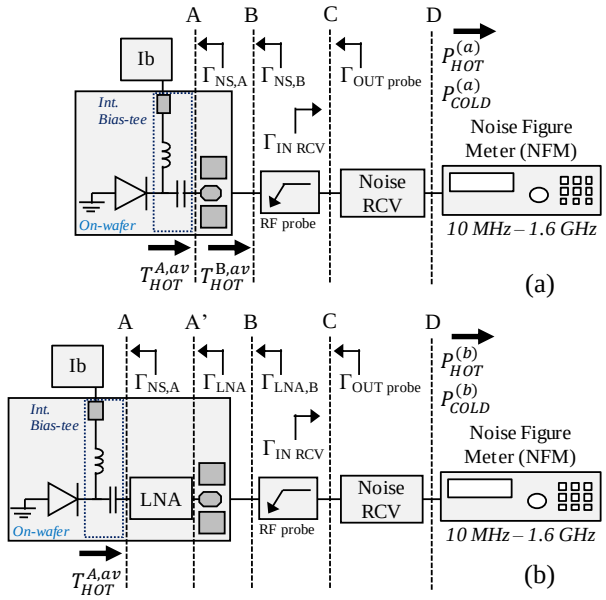

Fig. 14. Block diagrams of on- and off-wafer setup configurations used to perform on-wafer noise figure extraction of an LNA by the use of an integrated noise source. (a) Standalone noise source for ENR extraction on plane A, (b) noise source and LNA for noise characterization of the LNA.

The proposed two cascode stages LNA is designed in order to keep the lowest noise figure while presenting 50 Ω at its input in the whole D-band, using a double-stub matching network. For integration purposes, the output single-stub allows the singled-ended LNA to be 50 Ω matched. This circuit uses active and passive components provided by the Design Kit of the technology, such NPN transistors (HiCUM level 2 model), microstrip lines, MIM capacitors and resistors. The four bipolar transistors used are high speed NPN with 1 emitter of 5.56 µm of length and 0.2 µm of width. The dedicated electrical schematic is fully presented in [7]. The LNA was characterized within its operating frequency range (130 GHz -170 GHz). The aim of this characterization is the extraction of its noise figure by the use of the integrated noise source. First, the Excess Noise Ratio was extracted at plane A. The available hot noise temperature $T_{HOT}^{B,av}$ was extracted at plane B as explained previously. Using the same methodology, it can be transferred to the available hot noise temperature $T_{HOT}^{A,av}$ at plane A by the use of (13-14).

$$T_{HOT}^{A,av} = \frac{T_{HOT}^{B,av} - T_A.\left(1 - G_{av}^{pad}\right)}{G_{pad}^{av}} \quad (13)$$

$$G_{av}^{pad} = \left|S_{21}^{pad}\right|^2 \cdot \frac{\left(1-\left|\Gamma_{NS,A}\right|^2\right)}{\left(1-S_{11}^{pad}\Gamma_{NS,A}\right)^2 \cdot \left(1-\left|\Gamma_{NS,B}\right|^2\right)} \quad (14)$$

The S-parameters of the pad are obtained by the simulation of its SPICE electrical model extracted from S parameters measurement of PAD-OPEN test structure up to 320 GHz, the gamma presented at plane B ($\Gamma_{NS,B}$) is deducted from the S-parameters measurement of the diode and at plane A ($\Gamma_{NS,A}$) it is deducted by pad de-embedding. The measured S parameters of the test structure on D band for OFF state and variable bias current condition are shown on Fig. 15.

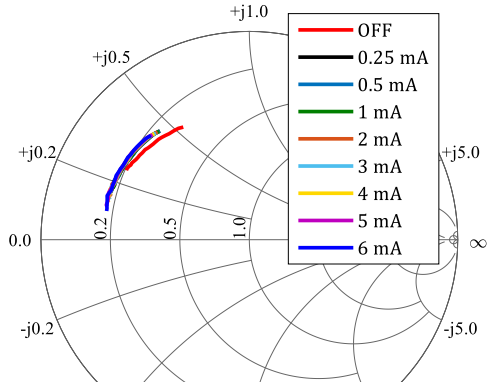

Fig. 15 Measured S parameters of the test structure on D band for OFF state and variable bias current condition between 0.25 mA and 6 mA.

The noise figure of the LNA (NF_{LNA}) has been simulated by taking into account the impedance presented by the noise source ($\Gamma_{NS,A}$). It is assumed that, for the simulated noise figure, the available noise temperature of the noise source is used at the input, and 50 Ω is presented at the output (reflected the LNA output impedance, matched to 50 Ω). Thus, for the extraction, we use the available noise temperature ($T_{HOT}^{A,av}$) previously extracted. Knowing the available noise temperature of the noise source, the noise figure extraction of the integrated LNA can be processed as follow (15-16).

First the total equivalent noise temperature of cascaded two-port networks between noise source (plane A, Fig. 14, b) and NFM (plane D, Fig. 14, b) can be extracted using (2) and then it can be converted to the total noise factor using (3), where the Y-factor is calculated as previously (1) and the available hot noise temperature is defined on plane A.

Finally, the extraction of the noise factor of the integrated LNA (F_{LNA}) is done using FRIIS formula, by the use of (15). All mismatches were taken into account (reflection coefficients in plans A/A'/B/C).

The LNA gain (G_{LNA}) used here is extracted using (16) and is defined as the ratio between the ON-OFF noise power difference with LNA (Fig. 14,b) and the ON-OFF noise power difference without LNA (Fig. 14,a).

$$F_{LNA} = F_{tot} - \frac{F_{pad}-1}{G_{LNA}} - \frac{F_{probe}-1}{G_{LNA}.G_{av}^{pad}} - \frac{F_{RCV}-1}{G_{LNA}.G_{av}^{pad}.G_{av}^{probe}} \quad (15)$$

$$G_{LNA} = \frac{P_{HOT}^{(b)} - P_{COLD}^{(b)}}{P_{HOT}^{(a)} - P_{COLD}^{(a)}} \quad (16)$$

Fig. 16 shows the noise figure of the LNA, extracted for variable noise source bias currents, in comparison with the simulation data (solid line). The extracted noise figure is close to the simulated one, mainly for diode noise source bias currents ranged between 2 and 7 mA. However, below 2 mA the result of extraction is shifting from the SPICE simulation. This is due to the insufficient noise power supplied by the noise source to the amplifier leading to insufficient noise power at the NFM input plane and values of the Y-factor tends to the critical "1" value (for low bias currents of the diode noise source, as we can see on Table II at 170 GHz).

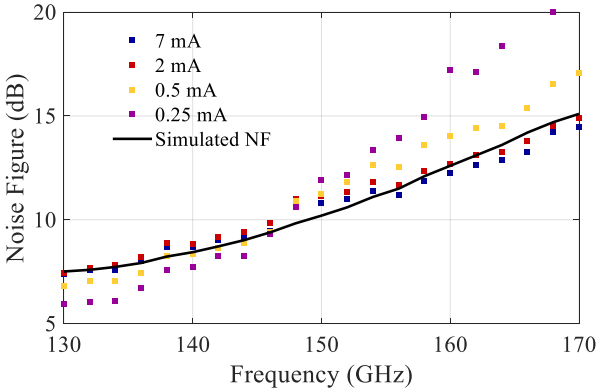

Fig. 16. Noise figure of the integrated low noise amplifier, extracted for variable diode noise source bias currents and simulated on noise source impedance.

TABLE II
MEASURED Y-FACTOR VALUES AT 170 GHZ

I_{bias} (mA)	0.25	0.5	1	2	3	4	5	6	7
Y	1.00	1.02	1.05	1.11	1.19	1.26	1.34	1.43	1.52

Fig. 17 shows the gain of the integrated LNA extracted from measured S parameters (solid line) and from noise measurement (dashed line). A discrepancy between extracted values from S parameters and noise measurement is observed, supposed due to the complexity of the pad de-embedding procedure on S parameters measurements.

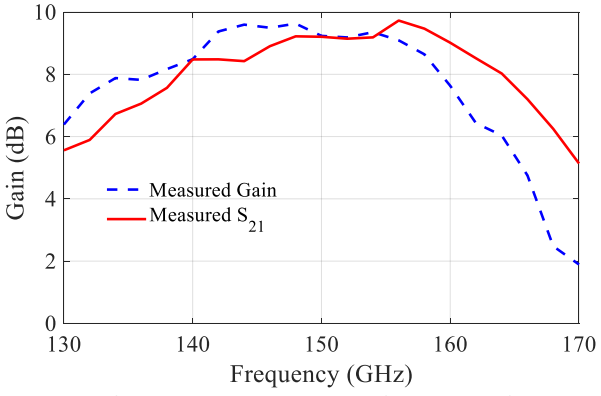

Fig. 17. Gain of the integrated low noise amplifier, extracted from measured S parameters and form noise measurement.

B. *Solid-State Noise Source Based Extraction*

In order to extract the noise figure of the integrated LNA on 50 Ohms (NF_{LNA}^{50}), it was characterized using the solid-state noise source (ELVA-1). It also allowed to validate the noise figure extraction, using integrated and solid-state noise sources. It is important to note that, due to the different reflection coefficients presented by solid-state and integrated noise source, it leads to different noise figure values.

Fig. 18 shows the block diagram of the setup used to perform the noise characterization of the integrated LNA using solid-state noise source.

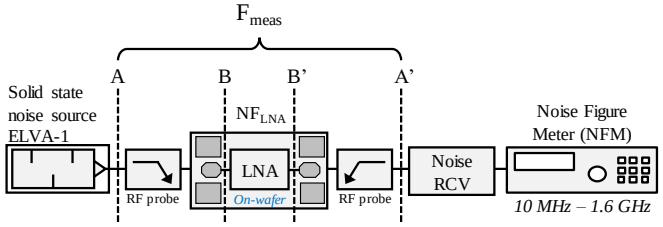

Fig. 18 Block diagram of the setup used to perform the noise characterization of the integrated LNA using solid-state noise source.

In this configuration, the RF-probe on the left side is used to connect the noise source to the LNA through the RF-pad. A noise calibration is performed by the connection of the noise source to the noise receiver. In this case the measured noise factor (F_{meas}) corresponds to the noise factor of all devices placed between plane A and A' (Fig. 18). Finally, the noise factor of the integrated LNA (F_{LNA}^{50}) is calculated using FRIIS formula, by the use of (17).

$$F_{LNA}^{50} = \left(F_{meas} - F_{probeL} - \frac{F_{pad}-1}{G_{av}^{probe,L}} - \frac{F_{pad}-1}{G_{av}^{probe,L} G_{av}^{pad} G_{LNA}} - \frac{F_{probe,R}-1}{G_{av}^{probe,L} \left(G_{av}^{pad}\right)^2 G_{LNA}} \right) G_{av}^{probe,L} G_{av}^{pad} + 1 \quad (17)$$

Fig. 19 shows the noise figure of the LNA, extracted from noise measurement, simulated on 50 Ohms and simulated with the reflection coefficient presented by the probe (Γ_{probe}) through the RF-pad.

Even if the noise source is well matched, the probe does not present 50 Ohms at contact pad plane. That induces alteration of the extracted noise figure, as we can see on Fig. 19. However, the extracted noise figure is close to the simulated one up to 150 GHz. Beyond this frequency, a discrepancy is observed between simulation and measurement, with several reasons that may explain this difference; (i) the noise source is placed far away from the device to be characterized, inducing a reduction of the ENR value at the input of the LNA, (ii) the noise de-embedding procedure to translate the measured noise figure (between planes [AA']) to the device noise figure (between planes [BB']) is directly related to the LNA contribution, which appears only as the third term in FRIIS formula.

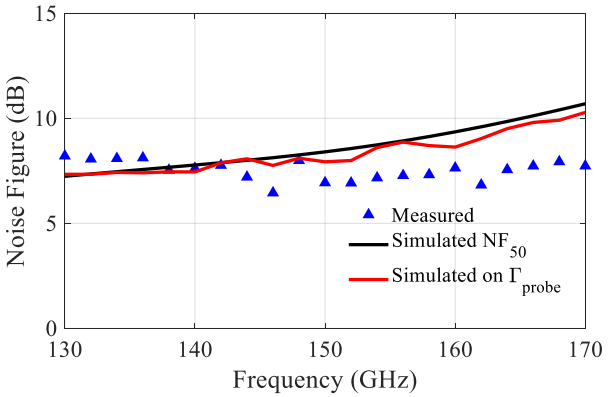

Fig. 19. Noise figure of the integrated low noise amplifier, extracted from noise measurement, simulated on 50 Ohms (black line) and simulated on reflection coefficient presented by the probe (Γ_{probe}) through the RF-pad (red line).

VI. Packaged Amplifier Characterization

In order to validate the use of the developed noise source above 170 GHz, a packaged amplifier was chosen to perform the noise characterization on 220 GHz to 260 GHz frequency range. Fig. 20 shows the setup used in order to perform the noise characterization of the packaged amplifier.

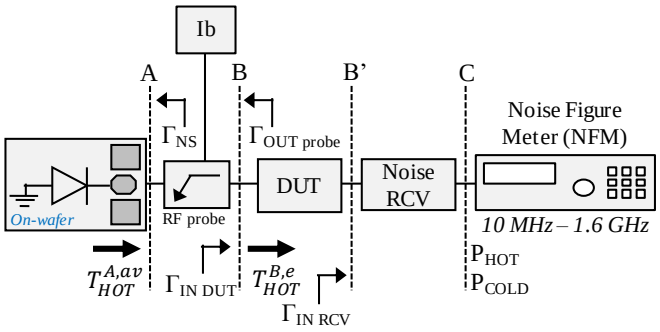

Fig. 20. Block diagram of the setup used to perform DUT noise characterization on waveguide flange.

For waveguide noise characterization, the DUT is placed between the RF probe waveguide flange and the input of the noise RCV. Based on the setup presented in Fig. 9, the noise source has been used in waveguide flange at plan B, through the RF probe. The diode is contacted by the RF probe and biased through the bias tee of the RF probe in its avalanche regime. The available hot noise temperature at plane B ($T_{HOT}^{B,av}$) previously extracted is directly used as ON state noise temperature of the noise source.

The device to characterize is a packaged amplifier with variable attenuators at the input and output planes, as we can see in Fig. 21.

The amplifier characterized in this section shows a poor matching, so the attenuators were used to improve the matching, despite it increases the noise figure of the device. The attenuation value was chosen by varying the position of the attenuator nob. Several configurations could be set regarding the attenuator values at the input and output of the amplifier. Table III shows the attenuation values for the three configurations used.

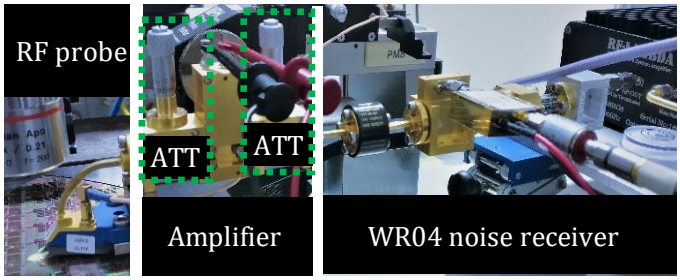

Fig. 21. Photograph of the setup used to extract the noise figure of the packaged amplifier.

TABLE III
INPUT AND OUTPUT ATTENUATION VALUES FUNCTION OF THE KNOB POSITION FOR THREE CONFIGURATIONS

Configuration	Input attenuator value (dB)	Output Attenuator value (dB)
1	7.9	9.5
2	0.8	9.5
3	0.8	0.5

Knowing the available hot noise temperature at plane B, the equivalent noise temperature between planes B and C could be extracted using the Y-factor method (1-3). Using the same methodology as before, the noise temperature T_{tot} and the noise figure F_{tot} were then extracted. Then, the extraction of the noise factor of the packaged amplifier was deducted using FRIIS formula (18). The gain of the amplifier was extracted using the same method as for the LNA.

$$F_{Amplifier} = F_{tot} - \frac{F_{RCV} - 1}{G_{Amplifier}} \tag{18}$$

The measurements and extractions were performed for variable bias current condition of the diode noise source, between 0.25 mA and 7 mA, as shown in Fig. 22 and Fig. 23. As for the LNA extraction (section 5.A), we notice that for biasing currents below 2 mA the extracted noise figure shifts from the extracted values done between 2 mA and 7 mA, this is due to the insufficient noise power supplied by the noise source to the amplifier. This can be seen in Fig. 11 where the ENR value for low biasing currents is very small in this frequency range, and it is further attenuated after the probe.

The extracted gain (deduced from noise measurements) is close to the measured S_{21} parameter, for the configuration 3.

The noise figure and gain of the amplifier has also been extracted for the three configurations, for a biasing current of the diode at 7 mA. The curves are shown in Fig. 24 and Fig. 25. The extracted noise figure of configuration 2 and 3 are close between 230 GHz and 260 GHz, which is due to the gain of the amplifier that masks the attenuation of the output attenuator. As for configuration 1, a signature of the input attenuator losses is clearly observable because the noise figure is increased by the difference of attenuation between configuration 1 and the other two configurations (7 dB) over the whole frequency range. As a matter of fact, the gain response of the amplifier changes as a function of the total attenuation between the different configurations.

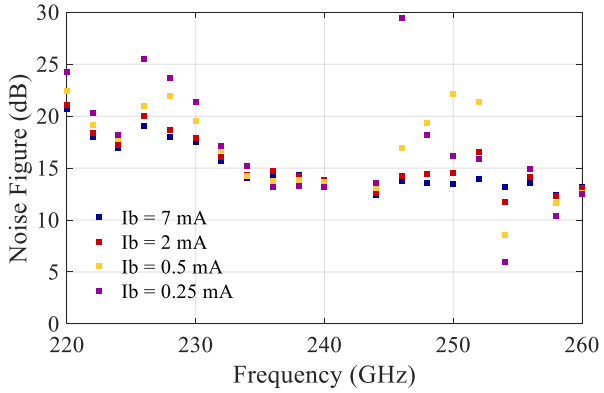

Fig. 22. Extracted noise figure of the packaged amplifier, extracted for variable biasing current of the diode noise source.

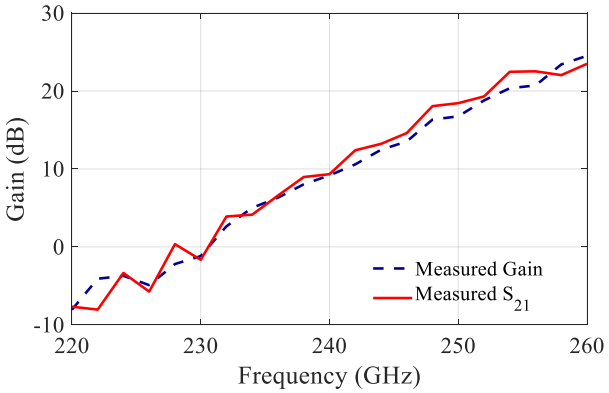

Fig. 23. Gain of the packaged amplifier, extracted from measured S parameters and form noise measurement.

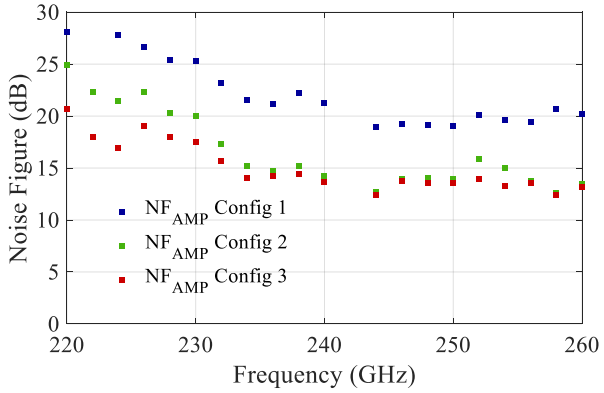

Fig. 24. Noise figure of the packaged amplifier, extracted from noise measurements for configurations (1), (2) and (3).

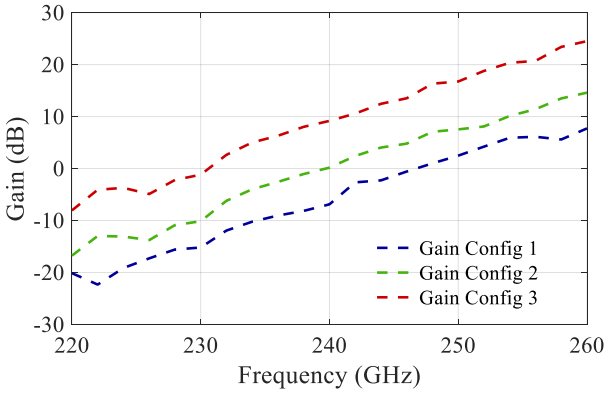

Fig. 25. Gain of the packaged amplifier, extracted from noise measurements for configurations (1), (2) and (3).

VII. Conclusion

mmW noise source development was presented in this paper. The developed noise source is based on an integrated diode structure operating in the avalanche regime and was characterized in the 130 GHz to 260 GHz frequency range. The presented test structure achieve a tunable ENR between 0 dB and 20 dB by bias current monitoring.

Such setup can be used to perform in-situ noise characterization measurements. The noise figure of active devices was extracted in two cases: (i) using the in-situ noise source integrated onto silicon with a LNA, operating in D Band frequency range, (ii) using the noise source along with packaged LNA, operating in 220 GHz - 260 GHz frequency range.

Further studies will be done in future to extract the four noise parameters of a heterojunction bipolar transistor using the diode structure as a noise source. Moreover, this noise source will be investigated in higher frequency range (>260 GHz) to perform in-situ noise measurements.

References

[1] P. Chevalier *et al.*, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proc. IEEE*, vol. 105, no. 6, pp. 1035–1050, Jun. 2017.

[2] M. Schröter *et al.*, "SiGe HBT Technology: Future Trends and TCAD-Based Roadmap," *Proc. IEEE*, vol. 105, no. 6, pp. 1068–1086, Jun. 2017.

[3] T. Quémerais, D. Gloria, S. Jan, N. Derrier, and P. Chevalier, "Millimeter-wave characterization of Si/SiGe HBTs noise parameters featuring fT/fMAX of 310/400 GHz," in *2012 IEEE Radio Frequency Integrated Circuits Symposium*, 2012, pp. 351–354.

[4] K. H. K. Yau, P. Chevalier, A. Chantre, and S. P. Voinigescu, "Characterization of the Noise Parameters of SiGe HBTs in the 70 #x2013;170-GHz Range," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 8, pp. 1983–2000, Aug. 2011.

[5] M. Deng *et al.*, "Millimeter-Wave In Situ Tuner: An Efficient Solution to Extract the Noise Parameters of SiGe HBTs in the Whole 130 #x2013;170 GHz Range," *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, no. 9, pp. 649–651, Sep. 2014.

[6] V. Adamian and A. Uhlir, "A Novel Procedure for Receiver Noise Characterization," *IEEE Trans. Instrum. Meas.*, vol. 22, no. 2, pp. 181–182, Jun. 1973.

[7] S. Bouvot *et al.*, "A 140 GHz to 160 GHz active impedance tuner for in-situ noise characterization in BiCMOS 55 nm," in *2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2017, pp. 153–155.

[8] N. Ehsan, J. Piepmeier, M. Solly, S. Macmurphy, J. Lucey, and E. Wollack, "A robust waveguide millimeter-wave noise source," in *2015 European Microwave Conference (EuMC)*, 2015, pp. 853–856.

[9] H. J. Song and M. Yaita, "On-Wafer Noise Measurement at 300 GHz Using UTC-PD as Noise Source," *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, no. 8, pp. 578–580, Aug. 2014.

[10] F. Alimenti, G. Tasselli, C. Botteron, P. Farine, and C. Enz, "Avalanche Microwave Noise Sources in Commercial 90-nm CMOS Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 5, pp. 1409–1418, May 2016.

[11] M. Ghadiri-Sadrabadi, A. Subramanian, A. H. Coskun, and J. C. Bardin, "In-situ noise characterization of a 20–35 GHz 32 nm SOI CMOS reconfigurable LNA using a broadband on-chip noise source," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 51–54.

[12] C. Maya, A. Lázaro, and L. Pradell, "On-wafer noise sources characterization," in *Noise in Devices and Circuits II*, 2004, vol. 5470, pp. 448–460.

[13] J. R. Forrest and J. P. Meeson, "The avalanche diode high-level microwave noise source," *J. Phys. Appl. Phys.*, vol. 11, no. 13, p. 1831, 1978.

[14] R. H. Haitz and F. L. Opp, "A solid state broadband microwave noise source," in *1968 International Electron Devices Meeting*, 1968, vol. 14, pp. 46–46.

[15] A. Rodriguez, L. P. Dunleavy, and P. Kirby, "Best Practice for On-Wafer Millimeter Wave Noise Figure Measurements," in *57th ARFTG Conference Digest*, 2001, vol. 39, pp. 1–13.

[16] L. P. Dunleavy, J. Randa, D. K. Walker, R. Billinger, and J. Rice, "Characterization and applications of on-wafer diode noise sources," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 12, pp. 2620–2628, Dec. 1998.

[17] M. C. Maya, A. Lázaro, and L. Pradell, "Extraction of an avalanche diode noise model for its application as an on-wafer noise source," *Microw. Opt. Technol. Lett.*, vol. 38, no. 2, pp. 89–92, Jul. 2003.

[18] F. Alimenti, G. Tasselli, C. Botteron, P. A. Farine, and C. Enz, "Avalanche noise diodes: A compact circuit model compatible with advanced CAD tools," in *2015 International Conference on Noise and Fluctuations (ICNF)*, 2015, pp. 1–4.

João Carlos Azevedo Gonçalves received the M.S. degree in "Microélectronique Nanotechnologie & Telecom" from University of Lille, Villeneuve d'Ascq, France in 2015, and the Ph.D. degree in electrical engineering from the institute of Electronics, Microelectronics and Nanotechnology (IEMN), University of Lille, Villeneuve d'Ascq, France in 2015. Its research interest is in Advanced Silicon devices noise and large signal characterization up to 320 GHz. He is currently working at STMicroelectronics in the Technology Design Platform department Crolles on RF & mmW characterization for BiCMOS and CMOS advanced technologies.

H. Ghanem obtained a Diploma in electronics from the Lebanese University (LU) in 2014, and a master degree from the University of Grenople Alpes (UGA), France in 2017. Now, he is currently pursuing his PhD studies at the IEMN (Institute of Electronics, Microelectronics and Nanotechnology) /University of Lille. His PhD thesis is concerned with the millimetre wave noise measurements, characterizations using silicon and III-V technologies, especially for "on" and "off" wafer noise test benches towards evaluation of silicon devices up to 325 GHz.

Simon Bouvot received the M.S. degree in automatic control and electronics from INSA Toulouse, France, in 2014 and the Ph.D. degree in electrical engineering from Institute of Electronics, Microelectronics, and Nanotechnologies (IEMN), University of Lille, France, in 2018. Its research interest is in built-in self-test for Silicon noise characterization above 110 GHz. He is currently working at STMicroelectronics R&D on RF & mmW BiCMOS and CMOS circuits characterization.

Daniel Gloria received in 1995, the engineering degree in electronics from the Ecole Nationale Supérieure d'Electronique et de Radioélectricité and the M.S.E.E. in Optics, Optoelectronics and Microwaves design systems from the Institut National de Grenoble (INPG).

He spent two years, from 1995 to 1997, in ALCATEL Bell Network System Labs, in Charleroi (Belgium) as an RF designer engineer and was involved in the development of the Cablephone RF front end and its integration in Hybrid-Fiber-Coax telecommunication networks. Since 1997, he has been working for ST Microelectronics, in the Technology Design Platform department Crolles. His interests are in optimisation of RF&Photonics platforms for applications in BiCMOS and CMOS advanced technologies.

Sylvie Lepilliet was born in Béthune, France, on May 20, 1964. She received the B.E. degree in Electronics from the Centre National des Arts et Métiers (CNAM), Lille, France, in 1991. In 1986, she joined the Centre Hyperfréquences et Semiconducteurs, University Lille, Lille, France. She is currently in charge of the high-frequency measurement facilities of the Institute of Electronics, Microelectronics, and Nanotechnology, University Lille I, Villeneuve d'Ascq, France, particularly of the noise test set.

G. Ducournau obtained the Diplome d'ingénieur from ESIGELEC, Rouen, France in 2002. In 2002, he worked in Canada (Montréal) on the characterization of optical fiber Bragg gratings for core optical networks. In 2005, he obtained the PhD degree from Université de Rouen, France on fiber optic communication systems using DPSK modulation schemes. He was an Assistant Professor at the IEMN (Institute of Electronics, Microelectronics and Nanotechnology) / University of Lille 1 and Polytech'Lille Graduate School, in the THz Photonics group during 2007-2018. He is full professor since 2018. G. Ducournau is the leader of the THz wireless communications activity at IEMN using optoelectronic THz photomixers, electronic receivers, THz instrumentation and mm-wave characterization. He is author or co-author of more than 130 publications in peer-reviewed international journals or peer reviewed conferences proceedings and holds 1 patent. He has worked on several ANR and European projects (ITN "MITEPHO" and STREP "ROOTHz"). G. Ducournau was the coordinator of the COM'TONIQ project (2014-2017) funded by ANR (INFRA 2013) dedicated to THz communications in the 300 GHz band. He actually coordinates the ERA-NET TERALINKS program in which the main goal is the achievement of THz system level demonstrators based on advanced technologies in the 220-320 GHz range, and the ANR/DFG TERASONIC project for the use of THz photonics technologies and electrical solid-state technologies towards a complete 300 GHz transmission system for 100 Gbps wireless links. He is also participating to the ThOR project, an EU-Japan funded project for the developpement of km-range super-heterodyne THz transmission systems for the new IEEE 802.15.3d standard.

Christophe Gaquière received the Ph.D. degree in electronic from the University of Lille in 1995. He is currently full professor at the University of Lille (Polytech'Lille), and carries out his research activity at the Institut d'Electronique de Microélectronique et de Nanotechnology (IEMN). The topics concern design, fabrication, characterization and modeling of HEMT's and HBT devices. He works on GaAs, InP, metamorphic HEMT's and now he is involved in the GaN activities. His main activities are microwave characterizations (small and large signal between 1 and 500 GHz) in order to correlate the microwave performances with the technological and topology parameters. Today, his activities concern mainly the investigation of two-dimensional electronic plasmons and gunn like effects for THz solid state GaN based detectors and emitters (HEMT and SSD), AlGaN/GaN nano-wires for microwave applications and MEMS activities based also on GaN. He was responsible for the microwave characterization part of the common laboratory between Thales TRT and IEMN focus on wide band gap semiconductor (GaN, SiC, and Diamond) rom 2003 up to 2007. He is in the TPC of several European conferences. At the present time he has in charge the Silicon millimeter wave advanced technologies part of the common lab between ST microelectronics and IEMN. He has created the company MC2-technolgies. Christophe Gaquière is the author or co-author of more than 150 publications and 300 communications.

François Danneville received the PhD in Electronics and the « Habilitation à Diriger les Recherches » from Lille1 University, Sciences and Technology, in 1991 and 1999, respectively. Until 2000, as Assistant Professor at Lille1 University, he has studied the noise of III-V devices operating in linear and nonlinear operation (in LNA, Mixer and Oscillator). In 1998, on the aforementioned research topic, he made one year sabbatical as Visitor Scientist in HP (nowadays Keysight Technologies), Santa Rosa (USA). Since 2001, he has been Full Professor at Lille University where his research has focused on the small (large) signal and noise properties in high frequency range (centimeter and millimeter waves) of advanced Silicon Technologies (CMOS and SiGe HBTs), including alternative architectures and circuits design. In these areas, Professor François Danneville has published over 160 papers in international journals and conferences and has supervised 24

PhD students (2 on-going). Since 2014, his research work has focused also on the development of an ultra-low power silicon CMOS artificial neuron (published in Frontiers in Neuroscience –March 2017-) and is currently focusing on the integration (scaling) of this new neuromorphic technology within neural networks. His research areas of interest (to cite a few) are: - Biocomputing - Smart Visual and Hearing Sensors - Electronic systems for Neural recording and stimulation - fluctuations and noise in artificial and biologic neural systems.