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Concept and Realization of an Integrated 79-GHz Sequential Sampling Pulse Radar

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***Abstract*— A novel power-efficient integrated realization of a sequential sampling pulse radar, operating at 79 GHz, is presented in this article. The developed mathematical framework for the proposed concept illuminates the demands on the major building blocks and is substantiated by circuit simulations as well as in-system measurements of the fabricated chip. The presented self-biased current-output pulsed mixer concept achieves a conversion gain of 6 dB in measurements and simulations, operated with a pulse duration of 1 ns while maintaining zero power consumption between the pulses.**

***Index Terms*— Millimeter-wave integrated circuits, millimeter-wave radar, monolithic microwave integrated circuits (MMICs), pulse modulation, pulsed circuits.**

I. Introduction

SINCE the invention of radars, the advantages of contactless sensing have driven the development of different radar concepts optimized for various applications. In addition to the widely used frequency-modulated continuous-wave (FMCW) concept, the classical pulse radar concept is still present in chip-integrated solutions [1].

Power efficiency and system cost were the driving factors that led to the development of the sequential sampling pulse radar (SSPR) based on a time-spreading technique presented in [2]. Discrete realizations, first operating at 5 GHz [3] and later working at 24 GHz [4]–[6], find their application, for example, in liquid-level sensors [7], [8].

The SSPR concept allows to switch OFF the entire radio-frequency (RF) front end between the short RF pulses. Hence, both the average power consumption of the radar and the radio-channel occupancy scale down with the 1% duty cycle of the RF pulses. Furthermore, the SSPR concept economizes IF signal processing to an unsophisticated peak detection by embedding the autocorrelation functionality into the analog hardware, which reduces the digital signal processing expenditure by one fast-Fourier-transformation (FFT) stage.

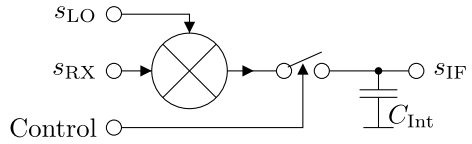

Fig. 1. Functional block diagram of the switch-based receiver presented in [9].

The simplicity and power efficiency of this concept make it attractive for low-power applications like parking aids or liquid-level sensors [7] and have motivated the development of an integrated realization at an operating frequency of 79 GHz. To the best of our knowledge, this article and [9] are the only published SiGe-integrated SSPR in the 77-GHz band.

A first working prototype reported in [9] combines a mixer concept, based on biased diodes as presented in [10], with a transmission gate switch. The integrator unit consists of the mixer, modeled by its output resistance, and the connected load capacitor, where the switch prevents the capacitor from discharging between the pulses. The block diagram of this receiver is depicted in Fig. 1. In this receiver concept, the mixer is almost off between the pulses, but the performance of the system strongly depends on precise switch timing, which counters the simplicity of the concept. In practice, the improper switch timing decreased the receiver gain to -13 dB.

In this article, the key parameters for operating the SSPR at millimeter-wave (mm-Wave) frequencies and the challenges for the chip-integrated realization of the required mixer–integrator unit are investigated. The proposed concept for a power-efficient mixer realization for a chip-integrated SSPR in a 250-GHz f_T SiGe BiCMOS technology mitigates the critical switch from [9] and, hence, provides significantly more gain without the need for a precise timing unit. The expected improvements are validated by measurements with the fabricated chip being assembled in a prototype demonstrator system. Furthermore, in this article, the impact of the major RF building blocks of the SSPR and their impairments on the performance of the system are illuminated, and a mathematical framework for the pulse radar is developed. The correctness of the derived equations is authenticated with the results from circuit simulations, and finally, measurement results verify the theoretical framework around the SSPR.

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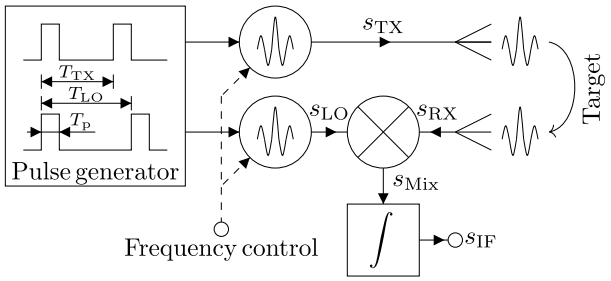

Fig. 2. Functional block diagram of the SSPR.

II. Concept and Signal Model

The SSPR concept involves the sequences of ultrashort, phase-coherent, RF pulses with duty cycles in the range of 1% or below, which constitutes special challenges on circuit implementation. Fig. 2 shows a functional block diagram of the SSPR.

The analytical description of a single RF pulse with the duration T_p is given by

$$p(t) = e(t)\sin(\omega_0 t) \quad \text{for } 0 \le t \le T_p \text{ else } 0. \tag{1}$$

The pulse shape is defined by the time-limited and normalized envelope function $e(t)$, which is modulated onto a harmonic carrier signal with the angular frequency ω_0. The transmit (TX) signal and the local oscillator (LO) signal are composed from the periodic repetitions of the single RF pulses. The pulse generator visible on the left-hand side of Fig. 2 controls the pulse duration T_p as well as the pulse-repetition times T_{TX} and T_{LO} of the generated pulse series. The RF pulses are generated from two independent, coherent start-up pulse oscillators. The concept of the pulse oscillators was presented in [11]. With the pulse-repetition times T_{TX} and T_{LO} chosen such that the time-spreading factor $\beta = T_{LO}/(T_{LO} - T_{TX})$ becomes an integer, the pulse sequence repeats after β samples. One period of the LO signal can then be expressed as

$$s_{LO}(t) = \sum_{k=-\lfloor \frac{\beta}{2} \rfloor}^{\lceil \frac{\beta}{2} \rceil} e(t - kT_{LO})\sin(\omega_0(t - kT_{LO})). \tag{2}$$

The period boundaries have been chosen such that the maximum of the IF signal envelope occurs at index $k = 0$. $\lfloor\cdot\rfloor$ denotes the floor operator $\lfloor a \rfloor := \max\{k \in \mathbb{Z} | k \le a\}$ and $\lceil\cdot\rceil$ denotes the ceil operator $\lceil a \rceil := \min\{k \in \mathbb{Z} | k \ge a\}$, respectively. In order to describe the TX signal, (2) can be reused with the TX pulse-repetition time T_{TX} instead of the LO pulse-repetition time T_{LO} and with the magnitude A_0

$$s_{TX}(t) = A_0 \sum_{k=-\lfloor \frac{\beta}{2} \rfloor}^{\lceil \frac{\beta}{2} \rceil} e(t - kT_{TX})\sin(\omega_0(t - kT_{TX})). \tag{3}$$

The ideal mixer in the block diagram (see Fig. 2) multiplies the LO signal with the received reflection s_{RX} of the TX signal s_{TX} and scales the result with the mixer gain g_{Mix}

$$s_{Mix}(t) = g_{Mix} s_{LO}(t) s_{RX}(t). \tag{4}$$

It is assumed that the reflecting target is at position zero and, therefore, $s_{RX} = s_{TX}$. Provided that the duty cycle of the pulses is less than 50%, only pulses with the same index in the pulse sequences interfere with each other. The product of sums at the mixer output can then be transformed into the sum of products. The double-frequency term associated with the product of the two sine functions can be neglected because of the low-pass characteristic of the consecutive integrator. With the time-spread carrier frequency $\Omega_0 = T_{TX}\omega_0/\beta$ and the product of the envelopes

$$ee(t,k) = e(t - kT_{TX})e(t - kT_{LO}) \tag{5}$$

the resulting expression for the output signal of the mixer is

$$s_{Mix}(t) = A_0 g_{Mix} \sum_{k=-\lfloor \frac{\beta}{2} \rfloor}^{\lceil \frac{\beta}{2} \rceil} ee(t,k)\cos(k\Omega_0). \tag{6}$$

The final processing step in Fig. 2 is the integration of the mixer output signal in the time domain. Because of linearity, the sum in (6) and the integration can be swapped, which leads to

$$s_{IF}(t) = A_0 g_{Mix} \sum_{k=-\lfloor \frac{\beta}{2} \rfloor}^{\lceil \frac{\beta}{2} \rceil} \cos(k\Omega_0) \int_{-\infty}^{t} ee(t,k)dt. \tag{7}$$

Now the output signal is sampled right before the beginning of each pulse. Hence, the sum can be stopped at the $(n-1)$th sample and the integration limit can be expanded to infinity. This condenses the entire integral to the autocorrelation function φ_{ee} of the pulse envelope. With the substitution $\Delta T = T_{LO} - T_{TX}$, the sampled output signal of the SSPR can be written as

$$s_{IF}[n] = A_0 g_{Mix} \sum_{k=-\lfloor \frac{\beta}{2} \rfloor}^{n-\lceil \frac{\beta}{2} \rceil - 1} \cos(k\Omega_0)\varphi_{ee}(k\Delta T). \tag{8}$$

In the later development of the proposed mixer pulse-conversion gain, the sample timing is of essential importance. The IF signal of the SSPR shows a constant frequency, and the distance information is embedded in the envelope and phase of the IF signal, respectively.

The output of the ideal SSPR from Fig. 2 was simulated on a computer math software package. For the simulation, rectangle-shaped LO and RF pulses with a carrier frequency of 79 GHz and a pulse duration of 1 ns have been used. The pulse-repetition time was 100 ns with a difference ΔT of 1 ps, which gives a time-spreading factor of $\beta = 10^5$. For the simulation, it was assumed that the target is at zero distance, which corresponds to a zero round-trip delay time.

Fig. 3 illustrates the simulated output signal, where the peak indicates the target position. The triangular shape of the output signal corresponds to the autocorrelation function φ_{ee} of the RF pulse rectangle-shaped envelope. The IF pulse duration of $2\beta T_p = 200\ \mu$s as well as the carrier frequency of 790 kHz reflect the time-stretching behavior of the SSPR [2].

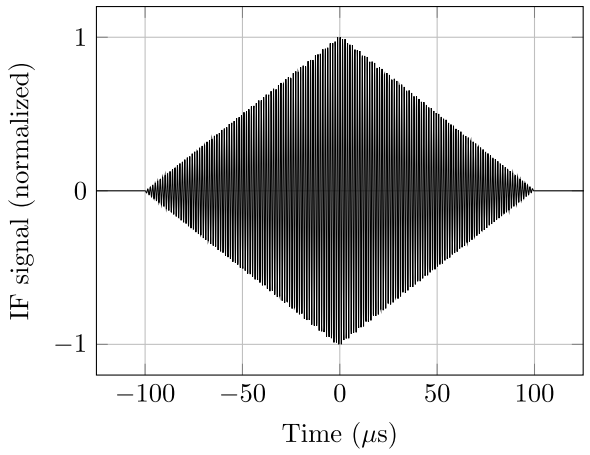

Fig. 3. Simulated IF output pulse of the ideal SSPR, which illustrates the envelope transformation and the time-stretching behavior of the SSPR.

A. Jitter Loss

The purpose of this section is to highlight the importance of the coherent start-up condition of the voltage controlled oscillator (VCO) and to analyze the impact of the start-up phase jitter on the SSPR. The design procedure of the coherent start-up VCO described in detail in [11] minimizes the intrinsic start-up phase jitter of the VCO, but also the jitter of the clock signals contributes to the overall phase jitter. For the purpose of this analysis, the signal model is extended with the random variable $\tau_j \sim \mathcal{N}(0, t_j^2)$, which describes the overall jitter of the VCO and the clock signal. It is assumed that the jitter follows a normal distribution with the standard deviation given by the rms jitter t_j. The jitter fluctuates the position of the pulses in the time domain according to

$$p(t) = e(t - \tau_j)\sin(\omega_0(t - \tau_j)). \tag{9}$$

It can be assumed that the jitter is small compared with the pulse duration T_p, and thus, the effect on the envelope $e(t)$ of the pulse is negligible

$$p(t) \approx e(t)\sin(\omega_0(t - \tau_j)). \tag{10}$$

Repeating the steps for the deviation of the signal model from the previous chapter with the extension from (10) leads to the description of the distorted output signal

$$s_{\mathrm{IF}}[n] \approx A_0 g_{\mathrm{Mix}} \sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{n-\lceil\frac{\beta}{2}\rceil-1} \cos(k\Omega_0 + \phi_j)\varphi_{ee}(k\Delta T) \tag{11}$$

where the random variable $\phi_j = \omega_0(\tau_{j,\mathrm{TX}} - \tau_{j,\mathrm{LO}}) \sim \mathcal{N}(0, 2(\omega_0 t_j)^2)$ accounts for the combined jitter of the TX VCO and the LO. It is assumed that both VCOs are identical circuits and, hence, generate the same but uncorrelated jitter. The result (11) shows that jitter introduces a random phase modulation to the carrier of the output signal of the SSPR. Compared with the phase noise of the VCO, the jitter usually dominates the phase error. The random phase modulation scatters a part of the IF signal power away from the carrier frequency. Combined with the bandpass filter (BPF) behavior formed by the antialiasing filter and the dc block capacitor, it leads to a loss of IF signal power. When the jitter is reasonably small, the effect on the envelope can be neglected and further derivations focus on the carrier signal only. The jitterless carrier signal is given by $s_{\mathrm{ideal}}(k) = \sin(k\Omega_0)$, and the distorted carrier signal is given by $s_j(k) = \sin(k\Omega_0 + \phi_j)$, respectively. The loss due to jitter (jitter loss) α_j can then be expressed as the ratio of the Fourier coefficients at the carrier frequency Ω_0 of the distorted signal related to the jitterless case

$$\alpha_j = 20\log_{10}\left(\frac{|S_j(\Omega_0)|}{|S_{\mathrm{ideal}}(\Omega_0)|}\right). \tag{12}$$

For the jitterless case, the Fourier coefficient is given by

$$|S_{\mathrm{ideal}}(\Omega_0)| = \frac{2}{\beta}\left|\sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{\lceil\frac{\beta}{2}\rceil} s_{\mathrm{ideal}}(k)e^{-\imath k\Omega_0}\right| = 1. \tag{13}$$

In the case of the distorted IF signal, the expectation value $E\{\cdot\}$ of the Fourier coefficient must be calculated

$$|S_j(\Omega_0)| = \frac{2}{\beta}\left|E\left\{\sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{\lceil\frac{\beta}{2}\rceil} s_j(k)e^{-\imath k\Omega_0}\right\}\right|. \tag{14}$$

In a first step, the complex exponential function is expanded into sin and cos terms by applying the Euler identity $e^{-\imath k\Omega_0} = \cos(k\Omega_0) - \imath\sin(k\Omega_0)$ and $s_j(k)$ is inserted

$$\begin{aligned}|S_j(\Omega_0)| &= \frac{2}{\beta}\left|E\left\{\sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{\lceil\frac{\beta}{2}\rceil} \sin(k\Omega_0 + \phi_j)\cos(k\Omega_0)\right.\right.\\ &\qquad\left.\left. -\imath\sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{\lceil\frac{\beta}{2}\rceil} \sin(k\Omega_0 + \phi_j)\sin(k\Omega_0)\right\}\right|.\end{aligned} \tag{15}$$

The above equation can be simplified by using the trigonometric identities. In addition, neglecting the double-frequency terms leads to

$$|S_j(\Omega_0)| = \frac{1}{\beta}\left|E\left\{\sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{\lceil\frac{\beta}{2}\rceil} \sin(\phi_j) - \imath\cos(\phi_j)\right\}\right|. \tag{16}$$

Again applying the Euler identity and pulling the k-independent term out of the sum leads to

$$|S_j(\Omega_0)| = \frac{1}{\beta}|E\{e^{-\imath\phi_j}\}|\sum_{k=-\lfloor\frac{\beta}{2}\rfloor}^{\lceil\frac{\beta}{2}\rceil} 1 = |E\{e^{-\imath\phi_j}\}|. \tag{17}$$

The expectation value of a transformed random variable X is given by

$$E\{g(x)\} = \int_{-\infty}^{\infty} g(x)f_X dx \tag{18}$$

where f_X is the probability density function (pdf) of the random variable X. In the case of the SSPR, the pdf of the

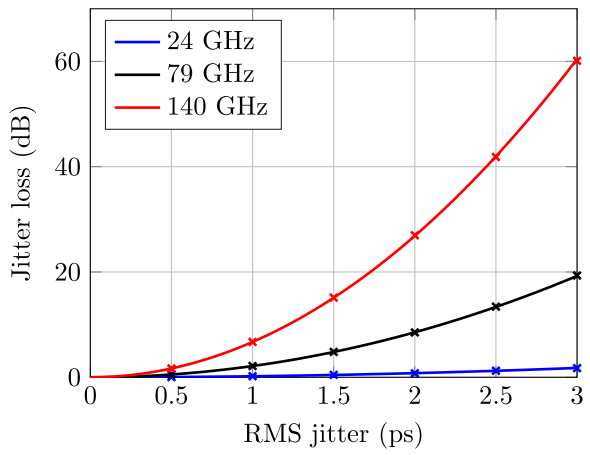

Fig. 4. Calculated (solid) and numerically simulated (crosses) jitter loss as a function of the rms jitter at different operating frequencies of the SSPR.

phase error ϕ_j is given by

$$f_{\phi_j}(x) = \frac{1}{\sqrt{4\pi\,(\omega_0 t_j)^2}} e^{-\left(\frac{x}{2\omega_0 t_j}\right)^2}. \tag{19}$$

Based on (19) and (18), the expectation value of (17) can be expressed as

$$|S_j(\Omega_0)| = \frac{1}{\sqrt{4\pi\,(\omega_0 t_j)^2}} \left| \int_{-\infty}^{\infty} e^{-\frac{x^2}{4(\omega_0 t_j)^2}} e^{\imath x} dx \right|. \tag{20}$$

This equation has the form of a Fourier transform $F\{\cdot\}$ of the Gaussian curve, evaluated at $\omega = 1$

$$|S_j(\Omega_0)| = \frac{1}{\sqrt{4\pi\,(\omega_0 t_j)^2}} \left| \mathcal{F}\left\{ e^{-\frac{x^2}{4(\omega_0 t_j)^2}} \right\}\Big|_{\omega=1} \right|. \tag{21}$$

Using the corresponding Fourier transform pair yields the compact result

$$|S_j(\Omega_0)| = e^{-(\omega_0 t_j)^2}. \tag{22}$$

Based on this result, the jitter loss (12) can be written as

$$\alpha_j = 20\log_{10}\left(e^{(\omega_0 t_j)^2}\right) \approx 8.68(\omega_0 t_j)^2. \tag{23}$$

In Fig. 4, the calculated jitter loss for different carrier frequencies is plotted. It shows the strong increase in the demands on the phase jitter of the VCO and the clock signal with higher operating frequencies of the SSPR.

The crosses in Fig. 4 indicate the jitter loss obtained from numerical simulations. For each simulation point, 1000 realizations of the jittered IF pulse have been created.

III. Circuit Design

A. Coherent Start-Up VCO

In the previous chapter, the importance of the coherent start-up of the VCO by means of phase jitter has been highlighted. In this section, a brief overview of the designed coherent start-up VCO [11] is given. The design procedure published in [11] minimizes the turn-on phase jitter by fast switching ON and

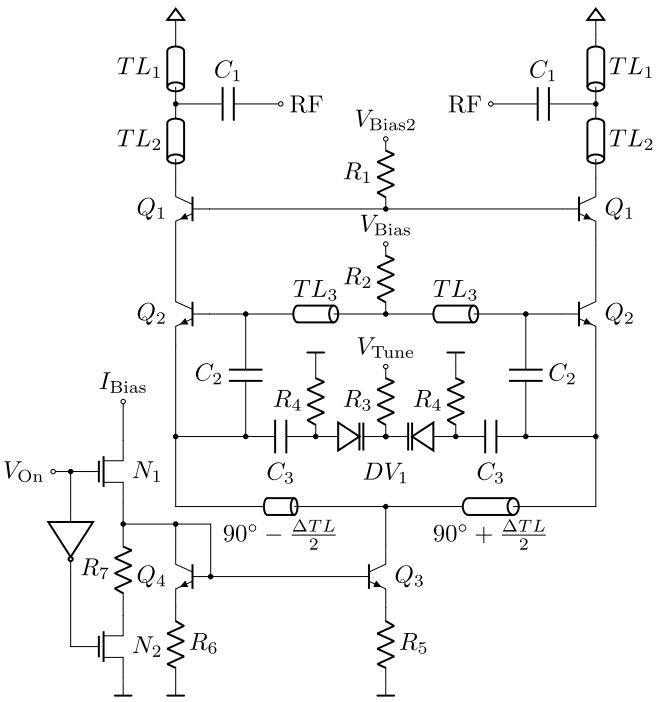

Fig. 5. Schematic of the updated coherent start-up VCO based on the design in [11].

TABLE I
Parameters of the Components Used in the Designed VCO

Component	Value	Component	Value
C_1	300 fF	TL_3	22.7 °, 50 Ω
C_2	70 fF	Q_1	L=10 μm
C_3	400 fF	Q_2	L=6 μm
DV_1	Varactor	Q_3	L=18 μm
R_1,R_2,R_3	100 Ω	Q_4	L=4 μm
R_4	420 Ω	N_1	$^W/_L = 416.7$
R_5	5.55 Ω	N_2	$^W/_L = 83.3$
R_6	50 Ω	V_{Bias}	1.55 V
R_7	350 Ω	V_{Bias2}	2.75 V
ΔTL	38 °, 50 Ω	I_{Bias}	2 mA
TL_1, TL_2	19 °, 50 Ω	V_{On}	1.8 V CMOS logic level

by displacing the tail current source Q_3 by ΔTL from the circuit's symmetry axis. The circuit diagram in Fig. 5 shows the differential Colpitts VCO core (Q_2, TL_3, C_2, C_3, DV_1, and the 180° tail transmission line) with the cascode stage output buffer Q_1 and the shifted tail current mirror Q_3 and Q_4. Furthermore, the VCO switch consisting of N_1 and N_2 is shown in Fig. 5, where the bias current I_{Bias} is provided from a bandgap reference circuit. A high logic level of the input signal V_{ON} activates N_1, and current flow is enabled while simultaneously N_2 is switched OFF. When the logic level on V_{ON} is low, N_1 is OFF and N_2 shorts the bases of the tail current mirror to ground. Compared with the design presented [11], the center frequency of the VCO has been adjusted and the output matching networks TL_1, TL_2, and C_1 have been optimized. Table I summarizes the parameters of the components used in the VCO.

B. Current Output Sampling Mixer

In order to circumvent the difficult precise switch timing from [9], but still preventing the integrating capacitor C_{Int}

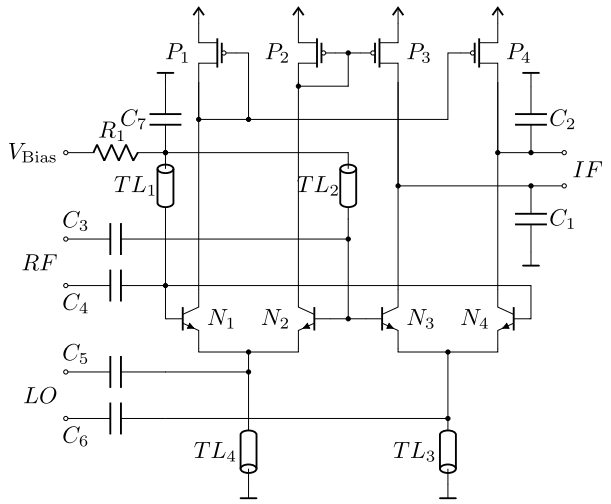

Fig. 6. Schematic of the proposed LO controlled mixer with current output.

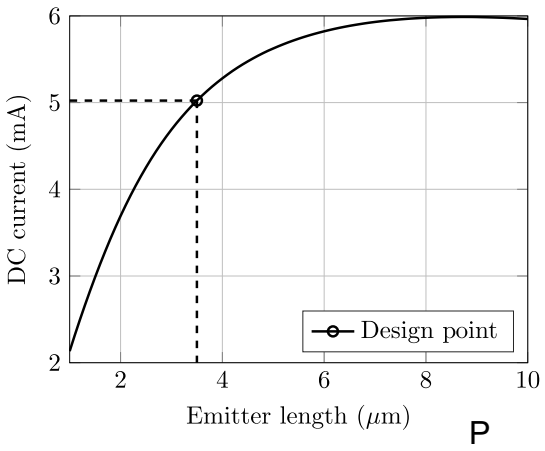

Fig. 7. Simulated dc branch current as a function of the emitter length of the bipolar transistor.

TABLE II

PARAMETERS OF THE COMPONENTS USED IN THE PROPOSED MIXER

Component	Value	Component	Value
C_1, C_2	0 to 9.375 pF	TL_1, TL_2	26 °, 50 Ω
C_3, C_4	90 fF	TL_3, TL_4	35 °, 50 Ω
C_5, C_6	280 fF	P_1 to P_4	$^{W}/_{L} = 250$
C_7	2 pF	N_1 to N_4	L=3.5 μm
R_1	1.9 kΩ	V_{Bias}	0.55 V

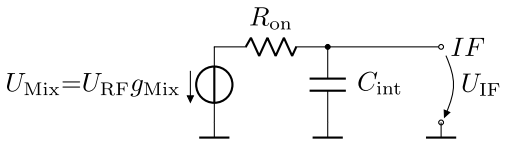

Fig. 8. Small-signal equivalent circuit diagram for the IF output of the proposed mixer.

from discharging, an LO controlled mixer with a current output like in an operational transconductance amplifier (OTA) is suggested. In combination with a load capacitor, an OTA-C integrator topology is realized. Fig. 6 shows the schematic of the proposed mixer.

The core of the mixer is formed by the four high-speed n-p-n transistors N_1 to N_4, which perform the actual mixing of the RF signals. The RF signal enters the circuit by the matching network C_3, C_4, TL_1, and TL_2 at the bases of the transistors. The LO signal is connected to the emitters by the matching network formed by C_5, C_6, TL_3, and TL_4. In the proposed configuration, the transistors are in common-emitter configuration from the RF signal point of view. Compared with an accustomed common-base configuration, where the LO signal drives the bases of the bipolar transistors, the common-emitter configuration can provide a significantly higher current gain, which is very appreciated for the current output of the mixer. An additional transconductor stage at the RF input cannot be used in the proposed mixer, because the required bias voltages would prevent the mixer from switching OFF between the pulses. The bias voltage V_{Bias} was chosen such that without LO Power, the bipolar transistors N_1–N_4 are OFF. This selection of the bias voltage increases the mixer output resistance between the pulses and prevents the capacitor from discharging. Based on Monte Carlo simulations, a value of 550 mV was found. When an LO pulse is present, the negative half period of the LO signal decreases the emitter potential of the respective mixer branch. Hence, the collector current rises and the mixer branch turns on. During the positive half period of the LO signal, the respective base–emitter diode is reverse-biased and the corresponding branch is OFF. The periodic commutation of the mixer branches leads to the desired frequency conversion. The simulated average dc current is shown in Fig. 7 as a function of the transistor emitter length simulated with an LO power of 7.25 dBm. The size of the n-p-n transistors was designed to reach the required collector current density for the highest f_T.

The self-biasing concept links the mixer state directly to the LO signal and, hence, mitigates the critical switch timing, which is required for the mixer in [9]. The bidirectional current output of the mixer is implemented with the PMOS current mirrors P_1–P_4. Initially, the PMOS transistors have been sized based on the mixer dc current to achieve a threshold voltage of 500 mV. The resulting huge transistor size counters the operation of the mixer with the required very short pulse-durations. Hence, the transistor size has been reduced on the expense of additional 500 mV of output voltage swing. The integrating capacitors C_1 and C_2 are implemented as switchable capacitors, and the supply voltage of the mixer is 1.8 V. Finally, the impedance matching network of the mixer was optimized based on circuit simulations.

Table II summarizes the parameters of the components used, where for the transmission lines, the characteristic impedance and the electrical length in degrees are given.

C. Signal Model

In this section, the proposed mixer gets integrated into the signal model from Section II and a formula for the pulse-conversion gain of the SSPR receiver is derived. In Fig. 8, a first-order approximation for the IF output of the mixer in ON-state is shown. The mixer is included as a voltage

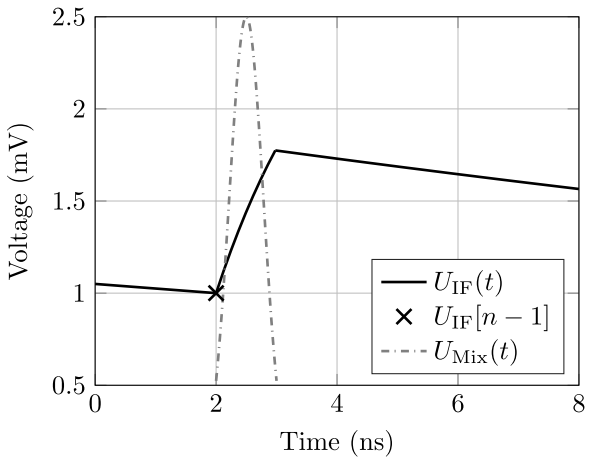

Fig. 9. Sketch of the IF voltage in time domain during an IF pulse.

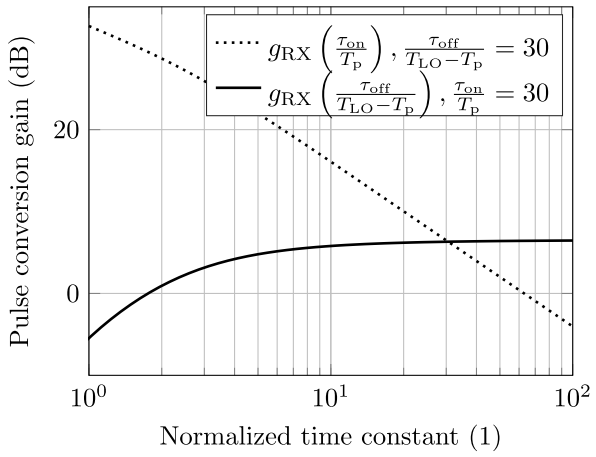

Fig. 10. Calculated pulse-conversion gain versus the time constants τ_{ON} and τ_{OFF} normalized to the pulse duration T_p and to the break time $T_{\mathrm{LO}} - T_p$, respectively.

source, where the nonlinear conversion from RF to IF is modeled with the mixer voltage conversion gain g_{Mix}. The voltage U_{RF} denotes the peak amplitude of the applied RF pulses. The mixer output signal for the nth step is given by $ee(t,n)\cos(n\Omega_0)$, as derived in Section II. The mixer output resistance in ON-state R_{ON} together with the integrating capacitor C_{int} forms a first-order low-pass filter. The 3-dB corner frequency of the low-pass filter is given by

$$f_{c,\mathrm{ON}} = \frac{1}{2\pi\, R_{\mathrm{ON}} C_{\mathrm{int}}} = \frac{1}{2\pi\,\tau_{\mathrm{ON}}}. \tag{24}$$

Both parameters, the mixer gain and the 3-dB corner frequency, can be measured and simulated with the mixer in continuous-wave (CW) operation. Fig. 9 shows a sketch of the IF voltage during one pulse.

During a pulse, the mixer charges the capacitor with the time constant τ_{ON}, and simultaneously, the previous sample $u_{\mathrm{IF}}[n-1]$ gets discharged with the same time constant. When the mixer is OFF between the pulses, the output resistance increases to the value R_{OFF}, and the capacitor is slowly discharged with the time constant being named τ_{OFF}.

The IF output voltage at the sampling points right before the next pulse occurs can, therefore, be described with the difference equation

$$u_{\mathrm{IF}}[n] = \left(u_{\mathrm{IF}}[n-1]e^{-\frac{T_p}{\tau_{\mathrm{ON}}}} + u_{\mathrm{step}}[n]\right) e^{-\frac{T_{\mathrm{LO}}-T_p}{\tau_{\mathrm{OFF}}}}. \tag{25}$$

The pulse-conversion gain of the receiver g_{RX} relates the peak amplitude of the IF output voltage u_{IF} to the peak amplitude of the received RF signal U_{RF}. In order to calculate the pulse-conversion gain, (25) is first transformed into z-domain

$$u_{\mathrm{IF}}(z) = (u_{\mathrm{IF}} z^{-1}\alpha_{\mathrm{ON}} + u_{\mathrm{step}}(z))\alpha_{\mathrm{OFF}} \tag{26}$$

with $\alpha_{\mathrm{ON}} = e^{-T_p/\tau_{\mathrm{ON}}}$ and $\alpha_{\mathrm{OFF}} = e^{-(T_{\mathrm{LO}}-T_p)/\tau_{\mathrm{OFF}}}$. The equation is then rearranged to find the transfer function of the described system

$$H(z) = \frac{u_{\mathrm{IF}}(z)}{u_{\mathrm{step}}(z)} = \frac{\alpha_{\mathrm{OFF}}}{1 - z^{-1}\alpha_{\mathrm{ON}}\alpha_{\mathrm{OFF}}}. \tag{27}$$

The pulse-conversion gain can now be found by evaluating the magnitude of the transfer function $H(z)$ at the discrete IF signal frequency $z = e^{j\Omega_0}$

$$|H(e^{j\Omega_0})|^2 = \frac{\alpha_{\mathrm{OFF}}^2}{1 + \alpha_{\mathrm{ON}}^2\alpha_{\mathrm{OFF}}^2 - 2\alpha_{\mathrm{ON}}\alpha_{\mathrm{OFF}}\cos(\Omega_0)}. \tag{28}$$

Next, the voltage step $u_{\mathrm{step}}[n]$ of the nth pulse can be calculated from the convolution of the mixer output signal with the impulse response of the first-order low-pass filter according to

$$u_{\mathrm{step}}[n] = U_{\mathrm{RF}}\frac{g_{\mathrm{Mix}}\cos(n\Omega_0)}{\tau_{\mathrm{ON}}}\left(ee(\xi,n) * e^{-\frac{\xi}{\tau_{\mathrm{ON}}}}\right). \tag{29}$$

Using the assumption that the pulse duration T_p is significantly shorter than the mixer time constant in the ON-state, the voltage step can be approximated by

$$u_{\mathrm{step}}[n] \approx \frac{U_{\mathrm{RF}} g_{\mathrm{Mix}}\cos(n\Omega_0)}{\tau_{\mathrm{ON}}}(ee(\xi,n) * 1). \tag{30}$$

The convolution then reduces to the following integral:

$$u_{\mathrm{step}}[n] \approx \frac{U_{\mathrm{RF}} g_{\mathrm{Mix}}\cos(n\Omega_0)}{\tau_{\mathrm{ON}}}\int_{-\infty}^{\infty} ee(\xi,n)d\xi \tag{31}$$

which is equal to the autocorrelation function of the RF pulse envelope similar to (8)

$$u_{\mathrm{step}}[n] \approx \frac{U_{\mathrm{RF}} g_{\mathrm{Mix}}\cos(n\Omega_0)}{\tau_{\mathrm{ON}}}\varphi_{ee}(n\Delta T). \tag{32}$$

The peak amplitude occurs at $n = 0$ and is given by

$$u_{\mathrm{step}}[0] \approx \frac{U_{\mathrm{RF}} g_{\mathrm{Mix}}}{\tau_{\mathrm{ON}}}\varphi_{ee}(0). \tag{33}$$

Combining this result with (28) gives an approximation for the pulse-conversion gain of the proposed mixer

$$g_{\mathrm{RX}} \approx \frac{g_{\mathrm{Mix}}\varphi_{ee}(0)}{\tau_{\mathrm{ON}}}|H(e^{j\Omega_0})|. \tag{34}$$

The dotted line in Fig. 10 visualizes the dependence of the pulse-conversion gain g_{RX} on the time constant in the ON-state τ_{ON} normalized to the pulse duration T_p. A smaller time constant here is equal to a larger bandwidth, which leads to a higher pulse-conversion gain. The solid line in Fig. 10 shows

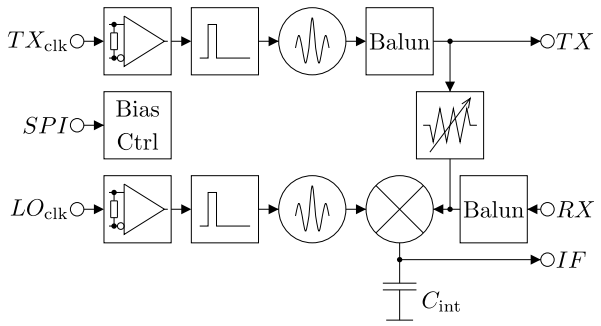

Fig. 11. Block diagram of the designed SSPR chip.

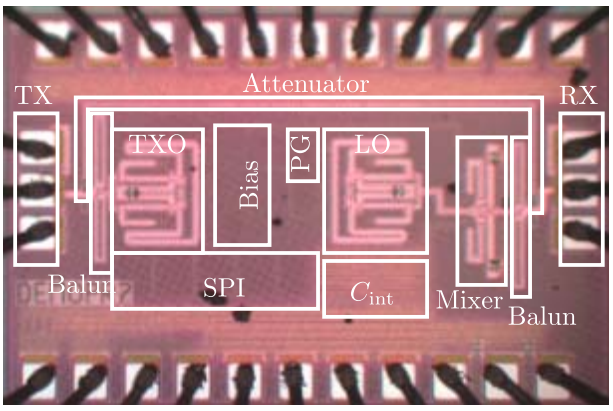

Fig. 12. Annotated micrograph of the fabricated pulse radar chip. The transmission lines on the top metal layer make the RF building blocks clearly visible.

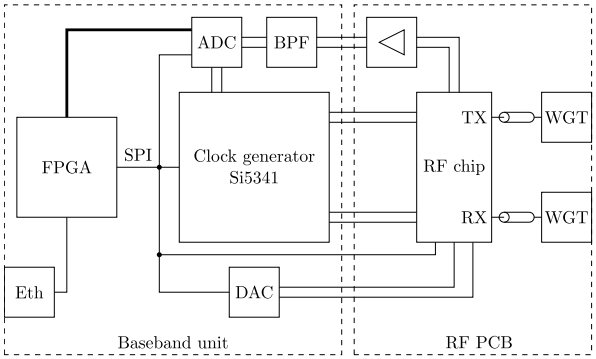

Fig. 13. Logical block diagram of the assembled pulse radar unit reflecting the structure and interconnections of the RF PCB and FPGA baseband unit.

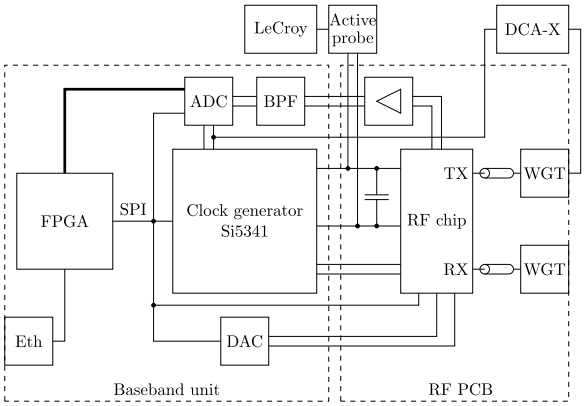

Fig. 14. Block diagram of the measurement setup used for the pulse envelope measurements and jitter loss measurements.

the behavior of the pulse-conversion gain across the OFF-state time constant τ_{OFF} relative to the break time $T_{\mathrm{LO}} - T_p$. In the OFF-state, a higher time constant, which equally describes a lower capacitor discharge, is desirable. A realizable value of 30 is used for the remaining free parameter of each curve in Fig. 10.

D. Chip Overview

Fig. 11 shows a block diagram of the designed chip, which is based on the design presented in [9], except for the pulse oscillator and the mixer. Like in [9], the TX and LO clock signals are applied by low voltage differential signaling (LVDS) interfaces and an SPI interface is used to configure the digital parts of the chip. A digitally switchable attenuator connects TX and RX, which creates a reference pulse at the IF output.

IV. Measurements

A. Preparation

The fabricated chip, which has the dimensions of 1448 μm $\times$ 930 μm was mounted bare die onto an RF PCB. Fig. 12 shows an annotated micrograph of the bonded chip. Apart from the new mixer, the chip layout is similar to the layout of the chip in [9].

The RF PCB includes two waveguide transitions (WGTs) for mounting WR12 horn antennas and a unity gain buffer amplifier, which decouples the IF output of the chip from the following stage. For the RF path, the same loss of 8.9 dB, as reported in [9], applies. Because of the increased receiver gain, the active IF filter that was used in [9] could be replaced by a passive BPF. A block diagram of the fully assembled radar unit is shown in Fig. 13.

B. Transmitter Measurement

1) CW Measurement: Before conducting any measurements in pulse mode, the VCO was first verified in the CW operating mode. Therefore, the clock generator was switched OFF and the pulse generator was programmed for infinite pulsewidth. At the TX WGT, an output power of -1.27 dBm was measured with an Agilent E4416A power meter. By correcting this value with the RF path loss, the calculated output power of the VCO is found to be 7.63 dBm. This result corresponds well with the simulated VCO output power of 7.41 dBm.

2) Pulsed Measurement: In order to verify the VCO in pulsed mode, a Keysight DCA-X 86100D sampling scope was connected to the TX WGT of the RF PCB. A block diagram of the measurement setup is shown in Fig. 14. The AD converter clock served as a trigger signal for the sampling scope. The active probe together with a LeCroy oscilloscope was used for the later measurement of the risetime of the clock signal. The capacitor was not installed yet. As a first step, the pulse shape of the VCO was measured. Therefore, the sampling scope was

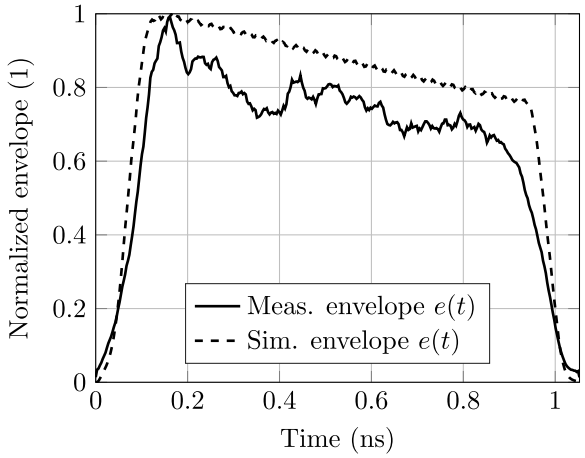

Fig. 15. Measured (solid) and simulated (dashed) envelopes of the TX pulse in the time domain captured with a Keysight DCA-X 86100D sampling scope.

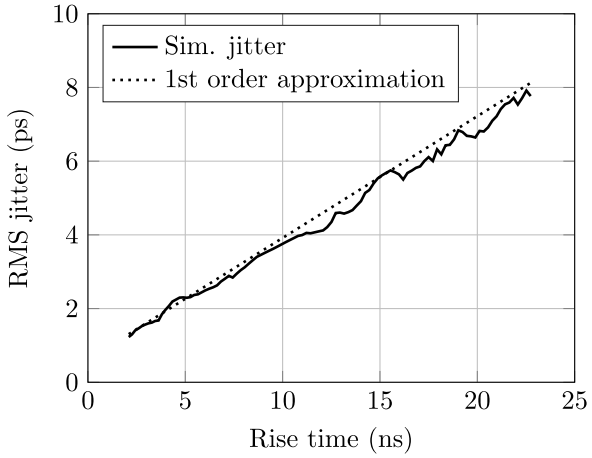

Fig. 16. Simulated jitter of the LVDS interface used across the risetime of the applied clock signal (solid) and first-order approximation (dashed).

TABLE III
CALCULATED MAXIMUM VALUES OF THE AUTOCORRELATION FUNCTION OF THE MEASURED AND SIMULATED PULSES

Sim. $\varphi_{ee}(0)$	Meas. $\varphi_{ee}(0)$
$655 \cdot 10^{-12}$	$502.8 \cdot 10^{-12}$

configured to capture the RF pulse in the time domain and acquired a total of 8192 samples from consecutive RF pulses. In Fig. 15, the simulated and measured normalized envelopes are visualized.

For the calculation of the pulse-conversion gain according to (34), the maximum value of the autocorrelation function φ_{ee} of the pulse envelope needs to be calculated from the measured and from the simulated pulse shape. The resulting values in Table III show that the simulation predicts a 30% higher maximum of the autocorrelation function than the measurement.

3) Jitter Loss Measurement: Next, the jitter loss result (23) is validated. Therefore, a clock signal with adjustable jitter is required. In a first-order approximation, the jitter after a threshold switch is linear proportional to the risetime of the applied input signal. In Fig. 16, the simulated jitter of the pulse radar LVDS interface is shown across the risetime of the input clock. For comparison, the results of a first-order approximation are shown with the dashed line.

In the case of the existing hardware, the risetime of the clock signal can be easily increased by installing a capacitor in the clock trace, as illustrated in Fig. 14. The effect of the capacitor on the risetime of the clock signal was simulated under the assumption that the differential output resistance of the clock chip is 100 Ω. For the measurement of the risetime, the built-in 10% to 90% risetime function of the Lecroy oscilloscope was used. The solid line in Fig. 17 illustrates the measured risetime for different installed capacitors, and the dashed line displays the results from circuit simulation. Most likely, the deviations are caused by the tolerances of the capacitor values.

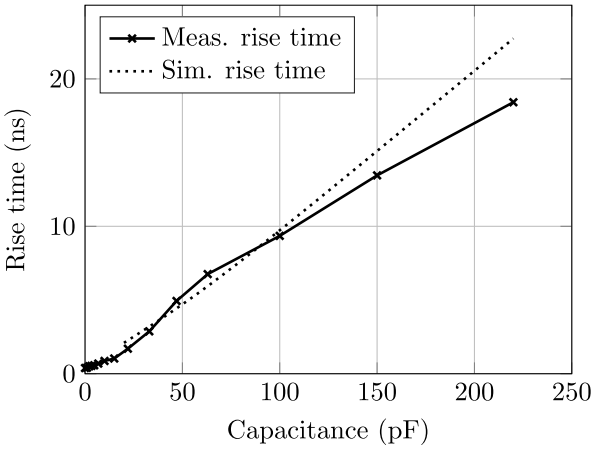

Fig. 17. Measured (solid) and simulated (dashed) risetimes of the clock signal for different values of the installed capacitor.

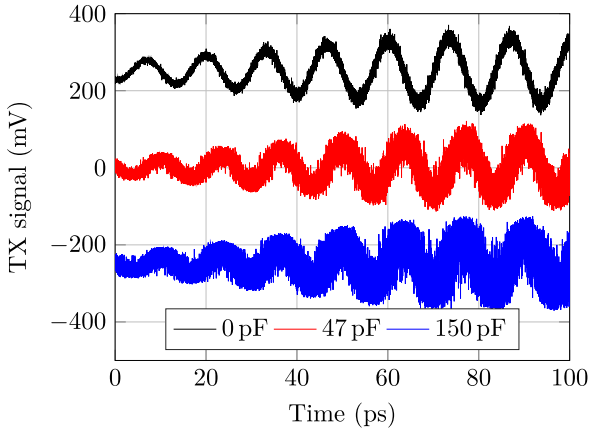

Fig. 18. Measured starting cycles of the TX signal, demonstrating the effect of increasing phase jitter on the TX pulses.

The effect of the increased jitter on the TX signal can directly be observed at the sampling scope. In Fig. 18, the first cycles of the measured TX pulses is shown without an installed capacitor (black), with 47 pF (red), and with

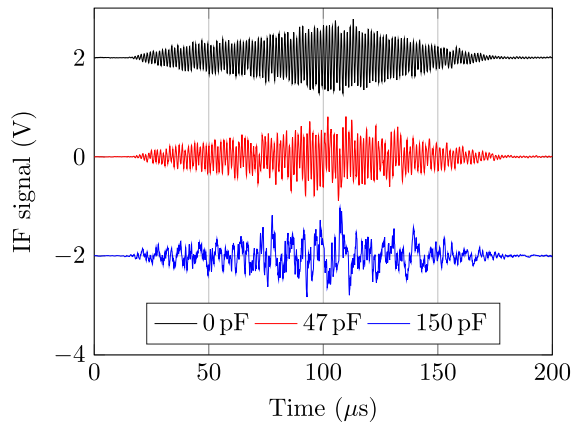

Fig. 19. Measured IF signal of the SSPR, visualizing the phase distortion introduced by phase jitter.

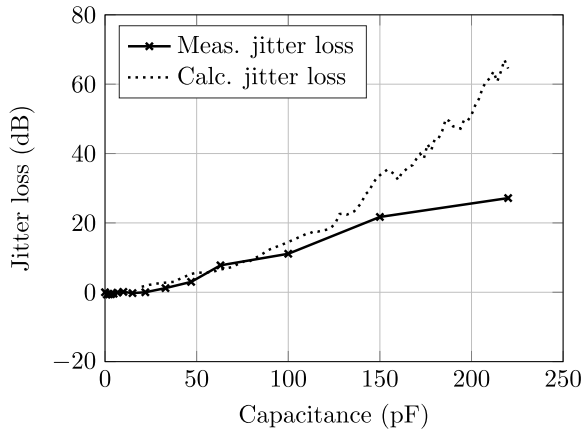

Fig. 20. Measured (solid) and calculated (dashed) jitter loss for various installed capacitor values.

150 pF (blue). The corresponding IF signal for each installed capacitor was acquired with the baseband board. Fig. 19 shows the measured IF pulse without an installed capacitor (black), with 47 pF (red), and with 150 pF (blue). It shows that the phase distortion of the IF signal increases with the rising jitter, but the effect of jitter on the envelope is small, as predicted in Section II-A.

In order to determine the jitter loss (12), the power of the measured IF signal was calculated. For the undistorted reference signal, the measured IF signal without an installed capacitor was used. The resulting jitter loss is depicted with the solid line in Fig. 20. The noise floor of the system limits the lower border of the measureable IF signal power and causes the saturation of the measured jitter loss. The dashed line in Fig. 20 shows the calculated jitter loss according to (23), based on the simulated jitter of the LVDS interface (see Fig. 16) at the measured risetimes (see Fig. 17). The measurement results coincidence well with the prediction based on analytical calculations. For a proper comparison of the measurement results with (23), it must be observed that in the measurements, only the jitter of one clock has been increased. Hence, the jitter value from Fig. 16 has to be divided by $\sqrt{2}$ to match the assumption made in Section II-A.

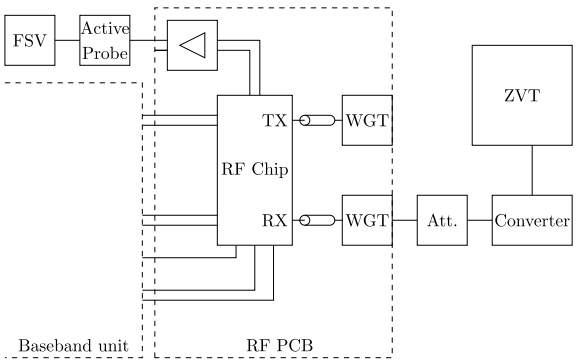

Fig. 21. Block diagram of the measurement setup, which was used in the CW gain measurement.

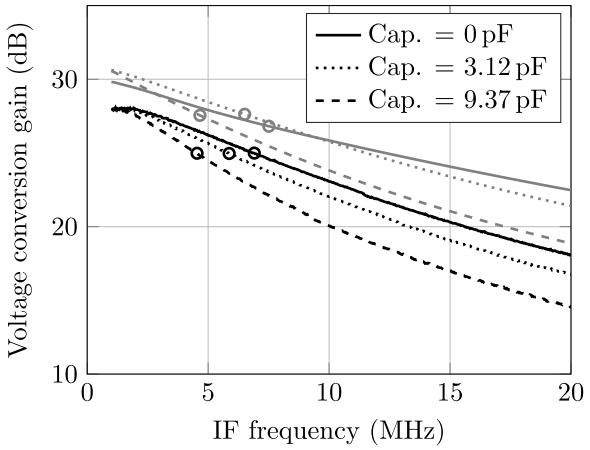

Fig. 22. Measured and simulated gain of the mixer in CW-mode operation. The circles indicate the 3-dB corner frequencies.

C. Receiver Measurement

Similar to the VCO, the mixer was first verified in CW-mode operation using a measurement setup according to the block diagram shown in Fig. 21. The input signal for the mixer was generated with an R&S ZVA-Z110E frequency converter, which was driven by an R&S ZVT20 vector network analyzer. The power level of the converter output was maintained using an Agilent E4416A power meter. The additional attenuator shown in Fig. 21 was used to further reduce the RF input power by 20 dB to avoid the gain compression of the mixer. An R&S RT-ZS30 active probe combined with an R&S high impedance adapter RT-ZA9 was employed to measure the IF signal with an R&S FSV spectrum analyzer.

1) CW Gain: In addition to a functional check of the mixer, this measurement targets the determination of the receiver pulse-conversion gain (34) based on the measurement results. Therefore, not only the conversion gain but also the IF bandwidth (24) of the mixer need to be measured. For this measurement, the output power of the converter was set to -10 dBm, which results in a power level of -38.9 dBm at the mixer input. The frequency of the converter was swept around the LO frequency of the SSPR in order to measure the mixer IF bandwidth. The measurement was carried out with three different settings for the integrating capacitor. Fig. 22 shows the measured gain of the mixer

TABLE IV

MEASURED AND SIMULATED CW GAIN AND 3-dB CORNER FREQUENCY OF THE MIXER AND CALCULATED PULSE-CONVERSION GAIN

Cap.	0 pF	3.125 pF	9.325 pF
Simulated gain	29.8 dB	30.6 dB	30.5 dB
Measured gain	28 dB	28 dB	28 dB
Sim. 3 dB corner frequency	7.5 MHz	6.5 MHz	4.6 MHz
Meas. 3 dB corner frequency	6.9 MHz	5.9 MHz	4.5 MHz
Calc. pulse gain (sim.)	9.4 dB	8.9 dB	5.8 dB
Calc. pulse gain (meas.)	6.8 dB	5.5 dB	3.1 dB

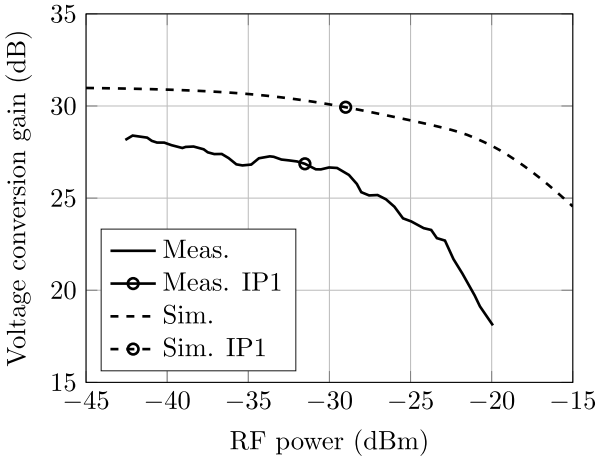

Fig. 23. Measured (solid) and simulated (dashed) conversion gain of the mixer as a function of the applied RF power. The circles indicate the 1-dB compression point.

with the black lines and the simulated gain of the mixer with the gray lines. The markers in Fig. 22 indicate the 3-dB corner frequencies, which are summarized in Table IV together with the mixer gain, where the losses of the RF path have already been corrected. In order to include the input capacitance of the unity gain buffer of 6 pF and the parasitic capacitance of the PCB routing in the simulation, an 8.5-pF capacitor was installed at each of the mixer IF outputs. The simulation results show about 2.5 dB more gain and approximately 10% more bandwidth than the measurement results.

Based on the collected data from Tables III and IV, the pulse conversion gain can be calculated by exercising (34). For the calculation, a capacitor discharge α_{OFF} of 3% is assumed based on simulation results. For the simulation of the pulse-conversion gain, the measured envelope of the RF pulse is used.

2) CW Gain Compression: Next, the input-referred 1-dB compression point (IP1) of the mixer was measured. Therefore, the converter frequency was adjusted to obtain a 1-MHz IF signal and the conversion gain of the mixer is measured for various settings of the output power of the converter. The measurement results are visualized in Fig. 23 together with the results from simulations. The extracted IP1 based on the measurements is −31.51 dBm, where the simulation predicts a slightly better value of −29 dBm.

TABLE V

MEASURED IF SIGNAL PEAK AMPLITUDE AND CALCULATED PULSE-CONVERSION GAIN

Cap. setting	Meas. peak	Corr. peak	Calc. gain	Sim. gain
0 pF	26.1 mV	7.4 mV	6.7 dB	10 dB
3.125 pF	23.9 mV	6.7 mV	5.9 dB	8.4 dB
9.375 pF	18.8 mV	5.3 mV	3.8 dB	5.8 dB

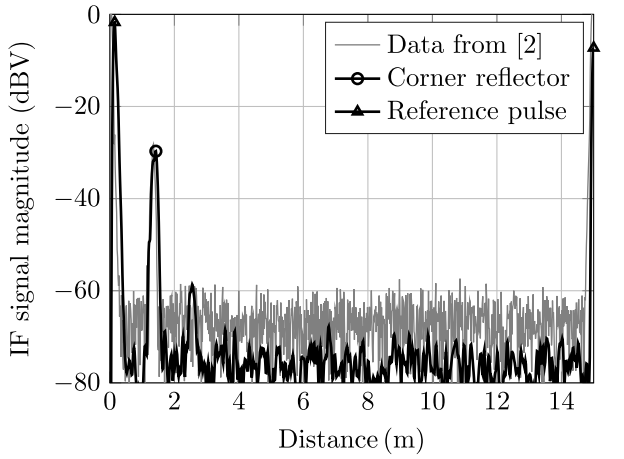

Fig. 24. Measured magnitude of the IF signal of the new pulse radar chip (black) and data from [9] (gray) acquired from interrogating similar radar scenarios.

3) Pulse-Conversion Gain: In order to verify (34), the pulse-conversion gain of the SSPR is measured in the pulsed mode. Therefore, an assembly consisting of a 20-dB waveguide coupler and a Gore coaxial cable is used to establish a connection with a defined attenuation between the TX and RX WGTs. The measured attenuation of the waveguide assembly is 29.2 dB. Together with the losses of the RF PCB, the total path loss is 47 dB. Based on the measured TX power, the calculated voltage level at the RX input of the mixer is 3.4 mV. A pulse radar measurement was performed, and the IF signal was captured using the baseband unit. The measured peak amplitude of the IF signal and the magnitude after correcting for the AD converter gain setting of 11 dB are summarized on the left-hand side of Table V. The calculated pulse-conversion gain is itemized on the right-hand side in Table V, together with the gain obtained from transient simulations for comparison.

It shows that the measurement data and simulation results are consistent and that the results calculated using (34) are congruent with the results from pulse-mode measurement.

D. Radar Measurement

Finally, a radar measurement was carried out with the new pulse radar unit. Similar to the scenario that was used in [9], the pulse radar unit was placed in the anechoic chamber at a distance of approximately 1.3 m to a static corner reflector. The corner reflector had a radar cross section of 18 dBsm. The same clock setting as in [9], with a TX clock of 10 MHz and an LO clock of 10 MHz + 100 Hz, was applied. This results

TABLE VI
POWER CONSUMPTION OF RF BUILDING BLOCKS

Ref.	[12]	[9]	This work
TX (mW)	490	0.825	0.825
LO (mW)	-	0.858	0.858
Mixer (mW)	50	0.234	0.365
Total (mW)	540	1.917	2.048

TABLE VII
COMPARISON WITH OTHER RADAR SENSORS

Ref.	[12]	[1]	[4]	[9]	This work
Technology	SigGe	CMOS	discrete	SiGe	SiGe
Concept	FMCW	Pulse	SSPR	SSPR	SSPR
Frequency (GHz)	79	160	24	79	79
TX power (dBm)	6	4	4	5.5	5.5
Bandwidth (GHz)	3.6	7	1	1	1
RX gain (dB)	26	29.3	-	-13	6
RX NF (dB)	10.2	22.5	-	22.5	18.3
Power dis. (W)	0.724	2.2	-	0.02	0.02

in a time-spreading factor β of 10^5 and an unambiguous range of 15 m.

The magnitude of the measured IF signal is shown in Fig. 24. Compared with [9], an improvement in the SNR of approximately 10 dB is observed. The input-referred noise of the mixer was extracted from the data shown in Fig. 24, which results in 165 nV/$\sqrt{\text{Hz}}$ for the mixer from [9] and 62 nV/$\sqrt{\text{Hz}}$ for this article, respectively.

V. CONCLUSION

The analysis of the SSPR concept presented in this article has highlighted a low VCO start-up phase jitter as one of the key parameters for the SSPR at higher operating frequencies. Furthermore, the theory developed in this article points out that the confluence among the required integrator unit, the mixer, and the load at the IF output is an important factor for the performance of the SSPR. Predictions based on the developed analytical framework match well with circuit simulations and results from measurements. The presented power-efficient integrated realization of the mixer achieves an improvement of 10 dB in the SNR compared with [9], while, concomitantly, the increased RX gain mitigates an external IF amplifier stage. The SNR performance of the developed core system can be improved by adding LNA and PA, respectively, for real application. Furthermore, the curve in Fig. 4 indicates that even higher operating frequencies in the range of 140 GHz should be possible.

For the comparison of the power consumption in Table VI of the individual RF blocks, the work presented in [12] was chosen because of the comparable RF performance achieved in a similar technology and because of the clearly separated power consumption of the individual blocks.

A comparison of typical radar parameters of this article with other radar sensors is shown in Table VII. For the SSPR, the bandwidth is given by the reciprocal pulsewidth $B = 1/T_p$.

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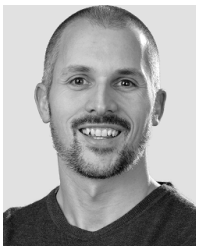

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