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A SiGe HBT BiCMOS 1-to-4 ADC frontend enabling low bandwidth digitization of 100 GBaud PAM4 data

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(Invited Paper)

***Abstract*— Market forecasts for intra and inter data center interconnects predict high growth rates in the upcoming years. This is associated with increasing requirements in terms of costs, power consumption and bit rate per wavelength. Today, PAM4 systems are frequently used at up to 100 Gb/s per wavelength. The next logical step is to double the symbol rate to allow bit rates of 200 Gb/s at the same modulation format and at the same direct detection scheme. Such systems require three-digit gigasample analog-to-digital converters with bandwidths larger than 50 GHz, which are not available today as CMOS components. To extend the bandwidth of CMOS converters, we suggest the use of ADC frontends, which sample and demultiplex the analog input signals simultaneously. At the outputs of such ADC frontends, the signals can then be digitized by parallel converters with lower bandwidth and at a lower conversion rate.**

In this paper we present the circuit implementation of a 1-to-4 ADC frontend in IHP 130 nm SiGe HBT BiCMOS and demonstrate its integration into a 100 GBaud PAM4 transmission system with only 14 GHz of digitizer bandwidth. For optimum performance, the mitigation of intersymbol and interchannel interferences is mandatory in the transmission system. We describe and compare two different receiver DSP architectures for reduction of these interferences and evaluate their performances in electrical and optical back-to-back experiments. Furthermore, we report on transmission experiments over 500 m, 10 km and 40 km SMF at 1550 nm wavelength. With linear equalization we obtained a BER below the HD-FEC threshold of 3.8×10^{-3} and with 3rd order Volterra equalization we even achieved a BER below the KP4 threshold of 2.3×10^{-4}.

***Index Terms*— Optical fiber communication, direct detection, amplitude modulation, Ethernet networks, optical interconnections, data center interconnect, BiCMOS integrated circuits, analog-digital conversion, optical receivers.**

I. Introduction

THE demand for higher fiber transmission capacities is driving research towards increasing channel rates by increasing the symbol rate and/or the spectral efficiency. For short-range transmission systems, four-level pulse-amplitude modulation (PAM4) is a well-established format that transmits 2 bits per symbol while guaranteeing the required maximum transmission reach. By using such formats, many applications have been implemented today at 50 and 100 Gb/s relying on symbol rates of 26 and 53 GBaud [2, 3]. The next higher rate beyond 100 Gb/s is e.g. 200 Gb/s, towards this target first experimental assessments have been reported for PAM4 at symbol rates of 100 GBaud [4].

Most of today's gigabaud transponders base on digital signal processors (DSPs) with digital-to-analog converters (DACs) on the transmitter (Tx) and analog-to-digital converters (ADCs) on the receiver (Rx) side. The electrical bandwidth of the fastest CMOS converters is still low with e.g. a bandwidth of roughly 20 GHz for 92 GSa/s ADCs [5, 6]. At high symbol rates, the converters are typically operated beyond their 3-dB bandwidth limit with remarkable attenuation, resulting in a reduced signal-to-noise ratio (SNR) after conversion [5, 7, 8]. For the implementation of 100 GBaud systems, converters with a Nyquist frequency larger than 50 GHz are required and thus sampling rates need to transcend clearly 100 GSa/s. In addition, to integrate the converters together with the DSP, they have to be implemented in CMOS. Unfortunately, such fast data converters, especially analog-to-digital converters, are not available today despite CMOS nodes have scaled down to 7 nm [9].

State-of-the-art real-time oscilloscopes exploit best-in-class InP semiconductor technologies to enable sample rates beyond

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200 GSa/s and bandwidths beyond 100 GHz [10]. Due to the low integration capability of InP, the implementation of the data digitization however requires multiple hybrid chip sets. Their high costs, high power consumption, large physical size and limited suitability for co-integration with complex CMOS DSPs however prevent their applications in real communication systems.

With continuous advances in semiconductor technologies and high-speed data conversion circuits, >100 GSa/s ADC frontends with up to 60 GHz bandwidth have been proposed in Si/SiGe FDSOI CMOS and SiGe HBT BiCMOS [11, 12, 13]. Such ADC frontends represent an attractive solution to mitigate the bandwidth limitations of current high-speed CMOS ADCs. Optical receivers typically consist of optoelectronic converter circuits with integrated transimpedance amplifiers and a CMOS ASIC incorporating multiple ADCs. For bandwidth extension of these converters, such ADC frontend circuits could be placed in-between the transimpedance amplifiers and the CMOS ASIC. The ADC frontend circuit samples and demultiplexes the input signal of each receiver channel to m parallel lanes. The requirements onto the bandwidth and the sampling rate of the subsequent CMOS ADCs thereby decrease by factor 1/m each. This parallelization approach could simplify the ASIC implementation instead of further bandwidth pushing.

In this paper we present a 112 GSa/s 1-to-4 ADC frontend in IHP 130 nm SiGe BiCMOS with a frequency coverage up to 56 GHz. The performance of the wire-bonded IC module is demonstrated in a 100 GBaud PAM4 transmission system with 200 Gb/s gross data rate. We report on a feasibility experiment for electrical and optical back-to-back (B2B) transmission as well as optical fiber transmissions up to 40 km.

The paper is organized as follows: In section II we introduce the ADC frontend chip. We describe its operation principle, its circuit layout and present details on the chip technology and the packaging. In section III we give more insight into the system setup, in particular, the receiver and the different transmission scenarios from 500 m up to 40 km of single mode fiber (SMF). We emphasize on the implementation of the receiver DSP adaptations for the ADC frontend and elucidate them thoroughly in section IV. To demonstrate the ADC frontend circuit performance as well as the DSP receiver adaptions for 100 GBaud PAM4 reception, we report on electrical and optical B2B experiments in section V and fiber transmission experiments in section VI. Finally, we conclude the paper in section VII.

II. Analog Frontend Chip

The ADC frontend is based on a charge-sampling architecture which is used to mitigate high-frequency SNR degradations due to sampling clock jitter [13]. The fundamental operation principle of a charge sampler is illustrated in Fig. 1. a). A transconductance amplifier with linear V-I characteristic converts the input voltage v_{IN} first into an equivalent input current i_{IN}. The input current charges the integration capacitor C_I and then the sampling of the stored charge is performed. The acquisition of each charge sample is controlled by two switches (S_1 and S_2) and is achieved in three consecutive phases:

1. *Reset (R)*

   At the beginning of the sampling acquisition a discharge of the integration capacitor C_I is performed by closing S_2. The capacitor voltage decreases and the output voltage v_{OUT} increases towards the positive power supply V_{CC}.
2. *Integration (I)*

   After the output voltage has sufficiently settled, S_2 is opened and at the same time S_1 is closed. The input current charges C_I and the capacitor voltage increases. The output voltage decreases as a result.
3. *Hold (H)*

   By opening S_1 and S_2, the hold sample value is obtained. As no discharging currents can flow, the output voltage is held constant until the next sampling phase begins.

The acquisition of the next sample is performed with the same principle: C_I is first reset (R), then charged by current integration (I) and finally decoupled to initiate the hold phase (H). The reset and the integration phases each consume 25% of the full

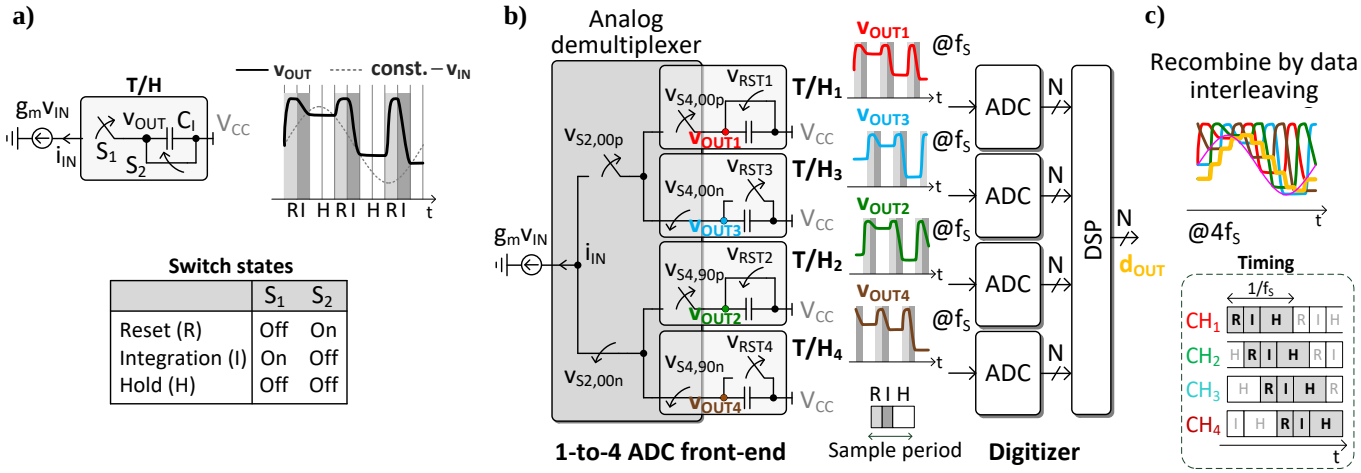

Fig.1.a) Operation principle of a single-core charge sampler. b) Time-interleaved configuration of a 1-to-4 charge sampler. c) The sketches show the sampling of a sinusoidal signal with final reconstruction of it. The table shows the order of the phases of all 4 samplers.

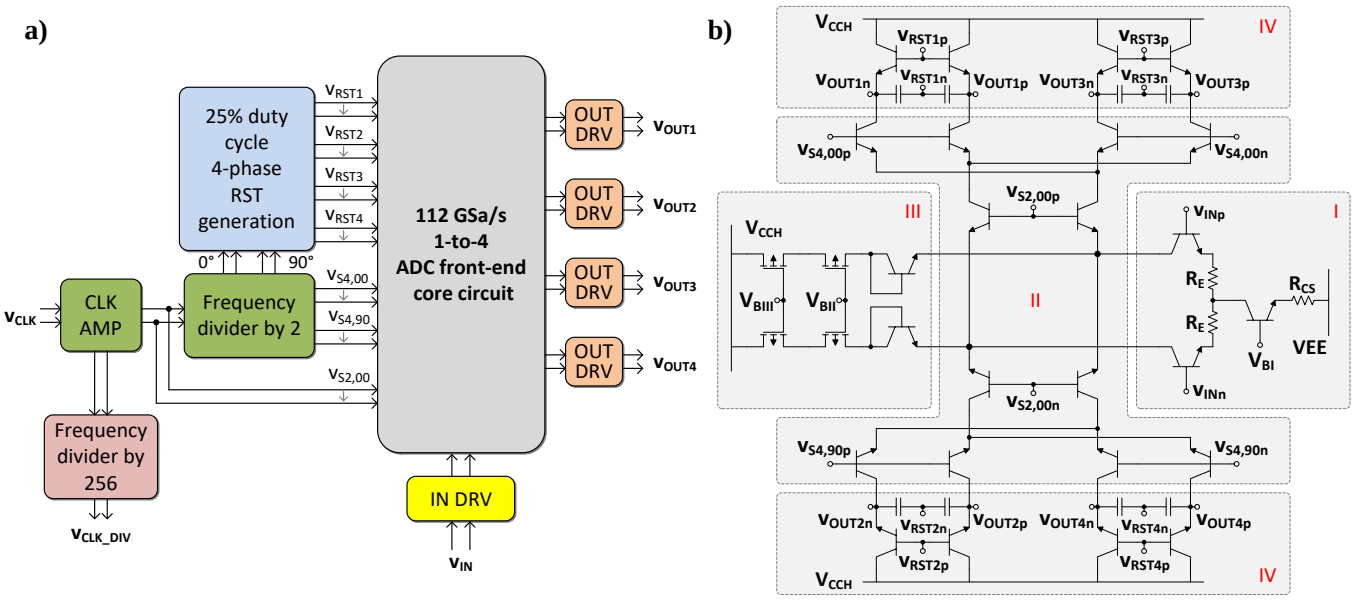

Fig. 2. a) Simplified block diagram of the 112 GS/s 1-to-4 ADC frontend. b) Fully-differential implementation of the charge sampler core circuit in SiGe HBT BiCMOS.

sample period and the hold phase acquires the remaining 50% of time.

By combining four of these samplers with an analog current demultiplexer, time-interleaved operation can be implemented (cf. Fig. 1. b)). The demultiplexer consecutively deinterleaves the input current and subsequent track-and-hold operations (R, I, H) at each output effectively provide samples at four times the channel sample rate. Fig. 1. c) illustrates the four output waveforms of the 1-to-4 charge sampler for a sinusoidal input signal and further depicts a reconstructed version of the input signal after digitization by four sub-ADCs and following data interleaving in a DSP (see orange waveform). The timing diagram illustrates the time delay between the phases of the individual channels, which are one fourth of the sampling period, each.

Fig. 2. a) depicts a simplified block diagram of the 1-to-4 ADC frontend and Fig. 2. b) the schematic implementation of its core circuit in current mode logic. The linear transconductance stage is implemented with an emitter-degenerated differential pair (I). A hierarchical two-level current mode logic tree is used to implement the analog current demultiplexer (II). The first stage of the current demultiplexer is controlled by a half data rate clock ($v_{S2,00}$) and the second stage by two quadrature quarter data rate clocks ($v_{S4,00}$ and $v_{S4,90}$) that are derived by on-chip frequency divide-by-2 operations of the regenerated input clock. To improve the settling of the reset phase, the DC operation point of the demultiplexer's input current is reduced by two matched PMOS current sources (III). As less DC current is integrated on the integration capacitors, lesser charges have to be reset by the four switched emitter follower switches (IV). The control of these switches is achieved by four quadrature reset signals (v_{RST1}, v_{RST2}, v_{RST3} and v_{RST4}) with 25% duty cycles each. On-chip logic operations of the two divide-by-2 clocks ($v_{S,00}$ and $v_{S4,90}$) are used to generate these control signals.

The ADC frontend is implemented in a 130 nm SiGe BiCMOS technology from IHP (SG13G2) and has a chip size of 1.5 mm x 1.0 mm. The technology supports 300 GHz f_T and 450 GHz f_{max} for its heterojunction bipoloar transistors (HBTs) and offers up to 7 metal layers for routing. The IC is mounted in the cavity of a Rodgers 3006 printed circuit board with gold wire bond interconnects (cf. Fig. 3.). The chip is operated at 112 GSa/s with 56 GHz Nyquist bandwidth to support reception of 100 GBaud data signals. Fig. 4. depicts the dynamic range performance of the chip module. Up to input frequencies of 43 GHz (frequency limit of sine wave generator), a spurious-free dynamic range (SFDR) of more than 35-dBc and a signal-to-noise-and-distortion ratio (SNDR) of more than 28-dB are achieved [13]. The total static power consumption of the chip module is ~3.34 W. The demultiplexer core together with the

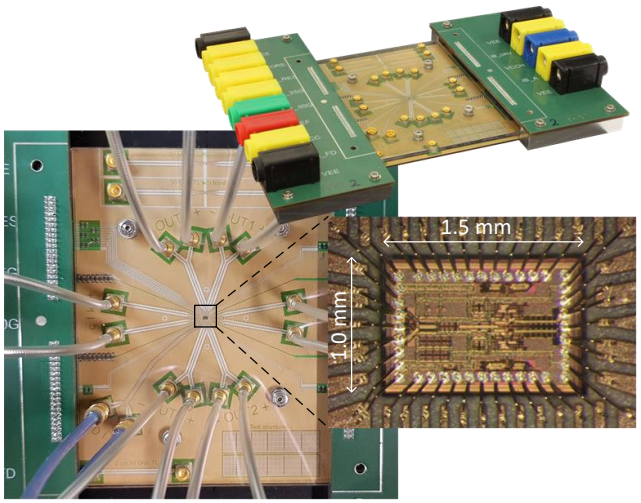

Fig. 3. Photography of the ADC frontend chip module. The die is mounted onto the cavity of a RF printed circuit board.

on-chip control and reset signal generation circuitry dissipate 2.28 W. The clock regeneration circuitry (0.24 W), the frequency divider by 256 (0.55 W) and the four output drivers (0.27 W) consume the remaining 1.06 W. As they are mainly required for chip characterization purposes, they can be omitted in a fully time-interleaved ADC implementation.

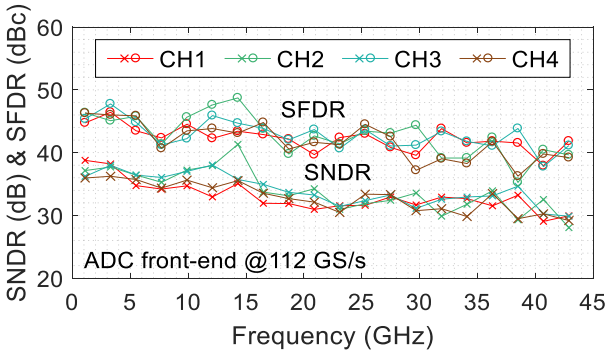

Fig. 4. Measured dynamic range performance of the ADC frontend chip module at a sampling rate of 112 GSa/s [13].

III. System Setup

The feasibility experiments target the demonstration of the proposed ADC frontend in a 100 GBaud PAM4 system for transmission over distances up to 40 km (cf. Fig. 5.). We used a 100 GSa/s DAC to generate the PAM4 data [14, 15]. In a first electrical back-to-back (B2B) experiment we connected the DAC directly to the 112 GSa/s 1-to-4 ADC frontend. With help of a four-channel Inphi 3217 amplifier, we converted the differential output signals of the ADC frontend to equivalent single-ended signal representations. For following data digitization, we then used a 50 GSa/s real-time oscilloscope with a programmable bandwidth between 14 and 20 GHz.

For optical transmission (cf. also to Fig. 5.) we fed the PAM4 signal to a driver amplifier (SHF 807C) and further to a 40-GHz bandwidth $LiNbO_3$ Mach Zehnder modulator. Moreover, we applied a digital pre-emphasis [5, 16] for compensation of the frequency characteristics of all transmitter components. The signal is modulated onto a 1550 nm wavelength carrier supplied by an external cavity laser (ECL) with a maximum output power of 16 dBm. In the receiver we optoelectronically (o/e) converted the signal using an 80-GHz bandwidth photodiode and further amplified it with a SHF 807C amplifier with 23 dB gain only (driver amplifier type) due to the unavailability of a photodiode integrated with a transimpedance amplifier (pin-TIA) at sufficient electrical bandwidth.

For PAM4 systems, typically hard decision forward error correction (FEC) schemes are applied to meet the low power consumption and the low latency requirements of the system application. Typical FEC schemes are the KP4 [17] and the 2nd generation HD-FEC [18] at roughly 7% overhead, each. At a gross symbol rate of 100 GBaud, the gross bit rate is 200 Gb/s and the net bit rates are 189 Gb/s and 187.5 Gb/s, respectively. Further details of the considered FEC schemes are summarized in Tab. 2.

Tab. 2. Details on FEC.

	FEC Over-head	pre FEC BER	Net bitrate @ 100 GBaud PAM4
KP4	5.8 %	2.3E-4	189 Gb/s
HD-FEC	6.69 %	3.8E-3	187.5 Gb/s

The optical transmission system targets standardized transmission distances from 500 m up to 40 km. The chromatic dispersion at 1550 nm wavelength goes beyond the dispersion limit at a symbol rate of 100 GBaud, therefore the application of optical dispersion compensation is mandatory at distances beyond 500 m. At 10-km distance we used a tunable dispersion compensator (TDC) while at 40-km distance the dispersion went beyond the tuning range of the TDC and a dispersion

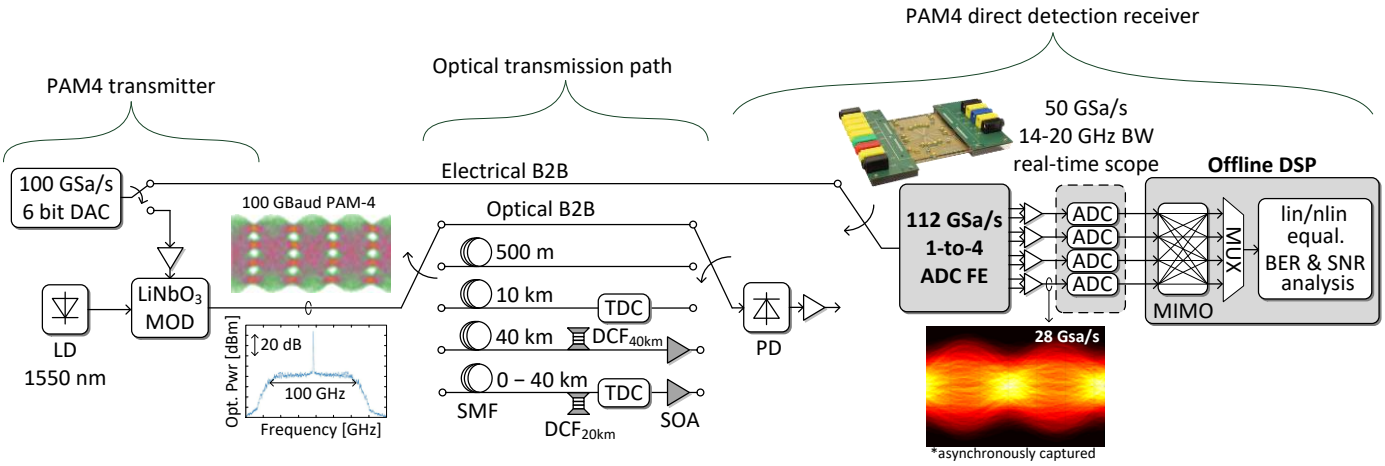

Fig. 5. System setup for electrical and optical B2B experiments as well as for optical transmission over up to 40 km. The insets show the PAM4 eye diagram at 100 GBaud, the optical spectra and the eye diagram at frontend output, where no open eye is visible due to asynchronous sampling.

Tab 3. Details of the transmission systems including optical dispersion compensation.

Distance [km]	ATT_{fiber} [dB]	ATT_{CDC} [dB]	ATT_{total} [dB]	CD [ps/nm/km]
0.50	0.2	-	0.1	8.5
10	2.0	4.0	6.0	0
40	8.0	3.0	11.0	0
0…40	0…8.0	7.0	7.0…15.0	0

compensating fiber (DCF) was required for CD compensation. The application of a DCF requires careful adjustment of its length to the length/dispersion of the transmission fiber due to the low dispersion tolerance. Hence, the combination of a DCF with the TDC is a good alternative to make the system implementation flexible. Furthermore at 40-km distance the attenuation of the transmission fiber and of the dispersion compensation fiber are high in total. Therefore, we added a semiconductor optical amplifier (SOA) with a noise figure of N_F = 8.5 dB. Such SOA could be co-integrated with e.g. the photodiode in the Rx. The SOA increases the power budget drastically and allows for implementation of different dispersion compensation schemes up to 40 km distance. The details on the link and dispersion compensation are summarized in Tab. 3.

After digitization of the signals, the data are parallelized, fed to an adapted DSP and finally re-multiplexed. In the DSP we target the compensation of the electro-optic-electrical (e/o/e) channel and the compensation of further electrical distortions that may come from the four-channel differential-to-single-ended amplifier as well as from the ADC frontend itself. Note that chromatic dispersion (also residual CD after optical CD compensation) cannot be compensated completely after square law detection in the photodiode because it is not a linear distortion anymore.

IV. Receiver DSP

The receiver DSP consists of a first MIMO equalizer (e.g. 4x4) with finite impulse response filters (FIR) in each branch. Such filters may compensate for electrical distortions and may mitigate the chromatic dispersion. Moreover, any intersymbol interference at the frontend input is translated into both, inter-channel and intersymbol interference (ISI and ICI). The MIMO filter requires a suitable parallelization. For operation it needs an implementable adaptation scheme for the tap weights of the filters. For simplification, we resampled the data at the filter input from 50 GSa/s to 56 GSa/s to process the data S_{O1} to S_{O4}, which are synchronous to the ADC-frontend sampler.

In a first receiver DSP implementation (*sampler synchronous out*) we designed a filter block at 56 GSa/s input rate (2 samples per sampling period of the frontend at each sampler output, cf. Fig. 6.). For each output tributary we implemented a separate 4-input 1-output filter to compensate for the ISI and ICI and we need 4 of these blocks in parallel for the 4 tributaries. Note that the overall effort for the DSP is not higher compared to a full serial implementation because due to speed limitations of ASICs serial processing is not implementable and

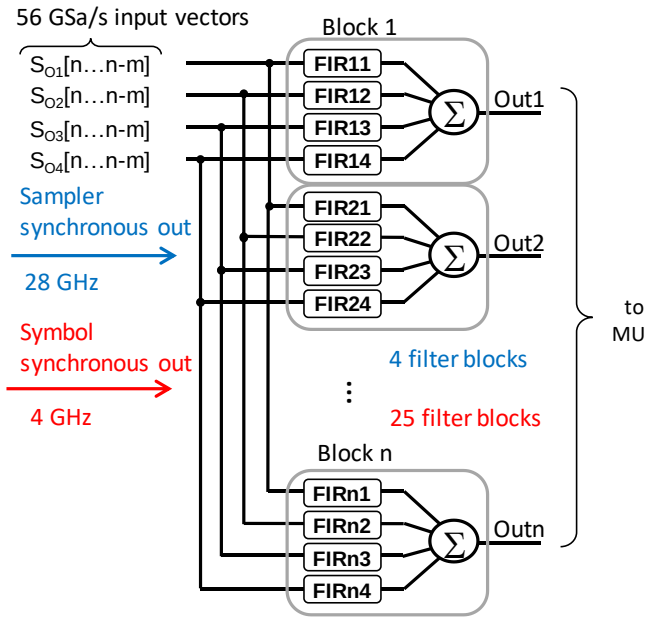

Fig. 6. DSP architecture of the receiver with n-fold (4-fold for sampler synchronous, 25-fold for symbol synchronous) parallelization of the MIMO filter for both implementations.

parallelization is mandatory anyhow. The input data are clocked at 28 GHz frequency through the filter and the output data rate is 28 GSa/s, which is still synchronous to the ADC frontend. In this first implementation the filter blocks are adapted by calibration as typically done in instruments, alternatively training schemes may be implemented, too. After multiplexing we resampled the 112 GSa/s data to 200 GSa/s (2 samples per PAM4 data symbol) and postprocessed them in a final FIR, where distortions from the optical channel can be mitigated and the timing to the data symbols is recovered (cf. Fig. 7.).

In a second implementation (*symbol synchronous out*) we used a filter block for 1/8.33-fold oversampling with a true 100 GSa/s output which is synchronous to the PAM4 data. It requires further parallelization depending on the least common multiple of the sampling period (35.7 ps at 112 GSa/s and 1-to-4 parallelization) and the symbol period (10 ps at 100 GBaud) which is 250 ps in this application. Therewith it relies on a periodicity of 7 sampler periods at the ADC frontend output with 4 channels in parallel to recover 25 symbols at the DSP output. The input data of the DSP are sampled at 56 GSa/s. Note that different sampling rates for the data may be applied in this implementation, e.g. the 50 GSa/s data coming from the scope ADCs could be processed directly without resampling. The data are clocked at 4 GHz frequency through the filters and the output rate is 4 GSa/s each (4 GSa/s ×25 = 100 GSa/s). For each of the 25 outputs we need an individual 4-input 1-output filter block with 25 parallel blocks in total. This architecture allows for a one step signal processing and the symbols can be output directly after the 25:1 MUX. The adaptation of all filter tap weights of all blocks has been implemented by using the decided data (decision directed filter adaptation) and no training or calibration is needed anymore. For performance comparison we implemented a data aided adaptation scheme too.

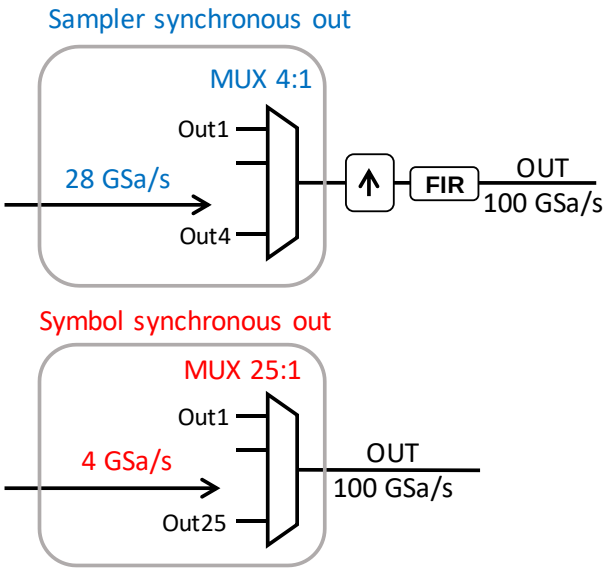

Fig. 7. MUX architecture with optional output filter for both MIMO implementations.

The individual FIR filters are of length 187. Optionally a third order Volterra equalization (187 linear taps, 11 2nd order taps and 11 3rd order taps) may improve the signal quality further by mitigating residual non-linearities, which mainly come from the non-linear input – output characteristics of the electrical amplifiers. Such long filters are especially needed when RF integration is less miniaturized and RF matching is not optimal. Then possible echo distortions can be compensated by filters with large tap count. In possible products, the individual components would be better matched, and the integration further miniaturized, so that filters with a small tap count would suffice. The further signal improvement by non-linear equalization is only effective if non-linear distortions are present. We have mainly detected these in the electrical amplifiers. Due to the interaction of chromatic dispersion, non-linearity and bandwidth limitation, the non-linearity is also smeared on adjacent symbols. In our experiment we showed the successful compensation of this non-linearity with a Volterra filter. Furthermore, we did not observe anomalous error statistics in case of Volterra equalization. In a commercial product the implementation of an amplifier with improved linearity would be preferred to mitigate the need for nonlinear equalization. Finally, the system performance was assessed by bit error counting or by SNR estimation.

V. Back-to-back Experiments

In electrical B2B experiments we measured the SNR at a variable symbol rate of PAM4 data. From 60 GBaud to 90 GBaud the data were generated with an oversampled rate in the transmitter DSP while at 100 GBaud we operated the converter at 1 sample per symbol. At 60 GBaud we measured a SNR of up to 24 dB which dropped down to 18.9 dB at 90 GBaud (cf. Fig. 8.). At 100 GBaud we determined a SNR of 19 dB. These SNR values represent the performance of the entire electrical B2B setup. In the electrical chain there are numerous components limiting the performance: the DAC with an effective number of bits (ENOB) of 4 to 4.5 bits supplying data at an SNR of up to 27 dB at 100 GBaud, the driver amplifier limiting the SNR to 20.5 dB. In the receiver we are concatenating the frontend with a SNR >25 dB, the amplifier with a SNR >30 dB and the real-time oscilloscope with ENOB > 5 bit. From this assessment we draw the conclusion, that the end to end performance is limited more by the transmitter and less by the receiver, where the ADC frontend is the most performance dominating element. The inaccuracy of the individual numbers prevented us from the calculation of a true SNR for the frontend.

In the optical B2B setup, the SNR slightly dropped down further to 18.2 dB. Fig. 9. shows the SNR versus the received optical power. At higher power the SNR is only weakly dependent on the power and saturates. At this operation condition the SNR is mostly dominated by the noise and the distortions

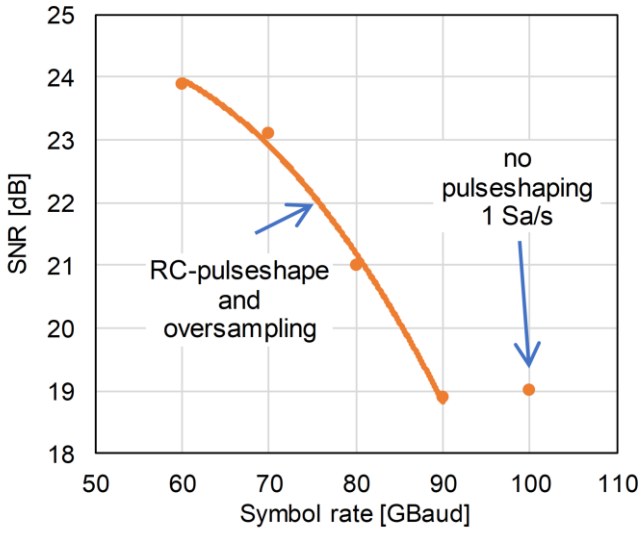

Fig. 8. Electrical B2B measurement of the SNR at variable symbol rate.

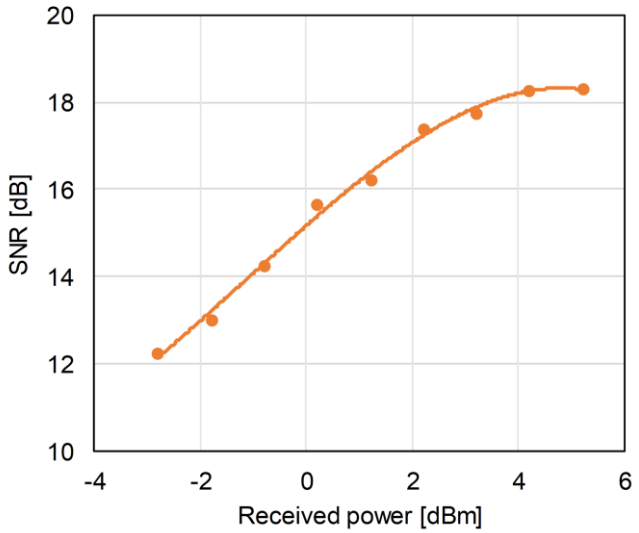

Fig. 9. Optical B2B at 100 GBaud and PAM4 modulation: SNR versus received optical power.

generated in the transponders itself. Below 0 dBm we see the expected linear dependency of the SNR on the received power.

We observed a similar behavior for the dependency of the bit error ratio (BER) versus the received optical power with a flooring of the BER beyond 0 dBm (cf. Fig. 10). In this B2B experiment we compared the different receiver DSP schemes as described in section IV: symbol synchronous output with data aided (DA) filter adaptation, symbol synchronous output with decision directed (DD) filter adaptation and sampler synchronous output with data aided adaptation. The comparison yields the best characteristics for the symbol sync out DD DSP. At KP4 threshold a received power of 3.1 dBm is required while for HD-FEC we need −0.45 dBm input power. When setting the ECL's output power to its maximum of 16 dBm, the maximum fiber launch power after the modulator is 6.1 dBm; the optical power budgets for transmission are 3.0 dB at KP4 threshold and 6.55 dB at HD-FEC threshold. The sampler sync out DSP performs slightly worse with a penalty of 0.2 dB at HD-FEC threshold and 0.4 dB at KP4 threshold. A slightly higher degradation has been observed for the symbol sync out DSP with DA filter adaptation versus DD adaptation with 0.55 dB and 1.5 dB penalty for the HD-FEC and KP4 thresholds, respectively.

Next, we measured the BER at variable received power values versus the electrical bandwidth of the digitizer (ADC), which was adjusted by a built-in brick wall DSP filter in the real-time oscilloscope. From a 20-GHz bandwidth down to 16 GHz the BER has been found to be almost constant (cf. Fig. 11.) and independent on the bandwidth. Below this bandwidth we see a slight increase of the BER. This worsening is almost the same for all 3 launch power values. The BER degradation at 14-GHz bandwidth corresponds to a 0.8 dB power penalty. The 14-GHz bandwidth limit corresponds in first order to a bandwidth of 56 GHz (= 4 × 14 GHz) in case of direct and serial digitization and is quite competitive for 100 GBaud signals.

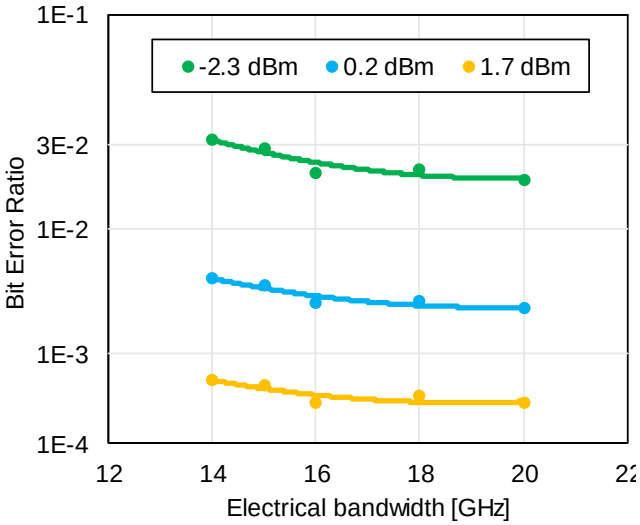

Fig. 11. BER versus the electrical bandwidth of the digitizer (ADC) for three different launch power values. The variable bandwidth has been implemented by an oscilloscope built-in brick wall filter.

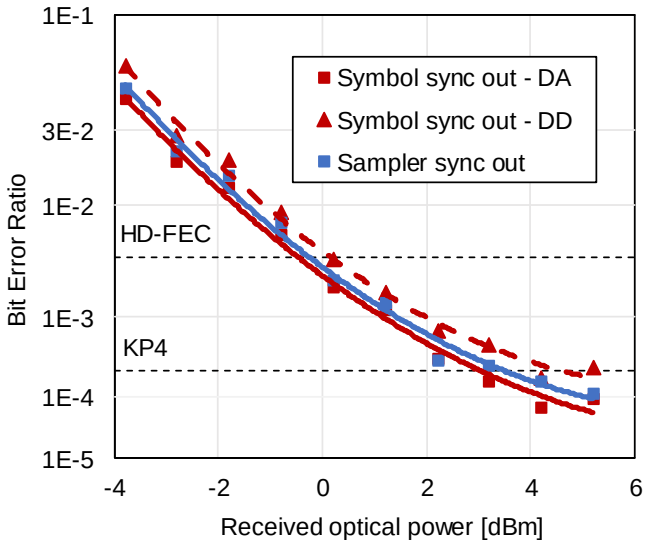

Fig. 10. Optical B2B at 100 GBaud and PAM4 modulation: BER versus received optical power. The dashed lines show FEC thresholds for successful decoding.

VI. Optical Fiber Transmission

Optical transmission experiments were performed at 1550 nm, where chromatic dispersion (CD) of ~17 ps/nm/km causes significant signal distortion and limits the transmission distance. At 500-m distance (datacenter reach – DR) the attenuation of the transmission link is negligible (cf. Tab. 3) and the signal is distorted by chromatic dispersion, only. The linear equalizer was able to mitigate CD to achieve a BER below the HD-FEC threshold (cf. Fig. 12.). By a further increase of the transmission distance we determined the maximum transmission distance at roughly 600 m, which is the chromatic dispersion limit at 100 GBaud and PAM4. By applying the Volterra filter in the receiver we found a BER improvement of half a decade and arrived at the KP4 threshold at 500 m distance. The gain of Volterra equalization with regard to the maximum transmission distance is in the range of 100 m, only.

Next distance target of 10 km (long reach – LR) required optical dispersion compensation as the system was operated beyond its dispersion limit of 600-m distance. With the attenuation of the fiber plus the tunable dispersion compensator with 4 dB of additional loss, we arrived close to the limit of the power budget. At 10 km we measured a BER clearly below the HD-FEC threshold (cf. Fig. 13.). At a further increase of the distance to 20 km we see a huge increase of the BER, which is mainly due to power budget limitations while the CD is compensated adaptively. The distance limit has been determined at 11.5 km. Even in this application the Volterra equalizer improves the BER by half a decade and delivers a distance gain of

roughly 1 km.

At 40-km transmission distance (extended reach – ER) we are limited by the power budget (cf. Tab. 3.), which is lower than the total attenuation. After passing the DCF with 3 dB insertion loss, the SOA increases the power budget to 15 dB (cf. Fig. 5.) and enables transmission at this distance. In a first experiment we compensated the dispersion for 40-km distance and measured a BER far below the HD-FEC threshold for the linear equalizer. The corresponding eye diagram is shown in Fig. 14. The Volterra equalizer improves the BER by slightly more than half a decade. In another experiment we compensated the CD by a concatenation of a DCF and a TDC, where the DCF compensates for the dispersion of 20-km SMF. This is the most flexible setup because it allows for careful adaptation of the CD compensation for all distances. We measured the BER from 0 km up to 40 km (cf. Fig. 15.). The overall attenuation of fiber varies from 0 to 8 dB. At 20 km we have the perfect CD compensation including the dispersion slope.

VII. Conclusion

For digitization of 100 GBaud data signals, ADCs with bandwidths of ≥50 GHz and sample rates of ≥100 GS/s are required. Today no commercial CMOS converter can fulfill this requirement and advanced real-time oscilloscopes are only suitable for lab applications. By employing a 112 GSa/s 1-to-4 analog demultiplexer as an ADC frontend, we propose a receiver component suitable for hybrid integration schemes relying on ADC frontends in combination with CMOS ASICs incorporating ADCs. The frontend is implemented in a SiGe HBT BiCMOS technology. Moreover, we integrated it into a 100 GBaud

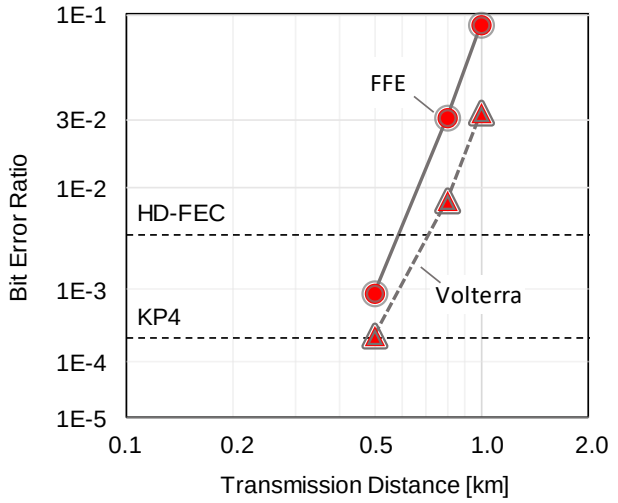

Fig. 12. BER versus transmission distance for data reach (DR) applications.

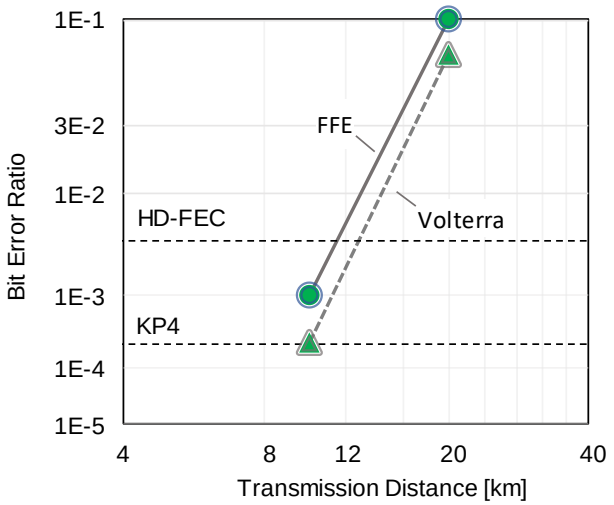

Fig. 13. BER versus transmission distance for long reach (LR) applications. The CD was compensated by a TDC.

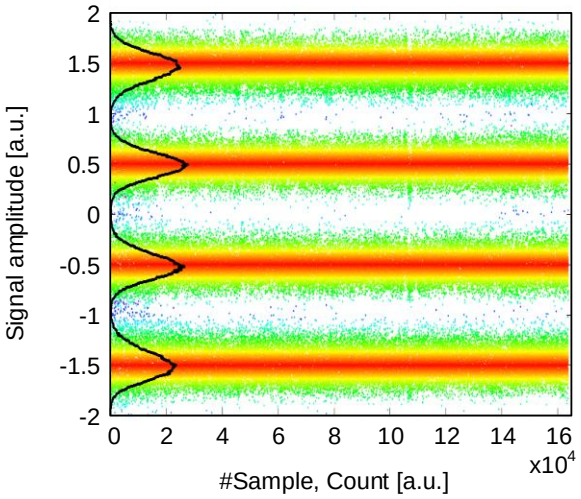

Fig. 14. Constellation and histogram at 40 km distance for a PAM4 signal at 100 GBaud.

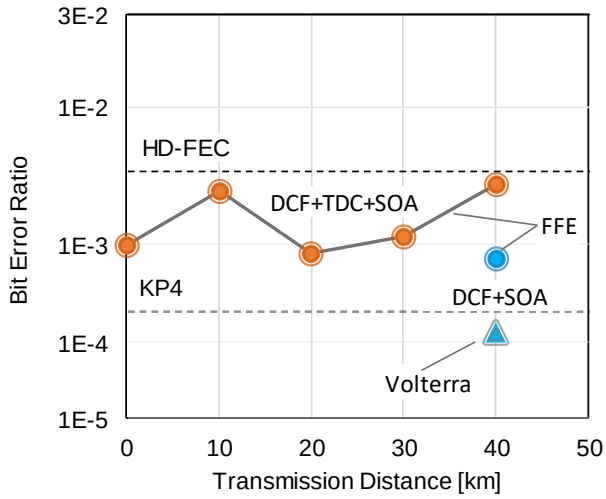

Fig. 15. BER versus transmission distance targeting ER distances, which require optical amplification.

PAM4 transmission system and demonstrate successful data reception at electrical digitizer bandwidths down to 14 GHz at a digitizer sampling rate of 50 GSa/s. Electrical and optical back to back measurements yield maximum SNR values of 19.0 and 18.2 dB, respectively, where the SNR limitation being dominated in particular by the transmitter. The maximum achievable SNR of the overall system drastically limits the transmission margins, especially at the KP4 FEC threshold. Although a performance assessment at this threshold is possible, typical margins known from standardized transmission systems are not available at the current state of the research system.

The receiver requires a well-adapted DSP before multiplexing the data. We compared two different filter architectures and two adaptation schemes, where the symbol synchronous out architecture with data-aided filter adaptation seems to be the best compromise for a transponder implementation.

Optical B2B measurements at 1550 nm wavelength further yield a 6.4 dB optical power margin for transmission, which will be consumed by the fiber transmission itself and by the mandatory optical dispersion compensation at distances beyond 500 m. We successfully demonstrated transmission over 500 m and 10 km, where the degradation is determined by chromatic dispersion and attenuation/noise, respectively. At 40 km we run out of optical power and therefore we applied an additional semiconductor optical amplifier. At 500-m, 10-km and 40-km distances, we measured BERs below the HD-FEC threshold highlighting the circuit capability for single-channel 200 Gbit/s DR, LR and ER transmission with linear equalization. Even operation below KP4 FEC threshold has been demonstrated by further 3rd order Volterra equalization. Short reach systems are typically operated around 1300 nm. At this wavelength, the dispersion is negligibly small and does not require optical compensation, but the attenuation is about twice as high. Assuming a 1300 nm transmitter with same characteristics leading to same power margin, data could be safely transmitted up to 10 km, and at longer reaches the fiber attenuations would be far greater than the available power budget.

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