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A 30.1 mW / µm² SiGe:C HBT featuring an implanted collector in a 55-nm CMOS node

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***Abstract*—This letter deals with the load-pull measurements at 94 GHz of 450 GHz Si/SiGe f_T HBTs. On the one hand the technological modifications performed to improve large signal performances are presented and on the other hand, load-pull measurements are presented after having describing the measurement setup. A state-of-the-art 30.1 mW / µm² Si/SiGe HBT is demonstrated thanks to a layout optimization.**

***Keywords*—Load-pull, SiGe HBT, W-band, implanted collector.**

I. Introduction

W-band is going to be more and more used in the wireless communication market in addition to automotive radars and active imaging. Yet, in order to assume the link between the transceiver and the receiver, high power levels are needed. For several years now, the silicon-made chips have been winning hearts of designers [1] since it is much cheaper than traditionally used III-V components. Especially, BiCMOS technologies can be used in this type of applications thanks to high maximum oscillation frequency f_{MAX} performances to address analog needs and high digital computing power.

The BiCMOS055 technology in production at STMicroelectronics features Si/SiGe Heterojunction Bipolar Transistor (HBT) performances (320 GHz f_T and 370 GHz f_{MAX}) in a 55-nm CMOS node [2]. Nevertheless, technology cost reduction and always-higher performances demand drive STMicroelectronics to evaluate new technological options. A specific focus was put on the f_T improvement in order to decrease the power consumption of applications like optical-circuit designs associated to an improvement of the thermal dissipation. As a part of this work, a major modification of the HBT collector module was performed by replacing the well-known buried layer by a fully implanted collector.

The work presented in this letter is divided in three main parts. Firstly, the technological modifications are explained. In a second time, the load-pull measurements at 94 GHz set-up is described. Eventually, the power performances of the implanted-collector devices are compared to regular ones which are used in B55.

II. Technological modifications

Several technological modifications were introduced to increase f_T performance. First, the thermal budget was optimized to improve HBT f_T performance up to 355 GHz while keeping BiCMOS055 MOSFET models compatibility [3]. In a second part, the standard collector module was replaced by a fully implanted one. The buried layer was replaced by an implanted area also called implanted collector.

The carbon-phosphorous co-implantation showed very promising results in term of defects generation, dopants profile control and performances. The use of specific base crenels structure as displayed in Figure 1 (FEOL HBT layout optimization) led to a remarkable 450 GHz f_T [4] thanks to highly reduced base-collector capacitance and collector resistance. At the same time, f_{MAX} was dramatically reduced down to 160 GHz because of much higher base resistance (Table 1). Finally, it was demonstrated that the number of crenels could dramatically change the trade-off between f_T and f_{MAX} performances.

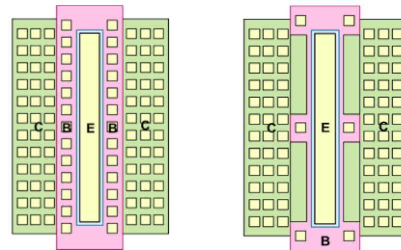

Figure 1 Sketches of SiGe HBT featuring a standard collector (on the left) and an implanted collector (on the right)

III. Measurements Set-Up

The load-pull measurements were performed at the IEMN laboratory. As it can be seen in Figure 2, the bench is composed of six main electronic setups plus a power meter. Firstly, a network analyzer is used to generate a 15.667 GHz signal. Then, a sextupler multiplies the frequency to reach 94 GHz. A variable attenuator controls the input power injected in a power amplifier. This last one is used to have sufficient power level to reach the non-linear behavior of the device under test. A millimetric downconverter is introduced to measure the injected and reflected waves allowing the extraction of the complex S'11 coefficient. Thanks to that, it is possible to extract the input power absorbed by the DUT. At the output of the DUT, a variable impedance tuner is used to adjust the load impedance and hence maximize the performances of power gain G_P, power added efficiency *PAE* or output power following the application P_{OUT}.

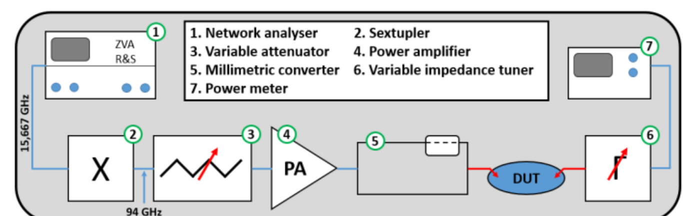

Figure 2 Test bench schematics for load-pull measurements at 94 GHz

IV. MEASUREMENTS

The results reported in this section refer to single-finger 0.2×5.56 µm² CBEBC (drawn dimensions) high-speed HBT and are extracted from on-silicon measurements.

Firstly, it is interested to notice in Figure 3 that the devices featuring an implanted collector (IC on the graphs) either with regulars or X-crenels layouts show quite similar behaviors in terms of P_{OUT}. On the contrary, the B55 device shows a higher slope coefficient but saturates at a lower injected input power level. A 11.0 dBm P_{OUT} at 1-dB power gain compression is obtained for the implanted-collector devices (V_{BE} = 0.86 V, V_{CE} = 1.9 V and $\Gamma_{OPT} = 0.46^{142°}$ for both regular and 5-crenels structures) compared to 8.2 dBm for a reference B55 device (V_{BE} = 0.87 V, V_{CE} = 1.9 V and $\Gamma_{OPT} = 0.43^{148°}$). As expected, the best bias point is the same than the peak f_{MAX}. TEM cross-sections to calculate the effective HBT surface were performed and a remarkable 30.1 mW / µm² was obtained. It represents a 67 % improvement compared to the last state-of-the-art power density published in [5].

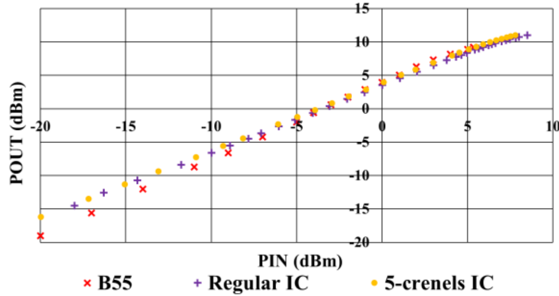

Figure 3 $P_{OUT} = f(P_{IN})$ at 94 GHz for different layouts

This can be mainly explained by the removal of isolation structures (DTI) from the implanted collector devices. Indeed, a junction isolation can be used instead of DTI since the doping region is much closer to the surface compared to a buried layer. As we can see in Figure 4, the temperature in the active part of the component is highly reduced.

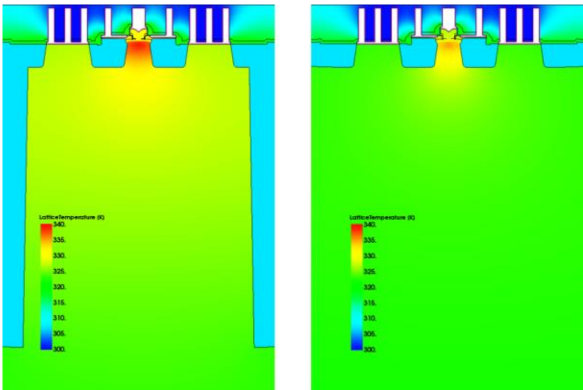

Figure 4 TCAD 2D cross-sections of HBTs internal temperature for a regular collector use (on the left) and an implanted collector (on the right)

Small signal measurements were also performed in order to quantify the impact of the DTI removal on the HBT performances. As it can be seen in Figure 5, both f_T (+ 15 GHz) and f_{MAX} (+ 5 GHz) take advantages from this kind of layouts.

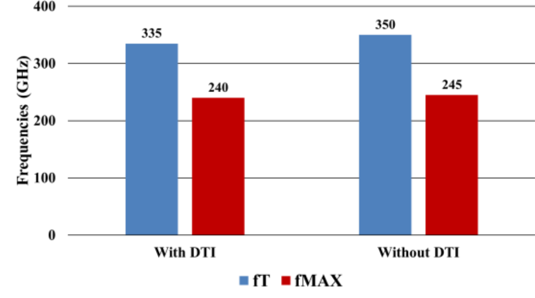

Figure 5 HBT performances depending on the use of DTI structures

The *PAE* of the transistor is a critical parameter and especially at 94 GHz since it represents the ability of the HBT to transform the *DC* power into *RF*. Figure 6 underlines that an implanted-collector device featuring a 5-crenels layout presents the same level of *PAE* than standard B55 ones (22.2 %). On the opposite, a regular implanted collector drops to 16.3 %. That variation can be explained by a more efficient heat drainage with crenels-like structures. Indeed, the silicidation of the collector comes very close to the active part of the component and helps a lot to drain the heat off (a 20 K difference was obtained with TCAD simulations and show a very low thermal resistance in this case). Consequently, much better *PAE* can be obtained.

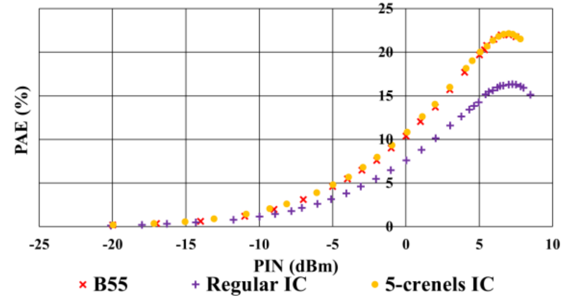

Figure 7 $PAE = f(P_{IN})$ at 94 GHz for different layouts

Figure 6 Temperature = f(depth) for two types of collectors extracted from TCAD simulations

As we can see in Figure 8, the *PAE* of the transistor is highly degraded by decreasing the number of crenels. This parameter goes from 22.2 % for a 5-crenels-layout HBT down to 16.2 % for a 3-crenels structure. This variation can be explained by a lower f_{MAX} due to higher R_B as it can be seen in Table 1. Consequently, it also results in a lower power gain G_P as it can be read in Table 2.

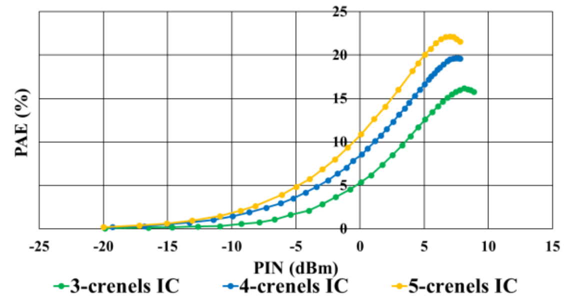

Figure 8 *PAE* at 94 GHz of a $0,2 \times 5,56$ µm HBT featuring an implanted collector depending on its layout

V. Conclusion

To conclude, load-pull measurements have been performed at 94 GHz. Very good *PAE* values (22.2%) were obtained with both devices used in B55 and those featuring an-implanted collector thanks to the implementation of a suitable 5-crenels layout. A state-of-the-art power density of 30.1 mW / µm² was measured for a silicon / silicon-germanium HBT featuring this layout. As a perspective, noise and leakage investigations could be performed to evaluate the impact of the use of carbon in the collector.

Table 1 Synthesis of *DC* parameters

Type of collector	Layout	R_C (Ohms/sq.)	C_{BC} (fF)	R_B (Ohms)
Buried	Regular	27	9.7	24.1
Implanted		294	14.0	26.1
	5-crenels		13.3	35.0
	4-crenels		13.1	38.8
	3-crenels		12.8	43.3

Table 2 Synthesis of small and large signal performances

Type of collector	Layout	f_T (GHz)	f_{MAX} (GHz)	P_{OUT} (dBm)	G_P	*PAE* (%)
Buried	Regular	320	370	8.2	5.4	22.2
Implanted		350	260	11.0	4.25	16.3
	5-crenels	410	260	11.0	4.80	22.2
	4-crenels	420	250	10.8	3.80	19.6
	3-crenels	430	220	10.6	2.70	16.2

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