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Methods for determining the collector series resistance in SiGe HBTs: A review and evaluation across different technologies

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***Abstract* - Many methods have been proposed for the experimental determination of the collector resistance in BJTs and HBTs. In this paper, the most widely used methods are reviewed and applied to SiGe HBTs with a large variety of device sizes fabricated in different technologies and generations, including high-speed and high-voltage transistors. First, the accuracy of those methods, which are based on an extraction from single transistor characteristics, is evaluated from simulated data using a sophisticated compact model and, where applicable, also device simulation. This approach allows the origin of observed inaccuracies or failures of certain methods to be identified. Second, test structure based methods are reviewed and, third, all methods were applied to experimental data. This study and its results provide insight into each method's accuracy, its application limits with respect to a technology, device size and operating range as well as its requirements in terms of equipment and extraction effort.**

***Index Terms* - Bipolar transistors, SiGe HBT, collector resistance, compact modeling, parameter extraction.**

I. Introduction

With advancing technology nodes [1-3] and the respective shrink in vertical dimensions and contact size, the impact of series resistances generally increases. The collector resistance R_C impacts the high-frequency (HF) performance of bipolar transistors through the corresponding time constants [4] and also the DC output characteristics at low collector-emitter voltages. In the literature, many methods have been proposed that aim at accurately determining the collector resistance [5-26]. The latter list of references corresponds to a careful selection of the most popular or promising methods that have been reviewed and applied in this work to SiGe HBTs from a wide variety of process technologies.

There are two fundamentally different approaches for determining the collector series resistance. One approach attempts to extract the resistance directly from measured transistor characteristics after suitably manipulating the terminal parameters and assuming a more or less simplified equivalent circuit [5-22]. The other approach calculates the resistance from its components based on device geometry and sheet resistances and (area or length) specific contact or interface resistances, which are measured on special test structures [23-26]. The results of both approaches are reviewed in this paper.

Typically, when a proposed method for extracting R_C is applied directly to the transistor terminal characteristics, the obtained results are either compared to another method or are validated on a selected device characteristic. Unfortunately, this does not prove whether a correct value for R_C has actually been obtained. As will be shown in this work, the various methods lead to quite a large spread in the results for the *same* transistor. There are many causes for this spread, which will also be discussed in detail.

Generally, all methods for determining transistor series resistances assume a more or less simplified equivalent circuit (EC) and compact model compared to the one actually used for circuit simulation and design. Furthermore, each method relies on a particular DC or small-signal characteristic. Therefore, the result for the extracted resistance generally depends on both the assumed EC and terminal characteristics considered. When inserted into a (production) compact model, the extracted resistance value may give neither the same result for the considered characteristics nor correct results for other device characteristics. This is another reason for using a complete (production-type) compact model for verifying the actual accuracy of an extraction method.

II. Investigated process technologies

Table I provides an overview of the process technologies the various extraction methods have been applied to and are reported on in this paper. Subsequently, just the process names without the company name will be used. Except for the high-voltage transistors of B7HF500hv, the other transistors correspond to the high-performance version of quite different process generations and architectures including both production and prototyping technologies. For each technology, between seven and twenty widely different emitter sizes have been used. This broad range of both HBTs and geometries makes the obtained results representative for existing and future production process technologies. Only npn transistors are considered.

Table I: Overview of the most relevant parameters (at $T = 300$K) for characterizing the investigated SiGe HBT process technologies from ST Microelectronics (ST), Infineon (IFX), and Innovations for High Performance Microelectronics (IHP). The variables have their usual meaning; b_{E0} is the emitter window width (i.e. the width of the poly-to

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mono-silicon interface between the base-emitter spacers). Note that B5T, B7HF500 and SG13G2 are prototyping processes.

process \ parameters	f_T, f_{max} (GHz)	BV_{CE0} (V)	b_{E0} (µm)
IHP SG13G2 [27]	300, 480	1.6 ... 1.8	0.09 ... 0.74
ST B5T [28]	320, 350	1.4	0.12 ... 0.16
IFX B7HF500hs [29]	250, 300	1.8	0.13 ... 2.15
ST BiCMOS 7 [30]	55, 200	3.3	0.23 ... 1.43
IHP SGB25V [33]	75, 95	2.4	0.42 ... 1.50
IFX B7HF500hv	50, 180	4.0	0.17 ... 0.29

III. Single Transistor Based Extraction Methods

This section covers those extraction methods that are based on measurements taken directly from just a single transistor. These methods can be verified by applying them to a compact model, in which R_C is known exactly (and is designated below as "actual" value). In addition, device simulation results are used where necessary support the explanation of limitations of a particular method.

Since all extraction methods are based on a strongly simplified model as shown in Fig. 1, any reasonably sophisticated physics-based compact model (CM) typically used in industry that includes the physical effects involved for a particular extraction method and reproduces the measured terminal characteristics sufficiently well is suitable for generating the reference data. The CMs mainly used in industry differ by their description of the internal (epi) collector region. Here, the SPICE Gummel-Poon model (SGPM) with its bias independent collector resistance seems to be least suited for this investigation. The bias dependent conductivity modulation and space-charge limited current flow in the (entire) epi region (i.e. between BC junction and buried layer) are described in VBIC [31] and MEXTRAM [32] with a separate nonlinear controlled current source in an internal BC branch, while the corresponding high-current effects are included HICUM via the GICCR in the transfer current source directly, i.e. without an additional internal BC branch [34]. Notice that none of these models describes an internal collector resistance R_{Ci} (see next paragraph) directly. For evaluating the extraction methods, only the same simplified model in Fig. 1 that has been used in the original description of the various methods has been applied.

In this work, HICUM/L2 was employed as a vehicle for generating reference terminal characteristics. The complete set of model parameters were carefully determined from a geometry scalable extraction procedure using transistors with different size and dedicated test structures. For each process technology, the resulting model characteristics were verified over a wide range of bias, frequency, temperature and device geometry (e.g. [35, 36, 37, 4]). Capturing the essential features of fabricated transistors with parameters that are believed to be reasonably physics-based is a necessary condition for the purpose of this work. HICUM/L2 with its quite sophisticated EC includes all known physical effects of even the most advanced SiGe HBTs (e.g. [38, 39]).

All R_C extraction methods assume a much simpler EC, the most complicated one being shown in Fig. 1, since it includes relevant elements of the parasitic substrate transistor. Fig. 1 also defines the various elements and variables used later in this work. . Since all CMs contain a bias independent external collector resistance R_{Cx}, the node C' here just separates R_{Cx} from the epi collector region with its strongly bias dependent resistance R_{Ci}. The physical location of C' has been defined differently in both the compact modeling and extraction literature. As can be seen in Fig. 2, the electron quasi-Fermi potential φ_n changes its shape significantly between the low to high injection regime. In all cases though the value of φ_n at the end of the collector epi region sufficiently far in the buried layer equals the 1D collector terminal potential, which can be clearly related to the terminal potential of a real structure via the *external* collector resistance R_{Cx}. Trying to define C' at the BC junction would not give the internal collector resistance R_{Ci} due to the drop of φ_n across the BC SCR, especially at low injection. Defining C' somewhere in the epi-collector would become arbitrary at high current densities e.g. when the slope of the electric field in the collector becomes zero) or high C E voltages (when the epi collector is fully depleted). Hence such a definition would also not yield any uniquely defined resistor element R_{Ci} for a compact model as can be observed from φ_n at high injection, which exhibits a changing slope (and thus differential resistance) across the entire epi collector . As was shown in [32], these issues can be circumvented by including R_{Ci} in the transfer current formulation which then allows to define C' such that it is connected with the terminal node C through just R_{Cx}. The latter includes the sinker resistance, contact resistance and lateral resistance component of the buried layer.

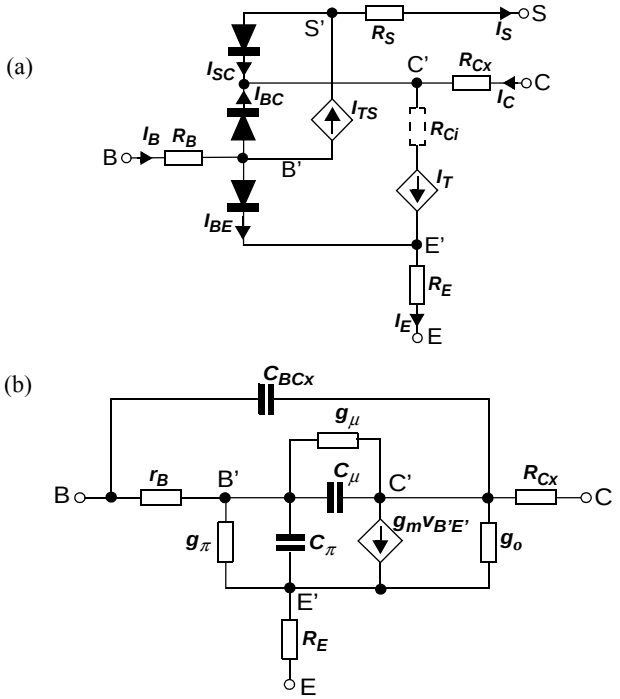


Fig. 1. Equivalent circuit assumed for determining R_C by the methods considered in this work: (a) DC EC with relevant substrate transistor elements and (possibly used) internal collector series resistance R_{Ci}; (b) small-signal EC without substrate transistor and R_{Ci}. For some methods, even more simple EC versions have been used.

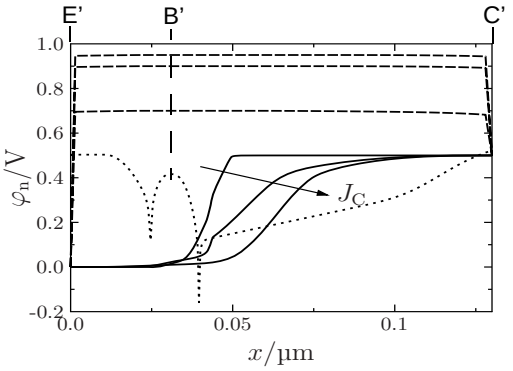


Fig. 2. Electron quasi-Fermi potential obtained from device simulation of a 1D npn transistor operated at different collector current densities J_C and V_{CE} = 0.5 V. The arrow indicates increasing current densities. The dotted line shows the doping profile, which corresponds to that of a SiGe HBT with about 250 GHz transit frequency.

In this section, the basic principle of each extraction method is explained briefly, supported by showing the typical characteristic from which R_C is obtained. The results of each method, applied to the compact model, are then displayed in a single plot for all investigated technologies and compared to the actual value. This provides a quick overview of trends regarding the accuracy as a function of size and technology. The causes for an observed failure or exceptional agreement will then be discussed along with the sensitivity of a method with respect to relevant physical effects and the resulting consequences for selecting the proper bias or frequency range.

A. Open-emitter method

This method is based on the flyback approach originally proposed in [5] for open-collector operation and later on also published in [6, 7]. By interchanging collector and emitter and biasing the transistor in inverse operation, R_C instead of R_E is attempted to be determined from the current dependence of the external EC saturation voltage $V_{ECs} = V_{EC}(I_E = 0)$[1],

$$V_{ECs} = V_{E'C's} - R_C I_C , \qquad (1)$$

with $I_C = -I_B$ in Fig. 1(a) due to the open emitter and, in the classical case, also open substrate terminal. As known from the open-collector method [22, 40], the internal EC voltage is bias dependent and can be well approximated by [22]

$$V_{E'C's} = V_{E'C'\mu} \ln\left(1 + \sqrt{\frac{I_B}{I_{rEs}}}\right). \qquad (2)$$

Here, $V_{E'C'\mu}$ and I_{rEs} are two parameters that are fitted to the measured curve (1) in addition to R_C. A discussion on how to use this method properly and its limitations was already given in [40]. Connecting the substrate terminal (i.e. $I_C = -I_B - I_S$) and forward biasing the SC junction yields similar results.

Fig. 3(a) shows examples for typically observed curvatures of the terminal voltage V_{ECs} and also the correction voltage $V_{E'C's}$ along with the corresponding fits. The (1D) device simulation clearly demonstrates the necessity of the correction as well as the suitability of eq. (2) for describing the curvature also for the open-emitter method. According to Fig. 3(b), the fit results in a bias dependent resistance R_C. This is due to the (very) high forward bias of the BC junction, which leads to a modulation of the resistivity of the internal (lower doped) collector region and contributes additionally to the bias dependence of the measurable V_{ECs}. Without knowing the actual bias dependence of $V_{E'C's}$ only the constant portion R_{Cx} can be extracted with this method. This is confirmed by the device simulation results with and without an externally connected R_{Cx}. Its value can be recovered very accurately at sufficiently high currents by using eq. (2) in eq. (1).

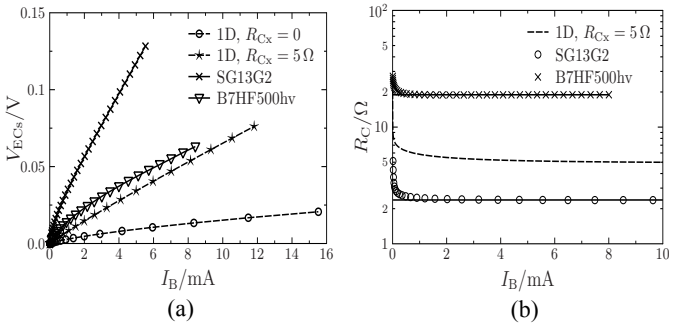


Fig. 3. (a) Current dependent terminal voltage V_{ECs} from *1D mixed-mode*[2] *device simulation* (o and *) and *measurements* of SG13G2 (x) and B7HF500hs (∇) for an open substrate along with the fit according to eq. (2) (lines). In the mixed-mode device simulation R_{Cx} = 5 Ω was added externally. (b) Results from fitting (1) and (2) to the data of the device simulation (dashed line) and of the compact model (symbols) with the solid lines indicating the actual value.

Fig. 4 shows the results of this method for different process technologies and emitter sizes. Very accurate values for R_{Cx} are obtained. The results are not impacted by self-heating due to the small CE voltages. A possible cause for failure may be that eq. (2) is based on a 1D analysis and ignores the impact of the injection across the highly forward biased *external* BC junction. Also, the analysis in [22] assumes no BC barrier and thus yields only a rough approximation for advanced HBTs. A drawback of this method is that it requires separate access to the emitter node of the transistor, which is not possible for standard integrated RF test structures in GSG pads.

1. Note that eq. (1) represents the generally used formulation in which C' is not (well), i.e. not as clearly, defined as in Fig. 2.

2. Here, mixed-mode refers to numerical device simulations combined with a circuit simulation for adding external elements.

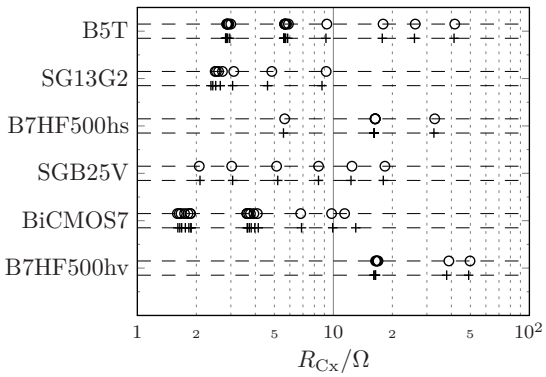


Fig. 4. Comparison of the results (in log scale) of the open-emitter extraction method for different process technologies. For each technology, the lower row (crosses) represents the actual value as a reference while the upper row (circles) shows the extracted results.

B. Forced-beta methods

First of all, these are all DC methods so that the use of the small-signal current gain β in the literature is misleading and should be replaced by the DC current gain. The method itself is an extension of the open-collector method for determining R_E [5] by allowing a non-zero collector current $I_C > 0$. The transistor is operated in saturation such that the measured CE voltage is given by

$$V_{CE} = V_{C'E's} + R_C I_C + R_E I_E \ . \tag{3}$$

Originally [9, 11], the internal CE saturation voltage $V_{C'E's}$ was calculated from an Ebers-Moll model, but an improved expression can be obtained from the SPICE Gummel-Poon model (SGPM) (e.g. [10, 13])

$$V_{C'E's} = V_T \ln\left(\frac{\frac{1}{q_B} + \left(1 + \frac{I_C}{I_B}\right)\frac{1}{B_{ri}}}{\frac{1}{q_B} - \frac{1}{B_{fi}}\frac{I_C}{I_B}}\right) . \tag{4}$$

Here, B_{fi} (B_{ri}) is the *ideal DC* forward (inverse) current gain in CE configuration, defined by the ratio of the transfer *saturation* current to the BE (BC) diode *saturation* current; q_B is the bias dependent normalized "base" charge in the SGPM.

In the original method [9, 11], q_B equals one and $V_{C'E's}$ is assumed to be bias *independent* by fixing the value for the actual DC current gain $B_f = I_C/I_B$, which coined the name of this method. In [10], it is attempted to determine $V_{C'E's}$ at low injection, while in [13] the influence of $q_B > 1$ is realized. There, it is argued that measurement and extraction should be performed at "sufficiently" low injection to avoid carrier injection into the collector so as to keep q_B and thus $V_{C'E's}$ bias independent. Then, R_C is determined from the slope of $V_{CE}(I_C)$ according to eq. (3):

$$R_C = \frac{\Delta V_{CE}}{\Delta I_C} - R_E\left(1 + \frac{1}{B_f}\right) . \tag{5}$$

However, a low current level makes it difficult to accurately measure the voltage drop across R_C. Note, that the emitter resistance R_E was either neglected [9] or has to be known from a previous extraction step [10, 11, 12, 13].

Various methods for acquiring the data have been suggested. Originally, in [9, 11] a set of (I_B, V_{CE}) curves at constant I_C was displayed on a curve tracer, from which the points (V_{CE}, I_C) at constant B_f were determined. In [12], the "offset" $V_{C'E's} + R_E I_E$ in eq. (3) was determined from the minimum of the $V_{CE}(I_C)$ curve at constant B_f calculated by the SGPM. A more accurate and, especially with modern data acquisition software, convenient method is to determine the (V_{CE}, I_C) points from data of the output characteristics by linear interpolation of the corresponding $B_f(V_{CE})$ curves [13]. The latter curves also quite clearly indicate the suitable extraction region.

In all methods discussed above, the internal BC junction is slightly forward biased and carrier injection into the collector is avoided explicitly in [13]. Thus, the measured resistance R_C corresponds to the sum of R_{Cx} and the resistance R_{Ci} of the undepleted collector region. Employing this total R_C in the SGPM indeed improves its output characteristics [13] while in HICUM the description of the internal collector region is already included in its transfer current [48, 38] such that the determination of only R_{Cx} is required. In fact, this also applies to MEXTRAM and VBIC since their parameters for describing the epi collector are determined from separate characteristics.

In contrast to the methods described above, the measurements in [14] are performed at $V_{BC} = 0$ (i.e. $V_{CE} = V_{BE}$) and at (very) high injection, such that the voltage drop across R_C forces the internal transistor into saturation. Then, R_C *and* R_E are determined simultaneously from

$$(R_C + R_E) + R_E\frac{I_B}{I_C} = \frac{V_{BE} - V_{C'E's}}{I_C} \tag{6}$$

by plotting the r.h.s. versus I_B/I_C; the bias dependence of $V_{C'E's}$ is calculated by a fitting equation with previously determined parameters B_{fi}, B_{ri}, and the SGPM knee current I_{KF} describing high-current effects in q_B. Thus, R_C depends on the accuracy of both these parameters and the SGPM at high injection, where the accuracy of latter is very limited though. Moreover, applying this method requires a floating substrate since otherwise a portion of the base current flows toward the substrate which would make constant I_C/I_B difficult to maintain. Note that a non-zero V_{BC} can also be applied and included easily into eq. (6), e.g., to reduce the level of carrier injection into the collector.

Fig. 5(a) shows examples for typically observed curvatures of $V_{C'E's}$ and V_{CEs}. It is evident from both the compact model and (1D) device simulation that the assumption of $V_{C'E's}$ being bias independent is invalid at high injection. Thus, the slope of V_{CEs} is not an accurate representation of the series resistances. Further, inserting the normalized weighted hole charge into eq. (4) led to negative values in the denominator even for medium injection. It is therefore not included in the curve for eq. (4).

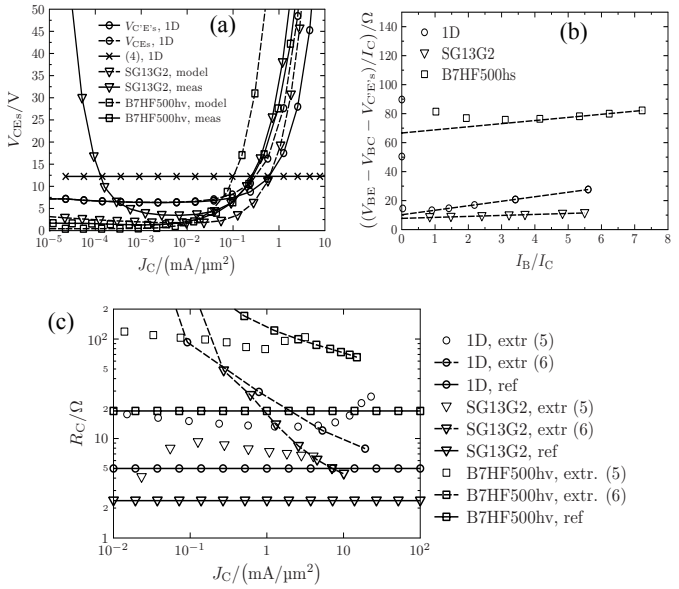


Fig. 5. (a) Bias dependent CE saturation voltages V_{CEs} (o, dashed line), $V_{C'E's}$ (o, solid line), and eq. (4) (x, solid line) all from 1D device simulation with externally added R_{Cx}=5Ω and R_E=3Ω as well as compact model (dashed lines with symbols) for SG13G2 (∇ and and B7HF500hv (□) with corresponding measurement (solid lines with ∇ , □). (b) R.h.s. of eq. (6) vs. I_B/I_C (symbols) along with the corresponding LSQ fit (dashed lines). (c) Resulting R_{Cx} for the cases in (a) according to eq. (5) (o, ∇ , □) and eq. (6) (dashed lines with o, ∇ , □), obtained from LSQ fits of five bias points centered around a varying I_C value. The (bias independent) reference values are marked as solid lines. Note that for evaluating eq. (6) J_B is used rather than J_C.

Fig. 6 shows the results of this method using eq. (6) for different process technologies and emitter sizes. The results improve with increasing b_{E0} due to the increase of the voltage drop across R_{Cx}, which leads to stronger saturation. The deviations observed in Fig. 6 are caused by (i) underestimation of $V_{C'E's}$, (ii) the influence of the parasitic substrate pnp transistor (which has been included in the compact model), and (iii) the impact of the non-depleted conductivity modulated internal collector region. The older versions [10, 12, 11] of this method yield poor results for both high-voltage and high-speed transistors which is attributed to the invalid underlying assumption of a constant internal CE saturation voltage $V_{C'E's}$.

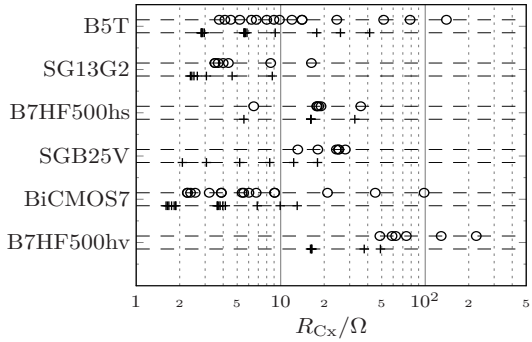


Fig. 6. Comparison of the results (in log scale) of the forced-beta method according to eq. (6) for different process technologies. (Same legend as in Fig. 4.

C. Substrate transistor based methods

These methods all require the substrate terminal to be accessed separately for measuring I_S (cf. Fig. 1(a)). The various proposed methods differ by their operation of the npn and its substrate pnp. In principle R_{Cx} can be measured from the voltage difference $V_{CC'}$ between the collector terminal node C and the internal collector node C' in Fig. 1(a).

In [16, 17] the location of C' in the actual transistor structure is discussed in great length. It is claimed in [17] that operating the pnp at forward bias (i.e. with the npn base region as its emitter) allows to extract the total collector resistance including R_{Ci}. As concluded from Fig. 2 though, C' should be located at the buried layer end of the internal collector regardless of the npn forward bias. This was also concluded in [16] after a quite lengthy discussion. As a consequence of the location of C', substrate transistor based methods only yield R_{Cx} but not R_{Ci}.

The method proposed in [16] attempts to determine the potential at C' via measuring the DC transfer current $I_{TS} = I_S$ of the forward biased substrate pnp transistor. Keeping I_S constant forces the internal emitter-base voltage of the pnp, $V_{E'B'pnp}$ (= $V_{B'C'npn}$), to remain constant, while sweeping I_C of the npn independently. From the respective voltage loop in Fig. 1(a) one obtains

$$\boldsymbol{V_{EBpnp} = V_{BCnpn} = V_{B'C'npn} - (R_{Cx} - R_B/B_f) I_C}. \qquad (7)$$

R_{Cx} is then determined from the slope of the measured npn terminal voltage V_{BCnpn} vs. measured collector current I_C and a correction by R_B/B_f using previously determined parameters. The latter correction is negligible for advanced HBTs with high B_f and low R_B. According to Fig. 7, eq. (7) behaves quite linearly. The internal voltage $V_{B'C'npn}$ decreases slightly due to self-heating, which causes an error in determining R_{Cx}.

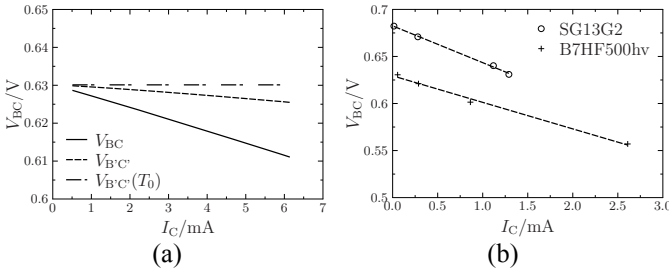


Fig. 7. BC terminal voltage vs. collector current for constant substrate current. (a) SG13G2 compact model data showing in addition the internal voltage $V_{B'C'}$ with and without self-heating included. (b) Measured data for SG13G2 (o) and B7HF500hv (+) with LQS fit (dashed lines).

Fig. 8 shows the results of this method. Note that the SGB25V transistors are not included in the evaluation due to the lack of suitable structures. The impact of self-heating can be especially seen for B5T for which the error drops from 40...50% down to 2...3% when turning self-heating off. Overall, the method yields quite good results with errors in the range of 10% if self-heating can be kept low. A detailed analysis of the temperature behavior shows that error compensation can be achieved by choosing I_S as high as possible.

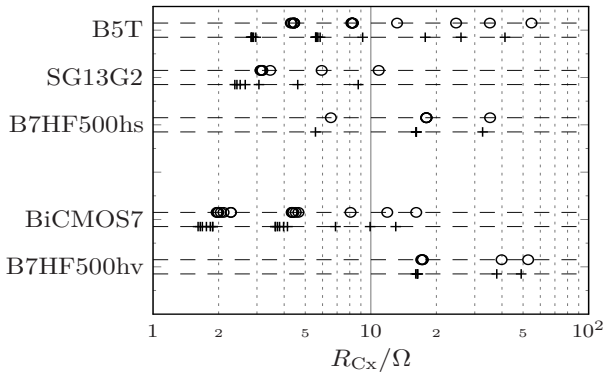


Fig. 8. Comparison of the results (in log scale) of the substrate-transistor based method proposed in [16] for different process technologies. (Same legend as in Fig. 4.)

In [17] the npn is biased in forward active operation, while its collector current I_C passing through R_{Cx} is used to turn on the substrate-collector junction by driving C' to a lower value and operating the substrate pnp in inverse (i.e. upwards) operation, i.e. with holes from the substrate injected into the buried layer. Then, according to the EC in Fig. 1(a), the pnp's collector-base voltage is given by (note that $I_S < 0$)

$$V_{CBpnp} = V_{SCnpn} = V_{S'C'} - R_S I_S - R_{Cx} I_C \,. \tag{8}$$

Keeping I_S (and thus $V_{S'C'} - R_S I_S$) as well as V_C at a fixed value while sweeping I_C by changing V_{BEnpn}, one obtains R_{Cx} from the slope of $V_{SCnpn}(I_C)$. An example for the resulting R_{Cx} vs. I_C curve is presented in Fig. 9(a).

Originally, a reasonably large V_{CE} ($\approx V_{CS}$) was supposed to be applied to turn off the substrate transistor for low I_C and than have it turned on due to the voltage drop across R_{Cx}. However, the method works better for very low V_{CE} (e.g. 0.2 V) which strongly reduces self-heating, but also decreases the slope and the suitable voltage range. In this case, the substrate transistor is heavily turned on and carrier back-injection into the substrate impacts the result [4] (which has not been included here in the model).

The method gives acceptable results for most of the investigated technologies (cf. Fig. 10(a)) with relative deviations below 50%, except for B5T where the range of relative errors is [15-115]%. An emitter size dependence of the error was not observed, but may occur for significant current crowding in the buried layer along the CS junction. Switching self-heating off reduces the error to below 5% and yields an almost bias independent result (cf. Fig. 9(a)).

In [16], the npn is operated in forward saturation mode, while the pnp works in forward active mode by negatively biasing the substrate potential. As in [17], the voltage drop across R_{Cx}, caused by the I_C of the npn, is used for turning on the pnp:

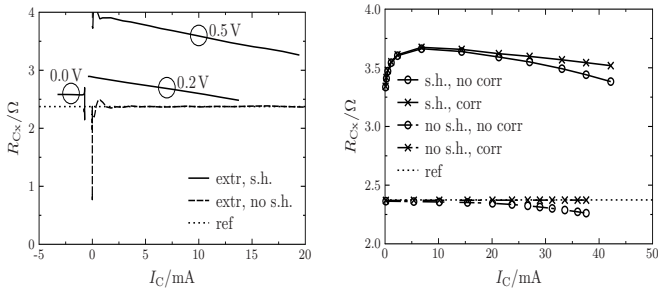
$$V_{E'B'pnp} = V_{B'C'npn} = V_{BC} - R_B I_B + R_{Cx} I_C \,. \tag{9}$$

Varying I_C via reducing V_E in Fig. 1(a) at constant V_{BC} and assuming the substrate current related components to flow entirely through the external base gives after subtracting two such bias points

$$R_{Cx} = \frac{m_{Sf} V_T \ln(I_{S2}/I_{S1}) + R_{Bx}(I_{B2} - I_{B1})}{I_{C2} - I_{C1}} \tag{10}$$

where $V_{E'B'pnp,2}$-$V_{E'B'pnp,1}$ was replaced by $V_T \ln(I_{S2}/I_{S1})$ using the measured substrate currents. This evaluation is performed in the region where I_S exhibits for increasing V_{BEnpn} a straight line (in semi-log scale) with the slope $1/(m_{Sf} V_T)$. Taking the difference of measured points obviates the need for measuring and modeling the $I_S(V_{EBpnp})$ characteristic. Operating the npn deep in saturation allows to reduce V_{CEnpn} and hence self-heating significantly compared to the method in [17]. Debiasing the pnp through the voltage drop across R_{Bx} can be avoided by keeping V_{CEnpn} as low as possible. Otherwise and also for transistors with a low forward current gain, R_{Bx} has to be known.

Fig. 9(b) shows examples for typically observed results. The very high I_C needed for turning on the pnp causes significant self-heating, while the error from the voltage drop across R_{Bx} is relatively small. The method as proposed in [16] gives results with relative errors up to 50% for all processes and even higher for B5T. If self-heating is turned-off the relative deviation decreases below 8%.



(a) (b)

Fig. 9. Typical results for the bias dependent external collector resistance R_{Cx} obtained from substrate transistor based methods. (a) Eq. (8) [17] for different V_{CE} with R_{Cx} extracted from a LSQ fit of five points around the swept I_C value. (b) Eq. (10) [16] at $V_{BC} = 0.5$ V with self-heating included (solid lines) and excluded (dashed lines) as well as with and without R_{Bx} correction. The reference value is 2.3 Ω (0.13x10.16 µm² HBT from SG13G2).

Further investigations have shown that the error can be significantly reduced by increasing V_{BC} (e.g. to 0.7 V or higher) and thus by lowering V_{CE} and self-heating. The corresponding results are shown in Fig. 10(b). A further improvement can be obtained by keeping I_B constant, which circumvents the impact and correction of R_{Bx}. Moreover, keeping I_C constant even allows R_{Bx} to be extracted. However, an important condition for the method to work is a near-ideal $I_{TS}(V_{BC})$ characteristic within the extraction bias range or a more sophisticated substrate current model as the one used in eq. (10) as well as an accurate temperature dependent description of I_{TS}. The value of V_S does not matter much for determining R_{Cx} as long as the substrate transistor operates in forward active mode. Finally, a size dependence of the error was not observed.

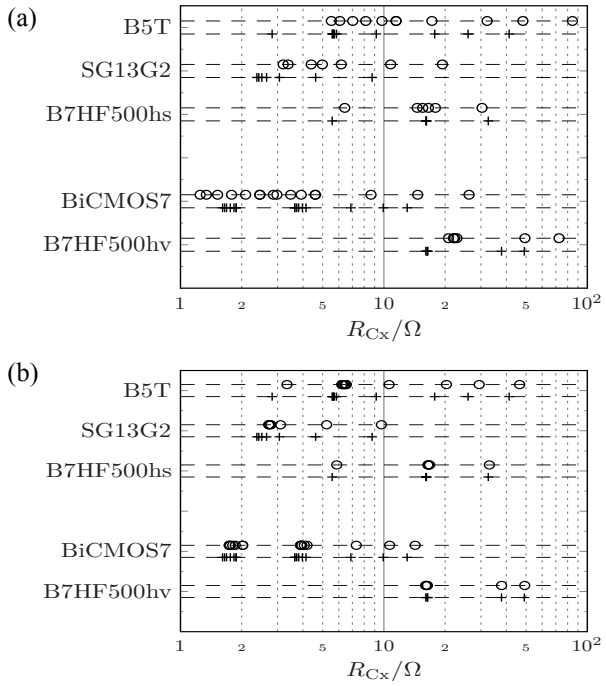


Fig. 10. Comparison of the results (in log scale) of substrate-transistor based methods proposed (a) in [17] at V_{CE} = 0.5 V and (b) in [16] without R_{Bx} correction for different process technologies and V_{BC} = 0.7 V. (Same legend as in Fig. 4.)

D. Methods based on collector impact ionization

For forward active operation at high reverse BC voltage, the measurable CB terminal voltage is given by

$$V_{CB} = V_{C'B'} + R_{Cx}I_C - R_BI_B, \tag{11}$$

where $R_C = R_{Cx}$ since the epi collector is fully depleted. A DC sweep of V_{CB} into the avalanche region causes I_B to become zero at V_{CBz}=V_{CB}(I_B=0), thus eliminating the voltage drop across R_B:

$$V_{CBz} = V_{C'B'z} + R_{Cx}I_{Cz}. \tag{12}$$

R_{Cx} can then be obtained from the slope of V_{CBz} versus I_{Cz}, if $V_{C'B'z}$ can be assumed to be bias independent [19].

Fig. 11(a) shows typical results for the bias dependence of the external and internal CB voltages at I_B zero-crossing, taken here as difference with respect to a value at low J_C. From the data of the two different technologies, it is clearly seen that the slope of V_{CBz} is mainly determined by the bias dependence of $V_{C'B'z}$ and much less by the voltage drop across R_{Cx}. Thus, the latter is strongly overestimated by this method. It is also difficult to find a suitable linear range for the extraction at all. Performing a LSQ fit over five points gives the results in Fig. 11(b), where J_{Cz} corresponds to the respective central bias current.

Fig. 12(b) shows the results of this method for different process technologies and emitter sizes. For a reasonable voltage drop across R_{Cx} large currents are required, causing self-heating and the current gain to drop with J_C. Since $V_{C'B'z}$ is the voltage at which the multiplication factor M equals $1/(1+B_f)$, the method requires a bias independent M and B_f. These conditions define the suitable bias range for the extraction. This range is quite limited in advanced technologies due to BE recombination and tunneling at low bias as well as Ge related effects in the BE junction at medium bias [39]. Therefore, the method always leads to an overestimation of R_{Cx}. This turned out to be true also for InP HBTs where the current gain is strongly bias dependent and the method does not work at all [42].

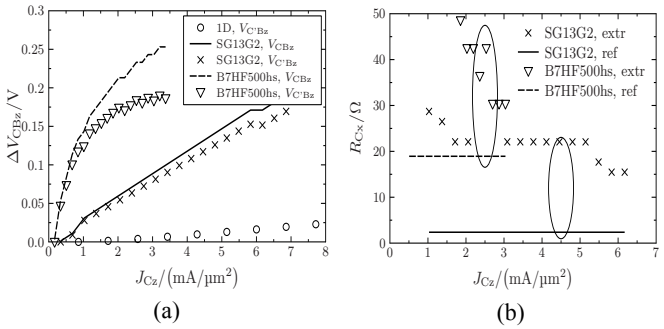


Fig. 11. Typical results obtained for the impact ionization based extraction method: (a) Terminal voltage difference ΔV_{CBz} (lines) and internal voltage difference $\Delta V_{C'Bz}$ (symbols) at I_B=0 vs. I_{Cz} for SG13G2 (x, solid line) and B7HF500hv (∇, dashed line) as well as 1D device simulation (o); the reference (offset) value was taken at J_C = {1, 0.3, 0.2} mA/ µm^2 for {1D simulation, SG13G2, B7HF500hs}. (b) Extracted R_{Cx} (symbols) vs. J_C for the same technologies as in (a) with their reference values (solid and dashed line).

Note that a significant improvement of this method can be obtained by first determining $M(V_{C'B'})$ from measured data at low J_C and then calculating the bias dependent $V_{C'B'z}$ from M as determined from the zero-crossing condition. However, the accuracy of the fit still needs to be quite high for an accurate extraction of R_{Cx}. The method tends to yield better results for wide transistors compared to narrow ones. This is attributed to the fact that for increasing width the absolute current increases for the same current density but R_{Cx} remains almost constant. Thus the desired impact of $R_{Cx}I_{Cz}$ on $V_{BCz}(I_{Cz})$ is larger compared to narrow transistors.

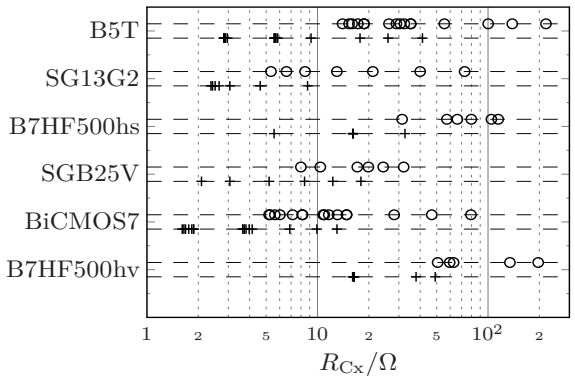


Fig. 12. Comparison of the results of the impact-ionization based R_C extraction method for different process technologies. (Same legend as in Fig. 4.)

E. Z-parameter method

The Z-parameter method was originally proposed in [15] for determining R_E from $\underline{Z}_{12}$ in common-E configuration. Apply-

ing the same principle to determining R_C from $\underline{Z}_{12,C}$ in common-collector configuration was deemed there to be too inaccurate. In a later revision of the method [21] the HBT is biased in deep saturation and at a very large forward base current in order to neglect the influence of the internal conductances and capacitances. Thus, the transistor can be represented by a simple EC consisting of external resistances only. Due to these bias conditions, only R_{Cx} can be measured according to

$$\boldsymbol{R_{Cx}} = \lim_{\boldsymbol{I_B}\to\infty} \boldsymbol{Re}\{\underline{\boldsymbol{Z}}_{22} - \underline{\boldsymbol{Z}}_{12}\}\,. \tag{13}$$

Inspection of the r.h.s. shows a strong bias dependent variation with frequency (cf. Fig. 13(a)) and an opposite trend for the two technologies displayed. This makes a general guideline for a proper selection of the frequency range difficult. In practice, R_{Cx} is then obtained from an extrapolation of $\boldsymbol{Re}\{\underline{\boldsymbol{Z}}_{22} - \underline{\boldsymbol{Z}}_{12}\}$ at a selected frequency vs. $1/I_B$ towards infinite base currents as can be seen in Fig. 13(b).

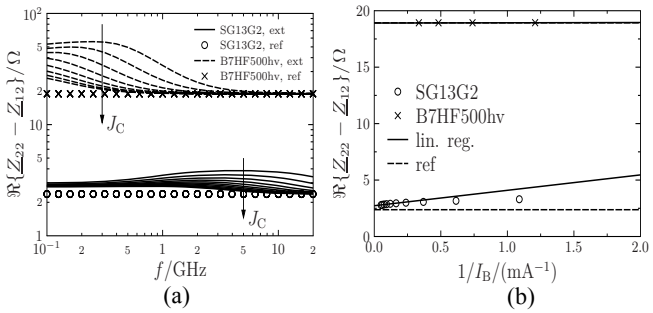


Fig. 13. Typical results for determining R_{Cx} from the Z-parameter method (V_{CE} = 0 V). (a) Frequency dependence of the r.h.s. of eq. (13) at different injection levels for SG13G2 (solid line, o) and B7HF500hv (dashed line, x). Symbols show the actual R_{Cx} for reference. (b) Extracted R_{Cx} vs. $1/I_B$ and respective LSQ fit (solid lines) for SG13G2 (at 10 GHz) (o) and B7HF500hv (at 1 GHz) (x). Symbols represent extraction results and dashed lines the reference values for R_{Cx} (not visible for B7HF500hv, since superimposed by solid line).

According to Fig. 14, the method shows very good accuracy with errors below 5% for all investigated technologies. While self-heating has only little influence due to the very low V_{CE} values used, the impact of the substrate current and the diffusion capacitance C_{dS} of the downward substrate transistor is significant. Due to the lack of suitable DC structures, substrate current related DC parameters could not be extracted for SGB25V and the respective results are not shown here. In the HF structures used for determining the Z parameters, the S terminal is shorted with the E terminal.

The suitable frequency range for this method is given by the requirement for a negligible impact of the capacitances; in particular, the external capacitances should not shunt the external series resistances.

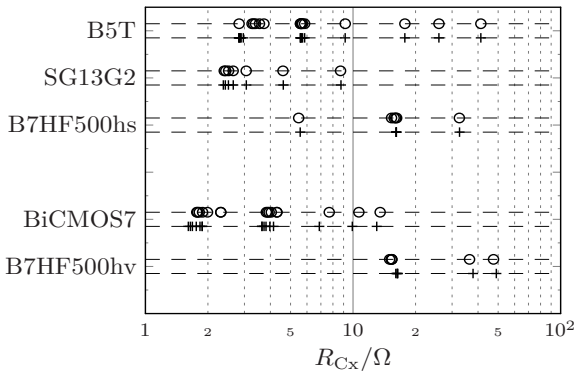


Fig. 14. Comparison of the results of the Z-parameter based extraction method for different process technologies. (Same legend as in Fig. 4.)

In [20] a more sophisticated small-signal EC than the one in Fig. 1(b) is assumed that includes a separate element for the internal collector resistance R_{Ci}. It is attempted to determine R_{Ci} from $Re\{Z_{12}\}$ in saturation. The determination requires R_E and R_{Bi} to be known, and yields just a single value which corresponds to that of a highly modulated collector region. For verification, a comparison of a complete compact model with measured characteristics was performed in [20], which is not conclusive regarding the accuracy of a method. Since R_{Ci} is neither required nor explicitly modeled in any compact model (see [48]), this method is not further discussed here.

F. High-frequency small-signal methods

In [8], the elements of a small-signal T-EC for III-V HBTs are attempted to be extracted from measured *S* parameters after conversion to common-emitter *H* parameters. The T-EC can be transformed into the Π-EC shown in Fig. 1(b). Neglecting R_{Ci}, the corresponding expression for R_{Cx} can be written as [8]

$$\boldsymbol{R_{Cx}} + \frac{\boldsymbol{g}_\mu}{\boldsymbol{g}_\mu^2 + (\omega \boldsymbol{C}_\mu)^2} = \boldsymbol{Re}\left\{\frac{1 + \underline{\boldsymbol{H}}_{21}}{\underline{\boldsymbol{H}}_{22}}\right\}. \tag{14}$$

For sufficiently high frequencies, the l.h.s. is expected to reduce to R_{Cx} for all bias conditions. Fig. 15 shows typical results for the condition $V_{BC} = 0$ which is similar to the one recommended in [8]. In this case, self-heating is a major issue, and for the technologies investigated here far too large values are obtained even at high frequencies.

Eq. (14) suggests as alternative for minimizing the second term on the l.h.s. the increase of g_μ through operation in hard saturation, which at the same time strongly reduces the self-heating. In this case, also the output conductance g_o needs to be considered though and one obtains

$$\boldsymbol{R_{Cx}} + \frac{\boldsymbol{g}_\mu + \boldsymbol{g_o}}{(\boldsymbol{g}_\mu + \boldsymbol{g_o}^2) + (\omega \boldsymbol{C}_\mu)^2} = \boldsymbol{Re}\left\{\frac{1 + \underline{\boldsymbol{H}}_{21}}{\underline{\boldsymbol{H}}_{22}}\right\}. \tag{15}$$

The corresponding results in Fig. 15 are much closer to the reference values and permit a much lower extraction frequency. Generally though, the error can be reduced by using higher frequencies.

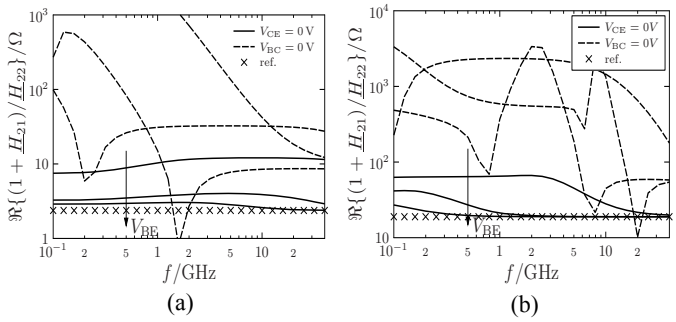


Fig. 15. The HF extraction method for different technologies and different operating modes of the transistors (a) 0.1 3 x 10.16 µm² (SG13G2) and (b) 0.22 x 5 µm² (B7HF500hv). In both cases, V_{BE} = 0.8...1 V. Arrows indicate increasing V_{BE} for V_{CE} = 0 V.

According to Fig. 16, the improved method shows quite good results for all investigated technologies. The minor deviations for SG13G2 decrease with increased emitter width. This is attributed to the positive impact of larger C_μ (see eq. (14)). Note that this will reduce the suitability of the method for transistors with very high f_{max}. Since for HF measurements the E and S terminal are connected, a large C_{dS} also helps improving the accuracy of the method since it provides an additional short to ground. Since the lack of suitable test structures did not allow to determine the parameters of the substrate transistor, results for SGB25V are missing in Fig. 16.

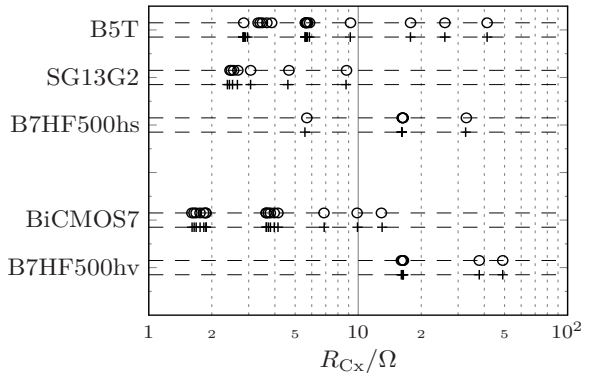


Fig. 16. Comparison of the results of the HF extraction method for different process technologies. (Same legend as in Fig. 4.). The extraction was performed at $V_{BE} = V_{BC}$ = 1.0 V and 5 GHz for all transistors.

IV. Extraction from Special Test Structures

Circuit design and optimization demands foundries to delivery geometry scalable compact models in their PDKs. Anticipating and measuring all transistor sizes[1] possibly employed during circuit design, and performing a parameter extraction for each single transistor would be by far too time consuming. Thus a more efficient way of meeting the demand for scalable models is the determination of the components of EC elements from special test structures. The EC element values can then be *calculated* for any given device geometry and dimensions based on sheet resistances, contact resistivities, current and capacitances per area and length [43, 38].

Fig. 17 shows a simple test structure with separate Kelvin collector contacts C_1, C_2, and C_3 [23]. The contact spacings b_{12}, b_{23} and length l can be chosen the same as for a (standard) transistor. Determining the buried layer sheet resistance r_{Sbl} requires a homogeneous parallel current flow between the contacts. This is achieved by taking the difference ΔI of the current measured on two structures with different length but the same b_{12} and b_{23}. Selecting the length difference $\Delta l = b_{12}$ then yields for the total resistor related to homogeneous current flow

$$R_{12} = \frac{\Delta V_{12}}{\Delta I_{12}} = r_{sBl} + 2\frac{r'_{snk}}{\Delta l} \qquad (16)$$

with r'_{snk} as the length-specific sinker resistance (e.g. in Ωµm). The two components in eq. (16) can be easily separated by subtracting R_{12} from R_{23}, which directly yields r_{Sbl} for $b_{23} = 2b_{12}$. From this and eq. (16) then r'_{snk} is obtained. Finally, the resistance related to the inhomogeneous current flow at the fore sides can be determined from the difference in the measured and calculated resistance of one of the structures with the full length l. From the extracted specific parameters, R_{Cx} can then be calculated for different device geometries, including multi-finger transistors, according to [43, 38, 24, 26].

In [26], a transistor structure with two collector contacts is measured, which does not provide new or more information than the simple structure in Fig. 17. In fact, the latter even allows additional independent measurements that can be used to further improve the accuracy.

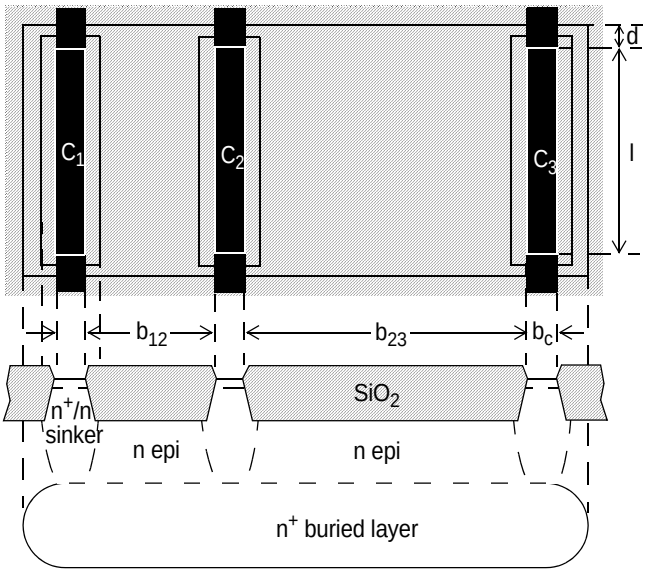


Fig. 17. Schematic layout and cross-section of a simple test structure for separately extracting the buried layer and collector sinker resistance.

An obvious advantage of using a special test structure is the independent determination of R_{Cx} and its components without requiring knowledge about any other transistor parameters. In addition, the same structures can be (and in fact have been) employed for process development and as process control

1. These include also transistors with multi-emitter fingers and non-conventional collector contact layout.

monitors for statistical modeling (e.g. [44, 45, 47]). The R_{Cx} values obtained using s uch as structure ca n be considered as reference for comparing the experimental results of the various single transistor based methods.

Moreover, section IV on the test structure based method is generally applicable to determi ne the external collector resistance existing as a separate element in the equivalent circuit of any of the compact models

V. Experimental results

Having established the suitability, issues and li mits of the various extraction methods, they were applied to experimental data. The large amount of results has been organized such that for each process technology the extracted R_{Cx} from various methods is di splayed in Fig. 18 versus the reciprocal emitter window length, $1/l_{E0}$, while the emitter width is kept constant. For determining R_{Cx} from the Z- and high-frequency methods the same RF structures were us ed as for extracting the corresponding compact model parameters, while for all remaining methods, transistors in four terminal DC-pad configuration were utilized. Note that for some of these transistors just a single length was available. Only those methods that did not exhibit complete failure in the previo us section were chosen for each technology. This excl udes already the impa ct ionization method. Additional data at different emitter width are not shown here since they confirmed the trends o bserved in Fig. 18. As reference and guide for the eye, the data from the respective test structure (if available) have also been inserted.

The results o f most single-transistor based methods exhibit the expected geometry dependence, but the spread among the different methods is larger than expected from the model based evaluations. This is caused by distributed effects, which are not taken into account in both simplified and production models, but occur under transistor operation at very low V_{CE}. These effects cause the measured R_{Cx} value to differ from the one required for typical circuit operation of the transistor. The di fference depends on the strength of t he distributed effects. As was shown in [4] for the op en-emitter and Z-parameter method, adding the corresponding elements and a bias dependent substrate resistance in the HICUM/L2 equ ivalent circuit eliminates the observed discrepancies. At high frequencies, distributed capacitive ef fects can also impact the extraction results. Therefore, one ha s to be careful about the operating conditions under which R_{Cx} is determined versus tho se where the transistors are operated in circuits.

The results in Fig. 18 show that the Z-parameter method agrees most often quite well with the resistance determined from the special test structure. The HF method mostly yields too low values as does the ope n-collector method. All other DC methods exhibit unreliable results. In case of SGB25V, the data of the frequency dependent methods might be impacted by the unconnected substrate contact in the HF structures; also, the reference line is missing since no special test structure was available. For BiC MOS7 and B5T , no DC structures were available. In addition, the BiCMOS7 measurements were performed at V_{BC} = 0.5V, which is unsuitable for the application of the small-signal methods an d therefore yields much lar ger R_{Cx} values.

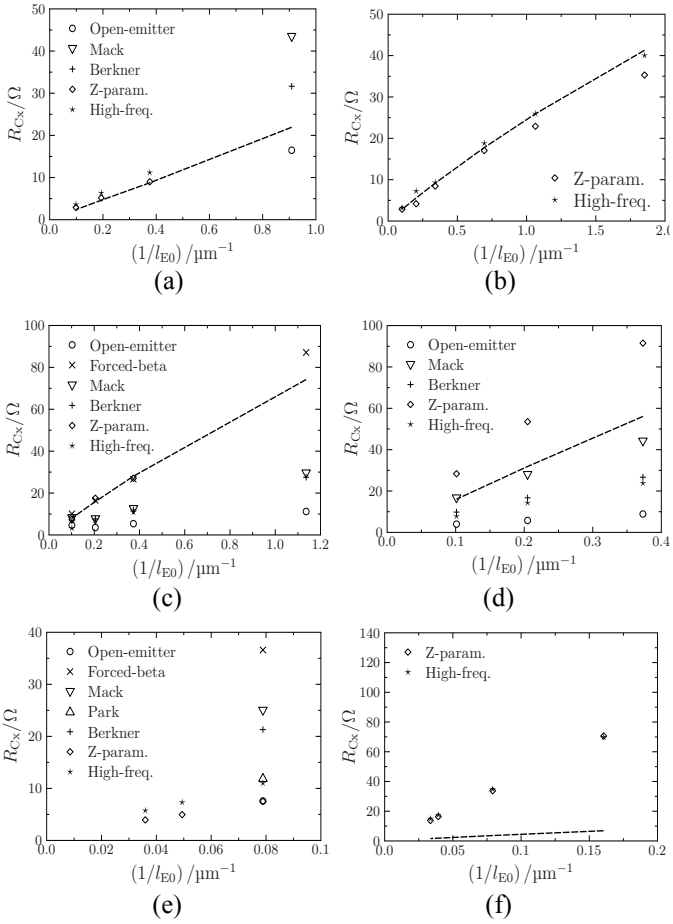


Fig. 18. Extraction results for (a) SG13G2, (b) B5T, (c) B7HF500hs, (d) B7HF500hv, (e) SGB25V, (f) BiCMOS7. The dashed line shows the results of the special test structure. For the reference of each method refer to Table II.

VI. Conclusions

A comprehensive and detailed study of eigh t widely used methods (and their variants) for extracting the collector series resistance of bipolar transistors has been presented. The methods have been applied to SiGe HBTs from six different process technologies, ranging from established production to advanced prototyping processes. Using also high-performance and high-voltage devices with a wi de range of up to twenty different emitter sizes, the results of this study are believed to be representative for the actual accuracy and applicability of the various extraction methods. For al l methods, the causes for possible or observed failures have been in vestigated and explained, providing a guidance towards their s uccessful usage. The most important causes for deviations are the strongly simplified equivalent circuit and the neg lect or too strong simplification of the d escription of i mportant physical effects such as self-heating, high-injection, and bias dependent saturation voltage. Some methods (B, C, D, F) require previously known parameters. In those cases, the parameter values from the reference mode l card were used, yielding the base case results for the particular method. A summary of the requirements and is sues of each method is provided in

Table II. Similar results have been obtained for InP HBTs [42].

Table II: Summary of conditions prohibiting the use of a method.

method	requirements, comments, issues
Open emitter [6, 7]	need– structures with separate emitter contact
Forced-beta [9, 11]	not recommended; method relies on too simplified assumptions for internal saturation voltage
Mack [16] (substrate trans.)	need DC structures with separate substrate contact; strong self-heating
Park [17] (substrate trans.)	need DC structures with separate substrate contact
Berkner [16] (substrate trans.)	need DC structures with separate substrate contact and value of base resistance; self-heating
Impact ionization [19]	very inaccurate, not recommended due to current dependence of multiplication factor (present in all transistors); neeed wide emitter transistors
Z-parameters [21]	best accuracy in most cases; need RF transistors with grounded substrate
High-frequency [8]	need RF transistors with grounded substrate; works reasonably well if operated at $V_{CE} = 0$V

As a rule of thumb, methods that rely on (simple) model equations for corrections, e.g. in the saturation region such as the forced beta method, should not be used. Furthermore, one has to be careful under which operating conditions R_{Cx} has been extracted. The resulting value may not always be representative for typical circuit applications. Hence, methods that rely on a correct equivalent circuit which includes the circuit operation related series resistance, such as both RF methods, will usually yield more accurate results. Finally, all methods attempt to determine the (external) DC collector resistance, which is different from its small-signal value at high frequencies due to dynamic and distributed current components.

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