

Comparison of on-wafer TRL calibration to ISS SOLT calibration with open-short de-embedding up to 500 GHz

Sebastien FREGONESE, Marina DENG, Magali DE MATOS, Chandan Yadav, Simon JOLY, Bernard PLANO, Christian Raya, Bertrand Ardouin and Thomas ZIMMER

Abstract – Sub-mm circuit design requires accurate on-wafer characterization of passive and active devices. In industry, characterization of these devices is often performed with off-wafer SOLT calibration. In this work, validity of this characterization procedure above 110 GHz is investigated by an exhaustive study of on-wafer and alumina off-wafer calibration using measurement and electromagnetic (EM) simulation up to 500 GHz. The EM simulation is performed at two different levels, first at the intrinsic level of the devices under test for reference and afterward up to the probe level to simulate different standards used in the off-wafer calibration or in the on-wafer calibration in presence of the probe. Further, EM simulation data is calibrated with the same procedures and tools that is used in the measurement; therefore, it includes the probe-to-substrate coupling. In addition, precise EM model of a commercial impedance standard substrate (ISS) is developed and used to perform the SOLT calibration. A good agreement is observed between measurement and EM modelling for the off-wafer calibration as well as for the on-wafer calibration. Results clearly highlights a limitation of alumina off-wafer methodology above 200 GHz for characterization of Silicon based technologies. Finally a discussion is given on the pros and cons of the off-wafer and on-wafer methodologies.

Index Terms— S-parameter measurement, probe station, THz, SiGe HBT, on-wafer, calibration, SOLT, TRL, 500 GHz

I. INTRODUCTION

THE development of sub-THz system requires dedicated procedures for the circuit design, compact modelling and device characterization. In the field of S-parameter characterization, well established measurement methodologies have been adopted and used during many decades for measurement up to 110 GHz.

Numerous off-wafer calibration methodologies such as Short-Open-Load-Thru (SOLT), Line-Reflect-Reflect-Match (LRRM) are commonly used in production environment. These methods have been embraced due to practical reasons

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such as their wide band capability and the use of easily available commercial impedance standard substrate (ISS) discard the design and precise characterization of a homemade calibration kit [1]–[3]. Usually, these calibration methods have been analyzed and compared only up to 110 GHz [4] with the Thru-Reflect-Line (TRL) calibration. For example in [2] and [5], different calibration methods have been employed to show limitations of the calibration on ISS compared to the on-wafer TRL calibration – fact is that in ISS calibration both calibration standards and test structures do not share the same substrate. One issue related to the off-wafer calibration with ISS calibration kit is concerned with the substrate-to-probe coupling properties which leads to a systematic error [13]. Impact of the spurious wave modes propagating into the ISS substrate are “unintentionally reported and superimposed to the measurement data” [6]. The ISS calibration locates the measurement reference plane at the probe tip, this is another drawback of this method. This reference position is considered as “somewhat approximate” in [7] due to the discontinuity of the domains (transition of probe-tip to on-wafer). In [7]–[9], on-wafer methodologies have been studied below 110 GHz using 100 μm pitch probe and shows advantages on the measurement accuracy with a well-defined reference plane and unchanging probe-to-substrate coupling during calibration and measurement. Despite above mentioned arguments concerning probe-to-substrate coupling, some research groups still employ ISS based calibration method such as LRRM and TRL for characterization of BiCMOS technologies above 100 GHz and up to 325 GHz [10], [11].

It is worth to point out that in contrast to the TRL calibration which uses transmission lines, SOLT calibration uses mainly lumped elements. Since, lumped elements can be considered as non-distributed elements only if the wave length of the signal is sufficiently large compared to the physical size of the elements. Therefore, with the reduction of the probe pitch, it is of the utmost interest to the device community to reconsider the frequency range validity of the SOLT calibration above 110 GHz.

In this paper, the off-wafer SOLT calibration, which is widely used in the industry, is compared to the on-wafer TRL calibration and the limitations of the former are investigated. For the first time, this analysis is performed in the upper frequency bands up to 500 GHz on a silicon germanium (SiGe) technology using scaled GSG pad dedicated to 50 μm pitch probe. Moreover, for the first time this comparison is

validated step by step with the support of electro-magnetic (EM) simulation including the probe into the simulation environment to include the probe-to-substrate coupling and the crosstalk between probe to probe. The calibration algorithm applied to the simulation is the same as the one applied to the measurement using our in-house TRL and SOLT toolkit. The paper is organized as follows: the first section describes the ISS, test structures and EM modelling, the second section presents the on-wafer test structures. The third part is dedicated to the measurements of the off-wafer SOLT and on-wafer TRL up to 500 GHz and a validation with the EM simulation. Finally, an analysis comparing off-wafer (ISS) SOLT and TRL with de-embedding along with the on-wafer TRL is presented with detailed discussion on the pro and cons of the different types of calibration methods.

II. TEST STRUCTURES AND ELECTROMAGNETIC SIMULATION

A. Characterization and Electromagnetic simulation of ISS

In order to evaluate the SOLT calibration accuracy for avoiding uncertainties in the measurement, an exhaustive EM simulation study has been performed in parallel to the measurements by applying the same procedure on EM simulation data as used for the measurement data. To reach on the goal, first, the ISS calibration kit (GGB CS15) structures have been investigated (see Fig. 1) and characterized to implement them in the EM simulation tool. The physical length of the coplanar-wave-guide thru is $250\mu\text{m}$. The width of the signal line is about $25\mu\text{m}$ while the gap between ground and signal is about $13\mu\text{m}$. Gold metal thickness has been measured by interferometry. A value of $3.5\mu\text{m}$ has been found and was used within the EM simulation tool (see Fig. 1). Applying the same procedure, the layer thickness of the load resistances has been measured and its thickness was found to be 50 nm . Using these findings, the open, short, load, thru and line structures from the CS15 ISS substrate designed by GGB Industries have been implemented in the Ansys HFSS EM simulator (see Fig. 2).

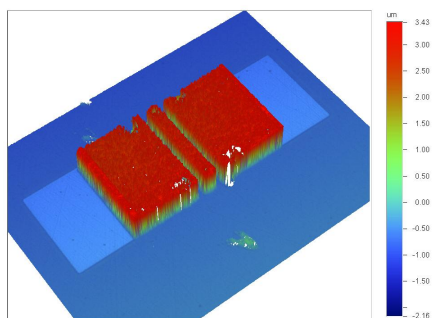


Fig. 1: Interferometry image of the thru from the ISS (GGB-CS15)

Furthermore, one single and simplified probe geometry has been designed in the EM simulator for the full frequency range under study (1 to 500 GHz). It has a GSG configuration and a $50\mu\text{m}$ pitch. Figure 2 presents the probe model implemented in the EM simulator.

Using the designed probe model, open, short, load, thru and lines of the ISS standard from GGB CS15 have been simulated in HFSS. To reduce the computation time, we used the symmetry of the structure and simulated only half of it. The permittivity of the substrate has been set to 9. The inter-probe distance is $150\mu\text{m}$ and is given by the CS15 calibration kit. The length of each probe is about $300\mu\text{m}$. The substrate thickness is $300\mu\text{m}$. With the exception of the symmetry plane, we consider a “radiation box” in HFSS all around the structure as a boundary condition meaning that the evanescent electromagnetic waves are absorbed. Please note that doing so, the simulation and measurement is consistent since an ISS absorbing holder is used in the measurement below the substrate.

The data obtained from these simulations have a reference plane located at the transition point of the coaxial part of the probe to the CPW probe tips (Fig. 5a red rectangle). Applying the TRL to the simulation data using the thru, the open (used as the “reflect”) and the line, one can move the reference plane from the input of the probe to the probe tip contact. Impedance correction is not performed here, because the characteristic impedance of the ISS standards is considered to be close to 50Ω in the whole frequency band. In addition, using the TRL calibrated results each standard has been characterized to obtain the input parameters that are needed for a SOLT calibration. The extracted parameters comparison with the datasheet of the CS15 calkit from GGB is given in Table 1.

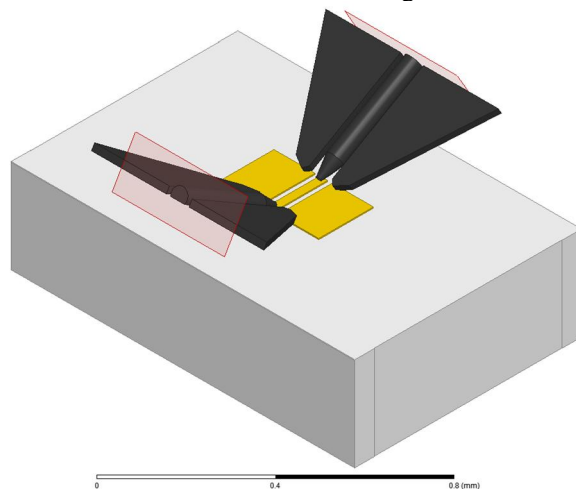


Fig. 2: EM simulation structure used for the thru on ISS: white is the alumina, yellow is the gold and the probes are in the black. Description of the probe: length is $350\mu\text{m}$, largest width is $550\mu\text{m}$, signal conductor width is $39\mu\text{m}$, gap between signal and ground is $13.6\mu\text{m}$.

EM simulation study shows very similar results compared to the datasheet. Unfortunately, the values from the datasheet are not probe geometry and pitch dependent while it is obvious that the pitch of the probe has a direct impact on the value of the short and can impact some other parameters like the capacitance of the open.

Standard	Values given in Data sheet of CS15	Values extracted using EM simulation
Open	3.25fF	3.2-3.4fF
Short	2pH	1.5 pH-2.5pH
Load	1.5fF	1.4-2.2fF
Thru	1.13ps	1.10ps

Table 1: Comparison of extracted parameters values of each standard with the values given in data sheet of the CS15 calibration kit. Note that values in data sheet is provided by Picoprobe GGB industries and is applicable for 50 μm – 125 μm pitch probe. To extract parameters values (shown at 60 GHz and 250 GHz), 50 μm pitch probe model is used to perform EM simulation which is followed by TRL calibration of standards.

Using the results obtained above, we are able to perform off-wafer SOLT calibration which brings the reference plane to the probe tips. In the succeeding sections of the paper, results from the SOLT calibration is compared with the on-wafer TRL calibration performed using dedicated test structures. A detailed description of the on-wafer test structures is given in the following section.

B. Description of on-wafer test structures

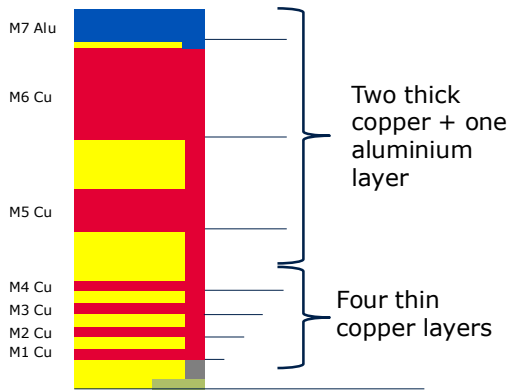


Fig. 3: Schematic view of the BEOL of Infineon's B11HFC process [12], [13].

The on-wafer test structures have been designed on a 130nm BiCMOS technology of INFINEON where back-end-of-line (BEOL) has 6 levels of copper layers (see Fig. 3). The last level of copper layer is used for the design of the micro-strip line and is 2.8 μm thick. The ground plane is realized using metal-4 and the space covered by dielectric between ground plane and the micro-strip line is about 3.5 μm thick. In the structures, pads are designed for 50 μm pitch probe and a pad access line of 4 μm is included in the design to shift the reference plane after the pad at the end of access line (see Fig. 4a).

To perform on-wafer TRL calibration, designed thru has length of 50 μm while the lines have lengths of 160 μm and 560 μm (see Fig. 4a and Fig. 4c). A pad-open is used as reflect and finally a load is used to extract the characteristic impedance of transmission lines using the methodology described in [15]. Using method of [15], we could take into

account the characteristic impedance of the transmission lines and transform the reference impedance of the TRL calibration to 50 Ω .

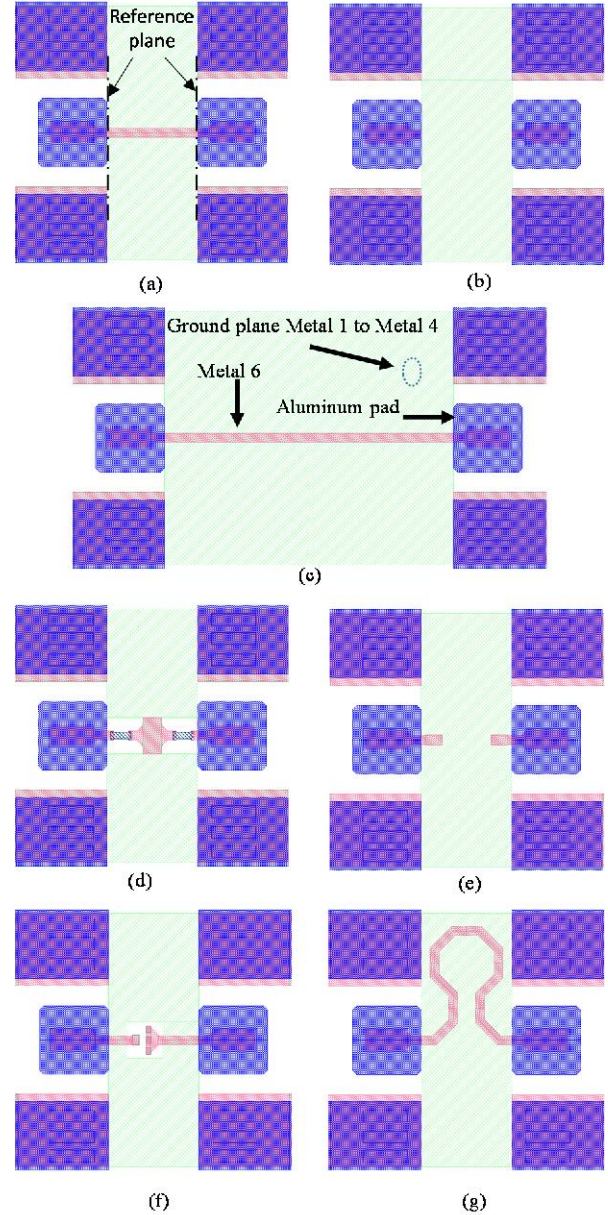


Fig. 4: Simplified representation of the layout of some of the test structures: (green dashed line) is Metal 1 to Metal 4 (Ground plane), red right-hatched is metal 6, blue dotted is aluminum used for the pad. The probe pitch is 50 μm . a) Thru of 50 μm , b) Reflect pad open, c) Line of 160 μm , d) Load, e) Pad short, f) Transistor-open and g) Meander line.

C. EM simulation of on-wafer test structures

The on-wafer test structures described above have been investigated using 3D-EM simulation. We employed the following simulation strategy: i) simulate the intrinsic structures at the reference plane just after the pad as shown in Fig. 5b or Fig. 5c; ii) simulate all the structures including the probe (see Fig 5a) - four structures on the ISS i.e. open, short, load, thru and eight on-wafer structures thru, line, load, open-pad, short-pad, transistor-open, transistor-short, and meander line has been simulated. Further, using the simulated data of

required test structures both the off-wafer SOLT and the on-wafer TRL calibrations are applied.

Applying the on-wafer TRL shifts the reference plane at the end of the pad (see Fig. 4a), while off-wafer SOLT shifts the reference plane at the probe tip. Hence, the off-wafer SOLT and the on-wafer TRL cannot be compared directly. In order to move the reference plane of the off-wafer SOLT after the pad, a pad-open/pad-short de-embedding procedure is applied. Consequently, the intrinsic structure, the on-wafer TRL and the off-wafer SOLT ISS plus de-embedding have the same reference plane and can be compared. Note that seven simulated structures are required to apply an off-wafer SOLT with pad-open/pad-short de-embedding while only four structures are required for the on-wafer TRL to set reference plane at the same position.

This methodology is applied to the full set of structures and results are shown with the measurement in the next section for the pad open, pad short, transistor-open and meander line.

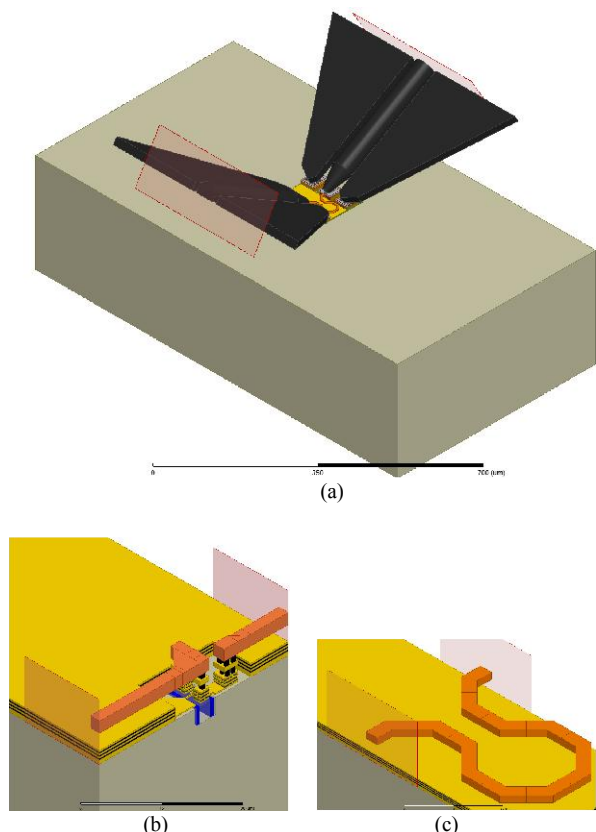


Fig. 5: EM simulation of a) the EM full structure including probes, pad and transistor open and b) half intrinsic transistor open used as a reference simulation c) intrinsic meander line used as a reference simulation (wave ports corresponds to reference plane of the TRL calibration). (M6: orange, M1-M5: yellow, vias: black, Si: grey, deep trench isolation: blue). Dielectrics of the BEOL are not shown for clarity.

III. MEASUREMENT RESULTS AND COMPARISON TO EM SIMULATION

Four measurement benches were used to cover the frequency range from 1 GHz to 500 GHz. First, an E8361A Vector Network Analyzer (VNA) from Agilent working up to 110 GHz using extenders (N5260-60003) above 67 GHz is used up to 110 GHz. Then, for the remaining frequency bands 140-220

GHz, 220-330 GHz and 325-500 GHz, measurements are performed with a four-port Rohde & Schwarz ZVA24 VNA coupled with Rohde & Schwarz VNA extenders (ZC220-ZC330-ZC500). The extenders are installed on a Signatone probe station. The RF probes used in this work are from Picoprobe GGB with a pitch of 50 μm in each frequency band.

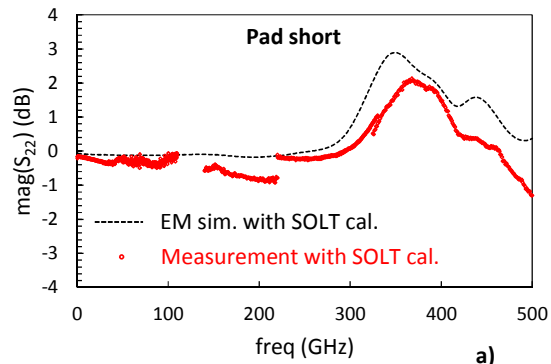
For all the frequency bands, the CS15 calibration kit from GGB has been used for the off-wafer SOLT calibration. The test structures implemented in Infineon B11HFC BiCMOS technology: pad open, pad short, transistor-open, transistor-short and a meander line have been measured over the whole frequency range.

A. Off-wafer SOLT on ISS

First, we show the comparison of measurement results with EM simulation for test structures after applying off-wafer SOLT calibration on them.

In Fig. 6 and Fig. 7, measurement and simulation results obtained after off-wafer SOLT calibration for the pad-short (see Fig. 4b) and pad-open (see Fig. 4e) are shown.

If we look into measurement results, a pretty good frequency band continuity can be observed despite the different measurement setups used in each frequency range. Further consistency of the measurement is validated. A drop in reflection coefficient S_{22} of the pad-open (Fig. 7a) between 70 GHz and 140 GHz is attributed to coupling between the probe to neighboring structures [14] which is not accounted for in the present EM simulation study. The distance between two adjacent structures from signal-pad to signal-pad is about 25 μm . The overall trend observed in the measurement (Fig. 6 and Fig. 7), both in the S_{22} magnitude and phase are clearly reproduced with the EM simulator which gives confidence in the simulation data. Regarding the relevance of the SOLT on ISS calibration in the upper frequency band, we can observe that in both pad-short (Fig. 6a) and pad-open (Fig. 7a), an unphysical behavior is observed on the magnitude of S_{22} parameter above 250 GHz. In fact, the magnitude of S_{22} becomes higher than 0 dB showing a non-physical behavior with a curve going out of the Smith chart.



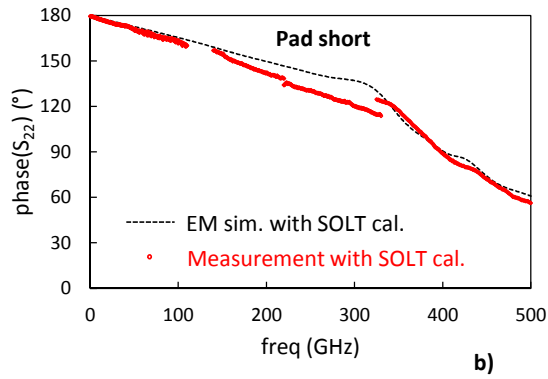


Fig. 6: a) Magnitude and b) phase of S_{22} parameter versus frequency of **pad-short** (see Fig. 4e) after off-wafer SOLT calibration (GGB CS15) –Solid line is measurement and dashed line is EM simulation. Note that after SOLT calibration, reference plane is set at the probe tips.

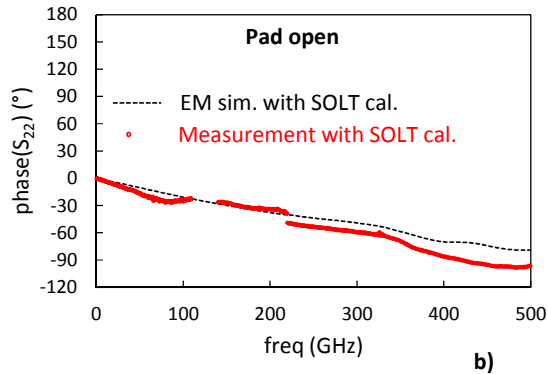
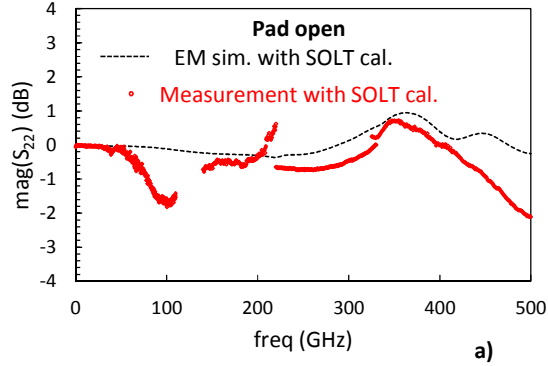


Fig. 7: a) Magnitude and b) phase of S_{22} parameter versus frequency of **pad-open** (see fig 4. b) after a SOLT ISS calibration (GGB-CS15) –Solid line is measurement and dashed line is EM simulation. Reference plane is set at the probe tip.

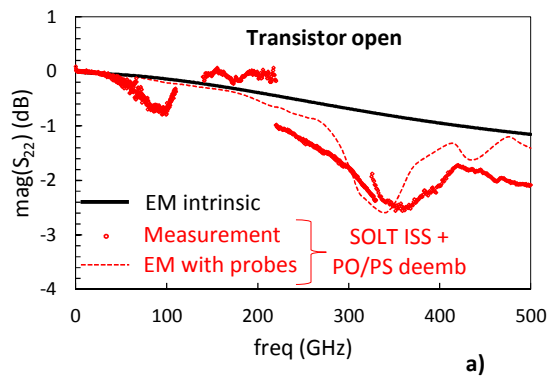
B. Comparison of on-wafer TRL with off-wafer SOLT on ISS with de-embedding

In order to analyze the limitations of the off-wafer SOLT on ISS calibration, a comparison with other methods along with a reference data is required. Hence, the off-wafer SOLT calibration on ISS is compared to the on-wafer TRL on silicon substrate. To make a fair comparison between the off-wafer SOLT and on-wafer TRL calibration, reference plane should be set at the same position after applying both the methods. To set reference plane at same position in both methods, reference plane after SOLT calibration is moved from probe tips to the end of the pad by applying a pad-open/pad-short de-embedding procedure. Finally, the simulation results of the

intrinsic structure, i.e. after the pad (see Fig. 8 and Fig. 9, black solid line) is used as a reference data for the final assessment.

In Fig. 8, EM simulation and measurement results of the magnitude and the phase of the transistor-open is shown after the on-wafer TRL and the off-wafer SOLT calibrations with a common reference plane set after the pad. The transistor-open structure is chosen as a representative because it is a key structure having a complex backend of the line starting from top metal down to metal 1 and its measurement accuracy strongly affect the measurement quality of the transistor. The EM simulations clearly reproduce the trends observed in the measurement despite the numerous steps of measurements and simulation. A first major conclusion is that these trends are not artifacts or problems of reproducibility of the measurement setup but these trends are introduced by the calibration and de-embedding procedure. For example, one can observe a drop in magnitude of S_{22} from off-wafer SOLT on ISS data around 330 GHz in both measurement and EM simulation. In the case of the on-wafer TRL calibration, a quite good matching is observed between both measurement and simulation results and the intrinsic EM data giving confidence in both the measurement quality and the calibration methodology. The inaccuracies observed in the case of the on-wafer TRL seems to be correlated to the contact quality.

The same measurement versus simulation comparison is carried out for the meander line (see Fig. 9). In Fig. 9, results obtained from measurement and simulation shows that phase of S_{21} parameter is well captured by both the off-wafer SOLT and the on-wafer TRL calibration simulations, but magnitude depicts an unphysical behavior in case of the off-wafer SOLT calibration. The error introduced by the off-wafer SOLT is about 4 dB in measurement and 1 dB in simulation while the error given by the on-wafer TRL is about 1 dB in measurement and less than 0.2 dB for the simulation (see Fig. 9a beyond 300GHz). The EM simulation reproduces well the imperfection introduced by the off-wafer SOLT and again confirms the good accuracy of the on-wafer TRL.



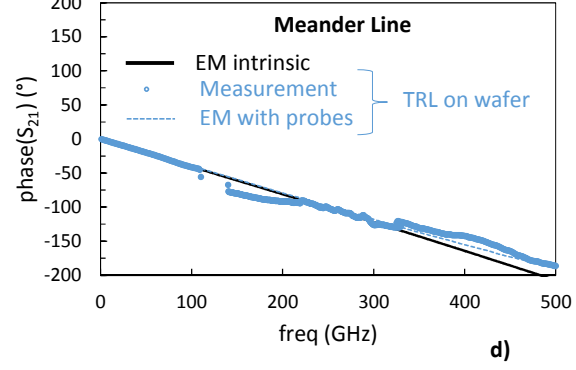
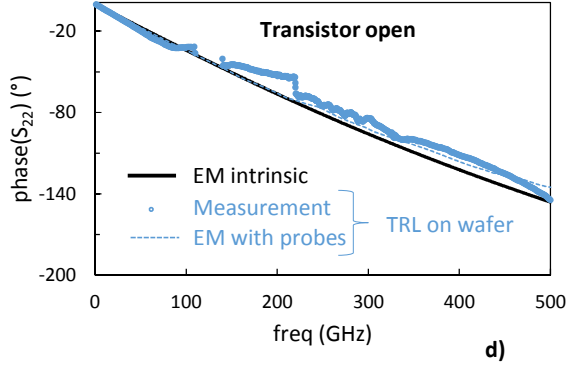
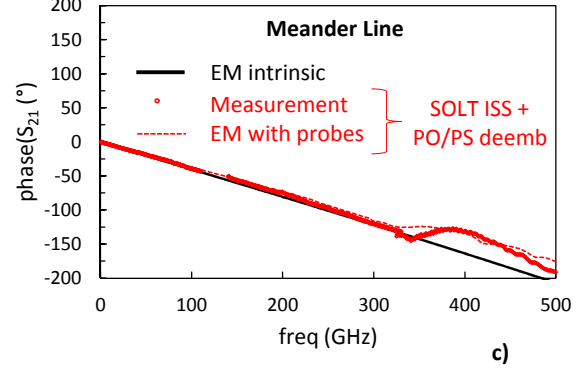
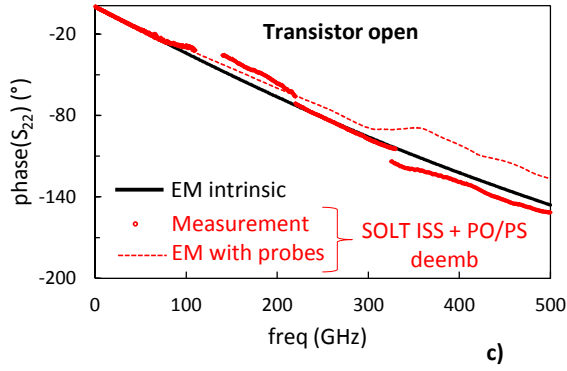
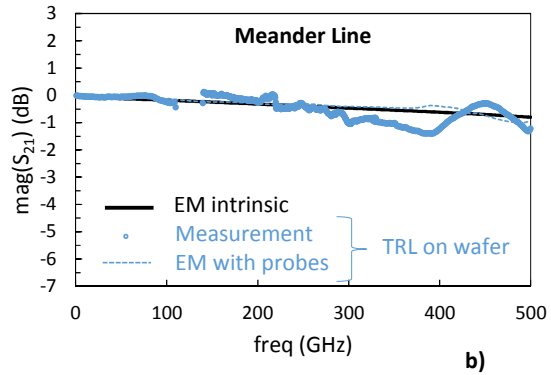
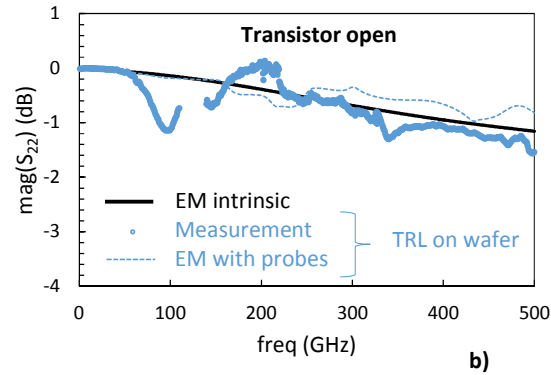
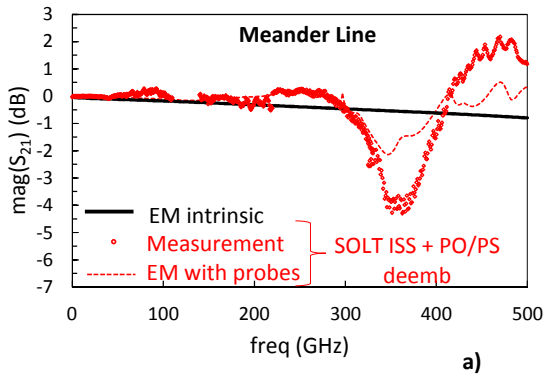


Fig. 8: S-parameter versus frequency of **transistor-open** where reference plane for each data is set after the pad (see Fig. 5). In all figures, symbols represents measurement, dashed line represents EM simulation with probes and black solid line represents EM simulation of the intrinsic structure (without pad and probes). Panel (a) – (c) represents; a) Magnitude of S22 calibrated with SOLT ISS + de-embedding; b) Magnitude of S22 calibrated with on wafer TRL; c) Phase of S22 calibrated with SOLT ISS + de-embedding and d) Phase of S22 calibrated with on wafer TRL

Fig. 9: S-parameter versus frequency of a **meander line** where reference plane for each data is set after the pad (see Fig. 5). Here, symbol, dashed line and solid line are used for the measurement data, EM simulation with probes and EM simulation of the intrinsic structure (without pad and probes), respectively. Results in each panels are corresponds to a) Magnitude of S22 calibrated with SOLT ISS + de-embedding, b) Magnitude of S22 calibrated with on wafer TRL, c) Phase of S22 calibrated with SOLT ISS + de-embedding and d) Phase of S22 calibrated with on wafer TRL.



From the results discussed in this section, we summarize that the on-wafer TRL calibration outperforms the off-wafer SOLT on ISS calibration above 200 GHz. The poor accuracy of the off-wafer SOLT in the upper frequency band is mainly explained by the probe-to-substrate coupling which is different during calibration and measurement. The de-embedding eventually reduces this coupling effect but it itself is a factor in SOLT calibration limitations due to concerns related to lumped elements models accuracy in the upper frequency band where distributed effects starts dominating. Note that the significance of these effects is directly correlated to the dimensions used in each layout. There is one more important reason behind observed SOLT limitation that is correlated to the algorithm of the SOLT itself which requires input

parameters for the calibration standards e.g. value of the capacitance of the open or the inductance of the short. These parameters provided by the manufacturer of the ISS substrate are constant with frequency and are not probe geometry dependent in this case. In fact, the probe pitch could impact model parameter values and this factor should be accounted for while calculating the model parameters corresponding to a standard. This last limitation doesn't exist in the algorithm of the TRL.

C. Comparison of on-wafer TRL calibration against off-wafer TRL and SOLT calibrations with de-embedding

In order to distinguish algorithm weakness of the SOLT compared to TRL, a comparative study between three calibration methods i.e. off-wafer SOLT calibration with de-embedding, off-wafer TRL calibration with de-embedding and on-wafer TRL calibration is presented. This study is solely based on the EM simulation data to avoid uncertainties inherent in the measurement such as probe contact quality, probe positioning and long term drift of the measurement equipment. The TRL calibration on ISS is performed using the simulation of a scaled model of the CS15 substrate from GGB. In fact, the length of the thru and the line of the original CS15 calibration kit limits the comparison below 250 GHz. Hence we reduced the inter-probe distance of 70 μm to extend the frequency limit above 400 GHz. The Fig. 10 shows the magnitude and phase of the transistor-open with a reference plane at the end of the pad. In Fig. 10, all the three calibration methods, i.e. SOLT ISS with de-embedding, TRL ISS with de-embedding and TRL on-wafer are compared to the intrinsic simulation. These results shows that off-wafer TRL on ISS behaves similarly to the off-wafer SOLT on ISS and is less accurate compared to the on-wafer TRL calibration. Hence, these results clearly highlight that the source of error is not the calibration algorithm itself and that off-wafer method on alumina is inappropriate for high frequency measurement above 200 GHz. As already underlined earlier, the main source of inaccuracy of the off-wafer calibration above 200 GHz is the coupling between the probe and the substrate which becomes predominant above 200 GHz and the limitation due to the de-embedding procedure. It would be worth to mention that in off-wafer calibration, substrate other than alumina having properties closer to the silicon could give better results for example fused silica studied in [13].

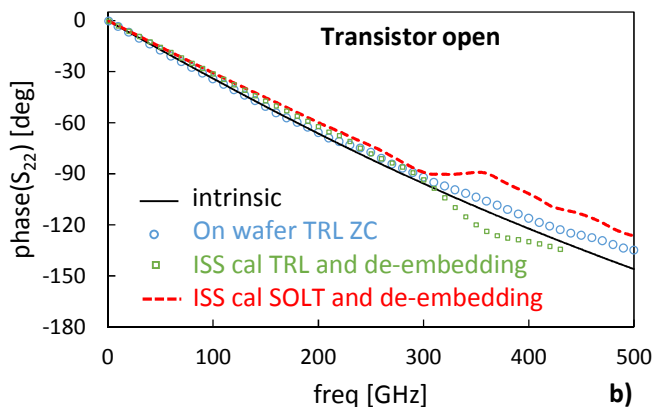
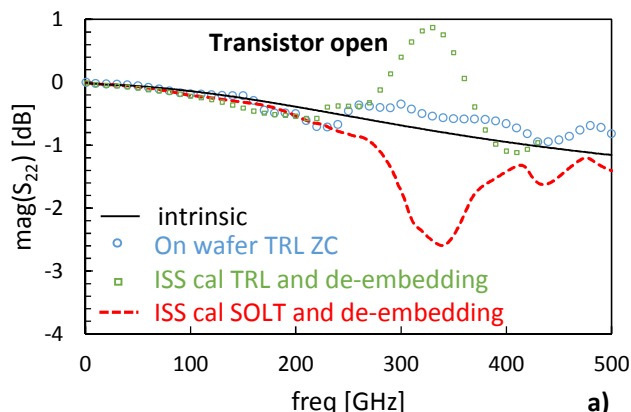


Fig. 10: EM simulation prediction of the transistor-open a) magnitude and b) phase of S_{22} parameter versus frequency. Included results are for SOLT ISS calibration with pad open – pad short de-embedding (red dashed line); TRL ISS calibration with pad open – pad short de-embedding (green square); on-wafer TRL calibration (blue circle) and intrinsic simulation without pad and probe (black line). Reference plane for each data is set after the pad (see Fig. 4a or Fig 5).

In terms of overall measurement uncertainty, a calibration method with higher number of standards requirement can be more prone to uncertainties due to increased errors owing to more number of standards. In the case of off-wafer SOLT with de-embedding, seven test structures are required to obtain the measurement of a transistor-open or transistor-short structure with a reference plane after the pad while the on-wafer TRL requires only four structures. Also, while the on-wafer calibration gives quasi-ideal results in simulation, its main drawback comes from the quality of the contact during the calibration procedure when measuring on-silicon test structures embedded with aluminum pad compared to gold pad [14]. In particular, Williams et al. have highlighted the difficulty of making repeatable contacts on aluminum pads, which is of utmost importance for the on-wafer calibration of silicon technologies [12]. This is of course not the case for the off-wafer calibration which is performed on gold pads, but we need at minimum two additional measurements on-silicon test structures for de-embedding purposes. Thus, there is no way to get rid-off the contact quality. In addition, probe positioning, the drift of the equipment and eventual effects of adjacent structures explain the uncertainties observed for on-wafer calibration results.

IV. CONCLUSION

Off-wafer SOLT on ISS calibration application frequency limit has been assessed using measurement and EM simulation for characterization of a silicon-based technology. The unexpected or unphysical trends observed in the measurement are reproduced by the EM simulation which indicates that these results are not artifices or problems of reproducibility of the measurement setup but these trends are introduced by the calibration and de-embedding procedure. Hence, the results show a clear limitation of this calibration and the associated de-embedding procedure above 200 GHz for the following reason: i) substrate coupling difference between ISS calibration standards and on-wafer test structures measurement, ii) de-embedding procedure which is no longer

valid since elements cannot be considered anymore as lumped elements beyond 200GHz, iii) only frequency independent input parameters for the calibration standards in the SOLT algorithm are available. In order to discriminate errors introduced by the calibration algorithm and the de-embedding procedure (which are strongly correlated to the use of the ISS), an off-wafer TRL on ISS has also been studied using EM simulation. Again, a clear limitation of the utilization of any off-wafer calibration is demonstrated due to both substrate coupling and de-embedding. Finally, the on-wafer TRL has been evaluated via both EM simulation and measurement and the results show that this procedure outperforms the off-wafer ISS calibration since it solves simultaneously the problem of calibration environment and avoid the de-embedding of the pad. The number of elements to be measured for calibration is reduced implying a reduction of the potential of manipulations errors and error propagation in S-parameter matrix calculations. Finally, the main limitation of on-wafer TRL technique comes from the contact quality on aluminum.

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