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Hot Carrier Degradation in SiGe HBTs: A Physical and Versatile Aging Compact Model

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***Abstract*—This paper presents a new physical compact model for interface state creation due to hot-carrier degradation in advanced SiGe HBTs. An analytical model for trap density is developed through an accurate solution of the rate equation describing generation and annihilation of interface traps. The analytical aging law has been derived and implemented in terms of base recombination current parameters in HiCuM compact model and its accuracy has been validated against results from long-term aging tests performed close to the safe-operating-areas of various HBT technologies. The model implementation uses a single additional node, alike previous implementations, thereby preserving its simplicity yet improving the accuracy and the physical basis of degradation.**

***Index Terms*— Aging, compact model, hot-carrier degradation, safe operating area, SiGe HBTs.**

I. Introduction

IMPROVED frequency performances of SiGe heterojunction bipolar transistors (HBTs) have been achieved at the cost of significantly increased operating current density and lower breakdown voltages [1]. Devices being operated closer and even beyond the classical safe-operating areas (SOA) limits stable operation due to several long-term reliability issues, such as hot-carrier degradation (HCD) that drastically affects the lifetime of a SiGe HBTs [2-4]. Apart from existing process imperfections, hot carriers can provide enough energy to break Si-H bonds thereby resulting in trap generation at the Si/SiO_2 interfaces. In modern SiGe HBTs, such traps at the emitter-base (EB) spacer oxide interface produce excess non-ideal base current in the forward operating mode via trap-assisted Shockley-Read-Hall (SRH) recombination, thus degrading current gain and input impedance [5] in the long-term operation. From a physical viewpoint of HCD, the reaction–diffusion (R–D) theory has long been a well-accepted framework for comprehensive understanding of the phenomena [2-4, 6-9]. In recent times, however, R-D model has been criticized, particularly in the MOS community, for its inaccuracy in explaining bias-temperature instability (BTI) [10-11], especially during the post-stress recovery phase. It is a general observation that actual recovery in MOS devices are too fast for R-D model to correctly predict, which some researchers have attributed to fast de-trapping using the hole-trapping model [7, 10, 12]. Alternative to R-D transport theory, multi-trapping (MT) dispersive transport [13] is also proposed for MOS systems [11, 14]. However, discrepancies between a generalized R-D model framework and dispersive transport are mainly attributed to how their initial and boundary conditions are chosen at the Si/SiO_2 interface [11]. On the other hand, some researchers have demonstrated for MOS systems that contrary to the popular belief, generation of interface traps can be correctly described by R-D model for long-term aging and the overall degradation/recovery characteristics can be predicted by a framework consisting of uncorrelated contributions from interface trap generation and hole trapping in pre-existing process-related oxide traps [12]. The scenario, however, is different for advanced HBTs, for which the recovery phase is not so commonly observed due to a very different electrostatic environment compared to MOS structures and permanent degradation of HBT characteristics are often reported [2-4, 8-9]. If dimensions of HBT E-B spacer and MOS gate oxide are compared from Fig. 9 of [16] (showing TEM views of an advanced BiCMOS technology), different electric field values can be estimated. In fact, while peak vertical electric fields at HBT collector can reach 400 kV /cm, it becomes negligible near the E-B spacer [15], while the electric field across the ultra-thin gate oxide often reaches values as high as 10 MV/cm under extreme conditions [7]. Schematics in Figs. 1(a) (HBT) and 1(b) (MOS) illustrate the degradation mechanisms and their respective locations. In MOS structures, due to a much thinner gate oxide and subsequently a much higher electric field, hot carriers created due to impact ionization can influence device characteristics significantly by both charge trapping in pre-existing traps and new interface state creation. On the other hand, only interface state creation in the HBT E-B spacer (in the absence of sufficient E-field) can be held responsible for permanent degradation [17]. Hence, interface state generation described by the R-D model can predict device degradation accurately enough in modern HBTs [2-4, 8-9, 15, 17-22]. Moreover, from designer's viewpoint, R-D model is preferable owing to its analytic form, especially for preserving a reasonable circuit simulation time yet maintaining the physical basis [18].

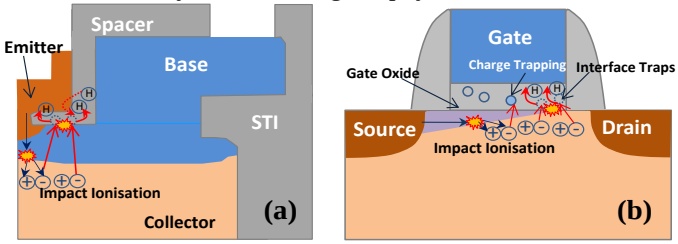

Fig. 1: Schematic illustration comparing hot carrier degradation in (a) HBT, (b) MOS architectures, showing interface state creation and charge trapping.

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An approximate solution of the R-D rate equation is widely used in which the time-dependence of the degradation is governed by a power law (t^n) [2-3, 6-9]. Although this solution accounts for the degradation phase in which atomic H diffuses away from the interface, which thereby governs the time-exponent of the aging law [6, 7], this power law does not account neither for the saturation of the degradation characteristics after long-term aging (when the trap density approaches the total number of available dangling bonds), nor for the initial phase when the generation process dominates (~t). To address this, Fischer *et al*. [2-3] proposed an empirical time dependence of the power law exponent that accounts for a change in slope towards a soft-saturation. An exponential model has been adopted for trap density in [4], based on the R-D model, however omitting the annihilation of the traps. Although fairly accurate in specific phases of the aging, these models do not capture all the phases of degradation in one single analytic form. In this paper, such an analytical solution of the R-D model has been developed that describes the entire degradation in one single form. Rest of the paper has been organized as follows; Section II illustrates the derivation of the analytical solution; Section III describes the device and the aging test conditions; Section IV describes HiCuM model implementation and validation; Section V extends model validation to different technologies.

II. Analytical Solution of the R-D Model

Hot-carrier-induced degradation in SiGe HBTs is attributed to Si-H bond dissociation near E-B spacer oxide [2-5, 17-18]. The rate at which the bonds break is determined by the chemical interaction between the carriers and the passivated Si-H bond. While the carrier energy transferred directly to the H atom is not sufficient for its release, bond breakage occurs when a bonding electron is excited to the transport state thereby inducing a repulsive force that detaches the H atom. [7]. The remaining Si dangling bonds act as interface traps while the H released from the bond can diffuse away from the interface or fill an existing trap. Therefore, the interface-trap density, N_T, increases with the net rate of reaction, which can be written by (1), as described by the R-D model,

$$\frac{dN_T}{dt} = K_F(N_F - N_T) - K_R N_T N_H^0 \tag{1}$$

Here, K_F is the rate of the forward reaction, *i.e.*, generation of trap, K_R is the rate of trap annihilation by hydrogen atoms, N_H^0 is the volumetric density of hydrogen at the interface and N_F is the total number of available bonds that can break. Considering a 1D approach, the hydrogen diffusion away from the interface is written by the following equation using Fick's second law of diffusion as,

$$\frac{\partial N_H(x,t)}{\partial t} = D_H \frac{\partial^2 N_H(x,t)}{\partial x^2} \tag{2}$$

Where, D_H is the diffusion constant of Hydrogen. The solution of this differential equation has the well-known form [23],

$$N_H(x,t) = N_H^0 erfc\left(\frac{x}{2\sqrt{D_H t}}\right) \tag{3}$$

When a Si–H breaks, every dangling Si bond is associated with a free H atom in the oxide [7], which therefore allows one to write the following,

$$N_T = \int_0^{2\sqrt{D_H t}} N_H(x,t)dx \tag{4}$$

where, $2\sqrt{D_H t}$ denotes the diffusion length. (4) can be further simplified, by calculating the integral in (4) using (3) as,

$$N_T = 2\sqrt{D_H t} \times N_H^0 \times 0.51 \approx N_H^0 \sqrt{D_H t} \tag{5}$$

Furthermore, the rate of the trap growth is proportional to the diffusion of H away from the interface governed by the following equation [6],

$$\frac{dN_T}{dt} = -D_H \left.\frac{dN_H}{dx}\right|_{x=0} \tag{6}$$

At the interface, this simplifies to the following using (3),

$$\frac{dN_T}{dt} = N_H^0 \sqrt{D_H / \pi t} \tag{7}$$

Using (5) and (7) one can rewrite (1) as the following,

$$N_H^0 \sqrt{D_H / \pi t} = K_F N_F - K_F N_H^0 \sqrt{D_H t} - K_R \left(N_H^0\right)^2 \sqrt{D_H t} \tag{8}$$

The solution of this quadratic equation has two roots, one of which can be neglected since N_H^0 cannot have a negative value. Hence, the only feasible solution is given by,

$$N_H^0 = \frac{\sqrt{\left(K_F\sqrt{D_H t} + \sqrt{D_H/\pi t}\right)^2 + 4K_F K_R N_F \sqrt{D_H t}} - \left(K_F\sqrt{D_H t} + \sqrt{D_H/\pi t}\right)}{2K_R\sqrt{D_H t}} \tag{9}$$

Using (5), we get the following expression for N_T,

$$N_T = \frac{\sqrt{\left(K_F\sqrt{D_H t} + \sqrt{D_H/\pi t}\right)^2 + 4K_F K_R N_F \sqrt{D_H t}} - \left(K_F\sqrt{D_H t} + \sqrt{D_H/\pi t}\right)}{2K_R} \tag{10}$$

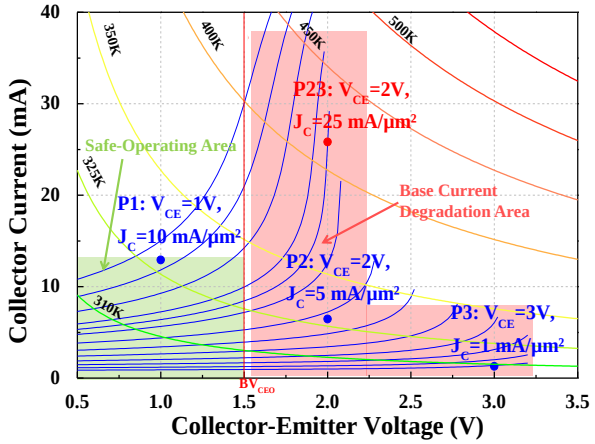

Fig. 2: Output characteristics of a SiGe HBT under test simulated using HICUM L2. Bias conditions of the (P1, P2 and P3) aging tests are also shown.

III. Device Description and Aging Tests

Preliminary DC Measurements/aging-tests were performed on SiGe NPN HBTs from Infineon Technologies [4, 24]. The DUTs in CBEBC configuration with a single drawn emitter size of 0.2×10 µm^2 have peak f_T/f_{MAX} of 240/380 GHz. To observe the evolution of the base and collector currents during aging tests, the Gummel plot of the device at V_{BC} = 0V has been recorded after fixed time intervals for a duration of 1000h [4]. Primarily, three stress bias conditions, P1, P2 and P3, close to the SOA edge of the technology, are used during the 1000h stress period, as highlighted in Fig. 2. The P1 bias

condition (V_{CE} = 1 V, J_C =10 mA/μm^2) is defined below BV_{CE0}. The other two bias points, P2 and P3, are defined above BV_{CE0} with V_{CE} = 2V, J_C =5 mA/μm^2 and V_{CE} = 3V, J_C =1 mA/μm^2, respectively. Another bias condition, P23, is chosen at same V_{CE} (=2V) as P2 but at higher J_C (=25mA/μm²) since P1 does not exhibit significant transistor degradation [4] and hence we focus on the results from P2, P23 and P3.

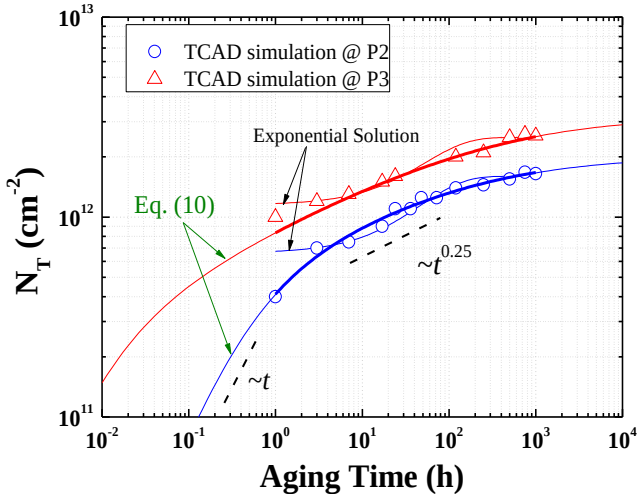

Fig. 3: Evolution of the trap density as a function of the aging time for the stress conditions P2 and P3 (symbols: TCAD, lines: analytical model (10)).

Equation (10) is plotted in Fig. 3 as a function of aging time shown in comparison with the conventional $t^{0.25}$ power law [2, 7-9] and the exponential solutions [4]. The analytical solution is compared with results obtained from TCAD simulation, which accounts for the degradation by introducing traps at the emitter-base periphery [4], showing good agreement during the entire degradation phase. The expression of N_T in (10) captures three specific regimes of the degradation. Firstly, for very small t, the degradation is simply proportional to t since the rate of trap generation remains constant in this phase. Secondly, when sufficient traps are generated, the degradation is diffusion dominated and the trap density follows the well-known $t^{0.25}$ relation. The third phase is the saturation of the trap density when all the available bonds are broken. From Fig. 3, it is evident that the analytical solution in (10) can capture the effects of both the power and the exponential law, ensuring accuracy and retaining the physical meaning of the reaction-diffusion theory. Table I summarizes the parameter values used in the model for stress conditions P2 and P3. Note that the slightly different values of N_F for P2 and P3 are due to process variation between two HBTs under test.

IV. Aging Model Implementation and Validation

The evolution of electrical characteristics during the aging has been attributed to trap activity at the emitter-base junction periphery [4, 17-18]. In the HiCuM compact model [25], the base current in this region is modeled by:

TABLE I: Model Parameter Values for Stress Conditions P2 and P3

Stress Bias	Junction Temp. (K)	D_H (cm^{2}s^{-1})	K_F (s^{-1})	K_R (cm^{3}s^{-1})	N_F (cm^{-2})
P2	325	4.5×10^{-10}	8.5×10^{-5}	6×10^{-19}	2.2×10^{12}
P3	310	1.5×10^{-10}	10^{-3}	1.5×10^{-18}	2.8×10^{12}

$$I_{jBEp} = I_{BEpS}\left[\exp\left(\frac{v_{BE}}{m_{BEp}V_T}\right)-1\right] + I_{REpS}\left[\exp\left(\frac{v_{BE}}{m_{REp}V_T}\right)-1\right] \quad (11)$$

Where, the saturation currents I_{BEpS} and I_{REpS} as well as the non-ideality factors m_{BEp} and m_{REp} are model parameters. The degradation due to hot carriers in the E-B spacer also causes an excess non-ideal base current via trap-assisted Shockley-Read-Hall (SRH) recombination [5]. Also, the evolution of the SRH recombination current in the E-B spacer region has a similar evolution as the trap density [4, 18-20]. Thus, the base current increase can be attributed to the recombination current parameter in the periphery, I_{REpS}. The other parameters in (11) including m_{REp} remain constant. Hence the evolution of excess I_{REpS} with aging time can be written similar to (10) as,

$$\Delta I_{REpS} = \frac{\sqrt{\left(K_{F,I}\sqrt{D_H t}+\sqrt{D_H/\pi t}\right)^2 + 4K_{R,I}K_{R,I}I_F\sqrt{D_H t}} - \left(K_{F,I}\sqrt{D_H t}+\sqrt{D_H/\pi t}\right)}{2K_{R,I}} \quad (12)$$

Here, $K_{F,I}$ is the rate of the forward reaction, in s^{-1}, $K_{R,I}$ is the rate of trap annihilation, in cmA^{-1}s^{-1}, and I_F is the final value of ΔI_{REpS}, in A, when all the available bonds are broken. Here, the parameters $K_{F,I}$ and $K_{R,I}$ are functions of the stress conditions. Additionally, junction temperature (T_j) dependence of D_H is considered (D_H (T_j) = $D_0 e^{-E0/kTj}$), with D_0=9.41×10^{-3} cm²/s, E_0=0.48 eV) [9]. Implementation of this aging law in Verilog A cannot be done in the same manner as [4], by representing it in the form of a differential equation of I_{REpS}, due to the computational complexity of (12). Therefore, we have implemented the function f (t) = t, using a differential equation of the form, df /dt=1. The solution of this differential equation has been used in place of the variable t in (12). The implementation of the function $f(t)$ has been done using an additional fictitious transistor node, as shown in Fig. 4 (a), similar to earlier implementations of aging laws [4, 18]. Since the variation of the base current takes hours to become observable, the Aging Time Scale Factor (ATSF) has been used here [4, 18-20] in order to reduce the simulation time down to a few nanoseconds equivalent to several thousand hours of measured aging. Hence, the differential equation for implementing f (t) has been represented as df/dt=ATSF. For our simulations, the parameter ATSF is fixed at 3.6×10^{14} to simulate 1000h of aging in equivalent time duration of 10ns. In addition, I_F, $K_{F,I}$ and $K_{R,I}$ are the three model parameters. In the modified HiCuM model I_{REpS} is no more a model parameter, but is calculated following (12). For clarification purposes the new model is named HiCuM-AL, where 'AL' stands for aging law. Fig. 4 (b) represents the evolution of the normalized excess base current ($\Delta I_B/I_{B0}$) at V_{BE} = 0.65V, obtained from both measurement and simulation, under P2 and P3 stress conditions, showing a good accuracy of the proposed model given in (12). In addition, the measured value of the normalized excess base current for the P23 bias condition is also compared with the aging model simulation which also demonstrates good model accuracy. In all three cases the extracted values of the aging model parameters ($K_{F,I}$, $K_{R,I}$ and I_F) are shown in table II. Interestingly, a gradual increase of the rate constants ($K_{F,I}$ and $K_{R,I}$) are observed as stress bias is increased from P2 to P3, while P23 shows a slightly different parameter set due to process variation between separate transistor sets. Fig. 5 (a) compares simulation results with measurements depicting the Gummel plot evolution under P3

stress condition after four stress intervals, in addition to the initial plot (0, 1, 7, 72, 1000h). A zoomed view of base-current shown in Fig. 5 (b) demonstrates very good agreement between measurement and simulation at all aging times.

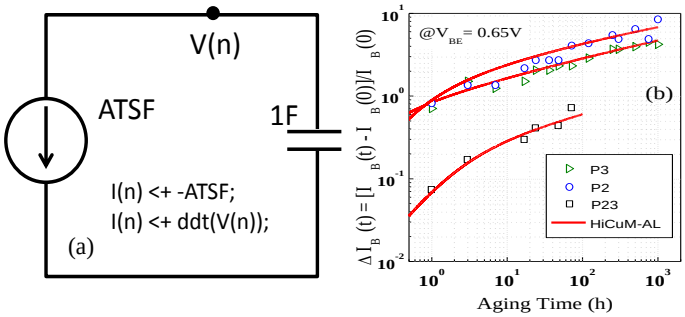

Fig. 4 (a): Equivalent circuit representation of the additional transistor node for aging law implementation in HiCuM model; (b) Comparison between measurement and HiCuM-AL simulation showing the evolution of the normalized excess base current at V_{BE} = 0.65 V for P2 and P3.

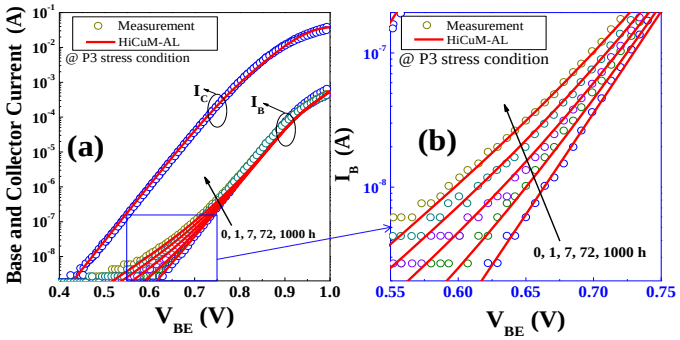

Fig. 5: Comparison between measurement and HiCuM-AL model simulation: (a) Gummel plot after five different stress intervals under P3 condition, (b) a close up of the base current variation in the V_{BE} range of 0.55 -0.75V.

V. Extended Validation on Different Technologies

In this section, we test the versatility of the aging model under various aging conditions through comparison between model simulation and measurement results of aging tests on different SiGe HBT technologies. First, the model is validated against aging test results from SiGe HBTs reported in [22]. Incidentally, the HBTs reported in this work are also from Infineon technologies (stress conditions being different) and an initial model calibration is done using the same scalable model card used in case of the HBTs in section IV, to perform more reliable aging parameter extraction. Figure 6 shows the model comparison with the measurements, depicting a good accuracy of the aging model.

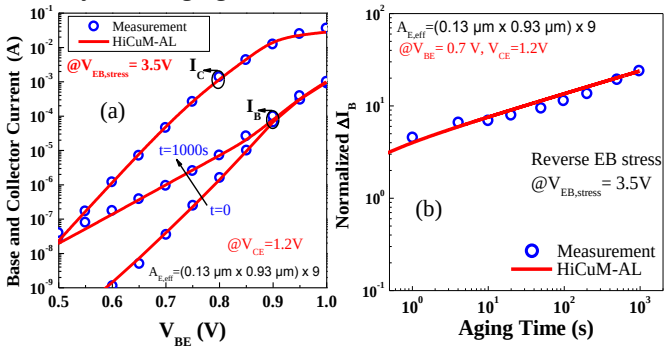

Fig. 6: Comparison between measurement [22] and HiCuM-AL model simulation: (a) Initial Gummel plot at V_{CE}=12V for initial and after 1000s of stress under the reverse E-B stress condition V_{EB}=3.5V at 300K, (b) the evolution of the normalized excess base current at V_{BE} = 0.7 V and V_{CE}=1V.

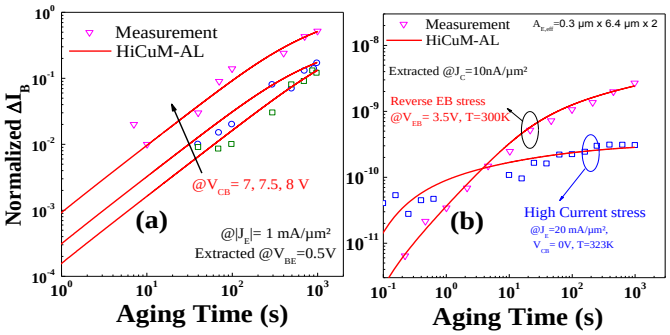

Fig. 7: Relative evolution of the normalized ΔI_B versus stress time for a wide range of stress conditions comparing measurement and HiCuM-AL model simulation: (a) at constant J_E for different V_{CB} extracted at V_{BE}=0.5V [15] and (b) for reverse E-B and high current stress extracted at J_C = 10 nA/µm² [21].

Figure 6 (a) shows the forward Gummel plot at a V_{CE} of 1.2V for the pre-stress condition and after a 1000s of reverse E-B stress at 3.5V. Figure 6(b) shows the base current degradation, ΔI_B, under $V_{EB\text{-}stress}$ of 3.5V extracted at V_{BE} = 0.7V and V_{CE} =1.2V. Extracted aging parameter values are shown in table II. Next, we compare the aging simulation with results of aging tests carried out on NPN SiGe HBTs reported in [15] and [21]. Considering that the entire degradation is observable in the base current, model simulation of (12) is sufficient to describe the measurement results. The mixed-mode aging bias conditions in [15] include high current stress at constant J_E =1 mA/µm² under three different V_{CB} stress voltages (7, 7.5 and 8 V), whereas in [20], results from both a reverse E-B stress at V_{EB}=3.5V (open collector) and a high current stress at V_{CB}=0V, J_E=20 mA/µm² (T=323K) for a stress duration of 1000s are reported. Aging simulations are performed and aging model parameters are extracted for all the stress conditions (values summarized in table II). Figs. 7 (a) and (b) shows the evolution of the post-stress excess base current normalized by its pre-stress value, depicting a good agreement between the aging model and the experimental results from both [15] and [21]. This illustrates the versatility of the aging model in (12) under various aging bias conditions. Also, the extracted values (table II) of the rate constants ($K_{F,I}$ and $K_{R,I}$) show an increasing dependence on the stress conditions.

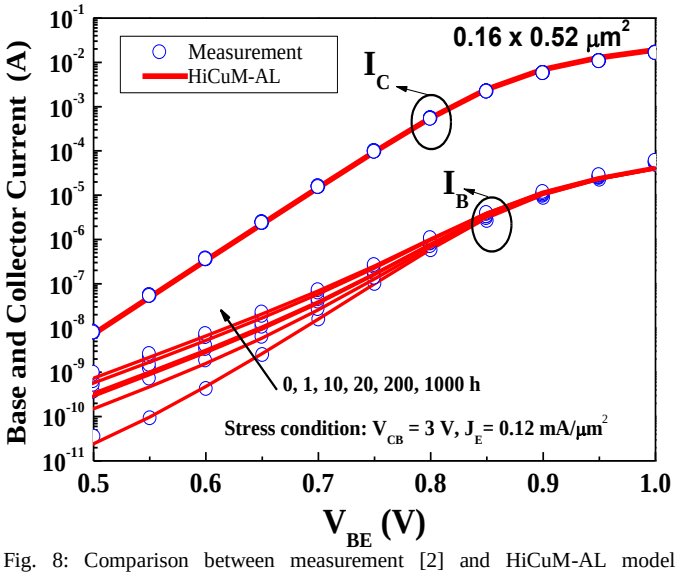

Fig. 8: Comparison between measurement [2] and HiCuM-AL model simulation showing the Gummel plot at five different stress intervals under the mixed-mode stress condition V_{CB}=3 V and J_E=0.12 mA/µm².

To further assess the capabilities of the aging model, the results from mixed-mode aging tests on SiGe HBTs of IHP's 0.13 µm BiCMOS technology [2, 3] have been compared with model simulations. These HBTs are high speed transistors with transit frequencies f_T/f_{max} = 250 GHz/300 GHz and breakdown voltages BV_{CEO}/BV_{CBO}=l.7 V/5.0 V, respectively. First, an initial fit to the pre-stress DC characteristics with HiCuM model was done to calibrate the model to the initial conditions using a scalable model card provided by IHP [3].

Next, the aging simulations were performed to compare with the measured base-current degradation under different mixed-mode stress conditions and corresponding values of the aging model parameters were extracted (values summarized in table II for different stress conditions). Similar to the observation for the parameters corresponding to Figs. 4(b), 6 and 7 (b), a gradual increase of the rate constant values has been observed as stress bias increases. The model simulation results are shown in comparison with the evolution of measured forward Gummel characteristics, for the stress condition V_{CB} = 3V and J_E = 0.12 mA/µm², in Fig. 8 showing an excellent agreement between the model and the experimental aging characteristics. Figure 9 shows the comparison between the simulated and experimental normalized base current degradation (ΔI_B) as a function of the aging time, under different mixed-mode stress conditions, depicting a good accuracy of the aging model.

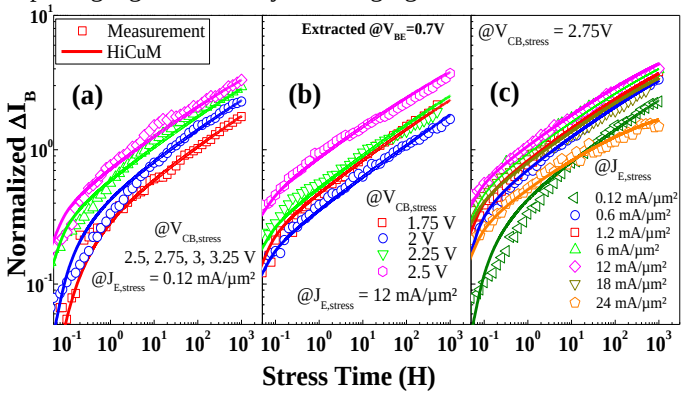

Fig. 9: Comparison between measurement [2] and HiCuM-AL simulation: Evolution of excess base current at V_{BE} = 0.7 V under $J_{E,stress}$ of (a) 0.12, (b) 12 mA/µm² for different $V_{CB,stress}$ and (c) $V_{CB,stress}$=2.75V for different $J_{E,stress}$.

VI. Discussions

Figure 10 shows the extracted values of the trap rate constants ($K_{F,I}$ and $K_{R,I}$) plotted as a function of the stress bias, obtained from the simulation shown in Fig. 9. It is observed that while $J_{E,stress}$ is kept constant, both $K_{F,I}$ and $K_{R,I}$ increase with $V_{CB,stress}$ following an exponential dependence. On the other hand, while $V_{CB,stress}$ is kept constant, the generation rate, $K_{F,I}$, demonstrates a peak value before starting to roll off. This is consistent with the behavior of ΔI_B in Fig. 9 (c). At such high stress current densities (V_{CB} = 2.75V and J_E = 18 mA/µm²) due to a decrease in the C-B electric field at the onset of the Kirk effect [8], the ΔI_B is reduced. In [2, 3] ΔI_B is expressed as an empirical function of the stress conditions ($V_{CB,stress}$, $J_{E,stress}$) to express this behavior. A similar expression is valid for $K_{F,I}$ which can be written as,

$$K_{F,I} = C_{MM,F} \exp\left(\mu_{0,F} V_{CB,stress}\right)\left[1/\left|J_{E,stress}\right| + \left|J_{E,stress}\right|/J_{Ehc,F}\right]^{\varepsilon_F} \quad (13)$$

TABLE II: Aging Model Parameters for Different Technologies

Tech.	Stress Bias Conditions	$K_{F,I}$ (s^{-1})	$K_{R,I}$ ($cmA^{-1}s^{-1}$)	I_F (A)
This work	P2: J_C=5mA/µm², V_{CE}=2V	2×10^{-5}	1.45×10^{7}	2×10^{-13}
	P3: J_C=1 mA/µm², V_{CE}=3V	6×10^{-5}	2.2×10^{7}	2×10^{-13}
	P23: J_C=25 mA/µm², V_{CE}=2V	1.8×10^{-6}	6×10^{7}	1×10^{-13}
Ref. [22]	$V_{EB\text{-}Stress}$=3.5V	1.5×10^{-2}	7×10^{7}	2×10^{-11}
Ref [15]	J_E=1mA/µm², V_{CB}=7V	2.5×10^{-5}	2×10^{9}	5×10^{-16}
	J_E=1mA/µm², V_{CB}=7.5V	5×10^{-5}	6×10^{9}	5×10^{-16}
	J_E=1mA/µm², V_{CB}=8V	1×10^{-3}	2.1×10^{10}	5×10^{-16}
Ref. [21]	V_{CB}=0V, J_E = 20 mA/µm², T=323K	5×10^{-1}	5×10^{10}	1×10^{-15}
	V_{EB} = 3.5V, T=300K	3×10^{-3}	2×10^{8}	2.2×10^{-14}
Ref. [2]	J_E=0.12 mA/µm², V_{CB}=2.5V	2.25×10^{-5}	1.8×10^{8}	3.5×10^{-14}
	J_E=0.12 mA/µm², V_{CB}=3V	1.4×10^{-4}	3.5×10^{8}	3.5×10^{-14}
	J_E=0.12 mA/µm², V_{CB}=3.25V	3.2×10^{-4}	5.5×10^{8}	3.5×10^{-14}
	J_E=12 mA/µm², V_{CB}=2V	6×10^{-4}	6.5×10^{9}	3.5×10^{-14}
	J_E=12 mA/µm², V_{CB}=2.5V	4×10^{-3}	7.5×10^{9}	3.5×10^{-14}

Where, the values chosen to fit the $K_{F,I}$ in Fig. 10 (a) are $C_{MM,F}$ =1.5×10^{-7}, degradation acceleration exponential factor $\mu_{0,F}$ = $3V^{-1}$, empirical fit factor $J_{Ehc,F}$ =105 mA/µm² and power exponent ε_F = -1.3. Although (13) is an empirical function, it is consistent with the simulated carrier generation (by impact ionization) rates at the B-C junction under the mixed-mode stress conditions [2, 8]. Trap annihilation rate demonstrates a slower variation with J_E and V_{CB} compared to $K_{F,I}$, which can be written using a similar empirical expression as (13),

$$K_{R,I} = C_{MM,R} \exp\left(\mu_{0,R} V_{CB,stress}\right)\left[1/\left|J_{E,stress}\right| + \left|J_{E,stress}\right|/J_{Ehc,R}\right]^{\varepsilon_R} \quad (14)$$

Where, $C_{MM,R}$ =2×10^{7}, $\mu_{0,R}$ = $1.5V^{-1}$, $J_{Ehc,R}$ = 355 mA/µm² and ε_R = -0.85 are chosen to fit $K_{R,I}$ in Fig. 10 (b). While $K_{R,I}$ is a weaker function of stress bias, at higher J_E, both generation and recombination rates roll-off, with $K_{F,I}$ decreasing earlier and faster than $K_{R,I}$. Their combined effect likely produces a reduction of ΔI_B observed at higher stress currents.

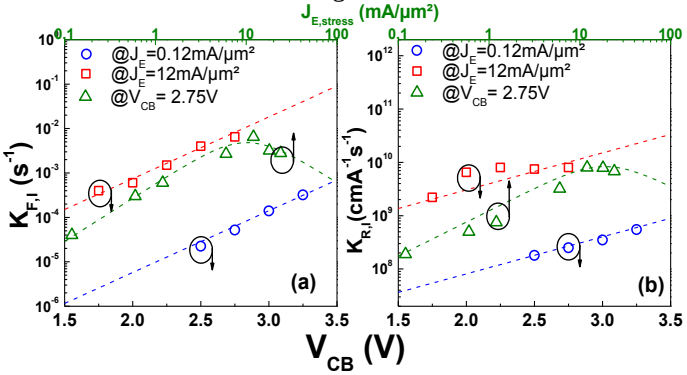

Fig. 10: Evolution of (a) $K_{F,I}$ and (b) $K_{R,I}$ for different $V_{CB,stress}$ and $J_{E,stress}$.

The current version of the aging model has been implemented keeping in mind that the parameters N_F and I_F are process-dependent and their values may vary with technology. While this could be easily managed using already available dedicated statistical software tools to account for the process variability in circuit simulation, in the current scope, this aspect is

omitted. Also, bias dependence of the $K_{F,I}$ and $K_{R,I}$ parameters need further exploration across a wider range of technologies and thus might require additional modeling effort.

VII. Conclusion

An aging compact model based on complete and analytical solution of the R-D framework has been proposed in this paper that can predict the physics of the entire hot carrier degradation phase quite accurately for modern HBTs. Due to absence of recovery, it has been shown that the aging compact model based on R-D framework is sufficient to describe device degradation accurately for bipolar circuit operation close to SOA. Implementation of the aging model is quite simple and versatile and it can be used for any aging law of analytic form. In all the different SiGe HBT technologies we have studied in this work, a good agreement between the model and measurements confirm the accuracy and versatility of the aging model. Given circuit designers' concern of reliable and stable circuit operation close to SOA limits, the proposed model will prove essential for predicting the degradation accurately at transistor level and, in the long run, for predicting reliability-aware circuit architectures.

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