96 GHz 4.7 mW low-power frequency tripler with 0.5 V supply voltage

W. Liang, A. Mukherjee, P. Sakalas, A. Pawlak and M. Schröter

Using forward biased base-collector voltage (V_{BC}) in high-speed circuits is usually not attractive due to the performance degradation compared with biasing heterojunction bipolar transistors (HBTs) in the forward-active region. However, the use of ultra-low supply voltage in millimeter-wave (mm-wave) circuits provides an interesting application scenario not only for demonstrating the potential of modern silicon germanium (SiGe) HBT technologies in implementing severely power-constrained wireless circuits on silicon but also for verifying the accuracy of compact models beyond standard characteristics typically measured by foundries. This paper presents the results of a 96 GHz frequency tripler deliberately designed with a reduced supply voltage (0.5 V) in a 130 nm SiGe HBT technology. With only 4.7 mW DC power consumption, this frequency tripler achieves a conversion loss of 3.8 dB, generating a 96 GHz output signal with only -10 dBm input signal at 32 GHz. The impact of transistor series resistances on the tripler performance is also analyzed.

Introduction: Maximum performance of mm-wave circuits is typically achieved by biasing SiGe HBTs at as large as possible reverse V_{BC}, while operation in saturation is often discouraged due to both performance degradation and inaccurate modelling in the saturation region. But a forward biased V_{BC} does not mean high-current injection and excess charge in the collector as long as the collector current density J_C is kept below peak transit frequency f_T. Especially when considering the performance advantage of modern SiGe HBT technologies over CMOS counterparts, it becomes attractive to implement silicon-based ultra-low power mm-wave circuits without excessively degrading the circuit performance. Inaccurate HBT modeling has been overcome here by employing the High-Current Model (HICUM) Level2 (L2) that, from its original conception, has included an accurate description of the stored charge in saturation and quasi-saturation operation [1], and is thus excellent candidate for designing circuits with reduced supply voltages and exploring the trade-offs encountered in low-power mm-wave circuit design.

In accordance with the practical needs towards lowering the power consumption of high-speed wireless systems, there has already been previous work on designing mm-wave circuits at low collector-emitter voltages. In [2] and [3], low-noise amplifiers (LNAs) for the 8-12 GHz and 10-22 GHz bands were designed with reduced supply voltages, while in [4] a 65 GHz LNA was implemented in a 130 nm SiGe HBT process. But to the authors' knowledge, circuits with a forward-biased base-collector junction around 94 GHz have not yet been reported. This paper introduces a frequency tripler designed with only 0.5 V collector supply voltage, aiming to explore the question on how far operation at low V_{CE}, in particular, at forward biased V_{BC}, might be beneficial for significantly reducing the DC power dissipation of mm-wave circuits without significantly compromising their high-frequency performance.

Circuit design: The topology of the frequency tripler consists of two parts: the harmonic generation part and the output buffer amplifier. The schematic of the core part of this frequency tripler is shown in Fig. 1.

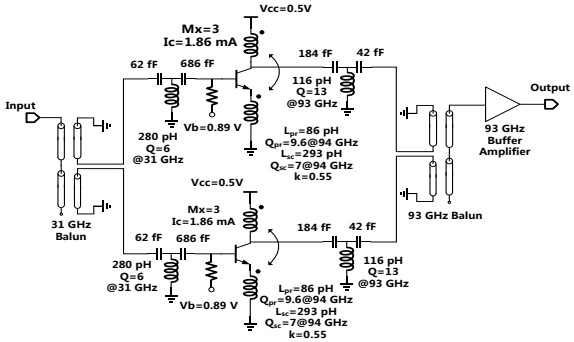

Fig. 1 Schematic of the harmonic generation part of the frequency tripler

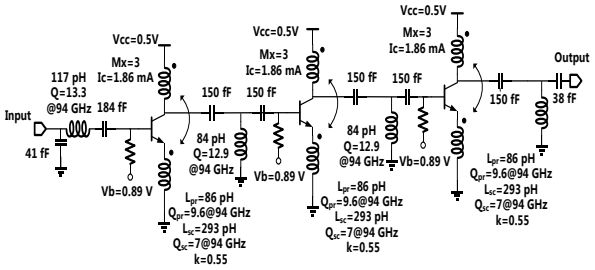

Fig. 2 Schematic of the buffer amplifier part of the frequency tripler.

Differential configuration is used in the harmonic generation part to suppress the even order harmonic signal, with the use of on-chip baluns for single-ended-to-differential conversion. Coupled inductors help to make it very easy to simultaneously implement DC decoupling and high frequency (HF) impedance matching to input/output baluns, with some sacrifice in conversion loss. The transistors used in the core harmonic generation cells have an emitter size of 0.07 μm × 0.9 μm × 3. The DC power consumption of the harmonic generation part is 1.9 mW with a 0.5 V supply voltage.

A buffer amplifier is used at the output of the harmonic generation part of the frequency tripler, to increase the output signal power. The schematic of the buffer amplifier is shown in Fig. 2. Emitter-collector transformer feedback is used extensively for improving both reverse isolation for ease of impedance matching and the stability of the buffer amplifier. The supply voltage of the buffer amplifier is also chosen as 0.5 V to reduce the DC power consumption of the buffer amplifier to 2.8 mW. All the component values used in the frequency tripler are given in Fig. 1 and Fig. 2, and the total power dissipation is 4.7 mW.

Experimental results: The frequency tripler was fabricated in an experimental 130 nm SiGe HBT technology from IHP Microelectronics [5]. The microphotograph of the chip is shown in Fig. 3 along with the 3D views of the input/output baluns and the core of harmonic generation circuit. The chip size is 0.66 ×1.1 mm^2. The output power of the frequency tripler was measured using an R&S spectrum analyzer with an FS-Z110 75-110 GHz harmonic mixer.

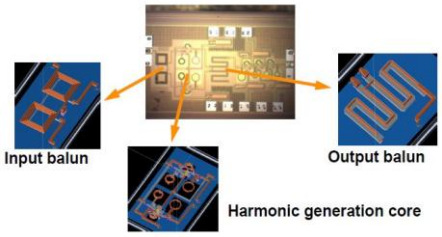

Fig. 3 Microphotograph of the frequency tripler chip, along with the 3D views of the baluns and the core layout.

Fig. 4 shows the conversion loss of the frequency tripler measured with an input signal power of -10 dBm over the input frequency range from 26 GHz to 36 GHz. The minimum conversion loss is 3.8 dB when generating a 96 GHz output signal. Furthermore, the reduction to 0.4 V collector supply voltage and 0.84 V base voltage with thus 1.6 mW total power dissipation shows 10.4 dB measured conversion loss at -2.5 dBm input power at 96 GHz, as indicated by Fig. 4.

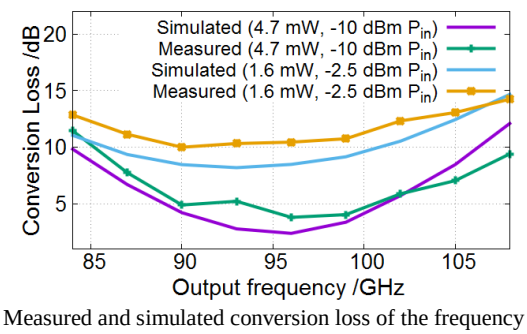

Fig. 4 Measured and simulated conversion loss of the frequency tripler.

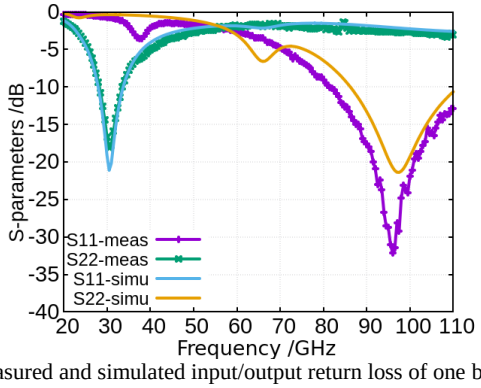

Fig. 5 Measured and simulated input/output return loss of one break-out cell in the harmonic generation part of the frequency tripler.

The small-signal input/output return loss results shown in Fig. 5 are measured from one break-out single-ended harmonic generation cell without balun. The data confirms that the strongest output signal occurs at around 96 GHz with an input at around 32 GHz. The excellent agreement of the simulation with the measurement resulted in first path success of the fabricated circuits.

Based on the good agreement between simulation and measurement HICUM/L2 was used to investigate the impact of transistor series resistances on the simulated conversion loss at 96 GHz with -10 dBm input signal power as shown in Fig. 6. At ±10% variation, the impact on the simulated conversion loss variation is 33% for the emitter resistance r_E, 20% for the external base resistance r_{Bx}, 12% for the external collector resistance r_{Cx}, and 6% for the internal base resistance r_{Bi}.

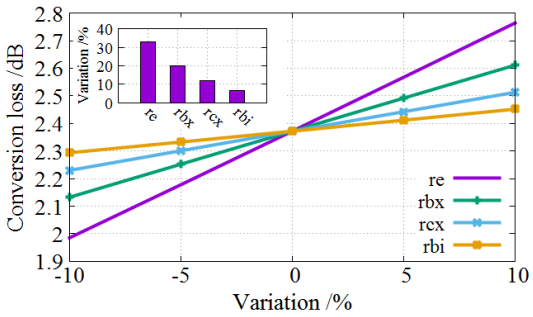

Fig. 6 The variation of simulated conversion loss at 96 GHz with swept HICUM/L2 model parameter values. The inset shows the variation of conversion loss in percentage.

Table 1: Performance comparison with previously reported W-band low-power frequency triplers.

Ref	[6]	[7]	[8]	This work
Tech	90 nm CMOS	90 nm CMOS	90 nm CMOS	130 nm SiGe
Freq (GHz)	90 ~ 115	91.2 ~ 97.2	75 ~ 87	88 ~ 103
P_{in} (dBm)	-2.5 ~ 14	-1	0	-10
G_c (dB)	-40 ~ -2	< -12	< -18	-6.8 ~ -3.8
P_{DC} (mW)	17	1.7	7.05	4.7

(P_{in}: input power; G_c: conv. gain; P_{DC}: total DC power consumption)

The performance of this frequency tripler is summarized in Table 1 along with the performance of some other reported W-band low-power frequency triplers. The work in [7] has also demonstrated an ultra-low power frequency tripler using the injection-locking mechanism, but compared to this work, the required input signal power and conversion loss with 0.7 V supply voltage are more than two times higher. The results of the frequency tripler reported in this work demonstrate that utilizing high-speed SiGe HBTs biased in the saturation region has a potential for implementing a functional W-band frequency tripler with competitive performance while greatly reducing the DC power consumption. Also notice that the presented design has been based on a relaxed and thus cost efficient lithography node (130 nm).

Conclusion: Biasing the HBTs in saturation at 0.5 V collector-emitter voltage, a W-band low-power frequency tripler was implemented in a 130 nm high-speed SiGe HBT technology. The HF performance of the tripler (incl. the buffer) was demonstrated to be highly competitive with existing designs in more advanced CMOS process nodes at a lower power consumption. Furthermore, with careful design and utilizing an accurate physics-based compact model (HICUM/L2), first path success of the fabricated circuits was achieved. The demonstrated excellent agreement between simulation and measurement also enables a meaningful analysis of the impact of transistor parameters and further supply voltage reduction on HF circuit performance.

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