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A Compact Formulation for Avalanche Multiplication in SiGe HBTs at high injection levels

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Abstract— **This paper presents a unified physical formulation for the avalanche effect in SiGe HBTs at different injection levels. Based on an analytical description of the resulting electric-field distribution, a closed-form analytical expression for the multiplication factor is derived and has been implemented in the HICUM compact model. The model accuracy close to and beyond the common-emitter breakdown voltage BV_{CEO} has been assessed over a wide temperature range by comparison to measurements of SiGe HBTs with different collector doping profiles and emitter geometries.**

***Index Terms*— SiGe HBTs, compact model, impact ionization, avalanche, Kirk effect, high injection, safe operating area (SOA)**

I. Introduction

ADVANCED Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs) have almost reached the THz range [1] and are expected to be well-suited for THz applications [2]. But boosting the frequency performances of HBTs has led to decreasing breakdown voltages. Thus, circuit operating at higher frequencies forces devices to operate closer to their physical limits in order to compensate for the loss of output power. This requires an accurate description of the transistor behavior in all operation regimes [3] [4], in particular when approaching the Safe Operating Area (SOA) limit. The degradation mechanisms that may occur in this operation regime have been discussed in [5] [6].

Several mechanisms dominate the SOA edges as presented in Fig. 1.a). For present SiGe HBTs, the impact ionization (also known as the avalanche effect) occurring in particular in the base-collector (BC) space charge region (SCR) causes a major limitation of the achievable output power. The well-known weak avalanche regime [7] is defined by a carrier multiplication factor only slightly larger than one and can be characterized through the open-base breakdown voltage BV_{CEO}. In contrast, the strong avalanche regime features a carrier multiplication factor much larger than one and is limited by the open-emitter breakdown voltage BV_{CBO}. Further SOA edges are defined by self-heating in the high power area which may result in the current pinch-in effect (current crowding at the center of the emitter) [3] [8] [9].

In order to address different circuit applications with a single technology platform, different transistor flavors are available, which are listed in the table below for the technology investigated in this work [10].

	High Speed (HS)	Medium Voltage (MV)	High Voltage (HV)
f_T (GHz) @V_{BC} = 0V	320 @J_C=8mA/μm^2	180 @J_C=2mA/μm^2	70 @J_C=0.8mA/μm^2
BV_{CEO} (V)	1.5	1.8	3.2
BV_{CBO} (V)	5.2	6.7	13.5

Table 1: Performances of the BiCMOS055 technology from STMicroelectronics for three different flavors

High-speed transistors are dedicated to high frequency applications, high voltage transistors are tailored towards high power applications and medium voltage transistors are designed for trade-offs between power and HF applications.

The main difference of the HV device with respect to the HS architecture is its low-doped collector (epi-layer) at the BC junction. Due to this low doping, this transistor is very sensitive to high-current effects. In addition, power applications require a collector-base (or collector–emitter) voltage range as large as possible, leading to operating points beyond BV_{CEO}. Inductive loads can lead to a combination of high-current effects with impact ionization and a device behavior which has not been accurately modeled so far. In addition, the impact of a spatially

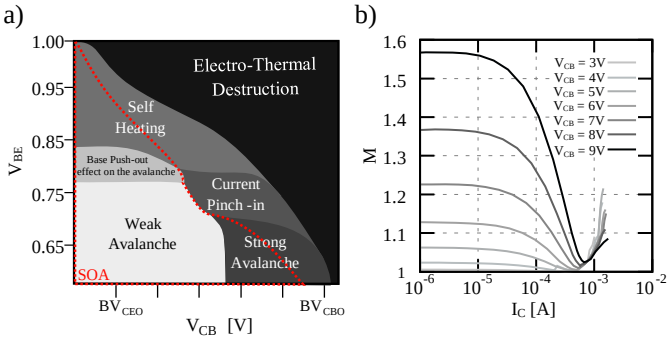

Fig. 1.a) Schematic of the base-emitter voltage as a function of the collector-base voltage showing the different mechanisms that dominate the transistor operation regimes. (b) TCAD simulation results of the avalanche multiplication factor as a function of the collector current for a lightly constant doped SiGe HBT (I_{LIM}=0.7mA, N_{epi}=10^{17} cm^{-3}).

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varying collector doping profile will also be analyzed. This paper is organized as follows:

Section II describes an analytical formulation for the avalanche regime including high current effects, as well as its implementation into HICUM, which is used as a vehicle for the evaluation. Section III presents the measurement set-up and the validation of the model formulation. First, it is applied to different device flavors of the BiCMOS055 technology (see table 1). Next, its scalability is investigated for different emitter widths and lengths. Finally, the temperature dependence is explored.

II. Impact Ionization in HBTs

In the following section, the emitter window width W is equal to 100 nm and its window length L is 4.42µm.

A. Model Formulation and Limitations

The impact ionization in bipolar transistors appears in the volume of the structure within the base-collector space-charge-region (BC-SCR) [5]. The physical origin of the avalanche effect is the high electric field in the BC-SCR, where some of the electrons acquire sufficient kinetic energy to generate electron-hole pairs through impact ionization. Those additional carriers contribute to the avalanche current I_{AVL} and are quantified by the multiplication factor M, defined as the ratio of the number of carrier leaving the BC-SCR at the collector end divided by the number of carriers entering the BC-SCR at the base end.

Therefore, the transfer current I_T can be directly calculated as

$$I_C = M\, I_T = I_T + I_{AVL} \tag{1}$$

The expression of the multiplication factor as a function of the electric field has already been given in [11]

$$1 - \frac{1}{M} = \int_0^{w_{BC}} a \exp\left(-\frac{b}{|E(x)|}\right) dx \tag{2}$$

with a and b as material dependent parameters and w_{BC} as the width of the BC SCR. Based on (2), an analytical formulation for describing weak avalanche is used in many compact models such as VBIC [12], HICUM [13], and MEXTRAM [14] :

$$M - 1 = f_{AVL}(V_{DCi} - V_{B'C'}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})}\right) \tag{3}$$

Here, $f_{AVL}(= a/b)$ and $q_{AVL}(= b)$ are model parameters related to impact ionization, C_{jCi} represents the internal BC depletion capacitance, and $V_{DCi} - V_{B'C'}$, is the internal potential difference across the BC-SCR.

This expression gives satisfying results for the weak avalanche regime. Based on (2), recently (3) has been extended towards the strong avalanche regime [15] [16] according to

$$M - 1 = \frac{f_{AVL}(V_{DCi} - V_{B'C'}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})}\right)}{1 - k_{AVL}\, f_{AVL}(V_{DCi} - V_{B'C'}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})}\right)} \tag{4}$$

where k_{AVL} is the avalanche parameter related to the strong avalanche phenomenon. Fig. 2 shows a comparison between the model using expression (4) and the measurement for the absolute value of the base current I_B as a function of the CB voltage. The base current sign reverses at $V_{CB} = BV_{CEO}$-V_{BE} due to the increase of the avalanche current. Then, further increasing V_{CB} leads to a negative base current, until BV_{CBO}. The model with equation (4) is accurate enough at low injection levels. However, towards higher injection, deviations can be observed, as shown in Fig. 2. This is related to high current effects and particularly pronounced for the HV-HBTs featuring low collector doping. For HS transistors, the avalanche effect is partially masked by self-heating. The stronger temperature increase leads not only to an increase in I_C but also to a decrease in the ionization coefficients and hence the multiplication factor. Thus, eq. (4) yields reasonable accuracy up to higher injection levels. Hence, the focus will be mainly on HV transistors.

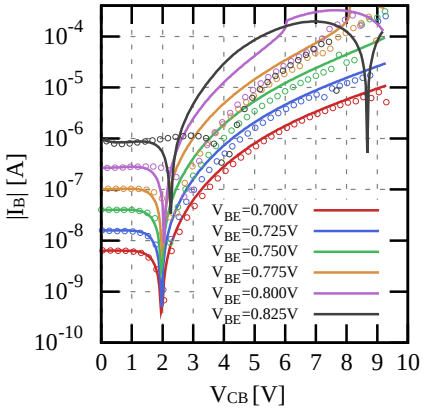

Fig. 2. Comparison between measurement (symbols) and model for HICUM/L2 version 2.4.0 (lines) at T=25°C for a HV transistor. Absolute value of the base current, $|I_B|$ as a function of collector-base voltage, V_{CB} for different constant base-emitter voltages at V_{BE}= 0.7V-0.825V. This plot is best viewed in the on-line color.

B. The impact of high-current effects on impact ionization

Fig. 1.b) shows TCAD simulation results of the multiplication factor as a function of the collector current for a SiGe HBT with a doping profile close to the BiCMOS055 technology [1] and for different V_{CB} ranging from 3V to 9V. It can be seen that M is not constant anymore at high I_C.

TCAD simulation results of the electric field distribution at the BC-junction for different current densities and at constant base-collector voltage for a transistor with a relatively low spatially independent collector doping concentration N_{epi} are shown in Fig. 3.a). With increasing the collector current density, the electric field in the epi-collector region changes its slope according to Poisson's equation [17].

$$\frac{\partial E}{\partial x} = \frac{q(N_{epi} - n)}{\varepsilon_{Si}} \tag{5}$$

where ε_{Si} is the permittivity of Si and q is the electron charge and n the electron concentration in the collector. Assuming saturation velocity, which is justified since the electric field in the BC-SCR must be sufficiently high for impact ionization to occur, (5) can be re-expressed as

$$\frac{\partial E}{\partial x} = \frac{qN_{epi}}{\varepsilon_{Si}}\left(1 - \frac{I_T}{I_{LIM}}\right) \tag{6}$$

and

$$I_{LIM} = q\, N_{epi}\, v_{S_n} A_E \tag{7}$$

where v_{S_n} represents the electron saturation velocity and A_E is the effective emitter area [18]. According to (6), the electrical field becomes horizontal at $I_T = I_{LIM}$. For $I_T > I_{LIM}$, the slope of the electrical field has flipped its sign and the peak of the field appears at the buried layer (end of the epi-collector). As a consequence, carrier multiplication depends on current density and reaches a minimum around $I_T = I_{LIM}$.

It is important to note that the electric field starts decreasing well before high-current effects are visible in the electrical characteristics such as the decrease of the transit frequency.

In order to obtain a closed-form solution for (6), the following section will discuss two asymptotic cases: $I_T < I_{LIM}$ and $I_T > I_{LIM}$. Depending on the slope of the electric field different boundary conditions apply for the solution of the Poisson equation.

1) Operation at $I_T < I_{LIM}$

Assuming a negligible voltage drop in the undepleted portion of the epi-collector (i.e. very low current densities or a narrow undepleted region), the electrical field is obtained by integrating (6) over the BC SCR with a zero-field boundary condition at $x = w_{BC}$. Thus, solving (6), the solution for the electric field is

$$E(x) = \frac{qN_{epi}}{\varepsilon_{Si}}\left(1 - \frac{I_T}{I_{LIM}}\right)(x - w_{BC}) \tag{8}$$

Therefore, with this solution for $E(x)$, the integral (2) can be solved as shown in the appendix (section V.A) and leads to the following expression for the multiplication factor

$$M - 1 = \frac{f_{AVL}\, E_{jC_{low}}\, w_{BC_{low}}\, e^{-\frac{q_{AVL}}{E_{jC_{low}} f_{corL}}}}{1 - f_{AVL}\, E_{jC_{low}}\, w_{BC_{low}}\, e^{-\frac{q_{AVL}}{E_{jC_{low}} f_{corL}}}} \tag{9}$$

The expressions for $E_{jC_{low}}$ and $w_{BC_{low}}$ are given in the appendix. Furthermore,

$$f_{corL} = \sqrt{1 - \frac{I_T}{I_{LIM}}} \tag{10}$$

Equation (9) tends to (4) under the condition $I_T << I_{LIM}$.

2) Operation at $I_T > I_{LIM}$

In this case, the current induces a space charge region of width w_{Ch} at the end of the epi-collector. A sufficiently simple solution for the corresponding electric field can only be obtained by assuming a negligible field in the (high current) injection zone ($x \le w_i$)

$$E(x) = \frac{qN_{epi}}{\varepsilon_{Si}}\left(1 - \frac{I_T}{I_{LIM}}\right)(x - w_i) \tag{11}$$

where w_i is the injection width. As the form of (11) is the same as (8) an expression similar to (10) is found for the multiplication factor. The only difference is that f_{corL} has to be replaced by

$$f_{corH} = \sqrt{\frac{I_T}{I_{LIM}} - 1} \tag{12}$$

3) Non constant doping concentration of the epi-layer

The above expressions (10) and (12) are valid for a constant doping profile in the epi-collector region. In order to account for the spatially dependent doping profile, different field distributions as shown in Fig. 3.b) need to be considered. Here, for enabling a direct comparison between constant and non-constant doping profile, the doping distribution has been chosen in such a way that the mean concentration over the entire epi-layer is the same. Therefore, I_{LIM} now changes with the depth and a horizontal field is reached locally at different depths x_{hor}. Thus, if I_T is increased beyond $I_{LIM}(x)$, the slope of the field is already negative for $x < x_{hor}$ while for $x > x_{hor}$ the slope is still positive. This leads to the bell shaped electric field distribution observed in Fig. 3.b) and its move towards the buried layer with increasing I_C.

Furthermore, the closed-form solution of the Poisson equation using an electric field distribution for a graded doping profile leads to a very complicated expression which is not suitable for a compact model. For the sake of efficiency, a simple relation

$$I_{LIM_{eff}}(I_T) = d_{AVL} I_{LIM} + h_{AVL}\, I_T \tag{13}$$

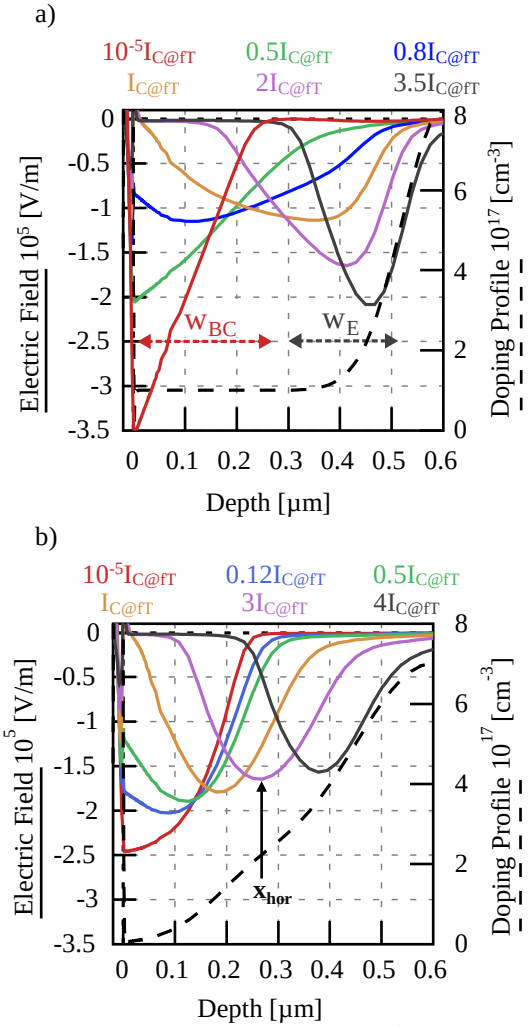

Fig. 3. TCAD simulation results showing the electric field distribution (y1) as a function of depth for different current densities at V_{CB}=3.5V in the BC-SCR showing the change of the slope sign at high current density (a) for a constant doping profile (dashed-lines) in the epi-collector region and (b) for an epi-layer with a graded doping profile (dashed-lines). This plot is best viewed in the on-line color.

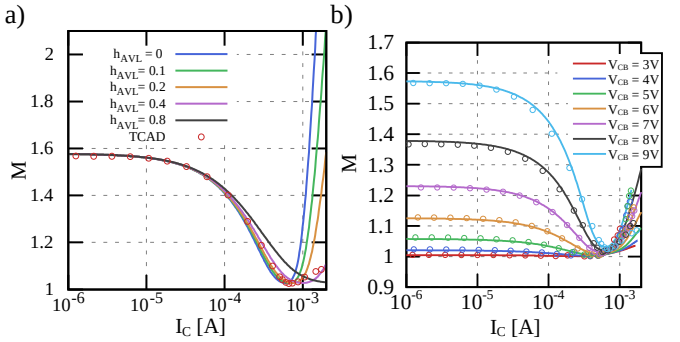

Fig. 4. Comparison of the multiplication factor as a function of the collector current for a graded doping profile (cf. Fig.3b) (a) for selected parameter values h_{AVL} (solid lines) and from TCAD simulations (symbols) at V_{CB}=9V and (b) for different V_{CB} from TCAD simulation (symbols) and from proposed model simulation (lines). This plot is best viewed in the on-line color.

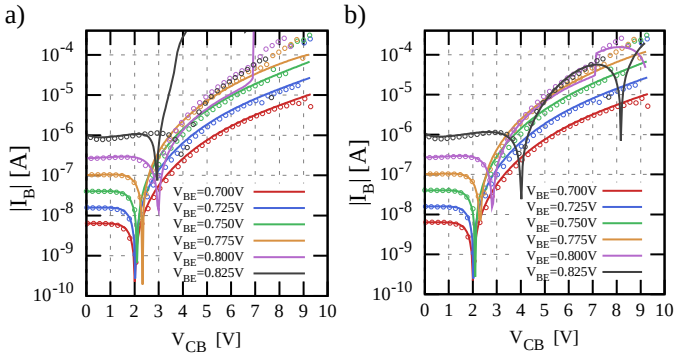

Fig. 5. Absolute value of the base current as a function of the collector-base voltage for different V_{BE} from 0.7V to 0.825V at T=25°C for a HV transistor comparing measurements (symbols) and simulations (lines) (a) with h_{AVL}=0 and d_{AVL}=0.23, (b) with h_{AVL}=0.36 and d_{AVL}=0.23.

is introduced in expressions (10) and (12) replacing the current expression of I_{LIM}. In (13), the parameters d_{AVL} is the factor for adapting I_{LIM} value for a spatially varying collector doping. h_{AVL} represents the current dependence of I_{LIM} in case of spatially varying collector doping. Note that I_{LIM} is obtained from extracting the model parameters describing the minority charge storage at high current densities.

4) Unified Model Expression

Equation (10) is valid for $I_T \leq I_{LIM_{eff}}$ and (12) for $I_T \geq I_{LIM_{eff}}$. At $I_T = I_{LIM_{eff}}$, the derivatives of equation (10) and (12) are not continuous. For the implementation in a compact model the discontinuity needs to be eliminated and the two asymptotic solutions need to be smoothly connected. These requirements are addressed by the formulation

$$f_{cor} = \sqrt{s_M \ln\left(\exp\left(\frac{c}{s_M}\right) - 2 + 2\cosh\left(\frac{1-\frac{I_T}{I_{LIM_{eff}}}}{s_M}\right)\right)} \qquad (14)$$

where s_M (equal to 0.1 as default value) is a smoothing factor for linking low and high collector current formulation. c is the ratio of the BC depletion capacitance C_{jCi} and its zero-bias value C_{jCi0}.

When $I_T = I_{LIM_{eff}}$, only the capacitance related exponential term in (14) remains. Hence, $\exp(C_{jCi}/C_{jCi0}/s_M)$ sets the minimum value of f_{cor}. Otherwise, when I_T differs sufficiently from $I_{LIM_{eff}}$, the exponential term can be neglected in comparison to the cosh term and the behavior approaches the one expected from (10) and (12).

Finally, the multiplication factor can be re-expressed as

$$M - 1 = \frac{f_{AVL}(V_{DCi} - V_{BC}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})f_{cor}}\right)}{1 - k_{AVL} f_{AVL}(V_{DCi} - V_{BC}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - V_{B'C'})f_{cor}}\right)} \qquad (15)$$

Fig. 4.a) shows the multiplication factor (15) as a function of I_C with different values of h_{AVL}. The value that yields the best agreement with TCAD data, is then used in Fig. 4.b), showing good agreement over a wide range of V_{CB} values.

III. Experimental Results and Validation

This section presents a comparison between measurements and the new avalanche model (15) implemented in HICUM. This comparison is shown on devices with two different doping profiles (HS, HV) [10] including a wide range of geometries and temperatures and for different current densities. We will focus on the investigation of the absolute value of the base current as a function of the base-collector voltage and compare the measurements with the new model.

As presented in (13), $I_{LIM_{eff}}$ depends on I_{LIM}. The corresponding current is given from the internal collector resistance at low electric field, R_{Ci0}, and the voltage separating the ohmic and the saturation velocity, V_{LIM} as

$$I_{LIM} = \frac{V_{LIM}}{R_{Ci0}} \qquad (16)$$

These two parameters are determined from the measured charge storage behavior at high current densities [13].

As the high injection avalanche mechanism interferes strongly with self-heating, the extraction of d_{AVL}, h_{AVL} and s_M requires very accurate values of model parameters concerning the weak avalanche region, the high injection region, as well as the temperature related parameters (f_{AVL}, q_{AVL}, k_{AVL}, R_{CI0}, V_{LIM}, R_{TH}). The parameters linked to the weak and strong avalanche can be extracted at low current density from the avalanche current at different V_{CB} [16]. The thermal resistance R_{TH} which defines the amount of self-heating can be extracted from the slope of $I_B(V_{CB})$ at constant V_{BE} and at relatively low V_{CB} [13].

Once these parameters have been obtained, d_{AVL} can be extracted (with s_M supposed to be constant) by setting h_{AVL} to 0 for $I_T < I_{LIM}$ by optimizing the $I_B(V_{CB})$ at medium current density. In a second step, h_{AVL} is optimized on the same characteristic at higher current density.

A. Doping profile variation

Fig. 6.a) and b) present the I_B (V_{CB}) measurement at 25°C for two different device types (HS, HV). The HS-devices have a SIC (selectively implanted collector) with quite high doping level whereas the HV-devices have no SIC. We can observe that in both cases the breakdown voltage is injection level dependent and the new model is able to describe this dependence accurately. We limited the V_{BE} range to 0.86V and 0.82V respectively. In fact at higher V_{BE}, self-heating starts to change

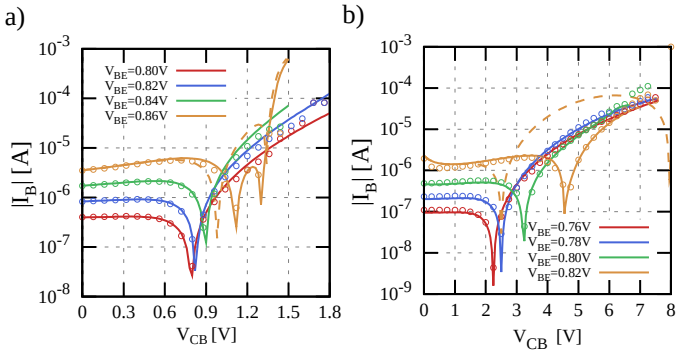

Fig. 6. Comparison of the base current measurement (symbols) with the extended avalanche model (lines) and without the current dependence (dashed lines) for two collector doping profiles at 25°C: (a) High doping (HS, W=100nm, L=4.42µm) with d_{AVL}=1, h_{AVL}=1, R_{Ci0}=17Ω, V_{LIM}=641mV, R_E=4.2Ω, f_{AVL}=19V^{-1}, q_{AVL}=12fC, k_{AVL}=0.22, R_{TH}=3360KW^{-1} and (b) low doping (HV, W=100nm, L=4.42µm) with d_{AVL}=0.23, h_{AVL}=0.36, R_{Ci0}=223Ω, V_{LIM}=842mV, R_E=3.12Ω, f_{AVL}=2.34 V^{-1}, q_{AVL}=4.2fC, k_{AVL}=0.3.

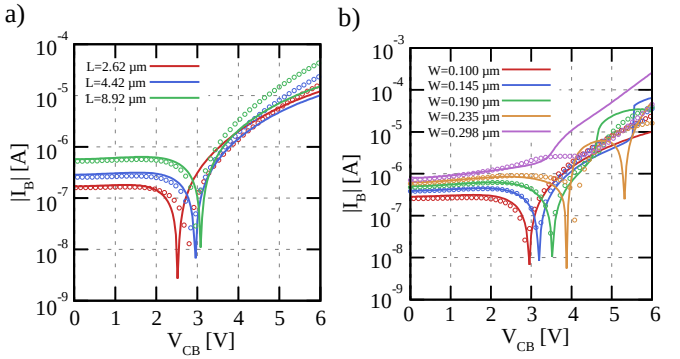

Fig. 7. Comparison of the base current measurement (symbols) at 25°C with the model (lines) at V_{BE}=0.8V for a HV transistor for different geometries: (a) For different emitter length values from 2.62 to 8.92µm with W = 0.1µm and (b) for different emitter width values from 0.1 to 0.298µm with L = 4.42µm. This plot is best viewed in the on-line color.

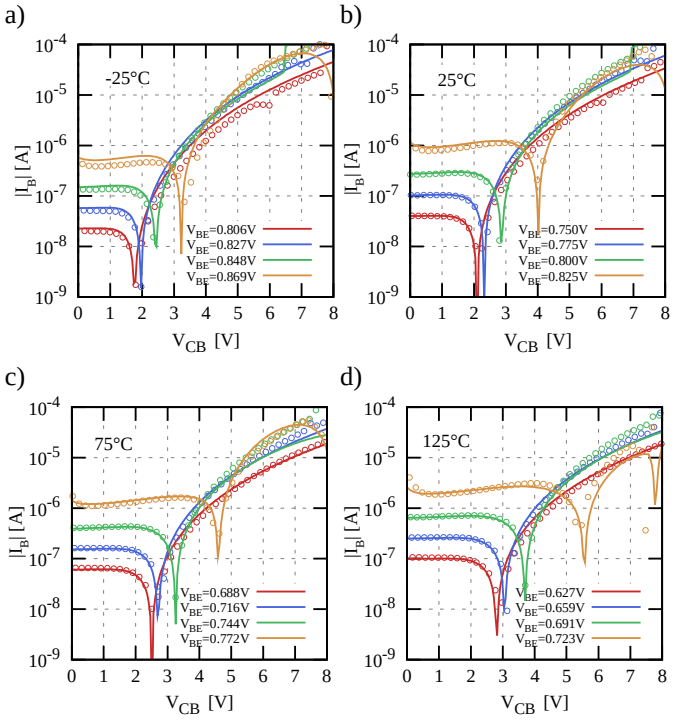

Fig. 8. Base current as a function of V_{CB} for different V_{BE} for a HV transistor (W=100nm, L=4.42µm) for different temperatures (a) -25°C, (b) 25°C, (c) 75°C, (d) 125°C: - comparison between the measurement (symbols) with the new model (lines). This plot is best viewed in the on-line color.

the electrical behavior and hides the avalanche effect for the two transistors.

B. Scaling

The STMicroelectronics model library for the BiCMOS055 process already contains HICUM model parameter sets that are scalable with respect to emitter width and length. Therefore, as R_{Ci0} is already scalable in ST's model library, no new scalable equations are needed for (13).

Fig. 7 compares $I_B(V_{CB})$ measurements for different emitter lengths (Fig. 7.a) and widths (Fig. 7.b) with the new model (15). Good agreement with the measurements, especially for different widths is obtained (Fig. 7.b). The agreement for different emitter lengths (Fig. 7.a) is less accurate and requires further investigation. In particular, the base current reversal does not change sufficiently for smaller lengths.

C. Temperature variation

The temperature dependent parameters relevant to the new formulation are discussed next. The extraction of the parameters specifically related to the avalanche effect was already presented in [16]. The main model parameters for the new I_{LIM} equation are R_{Ci0} and V_{LIM} and read [13]

$$R_{Ci0}(T) = R_{Ci0}(T_{nom})\left(\frac{T}{T_{nom}}\right)^{\zeta_{Ci}} \tag{17}$$

and

$$V_{LIM}(T) = V_{LIM}(T_{nom}).\left(\frac{T}{T_{nom}}\right)^{\zeta_{Ci}-A_{LVS}\,T_{nom}} \tag{18}$$

with the thermal coefficients $ZETA_{Ci}$ and AL_{VS}, T_{nom} as the nominal temperature. The extraction of both parameters follow the similar procedure described in [16] for the avalanche. Therefore, the temperature dependence of I_{LIM} is described by eq. (17) and (18) and the parameters d_{AVL} and h_{AVL} do not require additional temperature parameter.

Fig. 8 presents the base current as a function of V_{CB} for different temperatures ranging from 0°C to 125°C. V_{BE}-values were chosen where high-current effects are relevant. Excellent agreement with the new model and the measurements is observed for all temperatures. This figure also shows a limitation of the model for very high V_{CB}-values and the highest V_{BE}-value. In fact, as presented in Fig. 1.a) for these bias points, self-heating dominates compared to other physical effects. In particular, base pinch-in may occur that cannot be modelled by a lumped model but requires a distributed model.

IV. Conclusion

An improved avalanche model for low and high injection in SiGe HBTs has been proposed in this paper. This new formulation accounts for the electric field profile (apart from the punch-through case) and associated impact ionization dependence as a function of the injection level. A unified expression has been derived and implemented in HICUM/L2. It has been shown by comparison to measurements that this new avalanche model significantly improves the simulation

accuracy of the base current close to and beyond BV_{CEO}. The new model formulation has been compared to different types of SiGe HBTs with different epi-layer doping profiles, different geometries, and over a wide range of temperatures. It can be concluded that the accuracy of HICUM/L2 is enhanced for operation of the transistor close to the SOA edge. Furthermore, no convergence issues have been observed during simulation and the simulation time does not increased significantly (by < 4%).

V. Appendix

A. f_{corL} explanation

The integration of (8) leads to

$$\int_0^{w_{BC}} E(x)\,dx = \frac{qN_{epi}}{2\,\varepsilon_{Si}}\left(1-\frac{I_T}{I_{LIM}}\right)w_{BC}^2 + E_{jC}w_{BC} \tag{19}$$

It also equals the internal voltage drop across the SCR:

$$-\int_0^{w_{BC}} E(x)\,dx = V_{B'C'} - V_{DCi} \tag{20}$$

where V_{DCi} represents the built-in potential. Inserting from (8)

$$E_{jC} = \frac{qN_{epi}}{\varepsilon_{Si}}\left(1-\frac{I_T}{I_{LIM}}\right)w_{BC} \tag{21}$$

yields the current dependent BC SCR width

$$w_{BC} = \sqrt{\frac{V_{DCi}-V_{B'C'}}{\frac{q\,N_{epi}}{2\,\varepsilon_{Si}}\left(1-\frac{I_T}{I_{LIM}}\right)}} \tag{22}$$

Note that this equation does not account for the punch-through case mainly for two reasons: (i) A graded collector doping profile leads to unclear punch-through onset conditions; (ii) the analytical formulation even for a constant profile case is more complicated, leading to significant additional computational effort. However, the results shown here demonstrate that (15) is sufficiently accurate for modeling the collector current dependence of the avalanche effect. Finally, the equations of w_{BC} and E_{jC} are reformulated according to their expression developed previously in [16] for low current densities ($w_{BC_{low}}$ and $E_{jC_{low}}$) respectively:

$$w_{BC} = w_{BC_{low}}\sqrt{1-\frac{I_T}{I_{LIM}}}^{-1} \quad with\ w_{BC_{low}} = \frac{\varepsilon_{Si}\,A_E}{C_{jCi}} \tag{23}$$

$$E_{jC} = E_{jC_{low}}\sqrt{1-\frac{I_T}{I_{LIM}}}\ with\ E_{jC_{low}} = -\frac{2(V_{DCi}-V_{B'C'})C_{jCi}}{\varepsilon_{Si}\,A_E} \tag{24}$$

Replacing the low-current variables $w_{BC_{low}}$ and $E_{jC_{low}}$ in the corresponding multiplication factor formulation and using (10) leads to (9).

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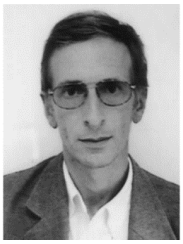

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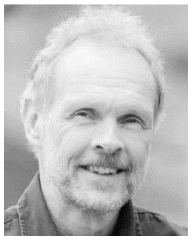

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