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12 mW 97 GHz Low-Power Down-Conversion Mixer with 0.7 V Supply Voltage

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***Abstract*—This letter presents a 97 GHz down-conversion mixer in a 130 nm SiGe HBT technology. For achieving the demonstrated ultra low DC power consumption, the mixer was designed with transistors operating in saturation using an accurate compact model. With 0.7 V supply voltage and -5 dBm local oscillator (LO) pumping power, this mixer achieves a double-sideband (DSB) conversion gain (CG) of 6.6 dB ± 3 dB over the RF frequency range from 91 GHz to 100 GHz, consuming 12 mW static DC power. With the supply voltage further reduced to 0.5 V, this mixer still works with a maximum upper-sideband (USB) CG of 5.2 dB from 94 GHz to 100 GHz, with only 8 mW static power consumption.**

***Index Terms*—Down-conversion mixer, SiGe HBT, HICUM model, low-power, W-band**

I. Introduction

SIGE HBTs and the corresponding BiCMOS technology have become very attractive for addressing mm-wave circuits and systems-on-chip with recent advancements and expected future performance [1]. One of the key demands for future wireless systems will be low power dissipation, which requires among others, a reduction in supply voltage. Since advanced SiGe HBTs offer still several hundreds of GHz cut-off frequencies even with forward biased BC junction V_{BC}, the investigation of mm-wave circuits with HBTs operating in saturation appears intriguing and was pursued in this work.

Low-power mm-wave SiGe HBT based circuit design work has been reported on before. In [2], a W-band frequency tripler together with a buffer amplifier was realised with a forward biased base-collector junction. A 200 GHz low-power mixer was reported in [3], but still biased at a negative V_{BC}. To the best of the authors' knowledge, mixers with forward-biased V_{BC} operating above 90 GHz have not yet been reported.

This letter demonstrates a 97 GHz low-power down-conversion mixer with 0.7 V supply voltage (V_{supply}), achieving a maximum upper-sideband (USB) conversion gain (CG) of 9.6 dB with 12 mW DC power from 91 GHz to 100 GHz.

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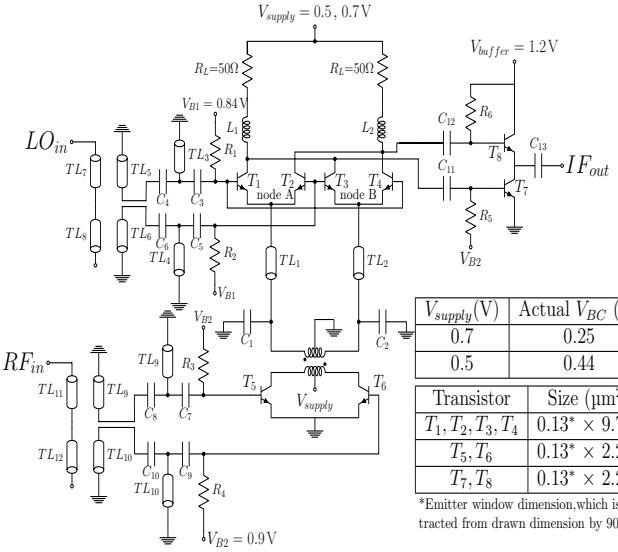


V_{supply}(V)	Actual V_{BC} (V)
0.7	0.25
0.5	0.44

Transistor	Size (μm²)
T_1, T_2, T_3, T_4	0.13* × 9.71*
T_5, T_6	0.13* × 2.21*
T_7, T_8	0.13* × 2.21*

*Emitter window dimension,which is subtracted from drawn dimension by 90 nm

Fig. 1. Schematic diagram of the designed low-power down-conversion mixer.

With an even lower bias voltage of V_{supply} = 0.5 V, this mixer still works with 5.2 dB USB CG, consuming only 8 mW DC power. The first-pass success design was enabled based on the compact model HICUM/L2 [4], which provides an accurate description of the DC and especially the dynamic HBT behaviour also in saturation.

II. Mixer Design and Circuit Implementation

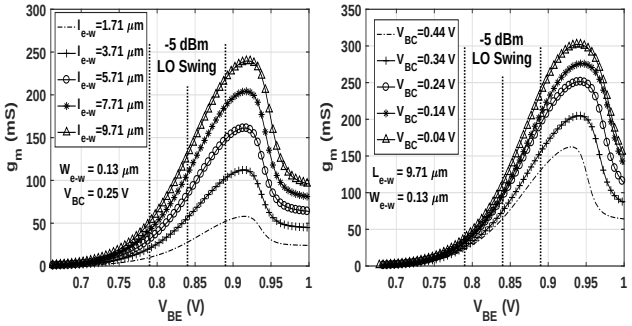
A. Mixer Topology

The schematic of this low-power mixer is presented in Fig. 1. Compared with a conventional Gilbert-cell based mixer, an on-chip transformer is used to not only couple the switching quad (T1-T4) with the transconductance stage (T5, T6), but also to reduce V_{supply} and to bias the two blocks separately in order to decrease DC power dissipation. Two broadband low-loss spiral baluns are implemented for single to differential conversion and mixer performance enhancement. Besides, an output differential buffer amplifier is designed to directly transfer the differential IF signal back to a single-ended signal with some amplification, obviating the need for an extra IF balun.

B. Low-Power Mixer Analysis

The power CG of a 1_{st} harmonic transconductance based mixer can be expressed as [5]

$$CG \cong [\frac{g_{max} - g_{min}}{\pi \omega_{RF}}]^2 R_L. \quad (1)$$



(a) (b)

Fig. 2. Simulated g_m versus V_{BE} of transistors (a) at actual V_{BC} of 0.25 V with different emitter window lengths L_{e-w}, and (b) with fixed L_{e-w} of 9.71 μm and different actual V_{BC}. The emitter window width W_{e-w} is 0.13 μm.

Here, R_L is the load resistance shown in Fig. 1, ω_{RF} is the angular RF frequency, g_{max} and g_{min} are the maximum and minimum value of the transconductance g_m during the large LO signal swing at the base of T1-T4. Generally, the center of the relevant g_m region can be selected by biased V_{BE}, while the size of such region is determined by the LO pumping power level.

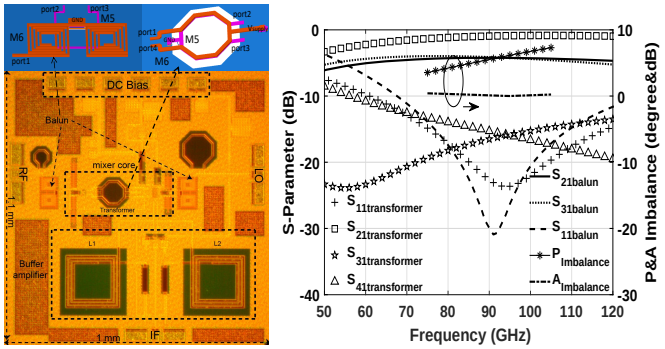
For the standard mixer design, CG can be boosted by using large values for R_L and the range $(g_{max} - g_{min})$ along with high V_{supply} and large LO power, if DC power dissipation is not a priority. However, when designing a low-power mixer with fixed LO power and low V_{supply}, it is challenging to enhance $(g_{max} - g_{min})$, and the use of large RL is prohibited.

Fig. 2(a) shows the simulated g_m versus V_{BE} of transistors with different emitter lengths, operating all at V_{BC} = 0.25 V. Also, the g_m range for a V_{BE} swing of approximately 0.05 V (corresponding to -5 dBm LO power) has been inserted. Since the absolute value of g_m and thus its absolute range increases with emitter area, a large but not reach the upper limit value of emitter window length l_{e-w} of 9.71 μm (emitter drawn length of 9.8 μm) has been selected in switching quad, which comes at the expense of an additional total DC power consumption of about 3 mW for the switching quad. R_L generally increases the actual V_{BC} and needs to be minimized to keep g_m as high as possible (cf. Fig. 2(b)). As a result, R_L = 50 Ω was selected as a compromise. This discussion shows the necessity of an optimisation for achieving a careful trade-off between CG and power consumption, which is impossible without accurate and geometry scalable compact models.

C. Circuit implementation

This mixer was fabricated in 130 nm SiGe BiCMOS technology from Infineon Technologies AG, which features high-speed npn-HBTs with peak f_T of 250 GHz and f_{MAX} of 370 GHz at V_{BC} = -0.5 V. As discussed, transistors of the switching quad are designed with an emitter window area A_{e-w} = 0.13 $\times$ 9.71 μm^2. For the other transistors (T5-T8) in transconductance stage and buffer amplifier, however, A_{e-w} = 0.13 $\times$ 2.21 μm^2 was selected in order to minimize the DC current while limiting the impact on the mixer performance.

Fig. 3(a) displays the micrograph of the fabricated chip, together with 3D views of the designed balun and transformer. In order to obtain the desired broadband and low-loss properties, the balun is implemented by two pairs of



(a) (b)

Fig. 3. (a) Chip micrograph and 3D views of balun and transformer; the total chip area is 1 mm $\times$ 1.1 mm. (b) Simulated S-parameters of balun and transformer as well as phase and amplitude imbalance of the balun.

λ/4 transmission lines (TL5-TL8 and TL9-TL12), which are located at the topmost metal layer M6 and are interleaved in a two-turn spiral configuration. EM simulation results of balun, as demonstrated in Fig. 3(b), predicts an insertion loss (IL) of 4.1 dB, with around 0.15 dB and 5° amplitude and phase imbalance from 75 GHz to 105 GHz, respectively. The single-turn on-chip transformer is designed in a completely overlapped broadside coupling configuration. Due to the symmetry of the transformer, EM simulation results of Port 1 are presented in Fig. 3(b) only, which indicate a 0.9 dB IL and around 15 dB isolation in W-band. Four T-type inter-matching networks, each consisting of a shunt short-stub together with two series MIM capacitors, are used between the mixer core and balun. The total size of the chip is 1 mm $\times$ 1.1 mm, including the DC and RF pad structures.

III. Results and Discussion

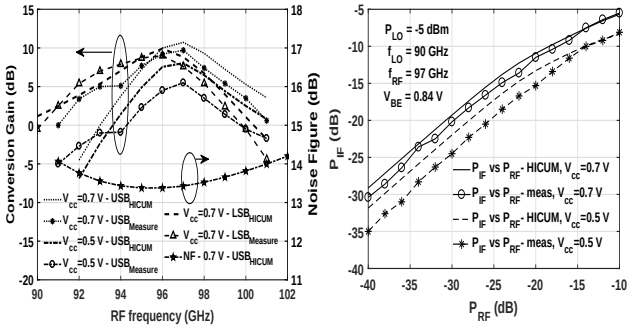
This mixer is measured on Wafer. The LO chain consists of a Tactron Elektronik 6 multiplier, the power of which is calibrated by a VDI Erickson PM5 power meter. The RF signal is automatically controlled by a VNA (Keysight PNA E8361C) with a W-band waveguide T/R module, which is also used in S-parameter measurements of the mixer. Probe loss from the LO and RF ports were subtracted to calculate the accurate on-chip power level. Finally, a spectrum analyser (Keysight PSA E4440A) was used to monitor the IF signal power.

Fig. 4(a) demonstrates the measured and simulated USB and lower-sideband (LSB) CG of this mixer, together with simulated USB Noise Figure (NF), with a fixed -5 dBm LO signal at 90 GHz (USB) and 103 GHz (LSB), respectively. With a 0.7 V V_{supply}, the mixer's double-sideband (DSB) CG was measured to be 6.6 dB $\pm$ 3 dB from 91 GHz to 100 GHz, with an overall maximum USB CG of 9.6 dB at 97 GHz and LSB CG of 8.8 dB at 96 GHz. The minimum USB NF is simulated to be 13.6 dB at 96 GHz. The entire static power dissipation was measured to be 12 mW, composed of 9.5 mW from the mixer core and 2.5 mW from the IF buffer amplifier. Furthermore, reducing V_{supply} to 0.5 V yields a measured maximum CG of 5.2 dB over the frequency range of 94 GHz to 99 GHz, consuming just 8 mW DC power in total.

Fig. 4(b) displays the simulated and measured results of the IF output power P_{IF} versus RF input power P_{RF} in USB case. The input 1 dB compression point P_{1dBin} is measured to be -20 dBm with 0.7 V bias and -16 dBm with 0.5 V bias.

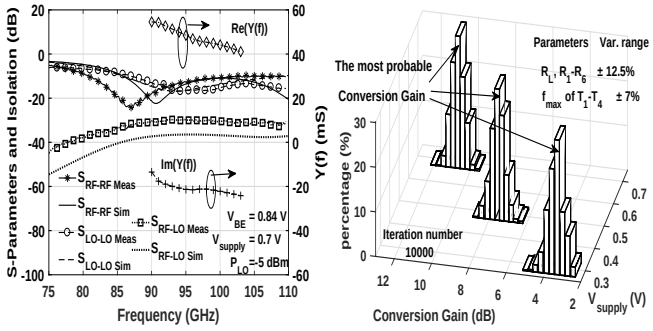
TABLE I
COMPARISON OF SiGe HBT BASED LOW-POWER MIXERS

Reference	f_{max} (GHz)	Topology	f_{RF} (GHz)	CG (dB)	P_{LO} (dBm)		DC supply (V)	P_{DC} (mW)		
					Mixer	On chip		Mixer	Buff.	Total
[3]	450	Gilbert cell+IF&LO buff.	200	5	-5	-20	3.3	17.4	22.5	39.9
[7]	370	Gilbert cell+IF&LO buff.	122	19.5	-5		3.3	50		
[8]	190	G_m-boosted	135	11.5	10		3	3.9		
This paper	**370**	**Gilbert cell+IF buff.**	**97**	**5/9.6**	**-5**		**0.5/0.7**	**6/9.5**	**2/2.5**	**8/12**



(a) (b)

Fig. 4. (a) Simulated and measured USB and LSB CG as well as the simulated USB NF of this mixer. (b) Simulated and measured results of P_{IF} versus P_{RF}, with 0.7 V_{supply} and -5 dBm LO signal at 90 GHz (USB).



(a) (b)

Fig. 5. (a) Simulated and measured reflection coefficients S_{RF-RF} at RF port, S_{LO-LO} at LO port and LO-to-RF isolation S_{RF-LO}, with P_{LO} = -5 dBm, and the simulated real & imaginary part of node admittance *Y(f)* at node A of Fig. 1. (b) Simulated statistical analysis of the USB CG with V_{supply}/V = (0.3, 0.5, 0.7).

The simulated and measured reflection coefficients and the isolation of the LO and RF port with P_{LO} = -5 dBm are shown in Fig. 5(a). More than -12 dB return loss from 80 GHz to 110 GHz have been observed, which indicates the good power injection at these two ports. Besides, around 30 dB LO-to-RF isolation is measured. Large signal stability of this mixer is analysed base on the mathod in [6]. By introducing a small independent auxiliary signal at node A (shown in Fig. 1), the node admittance *Y(f)* can be calculated in harmonic balance simulator with the -5 dBm LO power, the result of which is presented in Fig. 5(a). The positive value of the real part of *Y(f)* predicts the in-band stabilisation of this mixer.

A statistical analysis was performed for this mixer, considering mismatch and process tolerances of the most relevant transistor parameters (causing a $\pm$ 7 % change in f_{MAX} of T1-T4) and of most sensitive passive components such as RL and R1-R6 ($\pm$ 12.5 %). Since the varied parameters are linearly independent, the Monte Carlo method offered in the simulator was applicable. As shown in Fig. 5(b), simulation predicts a probability of $>$ 65 % for achieving a $\pm$ 1 dB variation for V_{supply} = 0.7 V, 0.5 V and even 0.3 V.

The performance of this low-power mixer is summarised in Table I, together with recently reported SiGe HBT based low-power mixers. The transistors in all these reported mixers are still operated in forward-active mode, which results in a higher DC power dissipation of the Gilbert based mixers, as shown in [3] and [7]. Mixers in [8], which was designed by G_m-boosted topology, exhibited a lower DC power consumption, but at the expense of requiring an about 30 times larger LO signal power (+ 10 dBm). Finally, compared with the W-band state-of-art low-power CMOS mixer in [9], the results reported in this paper demonstrate that SiGe HBTs with relaxed lithography (130 nm) can compete with significantly more advanced and costly CMOS technology in terms of power consumption and W-band circuit performance.

IV. CONCLUSION

A W-band low-power down-conversion mixer was implemented in 130 nm SiGe BiCMOS technology. Competitive performance in terms of conversion gain and required LO power along with signal injection has been achieved simultaneously with very low power dissipation. The letter has been enabled by a drastic reduction of the supply voltage, forcing all transistors to operate in saturation. The excellent agreement between simulation and measurement allowed a detailed analysis of the circuit performance.

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