Post-doc and Research Engineer positions in TIMA Laboratory SLS Team

October 13, 2023

Introduction

The TIMA Laboratory (website) is an academic research entity situated in Grenoble city, in France. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end.

The SLS team (System Level Synthesis - website) focuses on highly efficient architectures for general purpose computing or AI-dedicated algorithms, and system-level modeling and design methodology : specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware.

This document presents Post-doc and/or Research Engineer positions that are available in the SLS team, linked to acceleration of AI (Artificial Intelligence) on FPGA and to more generic hardware acceleration on FPGA through PCI-Express.

About TIMA: TIMA is located within historical building of the Grenoble Polytechnic Institute, just near the city train station. It is fully accessible for people with disabilities.

TIMA is a multinational team, with members and interns from all over the world. The Laboratory and its parent institutions ensure that everyone is treated equally, respectfully, regardless of gender, religion, disabilities, etc.

Requirements: New applicants should send a CV and an overview of their work experience and full course-work and grades, by email and preferably in PDF format, to the contacts below. Please present clear, exhaustive and verifiable curriculum, as there is a standard inquiry before taking position (especially for non-European applicants).

Contacts:

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2 Positions : High-performance communication interface for FPGA boards

2.1 Maturation and extension of RIFFA PCI-Express framework

Context: The RIFFA framework eases development of PCI-Express hardware accelerators on FPGA. It provides a convenient wrapper around the vendor-specific PCIe IPs, associated to software-side driver and library for user applications. This framework has been used, and is still used as main communication interface in the context of demonstration of various FPGA hardware accelerator projects.

But the RIFFA project has been inactive for several years and this limits what can be done with it. Notably, support for newer-generation PCIe generations and FPGA boards would enable more powerful accelerators. Flexibility of software API could also be improved. The action items of interest are listed below.

A workshop with other developers and users of RIFFA framework will be organized in the context of an international conference. The candidate will participate and help with organization of the workshop.

Duration : 18 to 24 months

Objectives, hardware side:

- support of other boards : past, current and future boards, with a procedure to build and test,
- support AXI as an alternative interface for user channels, to enable better usage of AXI IPs,
- reduce resource usage in specific cases (such as unique user channel, same clock domain, no offset/address, ...),
- better modularity regarding multi-channel implementation, to enable experiments with alternative time-multiplexing algorithms, priorities, etc,
- other items to be discussed.

Objectives, Linux driver side:

- better multi-user support (associate devices/channels to user that open it),
- create per-channel device driver files,
- enable to reset channel semaphores (revisit the current memory barrier implementation),
- improve the hardcoded limit to the number of PCIe devices in architecture of the driver,
- consider access to host PC memory from hardware accelerators,
- reconfiguration capability,
- other items to be discussed.

Objectives, user library side:

- integration with standard pkg-config,
- enable per-channel reset,
- other items to be discussed.

Requirements:

- Excellent programming skills (C, C++)
- Good knowledge of usual HDL lanquages (Verilog or VHDL)
- Good knowledge of usual toolchains and design flows for FPGA
- Good knowledge of git
- Experience with Xilinx Vivado/Vitis tools would be a plus
- Experience with linux drivers would be a plus
- Experience with PCI-Express communication would be a plus
- Interest in FPGA technologies and hardware acceleration

References:

- RIFFA project : https://github.com/KastnerRG/riffa