PhD positions in TIMA Laboratory - SLS Team

October 13, 2023

Introduction

The TIMA Laboratory (website) is an academic research entity situated in Grenoble city, in France. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end.

The SLS team (System Level Synthesis - website) focuses on highly efficient architectures for general purpose computing or AI-dedicated algorithms, and system-level modeling and design methodology : specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware.

This document presents several PhD positions that are available in the SLS team, linked to AI (Artificial Intelligence), in particular acceleration of AI and usage of AI for EDA (Electronic Design Automation).

About TIMA: TIMA is located within historical building of the Grenoble Polytechnic Institute, just near the city train station. It is fully accessible for people with disabilities.

TIMA is a multinational team, with members and interns from all over the world. The Laboratory and its parent institutions ensure that everyone is treated equally, respectfully, regardless of gender, religion, disabilities, etc.

Requirements: New applicants should send a CV and an overview of their work experience and full coursework and grades, by email and preferably in PDF format, to the contacts below. For students, Masters degree or engineer diploma or other degree with formal equivalence is mandatory. Please present clear, exhaustive and verifiable curriculum, as there is a standard inquiry before taking position (especially for non-European applicants).

Contacts:

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2 PhD positions : Usage of IA for EDA

2.1 AI-assisted design of compressor circuits for FPGA technologies

Context: FPGA targets are of high interest for acceleration of tasks where processed data is composed of numbers with reduced quantification or with custom representation (such as highly-parallel and quantized AI tasks, approximate computing, etc). This opens new opportunity to re-think how adder trees can be efficiently synthesized for FPGA technologies, in particular how base compressor blocks (also known as bitheaps) can be designed, scaled and adapted to different FPGA technologies.

The challenge consists in the design of base compressor blocks that can be assembled in a scalable way to compose large multi-input adders. Dedicated works involving a lot of human time and brain have been done, targeting specific FPGA technologies of interest at that time. However, these efforts can only cover a limited part of the combinations of current and future applications and of target FPGA technologies. Additionally, specific human design brings no guarantee that interesting solutions have been explored for a single technology.

The general trend in raising the level of abstraction of design languages for digital circuits and FPGA hardware acceleration (from VHDL and Verilog to C, C++, OpenMP, etc) also mandates that synthesis tools are expected to produce optimized implementations (if not optimal) for the targeted FPGA technology.

Objectives: The subject consists in exploring how AI technologies can help exploring and discovering pertinent implementation solutions of compressor blocks for various FPGA technologies, taking into account the architectural specificities and constraints of these technologies (size of LUTs, placement of carry chains, number of inputs/outputs per logic slice, routability, etc), and considering variants to signed inputs and more specific representations such as ternary number system.

A more specific interest exists for base compressor blocks with regular distribution of inputs, because such blocks enable to easily and quickly instantiate reasonably-optimized adder trees with usual HDL languages, instead of involving complex ILP solvers and HDL generators for each adder tree instance in a design.

Requirements:

- Experience with AI, machine learning and tools
- Good programming skills
- Knowledge of usual HDL lanquages
- Knowledge of usual toolchains and design flows for FPGA
- Interest in FPGA technologies
- Interest in problem solving

Previous works on compressor trees:

- Efficient High Speed Compression Trees on Xilinx FPGAs (2014)
  http://martin-kumm.de/preprints/2014_MBMV_Kumm.pdf
- Pipelined Compressor Tree Optimization using Integer Linear Programming (2014)
  http://martin-kumm.de/slides/2014_09_03_FPL.pdf
- Area optimized synthesis of compressor trees on xilinx fpgas using generalized parallel counters (2019)
  https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=8843959