Techniques de L'Informatique et de la Microélectronique pour L'Architecture des systèmes intégrés



Techniques of Informatics and Microelectronics for integrated systems Architecture

Opening for PhD thesis Robust and Secure RISC-V Architecture

Context

Modern microprocessors aim at providing the best possible performance (at a reasonable cost). For this reason, several architectural optimizations are often designed, engineered, and implemented, but such complexity is usually transparent to users and developers, who cannot see the hidden elements. Indeed, microarchitecture designers have progressively added many complex hardware blocks (for example, pipeline, cache memory, branch prediction, speculative execution, specialized blocks) in order to optimize program executions.

The increasing complexity of the microprocessor architectures and the applications they run, however, means that foreseeing the behavior of the system under nonnominal conditions is a hard and critical challenge. The behavior of the CPU (and of the full system) when external interferences affect the system may be largely affected by these hidden elements. Thus, it is highly important that the design flow should take into consideration from the very beginning the possibility of perturbations on the external clock, the power supply, or the electromagnetic surrounding that might alter the safe and secure execution of code.

Objectives

The candidate is expected to develop a RISC-V architecture intrinsically robust and secure against perturbation, error occurrences, and fault injections. A first step will focus on modeling the effects of complex fault occurrences and perturbations on the micro-architecture. The objective is to have a thorough understanding of the error mechanisms occurring within the RISC-V architecture, at different levels. Subsequently, the candidate will propose and evaluate architectural solutions in order to mitigate the identified vulnerabilities.

Profile

The candidate should be in possession of a BAC+5 degree in Electrical or Computer Engineering, with knowledge of CPU architecture and design. Knowledge of hardware security and physical attacks is a plus, but not strictly required.

Speaking French is not mandatory to apply, but a good level of English is necessary

The PhD will be based at TIMA Laboratory, Grenoble, France, and will begin approximately on October 2022 and last 3 years. Gross salary will be about 25600€/year.

Diversity statement

Our team welcomes applicants with diverse backgrounds and experiences. We regard gender equality and diversity as a strength and an asset.







Laboratoire TIMA 46 avenue Félix Viallet - 38031 GRENOBLE – FRANCE Tél : 04 76 57 50 79 E-mail : tima-direction@univ-grenoble-alpes.fr Web : http://tima.univ-grenoble-alpes.fr **TIMA Laboratory** 46 avenue Félix Viallet - 38031 GRENOBLE – FRANCE Tel: (+33) (0) 476 57 50 79 E-mail: tima-direction@univ-grenoble-alpes.fr Website: http://tima.univ-grenoble-alpes.fr Techniques de L'Informatique et de la Microélectronique pour L'Architecture des systèmes intégrés



Techniques of Informatics and Microelectronics for integrated systems Architecture

Contacts

The potential candidates should send their CV, motivation, and recommendation letters to:

Paolo MAISTRI, TIMA Laboratory, Grenoble (paolo.maistri@univ-grenoble-alpes.fr) Giorgio DI NATALE, TIMA Laboratory, Grenoble (giorgio.di-natale@univ-grenoble-alpes.fr)







Laboratoire TIMA 46 avenue Félix Viallet - 38031 GRENOBLE – FRANCE Tél : 04 76 57 50 79 E-mail : tima-direction@univ-grenoble-alpes.fr Web : http://tima.univ-grenoble-alpes.fr **TIMA Laboratory**

46 avenue Félix Viallet - 38031 GRENOBLE – FRANCE Tel: (+33) (0) 476 57 50 79 E-mail: tima-direction@univ-grenoble-alpes.fr Website: http://tima.univ-grenoble-alpes.fr