



## 2025-2026 Low-cost embedded solutions for detecting physical attacks on FPGAs

### **Abstract:**

Physical attacks have seen significant growth in recent years. These attacks target the hardware of electronic chips, which has traditionally been considered secure. Physical attacks include laser injections, X-ray radiation, electromagnetic disturbances, and temperature elevation. Such attacks can compromise or access protected data, or bias the responses of cryptography-oriented circuits, such as physically unclonable functions (PUFs). This highlights the need to design robust and low-cost methods capable of detecting these attacks.

### **Project description:**

This internship focuses on studying and understanding the effects of physical attacks on ring oscillators, which form the basis of many electronic circuits, including Ring Oscillator PUFs. The goal is to detect any abnormal frequency variations resulting from malicious manipulations, such as thermal, electromagnetic, or optical attacks. The intern will be responsible for designing, implementing, and testing real-time detection circuits capable of identifying any attempt to alter the behavior of ring oscillators, while minimizing FPGA resource usage. Subsequently, the intern will implement a RO-PUF on an FPGA, perform controlled physical attacks, and evaluate the effectiveness and robustness of the proposed detection technique.

### **Tasks of the internship:**

- Study and become familiar with the state-of-the-art on physical attacks and associated detection techniques.
- Design and implement an efficient, low-cost detection solution.
- Conduct experimental tests on real targets (FPGA).
- Implement a RO-PUF along with detection circuits, and monitor and analyze the PUF's behavior under normal conditions and under attack.

### **Scientific environment:**

The candidate will work within the TIMA Laboratory (<https://tima.univ-grenoble-alpes.fr/>) in collaboration with the AMfoRS (Architectures and Methods for Resilient Systems) research group.

### **Profile & requested skills:**

We are seeking a highly motivated student from an Engineering School or a Master's program (M2). Applicants should hold a Master 1 degree (or an equivalent qualification) obtained within the last three years at the time of application, in a relevant field such as microelectronics, digital electronics, or related disciplines. A strong foundation in HDL languages (Verilog/VHDL) and data processing tools such as Python is required. Candidates with a genuine interest in hardware security and experimental FPGA-based projects will be particularly encouraged to apply.

**Allowance:** Internship allowance will be provided.

### **Application instructions:**

If you are interested in the topic, please send your complete application to:  
[Aghiles.Douadi@univ-grenoble-alpes.fr](mailto:Aghiles.Douadi@univ-grenoble-alpes.fr)

---

**A complete application consists of:**

**Cover letter:** A brief motivation statement by the applicant, explaining their connection to the position, how the position aligns with their background, and how it supports their future career goals (maximum 1 page).

**CV:** Academic and professional background, detailing relevant experience, particularly research.

**Relevance for Application:** The applicant should include a clear description of how his or her scholarly background and expertise apply to the project outlined above and how they might add value to it.

Our laboratory welcomes applicants with diverse backgrounds and experiences. We regard gender equality and diversity as a strength and an asset.

**Contacts:**

Aghiles, Douadi  
Postdoctoral Researcher at TIMA Laboratory  
Université Grenoble Alpes  
Grenoble, France  
Email: [Aghiles.Douadi@univ-grenoble-alpes.fr](mailto:Aghiles.Douadi@univ-grenoble-alpes.fr)