Internship : Electrical modeling of TID effects on digital circuits

Keywords

Compact modeling, Cadence, Simulation

Context

TID (**T**otal **I**onizing **D**ose) effects on semiconductors is a wide topic and has been extensively studied for space applications in the past years. Several simulation models have been developed in order to better understand the effects of such radiations and to develop countermeasures. TID modeling techniques in the state-of-art can be classified into two categories : Modeling using a **pure physics/numerical** approach where experimental data are used to estimate variables of a physical equation [1]. Or modeling the **Electrical/analog** behaviour of the circuit under test, by fitting the parameters of the **compact model** of it's elementary components (transistors) with experimental data or data generated from numerical simulations [2]. Pure physics based models are mostly used in the case of need for a finite element method simulation using CAD methods [3]. Such simulations take a long time and describe the movement of particles inside a well-defined structure and as a result it provides all the computations defined by the model and more importantly, it provides visual representation of the spatial distribution of the particles. Compact modeling is used to perform SPICE oriented simulations of complex large circuits. These models usually use parameters defined in MOSFET models for SPICE simulation such as BSIM3v3, BSIM4 or custom defined models written in C language or Verilog-A. These parameters are then calibrated and extracted from experimental data using regression methods. Figure 1 describes the modeling approaches of device simulation by abstraction level and the trade-off in terms of accuracy and speed of simulation.

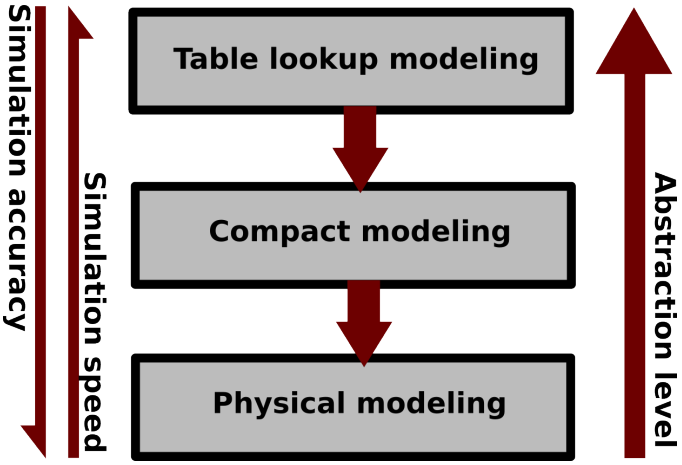

Figure 1: Description of different modeling approaches by abstraction level

Description of the internship

The goal of this internship is to develop a parameter extraction flow from the compact model BSIM4 in order to simulate the effects of TID radiations. The student is expected to develop a generic flow that will be applied on the target technology ST65nm and if the flow is generic enough, the parameters of a BSIM3V3 model will be extracted for the AMS350nm target. The experimental data for the parameter extraction will be generated using simulation and theoretical approximations from the literature. Finally, the student will perform simulations with the extracted parameters in order to model TID effects.

Tasks of the internship

1. Bibliography study on the state-of-the-art TID modeling and BSIM parameter extraction methods.
2. ASIC synthesis of a simple digital circuit.
3. Generation of the simulated experimental data and the development of the parameter extraction flow.
4. Simulation of the circuit under TID radiation with the extracted parameters.
5. Creation of a cross-layer fault model library

Profile

- Microelectronics background (Digital and analog).
- Cadence Virtuoso

Profil : 2A internship
Duration : 2 to 3 months (Starting May 2023)
Remuneration : about 600€/month

To apply, please send your CV and latest transcript to :

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Our team welcomes applicants with diverse backgrounds and experiences. We regard gender equality and diversity as strength and an asset.

References

[1] Gennady I. Zebrev, Vasily V. Orlov, Maxim S. Gorbunov, and Maxim G. Drosdetsky. Physics-based modeling of tid induced global static leakage in different cmos circuits. *Microelectronics Reliability*, 84:181–186, 2018.

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