Design and Evaluation of Content Addressable Memory (CAM)

Position: Internship

Duration of the project: 6 months

Context of the research work

Content-addressable memory (CAM) is a computer memory type built for extremely fast but very specific type of memory lookups. Content-addressable memory (CAM) is also known as associative memory, associative storage, or associative array. It compares input search data against the stored data, and returns the address of matching data. It is capable of searching its whole contents in a single clock cycle. The CAM a performance advantage over other memory search algorithms, such as binary or tree-based searches or look-aside tag buffers, by comparing the desired information against the entire list of pre-stored entries simultaneously, often resulting in an order-of-magnitude reduction in the search time.

The central building blocks of these memories are the core cells and many variations exist, each with its benefits and shortcomings in terms of area on silicone, speed of search, power consumption, reliability of data. The main objective of this project is to choose the core cell which best responds to our specifications and to design and evaluate a CAM array based on this cell design.

Expected Results:

- Identification of the core cell which best responds to specifications
- Custom design of CAM array
- Characterization of CAM array under different constraints and noise sources (static and dynamic)
- Mitigation techniques for the observed nonidealities.

Tasks:

- Survey of state-of-the art CAM core cells
- Spice design and validation of core CAM cell
- Spice design and validation of CAM search line
    - Study and characterise the impact of process variability of the search performance
    - Study and characterise the search performance in function of line depth and data position
- Layout of CAM search line and post-layout simulation
    - Study and characterise the impact of process variability of the search performance
    - Study and characterise the search performance in function of line depth and data position
- Compare Spice and Post-Layout simulation results
- Identify/propose circuit design techniques to mitigate nonlinearity and optimise the search procedure

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Required skills: gate-level design, post-layout simulations, Spice, Cadence

Work environment:

TIMA Laboratory is a public joint research laboratory located in Grenoble, France, and held jointly by Institut Polytechnique de Grenoble (Grenoble INP), University Grenoble-Alpes and French National Research Council (CNRS). TIMA is a multinational team of over 100 people, with members and interns from all over the world. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end. https://tima.univ-grenoble-alpes.fr/

Application instructions:

A complete application consists of:

- **Cover page:** short motivation of the applicant and connection with the position, including how this position serves future career goals. Include name and contact information of applicant (1 page max)
- **CV:** Academic background, detailing relevant courses and seminars.
- **Relevance for Application:** The applicant should include a clear description of how his or her scholarly background is applicable, and might add value, to the project set out above.

Our lab welcomes applicants with diverse backgrounds and experiences. We regard gender equality and diversity as strength and an asset.

Advisors:

Elena Ioana Vatajelu, CNRS Researcher – TIMA Laboratory
Adrien Post-Boucle, CNRS Engineer – TIMA Laboratory
Frédéric Pétrot, Professor – TIMA Laboratory