Joint IEEE & SoC^2 Day

On

Inversion Coefficient and its Applications

April the 3rd of 2023

Amphi Barbillon – Grenoble INP – 46 Av Felix Viallet
&
Remote acces with zoom visio-conference system

Chairman:
S. BOURDEL

Speakers:
C. Galup, F. Silveira, C Enz, T. Taris, F. Badets, P.M. Ferreira, K. Bouchoucha, D. Pino-Monroy, G. Britton, M. Siniscalchi.

Context:

With the development of advanced technologies, the complexity of electrical models of MOS transistors has increased significantly. Indeed, the reduction of the channel length generates effects that cannot be neglected anymore. Short channel effects such as channel length modulation, mobility reduction or DIBLE are predominant in advanced technologies and make the classical region-based model obsolete. This is a main issue for the development of design methods. Today, circuit pre-sizing using simple models has become very inaccurate and designers rely on intensive simulations to design their circuits in the early stages of design. Beyond a reduction in design efficiency, designers lose the link with the physical phenomena that govern the transistor. This is why the development of design-oriented models, allowing an accurate analytical pre-sizing, is very important and constitutes a fertile field of investigation.

Normalized inversion charge based models are good candidates because they can be implemented with a very small number of parameters. The EKV and ACM models are the most famous ones. Based on these models, many design methods have been developed since the 90s like g_m/I_D or I_C based approaches. Initially dedicated to low frequency domain, these approaches are now gaining radio frequencies. The models have been refined to take into account the short channel effects and allow today to design circuits in a quasi-analytical way while taking into account effects such as non-linearity or frequency limitations.

In addition, recent works report their use for cryogenic applications since the small number of parameters facilitate model extraction.

The purpose of this workshop is to review recent advances in the field of design-oriented modelling and design methods using these models.

Program:

MORNING: Inversion Charge Based Model

9:00 - Welcome Coffee

9:30 - Morning Keynote 1 : Inversion coefficient based MOS model

Abstract:
Compact MOSFET models are indispensable tools for both circuit design and simulation. Many of the existing MOSFET models, however, are not appropriate for design due to reasons such as lack of accuracy, complex equations to describe the MOSFET behavior, excessive number of parameters, and lack of physical meaning of parameters. The ACM model adopted the charge-based approach pioneered by Maher and Mead and fully exploit the inversion level concept, in terms of which the nonlinear behavior of the MOS transistor is easily understood and meaningfully applied to circuit design. Simple formulas in terms of the inversion level are valid in all operating regions, including moderate inversion. This all-region model, which is particularly suitable for the design in advanced CMOS technologies, allows the insightful exploration of the design space.
Contents:
1 Inversion level definition and properties, 2 gm/ID model, 3 All-region I-V MOSFET model, 4 Circuits for VT and IS extraction, 5 Dynamic and noise models.

Speaker: Carlos Galup-Montoro
Carlos Galup-Montoro (M'89) studied Engineering Sciences at the University of the Republic, Montevideo, Uruguay, and Electronic Engineering at the National Polytechnic School of Grenoble (INPG), France. He received an Engineering degree in electronics in 1979 and a doctorate degree in 1982, both from INPG. From 1982 to 1989 he worked at the University of São Paulo, Brazil. Since 1990 he has been with the Electrical Engineering Department, Federal University of Santa Catarina, Florianópolis, Brazil, where he is now a professor. In the second semester of the academic year 1997-998, he was a Research Associate with the Analog Mixed Signal Group, Texas A&M University. He was a Visiting Scholar with UC Berkeley from 2008 to 2009 and with IMEP/INPG in the first trimester of 2017.

10:30 – Coffee Break

11:00 - Morning Sessions:

11:00 - "From 3 to 7 parameters design oriented model". Dayana Pino-Monroy. **Tima Lab and STMicroelectronics**
11:20 - "Cryogenic Applications and their demand for Design Oriented Model". F. Badets – **CEA-LETI Grenoble**.
*11:40 - "Inversion Coefficient Modeling: Simulation-based extraction for Analog/RF Design"***.** T. Taris **– IMS Bordeaux.**
12:00 "Capacitances in compact 7-parameter model for analog design in nanoscale process". Mariana Siniscalchi. **Univ. de la Republica Montevideo URUGAY**.

12:20 – Lunch

AFTERNOON : Inversion coefficient based design

14:00 - Afternoon Keynote : Ratio based analog/RF design: a generalization of gm/ID and Inversion Coefficient methods

Abstract:
Design methods for analog integrated circuits based on gm/ID have the key feature of being based on a magnitude (the gm/ID ratio) that provides information about the transistor operation independently of its width (W, letting aside very narrow transistors rarely applied in analog design) and length (L), except for a slight dependence on L in short channel devices. A general characteristic for the transistors of a given length in a given process is obtained. Therefore, it gives a global view and orientation about the design space. This makes it very suitable for helping the designer to gain insight on how to tune the design and, particularly, aiding novel designers to quickly find their way in the analog design art. The same applies to the, somehow "dual", inversion coefficient (IC) based methods. Both methods are based on magnitudes (gm/ID and IC) that are ratios (or proportional to ratios) of key magnitudes of the transistor operation.
Extensions and evolutions of the gm/ID method have, implicitly or explicitly, identified this "ratio based characteristic" and have shown the advantages of considering other key ratios of magnitudes that share the same characteristics as gm/ID of be W independent. The approach presented is particularly appropriate for nanoscale devices where multiple unitary devices in parallel are usually applied.
This talk will provide an overview on these ratio based analog design approaches, contributing to show a general vision about them. These methods originally targeted small signal analog design. In the talk it will be shown examples of extension of the basic idea to nonlinear RF blocks (power amplifiers and envelope detectors) as well as to distortion analysis.

Speaker: Fernando Silveira
Fernando Silveira received the electrical engineering degree from Universidad de la República, Montevideo, Uruguay, in 1990, and the M.Sc. and Ph.D. degrees in microelectronics from

Université catholique de Louvain, Louvain-la-Neuve, Belgium, in 1995 and 2002, respectively. He is currently a Professor with the Electrical Engineering Department, Universidad de la República. His research interests include the design of ultra-low-power analog and RF integrated circuits and systems, in particular with biomedical application. In this field, he has co-authored two books and many technical papers. He has had multiple industrial activities including leading the design of an application specified integrated circuit for implantable pacemakers and designing analog circuit modules for implantable devices for various companies worldwide, field in which he continues to do consulting. He was member of the Technical Advisory Board of Gtronix, Inc, USA from 2006 to 2010, received the "Ingeniero Destacado" (Distinguished Engineer) award by the Uruguayan Association of Engineers in 2007 and was a member for 2011-2012 of the Distinguished Lecturers Program of the IEEE Circuits and Systems Society. Since 2017 he is a member of the Honorary Committee of the National Researchers System of Uruguay.

15:00 – Coffee Break

15:30 - Afternoon Sessions:

15:30 - "Energy Efficiency and Edge Artificial Intelligence using gm/ID and Inversion Coefficient methods", P. M. Ferreira. **CentraleSupélec Paris**.
15:50 - "The Gm/ID Current Efficiency at Cryogenic Temperature", C. Enz. ICLAB **EPFL Switzerland.**
16:10 - "LNA design for cryogenic applications", Giovani Britton. **Tima Lab and STMicroelectronics**
16:30"Ultra-Low voltage design method using 7-parameters design oriented model", Khalil Bouchoucha. **Tima Lab and STMicroelectronics.**

16:50 – End

Registration:

The workshop participation, including coffee breaks, lunch, etc., is free of any charges. To help the organizers with the logistics please register by sending an e-mail to Laurence Ben-Tito (laurence.ben-tito@univ-grenoble-alpes.fr). Fill the email with the following informations:

Name:
Company:
I will physically attend to the workshop:
I will remotely attend to the workshop:
I have specific demand concerning the lunch: