

RISC-V in Research and Education

- TIMA / LCIS / VERIMAG Laboratories -

July 9th, 2021 - ZOOM Meeting

Robustness, Hardware/ Simulation AMS/RF Async design, Emerging Sensors and Hardware Security Reliability, software and non-uniform circuits and Computing Actuators verification sampling Test codesign systems

| | Program |
|---------------|--|
| 9h00 – 9h10 | Brief introduction |
| 9h10 – 9h40 | RISC-V: An Opportunity for Research and Education – Noureddine Ait-Said |
| 9h40 – 10h10 | An In-Depth Vulnerability Analysis of RISC-V Micro-architecture Against Fault Injection Attack – Zahra Kazemi |
| 10h10 – 10h40 | Microarchitecture-aware Fault Models: Experimental Evidence and Cross- Layer Inference Methodology – Ihab Alshaer |
| 10h40 – 11h00 | Break |
| 11h00 – 11h30 | Introducing Scheduling Optimizations in CompCert with a posteriori verification – Cyril Six |
| 11h30 – 12h00 | Formally-verified Compiler Optimizations for Simple Embedded Cores – Léo Gourdin |

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Join Zoom Meeting

https://univ-grenoble-alpes-fr.zoom.us/j/92323210689?pwd=OUZIOXB0NExtekE2aHprcDcrRS8xZz09

Meeting ID: 923 2321 0689

Passcode: 563130