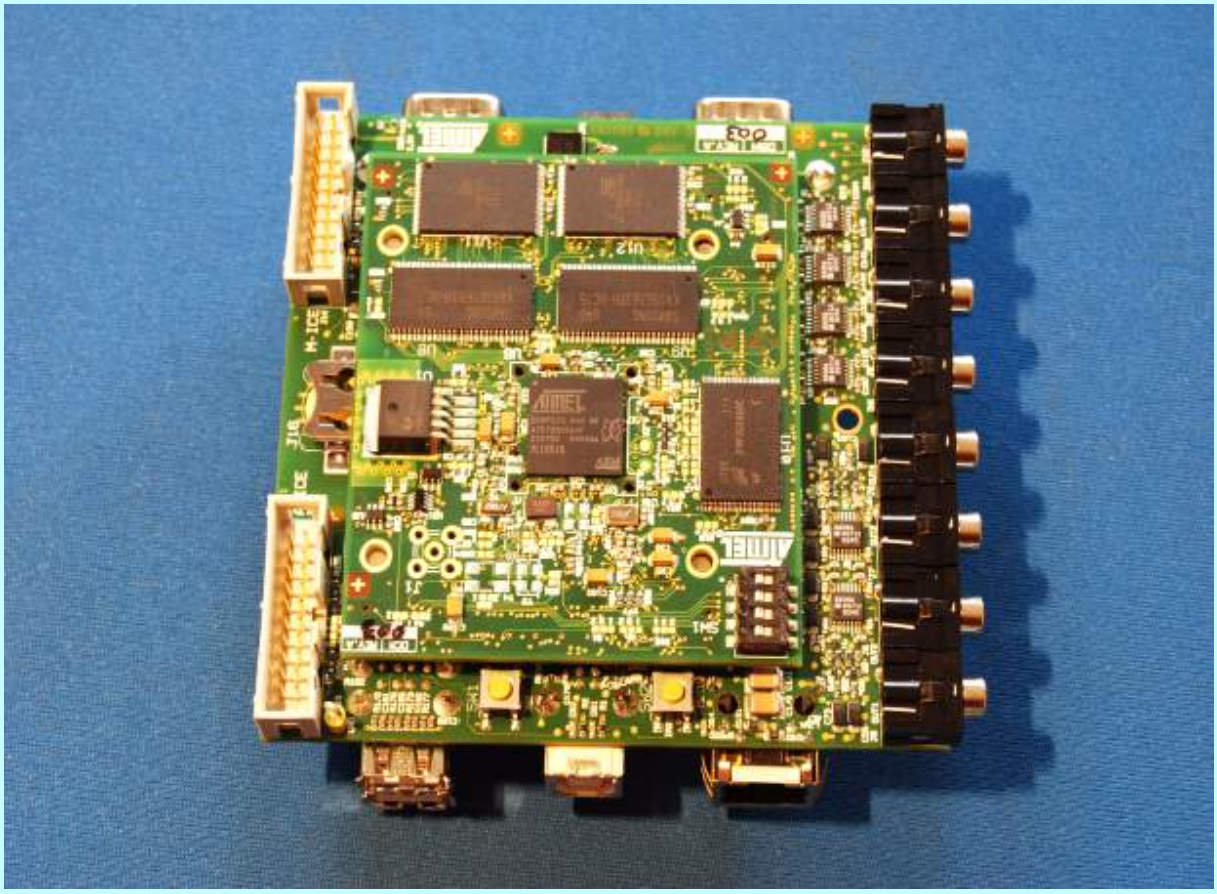
CNRS - Grenoble INP - UGA

SLS team



System Level Synthesis

System Level Synthesis (SLS team)

Research activities

The SLS team focuses on (a) highly efficient architectures for general purpose computing or AI-dedicated algorithms, (b) system-level modeling and design methodology : specification, simulation and verification of hardware/software systems on chip; design exploration and synthesis of hardware. The work of the team is included in the Laboratory themes “Hardware/software codesign” and “Simulation and verification of systems” described below.

Hardware/software codesign

Our research on high performance general purpose processors explores the use of value prediction in processor design. We have shown that simple value prediction can be implemented by reusing existing pipeline structures, leading to increased performance with reduced overheads. We have also shown that predicting values enables the dynamic "reduction" of some instructions (e.g., transforming an add into a nop at runtime), which further improves performance. So far, we have considered value prediction for out-of-order microarchitectures only.

Multi-core and many-core architectures have evolved towards a set of clusters. Each cluster integrates a set of cores, a cache memory and a local memory shared by all the cores of the cluster. We have worked on hardware methods for distributing memory bank accesses in many-core architectures by experimenting on the MPPA Kalray processor. In addition, we have proposed an innovative hardware support for synchronization locks. This decentralized solution manages dynamic re-homing of locks in a dedicated memory, close to the latest access-granted core.

On the dedicated architecture side, the team is still working on Artificial Intelligence. After our work on high-throughput ternary neural network, we have collaborated with the university of Salerno on the design of a tiny Binary Neural Network for human recognition applications.

Through a collaboration with OVHcloud, we also worked on a dedidated IP used in their mitigation systems to face Distributed Denial-of-Service (DDOS) attacks. In this domain, hard- ware developement has to be agile. By introducing the Chisel hardware construction language in the hardware design flow, we showcase how Chisel unleashes the power of agile development methodologies through development iterations. We have also shown through a General Matrix Multiply implementation case study that Chisel can be used to generate highly parametrizable circuits, bringing huge benefits in design exploration, reuse and designer productivity.

Along with the ever-increasing hardware IP development pace, System-on-Chips (SoCs) now integrate a tremendous amount of IPs, each of them specifying more and more interface registers. This exacerbates the already difficult hardware/software integration challenge, which remains a challenge despite the decades that separate us from the first days of computers. We have proposed a generic interface to devices, using message conduit instead of registers and interrupt, taking inspiration from USB and virtualization strategies. This strategy has the benefit of partitioning the driver in a front-end, which is device and operating system dependent, meaning that few distinct front-ends will be required in practice, and a backend that is the responsibility of the device maker. Our prototypes demonstrate that it is suitable for small systems with low latency and low throughput devices (FPGA IP integration), such as high-performance devices in the Linux kernel or in hypervised systems.

Simulation and verification of systems

Modeling and simulation of cyber-physical devices is challenging because of their heterogeneity: discrete events simulation progresses by discrete timesteps while continuous time simulation does so in a time continuum. The SystemC AMS synchronization strategy is based on fixed timesteps and can generate inaccuracies overcame only at expanse of simulation speed. We have proposed a new continuous time and discrete events synchronization algorithm on top of the SystemC framework and have proven its causality, completeness and liveness. In addition, we have also proposed an adaptive algorithm to adjust the synchronization step to provide near to optimum simulation speed. Results on various cases studies have demonstrated that our algorithm circumvents these challenges, attains high accuracy with respect to established tools, and improves simulation speed. This work aims at enlarging the modeling and simulation capabilities of SystemC as a heterogeneous design tool.

Today’s SoCs require a complex design and verification process. In early design stages, high-level debugging of the SoC functionality is feasible on TLM (Transaction-Level Modeling) descriptions. To ease

debugging of such SoC's models, Assertion-Based Verification (ABV) en- ables the runtime verification of temporal properties. In the last design stages, RTL (Register Transfer Level) descriptions of hardware blocks expose microarchitectural details. To gain confi- dence in the validity of system level properties after this TLM-to-RTL synthesis, transaction level assertions must be reverifiable on RTL models. To address that issue, we propose refinement rules for the automatic system level to signal level transformation of PSL assertions (Property Specification Language, IEEE standard 1850).

Many scientific applications require higher accuracy than what can be represented on 64 bits of the floating-point IEEE 754 standard, and to that end make use of dedicated arbitrary precision software libraries such as MPRF. To reach a good performance/accuracy trade-off, developers use variable precision, requiring e.g. more accuracy as the computation progresses. Hardware accelerators for this kind of computations do not exist yet, and independently of the actual quality of the underlying arithmetic computations, defining the right instruction set ar- chitecture, memory representations, etc, for them is a challenging task. We have investigated the support for arbitrary and variable precision arithmetic in a dynamic binary translator (QEMU implementation), to help gain an insight of what such an accelerator could provide as an interface to compilers, and thus programmers. Through collaborations, we also worked on a FP represen- tation supporting both static and dynamically variable precision : by designing its compilation flow to hardware FP instructions or software libraries, and by demonstrating its performance, far better than the Boost programming interface for the MPFR library on the PolyBench suite.

Publications

http://tima.univ-grenoble-alpes.fr/tima/fr/sls/slspublications.html

Academic and research members

Liliana ANDRADE

Position
Associate professor at UGA

Responsibilities
Researcher in SLS team

Arthur PERAIS

Position
Researcher at CNRS

Responsibilities
Researcher in SLS team since 01/10/2020

Laurence PIERRE

Position
Professor at UGA – IM2AG school

Responsibilities
Researcher in SLS team

Olivier MULLER

Position
Associate professor at Grenoble INP – ENSIMAG school

Responsibilities
Leader of SLS team since 01/01/2020
Researcher in SLS team

Frédéric PÉTROT

Position
Professor at Grenoble INP – ENSIMAG school

Responsibilities
Deputy Director of TIMA Lab. since 01/2015
Researcher in SLS team

Frédéric ROUSSEAU

Position
Professor at UGA – POLYTECH school

Responsibilities
Researcher in SLS team

CNRS (French National Center for Scientific Research)
ENSIMAG school (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. BADAROUX Marie
Title of thesis: **Fast and accurate simulation of multi/many-core SoCS**
Expected date of defense: **2023**
Previous degrees: Master – Grenoble INP – ENSIMAG, France (2020)

2. BAUMELA Thomas
Title of thesis: **Externalisation of device drivers from embedded processors to devices**
Expected date of defense: **2021**
Previous degrees: Engineer – Université Grenoble Alpes, France (2016)

3. BONICEL Louis
Title of thesis: **Study of an architectural model for code generation taking into account the real time constraints of an embedded system in the electrical measure and protection domain**
Expected date of defense: **2022**
Previous degrees: Engineer – Polytech Montpellier, France (2017)

4. BRUANT Jean
Title of thesis: **Abstracting FPGA development flow as a modern software development flow**
Expected date of defense: **2021**
Previous degrees: Engineer - Télécom Bretagne, France (2018)

5. CHRIST Maxime
Title of thesis: **Learning in very low precision**
Expected date of defense: **2022**
Previous degrees: Engineer - INSA Lyon, France (2017)

6. FERNANDEZ-MESA Breytner Joseph
Title of thesis: **Exploration of Direct Synchronization Approaches for a High-Level and Unified Simulation of Discrete-Event/Continuous-Time Systems**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidad de Los Andes – Mérida, Venezuela (2017)

7. FERRES Bruno
Title of thesis: **Task migration software/hardware in an heterogeneous and reconfigurable system**
Expected date of defense: **2022**
Previous degrees: Engineer – Grenoble INP - Ensimag, France (2018)

8. MILICI Giulio
Title of thesis: **Strategy of crosspoint non-volatile memory integration in cache hierarchy of a multicore architecture**
Expected date of defense: **2021**
Previous degrees: Engineer – Politecnico di Torino, Italy (2018)

9. TREVISAN JOST Tiago
Title of thesis: **Compiler-Hardware interface of emerging UNUM number formats**
Expected date of defense: **2022**
Previous degrees: Master – Federal University of Rio Grande do Sul, Brazil (2017)

10. VIANES Arthur
Title of thesis: **Integration of a Manycore Accelerator in a High-Performance Processor**
Expected date of defense: **2022**
Previous degrees: Engineer Polytech Grenoble, France (2018)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

No positions in 2020.

Visitors

Name	Forename	Country	Duration
1. DE VITA	Antonio		

Trainees

Name	Forename	Country	Duration
1. DJEAFEA SONWA	Medric Bruel	CAMEROON	
2. HAMAIN	Thomas Frederic Robert	RUSSIAN FED	
3. LAGAROSSE	Paul	FRANCE	
4. ROBE	Guillaume	FRANCE	
5. YADAV	Archit	INDIA	
6. ZHANG	Shuo	CHINA	
7. KEMEH	Marck-Edward	GHANA	

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANR

RAKES
Responsable scientifique : PETROT Frédéric
Durée : 2019 - 2023

ANRT

CIFRE Arthur VIANNES
Responsable scientifique : ROUSSEAU Frédéric
Durée : 2019 - 2022

CIFRE Jean BRUANT
Responsable scientifique : MULLER Olivier
Durée : 2018 - 2022

CIFRE Louis BONICEL
Titre : "Etude d'un modèle architectural pour la génération de code intégrant les contraintes d'un système temps réel embarqué dans le domaine de la mesure et la protection électrique"
Responsable scientifique : PETROT Frédéric
Durée : 2018 - 2021

CIFRE Lucas FERNANDEZ-BRILLET
Titre : "Architectures intégrrées 3D de réseaux de neurones CNN pour la vision embarquée"
Responsable scientifique : MANCINI Stéphane
Durée : 2017 - 2020

CEC-NATIONAL

AI4DI
Programme : ECSEL
Titre : Artificial Intelligence for Digitizing Industry
Responsable scientifique : PETROT Frédéric
Durée : 2019 - 2022

EPST

ARTE
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Architectures de Réseaux de neurones Ternaires dédiées pour l'Embarqué
Responsable scientifique : ANDRADE PORRAS Liliana Lilibeth
Durée : 2019 - 2020

Digital Hardware AI Architectures
Programme : MIAI (Multidisciplinary Institute in Artificial Intelligence)
Type : EPST
Responsable scientifique : PETROT Frédéric
Durée : 2019 - 2023

Organization and participation of international conferences, workshops, forums

31st International Workshop on Rapid System Prototyping (RSP'2020)
September 24-25, 2020, Virtual event, FRANCE
Rang : B
steering committee member: PETROT F., ROUSSEAU F.
technical program committee: MULLER O., PETROT F., ROUSSEAU F.
program chair: ROUSSEAU F.
publication chair: MULLER O.

Conférence francophone d'informatique en Parallélisme, Architecture et Système (COMPAS'2020)
June 30-July 03, 2020, Lyon, FRANCE
Rang : NC
technical program committee: PETROT F.
20th International Forum on MPSoC for Software-Defined Hardware (MPSoC'2020)
June 28-July 3, 2020, Megève, FRANCE
Rang : NC
general chair: PETROT F.
technical program committee: PETROT F.
finance chair: ROUSSEAU F.
local organization: MULLER O., ROUSSEAU F.

23rd Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS'2020)
April 22-24, 2020, Novi Sad, SERBIA
Rang : B
technical program committee: PIERRE L.

Design, Automation & Test in Europe (DATE'2020)
March 9-13, 2020, Grenoble, FRANCE
Rang : A+
University Booth Co-Chair: PETROT F.

12th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO'2020)
January 21, 2020, Bologna, ITALY
Rang : NC
technical program committee: PETROT F.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
ENSIMAG school École nationale supérieure d'informatique et de mathématiques appliquées				
Deputy Director	PETROT F.	01/09/2018	31/08/2022	
Restricted council member	MULLER O.	01/09/2017		Examine promotion files, invited professors, teaching assistants
	PETROT F.	01/09/2017		
School council member	MULLER O.	01/09/2017		Elected members - School Strategy, relations with industrial partners
	PETROT F.	01/09/2017		
POLYTECH Grenoble				
Manager of E2I branch	ANDRADE L.L.	01/10/2019		5th year - Apprenticeship training
Deputy director in charge of education and training	ROUSSEAU F.	01/09/2018		
Restricted council member	ROUSSEAU F.	01/09/2017		Examine promotion files, invited professors, teaching assistants
School council member	ROUSSEAU F.	01/09/2017		Elected members - School Strategy, relations with industrial partners
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Research commission member	PIERRE L.	01/09/2017		Examine promotion files, invited professors, teaching assistants
UFR Council member	PIERRE L.	01/09/2017		
TIMA laboratory				
Laboratory contact for european projects	ROUSSEAU F.	01/09/2017		
Research structures				
École doctorale EEATS Électronique Électrotechnique Automatique & Traitement du signal				
HDR commission member of EEATS doctoral school	ROUSSEAU F.	01/09/2017		
École doctorale MSTII Mathématiques, Sciences et Technologies de l'Information, Informatique				
Council member of MSTII doctoral school	PIERRE L.	01/09/2017		
HDR commission member of MSTII doctoral school	PETROT F.	01/09/2017		
LABEX PERSYVAL Pervasive Systems and Algorithms				
Education Board Member	PIERRE L.	01/06/2015		Training activities
Pôle MSTIC Mathématiques, sciences et technologies de l'information et de la communication				
TIMA representative of MSTIC cluster	PETROT F.	01/09/2016		
Parent institutions				
UGA Université Grenoble Alpes				
Manager of Informatics Master M1-M2 UGA – G-INP	PIERRE L.	01/09/2017		In charge for UGA

Scientific production

International journals

Fernandez-Mesa B.J., **Andrade Porras L.L.**, **Pétrot F.**, Synchronization of Continuous Time and Discrete Events Simulation in SystemC, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Ed. IEEE, Vol. , DOI: 10.1109/TCAD.2020.3019204, 2020

Invited conferences talks

1 **Pétrot F.**, **Anghel L.**, **Andrade Porras L.L.**, State of the art in hardware-accelerated neural networks, Invited Talk, Applied Machine Learning Days (AMLD 2020), Lausanne, SWITZERLAND, 27 au 29 janvier 2020

International conferences

Leclaire N., **Mancini S.**, **Delnondedieu C.**, **Henriques J.P.**, Efficient Implementation of Convolution and Winograd on ASMP Embedded Multicore Vector Processor, IEEE International Workshop on Signal Processing Systems (SIPS 2020), Coimbra (Virtual event), PORTUGAL, 20 au 22 octobre 2020

Trevisan Jost T., **Durand Y.**, **Fabre Ch.**, **Cohen A.**, **Pétrot F.**, VP Float: First Class Treatment for Variable Precision Floating Point Arithmetic, International Conference on Parallel Architectures and Compilation Techniques (PACT 2020), pp. 355-356, Atlanta, UNITED STATES, 5 au 7 octobre 2020

Pêcheux F., **Andrade Porras L.L.**, **Louërat M.-M.**, **Bournias I.**, **Chotin-Avot R.**, **Genius D.**, Virtual Prototyping of Open Source Heterogeneous Systems with an Open Source Framework Featuring SystemC MDVP Extensions, Forum for Specification and Design Languages (FDL 2020), pp. 1-8, Kiel, GERMANY, DOI: 10.1109/FDL50818.2020.9232947, 15 au 17 septembre 2020

De Vita A., **Pau D.**, **Di Benedetto L.**, **Rubino A.**, **Pétrot F.**, **Licciardo G.D.**, Low Power Tiny Binary Neural Network with improved accuracy in Human Recognition Systems, Euromicro Conference on Digital System Design (DSD 2020), pp. 309-315, Kranj, SLOVENIA, DOI: DOI 10.1109/DSD51259.2020.00057, 26 au 28 août 2020

France-Pillois M., **Martin J.**, **Rousseau F.**, Implementation and Evaluation of a Hardware Decentralized Synchronization Lock for MPSoCs, International Parallel and Distributed Processing Symposium (IPDPS 2020), pp. 1112-1121, New Orleans, UNITED STATES, DOI: 10.1109/IPDPS47924.2020.00117, 18 au 22 mai 2020

Fernandez-Mesa B.J., **Andrade Porras L.L.**, **Pétrot F.**, Accurate and Efficient Continuous Time and Discrete Events Simulation in SystemC, Design, Automation and Test in Europe (DATE 2020), Grenoble, FRANCE, 9 au 13 mars 2020

Other communications

Ferres Bruno, **Muller O.**, **Rousseau F.**, Chisel Usecase: Designing General Matrix Multiply for FPGA, Applied Reconfigurable Computing. Architectures, Tools, and Applications (ARC 2020), pp. 61-72, Toledo, SPAIN, DOI: 10.1007/978-3-030-44534-8_5, 2020

Christ M., **Forget L.**, **De Dinechin F.**, Lossless Differential Table Compression for Hardware Function Evaluation / Compression de table sans perte pour l'évaluation matérielle de fonctions, , Grenoble, FRANCE, 2020

Bruant J., **Horrein P.H.**, **Muller O.**, **Groleat T.**, **Pétrot F.**, (System)Verilog to Chisel Translation for Faster Hardware Design, 31th International Symposium on Rapid System Prototyping (RSP 2020), Virtual Conference, FRANCE, 2020