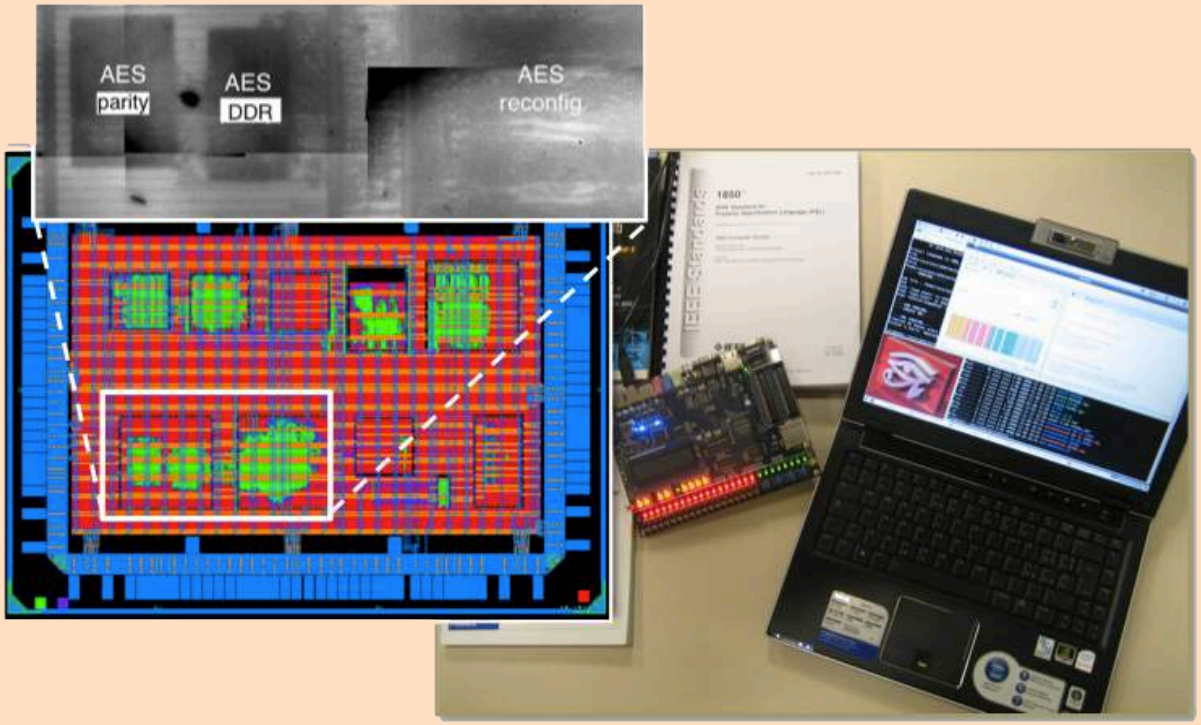
CNRS - Grenoble INP - UGA

AMfoRS team



Architectures and Methods for Resilient Systems

Architectures and Methods for Resilient Systems (AMfoRS team)

http://tima.univ-grenoble-alpes.fr/tima/fr/amfors/amforsoverview.html

The **AMfoRS** team addresses dependability and trust of digital systems at multiple abstraction levels for specific application domains (e.g., automotive, avionics, smartcards, IoT), by guaranteeing that digital circuits possess properties such as quality, reliability, safety, security, availability. The work of the team is focused on design and analysis methods, techniques and tools to assess and improve circuits dependability and trust, for the above-mentioned domains.

Research activities

Robustness and dependability

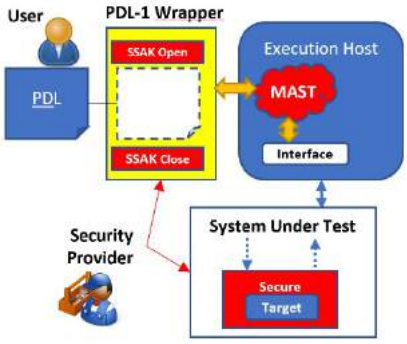
Many domains have functional safety among the classical list of design constraints, e.g. ISO 26262 standard in automotive. Our work aims at improving **early evaluations of dependability** w.r.t. errors induced by environmental disturbances. The goal, to reduce development and production costs, is to be able to evaluate accurately and at an early stage of the design the potential functional effects of soft and permanent errors. We have recently proposed a **cross-layer fault simulation method** to perform the robustness evaluation of RTL architectures used in critical embedded systems, based on both fault simulation in RTL and Transaction Level Model (TLM) descriptions to make a trade-off between simulation time and realism of the simulated high level faulty behaviors, with application to an airborne case study. In the context of **radiation** testing, we have evaluated the vulnerability of hardware-implemented machine learning algorithms, which are finding their way in various domains, including safety-critical applications. Thus, these algorithms have to perform correctly even in harsh environmental conditions, such as in avionics altitudes. Support Vector Machine (SVM) is an important Machine Learning that has been target of hardware implementation in recent years. We have presented the first evaluation of SVMs under thermal neutron radiation along with the first assessment of radiation effects on Multiclass SVMs, proving that Multiclass SVM present an overall higher reliability when compared to a Binary SVM.

We have recently worked on **memory system reliability**, which is a serious concern today and is becoming more worrisome as technology scales, system size grows and the demand of aggressive voltage reduction becomes more stringent. In this context, Error Correcting Codes (ECC)-based repair techniques were proposed and offer aggressive reduction of the repair cost for high defect densities, but this approach suffers from the fact that, single particles induce Single-Event Upsets (SEUs) may lead to Multi-Cell Upsets (MCUs) and Multi-Bit Upsets (MBUs) in the same memory word. Standard mitigating approaches based on interleaving exist, but the impact of MBUs on the repairing circuitry needs also to be mitigated, through a repair Content Addressable Memory (CAM) having interleaving at its data-words, or else an Offset CAM. We have presented and evaluated a novel repair approach based on the Offset CAM in ECC-based Memory Repair and hence permits the mitigation of the MBUs affecting it.

Due to technology scaling and transistor size getting smaller and closer to atomic size, the last generation of CMOS technologies presents more variability in various physical parameters. Moreover, circuit wear-out degradation leads to additional temporal variations, potentially resulting in timing and functional failures. To handle such problems, one conventional method consists in providing more safety margins (also called guard bands) at design-time. Therefore, the usage of delay violation **monitors** becomes a must. Placing the monitors is a critical task as the designer has to carefully select the place that will age the most and may become a potential point of failure in a given design.

We have explored the use of **Machine Learning techniques** in order to drive the automated selection of potential insertion points of such monitors. Digital delay analysis of basic gates using multiple linear regression has been modeled, predicted, and validated against original data using spice simulation. We have compared multiple linear regression algorithms and used them to study the aging mechanism of CMOS basic gates using supervised learning algorithms. We have showed how it is possible to reliably estimate activity-related path aging and tune the prediction framework by extracting activity profiles from simulations on a synthesized design, which allows a finer grain estimation by obtaining activity profiles at both the path and gate-level.

System-level test and standards



The IEEE 1687-2014 standard proposes solutions for the access and usage of Embedded Instruments, but Electronic Design Automation (EDA) is still limited to only a small subset of the new features. In this context, in the frame of the Eureka European project HADES, we improved our innovative Test Flow and Environment called **"Manager for SoC Test" (MAST)**, a software backend able to provide features and performance superior to the industrial legacy solutions. We have proposed an innovative solution that exploits the dynamic nature of the standard to obtain an Authentication-based Secure Access framework able to provide a trusted, configurable, efficient, and transparent interface to the test infrastructure depending on user-defined security levels. Our framework extends MAST with a novel solution developed within the team, the **"*Segment Set Authorization Keys*" (SSAK)** protocol. Security-wise, secret sharing is limited to a minimum; from a performance point of view, the tool fully leverages its strength in terms of topology resolution and concurrent execution. Last but not least, user experience is also optimal, as security is handled automatically and transparently.

Hardware security and trust

The team works on the design of cryptographic/secure primitives, and the analysis of security and trust threats, by proposing effective countermeasures. We work on algorithms, schemes, and protocols, such as the **SSAK protocol** for secure test access (see System- level Test), post-quantum cryptography, homomorphic encryption, and non-linear codes for protecting circuits against fault attacks. Concerning the security threats, we work regularly on implementation attacks. In 2020, we have set up a platform for **side channel attacks** on embedded systems. The environment allows the designer to perform power and EM analysis, and clock and voltage glitch attacks on ARM microcontrollers and FPGA boards. Near-Field EM probes complete the setup, in the LF and RF bandwidths. The platform is going to be extended by supporting EM Fault Injection (EMFI) equipment in the next year. This platform has been partially supported by IRT Nanoelec and by the CNRS (INS2I). In the context of **Control Flow Hardening**, we have proposed the use of nonlinear codes. Hardware-based control flow monitoring techniques enable to detect both errors in the control flow and the instruction stream being executed on a processor. However, these techniques may fail to detect malicious carefully tuned manipulation of the instruction stream in a basic block. We have shown how using a non-linear encoder and checker can cope with this weakness. Concerning the secure primitives, we are currently working on secure elements such as Physically Unclonable Functions to cope with reliability issues, and True Random Number Generators with memristive and spintronic devices. In this context, we have set up an experimental platform, financed by the CNRS/INS2I, for the evaluation of **SRAM-based PUFs**. Concerning the trust issues, we are working on methods to detect and possibly avoid the presence of hardware Trojan horses.

New hardware computing approaches

Today's computing systems are facing several issues related to architectural and technological limitations. To mitigate these issues, novel computing paradigms, such as **Computing-in-Memory**, **Neuromorphic Computing** and **Approximate Computing**, are being researched, in conjunction with novel emerging technologies such as memristive and spintronic devices. Concerning these devices, our research aims at using enhanced compact models to perform failure analysis, and define pertinent fault models to establish design-for-test and design-for-reliability methodologies. Concerning the Computing-in-Memory paradigm, we are investigating feasible design solutions, with a special focus on applications for security. Concerning Neuromorphic Computing, we are focusing on the reliability analysis and test of spiking neural networks. Concerning the Approximate Computing paradigm, which has been gaining momentum both in the industry and in academia, we are studying the trade-offs between selective approximation (or occasional violation of specifications) and power consumption. We are also working on an extension of a tool initially developed for dependability evaluation (EARS) in order to identify from RTL descriptions and a given application the operators that are the less sensitive to approximations.

Recent highlights

New recruitment

- Brice Colombier, Assistant Professor

Dissemination

- Book: **Di Natale G.**, Gizopoulos D., Di Carlo S., Bosio A., Canal R. (Eds.) *Cross-Layer Reliability of Computing Systems*, Ed. IET - The Institution of Engineering and Technology, 2020
- Invited talk: Regazzoni F., […], **Di Natale G.**, […], **Vatajelu I.**, et al., *Machine Learning and Hardware security: Challenges and Opportunities*, International Conference on Computer-Aided Design (ICCAD 2020)
- Keynote: **I. Vatajelu**, *Versatility of Emergent Memory Technologies: Friend or Foe?,*
- The 17th Biennial Baltic Electronics Conference, Tallin 2020

Involvement in research activities

- Participation to the IEEE P1687.1 Working Group
- Participation to the Grenoble Alpes CyberSecurity Institute for post-quantum cryptography

Platforms and demonstrators

- A comprehensive platform for hardware/software co-design based on the RISC-V processor architecture. The platform supports several RISC-V implementations (such as the Rocket Chip or CVA6) and it features high modularity and tuning capabilities (https://tima-amfors.gricad-pages.univ-grenoble-alpes.fr/learnv/)
- Hardware demonstrator for Secure Access to 1687 Test Infrastructure
- Experimental platforms for Side Channel Analysis and PUF evaluation
- Open-source fault injection tool for SNNs

Academic and research members

Lorena ANGHEL

Position
Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team until 31/05/2020

Mounir BENABDENBI

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Brice COLOMBIER

Position
Associate Professor at Grenoble INP - PHELMA school since 01/09/2020

Responsibilities
Researcher in AMfoRS team since 01/09/2020

Giorgio DI NATALE

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team
Director of TIMA Lab. Since 01/01/2021

Régis LEVEUGLE

Position
Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Paolo MAISTRI

Position
Researcher at CNRS

Responsibilities
Leader of AMfoRS team
Researcher in AMfoRS team

Mihail NICOLAIDIS

Position
Research Director at CNRS

Responsibilities
Researcher in AMfoRS team

Michele PORTOLAN

Position
Associate Professor at Grenoble INP - PHELMA school

Responsibilities
Researcher in AMfoRS team

Rodrigo POSSAMAI BASTOS

Position
Associate Professor at UGA - IM2AG school

Responsibilities
Researcher in AMfoRS team since 01/07/2020

Elena-Ioana VATAJELU

Position
Researcher at CNRS

Responsibilities
Researcher in AMfoRS team

Raoul VELAZCO

Position
Professor Emeritus at CNRS

Responsibilities
Researcher in AMfoRS team since 01/01/2020

Nacer-Eddine ZERGAINOH

Position
Associate Professor at UGA - POLYTECH school

Responsibilities
Researcher in AMfoRS team since 01/01/2020

CNRS (French National Center for Scientific Research)
Grenoble INP (Grenoble Institute of Technology)
IM2AG school (Informatique, Mathématiques et Mathématiques Appliquées)
PHELMA school (Physique-Electronique-Matériaux)
UGA (Université Grenoble Alpes)

Ph. D. candidates

1. AIT SAID Noureddine
Title of thesis: **Self adaptive precision in SoCs: design and verification techniques**
Expected date of defense: **2021**
Previous degrees: Engineer - Institut National des Postes et Télécommunications de Rabat, Morocco (2018)

2. ALI POUR Amir
Title of thesis: **PUF based Secure Computing for Constraint Cyber Physical Object**
Expected date of defense: **2022/2023**
Previous degrees: Engineer (2020)

3. ALSHAER Ihab
Title of thesis: **Cross-Layer Fault Analysis for Microprocessor Architectures (CLAM)**
Expected date of defense: **2023**
Previous degrees: Engineer

4. CINÇON Valérian
Title of thesis: **Ultra low power integration of neuro-morphic systems on FD-SOI**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2018)

5. DADDINOUNOU Salah
Title of thesis: **Test and reliability of spiking neural networks**
Expected date of defense: **2023**
Previous degrees: Engineer (2019)

6. FIORUCCI Tiziano
Title of thesis: **Qualification methodology for ISO26262 certification of automotive SoC systems**
Expected date of defense: **2023**
Previous degrees: Engineer

7. GARAY TRINDADE Matheus
Title of thesis: **Optimization and Qualification of Hardware Machine-Learning Systems under Radiation-Induced Effects**
Expected date of defense: **2021**
Previous degrees: Engineer – Universidade Federal de Santa Maria, Rio Grande do Sul, Brazil (2017)

8. GERBAUD Merlin
Title of thesis: **Hardware Security Techniques for Cryptographic Algorithms taking advantage of In-Memory Computing**
Expected date of defense: **2023**
Previous degrees: Engineer

9. INGLESE Pietro
Title of thesis: **Exploration of security threats in In-Memory Computing Paradigms**
Expected date of defense: **2023**
Previous degrees: Engineer – Politecnico di Torino, Italy (2019)

10. JAAMOUN Amine
Title of thesis: **Strategies for securing a memory hierarchy against software side channel attacks**
Expected date of defense: **2022/2023**
Previous degrees: Master 2 Systèmes électroniques et systèmes informatiques – Université Pierre et Marie Curie Paris 6 (2020)

11. KRAEMER SARZI SARTORI Tarso
Title of thesis: **Mitigation of Space-to-Ground Radiation Effects on Attitude Estimation Algorithms for Inertial Navigation Systems**
Expected date of defense: **2023**
Previous degrees: Engineer – Aerospace engineering – Federal University of Santa Maria, Brazil (2020)

12. LINARES Antoine
Title of thesis: **Flexible Hardware for Intrinsic Secure computing**
Expected date of defense: **2023**
Previous degrees: Engineer

13. MARTINOLI Valentin
Title of thesis: **Secure Processors with respect to Micro Architectural Attacks**
Expected date of defense: **2023**
Previous degrees: Engineer

14. REYNAUD Vincent
Title of thesis: **Secured access to IEEE 1687 test resources and lightweight crypto-processors in the IoT context**
Expected date of defense: **2021**
Previous degrees: Engineer – Grenoble INP – Phelma, France (2017)

15. SENTHAMARAI KANNAN Kalpana
Title of thesis: **Performance and Safety/Security Management in automotive and IoT applications**
Expected date of defense: **2021**
Previous degrees: Engineer - Pondichery University, India (2013)

16. SHAH Riddhi
Title of thesis: **HiRel Product Demonstration by Dynamic Wearout Management**
Completed on: **October 5th, 2020**
Previous degrees: Engineer – Nirma University, India (2016)

Other members

Post-doctoral position – Engineers – Experts – Teaching Assistants (ATER)

No positions in 2020

Visitors

Name	Forename	Country	Duration
1. GUPTA	Vishal	INDIA	3 months
2. HONORIO	Martin	SPAIN	3 months
3. IANNICELLI	Pierpaolo	ITALY	5 months

Trainees

Name	Forename	Country	Duration
1. AFLIHAOU	Houdeifa	ALGERIA	3 months
2. AMANS	Annabel	FRANCE	2 months
3. BOUDIAF	Imene Milissa	ALGERIA	2 months
4. GUIRONNET	Solenn	FRANCE	2 months 14 days
5. HO	Duc Nhan	VIET NAM	5 months
6. JABRANE	Kenza	MOROCCO	3 months
7. LIN	Jiaru	-	2 months
8. LUO	Zhifei	CHINA	2 months
9. MAILLEFERT	Antoine	FRANCE	2 months 8 days
10.MALDANER	LiÃ¨ge	BRAZIL	2 months
11.MESNAGER	Victor	FRANCE	2 months 13 days
12.OLIVEIRA	Alexandre	FRANCE	2 months 13 days
13.PASCAL-VALETTE	Djeson Franck	FRANCE	2 months 13 days
14.VARADARAJULU	Swetha	INDIA	6 months
15.VINAGRERO GUTIERREZ	Sergio	SPAIN	2 months 13 days
16.ZECH	Guillaume	FRANCE	2 months

Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2020.

ANR

EMINENT
Responsable scientifique : VATAJELU Ioana
Durée : 2019 - 2023

ANRT

CIFRE Antoine LINARES
Titre : Flexible Hardware for Intrinsic Secure Computing
Responsable scientifique : DI NATALE Giorgio
Durée : 2020 - 2023

CIFRE Valérian CINCON
Titre : "Etude et intégration de systèmes neuro-morphiques ultra basse consommation en technologie FD-SOI"
Responsable scientifique : ANGHEL Lorena
Durée : 2018 - 2021

CIFRE Riddhi J. SHAH
Titre : "Etude et réalisation de démonstrateurs ayant une gestion dynamique du vieillissement pour les applications exigeant une haute fiabilité"
Responsable scientifique : ANGHEL Lorena
Durée : 2017 - 2020

CEC

QUOG-DP
Programme : ATTRACT Project
Titre : Quantum Optimization of Worldwide LHC Computing Grid data placement
Responsable scientifique : ZERGAINOH Alain Nasserdine
Durée : 2019 - 2020

EPST

CLAM
Programme : Equipe-Action Labex Persyval
Titre : Cross-Layer Fault Analysis for Microprocessor Architectures
Responsable scientifique : MAISTRI Paolo
Durée : 2020 - 2023

AVOCAM
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Analyse de durée de Vie pour l'Optimisation de Calcul Approché Matériel
Responsable scientifique : LEVEUGLE Régis
Durée : 2020 - 2021

State
Responsable scientifique : POSSAMAI BASTOS Rodrigo
Durée : 2020 - 2023

IRT Vision embarquée
Programme : IRT
Responsable scientifique : BENABDENBI Mounir
Durée : 2020 - 2020

EPST (suite)

IRT Cybersécurité
Programme : IRT
Responsable scientifique : MAISTRI Paolo
Durée : 2020 - 2020

IRT Intelligence Artificielle et sécurité matérielle
Programme : IRT
Responsable scientifique : ANGHEL Lorena
Durée : 2020 - 2020

Hardware for spike-coded neural networks exploiting hybrid CMOS non-volatile technologies
Programme : MIAI (Multidisciplinary Institute in Artificial Intelligence)
Responsable scientifique : ANGHEL Lorena
Durée : 2019 - 2020

CADI
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Calcul Approché et Distribué dans les systèmes Intégrés
Responsable scientifique : BENABDENBI Mounir
Durée : 2019 - 2020

CROCHET
Programme : IRS (Initiative de Recherche Stratégique)
Titre : Low Cost Control Flow Checking for Secure Applications Based on Nonlinear Codes
Responsable scientifique : DI NATALE Giorgio
Durée : 2019 - 2020

Cyber@Alpes
Programme : Grenoble Alpes CyberSecurity Institute
Responsable scientifique : MAISTRI Paolo
Co-partage d'équipes (AMfoRS, CDSI)
Durée : 2018 – 2021

EUREKA

HADES
Programme : PENTA
Titre : Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems
Responsable scientifique : MIR Salvador
Co-partage d'équipes (AMfoRS, RMS)
Durée : 2017 - 2020

INDUSTRIE

Processeurs Sécurisés et Attaques de micro architectures
Responsable scientifique : LEVEUGLE Régis
Durée : 2020 - 2023

REGION

MULTIRAD
Programme : Pack Ambition International
Responsable scientifique : POSSAMAI BASTOS Rodrigo
Durée : 2020 - 2021

OVNIPROM
Programme : SCUSI
Titre : "Ordinateur de vol d'un nanosatellite implémenté dans un processeur many-core"
Responsable scientifique : VELAZCO Raoul
Durée : 2017 - 2020

SAFE-AIR
Programme : Pack Ambition Recherche
Titre : Safety Evaluation of Aircraft Systems using Virtual Platforms
Responsable scientifique : LEVEUGLE Régis
Durée : 2017 - 2022

SATT

Ovnipromsat / OVSAT
Responsable scientifique : PANCHER Fabrice
Durée : 2019 - 2020

Organization and participation of international conferences, workshops, forums

16th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA'2020)
December 1-4, 2020, Virtual event from Porto Alegre (Brazil), BRAZIL
Rang : NC
general chair: VELAZCO R.

IEEE International Test Conference (ITC'2020)
November 3-5, 2020, Washington DC, USA
Rang : A+
steering committee member: DI NATALE G.
technical program committee: VATAJELU E.I.

33rd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT'2020)
October 19-21, 2020, Frascati (Roma), ITALY
Rang : A
technical program committee: DI NATALE G.

26th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS'2020)
July 13-15, 2020, Virtual event from Naples (Italy), ITALY
Rang : B
general chair: NICOLAIDIS M.
technical program committee: DI NATALE G., LEVEUGLE R., NICOLAIDIS M., BENABDENBI M
steering committee member: NICOLAIDIS M.

8th Prague Embedded Systems Workshop (PESW'2020)
June 25-27, 2020, Roztoky u Prahy, CZECH REP.
Rang : NC
technical program committee: VATAJELU E.I., DI NATALE G.

25th IEEE European Test Symposium (ETS'2020)
May 25-29, 2020, Tallinn, ESTONIA
Rang : A
program co-chair: VATAJELU E.I.
technical program committee: DI NATALE G., VATAJELU E.I., ANGHEL L.
steering committee member: ANGHEL L., DI NATALE G., VATAJELU E.I.
topic chair: LEVEUGLE R., VATAJELU E.I.
embedded tutorial chair: ANGHEL L.
publication chair: DI NATALE G.

Test Spring School (TSS'2020)
May 22-25, 2020, Tallinn, ESTONIA
Rang : NC
technical program committee: VATAJELU E.I.

23rd Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS'2020)
April 22-24, 2020, Novi Sad, SERBIA
Rang : B
technical program committee: LEVEUGLE R., MAISTRI P., PORTOLAN M., VATAJELU E.I.

38th IEEE VLSI Test Symposium (VTS'2020)
April 5-8, 2020, San Diego, USA
Rang : A
general chair: ANGHEL L.
publication chair: VATAJELU E.I.
technical program committee: DI NATALE G.

15th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS'2020)
April 1-3, 2020, Marrakesh, MOROCCO
Rang : NC
track chair: VATAJELU E.I.
technical program committee: BENABDENBI M., VATAJELU E.I.

21st IEEE Latin-American Test Symposium (LATS'2020)
March 30-April 2, 2020, Jatiúca (Maceió), BRAZIL
Rang : NC
steering committee member: VELAZCO R.
technical program committee: LEVEUGLE R., VELAZCO R.

Design, Automation & Test in Europe (DATE'2020)
March 9-13, 2020, Grenoble, FRANCE
Rang : A+
general chair: DI NATALE G.
publication chair: VATAJELU E.I.
technical program committee: ANGHEL L., PORTOLAN M.
local organization: ANGHEL L.

Responsibilities

Role	TIMA member	Starts	Ends	Comments
Faculties / Schools				
PHELMA school PHysique, ÉLectronique, Matériaux				
Board of Directors member	ANGHEL L.	01/09/2017	31/05/2020	Strategy, jobs, promotion files, invited professors, teaching assistants
Co-responsible of SEI branch	BENABDENBI M.	01/09/2017		
Manager of SEOC/PHELMA branch	PORTOLAN M.	01/09/2017		
School council member	ANGHEL L.	01/09/2016	31/05/2020	Elected members - School Strategy, relations with industrial partners
UFR IM2AG Informatique, Mathématiques et Mathématiques Appliquées				
Manager of Office Automation and Informatics	POSSAMAI BASTOS R.	01/09/2017		Formation à tous les parcours du Département Licence Sciences et Technologies de l'UGA
Research structures				
CIME Nanotech Centre Interuniversitaire de MicroElectronique et Nanotechnologies				
Manager of Design platform	BENABDENBI M.	01/09/2017		
CSUG Centre Spatial Universitaire de Grenoble				
Technical manager	PANCHER F.	02/05/2018		
FMNT Fédération des Micro et Nanotechnologies				
Manager of Microelectronics Axis	ANGHEL L.	01/09/2017	31/05/2020	
MSTIC pole Mathématiques, sciences et technologies de l'Information et de la communication				
Council member of MSTIC cluster	LEVEUGLE R.	01/09/2015		Elected member - Examine invited professors files, mobilities, jobs prospectives for IATS/EC
Parent institutions				
Grenoble INP				
Deputy vice-president for Industry relations	ANGHEL L.	01/09/2017	31/05/2020	

Scientific production

International journals

1 **Morgül M.C., Frontini L., Tunali O., Anghel L., Ciriani V., Vatajelu I., Moritz C.A., Stan M., Alexandrescu D., Altun M.,** Circuit Design Steps for Nano-Crossbar Arrays: Area-Delay-Power Optimization with Fault Tolerance, IEEE transactions on Nanotechnology, Ed. IEEE, Vol. , DOI: 10.1109/TNANO.2020.3044017, décembre 2020
2 **Skaf A., Ezzadeen M., Benabdenbi M., Fesquet L.,** Clocked and event-driven redundant adjustable precision computing, Microelectronics Reliability, Ed. Elsevier, Vol. 111, pp. 113729, DOI: 10.1016/j.microrel.2020.113729, août 2020
3 **Anghel L., Bernasconi A., Ciriani V., Frontini L., Trucco G., Vatajelu I.,** Stuck-At Fault Mitigation of Emerging Technologies Based Switching Lattices, Journal of Electronic Testing: Theory and Applications, Ed. Springer , Vol. , pp. 313–326, DOI: 10.1007/s10836-020-05885-2, juin 2020
4 **Di Natale G., Bolchini C.,** Holding Conferences Online due to COVID-19: The DATE Experience, IEEE Design & Test, Ed. IEEE, Vol. 37, No. 3, pp. 116-118, DOI: 10.1109/MDAT.2020.2995140, juin 2020
5 **Fabero J.C., Mecha H., Franco F., Clemente J.A., Korkian G., Rey S., Cheymol B., Baylac M., Hubert G., Velazco R.,** Single Event Upsets Under 14-MeV Neutrons in a 28-nm SRAM-Based FPGA in Static Mode, IEEE Transactions on Nuclear Science, Ed. IEEE, Vol. 67, No. 7, pp. 1461-1469, DOI: 10.1109/TNS.2020.2977874, mars 2020

Invited conferences talks

1 **Regazzoni F., Bhasin S., Ali Pour A., Alshaer I., Aydin F., Aysu A., Beroulle V., Di Natale G., Franzon P., Hély D., Homma N., Ito A., Jap D., Kashyap P., Polian I., Potluri S., Ueno R., Vatajelu I., Yli-Mäyry V.,** Machine Learning and Hardware security: Challenges and Opportunities, Invited talk (Special Session), International Conference on Computer-Aided Design (ICCAD 2020), San Diego, UNITED STATES, 2 au 5 novembre 2020
2 **Pétrot F., Anghel L., Andrade Porras L.L.,** State of the art in hardware-accelerated neural networks, Invited Talk, Applied Machine Learning Days (AMLD 2020), Lausanne, SWITZERLAND, 27 au 29 janvier 2020

International conferences

1 **Garay Trindade M., Garibotti R.F., Ost L., Letiche M., Beaucour J., Possamai Bastos R.,** Assessment of Machine Learning Algorithms for Near-Sensor Computing Under Radiation Soft Errors, 16th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA 2020), Porto Alegre (Virtual edition), BRAZIL, 1 au 4 décembre 2020
2 **Garay Trindade M., Garibotti R.F., Ost L., Letiche M., Beaucour J., Possamai Bastos R.,** Assessment of Machine Learning Algorithms for Near-Sensor Computing Under Radiation Soft Errors, IEEE International conference on electronics, circuits & systems (ICECS 2020), Glasgow, SCOTLAND, UNITED KINGDOM, 23 au 25 novembre 2020
3 **Roux J., Beroulle V., Morin-Allory K., Leveugle R., Bossuet L., Cezilly F., Berthoz F., Genevrier G., Cerisier F.,** High Level Fault Injection Method for Evaluating Critical System Parameter Ranges, 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2020), pp. 1-4, Glasgow, UNITED KINGDOM, DOI: 10.1109/ICECS49266.2020.9294821, 23 au 25 novembre 2020
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