Reliable Mixed-signal Systems (RMS)

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Research Activities

Since its creation in 2002, the RMS group has addressed the integrated design, test and control of analog/mixed-signal/RF circuits and systems.

Design-for-test of AMS/RF circuits and systems

Testing the AMS-RF functions in a complex integrated system represents nowadays the largest fraction of the test cost. Therefore, simplifying the test of AMS-RF circuits is an area of innovation that may have a significant impact for the IC industry. In this line, Design-for-Test (DfT) solutions are aimed at reducing test cost and complexity by taking into consideration the testability of the circuit at the design stage. Our research in this area has focused on the development of AMS-RF state-of-the-art on-chip test instruments for Built-In Self-Test (BIST) applications and dedicated DfT techniques for reducing test time, complexity and cost. This research has been supported by EUREKA-PENTA European project HADES, and ECSEL European project TARANTO. The major results are described next.

Test solutions for the static linearity test of ADCs. Accurate static linearity test of high-resolution ADCs is one of the most challenging and time-consuming tasks in the production test of a mixed-signal system. Our group has developed two complementary strategies for reducing the cost of static test and relaxing its stringent requirements. Firstly, we have developed reduced-code static linearity test algorithms for pipeline and SAR ADCs. These test algorithms take advantage of the repetitive architecture and/or operation of certain ADC topologies for inferring the complete static linearity characteristics of an ADC from the measurement of a reduced subset of its output codes. Compared to standard histogram testing, we have demonstrated test time reductions in the order of 90% SAR ADCs [RI22], with accuracy better than one LSB. Secondly, we have developed a high-linearity on-chip step-wise ramp stimulus generator for enabling static linearity BIST applications. Our proposed solution is based on a discrete-time integrator whose input stage has been modified to produce a very small gain. A prototype has been designed in ST 65nm CMOS technology. Experimental results from 15 fabricated samples show an average static ENOB of 14.5 bits in a ±2 V differential output range [RI21], well ahead the state-of-the-art. Moreover, the proposed generator can be used for moving reduced-code techniques to a BIST scheme.

Embedded test instruments for the dynamic test of high-speed ADCs. One of the main key points to enable mixed-signal BIST solutions is the development of accurate on-chip analog signal generators that can provide appropriate test stimuli and replace costly external signal generators in standard analog and mixed-signal functional test protocols. In this line, the on-chip generation of sinusoidal stimuli is an unavoidable first step for moving many standard functional tests to a full-BIST solution. In the evaluated period, we have developed novel calibrated harmonic cancellation algorithms that can be employed for designing efficient on-chip sinusoidal signal generators with a high spectral quality using mostly-digital resources. A proof-of-concept demonstrator of the proposed sinusoidal signal generator has been designed in ST 28nm FDSOI technology. Experimental results from fabricated samples show a 10 dB THD and SFDR improvement with respect to the uncalibrated generator, for an output frequency range from 1.7 MHz to 333 MHz [CI43].

Control and optimization of performances for AMS/RF circuits

Our research in this domain has been partially funded by means of a collaboration with the University of Yaoundé, Cameroon, as part of the CETIC project (African Centre of Excellence in Information and Communication Technologies) funded by the World Bank.

Self-Healing of Image Sensors. We have developed a set of methods for monitoring and improving image quality based on the detection and correction of defective pixels, by concealing defective pixels present in the image sensors or introduced during transmission or decoding (VTS'19). The proposed error detection and correction process is based on scanning the image file, and isolating outlier pixel values and correcting them with a local median filtering that does not disturb healthy pixels. The results we are obtaining on the detection and correction of defective pixels now allow us to push the investigations further towards the diagnosis of image sensors, with the aim of identifying the sources of the defects detected and monitoring the ageing of these sensors.

Scheduling control for lifetime optimization in WSN. Limited energy autonomy is a significant barrier to the low-cost deployment of Wireless Sensor Nodes (WSN) technologies. As part of our collaboration with the University of Yaoundé within the CETIC research program, we have addressed the Maximum Lifetime Coverage Problem (MLCP) that aims at controlling a sleep/active schedule for sensors nodes in order to maximize the time span when all the targets are continuously covered by the network. Contrary to previous work that assumed that energy consumed in sleep mode is negligible, a non-zero sleeping energy of sensor nodes is considered in our proposal. The consideration of non-zero energy consumption of sensor nodes in sleep mode is more realistic but significantly increases the complexity of the problem. We address this question by proposing a greedy algorithm that gives priority to sensors with lowest energy, and uses a blacklist to limit the number of sensors covering critical targets. Simulations show that this algorithm outperforms the previously published solutions. Another contribution of this work is a formal framework, based on graph automorphisms and linear algebra, for ring connected networks that generalize a well-known tricky example of the literature. We have proposed for regular arrays, an analytical approach which shows that, for any optimal solution, all sensors' remaining energies are zero. This theoretical approach sheds new light on ring connected arrays of odd size that are known to be rather tricky when non-disjoint cover sets are considered [T12 – Thesis of D. Tchuani].

Design of AMS/RF circuits and systems

The development of advanced AMS/RF circuits has been carried out through the joint research laboratory PYXCAD created in 2018 with the start-up company XDIGIT (currently running for the period 2018-2020) and a doctoral contract (2016-2019).

High performance ADCs for industrial imaging applications. The goal of the joint laboratory PYXCAD is the development of very high performance analog/mixed-signal measurement interfaces and software solutions for the treatment of the generated data. The work in 2019 has continued with the optimized layout of switched-capacitor ADCs for image sensors, using customized capacitances rather than the usual pcells that are made available with the technological design kits. In parallel, an advanced characterization test bench has been developed, using an Applicos test equipment that is very flexible for testing converters.

Design of embedded sensors and tuning knobs for yield enhancement of RF and mmW circuits. In collaboration with the Laboratory RFICLab, we have designed tuning knobs based on variable decoupling cells which have been implemented for calibration purposes of a 60 GHz Power Amplifier designed in STMicroelectronics 55nm CMOS technology. A one-shot calibration procedure reads the output of embedded process monitors and then relies on a machine learning regression model to find the best configuration of the tuning knobs for optimizing the performance of the circuit and enhance fabrication yield [CI53].

Machine learning-based modeling of AMF/RF circuits and systems

This research has been partially supported by CNRS PICS project IndieTEST (PICS07703).

Feature selection and feature design in the context of machine learning-based test. The definition of the input space of signatures is one of the key aspects that limit the adoption of machine learning-based test as a methodology. Together with the Instituto de Microelectrónica de Sevilla (IMSE-CNM, CSIC-Universidad de Sevilla), Spain, we have explored efficient methodologies for feature selection and feature design in the context of machine learning-based test applications of analog, mixed-signal, and RF integrated circuits [CI48]. Feature selection techniques considered include filters based on the Brownian distance correlation metric, wrapper algorithms for feature selection, and we proposed a novel correlation-guided wrapper. Finally, we devised a novel algorithm to automate the design of features and assist in the physical implementation of machine learning-based test. Our proposal was demonstrated on a 60 GHz PA case study [CI53] showing the potential of indirect test techniques in the emerging field of mmW built-in test.

Estimation of analog/RF parametric test metrics. Analog/RF built-in test (BIT) techniques are essential for reducing the very high costs of specification-based tests and for high-safety applications. The adoption of a BIT technique needs to be decided at the design stage, and this can be facilitated by estimating the test quality in terms of errors such as Test Escapes (TE) and Yield Loss (YL). Test quality estimation at the design stage has been traditionally very difficult for analog/RF circuits due to the lack of fault models that properly cover parametric faulty behavior. The RMS group has developed several statistical modeling techniques for the estimation of these metrics with part-per-million (ppm) precision without the need to consider parametric fault models. The most recent work has considered a fast statistical simulation exploiting machine-learning techniques, providing the data required for using rigorous Extreme Value Theory (EVT) models for test metrics estimation. This modeling technique has demonstrated ppm precision for the evaluation of a RF LNA BIT technique using a large date set of 1 million simulated circuits [RI20].

Machine learning based image quality assessment. We proposed a set of new objective methods for Image Quality Assessment (IQA) based on machine learning. In order to cover the variety of applications for which knowledge of image quality is required, we have proposed two classes of objective perception quality assessment methods depending on whether or not a reference image is available. Objective image quality is computed by pooling several image features extracted from different concepts: the natural scene statistic in spatial domain, the gradient magnitude, the Laplacian of Gaussian, as well as the spectral and spatial entropies. The extracted features are used as the entries of regression machine learning techniques, to construct the models that can be used to estimate the quality of an image. The experimental results demonstrate that the proposed models produce the best image quality prediction, compared to the other state-of-art objective no-reference image quality assessment models. We proposed an implementation of the proposed models on an FPGA platform. The implementation has been tested using Xilinx Virtex 7 FPGA board, implemented with C/C++ code on Xilinx Vivado HLS [CI45 - VTS'2019].

Highlights

- Silicon demonstration of the indirect test of mmW circuits, with two invited talks in this domain (SMACD'19).
- Demonstration of new machine-learning based algorithms and techniques for image quality enhancement for video and CMOS imager applications.
- New research project in collaboration with STMicroelectronics on embedded integrated jitter measurement and analog test signal generation, in the frame of the Nano2022 program.

Indicators

Scientific production	2019
International journals	4
International conferences	11
Books & Edited Books	1
National conferences	2
Other communications	1
PhD thesis	3

Scientific recognition	2019
Invited conferences	3
Conference/workshop Committees	12
Journal Edition Committees	2

Contracts 2019		
ANR	1	Falcon (2017-2019)
ANRT	3	STMicroelectronics
Collectivités territoriales	1	Messi (2019-2022)
EPST	2	Conception analogique (2019-2020) / PICS – Indie TEST (2017-2019)
EUREKA	1	Hades (2017-2020)
Industrie	1	Pyxcad 2019 (2019)