Circuits, Devices and System Integration (CDSI)

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Research Activities

Event-driven strategies are fashionable techniques because they offer design flexibility in many field of applications. Indeed, event-driven circuits are known for a long time but they spark interest in really recent challenges such as reliable, safe and secure circuits, low-EM emissions or ultra-low power. Intel announced last year a 130.000 neuron chip based on an asynchronous Spiking Neural Network (SNN) and, very recently, aiCTX presents a 1 million neuron chip based on a Dynamic Neurormorphic Asynchronous Processor (DYNAP). These examples illustrate the today interest in event-driven technology. This latter is studied since 20 years at TIMA and has been applied to several domains. Event-driven strategies are deployed in the CDSI team through different activities covering ultra-low-power circuits, safe and secure circuits, low-EM circuits, reliable, advanced sampling techniques for near-sensor computing.

Nowadays the More than Moore approach is spread in a huge number of devices and systems. In this framework the CDSI team is involved in the design and fabrication of low power smart transducers for IoT and MedTech applications. To reach this target these transducers combines new electroactive materials, ultra-low power read-out circuits and near sensor processing (computing). For instance, the design of low power CMOS vision sensors is explored combining conventional pixels, asynchronous read-out circuit and near sensor processing. Another strong insight concerns the development and integration of new piezoelectric materials for MEMS devices used in acoustics applications, in energy harvesting generators for autonomous systems or for haptic rendering devices.

Probabilistic Machines for Low level Sensor Interpretation

The development of modern computers is principally devoted to increasing performance and decreasing size and energy consumption, without any modification of the principles of computation. In particular, all the components must always perform deterministic and exact operations on sets of binary signals. These constraints impede further progress in terms of speed, miniaturization and power consumption. In cooperation with LIG, Grenoble, we investigated a radically different approach using stochastic bit streams to perform calculation. Our goal has been to show that stochastic architectures can outperform standard computer when solving complex inference problems such as source localization [T4 – Thesis of R. Frisch] and separation both in terms of execution speed and power consumption. The project has been supported by the Persyval Labex and implies LIG, Gipsa and IF laboratories. One of the project results is the creation of the HawAI startup company.

Asynchronous Low-Power Systems (ALPS)

This work targets very ambitious objectives because we expect developing several design tools in a unique framework called ALPS. ALPS stands for Asynchronous Low-Power Systems but integrates different tools able to provide a wide range of asynchronous solutions to designers. On one hand, designers face today problems in implementing circuits while the specifications cover not only the design functionalities but also requirements such as power, security, EMC or safety. On the other hand, the asynchronous strategy based on synchronizing circuits thanks to local handshakes offers a wide range of solutions for targeting at design time the non-functional circuit requirements. All these solutions share the asynchronous and event-based approach but also models and theory. Therefore, a complete framework has been setup in order to integrate several tools that could be connected together. Notice that these tools are complementary to those included in the commercial design flows.

Smart non-uniform sampling schemes

Reducing the power consumption in integrated systems has been the starting point. Indeed, the theoretical and practical researches, pushed in our team since 2000, has highlighted that the Nyquist-Shannon theory tends to capture useless samples. Therefore, Level-crossing sampling schemes (LCSS) have been devised and an Asynchronous Analog-to-Digital Converter (A-ADC) has been designed, fabricated and tested.

Our sampling techniques produce fewer samples than with the traditional Nyquist-Shannon techniques but the samples are not anymore captured thanks to a sampling clock! The consequence of these non-uniform sampling schemes is the non-regular arrival of the data. Nevertheless, this is absolutely not an issue if considering event-driven (asynchronous) circuits. Indeed, thanks to this parsimonious sampling, fewer data are produced and, thus lower activity and power consumption.

ALPS framework

The ALPS framework targets the automated synthesis of integrated systems based on a LCSS analog-to-digital conversion and an event-driven circuit able to process the data captured by the A-ADC. The framework offers the opportunity to evaluate the sampling scheme and the appropriate processing thanks to the SPASS library written in Matlab. Once the sampling scheme and the associate signal processing are fixed, the tools ALPS-HLS and ALPS-ADCGen respectively generate a netlist of the processing unit and another one for the A-ADC. As the designs are specified at an algorithmic level, an automated High-Level Synthesis (HLS, adapted version of AUGH from SLS team) has been targeted.

Shaping EM emissions

Electromagnetic Compatibility (EMC) specifications have always been a hard task for integrated circuit designers. Indeed, the unwanted generation, propagation and reception of electromagnetic energy in integrated circuits may cause unwanted effects such as electromagnetic interference (EMI) or, even worst, physical damage. This work only targets the mitigation of the EM field emitted by a circuit aggressor and tends to respond to this issue for the first time by a design strategy, which could easily be automated. With such an approach, fitting within a spectral mask should become a specific step in the integrated circuit design flow. This is ensured by a specific tool ALPS-EMShaper producing event-based asynchronous micropipeline circuits. Once the event-driven circuit is designed, the method determines the switching instants of the logic thanks to specific delays accordingly chosen with the specified spectral mask [RI10 - JLPEA'2019]. We obtained significant reductions of the electromagnetic spectral peaks with this strategy compared to the spectrum of its synchronous counterpart. A test chip in 40 nm from ST Microelectronics has been designed, fabricated and tested for validating the approach. This works have been done with academic collaborations, the GIPSA and LJK laboratories in Grenoble, and industrial partners such as STMicroelectronics and the Swatch Group in Switzerland.

Low-Power Event-Driven Image Sensors

As the power has become a leitmotiv for all the embedded applications including systems with embedded cameras such as smartphones, the power efficiency of the CMOS image sensors has been enhanced during the last two decades. Nevertheless, the standard reading architecture of image sensors requires an analog to digital converter (ADC), which is currently the most consuming part. Therefore, many studies have been provided in order to reduce the impact of the analog-to-digital converter. Furthermore, the classical reading method of the image sensor consists in reading the entire image for each frame, which induces extra power consumption and useless data. Therefore, the asynchronous event-based image sensors are becoming promising alternatives. The CDSI team proposed an event-driven sensor performing spatial redundancies suppression and thus a data flow reduction in still image and video streaming by only reading pixels with relevant information. In addition, we removed the analog-to-digital converter, and used instead a time-to-digital conversion to encode the pixel information. In order to demonstrate the potential of our approach, two test chips have been designed. The first one is a test chip designed fabricated and tested for characterizing the pixel behavior and comparing two pixel architectures. The second, a fully operational event-based image sensor has been taped-out in February 2019.

This image sensor principle is able to cover different kind of usages. Indeed, the architecture seems to be useful for Time-of-Flight (ToF) measurements and providing 3D vision. For such a purpose, the approach could be coupled to SPAD (Single Photon Avalanche Diodes) or low-noise photodiodes. These kinds of techniques are of interest for 3D vision but also for dust, smoke and fog vision. Moreover, the potentials of this image sensor architecture is large. It could be used as a low-power wake-up imager, High Dynamic Range vision (night and day), low-data rate imager or as high speed image sensor. This work has been supported by the Persyval LabEx and made in cooperation with iCube (Strasbourg), EPFL (Switzerland) and CEA-LETI (Grenoble).

Near Sensor Computing

Several imaging systems have been under investigations in order to develop advanced imaging systems such as adaptive imaging in nuclear medical imaging, video stitching, hyperspectral camera or near sensor deep learning. For instance, video stitching aims at gathering images from several video sources to build a larger image. This implies to implement on an FPGA algorithms performing non-linear mapping from several video sources to a final geometric space. This is typically used in surgery for per-operatory laparoscopy. Another example is the design of Convolutional Neural Network (CNN) targeting a CNN compression, which allows to precisely controlling the trade-off between detection quality, memory occupancy and computing power. All these studies are made in cooperation with Partners including STMicroelectronics, CEA, Gipsa and TIMC.

Event-driven circuit design techniques

Event-driven circuits appear today as an attractive solution for designing robust and low-power chips dedicated to smart sensing and IoT platforms. However, a massive adoption of this technology by the industry requires industrial-grade tools for the design flow. In order to facilitate its dissemination, we targeted asynchronous bundled-data circuits. Indeed, the gap between asynchronous bundled-data and synchronous circuits is sufficiently tight to exploit the existing commercial tools without impacting the design flow and time-to-market. As such an approach requires formal models, formal verification has also been used for checking liveliness and detecting deadlocks. Therefore, practical methods have been developed for specifying, verifying, optimizing and physically implementing asynchronous bundle-data circuits. The results show that asynchronous bundle-data circuits provide lower power consumption than its gated clock counterpart. Finally, this work has been done with several industrial partners among then STMicroelectronics, Dolphin Design, Starchip, IC'Alps, Swatch Group and academic partners IM2NP and EPFL.

Asynchronous Circuits for FDSOI technology

Low-voltage operation is an efficient and well-known strategy to save power at the price of a reduced speed. The Fully Depleted Silicon on Insulator (FDSOI) technology allows mitigating this speed loss thanks to body biasing. In addition, asynchronous circuits use communication protocols which indicate circuit activity. This is used to locally activate/deactivate body biasing when blocks are unused. The research works target the sizing of an optimal granularity for biasing asynchronous circuits in 28-nm FDSOI technology when operating in low-voltage mode. In order to bias small blocks, an analog standard cell - controlled by the asynchronous handshaking signals and dedicated to bias a small area - has been designed. Level shifter architectures were studied for this purpose. A complete asynchronous QDI design flow, dedicated to FDSOI technology, has been proposed and evaluated through this study. The FD-SOI 28-nm standard-cell design flow was developed with Synopsys, Cadence, Mentor and Tiempo CAD tools. This work has been successful thanks to a tight cooperation between STMicroelectronics, Tiempo and TIMA during the Things2Do ENIAC project.

Reliable and trusted systems

Among the design strategies for detecting transient faults caused by radiation or intentional sources, Bulk Built-In Current Sensors (BBICS) offer a promising solution that is perfectly suitable for system design flows based on CMOS standard cells of commercial libraries. BBICS combine the high detection efficiency of costly fault-tolerance schemes (e.g. duplication) with low area and power overheads. Several BBICS architectures have recently been proposed by our team to monitor transient faults induced by radiation or malicious sources. The technique has also been employed for tracking fabrication defects and hardware Trojans. This work has been made in cooperation with EMSE, Gardanne and LIRMM Montpellier.

Time-to-Digital Converters

Accurate time measurements between two events are required in many fields such as high-energy physics, time-of-flight measurement, satellite positioning and instrumentation. A new compact TDC architecture based on STR with sub-gate delay resolution has been devised. The STR allows generating evenly-spaced transitions that can be made arbitrarily close by simply increasing the number of stages. Thanks to these unique STR features, our TDC can virtually achieve a time resolution as fine as desired. The concept has been implemented and tested on an FPGA and on an ASIC in AMS CMOS 350. The work is supported by SCUSI contract from AuRA Région and is made in cooperation with INPT, Morocco.

Micro Power Generators for Autonomous Microsystems

Energy harvesting has been the subject of intense research over the last decades. Various transduction principles have been presented as potential ways of scavenging the ambient energy and transforming it into usable electrical energy. Among these principles, the piezoelectric transduction is probably the most studied one. Most of the approaches that we have studied so far were based on resonant piezoelectric devices with working frequencies above 200 Hz. However, our current work is focused on the development of energy harvesters designed to scavenge energy from real vibrational sources like the heartbeat. Such a design must consider a wideband spectral content of an acceleration source centered in a frequency band not exceeding 30 Hz. The dimensional aspects as the geometry and the volume as well as the energy requirements are critical constraints and play important role in the design strategy

Design and Technologies for Integrated Micro and Nano Systems

The design of new smart Micro and Nano Systems can be achieved in different way. For instance, we have used extensively a CMOS (AMS 0.35µm) compatible process for the design of acoustic transducers for airborne signals. The ultimate goal was the monolithic integration of a device working both as a source and a sensor with electronics, thus facilitating signal routing, suppressing parasitic effects, and improving the signal-to-noise ratio. More recently in the collaboration with the CityU, we presented an aluminum nitride (AlN) CMOS-compatible piezoelectric micromachined ultrasonic transducer (PMUT) capable of an extended detection range of up to 140 cm for touchless sensing applications. AlN-PMUTs have been of increasing interest for range-finding applications over PZT and ZnO films owing to their CMOS-compatibility and maturity of deposition techniques, but are limited to a detection range below 1 m. This technology was also used in collaboration with Univ. of Brescia for the design of new microfluidic components.

In the framework of the project NEED (Cross Disciplinary Project – UGA – Grenoble) we have started the study of thick films of hafnium zirconium oxide HZO. This oxide is a sustainable material and presents promising piezoelectric, pyroelectric, ferroelectric and electrocaloric properties. This material can pave the route of new piezoMEMS devices.

Finally, in the framework of the FMNT (Federation des Micro Nano Technologies), we are developing in collaboration with G2ELab and LMGP laboratories new Piezoelectret polymers using a PDMS matrix. This approach allows us to tailor the electromechanical properties (Young modulus, and piezoelectric coefficients) of stretchable and conformal thick films for soft autonomous sensors embedded in wearable devices.

Highlights

- Bayesian asynchronous computers (LIG, StartUp HawAI.Tech)

Indicators

Scientific production	2019
International journals	7
International conferences	24
Books & Edited Books	1
Softwares	1
PhD thesis	8

Scientific recognition	2019
Prizes and distinctions	1
Invited conferences	4
Conference/workshop Committees	13

Contracts 2019		
ANRT	4	STMicroelectronics (3) / StarChip (1)
Carnot	1	EBIS (2019-2020)
CEC National	2	Ocean 12 (2018-2021) / Things2Do (2014-2019)
EPST	1	Microbayes (2016-2019)
Industrie	2	Icalps (2018-2020) / Thesis of Grégoire GIMENEZ (2016-2020)
International	1	Brafisat (2019-2022)
Ministères-FUI	2	Imspoc-UV (2018-2021) / LISA (2014-2019)
Région	3	Gresam (2019-2020) / Fair (2018-2023) / Convertisseur temps numérique (2017-2020)