RMS team (Reliable Mixed-signal Circuits and Systems)

Themes

Mixed-signal/RF integrated devices
Test and control techniques
Design-for-test
Diagnosis
Embedded control
Behavioral and statistical modeling methods
Design of mmW integrated circuits
CAD tools for test and control

Expertise

Scientific
Test and diagnosis for mixed-signal/RF integrated devices, design-for-test, behavioral and statistical modeling, embedded control

Fields of expertise
Microelectronics, statistical modelling, control.

Know-how
Test metrics estimation, machine-learning-based test, non-intrusive test and control, diagnosis, mixed-signal/RF design-for-test

Industrial transfer
Techniques of integrated test for analog-to-digital signal converters, CAD software for test, embedded sensors diagnostic technique

Research keywords

Design-for-test, built-in self-test, design-for-manufacturing, calibration, density estimation, machine-learning, embedded control, mm-Wave RF-IC

Contact

Emmanuel SIMEU
UGA Associate Professor
(+33) 4 76 57 47 20
Emmanuel.Simeu@univ-grenoble-alpes.fr

ADC BIST for dynamic test

Members: H. Malloug, M.J. Barragán, S. Mir, E. Simeu

Cooperation: STMicroelectronics

Contracts: NANO2017

1. Introduction

In this work, we explore the use of harmonic cancellation strategies for the practical implementation of on-chip sinusoidal signal generators. Harmonic cancellation is a classical spectral manipulation technique based on combining phase-shifted and weighted versions of a periodic signal to provide a periodic signal in which a set of low-order harmonic components is cancelled. The proposed architecture, as shown in Fig.1, is based on a N-length circular shift-register that generates digital square-waves phase-shifted by $\frac{2\pi}{N}$. Subsequently, the set of selected phase-shifted square-waves from the shift-register are conveniently scaled with the help of current-steering sources and summed to generate a sinusoidal output.

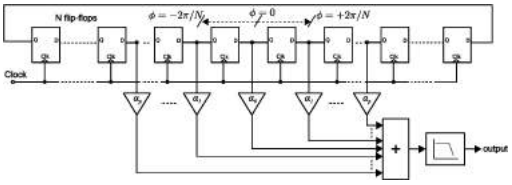

Figure 1: Conceptual block diagram of the proposed sinusoidal signal generator

Classical harmonic cancellation techniques [1] consist of combining “p” pairs of a square-wave phase-shifted and scaled with coefficients according to (1) to cancel all odd-order harmonic components lower than the 2(2p+1)-th order.

$$\begin{cases} \phi_i = i\frac{2\pi}{N} & 1 \le i \le p \\ \alpha_i = cos(i\frac{2\pi}{N}) & 1 \le i \le p \end{cases} \quad (1)$$

However, the effectiveness of the harmonic cancellation is very sensitive to mismatch and the scale weights provided by (1) are irritational which make its implementation challenging and requires careful layout of the weighting elements.

In this line, our goal is to explore and propose different solutions to the harmonic cancellation design equation that simplify the practical implementation of the scale weights.

2. Harmonic cancellation strategy with integer scale-weight ratios

Let us consider a generic periodic signal x(t) expressed as a Fourier series expansion:

$$x(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 t + \varphi_k) \quad (2)$$

Let us consider signal y1(t) defined as:

$$y_1(t) = 2x(t) + x(t+\Delta t_1) + x(t-\Delta t_1) = \sum_{k=1}^{\infty} 2A_k\,[1+\cos(k\phi_1)]\cos(k\omega_0 t + \varphi_k) \quad (3)$$

In this configuration, it is easy to demonstrate that the third-harmonic component of the original signal x(t) can be easily cancelled by setting $\Phi 1 = \pi/3$. Let us iterate the same process and define now signal y2(t) as

$$y_2(t) = 2y_1(t) + y_1(t+\Delta t_2) + y_1(t-\Delta t_2) = \sum_{k=1}^{\infty} 2^2 A_k\,[1+\cos(k\phi_1)][1+\cos(k\phi_2)]\cos(k\omega_0 t + \varphi_k) \quad (4)$$

As it can be observed, by setting $\Phi 1 = \frac{\pi}{3}$ and $\Phi 2 = \frac{\pi}{5}$ we can cancel the 3rd and 5th order harmonic components of the original signal x(t). This solution employs a combination of 9 square-waves sq1(t) to sq9(t), as it is schematically shown in Fig. 2. These 9 square-waves are distributed into three sets of square-waves, each set contains three square-waves with a relative phase-shift by $\frac{\pi}{3}$, and the sets are phase-shifted by $\frac{\pi}{5}$.

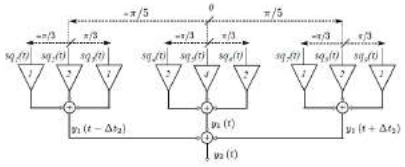

Figure 2: Harmonic cancellation strategy using integer scale weight ratios to cancel the 3rd and 5th harmonics

Based on the generator architecture shown in Fig.1, the required phase-shifts can be easily achieved using a shift-register with 30 flip-flops. In this case, scale factors ratios are integer and powers of 2 which simplifies matching of the different signal branches in a practical implementation.

3. Harmonic cancellation with unitary scale weight-ratios using odd number of signals

A similar strategy can be devised to achieve harmonic cancellation conditions using unitary weight ratios for all the signal phases. Let us consider signal y1(t) defined as:

$$y_1(t) = x(t) + x(t+\Delta t_1) + x(t-\Delta t_1) = \sum_{k=1}^{\infty} A_k\,[1+2\cos(k\phi_1)]\cos(k\omega_0 t + \varphi_k) \quad (5)$$

For instance, the third-order harmonic component can be cancelled by setting $\Phi 1 = \frac{2\pi}{9}$. Similarly to the previous case, the process can be iterated. Let us define signal y2(t) as:

$$y_2(t) = y_1(t) + y_1(t+\Delta t_2) + y_1(t-\Delta t_2)$$
$$= \sum_{k=1}^{\infty} A_k\,[1+2\cos(k\phi_1)][1+2\cos(k\phi_2)]\cos(k\omega_0 t+\varphi_k) \quad (6)$$

Again, the 3rd and 5th order harmonic components can be cancelled by setting $\Phi 1 = \frac{2\pi}{9}$ and $\Phi 2 = \frac{2\pi}{15}$.This harmonic cancellation strategy with unitary scale ratios can be easily implemented using 9 square-waves sq1(t) to sq9(t), as it is schematically shown in Fig.3.

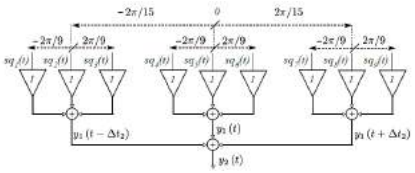

Figure 3: Harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel the 3rd and 5th harmonics

Based on the generator architecture shown in Fig.1, the required phase-shifts can be easily achieved using a shift-register with 90 flip-flops and unitary scale weights which relax the implementation of the weighting stage.

4. Harmonic cancellation with unitary scale weight-ratios using even number of signals

In order to further reduce the complexity of the previous generation strategy, we propose a similar harmonic cancellation strategy using unitary weight ratios with a reduced number of square-waves. Let us consider signal y1(t) defined as:

$$y_1(t) = x(t+\Delta t_1) + x(t-\Delta t_1)$$
$$= \sum_{k=1}^{\infty} 2A_k\cos(k\phi_1)\cos(k\omega_0 t+\varphi_k) \quad (7)$$

In this configuration, the 3rd harmonic component can be cancelled by setting $\Phi 1 = \frac{\pi}{6}$. Let us iterate the process and define y2(t) as :

$$y_2(t) = y_1(t+\Delta t_2) + y_1(t-\Delta t_2)$$
$$= \sum_{k=1}^{\infty} 2^2 A_k\cos(k\phi_1)\cos(k\phi_2)\cos(k\omega_0 t+\varphi_k) \quad (8)$$

In the resultant signal y2(t), 3rd and 5th harmonic components can be cancelled by carefully selecting variables $\Phi 1 = \frac{\pi}{6}$ and $\Phi 2 = \frac{\pi}{10}$. This harmonic cancellation strategy can be implemented by combining four square-waves sq1(t) to sq4(t), as schematically shown in Fig. 4.

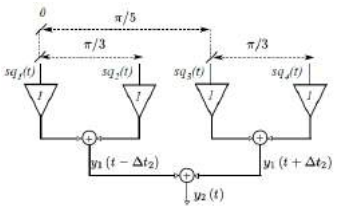

Figure 4: Harmonic cancellation strategy using integer scale weight ratios and even number of signals to cancel t3rd and 5th harmonics

Based on the generator architecture shown in Fig.1, the required phase-shifts can be easily achieved using a shift-register with 30 flip-flops and unitary scale weight which relax the implementation of the weighting stage.

5. Simulation results

In order to demonstrate the feasibility of the proposed harmonic cancellation strategies, we have developed realistic behavioral models for the irrational harmonic cancellation with 5-phase generator presented [1], and for the novel harmonic cancellation strategies described previously in Fig. 2, Fig. 3 and Fig. 4. The goal of these simulations is to analyze the effectiveness of the cancellation in the presence of fabrication imperfections that may introduce deviations in the scale weight ratios required for the considered harmonic cancellation techniques. A set of statistical behavioral simulations were performed in MATLAB considering mismatch between the scale weights. Two different operation scenarios were considered for all the proposed generators: a high-frequency scenario with clock frequencies fclk = 2 GHz, and a moderate-frequency scenario with fclk = 200 MHz. Notice that the frequency of the output sinusoidal signal for each generator will be fwave = fclk/N.

Fig. 5 shows boxplots of the THD obtained for the four considered harmonic cancellation strategies, for the two different operation frequencies considered, as a function of the maximum scale-weight mismatch in the summing network, obtained by behavioral level statistical simulations. A total of 100 generator instances were randomly generated for each combination of operation conditions. Scale-weight mismatch and delay errors were modeled as random variables. In this set of simulations, the time delay mismatch is set to a maximum of 0.1 ps for all simulations. As it can be observed, the impact of scale weight mismatch is practically identical for the four considered harmonic cancellation strategies which implies that implementation complexity will be considered as the most important criteria to select the most adequate generation strategy.

Table 1 summarizes the main characteristics of the four considered cancellation techniques and Fig. 6 further clarifies this trade-off. This figure represents the order of the first non-canceled harmonic as a function of the number of necessary phase-shifted square-waves for each of the presented sinusoidal signal generation techniques. Additionally, we indicate, for each data point, the set of different weights required for implementing each generator (for the generators with non-unitary weights).

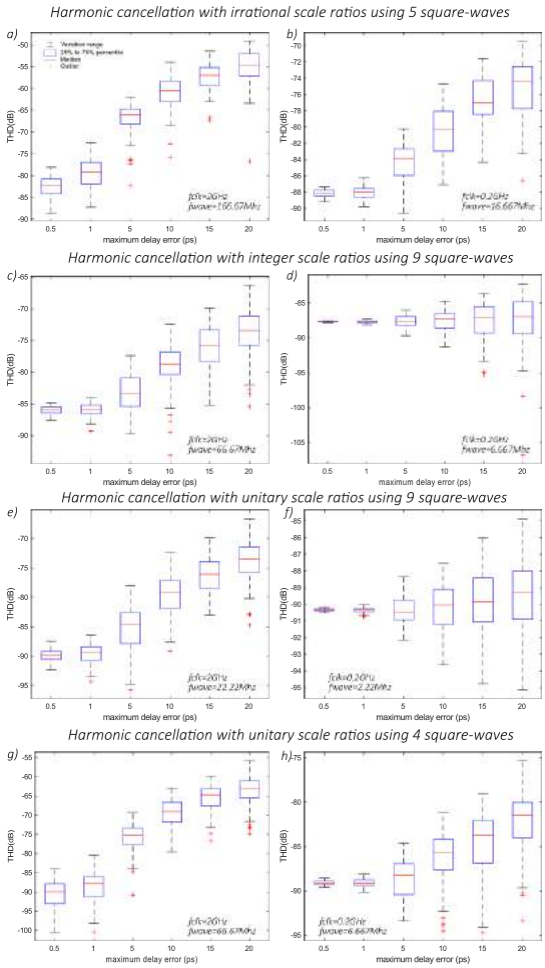

Figure 5: THD of the generated sinusoidal signal as function of the maximum scale weight mismatch

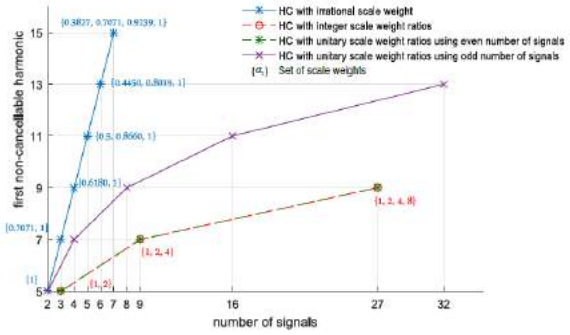

Figure 6: Comparison of the proposed harmonic cancellation strategies

Type of Scale ratios	Irrational	Integer	Unirtary	
Number of square-waves	5	9	9	4
length of flip-flops	12	30	90	30
Frequency of the generated sine-wave	$f_{clk}/12$	$f_{clk}/30$	$f_{clk}/90$	$f_{clk}/30$
Relative phase-shift	$\pi/6$	$\pi/15$	$\pi/45$	$\pi/15$
Harmonic components to be cancelled	$3^{rd}, 5^{th}, 7^{th}, 9^{th}$	$3^{rd}, 5^{th}$	$3^{rd}, 5^{th}$	$3^{rd}, 5^{th}$
Design complexity of the weighting stage	High	low	low	low

Table 1: Comparison of harmonic cancellation strategies

6. References

[1] H. Malloug, et al. Mostly-digital design of sinusoidal signal generators for mixed-signal BIST applications using harmonic cancellation," International Mixed-Signal Testing Workshop, 2016

Built-In Self-Test solutions for mmW integrated circuits

Members: F. Cilici, M.J. Barragán, S. Mir, E. Lauga-Larroze, S. Bourdel

Cooperation: IMEP-LaHC

1. Introduction

Testing RF subsystems embedded in complex Systems-on-Chip (SoCs) and Systems-in-Package (SiPs) represents a challenging task. It can be said that RF testing inherits the difficulties of analog testing, but adding also the problem of handling high-frequency signals. The direct test and diagnosis of an RF device are based on complex functional tests that apply a high-frequency stimulus to the Device Under Test (DUT) and observe its response to compute a performance metric. This usually requires the use of dedicated high-speed test equipment and the provision of an adequate test access. However, the increase in operation frequency and the fact that RF blocks are currently embedded within a complete integrated system, turn these requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals between the chip and the external tester.

The development of RF Built-In Self-Test (BIST) is a promising solution to overcome these issues. BIST strategies are aimed to move some of the tester functionality into the DUT itself, in such a way that the circuit becomes self-testable. Signal manipulations would remain internal, thus eliminating transport problems. However, the RF BIST road is not free of shortcomings either. Two key problems that any successful RF BIST should overcome are: (a) the high sensitivity of internal RF nodes to any added load during test; and (b) the internal generation of adequate RF test stimuli. Indeed, RF signal paths are extremely sensitive to parasitic loads. Tapping into an RF node during BIST operation to connect an embedded test instrument may have a huge impact on the functionality of the DUT, masking the actual performance of the device. In the same way, RF front-ends, and particularly the receiver sections, are usually tested at their operation frequency. BIST approaches can only be successful if we can devise strategies for simplifying (or avoid) the internal generation of RF test stimulus, since the cost of including RF test signal generators on-chip together with the DUT is usually prohibitive.

2. Research opportunities and proposed approaches

There is not a widely accepted solution yet for incorporating BIST into the building blocks of state-of-the-art integrated transceivers. This thesis is aimed at defining novel test solutions for mmW circuitry that:

- Minimize or eliminate added loads to the RF signal path. RF circuits, and specially mmW circuits, are extremely sensitive to loading effects.
- Simplify or avoid the generation of RF tones. Dedicated RF tone generators based on RF VCOs offer a great RF performance, but at the cost of design complexity and a considerable area and power overhead.
- Consider the co-design of BIST circuitry and DUT since the early design stages. Any built-in test instrument that taps into the RF signal path should be carefully co-designed to avoid performance degradation.
- Minimize the number of required measurements. A cost-driven optimization of the set of RF measurements to filter redundant and costly measurements is also a promising path for reducing RF test complexity and cost.

3. Initial stages

The design of a mmW Power Amplifier at 60 GHz in STMicroelectronics 55 nm BiCMOS technology has been envisaged. We have developed a methodological approach to the design of the PA. This exercise not only has provided as with an actual state-of-the-art case study, but it also has given us a valuable insight on mmW design that will guide our research in future stages.

4. Assisted design of non-intrusive indirect test

A 60 GHz class A one stage power amplifier has been designed in STMicroelectronics 55 nm BiCMOS technology. The chip dimensions are 300µm * 500µm. The performances of this circuit are not state of the art, though good enough for our purpose. As a matter of fact, this circuit was devised to be a proof of concept, for a new non-intrusive test methodology. The circuit has been sent for fabrication in November 2017.

Let us introduce the exact aim of this work. In this respect, let us consider a generic non-intrusive machine learning indirect test scenario in which we intend to regress a set of performances of a given DUT from a set of signatures measured from a set of non-intrusive process variation sensors. The problem we address in this work is: given the netlist of a particular DUT in a given technology and a set of target performances, how to systematize the proposal of the set of signatures and the design of the associated sensors.

The methodology that we propose is divided into two interrelated steps. The first step is aimed at unveiling the root causes of parametric performance variation in the simulation

environment. The second step is devised to find process variation sensors that are sensitive to the identified set of root causes.

Thus, the aforementioned PA is intended to be the DUT in this study.

Let us describe the two steps of the proposed methodology. The first one aims at unveiling the root causes of parametric performance variation. In this purpose, information provided by Monte Carlo (MC) models in the Process Design Kit are the key to understanding these root causes. Therefore, our methodology explores the space of MC parameters to find the minimum subset that explains the parametric performance variation of the PA.

Exploring this space can be seen as a feature selection problem in which we consider the MC parameters as candidate features to regress a given target performance using a machine learning regression model. Thus, we chose to adapt the Brownian distance correlation-directed search, previously presented by M. Barragán in one of his works. Regarding a given performance, this algorithm ranks the most relevant MC parameters. Then, for each specification of the DUT, we have a list of model parameters that explain its variation.

The second step is the assisted design of non-intrusive process variation sensors. As a matter of fact, MC process parameters are basically abstract mathematical entities. Nevertheless, since they are the link with the fabrication steps, there must be an underlying physical phenomenon which warrant their validity.

Thus, a set of sensors has been designed to translate MC parameters meaning in real measurements. Ideally, for each identified MC process parameter, there should be one signature (sensor + measurement) that correlates perfectly with it. Obviously, this is not the case, and yet, the decorrelation between the different signatures is good enough to ensure a good performance prediction. Figure 1 presents the predicted gain versus the actual gain of the amplifier. It is clear that the regression results are satisfying since there is very little difference between the two (0,08dB RMS error in the prediction for a standard deviation of 0,69dB for the actual gain).

We have presented a systematic methodology for generating a non-intrusive indirect test program for mm-wave circuits. The proposed strategy represents a promising step towards the fully automation of test generation for non-intrusive machine learning test. The proposed methodology is illustrated using a 60 GHz PA case study designed in STMicroelectronics 55 nm BiCMOS technology. We have shown that the presented assisted test design algorithm enables us to find the root causes of parametric performance degradation and guides the design of appropriate non-intrusive sensors and signatures for accurate performance prediction.

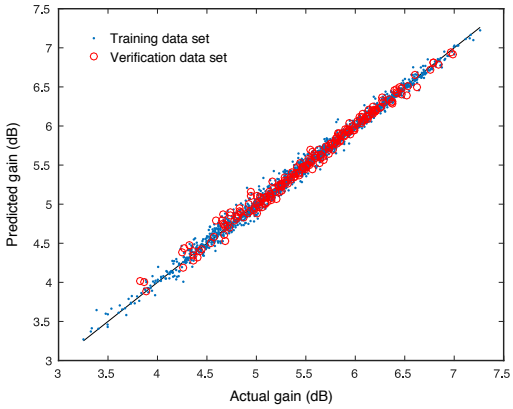

Figure 1 : Scatterplot of predicted versus actual gain of the PA using the generated indirect test program with 9 non-intrusive signatures

This work has received the best poster award in the national conference JNRDM 2018 [1]. An article has also been accepted in the international conference IEEE ETS 2018 [2].

The last step of this study will of course be silicon measurements to assert the validity and accuracy of the method.

5. Future work

A two stages power amplifier is currently being designed in order to provide state of the art performances alongside with non-intrusive test capabilities and maybe one shot calibration to balance the parametric process variations.

6. References

[1] F. Cilici, M. Barragan, E. Lauga-Larroze, S. Bourdel, S. Mir: "Conception en vue du test d'un amplificateur de puissance à 60 GHz", in *Journées Nationales du Réseau Doctoral en Micro-nanoélectronique 2017*

[2] F. Cilici, M. Barragan, S. Mir, E. Lauga-Larroze, S. Bourdel: "Assisted test design for non-intrusive machine learning indirect test of millimeter-wave circuits", Accepted for publication in *IEEE European Test Symposium 2018*

Design of mm-wave phase shifters in BiCMOS 55-nm technology with BIST capabilities

Members : M. Margalef-Rovira, M. J. Barragán, E. Pistono, P. Ferrari

Project: TARANTO ECSEL project

Cooperation: IMEP-LAHC

1. Introduction

Beam-forming techniques appear as promising solutions for the deployment of high-data-rate, low-power, point-to-point communications, such as 5G. These techniques rely on the usage of phased arrays. A phased array provides with a beam of energy that can be steered to point at different directions. They consist in an antenna array whose antennas are fed through phase shifters. The phase shifters are used to introduce a phase shift on the signal that is meant to be emitted in such a way that the existing phase difference between neighboring antennas will produce a steering of the beam. In this context, feeding each antenna with an accurately phase-shifted signal is a subject of great importance in the design of high-performance transceiver front-ends [1]. However, testing the provided phase shift is a cumbersome issue. Depending on the complexity of the phased array, it can greatly increase its production costs or even be impossible to perform its direct measurement due to the inaccessibility of the ports of the phase shifter.

For this reason, providing with test techniques that allow the extraction of the phase shifter performance is a subject of major interest in the design of phased arrays. In this context, the usage of a Built-In Self-Test (BIST) strategy that allows to avoid the usage of expensive dedicated measurement equipment, the Automated Test Equipment (ATE), appears as a good candidate to reduce costs and provide with measurements of the Device Under Test (DUT). BIST strategies pretend to move some of the functions performed by the ATE to on-chip circuitry. The BIST must output signals that can be read using low-cost instruments in order to effectively reduce the testing cost. Moreover, a successful BIST should introduce low area overhead and have a low impact on the DUT performance.

2. Research opportunities and proposed approaches

This thesis aims at using Oscillation-Based-Test (OBT) as the method to measure the provided phase shift. When performing OBT, the DUT is turned into an oscillator using additional circuitry. The features of the provided oscillations (e.g. frequency and amplitude) are then correlated with the actual performance of the device [2]. In our context, the usage of this technique is not free of shortcomings:

- The added circuitry has to provide with a low impact on the DUT performance and low area overhead.
- Additional on-chip circuitry has to be designed to output a signal that can be read with low cost equipment.
- The number of necessary measurements has to be minimized. Phase difference between neighboring DUTs has to be targeted instead of single DUT measurement.

3. Initial stages

We have designed a mm-Wave phase shifter at 60 GHz with circuitry to enhance BIST capabilities. The circuit has been designed in the BiCMOS 55-nm technology of STMicroelectronics. The designed phase shifter is based on a Reflection-Type Phase Shifter (RTPS) architecture. The RTPSs are composed of a 3-dB coupler and two reflective loads. In our case, the design of the 3-dB coupler has been done using a Coupled Slow-wave CoPlanar Waveguides topology and the reflective loads have been designed using varactors. Preliminary results have been sent for publication in [3].

In addition, other circuitry such as mm-Wave switches, transmission lines, couplers and characterization structures have been designed as elements that might be useful in future stages of the research in this topic.

4. References

[1] A. Hajimiri, H. Hashemi, A. Natarajan, X. Guan, A. Komijani: “Integrated Phased Array Systems in Silicon,” Proceedings of the IEEE, vol. 93, pp. 1637–1655, Sept 2005

[2] K. Arabi, B. Kaminska: “Oscillation-test strategy for analog and mixed-signal integrated circuits,” in Proceedings of 14th VLSI Test Symposium, pp. 476–482, Apr 1996

[3] M. Margalef-Rovira, M.J. Barragan, E. Sharma, P. Ferrari, E. Pistono, S. Bourdel: An Oscillation-Based Test technique for on-chip testing of mm-wave phase shifters, Accepted for publication in IEEE VLSI Test Symposium (VTS), 2018

Emerging Technology for RF and Millimeter-wave Circuits based on Carbon Nanotubes

Members: P.L. Doan, F. Podevin, P. Ferrari, E. Pistono

Cooperations: XLIM, CINTRA and III-V Lab

Contracts: TRICOT (ANR)

1. Introduction

This thesis is one part of a large ANR project called TRICOT, which has purpose on developing a new 3D integration technology dedicated to future wireless applications in mm-wave interconnects, circuits, nanopackaging and ultra-high-speed communications. A technology using carbon nanotubes (CNTs) is proposed to design functionalized interposer, which can operate up to 100 GHz, at least in a first step. This smart interposer will not only serve as a classical passive substrate for top to bottom connections, but also as a new artificial functionalized substrate, that can horizontally guide the EM waves with embedded and shielded critical passive circuits formed by empty waveguides or waveguides loaded by CNTs patterns. Such artificial substrate is based on CNT growth technology and Slow-Wave Substrate Integrated Waveguide (SW-SIW) concept.

For demonstrating the proof of concept of this new type of functionalized CNTs based interposer, we plan to design, fabricate, and characterize a 3D integrated E-band phased array using a Butler matrix embedded inside the interposer and addressing back-hauling for 5G mm-waves. A 2D Butler matrix will be considered to achieve the system-level demonstrator, an example of this concept is shown in figure 1.

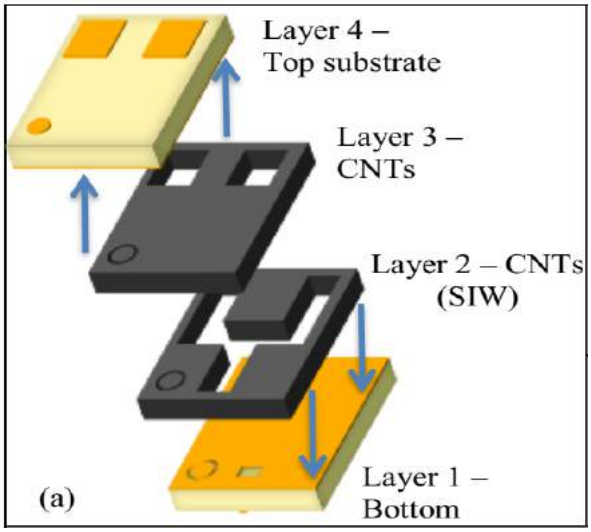

Figure 1: Sketched view illustrating the principle of the smart interposer

Five progressive steps with design, fabrication and characterization works will be considered to achieve the system-level demonstrator:

- **Step1**: SIW with CNTs lateral walls
- **Step2**: CNTs based SW-SIW
- **Step3**: Design of the Butler matrix elementary circuit blocks
- **Step4**: Assembly of the Butler matrix based on the elementary circuits blocks
- **Step5**: 3D integrated phased array in functionalized CNT-based interposer with Butler matrix slot coupled to a patch antenna array

In this work, TIMA will be in charge of studying, designing and fabricating the Butler matrix elementary circuits' blocks by using the CNTs based SW-SIW. Meanwhile, XLIM and CINTRA, two project partners, will take responsibility for CNT technology as well as the predictive electrical model of CNTs based SIW and SW-SIW, which can be simulated by 3D EM tools (ANSYS HFSS).

2. State of the art

2.1. Interposers

Interposer is an electrical interface that can be able to integrate various chips from various technologies on a very performing substrate that can eventually be multilayered and/or processed on both sides. The original idea was released by IBM Corporation that aimed at saving the computing time for data servers with particularly electrically performing connecting paths between processor chips [1]. From data server at the very beginning, applications turned now to mobility, which means integration density, low power and wireless. Three main technologies of interposer are competing at mm-waves: silicon, glass and organic. Meanwhile, the fourth technology: ceramic is predicted having a very specific application.

2.2. SIW and SW-SIW technologies

The SIW technology was invented at the early 2000s for mm-wave applications where a strong confinement of the wave is necessary, as well as high quality factors leading to the realization of low insertion loss devices. The concept is based on the realization of a waveguide embedded in a substrate by using a standard PCB technology, thus leading to low-cost waveguides. This is achieved by using doubled-face metallized substrates, and vias arranged in two parallel lines to define the lateral walls of the waveguide. After the first works presented in [2], the SIW technology

has been extensively studied and developed to design many passive circuits at low cost and high quality factor at mm-waves. More recently, the group in Grenoble has proposed a new concept of SIW: a slow-wave SIW, where several rows of metallized blind via holes are considered. This concept allows to reduce by 40 % the transversal dimension and the phase velocity as compared to a classical SIW designed for the same cutoff frequency, leading to a significant surface reduction and much more compact devices [3].

2.3. CNTs for RF applications

The physics and properties of CNTs have been studied for nearly three decades, and many possible applications for these nanomaterials have already been widely explored (as varied as the field effect transistor based on CNTs, or composite polymers, or conductive inks). As for the CINTRA and XLIM teams, they have been working on the use of CNTs for high-frequency applications and in particular for the nanopackaging: flip-chip bonding, circuits isolation and wireless interconnects. They demonstrated that the use of CNTs is an alternative approach for innovative solutions dedicated to 3D heterogeneous integration. Therefore, in this project, we will consider CNTs for the realization of SIW and SW-SIW and this new concept will be implemented on the basis of the expertise of CINTRA in the growth of CNTs where the CNTs will be modelled with the equivalent model that can be simulated with 3D EM tools.

3. Preliminary works and results

3.1. CNT based SIW

To obtain CNT based SIW, the lateral metallic walls of rectangular waveguides can be replaced by CNTs walls. First simulations were carried out by focusing on the density of the nanotubes and on the thickness of the walls. Two extreme densities of CNTs that can be obtained experimentally were considered, $10^{11}\,\mathrm{tubes/m^2}$ and $10^{14}\,\mathrm{tubes/m^2}$. After making simulation by using HFSS software, the results are shown in figure 2 (from Xlim).

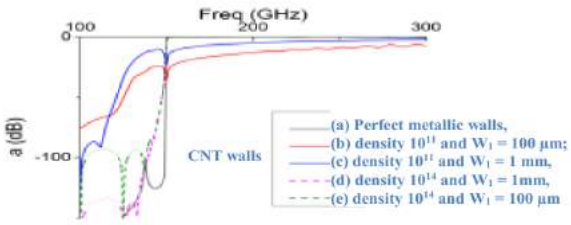

Figure 2: Transmission coefficient versus frequency

It is obvious that when using a high density of CNTs ($10^{14}\ tubes/m^2$), the transmission is the same as with a perfect conductor, even for a small wall thickness. It should be therefore possible to use CNT instead of metallic wall for the realization of waveguides.

3.2. CNT based SW-SIW

The concept of CNT based SW-SIW is described in figure 3, where the SIW is partially filled by a CNT's forest of height h_1. The electrical field is located only in the volume limited by h_2, whereas the magnetic field flows throughout the whole volume. Simulation results are shown in figure 4. They present the evolution of the transmission parameter S_{21}, where the reduction of the cut-off frequency can be observed with the increase of ratio $h_1/(h_1+h_2)$. It is clear that the SW-SIW cut-off frequency and phase velocity showed great reduction as compared to the conventional SIW.

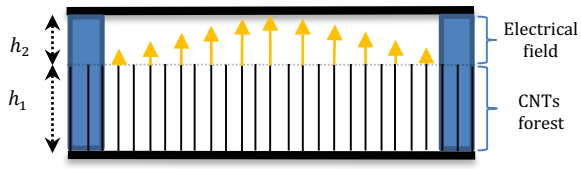

Figure 3: CNTs based SW-SIW concept

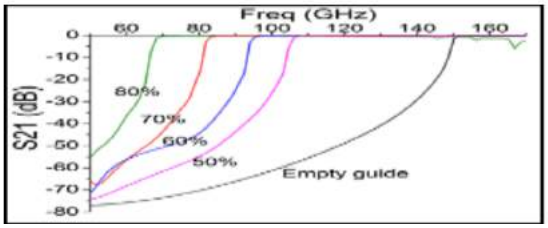

Figure 4: Simulation results of CNTs SW-SIW (cut-off frequency shift versus $h_1/(h_1+h_2)$

A method was proposed by Matthieu Bertrand to reduce the simulation time of periodic structures such as CNT based SW-SIW devices. It is based on the use of a unit cell that can be simulated by the eigen-mode solver in HFSS, instead of using the whole structure [4].

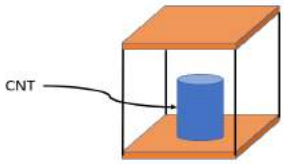

Figure 5: CNTs based SW-SIW unit cell

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Analog Serial Link

Members: M. Tmimi, P. Galy, S. D'Amico, P. Ferrari

Cooperation: STMicroelectronics Crolles

1. Introduction

The global internet Zettabyte traffic era and the need for higher computing performance always ask for higher data rates. Where the annual global IP traffic is projected to reach 3.3 zettabytes per year by 2021.To reach these goals, improvements have to be made to the existing serial links solutions, higher data rates need to be reached while taking into account the energy efficiency and the circuit complexity. Note that energy efficiency will probably become the main challenge in the next future. However, with the increasing data rates, signal integrity problems arise due to the losses in the channel, from the discontinuities caused by the different system components including impedance mismatches, cables and connectors transitions, DC power connections and vias. Furthermore, these losses make the channel vulnerable to higher losses in certain frequencies that might depend on the process. In that context the conventional serial links employ combinations of different equalization techniques including feedforward equalization (FFE), continuous-time linear equalization (CTLE) and decision feedback equalization (DFE) to compensate the channel impairments such as crosstalk or Inter-symbol interferences (ISI). To achieve more and more bandwidth and data processing capability, these equalization techniques complexity and sophistication skyrocketed in the last decades. Their implementation was possible and feasible because of the scaling of digital filters, they reduced both the surface area and power consumption as compared to previous technology nodes. However, the energy efficiency stopped scaling for the last technology nodes since the supply voltage has reached a limit.

An alternative approach will be investigated in this thesis. Communications techniques such as modulation and multi-tone signaling to allocate modulated carrier frequencies in the available bandwidths will be explored, while taking into consideration the channel state information and adapting the modulation schemes and frequencies to achieve the best performance from an energy and data rate point of view, with a probable trade-off.

2. Initial stages

A state-of-the-art study on wireline communications and mainly multi-tone signaling techniques is underway. Recently, researchers have been working on similar approaches, i.e replace equalization techniques with different modulation schemes as shown in Fig1. In these works, the modulation schemes were controlled using external components.

This thesis objective is to implement a full adaptive serial link that senses the channel state information (CSI) then decides which modulation schemes and transmission bandwidths to use, in order to maximize the data rate, minimize the power consumption and the silicon surface.

Furthermore, a reconfigurable Digital to Analog converter was designed in STMicroelectronics 28 nm FD-SOI technology, which is considered one of the key components in this architecture based on reconfigurable D/A and A/D converters [patent ref], and it is also a good design exercise for the initial thesis work. The design should be finished by February 2018.

3. Research opportunities and proposed approaches

Firstly, the used figure of merit (FoM) for conventional systems, which is energy efficiency per bit, does not take into consideration the modulation schemes and notches, thus an appropriate FoM will be investigated. Furthermore, a comparison of the existing solutions will be studied, since no such comparison or way of comparison exist to the best of our knowledge, the techniques will be compared for the same channel losses… using Matlab models. Beside the results, the advantages and disadvantages of each method will also be inspected.

Secondly, taking into consideration the possible trade-offs, the design of a robust and feasible adaptive system on ST 28nm FDSOI technology will be carried out.

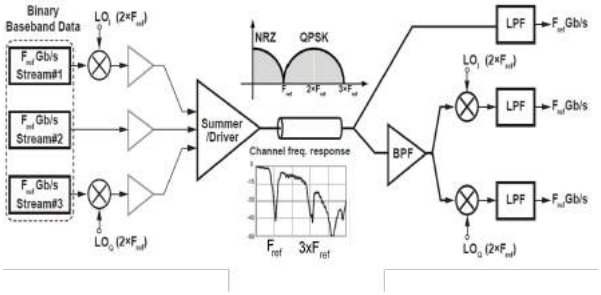


Figure 1: Hybrid serial link using NRZ/QPSK modulation

Performance monitoring and errors reconciliation in image decoder: blind image quality assessment

Keywords: Image quality, error concealment, no-reference metrics, fuzzy logic

Members: G. Takam-Tchendjou, E. Simeu, R. Alhakim, F. Lebowsky

Cooperation: STMicroelectronics

Contracts: NANO2017 A3

1. Introduction

Objective image quality assessment (IQA) seek automatically prediction of visual quality of an image without human judgments. In many recent works, objective IQA uses subjective IQA to evaluate and benchmark the objective IQA methods [1-3]. According to the level of information available on the reference image, objective IQA can be classified into three groups: Full-Reference (FR) IQA, which needs the complete reference image in order to be computed; Reduced-Reference (RR) IQA, where the reference image is only partially available in the form of a set of extracted features that help to evaluate the distorted image quality; and No-Reference (NR) IQA, which aims to automatically predict the quality of distorted images without any knowledge of reference image. This work presents the construction and implementation of a NR-IQA process, where the extracted features are based on a combination of natural scene statistic in the spatial domain, gradient magnitude, Laplacian of Gaussian, and on spatial and spectral entropies [4]. These features are trained using machine learning methods to construct the used model to predict the perceived image quality.

2. Features extraction methods

The extraction of features in this work is based on four principal axes: natural scene statistic (NSS) in spatial domain, gradient magnitude, Laplacian of Gaussian, and finally spatial and spectral entropies.

A. Natural scene statistic in spatial domain

The extraction of the features based on NSS in spatial domain starts by normalization of the image, to remove local mean displacements from zero log-contrast, and to normalize the local variance of the log contrast. The extracted features are composed of the symmetric and asymmetric parameters; where the asymmetric parameters are computed for four orientations. All the founded parameters are also computed for two scales. Finally, 17 NSS based features have been extracted.

B. Gradient magnitude and Laplacian of Gaussian

The second and third feature extraction methods are based on the joint statistics of the Gradient Magnitude (GM) and the Laplacian of Gaussian (LoG) contrast. These two elements GM and LoG are usually used to get semantic structure of any image. In this work, we have another usage of these elements as features to predict local image quality. 40 statistical features have been produced based on GM and LoG. However, many of them are highly correlated. So when using feature selection, only the independent features with the best correlation scores with the MOS are used, yielding 13 GM features and 09 LoG features.

C. Spatial and spectral entropies

Spatial entropy is a function of the probability distribution of the local pixel values, while spectral entropy is a function of the probability distribution of the local DCT coefficient values.

The process of extracting the spatial and spectral entropies features from images consists of three steps: 1) the first step is to decompose the image into three scales: low, middle and high. 2) The second step is to partition each scale of image into

8 x 8 blocks, and compute the spatial and spectral entropies within each block. 3) In the third step, pooling method is used to evaluate the mean and skew of blocks entropy within each scale.

At the end of the three steps, 09 independent features are extracted from the images.

3. Experimental results

Having extracted the independent features, the next step is to construct the models, which automatically predict the perceived quality of any input image without the reference image, using machine learning (ML) methods. The construction process of the objective NR-IQA block essentially consists of training (with 70 % of data) and validation phases.

Since the number of selected features is too big for one training (48 features), the used indirect process splits the training phase into three steps:

1) The first step is to distribute the features into classes, depending on the axes of the extracted features.

2) The second step tries to merge the features of each class in order to generate the appropriate intermediary metrics. The pooling process has then been carried out using different ML methods to create intermediary metrics M1, M2, M3 and M4 respectively. Finally, regression tree (RT) ML method produced the best results and is used to construct the intermediary metrics.

3) The third step is to use the four intermediary metrics in order to train ML models and derive the quality score estimators.

Table I presents the prediction performances of proposed process based on image quality assessment (IQA) models trained using TID2013 IQA database. The design of IQA models here consists of two training steps. The first step uses regression tree approach in order to merge the quality features into four intermediary metrics; the second training step uses different ML approaches (regression tree (RT), fuzzy logic (FL), Non-Linear regression (NLR), support vector machine (SVM) and artificial neural network (ANN)) for predicting quality score from the corresponding set of intermediary metrics.

Methods	PLCC	SRCC	KRCC	DCor
FL	0,931	0,922	0,782	0,915
SVM	0,850	0,849	0,696	0,840
RT	0,894	0,890	0,747	0,880
NLR	0,930	0,920	0,781	0,914
ANN	0,931	0,921	0,783	0,915

Table 1: Correlation between MOS and estimated MOS with TID2013 IQA database

The best-perceived image quality model is constructed by means of the two successive training steps: the first that uses regression tree ML method, while the second uses fuzzy logic ML method.

4. Implementation architectures and results

Having produced the simulation results of the MOS estimator on Matlab, this section presents the implementation architectures and results on FPGA platform for the best estimator method: which use the extracted features to produce intermediary metrics, and then, these intermediary metrics are used to construct the estimated MOS. This implementation has been done with Xilinx Vivado and Vivado HLS tool, and is implemented on Xilinx Virtex 7 (VC707) platform.

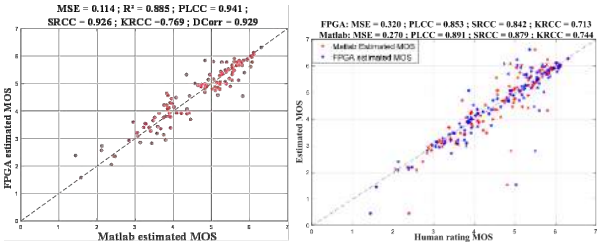
The architecture of the proposed implementation takes as input an image in AXI-Stream format, and produces its estimated score (MOS) as output. Five IP-cores divided in three groups have been implemented in HLS using C/C++ codes to evaluate the estimated score (MOS) of an image. The IP-cores in each group are executed in parallel.

The first group is for the feature extraction. This group contains three IP-cores: NSS_Core, GM-LOG_Core and SSE_Core; these IP-cores take as inputs an image as AXI-stream and the dimensions of this image: row and column sizes as integer; and produces as output 17 NSS features, 13 GM features and 09 LoG features, and 09 SSE features extracted in image, as a BRAM vectors.

The second group is for the production of the intermediary metrics. This group only contains the regression tree (RT) IP-core that takes as input the previously extracted features in a suitable vector format to produce as output the intermediary metrics in floating-point format.

The third and last group is for the production of the estimated score (MOS) of the image using the intermediary metrics. This group also has only the Fuzzy Logic (FL) IP-core that takes as input the four intermediary metrics produced by the RT_Core, and produces as output the estimated MOS in floating-point format, of the input image.

Fig.1 presents: in graph a), the comparison between the subjective MOS in x-axis and the MOS derived by FPGA implementation in y-axis; and in graph b), the comparison between the Matlab estimated score and the FPGA estimated score in y-axis and the subjective MOS in x-axis. This figure also presents the correlation score between the score in x-axis and the estimated score in y-axis on each graph.



a) *b)*

Figure 1: Comparison between MOS, Matlab estimated scores and FPGA implemented scores

5. Conclusions

In this work, we studied construction and implementation of an objective perceive image quality, using a no-reference IQA method. The produced process uses two training phases, the first to train the intermediary metrics with regression tree ML method, using the classes of independent features based on four axes, and the second to evaluate the image score with fuzzy logic ML method, using the produced intermediary metrics. The comparisons of the FPGA implementation results to the subjective MOS and to Matlab estimated results showed that this process is a reliable estimator of the perceived image quality.

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Energy modeling and management in wireless sensor networks

Keywords: Wireless Sensor Networks, Energy consumption, cover set, target coverage, approximation algorithms

Members: D. Tchuani-Tchakonte, E. Simeu, M. Tchuente

Cooperation: LIRIMA, IDASCO Team, Fac. of Sciences, Yaoundé Cameroun

1. Introduction

The energy constraint is a major issue in Wireless Sensor Networks (WSNs) since battery cells that supply sensor nodes have a limited amount of energy and are neither replaceable nor rechargeable in most cases. A common assumption is that the energy consumed by sensors in sleep mode is negligible. With this hypothesis, the usual approach is to iteratively consider subsets of nodes that cover all the targets. These subsets, also called cover sets, are then put in the active mode whereas the others are in the low-power or sleep mode. The scheduling of the appropriate cover sets in order to maximize the network lifetime is a challenging problem known to be NP-hard. Lifetime optimization of autonomous cooperating systems requires parsimonious energy management. This implies an accurate assessment of the consumption in the system components, including energy expenditure in sensor/actuator nodes as well as in the RF transceivers embedded for wireless communication. These precision requirements involve taking into account the consumption of the network sensor nodes not only in the active phases but also in the sleeping and standby phases, for which the energy consumption is not always negligible. The consideration of non-zero energy consumption of sensor nodes in sleep mode is more realistic but significantly increases the complexity of the problem. We propose a greedy algorithm that gives priority to sensors with lowest energy, and uses a blacklist to limit the number of sensors covering critical targets. We also propose an analytical approach for ring connected arrays of odd size, that are known to be rather tricky when non-disjoint cover sets are considered.

2. The greedy algorithm

Let r be the ratio between the energy in sleep mode P_v and the energy in active mode P_a, then $r = P_v/P_a$ and $r \in]0;1]$. Let t be a target covered by p sensors $s_0, s_1, \ldots, s_{p-1}$ with respective energies $E_0, E_1, \ldots, E_{p-1}$. We have shown that the coverage time D_t of the target t is maximal when the p sensors are activated according to the ascending order of their energies.

Considering this result, we propose a new algorithm based on two main ideas. The first idea is to limit in every cover set, the number of sensors that cover the critical targets by defining a. blacklist. The blacklist contains all the sensors not yet selected and that cover a critical target already covered by the cover set under construction. A sensor is selected from the blacklist only when none of the sensors out of the blacklist covers the remaining targets. The second idea is to give priority to sensors with minimal energy since the coverage time of a target is maximal when the sensors covering that target are activated in the ascending order of their initial energies. We conducted a set of simulations to estimate the performance of this algorithm and compared it to existing algorithms of the literature. These algorithms include Greedy-MSC [1], Static-CCF [2], Dynamic CCF [2], Adaptive algorithm [3], and MCS-based algorithm generating minimum size cover sets by using the classical greedy algorithm [4]. The metric used to measure the performance of each algorithm is the ratio between the network lifetime given by the algorithm and the upper bound of the network lifetime that is the maximal coverage time of the critical targets. Each algorithm tries to get a ratio close or equals to 1. Simulation results (Figure 1 and Figure 2) show that the greedy algorithm performs very well whether the energy consumed in sleep mode is negligible or not and no matter the dispersion of the sensors' energies, contrary to existing algorithms.

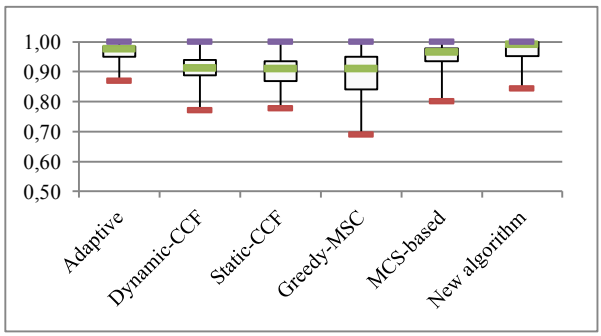

Figure 1: Performance of different algorithms when r = 0.1 and sensors' energies follow a Gaussian law of standard deviation 500

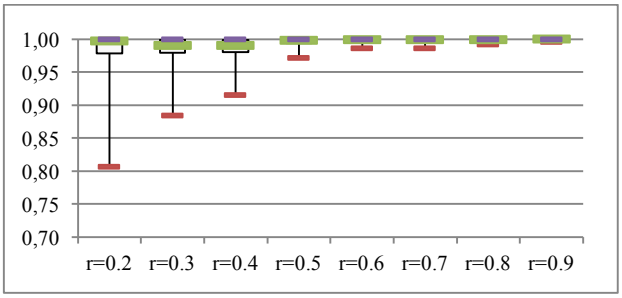

Figure 2: Performance of the new algorithm for different values or r when sensors' energies follow a Gaussian law of standard deviation 500.

3. A solution for general ring connected networks

We defined a family of instances of the Maximum Lifetime Coverage Problem, the family $\mathcal{F}$ of ring connected networks defined as follows. An instance $\mathcal{F}n$ of $\mathcal{F}$ is a bipartite ring-connected network where n sensor nodes $s_1,..,s_n$ and n targets $t_1,..,t_n$ alternate as illustrated in Figure 3. In such a network, each sensor covers exactly two targets and each target is covered by exactly two sensors.

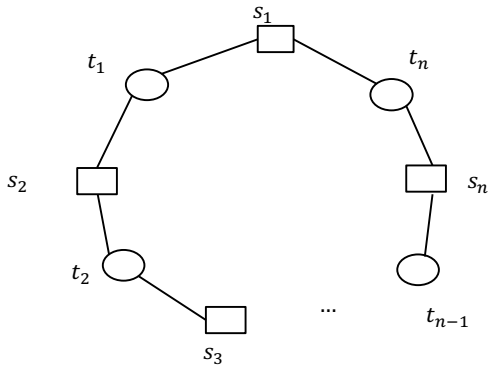

Figure 3: An instance $\mathcal{F}n$ of family $\mathcal{F}$

We proposed a solution for every instance $\mathcal{F}n$, $n = 2p + 1$, of family $\mathcal{F}$ when the energy consumed in sleep mode is negligible or not (i.e. $0 \leq r \leq 1$). Let us consider the sequence C_1, $C_2 = \sigma(C_1)$, …, $C_n = \sigma(C_{n-1})$, where C_1 is the minimal cover set $\{s_1, s_3, s_5, \dots, s_{n-1}\}$ and σ is the permutation defined by $\sigma(i) = i + 1$, for $i = 1, \dots, n-1$, and $\sigma(n) = 1$. Note that σ is an automorphism of the ring of order n. The activation duration Lt_j of the cover set C_j (for $j = 1, \dots, n$) is $Lt_j = \gamma_j * \frac{E}{P_a}$, where $\gamma_j \in \mathbb{R}^*$.

We considered the subclass of solutions where the battery of a sensor is exhausted after its last activation in a cover set. For each sensor s_i, let us denote K^i the index of the last cover set to which it belongs. With these hypotheses, the total energy consumed by sensor s_i is $P_a * \sum_{j=1}^{K^i} Lt_j * (\delta_{ij} + r * \overline{\delta_{ij}})$, where $\delta_{ij} = 1$ if $s_i \in C_j$ and $\delta_{ij} = 0$ otherwise. Indeed, the energy consumed by sensor s_i during the activation of C_j is equal to $P_a * Lt_j$ if sensor s_i belongs to C_j and is equal to $r * P_a * Lt_j$ otherwise.

Assuming that every sensor s_i has no remaining energy after belonging to the last cover set, it is easy to check that we obtain the following system of equations:

$$\begin{cases} \sum_{j=1}^{K^1} \gamma_j * (\delta_{1j} + r * \overline{\delta_{1j}}) = 1 \\ \sum_{j=1}^{K^2} \gamma_j * (\delta_{2j} + r * \overline{\delta_{2j}}) = 1 \\ \vdots \\ \sum_{j=1}^{K^n} \gamma_j * (\delta_{nj} + r * \overline{\delta_{nj}}) = 1 \end{cases} \quad (1)$$

The solution $(\gamma_1, \gamma_2, \dots, \gamma_n)$ of the system of equations (1) is: $\gamma_i = \frac{1}{(p+1)+ r*(p-1)}$ for $i = 1, \dots, n-1$, and $\gamma_n = \frac{1-r}{(p+1)+ r*(p-1)}$.

Let $\alpha = \frac{1}{(p+1)+ r*(p-1)}$. Each sensor belongs to $p + 1$ cover sets. The last cover set containing a sensor is either C_{n-1} or C_n. If the last cover set containing a sensor is C_{n-1}, then, after the activation of C_{n-1}, its battery has consumed $\alpha((p + 1) + r * (p - 1)) * E = E$. As a consequence, its battery is exhausted after its last activation. If the last cover set containing a sensor is C_n, then after the activation of C_n, its battery has consumed $\alpha(p + (1 - r) + r * p) * E = E$, hence its battery is exhausted after its last activation.

The network lifetime of this solution is $\Delta = \frac{n-r}{(p+1)+ r*(p-1)} * \frac{E}{P_a}$. We showed that this solution is optimal for $n = 3$, and we conjectured that it is optimal for every instance $\mathcal{F}n$, $n = 2p + 1$, of family $\mathcal{F}$.

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Synthesis of Low Cost Controllers for multiple source energy supply

Members: E. Simeu, G. Nzebop Ndenoka, M. Tabaa

Cooperation: LIRIMA, IDASCO Team, Fac. of Sciences, Yaoundé Cameroun,
LPRI Laboratory EMSI Casablanca, Morocco

1. Introduction

Information and Communication Technologies (ICT) have undergone enormous evolution in recent years. These changes have led to significant improvements in many application fields such as health care, education, commerce,... Automation is considered one of the most important sectors which has remarkably been developed thanks to the ICT revolution. For example, almost all digital devices, used to control automated electromechanical systems are nowadays based on sophisticated small microcontrollers instead of hard wired logic components (such as relays, cam timers, drum sequencers), that contribute explicitly to save time, energy, materials and money. Despite all these available advantages, sustainable development applications are slow to benefit from these to solve some implementation problems, such as energy and water distribution issues. The objective of this study is to design and implement energy control strategy for water supply problem in mountain villages as well as in city buildings having many floors.

2. Multiple energy sources control for water supply

The use of multiple water supply sources is a feasible solution allowing to face the recurring interruptions of urban water supply services. There are, however, a number of problems: some sources (wells/drillings) require electrical energy to operate. This energy can itself even be available in several possibilities including classical urban energy distribution as well as local sustainable sources. However, whether water or energy sources, their costs differ from one another. A management strategy must therefore be implemented to select available sources that are least costly at each operating time.

The importance to invest on renewable energy sources is highlighted (such as solar energy, wind energy,…) to permanently improve the availability of water [1]. Optimization methods can be useful in a context of household for minimizing energy consumption and to reduce leakage in a water distribution system (WDS) in a hydraulic context. A model of multi-criteria optimization for energy efficiency has been presents in [1]. But none of the existing methods presents the operational way of handling the issue of energy and water sources management.

The goal of our proposal is to find solution that combines sustainable solutions and the advantages of ICT tools in order to realize a complete and autonomous system for water and power supply, with a particular emphasize on saving energy. This involves the establishment of appropriate pumping mechanisms and an efficient process of switching between energy sources. The smart system should guarantee the continuous providing of water to households, and automatically switch between several water and power resources according to the source availability and the service costs.

3. Architectural structure

There exists many possible architectural structures for that problem, presenting different gain of energy. They depend on many factors: the number of tanks, the position of tanks with respect to floors, the pumping mechanisms. Whatever be the case, the final aim is to choose an architectural structure permitting to guarantee the supplying of every floor of the building while reducing considerably or minimizing the pumping energy consumed.

Generally, we may have any number k of tanks. In the case where there is only one tank ($k = 1$), that tank should supply water in all the floors of the building, which means that it would be situated above all the floors. It is then possible that the rainwater is not collected due to the position of that tank, which is relatively above the roof. However, if the rain water is not used, this leads to the loss of a very important source of water of relatively zero cost. The rainwater will be collected in a tank near the roof to allow the supply of any level of the building with zero energy.

When there are many tanks, every floor of the building could have its own tank. But if each of m floors has its own tank, it necessitates m tanks. This is costly since the cost of installation will be very huge unnecessarily. It is advantageous to group the floors in blocks to supply them with the same tank. Let ν be the number of floors supplied by each tank (for example $\nu = 3$ on Figure 1). $k = \left\lfloor \frac{m+1}{\nu} \right\rfloor$ is the number of tanks to supply the $(m + 1)$ floors of the building. Hence, every tank i is preferably supplying the floors $(i - 1)$, $\nu(i - 1) + 1$, $\nu(i - 1) + 2$, …, $\nu \times i - 1$, that are directly below that tank. It avoids waste of energy, because the water present in that tank may be probably pumped since the tanks that are at the bottom.

It would be possible (when there is a need) to drive water from a tank to another. If the tank from which water is convey to the other one is above, none energy is necessary.

To summarize it, we present on Figure 1 a generic architecture the floors supplied by tank with T_i

Every VT_i is the valve opening water from the tank T_i to the tank T_{i-1}, $i = 2, 3, \dots, k$.

VF_i is the valve opening water from the tank T_i to the corresponding floors, $i = 1, 2, 3, \dots, k$.

SP_i is the surface pump pumping water from the tank T_i to the tank T_{i+1} corresponding floors, $i = 1, 2, 3, \dots, k-1$.

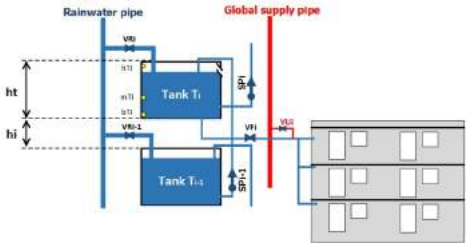

Figure 1: Schematic of an intermediary tank

4. Low cost devices for controller synthesis

In the IEC 61131-3 standard, there are five IEC standard programming languages [2] allow engineer to specify the operation of discrete event systems, even those who are more complex. However, they do not allow a direct realization on different control target devices like microcontrollers or FPGA. The objective here is to build an appropriate software tool that takes in input any PLC control program and treats it by successive refinements to produce an implementation on different types of targeted programmable devices. Because microcontrollers are not designed to survive in perturbed environments, another aim is to generate control codes that can detect and correct transitory errors that could occur in memory.

Several research studies have been occurred in order to find appropriate techniques which allow synthesizing any PLC control specification code and converting it to other executable programs (such as C, Fortran, VHDL) adapted with different hardware architectures [1], with a particular focus on the Grafcet model.

Therefore, carried out a novel software tool that can automatically convert any Grafcet specification sharp to bin-stream module and deploy it on any economic microcontroller, especially those of the Microship DsPIC, and Arduino family. The tool takes in entry the system functional requirements given in a Grafcet form. In effect, The Grafcet, one of the five IEC standard programming languages of IEC 61131-3, is a graphic language for modeling automated systems. It is the most international formalism used for high-level description of complex sequential systems [1]. This language is widely used in several domains such as home automation, automotive, power generation, manufacturing, environment, etc. It allows the specification of the expected behavior of a logic control system which is connected to a physical system with which it interacts, receiving logic signals that describe the physical environment and sending in response other signals in form of orders to serve as actions on that environment.

A Grafcet (program written in Grafcet language) is a graph that consists of two types of nodes: steps and transitions. A step is represented by a square, while a transition is represented by a horizontal line. The initial steps have a double square. Directed edges are necessarily used to connect steps to transitions or transitions to steps. Each step may be associated with several actions which represent the outputs of a Grafcet graph. An action is symbolized by a rectangle which is connected to a step. The same action can be connected to many steps and it becomes true if at least one of those steps is active. Some elements are used to separate structurally steps and transitions: "junction AND", "junction OR", "distribution AND" and "distribution OR".

We are also studying the synthesis using other PLC programming languages (LADDER, FBD ST) of the IEC 61131-3 standard. In fact, Grafcet or SFC can be used to structure a complex program written in the other languages of the same standard.

This tool is realized through a Model Driven approach. A Grafcet metamodel is used to describe the Grafcet language. As intermediate model, we have developed a Grafcet Matrix Model [4] that is a form of a low level Grafcet metamodel. It describes in a mathematical way all the necessary data structures for Grafcet realization. In order to address any µC, we use Feature Model Design techniques to express and implement targets characteristics. Figure 3 shows the feature model presenting the main characteristics of the µC to which we are interested when synthetizing control programs.

Figure 2: Feature Model of µCs

Given a grafcet specification of any logical control system, the synthesis process can be split into multiple steps broadly described on Figure 2. They are: Functional Design Specification (FDS) of the system, the design of the Grafcet model, the use of the *GrafcetConverter* tool and Integrated Circuit.

5. References

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