### Themes

- Mixed-signal/RF integrated devices
- Test and control techniques
- Design-for-test
- Diagnosis
- Embedded control
- Behavioral and statistical modeling methods
- CAD tools for test and control

### Expertise

**Scientific**
Test and diagnosis for mixed-signal/RF integrated devices, design-for-test, behavioral and statistical modeling, embedded control

**Fields of expertise**
Microelectronics, control, statistical modelling

**Know-how**
Test metrics estimation, machine-learning-based test, non-intrusive test and control, diagnosis, mixed-signal/RF design-for-test

**Industrial transfer**
Techniques of integrated test for analog-to-digital signal converters, CAD software for test, embedded sensors diagnostic technique

### Research keywords

Design-for-test, built-in self-test, design-for-manufacturing, calibration, density estimation, machine-learning, embedded control

### Contact

**Emmanuel SIMEU**
UGA Associate Professor
(+33) 4 76 57 47 25
emmanuel.simeu@univ-grenoble-alpes.fr
ADC BIST for static linearity test

Members: G. Renaud, M. Barragan, S. Mir

Cooperation: STMicroelectronics

Contracts: ELESIS (ENIAC)

1. Introduction
ADC static linearity test is one of the most time consuming tasks in production testing. The static performance of an ADC is characterized in terms of its DNL and INL figures that measure the deviation of the static transfer curve of the ADC from its ideal behavior. Traditional test methods for static test are based on applying a high-linearity test stimulus and then collecting a large number of samples per code to average the noise.

In this work, we have designed an on-chip ramp generator for high-resolution ADC BIST. This design will be implemented in an integrator-based servo-loop BIST scheme previously described in [1]. This scheme follows the classical servo-loop standardized test technique aimed at locating the transition voltages for a selected set of target codes, while enabling the use of the reduced code linearity test technique previously developed in our group [2]. The modified version of the servo-loop scheme is shown in Figure 1.

2. Practical implementation of the generator
The main challenge for moving the servo-loop technique to a practical on-chip implementation is the strict accuracy requirements for the input stimulus. In order to make a sufficiently precise measurement, the magnitude of the integration step should be below the LSB of the ADC, which is a challenging constraint for high-resolution ADCs.

In this work we opted for an on-chip ramp generator implementation based on a switch-capacitor (SC) integrator, as depicted in Figure 2. A detailed description of the design can be found in [3]-[4]. This implementation has phases $\Phi_{\text{up}}$ and $\Phi_{\text{down}}$ which control the sign of the ramp slope for each integration step. It also has a phase $\Phi_0$ that charges the output of the integrator to a voltage $V_a$ for calibration purposes [1]. To a first-order, the integration step in this integrator is defined by the capacitance difference between $C_{i1}$ and $C_{i2}$.

3. Design considerations
The operational amplifier is designed as a fully differential two-stage folded-cascode amplifier with Miller compensation and switched-capacitor common-mode feedback (SCCMFB). A differential configuration is chosen for its good behavior against common-mode noise while suppressing even harmonics, thus enhancing the linearity of the amplifier. The overall noise is reduced by design and an autozero technique is implemented to reduce the offset as well.

4. Experimental results
The proposed ramp generator has been designed and fabricated in STMicroelectronics 65 nm CMOS technology. Figure 3 shows a microphotograph of the fabricated circuit. The generator occupies an area of 0.1 mm² which is below 10% of the area of practical high-performance high-resolution ADCs.
A total of 15 packaged samples were available for characterization in the laboratory in terms of achieved resolution and linearity. Thus, Figure 4 shows a histogram of the average value of the step size and Figure 5 shows the histogram of the ENOB of the generated ramp, for the 15 fabricated samples. The clock frequency of the generator was set to 20 kHz, and the output swing of the generated differential ramp is ±2 V. Obtained results show a step size contained in the range 85 µV to 175 µV, and a static ENOB in the range 13.3 bits to 15.1 bits.

For further validation, Figure 7 shows a direct comparison between the obtained INL using the proposed generator (sample number 5 was used) and the actual INL obtained with external equipment.

5. References
ADC BIST for dynamic test

Members: H. Malloug, M. J. Barragán, S. Mir, E. Simeu

Cooperation: STMicroelectronics

Contracts: NANO2017

1. Introduction

We propose a novel generator architecture based on the concept of harmonic cancellation [1]. The proposed generator is aimed at a mostly-digital implementation that brings the advantages of easy design automation, portability, and migration, while providing compatibility with advanced technological nodes usually optimized for high performance digital applications. The proposed generator is based on a circular shift-register that produces time-delayed versions of a digital square-wave signal. Harmonic cancellation is used to cancel the low-frequency harmonic components of the digital square-wave signal, while a passive low-pass filter is employed for attenuating high-order harmonics and signal reconstruction. Additionally, we study a simple calibration strategy to mitigate the effects of process and mismatch variations which may degrade the effectiveness of the harmonic cancellation technique.

2. Harmonic cancellation

Let us consider a generic periodic signal \( x(t) \) expressed as a Fourier series expansion:

\[
x(t) = \sum_{k=1}^{\infty} A_k \cos(k \omega_0 t + \phi_k)
\]  

where \( A_k \) and \( \phi_k \) are the amplitude and phase of harmonic component \( k \) in signal \( x(t) \), respectively, and \( \omega_0 \) is the fundamental frequency of \( x(t) \). Let us define signal \( y(t) \) as the linear combination of the original signal \( x(t) \) and \( p \) pairs of scaled and shifted signals with opposite time-shifts \(+\Delta_t\) and \(-\Delta_t\) with respect to signal \( x(t) \) and scaled by a factor \( \alpha_i \). It can be derived that the spectrum of signal \( y(t) \) is given by:

\[
y(t) = \sum_{k=1}^{\infty} A_k \left[ 1 + 2 \sum_{i=1}^{p} \alpha_i \cos(k \phi_i) \right] \cos(k \omega_0 t + \phi_k)
\]

where \( \phi = \omega_0 \Delta t \) is the applied phase shift resulting from the time shift \( \Delta t \). That is, signal \( y(t) \) resulting from the combination of a periodic signal and its scaled and time-shifted versions with opposite time-shifts, has the same spectrum of signal \( 1 \) but the magnitude of the harmonic components are scaled by a factor \( I_k = 1 + 2 \sum_{i=1}^{p} \alpha_i \cos(k \phi_i) \). If the set of phase shifts and scale weights are properly selected such that the coefficients \( I_k \) are small for given values of \( k \), unwanted harmonic components in \( y(t) \) can be attenuated or completely cancelled.

In this work, our goal is to take advantage of this technique to generate high-quality analog sinusoidal stimuli from a set of time-shifted and scaled digital square-waves [2]. Digital square-waves are easily generated on-chip which makes this approach very suitable for BIST applications. Let us assume we have available \( N \) time-shifted versions of a unit-amplitude square-wave signal at discrete shift intervals of \( T/N \). From equation (4) it is easy to derive that adding \( p \) pairs of scaled and delayed square-waves to the original square-wave signal, all odd-order harmonic components lower than the \( 2(2p+1) \)th order will be cancelled if phase-shifted and weights are selected as:

\[
\begin{align*}
\phi_1 &= i \frac{\pi}{N} \\
\alpha_i &= \cos(i \frac{\pi}{N}) & 1 \leq i \leq p
\end{align*}
\]

(3)

3. Proposed architecture

We propose the hardware architecture in Figure 1 for our sinusoidal signal generator. The proposed generator design features a circular shift-register that provides a set of five time-delayed digital square-waves, a simple digital-to-analog interface that uses five current-steering branches with appropriately weighted currents, and a passive output filter for combining the five signals into an analog sinusoidal signal. We consider five time-delayed square-waves with opposite phase-shifts \( \phi_1=\pi/6 \), \( \phi_2=\pi/3 \) and scale weights \( \alpha_1=\sqrt{3}/2 \), \( \alpha_2=1/2 \). According to the analytical results in (4)-(5), this configuration cancels the third-, fifth-, seventh-, and ninth-order harmonic components in the original square-wave, while keeping a reduced design complexity.

![Figure 1: Conceptual block diagram of the proposed sinusoidal signal generator](image-url)
of two consecutive stages will be equal to $\pi/6$ by construction. The generated signals are fed to double-ended buffers that output two complementary square-waves without modifying the relative phase-shift and duty cycles. These complementary digital square-waves drive five fully-differential current-steering branches. The reference currents have been properly weighted to the ratios $I_1/I_0 = a_1 = \sqrt{3}/2$, and $I_2/I_0 = a_2 = 1/2$ to ensure harmonic cancellation. The differential output currents of the five branches are summed using an on-chip passive network that provides additional filtering and translates the generated signal to an output voltage signal. The use of current-steering sources is more convenient than using the resistors network for scaling the square-waves as it was proposed in [2] because it simplifies the implementation of the irrational scale factor and are easier to calibrate for process and mismatch variations. In this work, an external calibration algorithm has been implemented for controlling the bias current in the current-steering branches and calibrating the current ratios to assure harmonic cancellation conditions.

4. Simulation results
The proposed sinusoidal signal generator has been designed using STMicroelectronics 28 nm FDSOI technology. Electrical simulation results at transistor level are provided in order to show the feasibility and performance of the proposed sinusoidal signal generator. The circuit is clocked at 2 GHz in order to produce an output signal at 166.7 MHz. Figure 2 shows the spectrum of the generated output signal obtained from a transistor level simulation. Under typical corner conditions, the generated sinusoidal signal has a THD = −78 dB and a SFDR = 81 dB.

However, as discussed in [2], the performance of the proposed generation technique is very dependent on mismatch and process variations which introduce additional scaling errors and timing delays. Errors in the scale weight ratios will limit the effectiveness of the cancellation for the odd harmonic components, while timing deviations from a 50 % duty-cycle in the square-waves will introduce even-order harmonic components.

In order to show the feasibility of the proposed calibration technique, we selected the worst-case generator obtained by process and mismatch Monte Carlo simulation. The spectrum of the generated output sinusoid for this worst-case generator is plotted in Figure 3 which presents a THD = −39.5 dB and a SFDR = 40 dB. The proposed calibration algorithm tunes the currents in the current-steering branches in order to calibrate the current ratios that define the scale weights for the harmonic cancellation. The spectrum of the generated sinusoidal output after calibration is plotted in Figure 4. It is clear that odd-order harmonics are greatly attenuated after the calibration. The linearity of the calibrated signal is significantly improved, with a THD = −66.7 dB and a SFDR = 70 dB which corresponds to a 30 dB improvement with respect to the uncalibrated generator.

5. References
Built-in test in RF circuits using non-intrusive sensors

Members: A. Dimakos, H.-G. Stratigopoulos, S. Mir

Cooperation: CEA-LETI

Contracts: ELESIS (ENIAC), SACSO (ANR)

1. Introduction

Standard RF and millimeter (mm-wave) test practices incur a very high cost. An alternative technique with high potential to reduce test cost is built-in test, where the idea is to integrate on-chip some structures to facilitate the test, such as a test stimulus generator, response analyzer, etc. The most popular built-in test approach for RF transceivers is the loop-back test where the test signals are generated in the baseband and the transmitter’s output is switched to the receiver’s input to analyze the test response also in the baseband. Another popular built-in test technique relies on the use of envelope detectors and current sensors to extract DC/low-frequency test signatures that nevertheless carry RF information.

In this work, we propose to rely on non-intrusive built-in sensors that have the comparative advantage that let the design intact. The underlying idea is to monitor process variations instead of measuring directly the RF performances. For this purpose, we can employ Process Control Monitors (PCMs), such as single layout components (e.g. transistors, capacitors, resistors, inductors), and dummy circuits that are extracted from the CUT topology (e.g. bias stages, current mirrors, gain stages, level-shifters, etc.). These sensors are placed in close physical proximity and are matched to identical structures in the CUT. The sensors and the CUT “witness” the same die-to-die (D2D) and correlated within-die (WID) process variations and, as a result, the measurements obtained on the sensors will be correlated to the performances of the CUT to a very large extent. An indirect, low-cost test can be put in place by employing the alternate test paradigm to map the sensor measurements to the performances. We demonstrate the non-intrusive built-in strategy for a 60GHz mm-wave 3-stage Low Noise Amplifier (LNA) considering simulation data.

2. Results

Both the LNA and the non-intrusive variation-aware sensors have been designed using the 65nm CMOS065 bulk technology provided by ST Microelectronics. The schematic of the LNA is shown in Figure 1. The sensors that we have employed in the analysis include: (a) a dummy common source stage, (b) a dummy cascode stage, (c) a dummy N+ poly resistor, (d) a dummy metal-oxide-metal (MOM) capacitor , (e) a dummy transistor for monitoring variations in the gate resistance of MOS devises, and (f) a dummy transmission line, as shown in Figure 2. These dummy structures are built from identical components found in the topology of the circuit. In cases (d), (e), and (f), equivalent impedances are extracted at low frequencies and used as alternative measurements in alternate test.

For the simulation analysis, a Monte Carlo sample set of 1000 circuit instances was used to learn the regression functions in alternate test. Out of the 1000 instances, we used 800 circuit instances in the training set and the rest of 200 instances were used as a validation set to provide an unbiased estimate of the prediction error of alternate test. The prediction error is expressed in terms of: (a) average Root Mean Square (RMS) error, (b) absolute average RMS error, (c) correlation coefficient, and (d) maximum error between the simulated (e.g. “true) and predicted performances.

![Figure 1: 60GHz mm-wave 3-stage LNA schematic](image1.png)

![Figure 2: Variation-aware sensors built from identical components that exist in the topology of the 60GHz LNA](image2.png)

<table>
<thead>
<tr>
<th>Performance</th>
<th>Average RMS Error</th>
<th>Absolute Average RMS Error</th>
<th>Correlation Coefficient</th>
<th>Maximum Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{21}$</td>
<td>4.83 %</td>
<td>0.79 dB</td>
<td>64.07 %</td>
<td>3.08 dB</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>6.41 %</td>
<td>0.98 dB</td>
<td>47.82 %</td>
<td>2.41 dB</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>9.68 %</td>
<td>1.74 dB</td>
<td>64.31 %</td>
<td>4.16 dB</td>
</tr>
<tr>
<td>NF</td>
<td>4.74 %</td>
<td>0.27 dB</td>
<td>12.55 %</td>
<td>0.62 dB</td>
</tr>
<tr>
<td>IP$_{3}$</td>
<td>5.11 %</td>
<td>0.63 dB</td>
<td>34.55 %</td>
<td>1.45 dBm</td>
</tr>
</tbody>
</table>

Table 1: Alternate test prediction results using non-intrusive sensors (a), (b), (c), and (d), as shown in Figure 2
error metrics for a dummy transmission line does not improve appreciably but not dramatically, implying that variations in the transmission lines are not the main source of performance variability. This is also justified by the fact that the standard deviation of the performances is close to half standard deviation. The maximum error is smaller or at least comparable to the measurement and repeatability errors for some performances, such as $S_{21}$ and $S_{22}$.

Table 2 shows the prediction results when using non-intrusive sensors (a), (b), (c), (d), and (e), where compared to Table 1, we have added the dummy structure to measure $R_q$. As it can be seen, the prediction results have improved drastically. This is justified by the fact that variations in $R_q$ explain to a large degree the variations of most performances. For each performance the average absolute RMS error is smaller than one standard deviation for all performances except $S_{22}$. Overall, the predictions are deemed excellent for all performances except $S_{22}$.

Table 3 shows the prediction results when using non-intrusive sensors (a), (b), (c), (d), (e), and (f), where compared to Table 2 we have added the dummy transmission line. We observe that the prediction results compared to Table 2 have improved appreciably but not dramatically, implying that variations in the transmission lines are not the main source of performance variability. This is also justified by the fact that the standard deviation of the performances does not vary appreciably when statistical variations in transmission lines are disabled or enabled. We argue that it is perhaps unwise to deploy a dummy transmission line for the following reasons: (i) the prediction results for set B of non-intrusive sensors are already deemed excellent for all performances except $S_{22}$; (ii) the dummy transmission line does not improve the error metrics for $S_{22}$; (iii) the statistical model for the

Finally, Figure 3 shows a photograph of one fabricated chip from a set of 25 that are currently being measured. Figure 4 offers a visualization of the prediction results in Table 2 considering simulation data for NF performance. Each point corresponds to one circuit instance in the validation set.

Table 2: Alternate test prediction results using non-intrusive sensors (a), (b), (c), (d), and (e), as shown in Figure 2

<table>
<thead>
<tr>
<th>Performance</th>
<th>Average RMS Error</th>
<th>Absolute RMS Error</th>
<th>Correlation Coefficient</th>
<th>Maximum Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{21}$</td>
<td>3.77 %</td>
<td>0.62 dB</td>
<td>80.03 %</td>
<td>2.36 dB</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>3.42 %</td>
<td>0.53 dB</td>
<td>88.39 %</td>
<td>1.37 dB</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>9.88 %</td>
<td>1.74 dB</td>
<td>63.78 %</td>
<td>3.19 dB</td>
</tr>
<tr>
<td>NF</td>
<td>2.71 %</td>
<td>0.15 dB</td>
<td>81.40 %</td>
<td>0.41 dB</td>
</tr>
<tr>
<td>$IP_{1}$</td>
<td>3.13 %</td>
<td>0.38 dBm</td>
<td>81.09 %</td>
<td>1.07 dBm</td>
</tr>
</tbody>
</table>

Table 3: Alternate test prediction results using non-intrusive sensors (a), (b), (c), (d), (e), and (f), as shown in Figure 2

Table 1 shows the prediction results when using non-intrusive sensors (a), (b), (c), and (d). In fact, this set contains the sensors with the minimum area overhead possible. As it can be seen, the prediction results are not very satisfactory, but already we observe that the maximum error, however, can be as high as three standard deviations and is clearly higher than the measurement and repeatability errors.

3. References


Figure 3: Photo of fabricated 60GHz LNA chip

Figure 4: Scatter plot of measured vs. predicted values for NF performance of the LNA considering non-intrusive sensors (a), (b), (c), (d), and (e), as shown in Figure 2
One-shot non-intrusive calibration against process variations for analog/RF circuits

Members: M. Andraud, H.-G. Stratigopoulos, and E. Simeu

Contracts: SACSO (ANR), ELESIS (ENIAC JU), P-SOC (CNRS/INSIS)

1. Introduction
Deep sub-micrometer CMOS technologies drive a large proportion of innovation in many industries. A major challenge with these CMOS technologies is that the amount of process variation becomes particularly pronounced. Process variation causes measurable variance in the output performance especially in the case of analog/RF circuits. The trend nowadays is to integrate analog/RF circuits together on the same die with the digital processor and memory in advance process nodes. To address the problem of process variation, analog/RF circuits are often over-designed conservatively using large transistors, thus resulting in larger area and excessive power consumption.

2. Proposed one-shot calibration technique
This work proposes to design analog/RF circuits aggressively using minimum size transistors and leave large design margins by employing a calibration algorithm in post-manufacturing to recover yield loss and achieve overall a desired trade-off between output performances.

The proposed calibration algorithm, illustrated in Figure 1, is driven by measurements $M$ that offer an “image” of process variations. The measurements are obtained on low-overhead non-intrusive sensors. The non-intrusive property means that the sensors are not electrically connected to the circuit and, thus, are totally transparent to it. This is very appealing to designers since the circuit design is dissociated from the sensor integration and the sensor integration does not degrade the performances of the circuit. The sensors include single layout components and simple analog stages that are extracted from the topology of the circuit. Thus, this calibration approach is virtually applicable to any circuit. The core of the calibration algorithm is a regression model $P=z(M,TK)$ that expresses the relationship amongst the performances $P$ of the circuit, the sensor measurements $M$, and the tuning knob values $TK$. This regression model is learned based on initial production data and can be refined over time to account for process shifts. Thanks to the non-intrusive property, the sensor measurements stay invariant under changes of the tuning knobs. This means that it suffices to obtain the sensor measurements only once, plug their values into the regression model, and then optimize the resultant relationship between performances and tuning knobs without needing to repeat the sensor measurements for every tuning knob setting that is visited during the course of the optimization. In other words, the non-intrusive property allows us to perform the calibration efficiently in one-shot using a single test step and optimizing tuning knob values quickly in software in the background, which greatly reduces the calibration time.

3. Case study
Our case study is an RF Power Amplifier (PA). The PA and its associated non-intrusive built-in sensors have been designed using the 65nm CMOS065 bulk technology provided by ST Microelectronics. Figure 2 shows a microphotograph of one of the fabricated chips, highlighting the area of the circuit, and the Printed Circuit Board (PCB).

Figure 1: Proposed post-manufacturing calibration setup for RF circuits

Figure 2: a) Microphotograph of fabricated chip b) Photos of top and bottom of the PCB
The PA topology consists of a driver stage, a power stage, and three matching networks at the input (IM), output (OM), and inter-stage level (ISM), as illustrated in Figure 3. The matching networks have been implemented with discrete components on the PCB. The driver and power stage are based on the elementary stage shown in Figure 4, which is composed of the PA elementary stage and its associated non-intrusive sensors. The driver stage is composed of one PA elementary stage and the power stage is composed of four PA elementary stages connected in parallel.

As tuning knobs we have chosen the power supplies and bias voltages, that is, no alterations in the design have been made to insert extra tuning knobs. The set of non-intrusive sensors includes a dummy resistor, a dummy capacitor, and a dummy cascode gain stage for each PA elementary stage. These structures are extracted from the topology of the PA elementary stage, as shown in Figure 4. The set of measurements include the DC currents that flow through the two dummy resistors in the driver and power stages, the DC currents drawn by the two dummy cascode gain stages in the driver and power stages, and the values of the dummy capacitors.

To demonstrate the proposed calibration approach, we fabricated 3 wafers with FAST (i.e. FAST wafer), SLOW (i.e. SLOW wafer), and typical (i.e. TYP wafer) transistors. For the purpose of the experiment, we have at hand a total of 55 chips extracted from these 3 wafers.

4. Results

As an example, Figure 5 shows for the chips from the SLOW wafer, which are all non-functional before calibration, the histograms of the 4 main performances of the PA predicted by the regression model and measured after calibration. The yield recovery is 100% and the predictions point to the correct calibration decisions.

Figure 6 shows for the chips from the TYP wafer the histograms of the measured performances at a randomly selected tuning knob setting before calibration and the predicted and measured performances after calibration. We observe that before calibration the vast majority of chips violates the gain specification. The calibration algorithm was able to find appropriate tuning knob settings for these chips to fully recover yield loss and achieve a better performance trade-off.

5. References


Figure 3: Block diagram of the RF PA

Figure 4: Schematic of PA elementary stage with its associated sensors

Figure 5: Histograms of chips from SLOW wafer before and after calibration

Figure 6: Histograms of chips from TYP wafer before and after calibration
Built-In Self-Test solutions for mmW integrated circuits

Members: F. Cilici, M. J. Barragán, S. Mir, E. Lauga, S. Bourdel

Cooperation: IMEP-LACH

1. Introduction
Testing RF subsystems embedded in complex Systems-on-Chip (SoCs) and Systems-in-Package (SiPs) represents a challenging task. It can be said that RF testing inherits the difficulties of analog testing, but adding also the problem of handling high-frequency signals. The direct test and diagnosis of an RF device are based on complex functional tests that apply a high-frequency stimulus to the Device Under Test (DUT) and observe its response to compute a performance metric. This usually requires the use of dedicated high-speed test equipment and the provision of an adequate test access. However, the increase in operation frequency and the fact that RF blocks are currently embedded within a complete integrated system, turn these requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals between the chip and the external tester.

The development of RF Built-In Self-Test (BIST) is a promising solution to overcome these issues. BIST strategies are aimed to move some of the tester functionality into the DUT itself, in such a way that the circuit becomes self-testable. Signal manipulations would remain internal, thus eliminating transport problems. However, the RF BIST road is not free of shortcomings either. Two key problems that any successful RF BIST should overcome are: (a) the high sensitivity of internal RF nodes to any added load during test; and (b) the internal generation of adequate RF test stimuli. Indeed, RF signal paths are extremely sensitive to parasitic loads. Tapping into an RF node during BIST operation to connect an embedded test instrument may have a huge impact on the functionality of the DUT, masking the actual performance of the device. In the same way, RF front-ends, and particularly the receiver sections, are usually tested at their operation frequency. BIST approaches can only be successful if we can devise strategies for simplifying (or avoid) the internal generation of RF test stimulus, since the cost of including RF test signal generators on-chip together with the DUT is usually prohibitive.

2. Research opportunities and proposed approaches
There is not a widely accepted solution yet for incorporating BIST into the building blocks of state-of-the-art integrated transceivers. This thesis is aimed at defining novel test solutions for mmW circuitry that:

- Minimize or eliminate added loads to the RF signal path. RF circuits, and specially mmW circuits, are extremely sensitive to loading effects.
- Simplify or avoid the generation of RF tones. Dedicated RF tone generators based on RF VCOs offer a great RF performance, but at the cost of design complexity and a considerable area and power overhead.
- Consider the co-design of BIST circuitry and DUT since the early design stages. Any built-in test instrument that taps into the RF signal path should be carefully co-designed to avoid performance degradation.
- Minimize the number of required measurements. A cost-driven optimization of the set of RF measurements to filter redundant and costly measurements is also a promising path for reducing RF test complexity and cost.

3. Initial stages
The design of a mmW Power Amplifier at 60 GHz in STMicroelectronics 55 nm BiCMOS technology has been envisaged. We have developed a methodological approach to the design of the PA. This exercise not only has provided as with an actual state-of-the-art case study, but it also has given us a valuable insight on mmW design that will guide our research in future stages.
Performance monitoring and errors reconciliation in image decoders

**Keywords:** Image quality, error concealment, classification, regression

**Members:** G. Takam Tchendjou, E. Simeu, R. Alhakim, F. Lebowsky

**Cooperation:** STMicroelectronics

**Contracts:** NANO2017 A3

1. **Introduction**

Digital images are used in several life domains, such as video game, television, mobile device, traffic control, security services, medical, etc. [1]. All these domains do not have the same requirements in terms of image quality, but all of them follow similar processes that usually consist of five steps: 1) acquisition, 2) compression, 3) transmission, 4) storage and 5) display. Each step induces more or less significant distortions and artifacts on the original image which can produce the degradation of its visual quality. This work presents different machine learning (ML) algorithms that can be used for generating suitable objective IQA models. It focuses on applying fuzzy logic (FL) technique and optimizing its design parameters in order to build IQA models with high prediction performance and acceptable hardware-complexity. The results of the FL approach are compared with other IQA models, in terms of the accuracy and stability. Moreover, FPGA-based test platform is carried out to experimentally validate FL models.

2. **Fuzzy Logic**

The FL method can be considered as a generalization of the classical set theory by introducing the notion of degree in the verification of a condition; thus enabling a condition to be in a state other than 0 or 1. It provides a flexibility for reasoning, which makes it possible to take into account inaccuracies and uncertainties. The general architecture of a FL system can be described as follows:

- **Fuzzification module:** In this stage, the system input is transformed from its crisp number into fuzzy sets.
- **Knowledge base (Rules):** Which is represented by a set of IF-THEN rules provided by experts.
- **Inferences engine:** Which simulates the process of human reasoning. This is done by making fuzzy inference on the fuzzy inputs using the rules.
- **Defuzzification module:** It transforms the fuzzy set obtained by the inference engine into a crisp value.

Since IQA is basically a nonlinear problem, a solution using FL technique could be suitable for it. In our study case, the fuzzy inference system (FIS) has four input metrics \( X = \{x_1, x_2, x_3, x_4\} \) and one output \( y = \text{MOS} \).

The FL model can be automatically generated by applying Adaptive Neuro-Fuzzy Inference System (ANFIS). ANFIS is a combination of artificial neural network (ANN) and fuzzy inference systems (FIS). It works by extracting a training set of input-output data vector from image database TID2013, and applying the intelligent learning techniques of the ANN in order to derive the suitable fuzzy if-then rule set that permits minimizing the error between subjective MOS and the estimated MOS given by FL model. A typical ANFIS structure, as shown in Figure 1.

![ANFIS Architecture with two rules](image)

3. **Implementation architectures and results**

This section explains the implementation process on FPGA platform for two IQA models generated by FL method: the first model with Generalize Bell membership function, while the second with Gaussian membership function. The generated models have been implemented on Xilinx Kintex7 platform.

The overall architecture of this implementation is presented in Figure 2. It is composed of the following main blocks: IPCore of the FL IQA model, Microcontroller (MicroBlaze), DDR3 Memory, Interconnection units (such as AXI Interconnect and memory interface generator MIG) and other peripheries (such as UART and timer).

- **Microcontroller (MicroBlaze):** It executes the following main tasks: 1) initialize and configure all the parameters of the system, 2) coordinate the sequence of data movements into, out of, and between a system sub-units, and 3) perform certain logical and mathematical operations.
- **FL IP-Core:** This IP-core is built by means of a C/C++ codes in Vivado HLS tool to assess the image quality. It is managed by MicroBlaze through AXI interface.
- AXI interconnect unit: It permits to connect the MicroBlaze to all peripheries and DDR3 memory.
- Memory Interface Generator (MIG) is used as a convector between AXI and DDR3 interconnect protocols.
- UART unit is used to send the results from MicroBlaze to external machine.
- Timer unit is used to measure the elapsed time for certain process executions.

Figure 2: Implementation architecture

Two FL models have been built by means of Vivado HLS tool and by using C/C++ code. Vivado HLS tool permits also to synthesize (convert) the C/C++ code into VHDL RTL code. Moreover, thanks to vivado HLS tool, The generated VHDL RTL code is verified with RTL simulation, and is packaged to produce an IP-Core, where the generated FL IP-Core is considered as black-box composed of: 1) four floating-point inputs corresponding to the selected image metrics; 2) one floating-point output corresponding to the estimated MOS; 3) an output pointer, indicates that the image quality assessment process is successfully terminated and the result is ready at the output of the IP-core; and 4) other input signals (clock, reset and start).

Figure 3 gives the overall area used on Kintex 7 FPGA (KC705 evaluation platform xc7k325tffg900-2 device) of the FL model with the two MF types. The yellow area is the area utilized by FL IP-Core, while the blue area concerns the area of the rest of the system (other IP-cores, registers, microcontroller, interconnection, etc.).

Figure 4 presents the correlation results of model based on a) Gaussmf and b) Gbellmf. In these figures, simulation results are presented in x-axis and implementation results are presented in y-axis. This figures also presents the correlation scores (Pearson’s, Spearman’s, Kendall’s correlation; R2, and mean square error) between Matlab simulation results and FPGA implementation results.

4. Conclusions
In this work, we studied the methodology of IQA process based on fuzzy logic and its implementation on Xilinx Kintex7 FPGA by using vivado HLS tools with c/c++ language. The conclusion of the implementation phase is that the FL model with Gaussian MF gives the best performances in term of execution time and area overhead on FPGA-based chip, but the results produced by the Generalize Bell MF are more accurate and precise with the best correlation scores between FPGA implementation results and Matlab simulation results.

5. References
13Mpixel 55fps back-side-Illumination CMOS imager sensor with a calibrated piece-wise-linear ramp generator

Keywords: image sensors, CMOS, analog-to-digital converters, piece-wise-linear ramps

Members: C. Pastorelli, S. Mir

Cooperation: STMicroelectronics

Contracts: CIFRE

1. Introduction
The size of the pixel matrix in CMOS imager sensors (CIS) keeps increasing while there is a demand for high frame rates. In order to achieve higher levels of performance, the read out circuitry must be improved taking into account the highly constrained column pitch and the power consumption [1]. To get a high speed conversion at low power consumption in a small pitch-limited area, the single slope analog-to-digital converter (SS-ADC) is the best choice. It is well known that the main drawback of this ADC is the conversion speed. The use of a Piece-Wise-Linear (PWL) ramp in the read out circuit can increase the frame rate without degrading the image quality but this requires calibration. This work has developed a new calibration technique demonstrated in a 13 Mpixel sensor (4248 x 3216) at 55 frames/s, requiring a row reading time of 5.5μs that corresponds to an almost 20 % improvement with respect to similar imagers.

The time delay from the beginning of the ramp to the time when the ramp crosses the pixel value is measured by a counter. The converter Least Significant Bit (LSB) is defined by the slope of the ramp and the speed of the counter. Actually, the best way to reduce the conversion time without increasing the power consumption is to accelerate the ramp. This is possible taking into account the sources of pixel noise. The main source of electrical noise is the photon shot noise which follows a Poisson law of the form

\[ P(k) = \frac{n^k}{k!} e^{-n} \]  

with 'n' the number of photons. Therefore, \( \sigma^2 = n \) and \( SNR = \frac{n}{\sqrt{n}} = \sqrt{n} \). This is an absolute limit that comes from the light source. For an ADC that uses a piece-wise-linear ramp, the converter quantization noise at the output is given by \( \sigma_{ADC} = \frac{V_{LSB}}{\sqrt{12}} \). This quantization noise does not need to be low when the signal is strong, because it will be lower than the noise floor. This observation allows an increase of the quantization noise for stronger signals and the use of a piece-wise linear ramp [2].

2. CMOS imager architecture
Figure 1 shows the architecture of the CMOS imager [3,4]. The sensor has 4248x3216 pixels with an 1.1μm pitch, including dark and dummy pixels. The readout circuits use a digital CDS (DCDS) that allows for Vertical Fixed Pattern Noise (VFPN) free of mismatch. A 10-bit column-parallel ADC includes an integration capacitance which is a part of the PWL ramp generator, a buffer, a comparator and a ripple counter. A compiled digital calibration algorithm on the right side allows the calibration of the converted data. Column ADCs are located at the top and bottom of the array. This allows a pitch for the readout circuits of 2.2μm which is twice the pixel pitch.

Figure 2 shows a simplified schematic diagram of the PWL ramp generator. It is based on a switched current source with an integration capacitance. The variable current source is composed of an array of 11-bit thermometric unit elements and an integration capacitance distributed in column. The use of a buffer prevents smearing issues that can occur due to ramp distortion when many comparators simultaneously change state.
3. Calibration Techniques

The use of a PWL ramp can introduce distortion around the knee points of the ramp. This is due to comparator delays that depend on the ramp amplitude and mismatches on the overall array. To avoid these effects, we propose a calibration technique. The output data for the 1st PWL segment is automatically calibrated by the use of a digital CDS while the other segments are calibrated through additional measurements. In the case of 2 segments, a linear ramp conversion is applied with different slopes in order to measure the differential delay as shown in Figure 3. This calibration data is saved column by column for linearization.

4. Experimental results

The prototype image sensor has been fabricated in a 65nm 1P5M CIS process. Figure 4 shows a picture of the fabricated chip. The die size is 6.5mm(V)x6.3mm(H). The PWL ramp generator is placed on the left side of the chip at the exact middle of the array to get the same wiring length of the data transfer path to avoid differences between the readout on top and bottom sides.

Figure 5 shows the measured ADC differential non-linearity (DNL) with and without calibration. With calibration, DNL is -0.5/+0.5 LSB at a 10-bit resolution and 55 fps. The measured ADC noise is 1.89 e-rms, the random noise is 1.07 e-rms and a dynamic range of 61dB is reached at 55fps with an analogue gain of 1, while dissipating 82.4mW. Besides, the measured vertical fixed pattern noise (VFPN) is 0.03LSB.

5. References


Energy modeling and management in wireless sensor networks

**Keywords:** Wireless Sensor Networks, Energy consumption, cover set, target coverage, approximation algorithms

**Members:** D. Tchuani Tchakonte, E. Simeu, M. Tchuente

**Cooperation:** LIRIMA, Equipe IDASCO, Fac. Sciences, Yaoundé Cameroun

1. Introduction

WSNs consist of tiny sensor nodes with embedded microcontrollers, low power radios, battery cells and sensors which are used to monitor environmental conditions such as temperature, pressure, humidity, and vibration [1]. The energy constraint is a major issue in WSNs since battery cells that supply sensor nodes have a limited amount of energy and they are neither replaceable nor rechargeable in most cases. Target coverage applications are the category of WSN applications where there are several points of interest called targets that need to be continuously monitored by sensor nodes [2]. Due to the energy constraint, the main challenge in target coverage applications is to maximize the network lifetime defined as the time span that all the targets are continuously covered. A common approach to tackle this issue is to alternate the sensor nodes between active and sleep modes. Actually, a sensor node can work in two modes; the active mode and the sleep mode where the energy consumption is much less than this of the active mode. The problem of determining a sleep/active schedule for sensor nodes in order to maximize the network lifetime is called Maximum Lifetime Coverage Problem (MLCP) and is known to be NP-hard. This problem has been studied extensively in the literature but the common assumption is to consider that the energy consumption of a sensor node in the sleep mode is negligible. However, the experiments that we conducted showed that this assumption is not realistic. We designed a new algorithm for this problem by taking into account the energy consumption in the sleep mode.

2. Experiments and observations

In our experiments, we realized the sensor nodes with:
- Arduino Uno microcontroller
- LORA technology transceiver
- DS18B20 temperature sensors
- AA battery cells

The base station is made of a Raspberry Pi 3 computer on chip with a LORA technology transceiver and runs under Raspbian operating system.

![Figure 1: A temperature sensor node](image1.png)

The goal of these experiments is to verify if the energy consumption of a sensor node in the sleep mode is negligible compared to its consumption in the active mode. Thereby, we considered a wireless sensor network where a sensor node in the active mode takes a number of temperature measurements every active period \( T_\text{a} \) and sends them to the base station. The active sensor node also sends information about its remaining energy to the base station. A sensor node in a sleep mode sends one message containing its remaining energy every sleep period \( T_\text{s} \). That message is used to keep synchronization between a sensor node in the sleep mode and the base station. Let us note \( R \) the ratio between the active period and the sleep period, and \( r \) the ratio between the current consumed in the sleep mode and the current consumed in the active mode.

Figure 3 depicts the variation of the ratio \( r \) according to the number of samples sent per period to the base station. We observe that the ratio \( r \) is close to 0.5 when the active sensor node sends only one sample per active period. This ratio decreases progressively till approximately 0.1 when the number of transmitted samples increases till 10. We can also observe that the value of \( r \) slightly decreases when the value of \( R \) increases. These experiments show that the energy consumed in the sleep mode is not negligible compared the energy consumed in the active mode. Moreover, the ratio \( r \) could be much higher if a sensor node sends a sample only when the difference with the previous sample is significant. We can then conclude that neglecting the energy consumed in the sleep mode is not realistic.
3. Proposed algorithm

By taking into account the energy consumed by a sensor node in the sleep mode; we proposed a new greedy algorithm. The main ideas of this algorithm come from two observations. The first observation is that the order in which two sensor nodes are activated influences the network lifetime obtained. Thus, by activating firstly the sensor node with less energy, the lifetime obtained is greater than the one obtained when the sensor node with more energy is activated firstly. The second observation is that we should avoid as much as possible to select more than one sensor nodes that cover the critical target in the same cover set. Indeed, the upper bound of the coverage time of the critical target is the upper bound of the total network lifetime.

The new algorithm works as follows. To form a new cover set, we identify the critical targets and the black list is empty. At each iteration, we add in the cover set the sensor node with minimal energy and not in the black list that covers at least one target not yet covered by the cover set. Then, we insert in the black list the other sensor nodes covering the same critical targets as the selected sensor node. A sensor node is chosen in the black list when the targets not yet covered by the cover set are covered only by sensor nodes in the black list. At last, we remove redundant sensor nodes from the cover set if there are some.

We conducted a series of simulations to analyze the performance of that algorithm. The simulation results showed that the algorithm performs well when the ratio \( r \) tends to 0 and the algorithm is near-optimal when the ratio \( r \) is greater or equal to 0.1. Some results are shown on figures 3 and 4.

4. References


Synthesis of Low Cost Programmable Logic Controllers

Members: E. Simeu, G. Nzebop Ndenoka, R. Alhakim

Cooperation: LIRIMA, Equipe IDASCO, Fac. Sciences, Yaoundé Cameroun

1. Introduction
The widespread automation of production and information processing systems has been a decisive factor in the social and industrial development in developed countries. This has required equipment and advanced technologies in which the PLCs take pride of place. Nowadays, there is a wide variety of very cheap programmable circuits, which could functionally replace conventional PLCs in low cost automation applications. Unfortunately, these programmable devices are not often used in automation applications because they do not enjoy the benefits of a standardized specification and programming environment such as IEC 61131 that have been developed to standardize the specification and the programming of PLCs in automation applications.

2. PLC synthesis using low cost devices
In the IEC 61131-3 standard, there are five IEC standard programming languages [3] allow engineer to specify the operation of discrete event systems, even those who are more complex. However, they do not allow a direct realization on different control target devices like microcontrollers or FPGA. The objective here is to build an appropriate software tool that takes in input any PLC control program and treats it by successive refinements to produce an implementation on different types of targeted programmable devices. Because microcontrollers are not designed to survive in perturbed environments, another aim is to generate control codes that can detect and correct transitory errors that could occur in memory.

Several research studies have been occurred in order to find appropriate techniques which allow synthesizing any PLC control specification code and converting it to other executable programs (such as C, Fortran, VHDL) adapted with different hardware architectures [1-2], with a particular focus on the Grafcet model.

Therefore, carried out a novel software tool that can automatically convert any Grafcet specification sharp to bin-stream module and deploy it on any economic microcontroller, especially those of the Microship dsPIC, and Arduino family. The tool takes in entry the system functional requirements given in a Grafcet form. In effect, The Grafcet, one of the five IEC standard programming languages of IEC 61131-3, is a graphic language for modeling automated systems. It is the most international formalism used for high-level description of complex sequential systems [2]. This language is widely used in several domains such as home automation, automotive, power generation, manufacturing, environment, etc. It allows the specification of the expected behavior of a logic control system which is connected to a physical system with which it interacts, receiving logic signals that describe the physical environment and sending in response other signals in form of orders to serve as actions on that environment [5]. It describes states of a system and associated actions that permits to take into account necessary inputs and generate corresponding outputs, according to the PLC scan cycle described in Figure 1.

A grafcet (program written in Grafcet language) is a graph that consists of two types of nodes: steps and transitions. A step is represented by a square, while a transition is represented by a horizontal line. The initial steps have a double square. Directed edges are necessarily used to connect steps to transitions or transitions to steps. Each step may be associated with several actions which represent the outputs of a Grafcet graph. An action is symbolized by a rectangle which is connected to a step. The same action can be connected to many steps and it becomes true if at least one of those steps is active. Some elements are used to separate structurally steps and transitions: ”junction AND”, ”junction OR”, ”distribution AND” and ”distribution OR”.

We are also studying the synthesis of other PLC programming languages (LADDER, FBD ST) of the IEC 61131-3 standard. In fact, Grafcet or SFC can be used to structure a complex program written in the other languages of the same standard.

![Figure 1: PLC scan cycle](image-url)
3. Synthesis process implementation
Given a Grafcet specification of any logical control system, the synthesis process can be split into multiple steps broadly described on Figure 2. They are: Functional Design Specification (FDS) of the system, the design of the Grafcet model, the use of the GrafcetConverter tool and Integrated Circuit.

This tool is realized through a Model Driven approach [6]. A Grafcet metamodel is used to describe the Grafcet language. As intermediate model, we have developed a Grafcet Matrix Model [4] that is a form of a low level Grafcet metamodel. It describes in a mathematical way all the necessary data structures for Grafcet realization. In order to address any μC, we use Feature Model Design techniques [7] to express and implement targets characteristics. Figure 3 shows the feature model presenting the main characteristics of the μC to which we are interested when synthetizing control programs.

4. References