TIMA is a public research laboratory sponsored by Centre National de la Recherche Scientifique (CNRS), Grenoble Institute of Technology (Grenoble INP) and Université Joseph Fourier (UJF). TIMA addresses some of the most urgent and ambitious challenges related to the design of tomorrow’s circuits and systems on a chip. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end.

In 2015, TIMA is structured in five research teams, according to the domain of expertise and research communities of their members. The projects reported in this document are grouped according to these teams.

Architectures and Methods for Resilient Systems (AMfoRs). Multi-level specification and verification of hardware/software on-chip architectures; System-level modeling, analysis and testing; Dependability of integrated systems; Secured integrated architectures; Multi-level dependability evaluations.

Design of integrated devices, circuits and systems (CDSI). MEMS: microgenerators, acoustic sensors, Pressure microsensors; BIOMEMS microsystems. Asynchronous circuits and systems (asynchronous IP’s, NoCs, GALS, etc.); Non-uniform sampling and signal processing (algorithms, architectures, circuits); Reconfigurable asynchronous logic; Safe and secured robust asynchronous circuits; Smart CMOS vision sensors.

Robust Integrated Systems (RIS). Robust massively parallel single-chip architectures; Power management from the OS down to silicon; Fault tolerant and self-adaptive architectures; 3D NOC Robust Architectures; Design in Reliability face to aging, process variation and soft errors; Evaluation of robustness and qualification: radiation tests, fault injection; Architectures for Nanotechnologies.

Reliable Mixed-Signal circuits and systems (RMS). Mixed-signal/RF integrated devices; Test and control techniques; Design-for-test; Diagnosis; Embedded control; Behavioral and statistical modeling methods; CAD tools for test and control.

System Level Synthesis (SLS). HW/SW Architectures and CAD software for multiprocessor systems on chip; Specification, modeling, simulation and implementation of embedded systems on chip; Reconfigurable and prototyping.

The 2015 edition of TIMA annual report presents a brief and synthetic presentation of each research team, followed by a scientific summary of its main projects. Each project is well identified with the relevant key-words, investigators, cooperation and contracts. For detailed scientific information, the reader is referred to the relevant articles. A complete list of publications, classified by category and by topic, is also provided at the end of the document.

A large part of the research is financed by research grants and contracts. Some are large cooperative projects with industrial and academic partners, at the national, European or world level; others are bilateral industrial collaborations, linked to a CIFRE doctoral co-tutorship. Most contracts run for 3 to 4 years. In 2015, 39 contracts were in operation, out of which 12 new projects were started. Page 97 gives an overview of our contractual activity.

Among the highlights of the year, three publications were distinguished in a major international conference with a best paper award: L. Anghel et al. (AMfoRS) for the paper « Digital circuits reliability with in-situ monitors in 28nm fully depleted SOI » at DATE 2015, H. Le Galle et al. (RMS) for the paper « High frequency jitter estimator for SoCs » at ETS 2015, and J. Saadé et al. (SLS) for the paper « Line coding methods for high speed serial links » at ISM 2015. One patent has been filed in 2015, by V. Schwambach et al. (SLS) : « Procédé et dispositif de génération d’une représentation multi-résolutions d’une image et application à la détection d’objet utilisant une fenêtre de détection ».

Members of TIMA were active in the Technical Program Committee of many international conferences and workshops, with a particular involvement in the organization of IOLTS and IMSTW as General Chair. The details of these contributions to the scientific community are listed starting page 107.
Finally, TIMA takes an active part in the new organization of the research in the Grenoble Alpes University, being linked to the two poles "Mathematics, Informatics and Communication" (MSTIC) and "Physics, Engineering and Materials" (PEM). TIMA is also a member of the Carnot LSI Institute and a member of Persyval Lab.

Salvador MIR

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Team 1 / Architectures and Methods for Resilient Systems (AMfoRS)

Themes

Multi-level specification and verification of hardware/software on-chip architectures
System-level modeling, analysis and testing
Dependability of integrated systems
Secured integrated architectures
Multi-level dependability evaluations

Expertise

Scientific
Systems modeling, requirements formalization, temporal logics, automatic proofs, fault
detection/tolerance, modeling of aging effects, methods for robustness analysis, hardware security, system-
level testing

Fields of expertise
Correctness verification and dependability evaluation at various levels of the design flow, formal
methods, dependability improvement, hardware security, system-level testing

Know-how
Analysis and formalization of requirements, formal and semi-formal verification, assertion-based design,
fault tolerance or detection, fault injection, cryptographic accelerators, hardware attacks and counter-
measures for secured circuits, IEEE 1687-compliant testing

Industrial transfer
Transfer of HORUS technology in EDA tools for mixed systems by Dolphin Integration
IDSM functional continuous checking approach transferred to STMicroelectronics
MAST - CAD-tool for system-level testing based on IEEE 1687 under technological maturation

Research keywords
Specification and verification of complex systems, assertion-based verification, correct-by-
construction design, fault tolerance, security, aging, robustness analysis

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System-Level Test Architectures and Standards

Key-words: Testing, IEEE 1687, System-level approaches

Members: M. Portolan

Contracts: MAST (Linksium)

Context and goals

The digital automated testing field has been living a huge evolution in the latter years: chips are becoming more and more complex, System-on-Chips (SoCs) are now common and new approaches like 3D Chips/Stacked Dies are pushing design and performance boundaries even further. Testing these new components where traditional divisions between component, device and system are blurred is a formidable task, and the field is responding by generating new dedicated approaches. Most actors soon realized that such an effort is not feasible by one entity, so different standardizations were launched, some of which started bearing their first results. Of particular interest is the new IEEE 1687-2014 standard, which develops and extends over the widespread IEEE 1149.1 standard, commonly known as JTAG, by adding several disruptive innovations, among which of particular importance are:
- Dynamic-length scan chains;
- Instrument usage through a JTAG chain

These two elements have the potential not only to completely change the landscape of automated testing, but also to bring the current EDA tool to the brink of breaking. Current tooling is in fact based on a structural analysis of a System Under Test (SUT), helped by precise hardware assumptions, like for instance the fixed length of the scan chains, which are used to achieve global optimization with reasonable effort. Once these assumptions fall, the complexity explosion itself might be enough to render the tool helpless. Similarly, structural test implies a non-interactive environment where input vectors are applied to the SUT and the output are compared with pre-computed expected vectors: the complete flow is depicted in Figure 1

Future outcomes

The work has been focused on developing an innovative backend that is able to provide the features needed for the evolution of automated testing while maintaining a compatibility with IEEE standards and EDA tools. The goal is the development of a complementary solution to the current approaches, focusing on test execution rather than on test generation as it has been the case up until now.

The final proposal for a new Functional Execution Flow is based on State of the Art software and Operating System (OS) engineering and is depicted in Figure 2

In this solution, each hardware instrument (depicted in Yellow in the bottom left-hand corner) is associated with a Software Algorithm (depicted in Green in the top right-hand corner). Each algorithm $A_n$ can access its related Instrument $I_n$ thanks to an API based on the Procedural Description Language (PDL), defined in the IEEE 1687-2014 standard. These API requests are handled by an Execution Arbiter (EA) which polls them and translates them into system-level...
vectors thanks to an internal System Model (SM). This latter can be obtained from standard languages (ex: the Instrument Connectivity Language, ICL, defined by IEEE 1687-2014) through standard ADE tools, but it can also be extended to support custom structures. The System Model contains a copy of the state of the SUT and their coordination is assured by the Execution Arbiter: when the SM and SUT states are desynchronized, the EA is able to generate a series of actions (i.e. scan operations) to restore synchronization. This behavior is exploited to perform dynamic topology configuration: PDL operations are posted as modifications to the SM, so that the EA can generate the necessarily actions to restore synchronization and therefore obtain the desired configuration. This behavior has been completely specified and has been accompanied by an extensive analysis and generalization effort in order to define the minimal information set needed for the System Model. This knowledge has been used as the base for developing of piece of software, the MAAnager for System-centric Test (MAST) that implements the flow of Figure 2. The main reason for this effort is to validate the theoretical assumptions by applying them to industrial use cases, whose results can be used for scientific dissemination. This strategy was a success: we achieved publications in a top European conference [1], as well as invited talks to the two most important test conferences in the USA [2, 3] and to a new workshop dedicated to the impact of test standards [4].

MAST is also a piece of software with a high potential impact in the field of automated testing, well beyond traditional scan: its technical solutions are unique in the field and respond to the needs of new users that are proposing innovative use models that are not compatible with current EDA tools. Of particular importance is the usage of IEEE 1687-2014 to control Mixed-Signal instruments: demand for usage is growing, but no commercial tools are providing satisfying solution. We launched a new collaboration with the RMS group of TIMA on the subject, which resulted in a joint presentation at the above-mentioned workshop [5]. Recognizing its high market potential, valorization structures are financing a 12-month “Technological Maturation Project” through Linksium. The MAST software itself has been submitted to the “Agence pour la protection des programmes” (APP) of the French government [6] to assure IP protection.

References
[6] Depot APP (Software legal protection) IDDN.FR.001.260016.000S.P. 2015.000.10600, 18/06/2015
Runtime Monitoring of Hardware/Software Systems on Chip

Key-words: Temporal properties, Assertion-Based Verification, system level and software verification

Members: L.Pierre, M.Chabot, K.Mazet

Contracts: SPICA (FUI)

1. Context

The work reported here is part of a project that targets the validation of both System-level and software requirements of hardware/software systems on chip, see Figure 1. Previous work has produced a tool, ISIS [1], that provides Assertion-Based Verification (ABV) for high-level models of systems on chip (SystemC TLM virtual platforms), and also a refinement flow to convey system-level properties through the high-level synthesis (HLS) procedure [2]. On the virtual platform model, assertion checkers can ease the debugging process: produced from PSL temporal properties (Property Specification Language, IEEE standard 1850), they are used to instrument the platform to check (during simulation) system level requirements on the interactions between hardware or hardware/software components. At the Register Transfer level, they check the same properties, refined to take into account actual protocols and timing introduced during HLS. Such concretized assertion checkers can ultimately be implemented with the system in the final device, to perform online monitoring.

![Figure 1: Context: ABV infrastructure for Systems on Chip](image)

Recent work has also improved the support for the use of auxiliary (global and local) variables in temporal assertions, from a semantic and practical point of view [3].

2. Monitoring of C programs

The objective of the work reported here is to complement this original solution with assertion checkers for purely software requirements about the internal program behaviour (left side of Figure 1), to be checked either on a model of the system or on the final device. To specify the expected program behaviour, it must be possible to formalize properties in terms of variable values and function calls (for example "it is always true that, if the function call send_to_HW(addr2,0x0,0x3) occurs, then eventually the variable INTR is set" - P.Cheung, A.Forin, "A C-Language Binding for PSL," Proc. ICESS’2007).

Therefore, major events of interest to sample the execution trace and activate the assertion checkers accordingly are variable updateings, and function calls (or returns). But observing read actions (for example when the value of a variable is read to evaluate an expression) is crucial too, for instance:
- when the embedded firmware processes values that have been transferred into memory by an external component (e.g., a DMA that transfers values coming from sensors, antennas, etc),
- in case of faults, modifications of variables can occur independently of the programmer’s intention, and the checkers should be able to detect them.

We have specified and implemented a new tool, called OSIRIS, that automatically generates assertion checkers from PSL properties and instruments the program with these verification components, together with an observation mechanism that enables their event-driven activation [4]. The principles of this tool are inspired by the ones of the ISIS framework, but the observation model has been adapted to fit the needs of the sampling scheme described above.

For maximum flexibility, the current implementation proposes either to decorate the source code or to observe the binary code under execution.

3. Source code instrumentation

The first solution, which performs source code instrumentation, is definitely intrusive in the original code, but intrusiveness is extremely moderate. This instrumentation is produced as a decoration of the grammar rules for C expressions, such that calls to observation functions are appended to some sub-expressions.

The source files together with their requirements expressed in PSL files are provided as input, and OSIRIS proceeds as pictured by Figure 2: the module AssertionsToXML parses the assertions and creates an XML file that gathers information.
about the elements (variables and functions) that will have to be observed, with the corresponding events; the component SourcesTransform takes as input the source files, adds data in the XML file (variable types and function prototypes) and instruments the source files; the third component uses the assertions and the information of the XML file to produce the assertion checkers and their wrappers.

Figure 2: OSIRIS source code instrumentation

4. Binary surveillance

As an alternative, OSIRIS only requires the binary file and produces an infrastructure that enables surveillance during execution. The generated infrastructure assumes the presence of a POSIX-compliant OS. It uses the "ptrace" system call, and it runs two processes concurrently (as shown of Figure 3): Process 1 that executes the original application, and Process 2 (called the Tracer) that observes its execution and evaluates the assertions when relevant events are detected.

Figure 3: OSIRIS: Binary surveillance by a Tracer process

To produce such an infrastructure, OSIRIS makes use of a component dedicated to the analysis of the original binary code: it assumes that this code includes DWARF-2 information (i.e., has been compiled with the -gdwarf-2 option), and it captures the addresses for the events recorded by AssertionsToXML, to add them into the XML file. This software component is the only architecture-dependent module of OSIRIS. It has to be adapted in order to deal with different microprocessor architectures, but it only represents about 5% of the size of OSIRIS. Currently we have 3 versions: for Intel x86 32-bit and 64-bit, and for ARM Cortex-M4.

5. Future work

Experimental results have demonstrated that the CPU time overhead for the execution of the instrumented source remains limited (the assertion checkers are very efficient), but that it can become prohibitive for the binary surveillance solution, in particular when all the checkers are kept enabled all along the execution.

However this version is not likely to be kept as a definitive solution. It was developed as a first step towards an effective alternative to the source instrumentation. We plan to propose an instrumentation which would allow an efficient evaluation of the assertions. As pictured by Figure 4, the idea will be to have the assertion checkers as hardware components.

Figure 4: Monitoring with hardware assertion checkers

In a system on chip, they will enable to inspect the software under execution from a hardware block (not a software process like in Figure 3) which could be synthesized on an FPGA. In that context, notifications might be implemented by means of hardware signals like interrupts.

References
Hardware/Software dependability analysis from RT-Level descriptions

Key-words: dependability evaluation, fault injection, register criticality, high-level error models

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Cooperations: STMicroelectronics, LCIS, Ecole Nationale d'Ingénieurs de Sousse (ENISo, Tunisia)

Contracts: LIESSE (ANR)

Context and goals
Significant effort has been targeted since more than fifteen years on developing efficient techniques to analyse, at design time and early in the design flow, the functional consequences of soft errors. The goal is to precisely identify the soft errors leading to unacceptable application disturbances, in spite of all the possible masking effects due to the circuit architecture or to the application characteristics. Targets are mainly synchronous digital circuits. Most of the proposed techniques start from synthesizable RTL descriptions. Such descriptions are already close to the final hardware in terms of cycle accuracy and in terms of memory cells identification. Higher level descriptions may in some cases be used, with limited representation of soft error locations and reduced accuracy in terms of propagation analysis. Software is also taken into account in the case of systems based on microprocessors. Robustness evaluations may aim at (1) classifying the soft errors with respect to their functional impact, in order to compute derating factors on the application failure probability, (2) identifying error propagation paths, (3) identifying critical locations or registers, (4) ensure that a given set of behavioural properties always hold for a given set of soft errors (e.g., a given maximum multiplicity of erroneous bits). So-called fault injection techniques are used in most cases. For the latter case, the use of formal approaches had also been studied in collaboration with the former VDS group (today part of AMfoRS team) in order to avoid exhaustive fault injections, but with the classical limitations of formal techniques in terms of scalability. New techniques are today developed to improve or to avoid fault injections, without such limitations.

A whole set of techniques has therefore been developed to cover the wide range of analysis objectives and circuit characteristics.

Recent outcomes
The more recent fault injection platforms developed in the team are based on emulation and take advantage of the partial reconfiguration capabilities of some FPGAs. Maintaining such platforms is a permanent work. Improvements have been made in 2015 in order to make the approach freely available as scheduled in the LIESSE project supported by ANR. The last version of the platform is implemented on Xilinx Virtex 5 and has been called ATE-FIT5 for "AMfoRS' TIMA Emulation-based Fault Injection plaTform on Virtex-5". It allows designers to quickly implement an emulation-based fault injection campaign, either exhaustive or statistical, model-based (e.g., for a given multiplicity of bit-flips) or pattern-based (for a list of error patterns). The archive can be retrieved from [1] and includes the platform elements, documentation and a working example with tutorial. A new injection approach on Virtex 5 platforms has also been evaluated, partly in collaboration with A. Ammari, Assistant Professor at ENISo (Tunisia). The use of such platforms is discussed with several industrial partners, in two different contexts: evaluations with respect to natural disturbances (e.g., particles) and with respect to fault-based attacks on secure circuits.

In order to make fault injections more realistic in the context of laser-based attacks on secure circuits, work done in collaboration with LCIS laboratory led to the definition and validation of a multiple-bit error model, for focused (or "local") attack effects. This model is applied at RTL and exploits functional relations in order to estimate the physical proximity of different entities in the final circuit. Recent work was aimed at validating the high-level model with respect to actual representations of the placement of these entities within the circuit (i.e., the layout) [2, 3]. Figure 1 shows the coverage of the developed fault model with respect to a particular layout of an AES design: overall coverage is about 90%.

![Figure 1: Example of the RTL coverage with respect to the layout surface of an IC](image.png)
In parallel, a significant effort has been targeted towards new approaches, avoiding costly and time-consuming fault injections. It was demonstrated in 2014 that the dependability of software-based applications running on complex microprocessors can be accurately evaluated without resorting to fault injections. The approach was based on an executable model of the processor micro-architecture, allowing a software engineer to quickly evaluate the impact of any software modification on the lifetime of information actually handled within registers in the processor pipeline [4]. Critical registers could also be identified, taking into account the usage of resources for a given application. On-going work avoids the generation of such a micro-architectural model and can be applied directly on a synthesized circuit, leveraging the simulation environment developed for functional verification. The analysis tool developed in 2015 is currently being demonstrated on significant circuits, including crypto-processors and a microprocessor. The approach is based on analysing data lifetimes in digital circuit registers and achieves robustness evaluations with a precision comparable to statistical fault-injections and a speed even better than an emulation-based platform. The sensitivity of each register is evaluated with a precision sufficient to accurately identify the most critical ones.

References
Automatic Compilation of Properties into Synthesizable Designs

Key-words: Correct by construction, Assertion-Based Design (ABD), PSL

Members: N.Javaheri, K.Morin-Allory, D.Borrione

Declarative specifications are now widely adopted in the context of verification: declarative properties about the behavior of a design (Assertions) or its environment (Assumptions) are checked using dynamic or static verification tools. Once refined down to the register transfer level (RTL), a complete set of assertions unambiguously characterizes how a module reacts to signals sent to it, logically and temporally. Two languages have been standardized by IEEE to write assertions: Property Specification Language (PSL) and System Verilog Assertions (SVA). Many tools are now available to compile assertions into monitors, i.e. verification IP’s that check the design correctness, either by simulation or emulation.

Our current project considers the direct production of compliant control and communication modules from a set of assertions. A property is seen as the specification of the module to be designed, and we directly produce the synthesizable RTL design from its assertions. For each property, we obtain a compliant RTL component called reactant: its inputs and outputs are operands of the property, it reacts to the input values and produces output values so that the property holds.

This fast prototyping from assertions is not (yet) intended to replace manual design, the results are not currently competitive. Still, it may come early in the design flow, and resulting reactants can be used for:

- Replacing a nonavailable module by a fast prototype of it, to check a more comprehensive design.
- Replacing the (possibly very complex) environment of a designed module by a fast prototype of just the part of the environment that interacts with it.
- Debugging specifications by generating properties to be model-checked, during the compilation process.

Previously published works are based on automata and game theory. In contrast, our method is modular: it is based on the interconnection of primitive library modules for the logical and temporal operators of the property, according to its syntactic structure, a technology that we initially introduced to compile assertions into monitors (Horus). In the 2014 report, we illustrated the construction on the reactant for a property written in terms of temporal operators.

The achievement of 2015 was the extension of the method to SERE’s (sequential regular expressions) [2]. To our knowledge, this is an original feature, other authors only reported processing linear temporal operators.

Figure 1 shows the directed abstract syntax tree and Figure 2 gives the reactant for Property P2 defined in PSL as:

Property P2 is
always ({ q} |-> {a [ *6 ]; not a }; {a [ * ]; b });

Figure 1: Directed syntax tree for property P2

Figure 2: Reactant architecture for property P2

From each operator formal semantics, we defined a dependence relation between its operands, which expresses which operand may constrain the value of the other. The hardware interpretation of this relation is the foundation for our library of primitive reactants for the SERE operators. The approach derives from for the preceding development of the FL operators library [3].

In general, the specification has many properties, and a same variable may appear in several distinct properties. The originality of our approach is to avoid combining all the properties into one big automaton. Our method constructs the dependence between the design variables, and identifies which properties monitor a variable, and which properties generate its value. If a variable is an output for several reactants, these are combined with a solver to produce the final design.

SyntHorus-2 is the software prototype tool that implements these principles [1]. It takes as input the entity (interface) declaration of the specified module and a set of properties written in the simple subset of PSL, and produces a RTL design in the
The final circuit is constructed as the interconnection of the reactants for all the properties, together with solvers. It is a register transfer level model that is input to a conventional industrial synthesis tool to obtain the final implementation, either on FPGA or on an ASIC. Moreover, as an aid to specification debug, Synthorus-2 may generate a set of complementary properties to verify (by model checking) if the input set of properties are complete and consistent. Synthorus2 compiles several dozens properties in seconds, and produces a reasonably sized RTL circuit model. Experiments and performances are reported in [1, 3]

References
[1] Javaheri F.N., "Synthèse automatique de circuits numériques à partir de spécifications temporelles", PhD. Univ. Grenoble Alpes, October 1st, 2015 (in English)
Design of secured crypto-processors

Key-words: security, cryptographic systems, fault-based attacks, side-channel attacks, countermeasures

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Cooperations: STMicroelectronics, LIRMM, ENSMSE/CEA, Institut Fourier, Faculté des Sciences de Monastir (Tunisia), Univ. Massachusetts (USA), Univ; Assane Seck de Ziguinchor (Senegal)

Contracts: LIESSE (ANR), SCCyPhy (Labex Persyval-Lab, ANR), CRACL (Labex Persyval-Lab, ANR)

Context and goals
The current trend for many products, and in particular for consumer products, is toward an increasing need of security, in the form of confidentiality, data integrity, and/or authentication. These services rely on secure protocols and algorithms, which can be implemented in software or hardware according to the performance requirements, and to the cost constraints. Cryptography is at the heart of those systems. Many current secure implementations rely on specific hardware blocks to implement the main cryptographic functions. These functions can be tampered by various attacks, either active (fault-based attacks) or passive (side-channel attacks: computation time analysis, power analysis, observation of electromagnetic emissions…). So-called hardware attacks target the implementation rather than the algorithm itself and are today a significant threat for security, in addition to software- or network-based attacks.

The work done in the team aims at (1) better characterizing and modelling the effect of attacks, in particular fault-based attacks by various means, and (2) propose innovative countermeasures (i.e., protections) against the different types of attacks.

Our countermeasures are mainly implemented at RT-Level, even when targeting low-level characteristics such as power consumption analysis. A lot of work has been focused on the development and validation of robust re-usable cores (IPs) for cryptography. Previous and ongoing studies cover symmetric (mainly AES, but also PRESENT for lightweight implementations) and asymmetric (RSA, ECC) cryptosystems. Work is also on-going on hardware implementations for Full Homomorphic Encryption (FHE).

Recent outcomes
Part of the recent work has been focused on the development of cores for the widespread AES algorithm, taking into account various constraints from low- or medium-performance applications to highly demanding implementations for networking, and various types of attacks. Several AES crypto-processors have been manufactured by our partner STMicroelectronics in 28 nm bulk and FDSOI technologies, in the context of the LIESSE project supported by ANR. Laser attacks have been performed at ENSMSE in Gardanne in order to characterize the errors induced and derive a model that can be used for early evaluations at design time (see the section entitled "Hardware/Software dependability analysis from RT-Level descriptions"). Some results of the project have been published in [1]. Within the scope of the same project, a methodology for the development of a novel error detection scheme was presented in collaboration with LCIS, Valence. The methodology uses the information available through the above-cited model in order to protect independent functional blocks with error detecting codes. The work was applied to an AES design and protected by a parity code, where the check bits were defined with this approach [2]. Results have shown that after optimized synthesis, the area overhead was about 60%, while the error detection coverage with respect to the laser fault model was about 95%, performing much better than other comparable solutions. Higher coverage (99%) can be obtained at the cost of a higher overhead (80%).

The efficiency of the implemented countermeasures has also been analysed, in comparison with results obtained from RT-Level fault injections.

A significant part of the work in 2015 was targeted towards Elliptic Curve Cryptography (ECC) crypto-processors, on both attack and counter-measure sides.

We have designed and implemented an improved version of the windowing algorithm, where the size of each window used during the computation is randomly chosen at runtime. In order to protect also against timing attacks and to hide the size of the windows, dummy point additions are inserted randomly in the design. The number of operations is chosen in order to perform the same number of operations as in the worst case, i.e. choosing always the smallest possible window. The dummy operations can be inserted anytime.

This approach increases the number of ways by which the scalar coefficient can be partitioned, thus breaks synchronization of side-channel attacks. The approach has then been improved by inserting dummy doublings and starting with a...
pool of dummy operations in order to increase the uniformity of distribution [3, 4]. Work has also been done on the implementation of unified formulas (Jacobi Quartic Curve) and the practical evaluation of a new attack based on multiple horizontal power analysis. This work has been presented in [5] and results will be published in 2016. It is done in collaboration with Institut Fourier in the framework of the SCCyPHY team of Labex Persyval.

Another countermeasure has been evaluated against Simple Power Analysis for ECC, based on software functions run in parallel with the coprocessor executions. This countermeasure is well-suited to lightweight implementations e.g., in the context of the Internet-of-Things. Other works are on-going on lightweight implementations, and a collaboration started with Univ; Assane Seck de Ziguinchor (Senegal) with a 2-month visit in our team of one of their Assistant Professors.

Another part of our work was targeted towards the use of High Level Synthesis (HLS) for the complex case of large integer operations in asymmetric cryptography. This was applied to the scalar multiplication for ECC and work is on-going for polynomial multiplication in the context of FHE, targeting Cloud applications. Collaboration is on-going on this subject with Faculté des Sciences de Monastir (Tunisia) in the context of a co-advised PhD. FPGA implementations of polynomial multiplications for FHE have also been evaluated in collaboration with Institut Fourier in the framework of the CRACL project of Labex Persyval [6].

Figure 1 illustrates results obtained with HLS in the case of ECC. The tool used (AUGH) is developed at TIMA in the SLS team.

References

* LIRMM (Université Montpellier II /CNRS UMR 5506), Montpellier, France
** LCIS, France
*** ONERA, Toulouse, France
**** ENSMSE, Centre Microelectronique de Provence, France
***** STMicroelectronics, France


* IF, France
**RT-Level design for reliability/safety/availability and/or security**

**Key-words:** dependability improvement, control flow checking, behavioral checking

**Members:** R. Leveugle, L. Terras

**Cooperations:** STMicroelectronics, Dolphin Integration

**Contracts:** SPICA (FUI)

**Context and goals**
Protecting a design against natural perturbations or malicious attacks can be done at several levels. We mostly focus here on approaches that can be applied at RT-Level, therefore quite early in the design flow and easy to synthesize on several physical targets (several ASIC technologies, FPGAs ...). Previous studies also included operating systems or software modifications but we mainly focus here on hardware protection techniques. Some protections aim at improving reliability, safety and/or availability against natural perturbations (radiations, particles, electromagnetic fields) and other disturbances caused for example by process, voltage and temperature (PVT) variations. Some others are dedicated at improving security against malicious attacks, either passive (based on power or electromagnetic measures) or active (laser-, glitch- or electromagnetic-based perturbations). For protections dedicated to security, see the section entitled "Design of secured crypto-processors"; these aspects will not be developed in this section. We will focus in this part on approaches used for natural perturbations but that may also be used in a security context for fault-based attacks only.

**Recent outcomes**
Due to the increasing spatial multiplicity of error patterns, protecting a circuit with information redundancy is more and more difficult. This is particularly true when malicious attacks are concerned, but the problem exists also for natural perturbations. Another approach consists in using functional checks. In this context, we had proposed and demonstrated a new approach for microprocessor-based systems, called IDSM. This technique is non-intrusive and does not require a modification of the initial system. Checks include not only the control flow itself, but also the validity of operations and the integrity of critical data, with several possible trade-offs between overheads and error detection [1]. The approach allows checking not only the main application program, but also the boot phase and the calls to external functions, for which the source code is not available (e.g., pre-compiled library functions). No assumption is made on the error multiplicity. The approach is compatible with the norms requiring a complete separation between the nominal functions and the checking features (e.g., for automotive applications). Prototypes had been developed including (1) a specific watchdog processor (or infrastructure IP) and (2) development tools. The watchdog program was automatically generated at compile time by a modified version of the GCC compiler. Additional tools had been developed to cope with linkage constraints. A prototype had been demonstrated on the Leon3 processor [1]. Overheads are smaller than those induced by the classical lock-step duplication. Another advantage with respect to duplication is to ensure diversity, making successful malicious attacks much more difficult to achieve.

Work is on-going to transfer the principles of the approach on other processors. In 2015, after a first evaluation on a ARM core, the focus was put on a ST proprietary microprocessor. The approach has been revisited, taking the new micro-architectures as well as additional industrial constraints into account. Additional checks and new optimizations are currently studied for each particular requirement.

**References**
Test and diagnosis of new SRAM-based FPGA architectures

Key-words: Fault Tolerance, Reliability, FPGA, Test, Diagnosis, Mesh of clusters

Members: M. Benabdenbi, L. Anghel, S.-U. Rehman

Cooperations: LIP6, Telecom Paristech, FlexRAS (now Mentor Graphics)

Contracts: Robust FPGA (ANR)

Context and goals
The tremendous development of CMOS technology has enabled an increasing integration density. However, this trend of evolution is being slowed due to economic and physical limits. One particular key issue to focus on is the significant reduction in the manufacturing yield of new generation chips. At the same time, this yield loss induces more and more expensive manufacturing costs. This change brought a revolution in design practices. Designers should no longer think in terms of good and bad circuits after production testing. The challenge becomes to use a maximum of circuits while tolerating physical defects spread within them. The answer to this challenge will impact device models, architecture, dependability, safety and CAD tools.

In this context, the reconfigurable FPGA circuits are becoming increasingly popular because their performance and ability to integrate very complex applications have directly benefited from technological change. These circuits continuously increase their market share compared to ASICs. Thus, in the framework of a French National Research Project (ANR) called Robust FPGA, a design of a defect tolerant FPGA was developed. This project involved three major French laboratories: TIMA (Grenoble), LIP6 and Telecom-Paristech (Paris).

They combined their experience and expertise to explore new architectures for defect tolerant SRAM-based FPGA in deep submicron technology.

To achieve this, tools have been developed to enable the bypass of defective blocks and so enable implementation of applications on the defect-free blocks.

The project includes four main aspects:
1) Improving fault tolerance of FPGA by analyzing the robustness of the basic blocks.
2) Development of diagnostic/test methods for generating defective resource mapping
3) Development of a synthesis tool for FPGA fault tolerance
4) Development of tools for configuring the fault tolerant FPGA.

The scientific and technical benefits of this project are the development of innovative architectures, with the associated tools, for fault tolerant FPGAs with the introduction of the concept of synthesis for robustness. The benefits are numerous and involve both hardware and software aspects.

Test and Diagnosis Methodology
In this project, TIMA was mostly involved in the definition of the appropriate test and diagnosis methods of the new FPGA architectures.

Our approach mitigates permanent faults in FPGAs thanks to a combination of self-test, self-diagnosis, and defect-aware synthesis. In particular, we developed efficient self-test and diagnosis methods, which do not involve area cost for implementing dedicated built-in self-test (BIST) and built-in self-diagnosis (BISD) circuitry in the FPGA. Instead the regular resources of the FPGA are configured to implement the BIST and BISD blocks. Test and diagnosis is performed in several sessions. At each session, a region of the FPGA is selected to implement the BIST and BISD blocks, which perform the test and diagnosis of other regions of the FPGA. The regions configured into BIST and BISD blocks are tested in another session where new regions of the FPGA are configured to implement the BIST and BISD blocks. The BIST and BISD blocks are moved around the FPGA in order to test and diagnose all FPGA regions in a way that each region is tested and diagnosed several times in order to avoid fault masking.

The outcome of the test and diagnosis sessions is a map of defective blocks, which is used during the synthesis to map the application on fault-free blocks. This way faulty FPGAs can still be used, improving fabrication yield drastically.

To automate the use of this approach (figure 1), we have developed a set of tools, which translates the BIST algorithms into files acceptable by a non-commercial FPGA tool and integrate them into VTR-FPGA flow. VTR (Verilog-To-Routing) Project (11) is a reliable open source platform developed by multiple university research groups for FPGA research purposes.

To perform fault mapping and qualitative analysis, another set of tools were developed in order to plug into the commercial testability flow Synopsys TetraMAX®. The approach was applied to new FPGA architectures (figure 2) developed by the French startup FlexRAS Technologies (now Mentor Graphics) and the LIP6 laboratory.

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Different FPGA architectures were compared in terms of area, routability, fault masking, fault coverage, test time, power consumption, ... to select (i) the best architectural parameters leading to the best trade off and then (ii) study different hardened architectures to select the more “robust” one.

Table 1 Cluster Test Quality and Test time for different hardened architectures [3]

<table>
<thead>
<tr>
<th>Cluster architecture</th>
<th># test configurations</th>
<th>Max. fault coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>78</td>
<td>100%</td>
</tr>
<tr>
<td>With Fine Grain Redundancy</td>
<td>108</td>
<td>100%</td>
</tr>
<tr>
<td>With Distributed Feedback</td>
<td>88</td>
<td>100%</td>
</tr>
<tr>
<td>With Butterfly LUT</td>
<td>82</td>
<td>85.6%</td>
</tr>
</tbody>
</table>

References


[3] Saif Ur Rehman, Development of test and diagnosis techniques for a hierarchical mesh-based FPGA, PhD dissertation, 11/2015, Grenoble Institute of Technology
Early Digital System Failure Prediction due to Aging Induced Threats: Evaluation, Methodology of Implementation and Application Results

Key-words: Reliability, Aging, Performance Monitors, Aging Monitors, DVFS, AVS
Members: Lorena Anghel, Marine Saliva, Ahmed Benhassain, Ajith Sivadasan, Cheik Ndiaye
Cooperations: ST Microelectronics, Crolles
Contracts: theses CIFRE

Context and goals
With CMOS technology scaling, it becomes more and more difficult to guarantee circuit functionality for all process, voltage, temperature (PVT) corners. Moreover, circuit wear-out degradation lead to additional temporal variations, potentially resulting in timing and functional failures[1]. Under normal operation conditions, a transistor device can be affected by various aging effects such as Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB). Among the above mentioned aging phenomena, the NBTI impact on PMOSFETs as well as HCI impact have become the most critical reliability issues. Hence, accurate NBTI/HCI logic cells and design characterization are necessary for reliable digital circuit design. Accurate simulations with physical degradation models of the aging phenomena combined with silicon actual measures are necessary to better understand and assess the impact of aging on a complex digital design. As mentioned, these reliability threats can severely degrade the performance and in the worst case can provoke system failure, that can affect safety goals of specific reliable systems (automotive or health care embedded applications).

A conventional method handling such problems is to provide more safety margins (called guardband) in the circuit design phase. Adding pessimistic timing margin to guarantee all operating points under worse case conditions is no more acceptable due to the huge impact on design costs, such as up to 10% increase of slack time, with an upward trend as technology moves further.

Therefore the usage of in-situ monitors for pre-error detection becomes a must, as they allow decreasing the constraints imposed on the overall design. In addition to the reduction of design margin, adaptive voltage scaling (AVS) technique or Dynamic Voltage Frequency Scaling (DVFS) triggered by in-situ timing monitors may be used to reduce dynamically the frequency and the voltage according to the operating conditions and the application needs [1]. Thus, the performance degradation is compensated and the circuit’s lifetime can be extended.

Recent outcomes
In the framework of a long term on going collaboration between TIMA and ST Microelectronics several aspects have been tackled and arrived to some maturity in 2014-2015.

- Accurate BTI/HCI/TDDB impacts have been studied at circuit level for 28nm FDSOI technology digital cells. Dedicated test structures have been designed to track multiple BTI/HCI and oxide breakdown events and measure their real impact on logic gates performances and functionality. Different stress conditions were investigated to be closer to the operating conditions of a digital circuit (AC-DC effect, stress at low voltage, high gate oxide area, different temperatures, different input patterns). The measurements from dedicated test structures are scaled to device level measurements so as to propose a compact model that can be used further for predictive and quantitative simulations. This compact model applied to a logic cells path and the impact of aging threats in 28nm FDSOI technology has been analyzed. The results obtained were published in several conferences such as IEEE IRPS 2015 and DATE 2015 [5 and 6] and received the Best Paper Award of DATE 2015 conference [5].

- Pre-error detection In Situ Monitors are designed and inserted in digital designs. In Situ Monitors use a clocking double sampling method and they are placed in a feedback loop of the voltage regulation to provide global and within-the-die process, temperature and age compensation (figure 1) [4,5].

Figure 1a: In Situ Monitors with multiple timing windows
• Each sensor monitors detects potential induced delay faults on the paths sharing the same end at the expense of additional area and capacitive load applied on the path under test. The decision of placing these monitors on the right paths is not an easy task, as it can rapidly result in an explosion of the design area in addition to an increase of engineer efforts induced by the recursive place and route operations. Therefore, in 2014-2015 we have developed also an automatic methodology of placing the monitors by taking into account many tradeoffs and essential parameters such as workload, temperature, area and performance penalty have to be used [4].

• Further to that workload and temperature characterization of digital circuits using industry standard benchmarks can be performed to get an insight into the performance and energy characteristics of a given circuit. For embedded system applications, the workload may very well dictate different lifetime profile for a system considering the combination of BTI and HCI impact [2]. In 2015-2016 this work focused on the in-depth analysis of these influences over different workloads and temperatures and degradation of the critical paths has been observed. A top-down circuit activity and probability analysis was carried out leading to an accurate estimation of aging due to HCI and BTI of critical path elements at the design stage. A dedicated simulation flow is used from RTL simulation down to gate level cell timing analysis mapped onto 28nm FDSOI technology from STMicroelectronics. Through simulation results we show that the higher complexity of an execution program may not necessarily lead to a higher rate of degradation of the critical path considering that aging is primarily driven by the workload dependent activity and the probability of critical path combinational logic elements.

• Dynamic management of operating points parameters (Voltage and Frequency) by using In Situ Monitors feedback is demonstrated through post silicon measurements and more accurate data can be extracted. The effect of workload, monitor timing window and temperature degradations are analyzed depending on the supply voltage [3,4]. This data then can be used by higher level abstraction models to predict the lifetime of a complex circuit or a product.

References
Theme 2 / Design of Integrated devices
Circuits and Systems (CDSI)

Themes

MEMS microcomponents
- Microgenerators
- Acoustic microsensors
- Pressure microsensors
BIOMEMS microsystems
Asynchronous circuits and systems (asynchronous IP's, NoCs, GALS, etc…)
Non-uniform sampling and signal processing (algorithms, architectures, circuits)
Reconfigurable asynchronous Logic
Safe and secured robust asynchronous circuits
Smart CMOS vision sensors

Expertise

Scientific
Design, Modeling, Manufacturing and Characterization of MEMS
Modeling, simulation, verification, asynchronous digital and analog circuit synthesis
Fields of expertise
MEMS - Analytic modeling and finite elements
In-IC MEMS
Imagers design, asynchronous design tools, asynchronous systems design
Know-how
MEMS manufacturing in clean-rooms and by rapid prototyping
MEMS optical and electrical characterizations
Development of a logic-cells library, cameras for CMOS imagers, asynchronous circuits prototyping and manufacturing
Industrial transfer
2011: Creation of the UroMEMS company
2007 : Creation of the TIEMPO startup company

Research keywords

MEMS, Microsensors, Micro-energy, Micro-acoustics, BioMEMS
Asynchronous circuits and systems, CAD tools, CMOS imagers, non-uniformly sampled digital signal processing

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Micro Power Generators for Autonomous Microsystems

Key-words: Energy harvesting, Piezoelectric materials, Piezoelectric layers fabrication.


Cooperations: CEA – Leti, TRONICS, CEDRAT, EASii-IC, SORIN-CRM, Vermont, IEF, ESIEE-Paris, EPFL (Switzerland), ST Microelectronics

Contracts: Laureat (ANR 2014-17)

Energy harvesting has been the subject of intense research over the last decade. Various transduction principles have been presented as potential ways of scavenging the ambient energy (thermal, mechanical, radiative...) and transforming it into usable electrical energy. Among these principles, the piezoelectric transduction is probably the most studied one. The large-scale deployment of such devices will result in increased safety, lower maintenance costs and extended lifetime of autonomous sensors that are used in many application fields (medical implants, civilian and industrial structural health monitoring...).

Most of the approaches that we have studied so far were based on resonant piezoelectric devices which working frequencies are above 200Hz. The piezoelectric energy harvesters that we have proposed are currently at the state of the art.

However, while most of the piezoelectric vibration energy scavengers developed so far were designed to be effective at relatively high frequencies (above 200 Hz), we currently work on the development of energy harvesters designed to scavenge energy from real vibrational sources. Such a design must take into account a wide-band spectral content of a source acceleration centered in a frequency band not exceeding 100 Hz. The dimensional aspects as the geometry and the volume as well as the energy requirements are important constraints and play role in the design strategy.

In the following paragraphs, we will describe the simulation, fabrication and characterization of piezoelectric energy harvesters for three different applications.

1. Heart Beat Scavenging

Current version of implantable cardioverter defibrillators (ICDs) and pacemakers consists of a battery-powered pulse generator connected onto the heart through electrical leads inserted through veins. However, it is known that the long-term lead failure may occur and can cause the device dysfunction. When required, the removal of failed leads is a complex procedure associated with a potential risk of mortality.

As a consequence, main actors in the field of cardiac rhythm management (CRM) implants prepare miniaturized and autonomous leadless implants, which could be directly placed inside a human heart.

The idea of a stand-alone cardiac implant is not new and several approaches for powering the device have been suggested. More recently, researchers from University of Michigan, Ann Arbor, USA presented simulation results of a piezoelectric energy harvester operating at 40Hz that could in theory power a cardiac implant with heart-induced vibrations. Our colleagues from the Sorin and the CEA/Léti have obtained the heart acceleration spectrum by placing accelerometers inside several heart cavities. It appears that the heart vibration energy is rather localized at lower frequencies in a frequency band from 5 to 30 Hz.

We have obtained significant results during the HBS project (FUI 2010-13) that aimed at developing the technology of leadless pacemakers. The project gathered experiences from the industry (Sorin, EasiiIC, Cedrat, Tronics) together with the CEA-Léti and the TIMA laboratory. The TIMA laboratory was in charge of the design, fabrication and experimental characterization of a piezoelectric energy harvester prototype operating at very low frequency range (20 to 30 Hz). The device, in its final application, will be excited by the heartbeats and will make part of a new generation of pacemakers. The studied device is beam-like harvester made of two lead zirconate titanate (PZT) thick films assembled in bimorph configuration with dimensions chosen in a way to achieve the resonance in the required frequency range. At the same time, constraints applied on dimensions and generated power must be satisfied.

Heart acceleration signals have been first measured experimentally by placing a 3D accelerometer on heart muscles of both animals and human patients. The spectral content of these signals was studied and the energy distribution of these quasi-periodic signals has been analyzed.
Given the volume of the leadless pacemaker, we have shown that the PZT layers must be 60 to 65 µm thick in order to both comply with the energy source frequency and the heart stimulation energy requirements. However, it appears that none of current fabrication processes can be used for manufacturing such thick PZT films. Using processes derived from the microelectronic field such as Sol Gel deposition or sputtering, the maximum achievable thickness is about 2-5 µm. In contrary, using co-firing techniques, the PZT plates can hardly be thinner than 100 µm. The manufacturing of above described piezoelectric scavenger corresponds to an actual process blind window. As a consequence, we work on the implementation of fabrication processes of PZT thick films. We focus on the optimized grinding and polishing techniques of bulk ceramics.

After the proof-of-concept of a scaled-up demonstrator of the scavenger operating at 15 Hz, a new device taking into account the geometrical constrains of the real heart ambient has been fabricated and tested. The prototype (Figure 1) is composed of 2 piezoelectric layers, 60 µm thick, having opposite polarization directions. The layers are attached on a brass shim 12 µm thick. The tungsten mass design has been optimized to a cylindrical shape to allow the maximal displacement in the capsule.

Finite elements simulations in ANSYS are used to predict a resonant frequency, maximal stress level in the beam and an output power with an optimal load resistance under a harmonic acceleration and a real signal sequence. The characterization of the structure shows a good agreement with the simulation.

![Figure 1: Photograph of the fabricated cantilever scavenger mounted in the test clamping element](image)

The electrical performances of such devices are among the best published in the literature.

2. Micro Thermal Energy Harvester

The aim of this project is to conceive a micro energy harvester able to convert a thermal spatial gradient into usable electrical energy. The transduction is performed in two steps: a first thermo-mechanical conversion transforms the thermal energy into large mechanical displacement, followed by the second piezoelectric transduction that converts the mechanical displacements into electrical charges. In order to obtain large displacements, the initially curved-down structure is made of two layers with materials having a huge thermal expansion coefficient mismatch. The thermal stresses induced by contacting a hot source are causing a buckling of the clamped-clamped bilayer beam. Once buckled upward, the device is cooled down by convection and buckles down to its initial position, in contact with the hot source. A first macro-prototype has shown promising results and a model predicted an increase of the output power with the downsizing of the device.

Micro prototypes made of aluminum nitride (AlN) and aluminum (Al) have been fabricated using standard CMOS processes in a cleanroom (EPFL). The devices are electrically characterized in TIMA. A new setup has been built in order to push mechanically the structure from the backside and initiate the buckling in order to remove the thermal contribution of a final excitation method. An insulating glass tip is mounted on a multilayer stack of piezoelectric material that delivers a defined displacement at a precise frequency to the device. The displacement applied on the structure can then be increased progressively in a way to obtain initially only linear electrical response and then, after reaching a threshold displacement, a peak corresponding to the buckling. As the device is in an unstable position in its buckled state, it is coming back to its original position instantaneously. A power density of 48 nW.cm⁻² is obtained for a 1400 x 700 µm² structure with 0.5 µm of AlN and 0.5 µm of Al.

Finally, the prototypes were tested with a thermal actuation. The wafer was placed on a hot plate, whose surface temperature was measured by a thermocouple. By conduction through the silicon wafer, the bilayers were heated up and the same structure tested mechanically before buckled up at 114 °C. Then the hot plate is switched off and the device buckled down at 82 °C. The energy furnished during the buckling is estimated at 30 pJ.cm⁻².

The next step is to improve the setup by including a precise measurement of the temperature on the device and not on the hotplate surface, and also by implementing a faster thermal cycling allowing an estimation of the possible power that could be harvested by the structure in the final application.

3. Design of a thermo-magnetically triggered piezoelectric generator

The goal of this research is to design a thermo-magnetically triggered generator able to convert
small ambient temperature variations into electrical energy that will be usable to power wireless sensors. The energy harvester is composed of two main sections: the energy generator and the triggering system. On the one hand, the energy generator is based of a cantilever beam made of a piezoceramic material such as PSI5A4E. On the other hand, the triggering system consists of a magnetic circuit built of a hard permanent magnet (NdFeB) and a soft magnetic material such as the FeNi alloy. The principle of operation of our energy harvester relies on the vibration-to-electricity energy conversion by means of a piezoelectric transduction. In contrast to most classical solutions for vibration energy harvesters, which use mechanical vibrations as excitation source, we propose a new approach based on thermo-magnetic hybridization in order to use thermal changing as excitation source. The energy harvester has two position of stability, the closed one and the open one. Variations of ambient temperature trigger the switching between these two positions. At low temperatures, the hard magnet exerts an attraction force over the soft magnetic material, which is attached to the free end of the beam; causing a beam deflection. Inversely, at high temperatures, the soft magnetic material turns into paramagnetic, thus the attraction force decreases, resulting in the structure release. Figure 2 shows a schematic view of the piezoelectric generator and its two main components.

Figure 2: Schematic view of thermo-magnetically triggered piezoelectric generator and its two operation positions.

Currently, experimental tests are being performed of first prototypes showing valuable insights of the performance of energy harvester and its design methodology. Future work includes optimization and design of a circuit for electrical energy management.

References

Microsystems for Health

Key-words: Urinary sphincter, Medical needle, piezoresistive microgauges.

Members: S. Basrour, A. Bonvilain, L. Rufer, T. Le Pelletter, Aïteb Naimi, Ismail Bouhadda

Cooperations: UroMEMS, IMACTIS, CHU Grenoble, TIMC-IMAG, SIMaP,

Contracts: GAME_D (ANR 2013-2016)

1. Artificial Urinary Sphincter

This work is performed in collaboration with TIMC-IMAG laboratory, an urologist physician at la Pitié Salpêtrière hospital in Paris and the start-up UroMems. It proposes to solve the problem of urinary incontinence with a new adaptive autonomous artificial urinary sphincter.

Urinary incontinence is defined as the involuntary leakage of urine and there are several surgical methods to alleviate it. In the event of a major leak, the establishment of an artificial urinary sphincter can give patients a normal social life. Nowadays, there is only the prosthesis developed by the American Medical System Company (Figure 1 left), which remedies to severe incontinence.

Our work aim for replacing the manual pump mechanism used by many patients worldwide by a mechatronics implanted device.

The prototype developed is shown on Figure 1 (right). In this work, we propose a study on a dynamic control of the system, which improves its efficiency, by adjusting the behavior of the system to the patient and his lifestyle. We developed also a communication between the implant and the outside world via a RF link.

Some measurements are performed on the patient with microsensors. We extract various relevant information to adapt the occlusive pressure of the artificial urinary sphincter. The detection algorithm designed to be implemented in the artificial urinary sphincter is then established.

Finally we have designed and tested the prototype of the artificial urinary sphincter. The mechatronic system and the functionality of the device are then evaluated and validated, first in vitro, and then in vivo.

Nowadays, we work to minimize energy consumption to provide greater autonomy to the implant. Different ways are explored like the optimization of algorithms, of the signal data processing [1], and of the actuation.

2. Deformation measurements of a cylinder: particular case of a medical needle

This work is performed in collaboration with TIMC-IMAG laboratory, Grenoble Hospital and Imactis enterprise. It proposes to solve the problem of knowing the precise position of the tip of a flexible cylinder inserted in a non-transparent environment.

Percutaneous medical procedures for diagnosis or therapeutics, guided or not by imaging (ultrasound, fluoroscopy imaging, magnetic resonance imaging, etc.) aim at introducing, through the skin, an instrument to a previously identified target. However, the path of the instrument can be deviated by an obstacle (because of the inhomogeneity of human tissues).

To facilitate the implementation of these procedures, tools for tracking and navigation were specifically developed.

While these tools have really helped to revolutionize medical practices, they suffer from several limitations, among which two are specifically identified: the cost and the assumption of the dimensional stability of the instrument used. Indeed, the interaction of a deformable instrument with the human tissue is a source of its deformations, which can cause a failure of interventional medical procedure.

This work is focused on the integration of microsensors (piezoresistive microgauges) on the deformable tool to allow the real time monitoring of its deformations.
We first conducted a feasibility study by developing a macroscopic prototype consisting in a medical needle on which we manually glued commercial gauges. Experiments of this first prototype have allowed us to validate the analytical and numerical models.

In the next step, we aimed to integrate piezoresistive micro-gauges directly on the body of the needle. The challenge of this step consists in a micro-fabrication process that has to be performed on an unconventional substrate (in terms of form (curved) and material (stainless steel)) corresponding to a needle surface.

We determine the dimensions and the constitution of the germanium piezoresistive microgauges with the help of the previous analytical and numerical modeling. Then we developed the microfabrication process of the microgauges on the needles.

With these results (Figure 2), we have shown that it is possible to integrate microsensors on the body of the needle. These works will open a new way of monitoring deformable tools inserted in a non-transparent environment.

![Figure 2: Microgauges: a) on steel needle, and b) on NiTi needle.](image)

We have then begun to test these new microsensors after doing a bonding connection. The experimentations consist in making a controlled deflection to the tip of the needle, and to measure the variation of the resistance of the microsensor. The first results show five straight trajectories (6 mm) of the tip of the needle (3 mm on each side from the non deformed position). Thirteen measured points are defined. Several microgauges are already experimented in the same conditions (about 40), and the results are similar. So we can deduce that we have a good repeatability of the measures [2-5].

We can after calculate the experimental gauge factor (GF) of the microsensor. For the different experimented microgauges, we find a GF around 3. The theoretical one was about 45, so it is not as high as expected. This difference can be explained essentially by three reasons:
- the PI factor is not well known,
- the resistivity of the poly-Ge seems to be not homogeneous on the entire surface,
- all of the parameters of the crystallization of the Ge are also not well known.

So we have worked with SIMaP laboratory which is expert in materials, and we have determined the three most important parameters of the MIC (Metal Induced Crystallization): the thickness of the metal layer, the annealing temperature and the duration of the annealing.

Nowadays, we have improved the microfabrication process, and integrated the connections of the microgauges at the end of the needle (Figure 3). We are close to get a working prototype for experimentations.

![Figure 3: the geometry of the microgauges on a needle with their connections.](image)

References
[1] Giuseppe Roa, Tugdual Le Pelleter, Agnes Bonvilain, Alejandro Chagoya, Laurent Fesquet ; “Designing ultra-low power systems with non-uniform sampling and event-driven logic” ; SBCCI ; September 2014 ; Aracaju, Brazil.
[3] Aïteb Naimi, Agnès Bonvilain ; “Expérimentations de microgauges de déformation réalisées par microfabrication sur des aiguilles médicales ” ; JNRDM ; May 2014 ; Lille.
Design and Technologies for Integrated Micro and Nano Systems

Key-words: Acoustics, CMOS-MEMS, Ultrasound, Piezo-MEMS, Piezo-electret


Cooperations: STMicroelectronics, LMFA (Lyon), LIRMM (Montpellier), Hong Kong University of Science and Technology, EP- USP (Brazil), INRIA (Lille), Université de Lille 1, CEA Léti, AlphaUI, Orange Labs, EASII IC, LMOP (Tunis, Tunisia), Politecnico di Torino (Italy)


1. CMOS-MEMS for acoustics

A successful design of an efficient source generating acoustic pressure in the air by means of vibrating diaphragm must maximize the product of the diaphragm area, its vibrational velocity and frequency. Such a condition limits the exploitation of MEMS-based devices as acoustic sources, in particular in low frequency range, to in-ear or similar applications generating low power signals in closed couplers.

Various approaches to the acoustic generation in air with MEMS use magnetic or piezoelectric materials. Their principal disadvantage is the need to integrate a material that is not a part of a CMOS fabrication process. Another approach consists in digital sound reconstruction involving the summation of discrete acoustic pulses generated by individual acoustic transducers arranged in a matrix and operating in a binary way. Others presented such a digital speaker in a configuration using a capacitive principle.

Recently, different works showing the feasibility of MEMS using CMOS technology followed by surface micromachining without mask have been published. Unlike the older approach, where suspended MEMS components were obtained by silicon substrate etching, the proposed technology consists in etching oxide layers resulting from the CMOS process and thus releasing metallic layers of the same CMOS technology. Until now, various applications of this technology were reported and only few of them treat acoustic sources [1].

We show that the industrial 0.35µm CMOS technology can be considered also for sources of airborne acoustic signals. The ultimate goal is the monolithic integration of a device working both as a source and a sensor with electronics, thus facilitating signal routing, suppressing parasitic effects, and improving the signal-to-noise ratio. The acoustic source fabrication is based on AMS 0.35µm CMOS back-end process consisting in the silicon dioxide sacrificial layer removal by hydrofluoric acid (Silox Vapox III) wet etching. The electrostatic transducer structure (Fig. 1.) is composed of a squared perforated diaphragm (500 x 500 x 0.925 µm³) and a solid back plate, formed by CMOS metallic layers, separated by an air gap (2.64 µm). The holes size (5 µm) and position on the diaphragm have been chosen to allow a sacrificial layer etching and to avoid an excessive damping due to the air gap. The diaphragm is anchored, through vias.

![Figure 1: Schematics of the CMOS-MEMS acoustic source structure.](image)

We have performed the finite element modeling of the acoustic source and the fabrication of the device in the AMS 0.35µm CMOS technology backed-up with a post-CMOS etch followed by the device characterization.

The acoustic source was characterized with acoustic measurement chain (microphone B&K 4939, lock-in amplifier Zurich Instruments HF2LI). The preliminary results of the acoustic pressure generated by the MEMS device at a distance of 10mm are shown in Fig. 2.

![Figure 2: Frequency response of the CMOS-MEMS acoustic source](image)
2. Haptic Interface

Most of the available technological consumer objects neglect the sense of touch. Yet, this sense is one of the most important for human beings. The project called Touch-It plans to design a new haptic interface (i.e., an interface that allow a tactile feedback for the user) that could be implemented on every kind of existing tactile screens, from mobile phones to laptops, or remote controls.

The existing technologies concerning these applications present several drawbacks, among them the disappointing fineness of the texture, the relatively large electrical consumption (more than 600 mW), which is crippling for mobile applications, the low system integration, with a dedicated and bulky packaging.

Considering this, the project proposes an integrated solution using thin film piezoelectric actuators creating a squeeze film effect on the surface. This device allows a fine texture rendering by changing the friction coefficient.

The project is focused on five major aspects: transparency, electrical consumption reduction, integration, design of new applications and cost reduction. TIMA is supporting the fabrication of the actuators by the design and modeling.

TIMA proposed a whole finite elements study of the design of the actuators, taking into account the different materials, from silicon devices to glass applications, and geometries. We also set up a characterization bench using a velocimeter to measure the displacement amplitude of the mechanical vibrations. A retrofit of the measured devices has been made, showing a good agreement with finite elements results. The next step, which is aiming smartphones screens, is anticipated, and some issues were already solved.

The integration into mobile devices is the biggest challenge of this project. This involves a reduction of the power consumption for the actuation. Based on physical equations, an equivalent model of the vibration slab has been generated. Knowing the different parameter of the entire system, the vibration frequency can be adjusted to provide the best highest electro-mechanical transduction.

Thanks to piezoelectric transducers leaded as sensors, the equivalent model is integrated into the sensor detection in order to reduce the time of frequency adaptation.

A study on those sensors has been made. Fig 3 shows a glass slab with piezoelectric transducers made of thin AlN layer. A characterization of the best position providing the highest feedback signal has been carried-out [2]. A latency time of the entire feedback loop has been established and is compatible with the haptic rendering.

![Figure 3: 110x65 mm² glass slab with AlN transducers](image)

3. Polymer-based piezo-electret structures

The energy harvesting of the mechanical vibrations existing in our daily life can be a potential source to provide electrical energy for autonomous devices. We are based on the conversion via piezoelectric samples. However, these materials should exhibit a compromise between a very low Young’s modulus to be suitable for its integration as wearable devices adapted for any shape and size surfaces and having very low dielectric losses. For these reasons, we developed a novel micro-structured material made from PDMS referred as piezo-electret material. Piezo-electret PDMS exhibits piezoelectric effect in its actuator and sensor mode. This effect arises from their anisotropic structures. In fact, they are polymer matrix containing micro-cavities trapping air (Figure 4). The ionization of the air generate opposite charges that are implanted in the inner micro-cavities surfaces, each micro-cavity is considered as a macro-dipole. The macroscopic dipole moment is determined by the quantity of the charges and the distance between the separated charges. So, piezo-electret is sensitive to any external mechanical or electrical stress. In fact, if an external mechanical load compresses piezo-electret, the distance between opposite charges decreases and compensating charge distribution is generated in conductive electrodes. But, in the case of external applied ac-voltage, piezo-electret vibrates periodically. Due to these piezoelectric like effect of piezo-electrets and their low Young’s modulus, they can be utilized as functional materials in electromechanical micro-sensors.

![Figure 4: Schematic illustration of the micro-structured PDMS material with top and bottom gold electrodes](image)
1 μW.mm⁻³ for a moderate dynamic pressure of 120 Pa at 20Hz.

References
Team 3 / Robust Integrated Systems (RIS)

Themes

Robust massively parallel single-chip architectures
Power management from the OS down to silicon
Fault tolerant and self-adaptative architectures
3D NOC Robust Architectures
Design in Reliability face to aging, process variation and soft errors
Evaluation of robustness and qualification : radiation testings, fault injection
Architectures for Nanotechnologies

Expertise

Fields of expertise
Design for Reliability, Design for Test, Self-Repair, Fault-tolerance, Design for Soft-Error Mitigation: Methodologies, Tools and Architectures

Know-how
Multilevel platforms for fault simulation and robustness automatic insertion at several abstraction levels; 3D integration solutions
test platform for radiation faults measurement ; SEE error-rate prediction of circuits and systems

Research keywords
Fault tolerance, multi-core systems robustness, 3D circuits, aging, fault-injection

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The Cells Framework: Overall Description

Members: Michael Nicolaidis, Nacer-Eddine Zergainoh, Thierry Bonnoit, Amir Charif, Fraidy Bouesse, Michael Dimopoulos, Panagiota Papavramidou

Keywords: Ultimate CMOS and post-CMOS technologies, high defect densities, reliability, yield, low-power, massively parallel single-chip tera-device computers,

Cooperation: STmicroelectronics, iRoC, Atmel

Contracts: ELESIS, RESIST

Ultimate-CMOS and post-CMOS technologies promise integrating trillions devices in a single die, leading to single-chip massively parallel architectures comprising thousands interconnected processors, and enabling the next computation turn. But the aggressive technology scaling that paves the way to the ultimate CMOS nodes has dramatic impact to: process, voltage and temperature (PVT) variations; sensitivity to electromagnetic interferences (EMI), to atmospheric radiation (neutrons and protons) and to alpha particles; and circuit aging. It also imposes stringent power dissipation constraints. The resulting high defect levels, heterogeneous behavior of identical circuits, accelerated circuit degradation over time, and extreme complexity, affect adversely fabrication yield and/or prevent fabricating reliable chips in ultimate CMOS and post-CMOS technologies. These issues are becoming the main show-stoppers in the path leading to these technologies.

The Cells framework addresses the severe issues related to the design of massively parallel tera-device processors affected by high defect densities, in which we severe issues have to be addressed such us:

- After fabrication, all processing and routing nodes may be affected by some temporary faults such as delay faults, or clock skews.
- Fabrication faults altering persistently the circuit behavior may massively affect one or more regular blocks (RAMs, FIFOs, buses) in a large fraction of nodes. Such faults may also very frequently occur during product life.
- Fabrication faults altering persistently the behavior of irregular blocks (thus difficult to repair) may affect a significant portion of nodes. Such faults may also frequently occur during circuit life (e.g. every few days), and thus during application execution.
- New timing faults induced by circuit aging, as well as soft errors (SEUs and transients) may frequently occur during circuit life (and thus during application execution).
- Circuit degradation is continuous and requires continuous self-regulation of circuit parameters (clock-frequency, voltage levels, body bias), to maintain operational each processor node.

Clearly, no existing solution can cope with such massively defective systems, which invalidate even massive redundancy schemes (e.g. duplication, TMR), as all replicated parts may be defective. Such schemes also induce high area and power penalties.

Some approaches targeting the design of reliable single-chip massively parallel processors avoids massive redundancy by using self-tests (hardware implemented or software implemented to detect failures and create routing tables that are used subsequently to avoid failed processing nodes or failed routes. However, such approaches could not cope with the issues affecting ultimate CMOS and post CMOS technologies as:

- In highly defective technologies, the vast majority of nodes (processing elements and routers) may include one or another kind of faults (e.g. timing faults produced by process, voltage and temperature variations, EMI, or aging). Thus, declaring defective the nodes affected by any kind of faults will quickly waste the computational resources of the chip.
- Achieving high fault coverage for timing faults is very difficult. Thus, many of these faults may escape fabrication test and also periodic self-tests and produce run-time errors.
- Faults occurring during application execution can not be covered by self-tests.

In this project we develop a comprehensive approach enabling using in efficient and reliable manner all parts able to perform useful computations.

The Cells framework (On-Chip Self-healing Tera-Device Processors) [1-2] comprises several techniques spanning at all levels of the system: circuit, processor/architectural, array/routing, task-scheduling/allocation. Innovations are introduced at all levels of this framework, including its overall architecture, its particular components, and the way the cooperation of these components is architected to optimize the outcome. Developments concerning some of these components are presented in the next sections.

References

Publications on the Overall Cells Framework


Recent Publications on Cells’ Components


Early Publications on Cells’ Components


In massively parallel processor chips, a possible (and rather straightforward) approach may consist in exploiting the existence of large numbers of processing cores to implement fault tolerance, by using two processor cores to duplicated the execution of each task and comparing their outcome to detect errors (double modular redundancy-DMR), or by using three processor cores to triplicate the execution of each task and voting their outcome to correct errors (triple modular redundancy-TMR). These approaches have two major flaws: drastic decrease of processing power, and drastic increase of energy dissipation per task. Similarly, software implemented fault-tolerance drastically impacts performance and power, as it replicates the execution of each task. Hence, a breakthrough in fault-tolerant design is required for reducing drastically performance and energy dissipation penalties, and improve reliability.

Such a breakthrough was achieved by a scheme (referred hereafter as double-sampling) we proposed in reference [1] and evaluated in [2]. This scheme reduces drastically hardware and power costs, by avoiding both hardware replication and operations replication. Instead, to check the correctness of an output signal of a logic block; this scheme observes this signal at two different instants, by adding a redundant latch and driving it by means of a delayed clock signal (Figure 1a). This scheme was later extended in the RAZOR architecture [3] to also perform error correction: upon error detection Razor used the contents of the redundant latch to replace the contents of the functional flip-flop (Figure 1b). Reference [3] demonstrated that this scheme can achieve drastic power reduction, by reducing the supply voltage to very low levels and using RAZOR to detect and correct the timing errors induced by this reduction.

While the double-sampling scheme reduces drastically the area and power cost with respect to traditional fault-tolerant schemes, some area and power penalties are still introduced due to the redundant latches. Furthermore it suffers from two drawbacks:

- To avoid false alarms and miss-corrections, the path delays of the combinational circuits signals checked by the schemes in figure 1, must exceed the delay δ of the delayed clock. To ensure this constraint, buffers should be needed in the paths with delays shorter than δ, inducing no negligible area and power cost.
- Also, due to this issue, to avoid significant area and power penalties, we have to use moderate values for δ, limiting the duration of detectable faults.

**GRAAL ARCHITECTURE**

One goal of Cells is to explore new fault tolerant architectures that are exempt of the above problems. These problems are due to the fact that all the stages of a FF-based design compute at the same time. This leaves short stability time to the combinational circuit outputs that we could exploit for error checking. In flip-flops, when the master latch is transparent, the slave is on memorization and vice versa. Thus, if we transform a flip-flop-based design (Figure 2a), into its equivalent latch-based design, by moving the slave latches of the FFs to the middle of the combinational circuits, (as shown in Figure 2b where Ck and Ck of the FFs are replaced by non-overlapping clocks Φ1 and Φ2), we obtain a design that can work at the same clock frequency as the original one. In addition, the master
and slave latches operate at different phases. Then, the outputs of any combinational block (inputs of latches), are stable during the period in which its adjacent blocks are in computation. Thus, we can compare the outputs of the latches against their inputs to detect timing and transient faults of large duration, according to the GRAAL architecture (Figure 3) that we have introduced few years ago.

This scheme also detects SEUs as well as all kinds of latch faults (transition faults, retention faults). Thorough analysis shows that GRAAL detects delay faults with duration up to 100% of the circuit delays without imposing short path constraints. Thus, it offers comfortable timing margins that can be employed for detecting large delay faults, and at the same time reduce power dissipation by using the idea introduced by the University of Illinois (reduce Vdd and detect and correct induced timing errors). Note that, fault multiplicity is not an issue for GRAAL. Faults of any multiplicity are detected as far as their duration does not exceed this value. GRAAL also tolerates clock skews of up to 25% of the clock period, as an inherent property of latch-based designs. In addition, we show that larger clock skews that are not tolerated are always detected (thus they are recoverable by using instruction replay).

Our GRAAL architecture can be implemented in two ways. The one version uses redundant latches, which introduce non-negligible area and power penalties. Recently this first version of our GRAAL architecture was used by others in the so-called Bubble Razor implementation. The second version of GRAAL architecture is much more efficient as it does not use of redundant latches. Only a two-input XOR gate is added to each latch to compare its inputs against to its outputs. Thus, this version of GRAAL induces drastically lower area and power penalties with respect to any known error detection scheme.

Table 1 shows the evaluation results of the GRAAL architecture. These results are based on the implementation of GRAAL in the icyflex processor from CSEM [4][5], in ST Microelectronics 40nm technology. In order for the comparisons to be consistent, all implementations of icyflex, shown in table 1, were synthesized for the same clock frequency. Thus, the 150MHz clock frequency suggested by CSEM was selected for all these implementations.

Latch-based designs can be synthesized with or without time borrowing, and the synthesis was done by means of the Design Compiler [6], which supports latch-based design for both cases. Latch-based designs can be synthesized with or without time borrowing, and the synthesis was done by means of the Design Compiler [6], which supports latch-based design for both cases. The maximum duration of detectable faults is achieved by GRAAL when no time borrowing is used. Thus, no-time borrowing has been first selected for achieving the highest possible reliability.

### Table 1: GRAAL evaluation

<table>
<thead>
<tr>
<th>icyflex2 Implementations</th>
<th>Reference Latch no-time Borrowing</th>
<th>Latch GRAAL A no-time Borrowing</th>
<th>Flip-Flop</th>
<th>Latch Time Borrowing</th>
<th>Latch GRAAL B Time Borrowing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Library</td>
<td>1.10V</td>
<td>1.10V</td>
<td>1.10V</td>
<td>0.90V</td>
<td>0.90V</td>
</tr>
<tr>
<td>Area</td>
<td>100%</td>
<td>103.60%</td>
<td>92.72%</td>
<td>100.98%</td>
<td>108.16%</td>
</tr>
<tr>
<td>Power</td>
<td>100%</td>
<td>103.95%</td>
<td>156.7%</td>
<td>64.52%</td>
<td>70.81%</td>
</tr>
<tr>
<td>Duration Detectable Faults</td>
<td>—</td>
<td>100% path delay</td>
<td>—</td>
<td>—</td>
<td>72.4%</td>
</tr>
</tbody>
</table>

### No time borrowing implementation

For comparison purposes, we use “Reference” version, which is the unprotected icyflex version, synthesized without time borrowing by using a cell library targeting 1.10V supply voltage. The area and power of the “Reference” version are given in normalized terms (100% area and 100% power) in column 2 of table 1.

Column 3 shows the results for the GRAAL implementation, using the same cell library and no time-borrowing. We observe that this implementation achieves detection of faults that increase by 100% the delay of the affected path. This duration is very high and is achieved by means of very low cost (3.06% area and 3.95% power cost). Thus GRAAL architecture can achieve very high reliability in future highly defective technologies that could increase dramatically PVT (process, voltage, and temperature) variations, and circuit aging, due to a very aggressive reduction of device geometries. Thus, GRAAL is very suitable for the Cells framework.

To validate the efficiency of GRAAL also with respect to flip-flop based design, column 4 shows the area and power of the flip-flop implementation of icyflex, using
the same cell library and targeting the same clock frequency (150 MHz). We observe that, the flip-flop version requires 7.28% less area with respect to the “Reference” latch-based version, but much larger power (56.77%). Thus, the GRAAL no-time borrowing implementation achieves its high fault detection efficiency (faults that increase by 100% the delay of the affected paths) at a 11.73% area cost with respect to the unprotected flip-flop-based implementation, but at much lower power (33.66% less than the unprotected flip-flop-based implementation).

No time borrowing implementation
The implementation presented in the previous section does not use time borrowing and achieves the highest robustness, as faults of very high duration are detected (i.e. faults of so large duration that may duplicate the delay of the affected path). Note that the detection of faults of high duration can also be exploited for reducing power dissipation, by aggressively reducing the supply voltage level, and using GRAAL to detect and recover the resulting timing errors. However, a more efficient approach consists in using combining GRAAL with time borrowing.

To reduce power, we used the TT/0.90V/125°C cell library, which is designed for 0.90V supply voltage. However, as the delays of this cell library are higher than the delays of TT/1.10V/125°C*, achieving operation at 150 MHz will impact power dissipation and reduce the gains achieved by the reduction of supply voltage. Thus, to maximize the power reduction, we used the Design Compiler to synthesize the time-borrowing version of icyflex2 for the TT/0.90V/125°C.

Column 5 in table 1 shows the results of the unprotected version of icyflex2 using this cell library and time borrowing, and targeting 150MHz clock frequency. This version requires 0.98% more area with respect to the “Reference” version of column 2, and reduces power by 35.48%.

Column 6 in table 1 shows the results concerning the GRAAL version of the time-borrowing implementation of icyflex2, for the same cell library and clock frequency. This version detects faults of duration up to 72.4% of the delay of the path affected by the fault. Thus, the GRAAL architecture detects faults of very large duration, even for time borrowing implementations. This significant advantage is achieved at the small cost of 7.18% more area and 6.29% more power with respect to the unprotected time borrowing implementation of column 5. In comparison with the unprotected flip-flop implementation, this high detection efficiency is achieved at the cost of 16% more area and at the drastic advantage of 45.19% less power. Hence, the combination of GRAAL with time borrowing is also very suitable for the Cells framework, as power reduction is very important for Cells, and fault detection efficiency remains very high.

PROTECTING FLIP-FLOP BASED DESIGNS
Note that though the preferred error detection scheme in Cells is GRAAL, Cells is also compatible with any other error detection scheme. For flip-flop based designs, two double-sampling architectures were developed:

- The one, referred a ADDA architecture [6][7], allows operating the same design in 3 modes: the first is the mode used in earlier double-sampling schemes; the second allows early failure prediction; the third allows detecting transient faults of large duration, that could be encountered in hostile environments like space.
- The other, presented in [7][8], reduces drastically the area and power penalties of the double-sampling architecture, by removing the redundant sampling element. With this solution, the only cost for implementing double-sampling consists in the comparison of the flip-flop outputs against their inputs.

The evaluation of these architectures is on-going by implementing them in the LEON3 processor.

References
Memory and Interconnect Self-Repair for High Defect Densities in the Cells Framework

Members: Michael Nicolaidis, Lorena Anghel, Mounir Benabdenbi, Panagiota Papavramidou, Vladimir Pasca

Keywords: PVT variability; aging; timing faults; soft errors; memory repair; design for reliability, yield, and low-power.

Contracts: TOETS

Embedded memories occupy the largest part of SoCs and include even larger amounts of transistors. As memories are designed very tightly to the technology limits, they are more prone to failures than other circuits. Thus, they concentrate the large majority of fabrication defects and may affect yield adversely. In addition, failure rates are expected to be exacerbated as we approach the ultimate limits of CMOS, and should further worsen in post-CMOS technologies. Furthermore, low power requirements, which are stringent in modern electronic systems, will also be exacerbated as we move towards ultimate CMOS and post-CMOS, requiring aggressive reduction of supply voltage. Unfortunately, voltage reduction results in additional failures, as weak memory cells will not operate correctly at reduced voltage levels. Furthermore, as ultimate CMOS and post-CMOS are expected to exacerbate PVT variability and circuit aging, the ratio of weak cells will sharply increase. As a consequence, techniques enabling coping with high defect densities in memories are required in the Cells framework.

Memories and interconnection buses have very regular structure and enable easy repair. Various efficient memory and interconnections Built-In Self-Repair (BISR) schemes have been proposed in the past, and several of them are already industrial practice. However, for high defect densities, conventional memory repair schemes will induce excessive area and power penalties. Thus, innovative solutions are required able to drastically reduce these penalties. The ECC-based memory repair scheme, introduced by our group, is the only known scheme able to cope with high defect densities. However, while the ECC-based repair scheme drastically reduces area and power penalties with respect to conventional schemes, power penalty is still non-negligible. Furthermore, implementing self-diagnosis for the ECC-repair scheme, further increase area and power penalties. Our recent developments have eliminated these issues [1]. First, a new family of memory test algorithms was proposed eliminating diagnosis-related area and penalties at the expense of test length [2][3]. Then, an iterative diagnosis architecture was proposed [4], trading test length with area cost. In a third innovation [5], a hardware architecture is proposed drastically reducing power dissipation for both ECC-based repair and non-ECC-based repair. Further reduction of this power is achieved by introducing an approach that rearranges the faulty addresses stored in the repair circuitry, in a manner that disables most of the time a part of this circuitry [6]. Thanks to these improvements and the use of the ECC-based repair, an impressive power reduction is achieved with respect to conventional repair.

For instance, for a SoC comprising a total of 10 Gbit memory capacity distributed over 300 embedded SRAMs using words of 32 bits (plus 7 ECC check bits), conventional repair for a $10^{-3}$ probability that a memory cell is faulty, conventional repair induces a huge power penalty of 1629%, which is due to the fact that repairing such high fault rates requires using large repair CAMs, and also that CAMs are power hungry. Then, the combination of ECC-repair with the improved repair architectures in [5][6], reduces this penalty to only 7.36% [6]. Hence, these developments provide a comprehensive framework enabling low cost memory repair for high defect densities, which is very suitable for the Cells framework.

In other developments, we proposed a BIST architecture enabling the cooperation of transparent BIST with ECC-based repair [7]. Transparent BIST is an approach we introduced at 1996, and further developed and used by numerous authors and fault-tolerant systems. This approach transforms memory test algorithms into reversible processes, which preserve the information stored in the memory. Transparent BIST is essential in the context of Cells in order to preserve application context during periodic memory self-tests. The fundamental problem for making cooperating transparent BIST with ECC-based repair is that transparent BIST uses signature analysis allowing determining if a memory is faulty (go-nogo test), while ECC-memory repair requires more subtle diagnosis (i.e. determining if there are memory words containing multiple faulty cells). While the signature analysis alone does not allow making such diagnosis, and also the error detection and correction circuitry alone can also misdiagnose words containing more than two faulty cells, the new transparent BIST architecture we have developed in the context of Cells resolves this problem thanks to a subtle cooperation between the signature analysis and the ECC circuitries.
Integrating these approaches in the Cells project will enable healing tera-device processor chips comprising billions of defective memory cells. For instance, a massively parallel tera-device chip comprising thousands of embedded memories of a 1 Tera-bit total capacity and affected by a $10^{-3}$ defect density, will comprise $10^9$ faulty memory cells (including definitely faulty cells as well as weak cells failing during aggressive voltage reduction modes). The Cells project will be able making such a chip operational, and last but not least, this unprecedented goal will be achieved at very low area and power penalties.

Interconnections may also represent an important reliability challenge, especially for 3D systems where the vertical interconnects (TSVs) may be affected by high defect densities. Efficient Built-In Self-Repair schemes for TSV interconnect, using parallel message transmission and serial message transmission, allow resolving this issue in cost effective way.

References


Array-Level Approaches in the Cells Framework

Members: Michael Nicolaidis, Nacer-Eddine Zergainoh, Amir Charif, Michael Dimopoulos

Keywords: Ultimate CMOS and post-CMOS technologies, high defect densities, reliability, yield, low-power, massively parallel single-chip tera-device computers, array level self-adaptive approaches.

Adaptive fault tolerant routing

In complex grids comprising thousands of nodes, routing algorithms based on routing tables are congestion prone and have low adaptability to new failures. Hence, we developed distributed algorithms using local opportunistic decisions (get another path when a node/router/link is faulty or congested). Our simulation results show that they easily scale for grids comprising thousands nodes; tolerate multiple faulty nodes/routers/links; avoid congestions; and cope with new failures occurring at any time. But, as they are based on local decisions, they are deadlocks prone. To cope with we use virtual networks and pertinent rules acting at the local level.

Adaptive fault tolerant task scheduling and allocation and error recovery

At a first step we integrate in a single algorithm our FT routing approach (discussed above) with distributed FT scheduling and allocation. We also integrate in the same algorithm check-point-free rollback recovery. This is done by an approach which: uses an hierarchical task organization into parent-children trees; maintains this hierarchy during execution; and if a persistent fault occurs in a resource executing a child it goes back to the parent to redistribute the workload in fault-free resources. This way we avoid saving the internal states of the grid to external media (no check-pointing), which would congest the grid I/Os, and we can recover correct operation even after the occurrence of any multiple fault (by going up in the tree until a fault-free parent, which redistributes the aborted workload to fault-free resources).

Error recovery algorithms based on check-pointing were also implemented. A basic issue is related to the fact that as the state of the system is huge; we have to perform check-pointing for partial states of the system (e.g. states of tasks), while preserving its overall coherence. To cope with this issue a check-pointing algorithm for parallel processors maintaining system coherence was developed.

Variability awareness

In further developments we extended the algorithm to enable variability aware and power aware task scheduling and allocation. Again we use a distributed non-deterministic approach to handle computation complexity. One of the developed schemes maps different groups of tasks into different regions of the grid according to the energy dissipated by each group and the power-dissipation characteristics of the regions. Then, the leader of each region maps task clusters into sub-regions, and the leader of each sub-region maps each task to a node, by using similar power dissipation considerations. The clock frequency required for meeting the deadline of each task and the power/reliability priorities of the task are encapsulated in the header of each task. Each node knows its frequency/Vdd operating domains for various error occurrence rates (by monitoring its concurrent error detection signal). Thus, it can determine its clock frequency and Vdd level to reach the task deadline, minimize the energy dissipated, and achieve the target reliability level (in terms of error occurrence rate). Thus, circuit parameters (clock frequency and Vdd) are continuously regulated to minimize power, preserve reliability and adapt to circuit degradation induced by aging.

Our work on array level self-adaptive algorithms was presented in numerous articles published in various international conferences during the past few years [1][10]. The next step of our efforts concern the integration of these algorithms (together with the other techniques used in Cells), in a unified framework implemented in the GEM5 simulator and the Structural Simulation Toolkit (SST).

References


# Team 4 / Reliable Mixed-signal Circuits and Systems (RMS)

## Themes

- Mixed-signal/RF integrated devices
- Test and control techniques
- Design-for-test
- Diagnosis
- Embedded control
- Behavioral and statistical modeling methods
- CAD tools for test and control

## Expertise

### Scientific
Test and diagnosis for mixed-signal/RF integrated devices, design-for-test, behavioral and statistical modeling, embedded control

### Fields of expertise
Microelectronics, control, statistical modelling

### Know-how
Test metrics estimation, machine-learning-based test, non-intrusive test and control, diagnosis, mixed-signal/RF design-for-test

### Industrial transfer
Techniques of integrated test for analog-to-digital signal converters, CAD software for test, embedded sensors diagnostic technique

## Research keywords

Design-for-test, built-in self-test, design-for-manufacturing, calibration, density estimation, machine-learning, embedded control

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ADC BIST for static linearity test

Members: Guillaume Renaud, Manuel Barragan, Salvador Mir, Asma Laraba, Haralampos Stratigopoulos

Cooperation: STMicroelectronics

Contracts: ELESIS (ENIAC)

Introduction

ADC static linearity test is one of the most time-consuming tasks in production testing. The static performance of an ADC is characterized in terms of its DNL and INL figures, which measure the deviation of the static transfer curve of the ADC from its ideal behavior. Traditional test methods for static test are based on applying a high-linearity test stimulus and then collecting a large number of samples per code to average the noise.

In this work, we have designed an on-chip ramp generator for high-resolution ADC BIST. This design will be implemented in an integrator-based servo-loop BIST scheme previously described in [1]. This scheme follows the classical servo-loop standardized test technique aimed at locating the transition voltages for a selected set of target codes, while enabling the use of the reduced code linearity test technique previously developed in our group [2]. The modified version of the servo-loop scheme is shown in Fig. 1.

Practical implementation of the generator

The main challenge for moving the servo-loop technique to a practical on-chip implementation is the strict accuracy requirements for the input stimulus. In order to make a sufficiently precise measurement, the magnitude of the integration step should be below the LSB of the ADC, which is a challenging constraint for high-resolution ADCs.

In this work we opted for an on-chip ramp generator implementation based on a switch-capacitor (SC) integrator, as depicted in Fig. 2. A detailed description of the design can be found in [3]. This implementation has phases \( \Phi_{\text{up}} \) and \( \Phi_{\text{down}} \) which control the sign of the ramp slope for each integration step. It also has a phase \( \Phi_0 \) that charges the output of the integrator to a voltage \( V_a \) for calibration purposes [1]. To a first-order, the integration step in this integrator is defined by the capacitance difference between \( C_{i1} \) and \( C_{i2} \). We propose to implement this difference by suppressing a finger in one of the capacitor plates at layout level. This way, we assure a very small capacitance difference but we also introduce uncertainty in the value of the step due to process variations. Indeed, numerical simulations show that a direct implementation of the integrator assuming a capacitor mismatch of only 0.1% can lead to errors in the measurement of the INL of up to 40 LSBs for a 12-bit ADC, due to the accumulation of the step errors. To alleviate this issue, we decided to calibrate the transfer function of the integrator as explained in [1].

Design considerations

The operational amplifier is designed as a fully differential two-stage folded-cascode amplifier with Miller compensation and switched-capacitor common-mode feedback (SCCMFB). A differential configuration is chosen for its good behavior against common-mode noise while suppressing even harmonics, thus enhancing the linearity of the amplifier. The overall noise is reduced by design...
and an autozero technique is implemented to reduce the offset as well. The layout of the ramp generator has been designed and its area is 0.1 mm², which is below 10% of the area of practical high-performance ADCs at this resolution.

Simulation results

Simulations were conducted in Cadence with STMicroelectronics CMOS 65nm technology. The test bench applies a constant 1V voltage at the integrator input after establishing the common-mode voltages of the two stages of the amplifier. 250 Monte Carlo transient simulations are run from 0V and stopped when the integrator output reaches 1V, which is a usual value for the full scale of an ADC. The results are imported in Matlab to extract the linearity curve of each ramp generated. The ramp generator is simulated under typical process conditions, with a 200 kHz clock frequency, and using a 2 V differential DC input as voltage reference. The generated stepwise ramp has a nominal resolution of 13.3 bits, with an average step of 96.7 μV. The deviation of the step size is contained within the range [−3, 3] μV along the considered voltage range. The average slope error, that is, the average of slope errors per step over all steps, is computed to be −0.040%. The INL of the generated ramp is computed from the deviation of the step size, defined as the difference between the actual position of the middle point of each step and its ideal position, and is shown in Figure 3. The maximum INL of the generated ramp is around 580 μV, that is, around 6 average steps. The obtained resolution and step size are well contained in the range of 11.4-13.7 bits and 100-300 μV, respectively. The average ramp slope deviation is well centered around the −0.2% value and the observed worst case value is close to −6%.

The Monte-Carlo ramp signals are applied to an 11-bit, 2.5 bits-stage pipeline ADC IP provided by STMicroelectronics with the use of the reduced code linearity technique from [2]. The ADC model has been derived from the actual static characteristic of the ADC, which was measured in the lab using the standard histogram technique dedicated bench-top equipment. Only 132 out of 2046 codes of the ADCUT are measured, which represents about 6% of the total number of codes, resulting in a significant test time reduction. Figure 4 shows the estimated INL using the proposed BIST scheme. Each code is traversed 50 times in the servo-loop configuration so as to average out noise effects. Figure 4 also shows the actual INL values obtained from a traditional histogram test for the purpose of comparison, as well as the INL estimation error.

![Figure 3: INL of the generated ramp.](image)

As it can be seen, under nominal conditions the INL estimation error is well controlled in the range [−0.5LSB, +0.5LSB]. Figure 5 shows the histogram of the maximum INL estimation error in absolute values recorded for each run. As it can be seen, the INL estimation error is always below 1 LSB with an average absolute value around 0.5 LSB. According to the results in Figure 5, in the worst-case scenario, the non-linearity of the proposed ramp generator design only contributes an additional 0.5 LSB to the INL estimation error introduced by the reduced-code linearity test technique.

![Figure 5: Histogram of the maximum absolute INL estimation error obtained by the BIST by assuming different Monte Carlo instances of the ramp generator.](image)

References


TIMA Annual Report 2015 (RMS)
ADC BIST for dynamic test

Members: H. Malloug, M. J. Barragán, S. Mir, E. Simeu

Cooperation: STMicroelectronics

Contracts: NANO2017

Introduction

In this report we propose novel generator architecture based on the concept of harmonic cancellation [1]. The proposed generator is aimed at a mostly-digital implementation, which would bring the advantages of easy design automation, portability, and migration while providing compatibility with advanced technological nodes usually optimized for high performance digital applications. The proposed generator is based on a circular shift-register that produces time-delayed versions of a digital square-wave signal. Harmonic cancellation is used to cancel the low-frequency harmonic components of the digital square-wave signal, while a passive lowpass filter is employed for attenuating high-order harmonics and signal reconstruction. Additionally, we study a simple oneshot calibration strategy to mitigate the effects of process and mismatch variations, which may degrade the effectiveness of the harmonic cancellation technique.

Harmonic cancellation

Let us consider a generic periodic signal \( x(t) \) expressed as a Fourier series expansion:

\[
x(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 t + \phi_k) \quad (1)
\]

Where \( A_k \) and \( \phi_k \) are the amplitude and phase of harmonic component \( k \) in signal \( x(t) \), respectively, and \( \omega_0 \) is the fundamental frequency of \( x(t) \).

Let us consider a time-shifted version of signal (1),

\[
x(t + \Delta t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_0 (t + \Delta t) + \phi_k) - \sum_{k=1}^{\infty} A_k \sin(k\omega_0 \Delta t) \sin(k\omega_0 t + \phi_k) \quad (2)
\]

Where \( \Delta t \) is the applied phase shift resulting from the time shift \( \Delta t \). Without loss of generality, let us now define signal \( y(t) \) as the linear combination of the original signal \( x(t) \) and \( p \) pairs of scaled and shifted signals with opposite time-shifts \( \pm \Delta t \) with respect to signal \( x(t) \) and scaled by a factor \( \alpha_k \).

\[
y(t) = x(t) + \sum_{i=1}^{p} \alpha_i [x(t + \Delta t_i) + x(t - \Delta t_i)] \quad (3)
\]

From equations (1), (2), and (3) it can be derived,

\[
ger(t) = \sum_{k=1}^{\infty} A_k \left[ 1 + 2 \sum_{i=1}^{p} \alpha_i \cos(k\alpha_i) \cos(k\omega_0 t + \phi_k) \right] \quad (4)
\]

Thus, signal \( y(t) \) resulting from the combination of a periodic signal and its scaled and time-shifted versions with opposite time-shifts, if the set of phase shifts and scale weights are properly selected such that the coefficients \( \alpha_k \) are small for given values of \( k \), unwanted harmonic components in \( y(t) \) can be attenuated or completely canceled.

This harmonic cancellation will be applied on a square-wave with a duty-cycle of 50% to generate a sinusoidal signal. Let us assume we have available \( N \) time-shifted versions of square signal \( q(t) \) at discrete shift intervals of \( T=N \). From equation (4) it is easy to derive that adding \( p \) pairs of scaled and delayed square-waves to the original square-wave signal, all odd-order harmonic components lower than the \( 2(2p + 1) \)-th order can be canceled if phase shifts and weights are selected as : (numerator l’équation)

\[
\begin{align*}
\phi_i = \frac{i\pi}{N} & \quad 1 \leq i \leq p \\
\alpha_i = \cos(i\pi/2) & \quad 1 \leq i \leq p
\end{align*}
\]

Proposed architecture

We propose to generate five time-delayed square-waves signals (i.e. \( p = 2 \)), with opposite phase shifts \( \phi_1 = \pi/6 \) and \( \phi_2 = \pi/3 \) and scale weights \( \alpha_1 = \sqrt{3}/2 \) and \( \alpha_2 = \sqrt{2} \), according to the notation in (4). These coefficients allow canceling the third-, fifth-, seventh- and ninth-order harmonic components in the original square-wave signal.

The proposed architecture, illustrated in Fig. 1, is a digital generator that provides a set of time delayed digital square-waves, a simple analog to digital interface that uses 1-bit DACs, and a passive RC lowpass filter with a weighted resistor input network for scaling and combining the different square-wave phases and filtering the generator output.

The digital square-wave generator is composed of a simple circular shift-register. The frequency of the digital square-wave is then equal to \( \text{fclk}/N \), where \( N \) is the number of stages in the shift register.

The outputs of the digital square-wave generator are fed into a digital to analog conversion stage to isolate the outputs of flip-flops from the weighting resistor network and to provide noise-free voltage
references Vref+ and Vref− for logic ‘1’ and ‘0’ values, respectively.

The output RC lowpass filter is designed to scale and combine the selected five delayed squarewaves and to provide an attenuation of high-order harmonic components for signal reconstruction at the generator output. Assuming that the generator operates at a low enough frequency such as the timing errors in flip-flops and DACs are negligible, the performance of the proposed sinusoidal signal generator is mainly limited by the mismatch in the scale weights defined by the resistor network at the input of the low pass filter. We propose a simple calibration technique to mitigate this issue. The proposed technique, as shown in fig. 2, consists on estimating the weight error due to mismatch and applying the appropriate compensation to the corresponding resistors. The calibration stage starts by sending a ‘set’ signal to the flip-flops in the shift-register to set their outputs to a logic ‘1’ . Hence, nodes (2, 1, 0, 1, 2) are set to the voltage reference Vref+. Calibration switches Scal are then sequentially activated for the five signal paths and five measurements of the voltage drop across a calibration resistor are extracted (see Fig. 2 and 3). The actual value of the scaling weight for each signal path is proportional to the corresponding voltage drop across the calibration resistor. Notice that the precise value of this calibration resistor is not important, since the scale weights are defined as relative values with respect to R0. The measurement of these voltage drops can be performed on-chip using embedded resources, or they can be routed off-chip for external monitoring. Once the actual scale weights are estimated, digital calibration words are sent to each calibration block as depicted in Fig. 3 to select the appropriate resistance value for each signal path and compensate eventual mismatch errors.

**Simulation results**

We have developed a realistic behavioral model of the generator that takes into account the main non-idealities affecting its performance, including delay mismatch in the flip-flops, DACs, and resistor mismatch in the output RC filter, which produces inaccurate scaling weights.

Simulation results demonstrate that resistor mismatch has a significant impact in the linearity of the generator for low and medium generated frequencies (1.66Mhz and 16Mhz), while timing issues become dominant for the high generated frequency scenario (166Mhz).

Statistical behavioral simulations were performed in order to analyze the performance of the proposed one-shot calibration strategy. The proposed calibration strategy is able to significantly improve the THD of the generated output in the low and medium frequency scenarios, but it does not bring any improvement in the high frequency case. This result can be easily explained: because of the better resistor matching, the impact of time delay mismatch dominates at high operation frequencies. Improving the linearity of the generator in this case would require calibrating the delay mismatch between the different signal paths.

**Conclusion**

We have studied an efficient implementation of an on-chip sinusoidal signal generator based on digital circuitry and the use of calibrated harmonic cancellation. The simplicity of the digital resources used to implement the generator makes it very suitable for mixed-signal BIST applications and facilitates the migration of the generator across different technological nodes. Statistical behavioral simulation results are provided in order to explore the design trade-offs and performance limits of the proposed generation strategy.

**References**

Built-in test in RF circuits using non-intrusive sensors

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Cooperation: CEA-LETI

Contracts: ELESIS (ENIAC), SACSO (ANR)

Introduction

Standard RF and millimeter (mm-wave) test practices incur a very high cost. An alternative technique with high potential to reduce test cost is built-in test, where the idea is to integrate on-chip some structures to facilitate the test, such as a test stimulus generator, response analyzer, etc. The most popular built-in test approach for RF transceivers is the loop-back test where the test signals are generated in the baseband and the transmitter’s output is switched to the receiver’s input to analyze the test response also in the baseband. Another popular built-in test technique relies on the use of envelope detectors and current sensors to extract DC/low-frequency test signatures that nevertheless carry RF information.

For a successful implementation of a built-in test technique, different criteria need to be satisfied simultaneously: (a) the test accuracy of the standard method is maintained; (b) the performances of the Circuit Under Test (CUT) are not affected; (c) the pin and area overheads are acceptable; and (d) the achieved test cost reduction justifies the built-in test development effort. It is noteworthy that none of the aforementioned state-of-the-art built-in test techniques fully satisfies objective (b). For example, the loop-back connection requires the insertion of a switch and an attenuator and, for some types of receivers, even an extra mixer is inserted in the RF signal path. Envelope detectors and current sensors also tap into the RF signal path. In general, adding components in the RF signal path degrades the impedance matching and adds parasitics, which inevitably shift the performances and unbalance the performance trade-offs achieved by design.

To address this issue, built-in test circuitry needs to be co-designed with the CUT which increases design iterations to meet the target design specifications, if possible. For this reason, designers are rather reluctant to incorporate such built-in test techniques since the design specifications are stringent and exploit the full capabilities of advanced technology nodes.

Non-intrusive built-in test

In this work, we propose to rely on non-intrusive built-in sensors that have the comparative advantage that let the design intact. These non-intrusive sensors capitalize on the undesired phenomenon of process variations. The underlying idea is to monitor process variations instead of measuring directly the RF performances. For this purpose, we can employ Process Control Monitors (PCMs), such as single layout components (e.g. transistors, capacitors, resistors, inductors), and dummy circuits that are extracted from the CUT topology (e.g. bias stages, current mirrors, gain stages, level-shifters, etc.). These sensors are placed in close physical proximity and are matched to identical structures in the CUT. For example, we can place a dummy bias stage next to the bias stage of the CUT, a dummy transistor next to a critical transistor in the CUT, etc. In this way, the sensors and the CUT “witness” the same die-to-die (D2D) and correlated within-die (WID) process variations and, as a result, the measurements obtained on the sensors will be correlated to the performances of the CUT to a very large extent. An indirect, low-cost test can be put in place by employing the alternate test paradigm to map the sensor measurements to the performances. This test approach has been inspired by the PCMs typically placed in the scribe lines of a wafer to monitor variability and identify off-target process parameters.

The objective of this work is to demonstrate the non-intrusive built-in strategy for a typical inductive degenerated RF Low Noise Amplifier (LNA) operating at 2.4GHz considering both simulation and silicon data.

We observed that the variability in the inductors explains to a large degree the variability in the performances, thus it was deemed necessary to monitor the variability in the inductors. However, adding a dummy inductor PCM is not a smart choice since it incurs a large area overhead. For this reason, variability in the inductors was not considered at all in previous related work. In this work, we studied the sources of variability in the inductors and we found that most of the variability is due to the variability in the resistivity of the high-level metal and alucap layers that form the coils of the inductors and not due to the variability in the pure inductance of the coil. This led us to employ low area overhead metal and alucap resistor PCMs, instead of an area-hungry inductor PCM, in order to capture most of the variability in the inductors. We also demonstrate that WID variations, which cannot be handled by the non-intrusive variation-aware sensors, do not affect appreciably the prediction results.
Results
Both the LNA and the non-intrusive variation-aware sensors have been designed using the 65nm CMOS065 bulk technology provided by ST Microelectronics. The schematic of the LNA is shown in Fig. 1. The sensors that we have employed in the analysis include: (a) a dummy current mirror, (b) a dummy voltage divider, (c) a dummy bias stage, (d) a diode-connected MOS PCM, (e) a MOM capacitor PCM, (f) an inductor PCM, and (g) high-level metal and alucap resistor PCMs, as depicted in Fig. 2.

For the simulation analysis, a Monte Carlo sample set of 1000 circuit instances was used to learn the regression functions in alternate test. Out of the 1000 instances, we used 800 circuit instances in the training set and the rest of 200 instances were used as a validation set to provide an unbiased estimate of the prediction error of alternate test. The prediction error is expressed in terms of: (a) average Root Mean Square (RMS) error, (b) absolute average RMS error, (c) a Figure of Merit computed as the ratio between the RMS error and the standard deviation of the performance, (d) correlation coefficient, and (e) maximum error between the simulated (e.g. "true") and predicted performances.

Table 1. Alternate test results based on simulation, considering both D2D and WID variations.

<table>
<thead>
<tr>
<th>Performance</th>
<th>Average RMS Error</th>
<th>Average Absolute RMS Error</th>
<th>Correlation Coefficient</th>
<th>Maximum Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>S21</td>
<td>1.24 %</td>
<td>0.18 dB</td>
<td>84.25 %</td>
<td>0.18 dB</td>
</tr>
<tr>
<td>S11</td>
<td>1.58 %</td>
<td>0.14 dB</td>
<td>89.05 %</td>
<td>0.37 dB</td>
</tr>
<tr>
<td>S22</td>
<td>13.12 %</td>
<td>2.1 dB</td>
<td>55.96 %</td>
<td>5.26 dB</td>
</tr>
<tr>
<td>NF</td>
<td>1.16 %</td>
<td>0.02 dB</td>
<td>95.30 %</td>
<td>0.05 dB</td>
</tr>
<tr>
<td>1-dB CP</td>
<td>1.57 %</td>
<td>0.2 dBm</td>
<td>87.7 %</td>
<td>0.57 dBm</td>
</tr>
<tr>
<td>IMP</td>
<td>9.87 %</td>
<td>0.15 dBm</td>
<td>83.09 %</td>
<td>0.45 dBm</td>
</tr>
</tbody>
</table>

Table 2. Alternate test results based on real silicon measurements.

<table>
<thead>
<tr>
<th>Performance</th>
<th>Average Absolute RMS Error</th>
<th>Prediction figure-of-merit</th>
<th>Correlation Coefficient</th>
<th>Maximum Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>S21</td>
<td>0.24</td>
<td>0.87</td>
<td>59.96 %</td>
<td>1.15 dB</td>
</tr>
<tr>
<td>S11</td>
<td>0.45</td>
<td>0.94</td>
<td>57.34 %</td>
<td>1.91 dB</td>
</tr>
<tr>
<td>S22</td>
<td>0.64</td>
<td>0.67</td>
<td>74.71 %</td>
<td>1.99 dB</td>
</tr>
<tr>
<td>NF</td>
<td>0.12</td>
<td>1.43</td>
<td>14.46 %</td>
<td>0.72 dB</td>
</tr>
<tr>
<td>1-dB CP</td>
<td>0.17</td>
<td>0.80</td>
<td>62.2 %</td>
<td>0.63 dB</td>
</tr>
</tbody>
</table>

Figure 1: GHz CMOS inductive degenerated LNA schematic

Figure 2: Variation-aware sensors built from identical components that exist in the topology of the 2.4GHz LNA

Figure 3: Photograph of the fabricated chip

Figure 4: Scatter plot of measured vs. predicted values for performance S11 of the LNA considering a few simple low-cost non-intrusive variation-aware sensors
As it can be seen from Tables 1 and 2, the prediction results are satisfactory for all the performances. In Table 2, the error metrics for NF are not as good because NF showed practically no variability. In summary, a low-cost alternate test based on the selected sets of non-intrusive sensors is capable of replacing the standard specification tests for measuring the performances while maintaining practically the same test accuracy. Finally, it should be noted that there is an on-going work regarding a 65nm 60GHz mm-Wave LNA. A few chips have been taped-out and measurements will be performed within the following months.

References
One-shot non-intrusive calibration against process variations for analog/RF circuits

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Contracts: SACSO (ANR), ELESIS (ENIAC JU), P-SOC (CNRS/INSIS)

Introduction

Deep sub-micrometer CMOS technologies drive a large proportion of innovation in many industries. A major challenge with these CMOS technologies is that the amount of process variation becomes particularly pronounced. Process variation causes measurable variance in the output performance especially in the case of analog/RF circuits. The trend nowadays is to integrate analog/RF circuits together on the same die with the digital processor and memory in advance process nodes. To address the problem of process variation, analog/RF circuits are often over-designed conservatively using large transistors, thus resulting in larger area and excessive power consumption.

Proposed one-shot calibration technique

This work proposes to design analog/RF circuits aggressively using minimum size transistors and leave large design margins by employing a calibration algorithm in post-manufacturing to recover yield loss and achieve overall a desired trade-off between output performances.

The proposed calibration algorithm, illustrated in Figure 1, is driven by measurements M that offer an "image" of process variations. The measurements are obtained on low-overhead non-intrusive sensors. The non-intrusive property means that the sensors are not electrically connected to the circuit and, thus, are totally transparent to it. This is very appealing to designers since the circuit design is dissociated from the sensor integration and the sensor integration does not degrade the performances of the circuit. The sensors include single layout components and simple analog stages that are extracted from the topology of the circuit. Thus, this calibration approach is virtually applicable to any circuit. The core of the calibration algorithm is a regression model $P = z(M, TK)$ that expresses the relationship amongst the performances $P$ of the circuit, the sensor measurements $M$, and the tuning knob values $TK$. This regression model is learned based on initial production data and can be refined over time to account for process shifts. Thanks to the non-intrusive property, the sensor measurements stay invariant under changes of the tuning knobs. This means that it suffices to obtain the sensor measurements only once, plug their values into the regression model, and then optimize the resultant relationship between performances and tuning knobs without needing to repeat the sensor measurements for every tuning knob setting that is visited during the course of the optimization. In other words, the non-intrusive property allows us to perform the calibration efficiently in one-shot using a single test step and optimizing tuning knob values quickly in software in the background, which greatly reduces the calibration time.

Case study

Our case study is an RF Power Amplifier (PA). The PA and its associated non-intrusive built-in sensors have been designed using the 65nm CMOS065 bulk technology provided by ST Microelectronics. Figure 2 shows a microphotograph of one of the fabricated chips, highlighting the area of the circuit.

Figure 1: Proposed post-manufacturing calibration setup for RF circuits

Figure 2: Microphotograph of fabricated chip

The PA topology consists of a driver stage, a power stage, and three matching networks at the input (IM), output (OM), and inter-stage level (ISM), as illustrated in Figure 3. The matching networks have been implemented with discrete components on the
Printed Circuit Board (PCB). The driver and power stage are based on the elementary stage shown in Figure 4, which is composed of the PA elementary stage and its associated non-intrusive sensors. The driver stage is composed of one PA elementary stage and the power stage is composed of four PA elementary stages connected in parallel.

As tuning knobs we have chosen the power supplies and bias voltages, that is, no alterations in the design have been made to insert extra tuning knobs. The set of non-intrusive sensors includes a dummy resistor, a dummy capacitor, and a dummy cascode gain stage for each PA elementary stage. These structures are extracted from the topology of the PA elementary stage, as shown in Figure 4. The set of measurements includes the DC currents that flow through the two dummy resistors in the driver and power stages, the DC currents drawn by the two dummy cascode gain stages in the driver and power stages, and the values of the dummy capacitors.

To demonstrate the proposed calibration approach, we fabricated 3 wafers, namely with FAST (i.e. FAST wafer), SLOW (i.e. SLOW wafer), and typical (i.e. TYP wafer) transistors. For the purpose of the experiment, we have at hand a total of 55 chips extracted from these 3 wafers.

Results

As an example, Figure 5 shows for the chips from the SLOW wafer, which are all non-functional before calibration, the histograms of the 4 main performances of the PA predicted by the regression model and measured after calibration. The yield recovery is 100% and the predictions point to the correct calibration decisions.

Figure 6 shows for the chips from the TYP wafer the histograms of the measured performances at a randomly selected tuning knob setting before calibration and the predicted and measured performances after calibration. We observe that before calibration the vast majority of violates the gain specification. The calibration algorithm was able to find appropriate tuning knob settings for these chips to fully recover yield loss and achieve a better performance trade-off.

References

Performance monitoring and errors reconciliation in image decoders

Key-words: Image quality, error concealment, classification, regression,

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Cooperation: STMicroelectronics
Contracts: Nano2017 A3

Introduction
With the growing of perception in new technology devices, digital visual is required in various application domains (medical service, security service, entertainment sector, automated traffic control). The digital visual processing generally comprises an acquisition process, compression, transmission, the decoding, storage and display of images. Each step in the treatment process induces distortions on input image which leads to the degradation the final image quality [1]. Nowadays, the judgment of the image quality has become a hot topic in image processing research. Indeed, the output image quality plays a significant role in evaluating the performance of many visual processing applications and in enhancing artifact detection and concealment process.

Image Metric Selection for IQA Prediction
Several objective methods exist to evaluate the image quality [1]. The purpose in this work has been to evaluate and compare the prediction precision, and the stability of machine learning algorithms used for designing an IQA prediction model. We use the image quality database TID2013 in order to benchmark and evaluate the predicted models, this database provides 3000 images, and each image is related to 14 image quality metrics and human rating Mean Opinion Score (MOS). By using Pearson's correlation coefficient, we select the most pertinent metrics which have simultaneously high correlation with MOS and low mutual cross-correlation [2]. As a result, the number of metrics required for IQA prediction model has been reduced into four, and the reduced-size TID2013 is composed of \( N = 3000 \) image datasets on the form \((X_1,Y_1),..., (X_N,Y_N)\) where \( X_i \) is the image quality metric vector: \( X_i = (x_{i1}, x_{i2}, x_{i3}, x_{i4})^T \) corresponding to FSIMc, PSNR-HMA, PSNRc and SSIM respectively, and \( Y_i \) is the corresponding subjective MOS, where \( i \) represents the index of image set.

Machine Learning Methods
Objective IQA block construction consists essentially of a training phase using a given ML algorithm and a validation phase. During the training phase, ML algorithms are applied to create an appropriate mapping model that relates the quality metric vector of image to the provided subjective MOS of the same image. Six different ML methods studied in this work are presented as follows:

Linear Discriminant Analysis (LDA)
Linear discriminant analysis classification technique is usually used in statistic and machine learning, to find a linear combination of features that separates or classifies objects (such as images, products, customers, etc.) into two or more groups.

k-Nearest Neighbors (k-NN)
The key concept in the k-nearest neighbor classification method is to project all training set points on the metric space, then calculate the distance from these observation points and the point which we want to classify; and select the k-closest points. Finally the class corresponding to the studied point is determined by applying majority vote rule.

Artificial Neural Network (ANN)
Artificial neural network is a sophisticated learning method, inspired from the structure of biological neural networks, able to model nonlinear relationships between inputs and outputs. In [1], [2] the structure of ANN model used consists of two layers: hidden and output layers; the hidden layer is composed of four interconnected nodes and the logistic sigmoid activation function, while the output layer contains one node and a linear activation function.

Non-Linear Regression (NLR)
The polynomial non-linear regression method seeks to express MOS as an appropriate nonlinear polynomial combination of the metric vector elements. It is explained [1], [3] how to design an appropriate NLR model. It is shown that the image quality can efficiently be predicted with a polynomial regression model of degree 3 with 19 terms.

Decision Tree (DT)
Decision tree is a non-parametric and nonlinear method, built through a recursive binary-partitioning process. In [1] a mapping is created between the quality metrics and MOSs based on DT algorithms,
and the generated mapping model consists of a binary tree structure with 39 levels in which each internal node represents a test on some input metrics value, each tree branch represents the outcome of the test and each terminal leaf node contains the predicted MOS value.

**Fuzzy Logic (FL)**
The fuzzy logic method can be considered as a generalization of the classical set theory by introducing the notion of degree in the verification of a condition; thus enabling a condition to be in a state other than 0 or 1. It provides a flexibility for reasoning, which makes it possible to take into account inaccuracies and uncertainties.

**Implementation and results**
We implemented all aforementioned ML methods using Matlab, and at the end of the training phase, we get an objective ML model with four input metrics and one output, corresponding to the predicted MOS.
The validation phase is used to estimate how well the trained ML model predict the perceived image quality and to compare the accuracy and robustness of different ML methods. In this phase, we apply Monte Carlo cross validation (MCCV) [4], as follows: a) First, we split the data-set with a fixed fraction (α%) into training and validation set; where α% of the samples are randomly assigned to the training process in order to design a model, while the remaining samples are used for assessing the predictive accuracy of the model. b) Then, the first step is repeated k times. c) Finally, the correlation scores are averaged over k. In this report, α% = 70% and k = 1000. Validation results can be resumed on Table I and on Fig. 1. Table I gives the mean and standard deviation for all type of correlation scores (PLCC, SRCC, KRCC, determination correlation $R^2$ and mean square error MSE) derived during the validation phase. Fig. 1 presents the box-plot of Pearson’s correlation data generated during the validation phase for all proposed machine learning approaches. Comparing the prediction performance of the proposed ML methods, we can notice that Fuzzy logic model is considered as the best in fitting the subjective MOS, since it has the best mean and the smallest standard deviation of the correlation scores and the smallest MSE error.

**Table 1 : Average – STD for validation of ML methods.**

<table>
<thead>
<tr>
<th>Method</th>
<th>PLCC Mean</th>
<th>SRCC Mean</th>
<th>KRCC Mean</th>
<th>$R^2$ Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDA</td>
<td>82.13%</td>
<td>81.39%</td>
<td>73.93%</td>
<td>66.05%</td>
</tr>
<tr>
<td></td>
<td>0.88%</td>
<td>0.51%</td>
<td>0.54%</td>
<td>1.83%</td>
</tr>
<tr>
<td>KNN</td>
<td>86.12%</td>
<td>85.99%</td>
<td>79.14%</td>
<td>72.74%</td>
</tr>
<tr>
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**Conclusions**
In this paper, we analyzed the relevance of the use of machine learning techniques for objective assessment of image quality. Six machine learning methods are used to predict the image quality in agreement with the human visual perception. Implementation and validation results allow to conclude that Fuzzy Logic provides the model with the best stability and robustness property with the highest correlation average and smallest correlation standard validation. Thus, changing the training data or using another database, the prediction performances will not be significantly changed.

**References**
Analog BIST for CMOS imager array

Members: R. FEI, S. Mir

Cooperation: STMicroelectronics

Contracts: CIFRE

Introduction

Production testing of CMOS image sensors (CIS) is mainly based on detecting defects present in the images that are captured by the devices under test. Although this is a costly procedure, its fault coverage is not sufficient considering today quality requirements. Studies on devices produced at large volume have shown that Horizontal Fixed Pattern Noise (HFPN) is one of the common image failures encountered on products that present fault coverage problems. A detailed analysis of failed devices has demonstrated that HFPN failures arise from changes of electronic circuit topology in pixel addressing decoders or the metal lines required for pixel powering and control.

A built-in self-test (BIST) structure for the on-chip detection of catastrophic and non-catastrophic defects in the pixel power and control lines is proposed in our previous works. It is based on measuring the signals propagation delay in the lines of the pixel array. The lines under test (LUT) use the actual functional signals during image capturing, thus avoiding any additional test time of the BIST during production testing.

The novel BIST technique has first been evaluated by simulations that have demonstrated a good sensibility to small defects. Next, we have carried out the design and characterization of a test chip to fully validate the approach.

Principle of the BIST and its implantation

Defects in a line of a pixel array will result in a change of its RC behavior. If we assume that a rising (falling) edge is sent at one end of the line, the measurement of the rise (fall) time of the signal at the other end of the line can be used to test its change of RC behavior. The BIST implanted in the test chip is considered for the measurement of the rise time. The first stage, called Line Propagation Delay Detector (LPDD), generates two signals with a time interval between their rising edges that is proportional to the rise time of the signal in the LUT. The second stage is for readout of this time interval that is transmitted to the bit lines VXLTI and VXSMT that are read out for sorting the LUT defective lines.

The time interval between the pair of bit lines VXLTI and VXSMT is converted to a voltage by means of an on-chip Time-to-Voltage Converter (TVC), and this voltage is read out by an on board Analog to Digital Converter (ADC) as an additional pixel value. The TVC is designed with a layout compatible with the Correlated Double Sampling (CDS) read out circuitry of the CMOS sensor.
Test plan for validating the BIST

Three test cases are considered for validation of the BIST:

1. Fault free lines without BIST structure. This part is used to verify the normal function of the CIS and check its performances without influence of the BIST structure.

2. Fault free lines with BIST structure. This part is used to characterize the performances of the LPDD when measuring the fault free lines. This part can also show if the BIST structure has influence on the CIS normal function by comparing with the first test cases.

3. Lines with difference faults injected and with the BIST structure. These test cases are used to validate the performance of the BIST for detection of different kind of defects.

Characterization of the first prototype

The characterization of DSI_PHOENIX test chip has been carried out for an experimental validation of the test efficiency of the new BIST structure. Two wafers are ordered for this project within a ST MPW run. The characterization of the test chip was performed on the dies packaged in 68 pins Ceramic Pin Grade Array (CPGA68), as shown in Figure 3.

![Figure 3: Image of a packaged device](image1)

Figure 3: Image of a packaged device

Figure 4 shows an image captured by a test chip. The last 12 columns in the image are used for our test results readout.

![Figure 4: An image captured by a test chip](image2)

Results

The performance of the LPDD is first validated by measuring the LPDD outputs via an external monitoring block. As shown in Figure 5, the measured time interval between LPDD outputs LTI and SMT is proportional to the resistive defects injected into the LUT.

![Figure 5: The time interval between the LPDD outputs as a function of the injected resistive defects](image3)

More measurement results are obtained by using an automated test bench for test results readout considering the embedded monitoring blocks. Shown in Figure 6, we can see that all injected resistive and capacitive defects have been detected with good precision (fault free lines have an output around an output code of 4000).

![Figure 6: Measurement with test results read out via automat test bench](image4)

Conclusions

This invention has been presented in IEEE VTS 2015 [1]. The experimental results obtained with the fabricated samples have shown the test efficiency of this new BIST technique for detection of HFPN faults.

References

**Piece-Wise-Linear ramp generator for CMOS imagers and Calibration Techniques**

**Keywords:** image sensors, CMOS, converters, non-linear ramps

C. Pastorelli, S. Mir

**Cooperation:** STMicroelectronics

**Contracts:** CIFRE grant with STMicroelectronics

**Introduction**

The size of the pixel matrix in next generation CMOS sensors keeps increasing while there is a demand for high frame rates (120 fps). In order to achieve these levels of performance, the read out circuitry must be improved taking into account the highly constrained column pitch and the power consumption [1]. A possible way of improvement is to use a PWL ramp in the read out circuit to increase the frame rate without degrading the image quality.

**Image sensor architecture**

To get a high speed conversion at low power consumption in a small pitch-limited area, the single slope analog-to-digital (ADC) is the best choice. The time delay from the beginning of the ramp to the time when the ramp crosses the pixel value is measured by a counter as shown in Figure 1.

\[
P(k) = \frac{n^k}{k!} e^{-n} \quad [1]
\]

with ‘n’ the number of photons. Therefore, \( \sigma^2 = n \) and \( SNR = \frac{n}{\sqrt{n}} = \sqrt{n} \). This is an absolute limit that comes from the light source.

**ADC Piece-Wise-Linear ramp**

After conversion, the additional quantization noise at the output is \( \sigma_{ADC} = \frac{V_{LSB}}{\sqrt{12}} \) with \( V_{LSB} \) the LSB. As shown in Figure 2, the quantization noise does not need to be low when the signal is strong, because it will be lower than the noise floor. This observation allows an increase of the quantization noise for stronger signals and the use of a piece-wise linear ramp [2]. A high speed 13Mpix image sensor has been developed with a PWL ramp ADC.

![Figure 1: Single slope ADC architecture](image1)

![Figure 2: Single slope converters using linear and piece-wise linear ramps](image2)

**Architecture**

Figure 3 shows a block diagram of the sensor. The sensor has 4248x3216 pixels with an 1.1\( \mu \)m pitch, including dark and dummy pixels. The readout circuits use a digital CDS (D-CDS) that allows for Vertical Fixed Pattern Noise (VFPN)
free of mismatch. A 10b column-parallel ADC includes an integration capacitance which is a part of the PWL ramp generator, a buffer, a comparator and a ripple counter. A compiled digital calibration algorithm on the right side allows the calibration of the converted data. The ADC is located on the top and bottom of the pixel array that allow a layout pitch for the readout circuits of 2.2μm which is twice the pixel pitch.

Figure 3: Block diagram

Figure 4 shows a simplified schematic diagram of the PWL ramp generator. It is based on a switched current source with an integration capacitance. The variable current source is composed of an array of 11b thermometric unit elements and an integration capacitance distributed in column. The use of a buffer prevents smearing issues caused by a ramp distortion when many comparators simultaneously change state.

Figure 4: Schematic of the I/C ramp generator

Calibration Techniques

In the proposed technique, the output data for the 1st PWL segment is automatically calibrated by the use of a digital CDS while the other segments are calibrated through additional measurements. In the case of 2 segments, a linear ramp conversion is applied with different slopes in order to measure the differential delay as shown in Figure 5: This calibration data is saved column by column for linearization

Figure 5: Additional conversions for ADC linearization

Chip Micrograph

The prototype image sensor has been fabricated in a 65nm 1P5M CIS process as illustrated on Figure 6. The die size is 6.5mm(V)x6.3mm(H). The PWL ramp generator is placed on the left side of the chip.

Figure 6: Chip Micrograph

References
High Frequency Jitter Estimator for SoCs

Members: R. Alhakim, M. Valka, S. Mir, H. Stratigopoulos, E. Simeu,

Cooperation: STMicroelectronics

Contracts: NANO2017, ELESIS (ENIAC)

Introduction

As CMOS technology scales down, higher operating frequencies and data rates are made possible, continuously putting pressure for the development of appropriate test schemes that guarantee high production yield, adequate test quality, and affordable test costs. Testing for timing uncertainty of clock sources is mandatory. Several techniques exist for the estimation of jitter on SoCs, but these approaches have different implementation limitations, such as: require higher silicon overhead and power consumption, suffer from non-ideal effects due to on-chip parameter variations, require high computational complexity or a very time-consuming.

Therefore, the objective of this project is to validate an adequate Embedded Test Instrument (ETI), referred as jitter BIST, for measuring high frequency (HF) jitter in the clock signals of STMicroelectronics SoCs. The signatures provided by this ETI during production testing are used to reject devices with potential timing faults. As opposed to previous works, the circuit implementation of the proposed ETI is simple and robust with respect to on-chip non-ideal effects. We present experimental measurements that have been carried out using an FPGA-based test platform to validate the jitter measurement accuracy in the presence of non-idealities that can affect the ETI.

Under-sampling concept

The ETI is based on under-sampling the observed clock signal of frequency \( f_{\text{obs}} \) by means of a reference clock signal of frequency \( f_{\text{ref}} \), with \( f_{\text{ref}} \) being slightly lower than \( f_{\text{obs}} \) [1]. The difference \( \Delta \) between the periods of both signals is given by:

\[
\Delta = T_{\text{ref}} - T_{\text{obs}} = \frac{1}{f_{\text{ref}}} - \frac{1}{f_{\text{obs}}} \tag{1}
\]

where \( T_{\text{ref}} \) and \( T_{\text{obs}} \) are the periods of the reference and observed clocks, respectively. Thanks to the time difference \( \Delta \), the rising edges (sampling moments) of the reference signal slide along the observed signal a value \( \Delta \) during each clock period. As the result of this under-sampling process, the output signal, termed beat signal, will contain additional transitions (or unstable bits) around the rising/falling edges as shown in Fig. 1.

In [5] we demonstrate that there is a linear relationship between the number of unwanted signal transitions (or unstable bits) in the beat signal and the RMS HF jitter present in the observed clock signal, as shown in Fig. 2. Fig. 3 shows high matching between the jitter estimated by theoretical model and that estimated by a transistor-level simulation using the 65 nm CMOS bulk technology by ST Microelectronics.
Jitter Instrument Implementation

Fig. 4 shows the basic architecture of the ETI. It has three principal inputs (Tref, Tobs and enable) and two output registers referred as Transition (Tr) and Beat Edge Counter (BEC). The main components of the proposed architecture are the following: 1) Clock Gater (CG) allows defining the time window for jitter measurement; 2) Under-sampling Unit (USU) allows sampling the observed clock signal; and 3) Jitter Detection Unit (JDU) is composed of two counters and a median filter. The counter provides the total number of bit transitions while the median filter is used to filter the unstable bits due to jitter so as to provide the mean transitions of the beat signal.

Fig. 5 shows the experimental set-up for jitter estimation, composed of the following instruments: 1) Low-jitter reference clock generator; 2) Arbitrary Waveform Generator (AWG) for providing the observed clock signal with random voltage-controlled jitter; 3) Oscilloscope for measuring directly the clock jitter; 4) Xilinx Vertix-5 FPGA platform containing ETI unit.

Fig. 6 compares the experimental and simulation results. As it can be seen, the results match with negligible error. Small differences can only be seen for the lowest value of injected jitter, where the jitter estimated by the ETI cannot be lower than the under-sampling resolution \(\Delta\), combined with measurement error of the actual instruments.

To conclude, the circuitry implementation of HF jitter estimator is very simple and only consists of sampling Flip-flops and counters. The simplicity of the ETI is made possible by its inherent linearity. The ETI is today systematically embedded into all ST Microelectronics products in order to characterize all internal clock sources and to ensure high test coverage for the clock signal generators.

References

On-Chip power supply noise detector

Members: M. Valka, R. Alhakim, E. Simeu and S. Mir

Cooperation: STMicroelectronics

Contracts: NANO2017

Introduction

Power consumption is becoming the most significant constraint in electronic products due to large diffusion of portable devices. This need influences not only the design of devices, but also the choice of appropriate test schemes that have to deal with production yield, test quality and test cost. It is mandatory to test and to monitor the performances and to catch timing or delay faults. At-speed scan testing consists of using a rated (nominal) system clock period between launch and capture for each delay test pattern, while a longer clock period is normally used for scan shifting.

The major cause of yield loss due to at-speed scan testing is the Power Supply Noise (PSN), caused by excessive switching activity leading to excessive power consumption. Dedicated techniques are aimed at test pattern modification where the toggle activity is reduced for power-aware Design-for-Testability (DfT). However, such solutions may lead to test escapes and potential reliability problems. In this work, we target embedded low-complexity techniques allowing to determine and localize the power supply noise events. In order to validate the proposed solution we have built a PCB demonstrator and test-chip containing the proposed IP working at 1-2 GHz.

Power Supply Noise Detector (PSND)

Power Supply Noise Detectors (PSND) can be roughly classified into three categories, according to the type of detector used: ADC, Ring Oscillator and Delay Line. An ADC based detector uses a basic unit shown in Figure 1. This unit includes an inverter that is powered by the noisy signal. The flip-flop is powered by a safe signal. The variations at the output of the inverter are sampled by the flip-flop. A multi-bit ADC combines several of these units.

In a ring oscillator PSN detector, a process monitoring box (PMB) is used to determine the actual power consumption. The PMB is implemented as a ring oscillator that clocks a counter during a fixed time window. The output value of the counter depends on the ring oscillator frequency which in turn depends on the chip physical constraints and the actual power supply voltage.

Figure 2: Ring Oscillator based PSND

Finally, a PSN sensor based on delay lines is composed of delay elements (inverters) and capture elements (latches) to form a Time-to-Digital Converter (TDC). However, it suffers from the non-linearity of the TDC.

Proposed Power Supply Noise Detectors

It has been shown in [1] that PSN provokes timing uncertainty (Jitter) which is highly correlated to the PSN. Therefore PSN could be derived by means of measuring the jitter. Hence, in this work we have proposed a novel Embedded Test Instrument (ETI) that allows quantifying the jitter impacted by deterministic power supply noise events. The jitter estimator integrated inside the ETI is based on the under-sampling technique and consists only of Flip-flops and counters [2]. This solution can be easily integrated into a heavy industrial flow. In order to validate the proposed ETI we have built a printed circuit board (PCB) platform, working at high frequency of 2GHz. In addition to the jitter estimator (JE) unit, the PSND also contains a chain of buffers (CoBs) which works as PSN antenna and converts the noise in the power supply into jitter.

Figure 3 shows the experimental set-up for PSND, composed of the following instruments: 1) RF signal generator that ensures an efficient synchronization between different instruments; 2) low-jitter reference clock generator; 3) data generator that provides also a low-jitter clock but with frequency slightly higher than reference clock frequency; 4) noise Generator that provides a sinusoidal signal with controllable frequency and
amplitude; 5) power supply voltage generator for CoBs; 6) mixers to inject the sinusoidal noise to the source voltage of CoBs; 7) power supply voltage generator for JE; 8) PCB platform; 9) oscilloscope for measuring directly the jitter produced by PSN; and 10) a computer used for visualizing the estimated jitter value.

![Diagram](image)

Figure 3: Experimental validation on FPGA: (a) set-up, (b) snapshot

![Graph](image)

Figure 4: Noise sensitivity function

The results in Figure 4 show the relationship between the noise frequency and the corresponding estimated jitter for different values of noise amplitude. We can notice that an increase in the noise amplitude leads to an increase in the timing uncertainty. We can also see that the system space is divided into two zones: Go and No-Go zones. To conclude, we expect that an at-speed scan test can be modelled including a power supply noise generator which produces a noise signal with specific frequency. By measuring the system jitter using the proposed ETI and considering Figure 4, we can deduce the noise amplitude produced from the test process and make a decision whether the system will normally work or not during the test operation.

**Test chip Implementation**

The test chip shown in Figure 5 contains two parts: a power supply noise inducer (PSNI) and the PSND. This test chip has been implemented by using a technological node 28nm FDSOI. In order to simplify the implementation, the test chip has been split into two parts: (i) test chip core and (ii) io ring. Each part has been implemented individually. Measurements of the test chip will be conducted in 2016.

![Image](image)

Figure 5: Test chip for validation of PSND

**References**


Synthesis of Low Cost Programmable Logic Controllers

Members: E. Simeu, R. Alhakim, G. Nzebop Ndenoka,

Cooperation: LIRIMA, Equipe IDASCO, Fac. Sciences, Yaoundé Cameroun

Introduction

The widespread automation of production and information processing systems has been a decisive factor in the social and industrial development in developed countries. This has required equipment and advanced technologies in which the PLCs take pride of place. Such a generalization of automation is not applicable in most developing countries because of the prohibitive cost of the equipment required. Nowadays, there is a wide variety of very cheap programmable circuits, which could functionally replace conventional PLCs in low cost automation applications. Unfortunately, these programmable devices are not often used in automation applications because they do not enjoy the benefits of a standardized specification and programming environment such as IEC 61131 standards that have been developed to standardize the specification and the programming of PLCs in automation applications.

The objective of this work is to develop a specification and programming environment that facilitates the direct implementation of programmable circuits of very low cost (such as microcontrollers, FPGAs, microprocessors, ...) in control and automation applications, in lieu of the conventional PLC which is very expensive. This is done in order to popularize the development of automation applications in developing countries for which the conventional PLCs are too expensive and often not available in the academic laboratories.

PLC synthesis using low cost devices

In the IEC 61131-3 standard, there are five IEC standard programming languages [4] allow engineer to specify the operation of discrete event systems, even those who are more complex. However, they do not allow a direct realization on different control target devices like microcontrollers or FPGA. The objective in this work is to build an appropriate software tool that takes in input any PLC control program and treats it by successive refinements to produce an implementation on different types of targeted programmable device.

Several research studies have been occurred in order to find appropriate techniques which allow synthesizing any PLC control specification code and converting it to other executable programs (such as C, Fortran, VHDL) adapted with different hardware architectures [1-3], with a particular focus on the Grafcet model.

Therefore, we have carried out a novel software tool that permits to automatically convert any Grafcet specification code to bin-stream module and deploy it on any economic microcontroller, especially those of the Microchip dsPIC family. That tool takes in entry the functional requirements of the system given in a Grafcet form. In effect, The Grafcet (Graphe Fonctionnel de Commandes et d’Etapes/Transition), one of the five IEC standard programming languages, is a graphic language for modeling automated systems. It is the most international formalism used for high-level description of complex sequential systems [2]. This language is widely used in several domains such as home automation, automotive, power generation, manufacturing, environment, etc. It specifies the behavior of a logic control system that receives input signals, analyzes and generates output signals in form of orders or actions to perform specific acts.

Implementation of the synthesis process

Given a grafcet specification of any logical control system, the synthesis process can be split into multiple steps which are broadly described on Figure 1.

![Figure 1: Synthetic Approach of the solution](image)

The steps of the synthesis process are described as follows:

**Step 1. Functional Design Specification (FDS) of the system:**

The design and development of any system should start with the description of requirements. A FDS is the most important step in the design of any control system. It provides details of the proposed solution to be implemented, to meet user requirements. Thus, FDS is the documentation that defines what the system should do and what the functions and
facilities should be provided by this system in order to satisfy the requirement.

**Step 2. Grafcet model:**
The next step is to represent the technical specification of the system by Grafcet model. We propose UniSim software tool in order to edit Grafcet chart [5]. UniSim, is the graphical user interface (GUI), offering gallery of specific graphical objects (shapes) for all Grafcet elements (such as steps, transitions, transition-conditions and actions). The user can easily select these graphical objects, place them onto a drawing page and attach them together in order to create specific grafcet charts. Furthermore, UniSim tool permits to reformat Grafcet data into XML format [7], this option ensures that this information can be easily processed by another software application, as the GrafcetConverter tool.

**Step 3. GrafcetConverter tool:**
We have built this software tool in order to directly extract the Grafcet data from XML format file and convert it to a particular set of binary data, which is ready to be transmitted to EEPROM microcontroller memory through serial port. Furthermore, GrafcetConverter tool provides a simulation engine with which we can simulate the Grafcet program and verify whether it meets the requirements or not before transmitting it into a microcontroller.

**Step 4. Integrated Circuit:**
We are using the EASYdsPIC4A microcontroller. It is a full-featured and very powerful development system for PIC microcontrollers from Microchip [9]. It comes with a dsPIC30F4013 microprocessor. We have implemented in C language the Grafcet interpretation algorithm [2] for this microcontroller with the MPLAB IDE. The board is programed by generating a program in assembly language and transferring it to the EEPROM of the board through USB cable or RS-232 COM port. The microcontroller is then configured and ready to receive grafcet data of a system. After sending them since the SerialPortTerminal interface, the board should be Relnit to run the program with downloaded data. It then runs and serves as the sit control of the modeled system.

The general system architecture is presented on Figure 2.

This synthesis tool has been used in a case study to automate the optimal switching of energy sources in an autonomous domestic water supply application [6].

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References
Energy modeling and management in wireless sensor networks

Key-words: Wireless Sensor Networks, Energy consumption, cover set, target coverage, approximation algorithms.

Members ; D. Tchuani Tchakonte, E. Simeu, M. Tchuente

Cooperation: LIRIMA, Equipe IDASCO, Fac. Sciences, Yaoundé Cameroun

Introduction

Recent years have witnessed an increased interest in the use of wireless sensor networks (WSNs) in numerous applications. The WSNs help to overcome the constraint of wiring, which significantly limited the deployment of a large number of sensor nodes. It has thus become possible to deploy a network consisting of many collaborative sensors in order to monitor larger area of interest. In these applications, micro-sensor nodes equipped with embedded RF transceiver for communication are deployed to operate autonomously.

This new micro-sensor technology has opened new perspectives for various applications in many fields (disaster management, military, space exploration, environmental monitoring, medical, domestic ...) However, the use of WSNs still poses many challenges both from an algorithmic and practical point of view (deployment, location, autonomy, coverage, collection and data fusion, ...). In particular, energy consumption management is a key element for optimizing network performances. This study focuses on the optimization of the lifetime of the network, which is determined by the lifetime of the batteries. Indeed, the only source of energy of a sensor node is its battery, whose lifetime is limited.

Main objectives

Sensors are generally deployed over the area of interest to cover a set of specified locations called targets. The constraint is that each target should be covered at any time by at least one sensor. The problem of maximizing the network lifetime while preserving coverage of all targets is called target coverage. In a network where the sensors are deployed densely, a partial subset of the sensors can monitor all the targets, while other sensors are maintained in standby or sleep state to save energy. These subsets are cover sets. Assuming that each sensor has its own lifetime, the objective of our study is to find methods to form a collection of set covers and to assign them a period of activation so as to maximize the network lifetime. Since achieving that goal has been proven to be an NP-hard problem, we propose approximation algorithms: two deterministic heuristics and a stochastic one.

Adaptive healing procedure

We have proposed a new adaptive healing procedure to improve the lifetime of wireless sensor networks deployed over an area to monitor a set of targets. This adaptive healing procedure is a local dynamic maintenance procedure that only replaces the failed sensor in the current cover set to form a new one. We greedily build a new set cover by focusing on the coverage of all the critical targets and optimizing the selection of sensor nodes used to cover the maximum number of critical targets and the maximum number of uncovered targets. Another important point of our algorithm is to delete all the redundant sensors when the cover set has been formed. The experimental analysis has been performed to compare our adaptive procedure to the traditional dynamic process. The simulation results show that the new maintenance strategy gives the same network lifetime as the dynamic maintenance but reduces the network unavailability time up to 90 %. This improvement is shown on figure 1.

Figure 1: Improvement of the adaptive process compared to the dynamic process

Black List - based greedy heuristic

We have proposed a new greedy heuristic in order to maximize the network lifetime through the use of the blacklist concept. The basic idea of that algorithm is to build a cover set by avoiding to select more than one sensor which covers a critical target. Since there may be several critical targets in the network, we define a black list of sensors. This black list initially empty is assigned all the sensors we must avoid selecting. A sensor is added to the black list when
another sensor covering the same critical target is selected in the cover set. Therefore, the black list is updated every time when a sensor that covers a critical target is selected. When it is no possible to keep constructing the cover set without the use of a blacklisted sensor, we select the one that covers the highest number of uncovered critical targets. Once all the critical targets are covered, we take into consideration the black list in when selecting the sensors that cover the remaining uncovered targets. We have compared our algorithm to the one proposed by Zorbas and based on a Johnson idea whose goal is to minimize overlapping. Thus, this algorithm avoids selecting sensors that cover the same target by prioritizing the sensor that maximizes the ratio between the number of uncovered targets and the number of already covered ones among those that the sensor covers. Experiments have shown that our algorithm outperforms the existing one. The figure 2-3 depicts some results.

Figure 2: Number of trials among 100 where the algorithm returns the upper bound of the network lifetime

Figure 3: The maximum distance between the algorithm performance and the upper bound of the network lifetime among 100 trials

A genetic based heuristic

We have proposed a stochastic heuristic to maximize the network lifetime. That algorithm iteratively constructs a group of disjoint cover sets through the use of the genetic technique. In our algorithm, an individual is made of a set of disjoint cover sets and its fitness is computed as the sum of the lifetimes of these cover sets. At each iteration, the genetic algorithm randomly creates an initial population, then it generates a new generation by forming a new individual from the cross-over of two randomly chosen ones. This new child is dynamically mutated to ensure that it is actually made of disjoint cover sets. Then, it replaces a randomly chosen individual with a lower fitness. After, a predefined number of generations, the genetic algorithm returns the best individual of the population. Experiments showed that the genetic algorithm performs better in most cases than the black list – based greedy algorithm but at a higher time complexity.

Table 1. Genetic algorithm performance for the coverage of 50 targets.

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References

Team 5 / System Level Synthesis (SLS)

Themes

HW/SW Architectures and CAD software for multiprocessor systems on chip
Specification, modeling, simulation and implementation of embedded systems on chip
Reconfigurable and prototyping

Expertise

Scientific
Integration and optimization of multiprocessor hardware/software systems.

Fields of expertise
Multiprocessor architecture, Network on chip, Memory subsystems, On chip embedded operating system, Fast simulation of digital systems, Methods and tools for system level synthesis, Reconfigurable architectures.

Know-how
Design of integrated circuits and systems, FPGA, Operating systems, Software/hardware integration.

Industrial transfer
Patent pending on predictive cache, 5 CIFRE theses over the 4 last years (2011 – 2015), 2 spin-off projects.

Research keywords

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Reconfigurable : virtualization and prototyping

Keywords: HLS tools, dynamic reconfiguration, FPGA virtualization, ...

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Cooperations: ST Microelectronics, LIG, CEA, GIPSA, STEI-ITB

Contracts: HEAVEN (Persyval), HPES (Persyval), Esprit (Nano2017), VISE(SATT Linksium),...

Reconfigurable architectures, such as FPGA, are commonly used in research activities for a wide range of applications. During the report period, the SLS team has mainly conducted its research on the virtualization of reconfigurable architecture and on the use of FPGA prototype to demonstrate innovative application-specific accelerators. Both research activities are presented in the following sections.

Enabling context switch on reconfigurable system

To provide better computing efficiency, in terms of execution time, power consumption and area in a given technology, MPSoC architectures often integrate application-specific processors (IP). The nature and number of these dedicated hardware tasks are limited and have to be set up at design time. The reconfigurable computing paradigm gives the opportunity to a virtually infinite hardware task pool.

Typical reconfigurable systems are based on a fabric of cells (chunk of hardware resources, which can be dynamically reconfigured to host a hardware task while the rest of system is still running and computing), an interconnect, CPUs and an operating system. Thus, by time-multiplexing the reconfigurable cells, a reconfigurable system can tend towards better performance that heterogeneous one, while preserving flexibility. In spite of their tremendous potential, reconfigurable systems still fail to convince application programmers. One key reason is the cooperative multitasking typically used in reconfigurable systems to relax integration constraints of hardware tasks, while preemptive multitasking is the norm elsewhere. In preemptive multitasking, the operating system can start, pause and resume tasks at demand. In order to satisfy system demands, tasks have to rely on the context-switch technic.

In this work, we have proposed a high-level design flow, that automatically generates hardware tasks with context-switch ability from a C description. The design flow manipulates the intermediate representation of a High-Level Synthesis (HLS) tool to build the context extraction mechanism and to optimize performance for the circuit produced. The method is based on efficient checkpoint selection and insertion of a powerful scan-chain into the initial circuit as illustrated by the Figure 1.

![Figure 1: Proposed design flow](image-url)

The first step of the method consists in selecting good execution points, called hardware checkpoints, to perform a context switch on a reconfigurable resource. The obtained selection ensures that the context switch mechanism will respect the latency demanded by the system and tries to minimize the mechanism costs. The checkpoint selection method relies on a static analysis of the finite state machine of a circuit, accessible through the intermediate representation of the HLS tool.

This scan-chain insertion step manages the extraction of flip-flops or memory content, involved in the previous step. Experiments with the system produced show that it has a low hardware overhead for many benchmark applications, and that the hardware added has a negligible impact on application performance. Comparison with current standard methods highlights the efficiency of our contributions. The prototype tool, called CP3, is open-source.
Hardware acceleration for mining frequent Item set on streams. Extracting information from huge unorganized data has taken an increasing importance in the last decades. This information extraction takes place in a context in which more and more data sources are data streams, i.e. the data is produced by a continuous and uninterruptible source, leading to a virtually infinite amount of data. There exist many algorithms to extract specific patterns from data batches, such as frequent occurrences, association rules, etc. However many algorithms require the ability to store the entire data set in order to scan it several times, in an unconstrained processing time.

In this work, we focus on the Apriori algorithm, the seminal frequent item set mining algorithm, because it requires few or no preprocessing steps and exhibit a high level of fine grain parallelism that can be efficiently used by a specialized hardware device. We specified and implemented a parallel support counting accelerator. We tuned it for a PCIe capable FPGA, using specific placement directives allowing us to reach a global LUT usage of around 90%. We compared our implementation to the most efficient software implementation available today (LCM), and to the Micro Automata Processor board (AP). Depending on the dataset, we reach gains of 2.8x compared to LCM, and gains of above 12x compared to Micron’s circuit. In all cases, we were much more energy efficient, the AP consuming at worst 192W when the FPGA was consuming 24W.

References
Specification, modeling, simulation and implementation of embedded systems on chip

Keywords: simulation, debug, profiling


Cooperations: STMicroelectronics, Magillem Design Services, Kalray, CEA-LETI, UPMC-LIP6

Contracts: COVADEC (FUI), BENEFIC (CATRENE), CAPACITES (Investissements d’avenir), STMicroelectronics, Kalray

Fast simulation strategies

Simulation of large scale integrated multiprocessor platforms is a long lasting theme of the SLS group. This work is of primary necessity as the number of processors in integrated circuits is rising, and therefore the simulation times are increasing constantly. Current manycore systems contains tenths or even hundreds of processors, usually with a VLIW architectures (e.g. Tilera TileGx72 or Kalray MPPA256) for a high performance per watt ration. As a result, the execution of the software on Instruction Set Simulators during simulation (making the processor the ultimate hardware/software interface) is not viable anymore.

![Figure 1: Approximate CFG Mapping](image)

During this year, we have kept on working on dynamic binary translation, targeting a) optimization by studying firstly the behaviour of the translation caches, and secondly the interest of using an intermediate representation which follows the single state assignment principles, and b) accurate time modelling, by taking into account branch predictors. We also applied more broadly our simulation technique to evaluate several hardware/software architectures, by varying the level of parallelism of a given application. We experimented coarse grain parallelism with 1 to 8 processors, and fine grain parallelism through the use of SIMD instructions, to support high throughput applications in the context of driver assistance algorithms. Overall, using 8 cores and SIMD instructions led to a tenfold performance improvement compared to a scalar sequential implementation.

We have also continued our work on native simulation making use of the hardware assisted virtualization support available on modern processors. We were the first to point out in 2009 that the control flow graph (CFG) of code compiled on the target processor was not isomorphic to the CFG of the same code compiled on the host processor, making therefore timing estimates during native simulation at best a wild guess. Thanks to the fact that most compilers use an intermediate representation on which most of the non machine dependent optimizations are done, we defined an approach which does an approximate mapping between a fully optimized target CFG and the partially optimized host code in intermediate representation, as illustrated on Figure 1.

Another topic we focused on has been the native simulation of floating point software. As a matter of fact, and even though floating point representation has been standardized by the IEEE, target to host mapping is not as trivial as it seems, and even the simple example below leads to different results if the machine implements a fuse multiply and add or not.

```c
void main(void)
{
    volatile float a[2] = {0x1.000002p10, 0x1.000002 p10};
    volatile float acc = 0.0f;
    for (int i = 0; i < 100000; ++i)
        acc += -(0x1 .000004 p20f - a[0] * a[1]);
    printf("iterations results = %e\n", acc);
}
```

We devised strategies to perform correct computations under several hypothesis, and we showed that guaranteeing a given behavior is difficult when avoiding full floating point emulation, which costs a lot in term of simulation performance.

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Using simulation for software performance improvement
The goal of this research, done in cooperation with STMicroelectronics, is to help optimize software performance during hardware/software integration, by using simple metrics such as processor stalls and transactions latencies. To that aim, pretty time accurate simulation models are required since the effects of pipeline stalls, cache misses, memory contention and so on are very dependent on the moment at which they occur. Our preliminary results show that the optimization of software using a few prefetch instructions can lead to significant performance gains (up to 25% on data intensive benchmarks). However, our goal is to not to optimize code per se, but to automate the process of finding where to place these instructions taking benefit from the high observability provided by cycle accurate simulation platforms.

Memory hierarchy evaluation and design
Cache coherence has been a long lasting subject in computer architecture. With the emergence of integrated massively parallel machines, this subject is regaining importance, as the available throughput on network-on-chip is much higher than the one available on circuits that were previously implemented on different boards or on multi-chip modules.

A first line of work, done in cooperation with CEA-LIST, aims at quickly evaluating the performance of the handling of the list of sharers in distributed protocols. Indeed, the original way of maintaining this list is to maintain an exact count of the sharing processor by devoting a bit per processor per cache/memory line and perform multicast. Unfortunately, this hardly scales with hundreds or thousands of processors, as the list requires more memory resources than the data itself! Therefore, other ideas have been proposed, such as limiting the number of sharers to, lets say, 5, and perform a broadcast if the list overflows. However, doing experimentations to define the appropriate list size is very time consuming with cycle accurate models, and going up in abstraction is not simple, as contention has to be modeled. We devised a trace based approach which replays the traces and performs cache simulation, allowing to rank the protocols depending on their performance.

A second line of research, done in cooperation with the LIP6 lab in Paris, aims at introducing support for Network-on-Chip virtualization, allowing the implementation of a set of logical networks on top of a physical network. We call this virtualization since its goal is similar for network to the goal of processor virtualization. The technique leverages the Elevator First routing algorithm that we introduced a few years ago, by giving the user of a planar network, for example, the access to the topology of a cube. These virtual networks can be used for running independent applications and guaranteeing that their traffic will stay independent (from a functional point of view). It can also be used to support several traffic classes within a system. In that context, we devised a new cache coherence protocol implementation which uses the virtual network to share data between all caches at a given level, saving resources while still providing the traffic independence and thus the deadlock and livelock freeness properties of the underlying algorithms.

Encoding of serial data
Many modern devices use serial interfaces to exchange data in a reliable fashion at high speed. To get the ability to recover the clock and data from the transmitted data, specific encodings that ensure a minimal number of transitions on the bits and a maximal difference between the number of transmitted zeros and ones are used. Among all encoding, the most used one (in all flavors of USB) is 8b/10b, which encodes a byte using a carefully chosen subset of the 1024 bit combinations available on 10 bit. However, these nice properties come at the cost of a 25% overhead. To minimize this cost, this research, done in cooperation with STMicroelectronics, has led to the definition of a new encoding strategy. This strategy allows to bound both the run length (maximum number of identical bits) and the running disparity (maximum difference in number of 0 and 1 during a transmission), while minimizing the encoding overhead.

Our proposal (see Figure) is based on the combination of scrambling to randomize the data, an on-line polarity bit-insertion algorithm that ensures enough transitions are there without needing to send other information than the data, and a modified bit stuffing approach whose very simple idea is to add “01” or “10” instead of “0” and “1”, thus keeping the balance between 0 and 1 in the frame identical to what it was before bit stuffing, at an acceptable cost. As a result, the overhead for conditions equivalent to the 8b/10b encoding is 17.4%, for a hardware cost of 2 kilo gates. This work led to two patents, and has been discussed in the high-speed link MIPI standard.

References
**HW/SW architecture and CAD software for MPSoC**

**Key-words:** Embedded software, device driver, MPSoC, Network-on-Chip, task migration

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Designing a Multi-Processor System-on-Chip (MPSoC) implies a lot of knowledge specifically when the software interacts with the hardware in terms of architecture and tools. This domain is usually called hardware/software (HW/SW) interfaces.

The long term expertise acquired in the last 10-15 years in this HW/SW interface domain leads to deep scientific and technological breakthroughs: Device driver generation, software task migration in multi-tile architecture, Network-on-Chip (NoC) based systems, and traces analysis.

**Device driver generation**

Sharing the device driver development knowledge is complex (see Figure 1), and writing drivers is an error prone and a time consuming activity. Therefore, we are currently working on automatic driver generation from high-level hardware and software descriptions. From a practical point of view, this would simplify this task much.

In simplest terms, device drivers are means of communication between the kernel and hardware devices. In more advanced terms, a device driver is a specific type of software component/module in the OS that converts requests from higher-level software (e.g., the kernel or an application program) into a series of low-level input/output (I/O) operations specific to a hardware device (e.g., a network interface controller) abstracting the functionality of a physical or virtual device and managing their operation. It hides completely the details of how the device works.

A method, called Me3D, has been investigated to help in device driver generation. Step by step, information is requested from the designers (IP-XACT model of the platform or device, behavior of the driver, ...) for the final generation. Based on that methodology, a work on device driver portability is on-going. The idea is to extract from a C code the main properties of a driver for a specific OS, in order to generate a new version for another OS. Finally, as most of current IPs include a processor, we are also working on the idea of a driverless OS. This means that the driver is embedded with in the IP, and the OS uses standard API to access the driver interface, making what used to be a HW/SW interface a SW/SW interface.

**Task migration in non-SMP architecture**

Task migration is a well know feature in the context of SMP (Symmetrical Multi-Processor) architecture. This becomes very challenging when dealing with non-SMP architecture, and we are developing method and tool to provide such a feature. The main goal is to provide an answer to load balancing, thermal and fault tolerance awareness of processor in MPSoC.

The main idea of task migration is the transfer of a process state plus its address space from the source core (referred to also as home or host node) to the destination one (referred to also as destination node). Its significant cost is coming mainly from the process of transferring the address space. The address space is usually composed of the task stack and heap.
this is not the only task attribute to be transferred. The whole task state including the address space and the CPU registers, open files and ports, have to be transferred to the destination core to be eventually resumed/ restarted properly.

As a solution, we consider task replication: It consists in having replicas of tasks in the system. When a migration is needed, the task is suspended in its source processor and resumed in the destination processor after the transfer of the process state. The destinations for migrating tasks are determined statically prior to compilation and linking. This enables the system level design process more open for optimum locations of migrating tasks. Although the system level designer must be aware of the sources and corresponding possible destinations of all migrate- able tasks, our solution has been designed so that there is no involvement from the programmer side whatsoever regarding the migration process. Our solution is implemented as a layer between the operating system and the application. It has been chosen to utilize OS application software interface APIs without modifying the operating system itself and that's to make the solution capable of being plugged over any operating system.

One of the issues of task migration is the inconsistency in the communication arising from the change of the location where the task is supposed to be running in. This consequently, requires informing all the adjacent tasks to the migrating one in the task graph with its new location after migration to keep sending and receiving tokens correctly. Not only location update is important to keep the communication consistent, but also any remaining unprocessed tokens left in channels FIFOs have to be forwarded/re-sent to the right corresponding FIFOs after migration to ensure consistent completion.

Network-on-Chip based architecture

Network-on-Chip (NoC) is an interesting communication fabric for multi processing element architectures that benefits from the parallelism of algorithms.

We developed a method that uses a symbolic execution technique to extract the parallelism of an application to be mapped on FPGAs using the flexibility of a NoC communication infrastructure and the properties of a high level programming language. An application specific hardware is then generated using a High Level Synthesis flow. We provide a dedicated mechanism for data paths reconfiguration that allows different applications to run on the same set of processing elements. Thus, the output design is programmable and has a processor-less distributed control. This approach of using NoCs enables us to automatically design generic architectures that can be used on FPGA servers for High Performance Reconfigurable Computing.

Traces analysis

The increasing complexity of MPSoC makes the software developers life harder when chasing bugs. Even if executing a program many times is a conventional debugging process, the non-determinism due to parallel execution often leads to different execution paths and different behaviors. We propose an approach based on simulation, to ease pin-pointing bugs in a parallel execution. To that aim, we collect traces using a virtual platform, and when an execution fails, re-execute the traces, in either forward or reverse direction. We define a trace model suitable for this task, and detail a strategy for providing forward and reverse execution features to avoid long simulation times during a debug session. We demonstrate experimentally that re-execution is a deterministic process which, when debugging using the usual trial and error developer approach, is much faster than simulation.

As NoCs become a de facto standard for on-chip systems, traffic generation models become critical for system-on-chip (SoC) design. In that context, we also propose a new framework to process traces generated by message passing applications modeled as acyclic task graphs. This framework builds dependency-aware traffic generators (DATGs) by retrieving the packet dependencies from traces in a single simulation. The DATGs accurately replace the application nodes in emulations or simulations to explore the NoC design space.

References


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Previous degrees: Master

KACHROUDI, Achraf
Title of thesis: Development of new polymer materials for micro-sensors of vibrations
Expected date of defense: 2016
Previous degrees: Master

KALSING, Arthur
Title of thesis: Methods and tools for UPF x RTL correlation
Expected date of defense: 2018
Previous degrees: Engineer (2014)

KAZMA, Rabih
Title of thesis: Ultra High Sensitive CMOS Imager
Expected date of defense: 2016
Previous degrees: Master

KEBAILI, Mejid
Title of thesis: Definition of a structural and functional verification flow for clock domain crossing path on high performance integrated subsystem based on processors.
Expected date of defense: September 2017
Previous degrees: Engineer

LE PELLETER, Tugdual
Title of thesis: Energy consumption study and optimization for Sensor and order functions of an human implant device
Completed on: May 13, 2015
Previous degrees: Master

MALLOUG, Hani
Title of thesis: Built-in test strategies for dynamic test of high-performance Analog-to-Digital Converters
Expected date of defense: 2017
Previous degrees: Engineer

MATOUSSI, Omayma
Title of thesis: Simulation of Multi/Many-core SoC: Non-Functional Aspects and Parallelization
Expected date of defense: 2017
Previous degrees: Engineer (2014)
MKHININI, Asma
Title of thesis: Hardware implementation of homomorphic encryption
Expected date of defense: 2016
Previous degrees: Engineer

NJJOYAH NTAFAM, Perrin
Title of thesis: New performance evaluation methods for early and refined software development on SOC platforms
Expected date of defense: 2017
Previous degrees: Engineer

PASTORELLI, Cédric
Title of thesis: Nonlinear ramp generator for analog-to-digital signal conversion in CMOS imagers
Expected date of defense: 2016
Previous degrees: Engineer

PAYET, Matthieu
Title of thesis: Definition of an integrated emulation environment of Network-on-chip designed for an optimized multi-FPGA platform and its evaluation with financial and spectral imaging applications
Expected date of defense: 2015
Previous degrees: Engineer 3i (2011)

PLASSAN, Guillaume
Title of thesis: Semi-formal verification of clock domain crossing properties
Expected date of defense: December 2017
Previous degrees: Phelma Engineer Degree

PONTIE, Simon
Title of thesis: Design and validation of a secure crypto-processor for cryptography based on elliptic curves
Expected date of defense: 2016
Previous degrees: Agregation, Master M2R in Nano-Electronics and Nano-Technology

RAMOS, Pablo
Title of thesis: Methodology and tools for error rate prediction of applications implemented in advanced processors
Expected date of defense: 2016
Previous degrees: Master, Engineer

RENAUD, Guillaume
Title of thesis: Built In Self Test of pipeline Analog-to-Digital Converters
Expected date of defense: 2016
Previous degrees: Engineer

RENDON, Adrian
Title of thesis: Design and implementation of a piezoelectric micro-generator thermomagnetically triggered for autonomous sensors nodes
Expected date of defense: 2017
Previous degrees: Master (2012)

ROLLOFF, Otto Aureliano
Title of thesis: Design and evaluation of standard cells for asynchronous integrated circuits in low power nanotechnology
Expected date of defense: 2018
Previous degrees: Master (Brasil)

REHMAN, Saif Ur
Title of thesis: Defect Tolerant SRAM-Based FPGA: Design For Test and Diagnosis
Completed on: November 06, 2015
Previous degrees: Master

SALA, Marine
Title of thesis: Dynamic and statistical reliability modeling assessment and circuit/system reliability modeling & monitoring enabling
Completed on: October 02, 2015
Previous degrees: Engineer

SARRAZIN, Guillaume
Title of thesis: Nativesimulation technics for many-core systems
Expected date of defense: 2016
Previous degrees: Engineer

SCHWAMBACH COSTA, Vitor
Title of thesis: Generic Multiprocessor Architectures for Efficient Implementation of Video Analysis Algorithms
Completed on: March 30, 2015
Previous degrees: Master

SIMATIC, Jean
Title of thesis: Design flow for ultra-low power: Non-uniform sampling and asynchronous circuits
Expected date of defense: 2017
Previous degrees: Engineer (2014)

SIVADASAN, Ajith
Title of thesis: Modélisation Spice et FastSpice du vieillissement de circuit et technique avancées pour gérer la fiabilité par le design
Expected date of defense: 2018
Previous degrees: Master
TAKAM TCHENDJOU, Ghislain
Title of thesis: Performance monitoring and errors reconciliation in image decoders
Expected date of defense: 2018
Previous degrees: Master

TCHUANI TCHAKONTE, Diane
Title of thesis: Energy modeling and management in wireless sensor networks
Expected date of defense: 2017
Previous degrees: Master (2011) (Cameroon)

TERRAS, Lydie
Title of thesis: Audit processor for safe and secure embedded systems
Expected date of defense: 2017
Previous degrees: Master 2 (2014)

TRIOUX, Emilie
Title of thesis: Development and 3D integration of piezoelectric materials for energy harvesting applications
Completed on: November 25, 2015
Previous degrees: Engineer (2011)

VARGAS, Vanessa
Title of thesis: Software Environment for the development of reliable concurrent applications on multi-core and many-core platforms
Expected date of defense: 2016

WICAKSANA, Arief
Title of thesis: Portable Infrastructure for Heterogeneous Reconfigurable Devices in a Cloud-FPGA Environment
Expected date of defense: 2018
Previous degrees: Engineer (2015)
Others members of TIMA

Post-Doctoral position and Engineers

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Visitors

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### Trainees

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Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2015 (9).

ANR

ANR / LAUREAT project - Implants cardiaques autonomes intégrant un générateur d'énergie piézoélectrique miniaturisé fiable et robuste (Oct 01, 2014 - Sep 30, 2017)
Partners: Université Paris Sud - Paris 11 VERMON SA SORIN CRM SAS

Ce projet s'inscrit dans les recherches de développements actuels dans le domaine du traitement des insuffisances cardiaques, et plus spécifiquement dans le domaine des pacemakers leadless. Les pacemakers actuels ont un volume assez restreint, de l'ordre de 8cm³, mais leur utilisation requiert l'installation de fils, appelés "leads", qui relient le pacemaker aux zones stimulées électriquement à l'intérieur du cœur. Ces fils, ou leads, sont souvent désignés comme étant le point faible des pacemakers. Problèmes qui peuvent survenir : débranchement du lead, détérioration, infection de lead, perforation cardiaque, dissection du sinus coronaire, thrombose, blessure de valve cardiaque. Des défaillances dues aux leads surviennent dans 21% des cas sur les 10 années qui suivent l'implantation du pacemaker. Les progrès réalisés dans le domaine de la microélectronique et des micro-capteurs permettent à présent d'intégrer tous les composants de pacemaker dans un volume réduit à l'extrême. Un tel pacemaker peut être directement implanté dans une cavité cardiaque sans utiliser de leads. Ce type de pacemaker est ainsi appelé pacemaker leadless. les pacemakers leadless vont très certainement révolutionner les prochaines générations de pacemakers. Outre l'intérêt de supprimer les leads, ces dispositifs permettent de simplifier la procédure d'implantation, d'où une réduction des coûts et une amélioration du confort du patient.

Les progrès réalisés dans le domaine de la microélectronique et des micro-capteurs permettent à présent d'intégrer tous les composants de pacemaker dans un volume réduit à l'extrême. Un tel pacemaker peut être directement implanté dans une cavité cardiaque sans utiliser de leads. Ce type de pacemaker est ainsi appelé pacemaker leadless. les pacemakers leadless vont très certainement révolutionner les prochaines générations de pacemakers. Outre l'intérêt de supprimer les leads, ces dispositifs permettent de simplifier la procédure d'implantation, d'où une réduction des coûts et une amélioration du confort du patient. Avec des objectifs scientifiques concentrés sur la fiabilité et la robustesse du micro-générateur piézoélectrique, le projet LAUREAT vise à développer une brique technologique fondamentale pour aller vers l'industrialisation d'implants cardiaques à très grande durée de vie. Le projet portera sur une nouvelle technologie de micro-générateur piézoélectrique permettant de produire de l'énergie électrique à partir des mouvements du cœur. Le projet contribuera ainsi à ouvrir la voie vers l'industrialisation de pacemakers leadless sans pile, totalement autonome en énergie. L'objectif final est de réaliser une source d'énergie dont la durée de vie sera supérieure à 20 ans (au lieu de 9ans pour les piles au lithium), évitant ainsi des opérations chirurgicales de remplacement de la pile et contribuant à renforcer la compétitivité de l'industrie des dispositifs médicaux en France et en Europe.

ANR / LIESSE project - Effets laser et fautes sur les circuits intégrés dédiés à la sécurité (Oct 01, 2012 - Mar 31, 2016)
Partners: Université de Montpellier II, EC. NAT. SUP. des MINES ST-ETIENNE, Office National d'Etudes et recherches Aérospatiales, STMicroélectronics (Crolles 2) SA, TIMA/INP.

Several means of attacking integrated circuits are reported in the literature (for instance analysis of the computation time, of the correlation between the processed data and the current consumption, of electromagnetic emanation, of the noise caused by the emitted photons, etc.). Among them, laser illumination of the device has been reported to be one important and effective mean to perform attacks. The principle is to illuminate the circuit by mean of a laser and then to induce a faulty behavior. For instance, in so-called Differential Fault Analysis (DFA), an attacker can deduce the secret key used in the crypto-algorithms by comparing the faulty result and the correct one. The main goals of this project are : 1. to study and model the effect of laser shots onto submicronic circuits and 2. to provide efficient tools to circuit designers to prevent such laser attacks. For that, a first sub-goal is to model the effect to laser shots onto deep submicron integrated circuits and to derive electrical and logico-­temporal fault models that can be used in a design flow. A second goal of this project is to develop tools helping the designers to validate their
solutions against laser injections without neither actually having access to expensive laser equipment, nor to fabricate ICs. These tools will allow simulating the laser effects on the basis of the laser fault models developed within the project itself; the designers will thus benefit from the possibility to evaluate soon in the design flow the behavior of the systems with respect to the different parameters and variables highlighted during the experimentation campaigns. In order to accelerate the evaluation process, emulation will be taken into account: generic tools are already available at the partners and they will be refined and adapted to the results obtained during the project. A third goal is to anticipate new attacks based on the effects on these advanced technologies and thus to propose counter-measures for near-future circuits. A final objective of this project in the exploitation of the data collected during the experimental campaigns: the derived error models will be the basis for the definition of new attacks to secured cryptographic systems.

**ANR / ROBUST project - Concevoir un FPGA robuste tolérant aux défauts intégrant le test et le diagnostic**


**Partners:** INSTITUT TELECOM, Université PARIS VI (Pierre et Marie Curie), TIMA / Grenoble-INPG

Le défi auquel le projet veut répondre est de pouvoir utiliser des circuits tout en tolérant la présence de défauts physiques. La réponse à ce défi aura des répercussions sur les modèles des dispositifs, l'architecture, la sûreté de fonctionnement, la sécurité et les outils de CAO. Les circuits reconfigurables de type FPGA connaissent un succès croissant car leur performance et leur capacité d'intégrer des applications très complexes ont directement bénéfi cié de l'évolution technologique. Ces circuits accroissent en permanence leur part de marché relativement aux ASIC. Les partenaires de ce projet unissent leurs compétences pour étudier une nouvelle architecture FPGA à base de SRAM tolérante aux défauts physiques. Pour pouvoir exploiter cette architecture, des outils de configuration seront développés, permettant de contourner les blocs contenant des défauts physiques et de projeter les applications sur les blocs sains. Le projet comportera 4 volets principaux: - Amélioration de la tolérance aux défauts du FPGA par l'amélioration de la robustesse de ses blocs de base. - Développement de méthodes de test et diagnostic afin de générer une cartographie des ressources défectueuses. - Développement d'un outil de synthèse en vue de la tolérance aux défauts de FPGA. - Développement d'outils de configuration du FPGA tolérant les défauts. Les retombées scientifiques et techniques de ce projet sont le développement d'une architecture innovante de FPGA tolérante aux défauts avec l'introduction de la notion de synthèse en vue de la robustesse. Les industriels pourront exploiter les résultats de cette étude aussi bien pour les FPGA autonomes que pour ceux embarqués dans les SoC. En effet, les SoC intégreront de plus en plus des blocs flexibles et reconfigurables en fonction des applications à exécuter.

**ANR / GAME-D project - Guidage d'une Aiguille Médicale instrumentéÉ Déformable**


**Partners:** Université Grenoble I (UJF), CNRS DR-ALPES, Centre Hospitalier Universitaire de Grenoble

Les procédures médicales percutanées, guidées ou non par une imagerie, ont bénéficié des apports des outils de localisation et de navigation. Néanmoins, ces outils restent imparfaits. Dans le cadre de procédures percutanées utilisant une aiguille, nous voulons démontrer que l'on peut offrir au radiologue interventionnel un environnement augmenté qui lui permettra, d'une part, de répondre à sa problématique de maximisation du rapport bénéfice/risque et d'autre part, de repousser ses limites dans la réalisation de gestes jusqu'à ce jour non envisagés du fait d'outils insuffisamment performants.

Deux défis majeurs doivent être relevés pour concevoir la nouvelle génération d'outils d'assistance à la réalisation de gestes de radiologie interventionnelle guidés par une imagerie. 1/ L'hypothèse simplificatrice d'un modèle d'aiguille linéaire peut être source d'imprécisions majeures, pouvant ainsi entraîner des échecs du geste interventionnel, les nouveaux systèmes de navigation doivent donc prendre en compte, en temps réel, les déformations de l'aiguille. 2/ La connaissance de ces déformations et donc des déviations par rapport à une trajectoire idéale nécessite le développement de nouvelles modalités de correction, en temps réel, des trajectoires de l'aiguille.

Un consortium d'experts a été constitué pour relever ces défis: TIMA (Techniques de l'Informatique et de la Micro-électronique pour l'Architecture des systèmes intégrés), qui apporte son savoir-faire en microfabrication et micro-capteurs, a démontré la faisabilité d'une nouvelle modalité d'appréhension des déformations d'une aiguille. 3S-R (Sols, Solides, Structures, Risques) apporte au consortium son expertise dans le domaine de la physique et mécanique du comportement des matériaux et a démontré la faisabilité à contraindre activement la déformée d'une aiguille. TIMC-IMAG (Techniques de l'Ingénierie Médicale et de la Complexité - Informatique, Mathématiques et Applications de Grenoble) spécialisé dans les systèmes de navigation et les gestes médico-chirurgicaux assistés par ordinateur, propose une nouvelle génération d'environnement augmenté. Le CIC-IT (Centre d'Investigation Clinique – Innovation Technologique) du CHU de Grenoble apporte son savoir-faire dans le domaine de l'accompagnement de la maturation d'innovations.
technologiques en Santé en vue de déterminer objectivement et précocement les Services Médicaux 
Attendus associés aux innovations développées dans le projet. IMACTIS, PME spécialisée dans le domaine 
de la radiologie interventionnelle, apporte son expertise dans le développement et l'industrialisation de 
systèmes de navigation d'ailigues sur le marché de la radiologie interventionnelle. La fédération de ces 
experts au sein d’un même consortium permet de couvrir l’ensemble des spécialités (médico-légale, 
radiologie, logiciel, modélisation, électronique, micro-système, commande, mécanique, médico-légal) 
nécessaires pour relever les deux précédents défis.

Au terme de ce projet de recherche industrielle, l’ensemble des éléments scientifiques et techniques, ainsi 
que deux premiers démonstrateurs, seront disponibles pour valider la faisabilité de l’approche envisagée. 
Les enjeux sont perçus comme extrêmement stratégiques, en particulier dans le domaine de la radiologie 
interventionnelle. Nous pensons qu’au moins six publications majeures seront générées par le consortium. 
Enfin, le transfert industriel de ces innovations sera facilité par le partenaire IMACTIS, qui commercialisera 
les produits issus de ces travaux au travers de son réseau de distribution.

ANR / SACSO project - Solutions pour l’auto-adaptation in-situ de systèmes communicants (Jan 01, 
2012 - Nov 30, 2015)
Partners: CNRS Délégation régionale LANGUEDOC-ROUSSILLON, NXP SEMICONDUCTORS France, 
TIMA / Grenoble INPG

Dans le contexte de systèmes très performants et des applications critiques, l'objectif du projet est de 
concevoir des Systèmes Auto-adaptatifs capables de prendre en compte leur environnement proche et de 
s'adapter à différents scénarios. Dans ce projet, nous adressons deux cas d'auto-adaptabilité jusqu'à 
maintenant non-traités: auto-adaptation à l'application et auto-adaptation à l'environnement. 1. Auto-
adaptation à l'application: le fonctionnement d’un système entier dans l'application est limité par le 
fonctionnement de chaque composant. Malheureusement, le fonctionnement des composants individuels est 
dans la plupart des cas optimisé pour une grande gamme de systèmes ou d'applications et pas pour un 
système ou une application spécifique. L'originalité de l'approche proposée dans ce projet consiste à 
‘prévoir’ l'intégration du système au moment de la conception des composants. Le composant est alors 
conçu avec un Circuit d’Auto-adaptation intégré, qui permet au composant de modifier ses caractéristiques 
électriques en toute autonomie une fois qu’il est placé dans l'application, de façon à pouvoir optimiser le 
fonctionnement du système entier. 2. Auto-adaptation à l'environnement: le fonctionnement du système 
dépend aussi des changements de l'environnement; par exemple un téléphone portable communique 
différemment lorsqu’un obstacle est placé dans son environnement et vient perturber son comportement. 
Dans ce cas, le composant pourvu d’un Circuit d’Auto-adaptation peut changer lui-même ses 
caractéristiques électriques en fonction de l'environnement pour optimiser le fonctionnement du système. Le 
contexte d’e-santé est utilisé comme démonstrateur; le projet se concentre sur la télésurveillance pour 
laquelle le patient est équipé d'un capteur qui communique avec un dispositif électronique externe jouant le 
rôle d'une passerelle vers une infrastructure de réseau. Dans ce projet, nous développons des solutions 
génériques pour l'adaptation statique et dynamique d’un dispositif médical utilisé dans des systèmes de 
télésurveillance. Nous avons identifié trois cas majeurs dans les dispositifs électroniques médicaux : 
dispositifs avec “front-end” passif, dispositifs avec “front-end” actif et gestion de la puissance consommée. 
L'objectif de ce projet est d'adresser ces trois cas. Tous les développements seront validés sur deux 
prototypes : un circuit NFC pour illustrer un exemple de “front-end” passif et une pilule électronique pour 
illustrer un exemple de “front-end” actif et de la gestion de la consommation.

ANR / LACIS project - Capteurs d'image couleur adaptatif à son environnement (Oct 01, 2014 - Sep 
30, 2017)
Partners: CNRS Délégation Régionale Alpes SILIOS Technologies

The goal of the LACIS’s project is to demonstrate the validity of a new approach for color and spectral 
imaging sensor and camera systems. The demonstration will be given by building one or two prototypes 
showing the functionality of the novel approach and measuring the improvement compared to the state of 
the art. The novel approach is based on two principles inspired from the human visual system. 
The general goal of the project is to build a demonstrator composed by (1) new filters, either pseudo-random 
6x6 RGB, or multispectral based on COLOR SHADE technology, (2) a locally adaptive color CMOS sensor 
and (3) a motherboard including embedded processing for color or spectral image reconstruction optimized 
for spatio-spectral information. The demonstration will be given by a functioning prototype that will deliver 
images of size 256x256 and showing the properties of the new approach for color or spectral sensor.
ANRT

ANRT / CIFRE Matthieu PAYET project - Fabrication d'un prototype de plateforme pour l'émulation de NoC et sur un environnement d'aide à la conception, exploration et évaluation du système (May 15, 2012 - May 14, 2015)
Partners: Université Jean Mone (UJM) Laboratoire Curien, CNRS, UJF/Laboratoire TIMA, Floralis, Sté ADACSYS

ANRT / CIFRE Guillaume PLASSAN project - Semi-formal verification of clock domain crossing properties (Apr 07, 2014 - Apr 07, 2017)
Partners: ATRENTA France

ANRT / CIFRE Mélanie BERNARD project - Adéquation algorithme-architecture pour le traitement de données associé aux dispositifs d'imagerie gamma à base cdZnTe (Oct 24, 2014 - Oct 23, 2017)
Partners: CEA

ANRT / CIFRE GANA Mohamed project - "Méthodes et outils pour l'intégration de structures faible consommation pour circuits intégrés complexes basé sur un contôle distribué asynchrone" (Nov 01, 2013 - Oct 31, 2016)
Partners: Sté DEFACTO Technologies SA

ANRT / CIFRE Marina SALIVA project - Dynamic and statistical reliability modeling assessment and circuit/system reliability modeling & monitoring enablement (Oct 01, 2012 - Sep 30, 2015)
Partners: ST Microelectronics (Crolles2) SAS, TIMA/INPG SA

ANRT / CIFRE IORDACHE Mihai project - "Power estimation and reduction in 3D designs" (Jun 03, 2014 - Jun 02, 2017)
Partners: Sté ATRENTA France (Grenoble) SAS

ANRT / CIFRE Guillaume SARRAZIN project - "Techniques de simulation native de systèmes many-core" (Jan 01, 2013 - Dec 31, 2015)
Partners: ST2 KALRAY SA

ANRT / CIFRE Cédric PASTORELLI project - "Système de conversion analogique / numérique auto-testable à base de technique Sigma-Delta adaptée aux capteurs d'images CMOS" (Feb 18, 2013 - Feb 17, 2016)
Partners: STMicroélectronics (Grenoble 2) SAS, GRENOBLE INP & INPG ENTREPRISE SA

ANRT / CIFRE Emilie TRIOUX project - Développement et intégration en 3D de matériaux piezoelectriques pour les applications de récupération d'énergie (Jun 27, 2012 - Jun 26, 2015)
Partners: ST Microélectronics SA, Ecole Polytechnique Fédérale de LAUSANNE, UJF/Laboratoire TIMA, FLORALIS

Partners: STMicroelectronics (ROUSSETS) SAS

ANRT / CIFRE Ajith SIVADASAN project - Modelisation Spice et FastSpice du vieillissement de circuit et technique avancés pour gérer la fiabilité par le design (Jan 01, 2015 - Dec 31, 2017)
Partners: STMicroelectronics
ANRT / CIFRE Mejid KEBAILI project - Développement d’un flot de vérification structurelle, fonctionnelle et dynamique des chemins asynchrones avec les méthodologies et outils de vérification formelle appropriés, pour des sous systèmes intégrés haute performance à base de processeurs (Apr 07, 2014 - Apr 07, 2017)
Partners: STMicroelectronics

Partners: STMicroelectronics

ANRT / CIFRE Thomas DUCROUX project - Parallélisation d'application et gestion basse-consommation sur des architectures "multi-processeurs" (Feb 06, 2002 - Feb 06, 2015)
Partners: STMicroelectronics

ANRT / CIFRE Alexandre AYRES project - "Intégration monolithique en 3D : Etude du potentiel en terme de consommation, performance et surface pour le noeud technologique 14nm et au-delà" (Jul 01, 2014 - Jun 29, 2017)
Partners: STMicroélectronics (Crolles2), CEA-LETI, CNRS délégation ALPES
Intégration monolithique en 3D : Etude du potentiel en terme de consommation, performance et surface pour le noeud technologique 14nm et au-delà

ANRT / CIFRE Julien SAADE project - "Une approche générique au niveau système pour la conception de liens série très haut débit" (Jan 30, 2014 - Jan 29, 2017)
Partners: STMicroélectronics (Alps) SAS, TIMA / INPG SA

ANRT / CIFRE Ahmed BENHASSAIN project - Management in-situ et endurcissement au vieillissement des circuits (Dec 02, 2013 - Dec 01, 2016)
Partners: ST Microélectronics (Grenoble 2) SAS, TIMA / INPG SA
Management in-situ et endurcissement au vieillissement des circuits

ANRT / CIFRE Cheikh NDIAYE project - "Fiabilité des Circuits pour les Applications Analogiques" (Apr 22, 2014 - Apr 21, 2017)
Partners: ST MICROELECTRONICS (Crolles2) SAS

ANRT / CIFRE Thomas DUCROUX project - Parallélisation d'application et gestion basse-consommation sur des architectures multi-processeurs (Feb 06, 2012 - Feb 05, 2015)
Partners: ST Microélectronics

CEC

CEC / NANOxCOM project - (Dec 01, 2015 - Nov 30, 2019)
The main goal of this project is developing a complete synthesis and optimization methodology for switching nano-crossbar arrays that leads to the design and construction of an emerging nanocomputer. New computing models for diode, FET, and four-terminal switch based nanoarrays are developed. The proposed methodology implements both arithmetic and memory elements, necessitated by achieving a computer, by considering performance parameters such as area, delay, power dissipation, and reliability. With combination of arithmetic and memory elements a synchronous state machine (SSM), representation of a computer, is realized. The proposed methodology targets variety of emerging technologies including nanowire/nanotube crossbar arrays, magnetic switch-based structures, and crossbar memories. The results of this project will be a foundation of nano-crossbar based circuit design techniques and greatly contribute to the construction of emerging computers beyond CMOS.

The topic of this project can be considered under the research area of “Emerging Computing Models” or “Computational Nanoelectronics”, more specifically the design, modeling, and simulation of new nanoscale witches beyond CMOS. The topic is well addressed and fit in H2020 work programmes FET (Future and Emerging Technologies) and ICT-25 (Generic Micro- and Nano-electronic Technologies).
CEC-NATIONAL

CEC-NATIONAL / THINGS2DO project - Le projet THIGS2DO a pour but de créer Conception et développement de produits exploitant la technologie FDSOL (Jan 01, 2014 - Dec 31, 2017)
Partners: Union européenne, État, collectivités locales, autres personnes publiques...

La technologie FDSOL offre des perspectives uniques est un atout important pour la compétitivité des acteurs de l'industrie européenne dus semi conducteur. Aujourd'hui le premier nœud technologique FDSOL est disponible en 28 nm et offre des performances uniques alors que les technologies concurrentes connaissent un infilchéchissement dans leur processus. Le prochain nœud technologique FDSOL en 14 nm offrira des capacités d'intégration encore jamais atteinte.

CEC-NATIONAL / ELESIS project - European Library-based flow of Embedded Silicon test Instruments (Jun 01, 2012 - Sep 30, 2015)
Partners: NXP SEMICONDUCTORS France, ST MICROELECTRONICS (GRENOBLE 2) SAS, ATMEL NANTES SA, CEA, IROC TECHNOLOGIES, CNRS/DELEGATION LANGUEDOC ROUSSILLON, TEMENTO SYSTEMS, INFINEON TECHNOLOGIES AUSTRIA, INPG/TIMA, INESC PORTO, UNIVERSITEIT TWENTE, D4T SYSTEMS, JTAG TECHNOLOGIES B.V.

The ELESIS project is focused on improving the industrial test infrastructure for Integrated Circuits, leading to safe, reliable, high quality and low cost semiconductors products in Europe. The project is relevant to the Design Technologies domain and is addressing the Grand Challenges managing complexity, managing diversity and design for reliability and yield. ELESIS is a very ambitious project which plans to cover the mentioned targets (Safety, reliability, high quality and low cost) for mixed signal circuits in addition to digital, with special focus on Analog, RF and Sensors. The ELESIS project will also target a European Standard Interface to reduce test complexity and to manage access to the internal IP blocks from the top level IC. We will address the most important aspects of semiconductor testing within a framework of so-called “embedded test instruments” controlled through a common interface that is needed to ensure the best solutions to reach our challenging targets. The proposed standard interface will have a large economic impact by the creation of an Open Source Platform, which could be used by IP, IDM and Fabless companies in Europe and even worldwide.

EUREKA

EUREKA / BENEFIC project - Besst ENergy Efficiency solutions for heterogeneous multi-core Communicating (Jul 01, 2013 - Sep 30, 2016)
Partners: ST Microélectronics (GRENOBLE 2) SAS, ATRENTA France SAS, ST Microélectronics SA, Commissariat à l'Energie Atomique et aux Energies Alternatives THALES RESEARCH AND TECHNOLOGY THALES COMMUNICATION & SECURITY SAS CNRS MOY2000 COTE D'AZUR

Fournir une approche holistique intégrant de nouvelles sources de récupération d'énergie ("Harvesting Energy) et des approches novatrices de distribution d'énergie pour nos systèmes.

EUREKA / RESIST project - RESilient Integrated Systems (Sep 01, 2014 - Aug 31, 2017)
Partners: STM Microelectronics (CROLLES2) SAS STMicroelectronics SA IROC TECHNOLOGIES ISEN-TOULON ATMEL NANTES SA
Les systèmes électroniques des voitures et des avions deviennent de plus en plus sophistiqués et nécessitent toujours plus d'intégration et de performances. Cependant, l'utilisation de technologies fortement intégrées compromet la fiabilité, la sécurité et la durée de vie des systèmes. Il faut donc de nouvelles approches et solutions de design qui prennent en compte ce besoin de fiabilité. Le projet RESIST vise ces méthodes de design ainsi que des méthodes d'adaptation en temps réel pour la prochaine génération de systèmes électroniques durcis, résistants et adaptatifs pour en particulier l'automobile, l'aviique et l'aérospatial. RESIST se concentre sur la fiabilité, la résilience, le coût et la qualité des circuits à base de semi-conducteurs.
INDUSTRIE

INDUSTRIE / Contrat de collaboration d'Emmanuel SIMEU project - "Etude des systèmes de détection d'erreurs et compensation intégrées dans le décodeur vidéo numérique appuyant sur des techniques d'analyse statistique" (Apr 02, 2012 - Apr 01, 2015)
Partners: ST Microélectronics (Grenoble2) SAS, Grenoble INP & INPG Entreprise SA

With the evolution of multimedia technologies and requirements in quality of images being viewed by users, digital video decoders must provide satisfactory quality to decoded video. Then a new challenge arises which consists to ensure the best perceptual quality as possible to images at the output of multimedia devices, regarding to human visual perception. We then attempt to establish supervision loop of visual quality within a digital video decoder.

In modern video decoders, concealment of artifacts is mainly processed during a post processing stage in the time domain. These concealment methods seem to be reaching their limits due to the complexity of sequential systems architecture. Incorporating a monitoring and conciliation process faithfully with the human visual system into the video decoding loop is becoming a key challenge for the video decoder designers. This research program consisted in studying the error detection and compensation systems integrated into a digital video decoder based on advanced statistical analysis techniques. The goal is to develop a video quality assessment algorithm which enables real-time monitoring of video quality for standardized video decoders such as H.264 and achieve satisfactory correlation with judgment of human observers. One of the main contributions of the project is the supervision of a Multimedia system by a video Quality Monitoring Tool (VQMT) strongly correlated with human visual perception aiming to ensure a high level of visual quality of decoded images.

MINISTERES-FUI

Partners: UNIVERSITE de BRETAGNE SUD DOLPHIN INTEGRATION STMICROELECTRONICS ROUSSET SAS

Le projet SPICA vise une solution innovante pour les domaines de la vérification, de la sûreté et de la sécurité des systèmes critiques. L'objectif est le développement de méthodes et outils pour l'instrumentation automatique des systèmes sur puce complexes critiques par des composants dédiés à la vérification d'exigences de bonne conception, la sécurisation du dispositif, et la détection de dysfonctionnements et de malveillance en opération. L'originalité de l'approche proposée réside dans le fait qu'elle decline et exploite des concepts similaires dans les trois principales composantes de la conception : le système global, le logiciel embarqué, et les blocs matériels dédiés.

MINISTERES-FUI / LISA project - "Ultra low power Integrated circuit for Secure RF" (Mar 26, 2014 - Sep 25, 2017)
Partners: DOLPHIN INTEGRATION SMART PACKAGING SOLUTIONS UNIVERSITE D'AIX MARSEILLE MORPHO STARCHIP

Le marché sans contact /dual interface est en pleine croissance dans les 3 principaux domaines : le transport, l'identité et le bancaire. C'est l'industrie de la carte à puce des années 90 qui est à l'origine des produits sans contact actuels (Puce, Module, Antenne, Inlay). Le projet LISA propose de finaliser ce processus et de développer des objets sans contact, basée sur un nouveau module RF (13,56 Mhz/10 cm de portée) dual interface intégrée (puce & antenne) compatible avec les infrastructures existantes (mêmes lecteur), sans alimentation extérieure et compatible avec moyens actuels de production. Son objectif majeur est de diviser par 10 le besoin énergétique des solutions actuelles à performances égales. A cette fin les partenaires se fixeront comme sous objectifs de diviser par 5 la consommation de la puce et multiplier par 2 l'énergie récupérée par l'antenne.
Projet consistant à développer un ensemble de méthodes et techniques permettant la Conception et la Validation des systèmes Embarqués d’Aide à la conduite automobile, d’optimiser les scénarios de tests et ainsi réduire les centaines de milliers de km d’essais nécessaires à la validation des fonctions ADAS intégrés dans les véhicules, d’optimiser les phases de validation des systèmes ADAS en temps et effort humain, de répondre aux besoins des systèmes d’Aide à la conduite en terme de conformité aux normes de fiabilité fonctionnelle (L’ISO 26262), de prendre en compte des exigences de sûreté de fonctionnement en amont du développement des algorithmes de traitement d’image, d’accompagner le développement des fonctions ADAS et d’assurer l’interopérabilité entre les plateformes de tests avec les autres plateformes de développement (RTMAPS, ADTF) et de simulation (PRO-SIVIC).

MINISTERES-FUI / COVADEC project - COnception et VAlidation Des Systèmes Embarqués d’Aide à la Conduite (Sep 18, 2013 - Aug 30, 2016)
Partners: ALL4TEC, CIVITEC, INTEMPORA, MAGILLEM, PEUGEOT CITROEN AUTOMOBILES SA, VALEO ETUDES ELECTRONIQUES, ARMINES Laboratoire, GRENOBLE-INP/TIMA

L’objectif du projet est d’améliorer le processus de conception des systèmes sur puce exigeant une forte maîtrise de leur dissipation de puissance. L’appareillage nomade, le calcul intensif et les infrastructures de télécommunications, tireront profit des solutions issues de ce projet. Les bénéfices attendus sont une meilleure productivité des équipes de conception et une qualité accrue des circuits développés vis-à-vis de leur consommation. L’innovation soutenue par le projet consiste à briser le cloisonnement existant entre des niveaux du processus de conception en usage, et plus particulièrement entre d’une part le niveau architectural, propre à définir l’agencement des composants d’un circuit, et d’autre part les niveaux RTL et portes logiques, où l’implémentation d’un circuit est menée. Dans ce cadre, des techniques automatisées portant sur les aspects d’estimation de la consommation, de vérification des représentations du circuit et d’insertion de structures dites de “low power” seront proposées. Elle seront unifiées par un flot formalisé, ascendant et descendant, centré sur le niveau architecture et couvrant en complément les niveaux RTL et portes logiques. En comparaison, les solutions de conception actuelles, relativement à la consommation d’énergie, forment une succession de tâches disparates, fortement manuelles dans le sens ascendant du flot, et centrées au niveau RTL. Grâce à la mise en place d’un flot structuré et composé de tâches cohérentes, une réduction d’un facteur 10 du temps consacré aux aspects basse consommation dans la partie amont du cycle de conception est ainsi envisagée. Ceci se traduira par une compétitivité significativement améliorée sur le marché des systèmes sur puce à faible dissipation de puissance.

MINISTERES-FUI / HICOOL project - Solutions amont pour la conception orientée basse consommation de circuits intégrés complexes (Aug 01, 2012 - Sep 30, 2016)
Partners: ST Microélectronics (Grenoble2) SAS, DEFACTO TECHNOLOGIE, DOCEA POWER, CNRS, GRENOBLE-INP/TIMA

Né d’un challenge d’innovation interne à STMicroelectronics, le projet TOUCHIT porte sur le développement d’une solution pour ajouter la notion de retour haptique à toutes les interfaces avec un écran tactile grand public (téléphone, ordinateur portable, tablette PC, touch pad, télécommande…). Par définition, l’haptique est la science du toucher. Dans le cadre du projet, nous appellerons haptique la notion de rendu de texture, contour de forme, relief... La volonté du projet est de révolutionner le domaine des écrans tactiles et ceci en suivant plusieurs axes: - l’implémentation d’une solution de retour haptique unique, offrant une finesse de restitution tactile jamais atteinte ; - le développement d’une plateforme silicium combinant des technologies de dépôt de couches piézoélectriques et des solutions de packaging par report puce à puce ; - la définition de nouvelles applications embarquées avec comme finalité une meilleure interaction homme-machine, plus intuitive, ludique et efficace grâce à la compréhension des mécanismes psychophysiques liés au frottement.

MINISTERES-FUI / TOUCHIT project - Tactile Open Usage with Customized Haptic Inter face Technology (Mar 01, 2012 - Mar 30, 2016)

CAPACITES vise à émerger une plateforme matérielle et logicielle s’appuyant sur l’exploitation de processus pluri-coeurs intégrés et de démontrer la pertinence des ces architectures pluri-coeurs et l’implémentation qu’en fait KALRAY pour plusieurs applications industrielles.
SATT

SATT / VISE project - (Jun 01, 2015 - Sep 30, 2016)
Partners: SATT Linksium

Collectivités Territoriales

NANO 2017 - BIST ADC project - Le développement de techniques d'adaptation algorithmique intégrant la perception visuelle et son implémentation sur SoC pour l'amélioration de la qualité d'images vidéo. (Jan 01, 2014 - Dec 31, 2017)

Ce projet vise le développement de nouvelles structures embarquées pour le test dynamique SoCs mixtes visant en particulier des techniques de test pour les ADCs et les capteurs de bruit. deux thèmes de recherche sont visés par ce projet : 1) Test de convertisseurs analogique/numérique et 2) Mesures de bruits dans des SoCs mixtes. Le laboratoire TIMA a fourni quatre livrables début 2015 décrivant les tâches réalisées : D1.1 Rapport sur l'évaluation de l'état de l'art sur les structures intégrées de test dynamique d'ADC. D1.2 Rapport sur les opportunités identifiées afin de définir de nouvelles stratégies de test ou l'amélioration de celles existantes. D2.1 Rapport sur l'évaluation de l'état de l'art de structures des instruments de test pour la détection et l'analyse de la gigue. D2.2 Rapport sur les opportunités identifiées pour définir de nouvelles stratégies de test ou l'amélioration de celles existantes. Dans ces livrables nous nous focalisons sur l'identification des lignes de recherche pour développer avec succès des instruments intégrés dans applications de BIST dynamique de convertisseurs de signal et de détection de bruit pour les applications de hautes performance.

NANO 2017 - A3 project - le développement de nouvelles structures embarquées pour le test dynamique de SoCs mixtes visant en particulier des techniques de test pour les ADCs et des capteurs de bruits (Jan 01, 2014 - Dec 31, 2017)

Ce projet vise le développement de techniques d'adaptation algorithmique intégrant la perception visuelle et son implémentation sur SoC pour l'amélioration de la qualité d'images vidéo. deux thèmes de recherche sont visés par ce projet : 1) Compression fonctionnelle paramétrique (CFP) après décodage HEVC Ultra+HD 10 bit. 2) correction des artefacts vidéo (CAV) après décodage HEVC Ultra HD 10-bit. Un rapport de fourniture a été fourni. La toute première phase de l'étude a concerné l'utilisation des méthodes avancées d'analyse statistique pour la détection d'erreur intégrée dans décodeur d'image. Dans la suite il s'agira de s'appuyer sur les méthodes d'évaluation de la qualité visuelle d'image développée pour optimiser les algorithmes de la compression tout en préservant le niveau de qualité visuelle de l'image exigé après la décompression. L'objectif est de développer une boucle de surveillance et d'ajustement de la qualité visuelle dans un décodeur vidéo numérique, mettant en œuvre des méthodes de détection et correction adaptative d'artefacts vidéo basées sur la correction de distance et la régression non-linéaire en s'appuyant sur des méthodes statistiques avancées. Le but visé est de garantir une qualité de perception d'images restituée confortable pour le système visuel humain.

NANO 2017 - ESPRIT project - le développement d'une solution matérielle et logicielle efficace pour le pattern mining dans des flux de données à très haut débit en collaboration avec le laboratoire LIG de Grenoble (Jan 01, 2014 - Dec 31, 2017)
Partners: Laboratoire LIG
International activities

This section gives an overview of international activities in which the members of the Laboratory participated.

International cooperation agreements

The Laboratory is engaged or has been recently engaged in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations took various forms, e.g. extended visits of researchers at the cooperative location, organization of joint research, organization of workshops, etc.

Architectures and Methods for Resilient Systems (AMfoRS)

- Ecole Nationale d'Ingénieurs de Sousse (ENISo), Sousse, Tunisia and Faculté des Sciences de Monastir (FSM), Monastir, Tunisia (from 2012)
  This cooperation involves exchanges and collaborations both on research and teaching sides. In terms of research, a co-tutelle thesis has been started in 2014 between TIMA and the laboratory of Electronics and Microelectronics (LEµE) at FSM. Work has also been done in collaboration with A. Ammari, Assistant Professor at ENISo. A PhD student at LEµE was invited at TIMA for a 3-month period in 2014. In terms of teaching, R. Leveugle was invited in June 2013 to contribute on a review of curricula at ENISo. He was also invited in November 2013 to teach a course on hardware security for two departments of ENISo. The team offered 6 trainee positions to last year students of ENISo in 2013 and 2014; two of them are currently pursuing as PhD students. A third one spent one year as engineer in the team in 2015; he is now working for Airbus. A long-term agreement about student exchanges has also been discussed with INP.

- Département de Physique, UFR des Sciences et Technologies, Université Assane Seck de Ziguinchor, Senegal (from 2014)
  A collaboration has been started between R. Leveugle and A. Ndiaye, Assistant Professor at Université Assane Seck de Ziguinchor, on the design of lightweight crypto-processors. A. Ndiaye was invited at TIMA for a 2-month period in 2015.

- Université de Massachussets à Amherst (2015)
  Coopération dans le cadre d’un projet européen COST MEDIAN concernant l'étude de fiabilité de nanowires dans des technologies 3D monolithiques (L. Anghel)

Design of integrated devices, circuits and systems (CDSI)

- Federal University of Minas Gerais (UFMG), Brazil (2014-2016)
  Title: Making a technique for transient-fault robust circuits feasible
  Programme: Brazilian UNIVERSAL MCT/CNPq Program
  Leaders: Frank Sill Torres (UFMG), Rodrigo Possamai Bastos (TIMA)

Reliable Mixed signal Systems (RMS)

- University of Yaoundé I Cameroun, CETIC Project: African Centre of Excellence in Information and Communication Technologies
  Title: Low Cost Embedded Control Devices
  Leader: Emmanuel Simeu (TIMA)
**Organisation of International Conferences, Workshops, Forums in 2015**

In the following table, TIMA researchers were involved in the organization of the listed events.

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<td>MORIN-ALLORY K.</td>
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<td>NICOLAIIDIS M.</td>
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<td>PETROT F.</td>
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<tr>
<td>DDECS</td>
<td>IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems</td>
<td>Belgrade Serbia</td>
<td>Program Committee</td>
<td>BORRIONE D.</td>
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<td>DFTS</td>
<td>Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium</td>
<td>Amherst (MA) USA</td>
<td>Program Committee</td>
<td>ANGHEL L.</td>
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<td>DTIS</td>
<td>IEEE Design and Test of Integrated Systems</td>
<td>Naples Italy</td>
<td>Topic Chair</td>
<td>ANGHEL L.</td>
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<td>Program Committee</td>
<td>STRATIGOPOULOS H.</td>
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<td>ETS</td>
<td>IEEE European Test Symposium</td>
<td>Cluj-Napoca Romania</td>
<td>Steering Committee</td>
<td>ANGHEL L.</td>
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<tr>
<td>FAC</td>
<td>Frontiers on Analog CAD</td>
<td>Austin, TX, USA</td>
<td>Program Committee</td>
<td>STRATIGOPOULOS H.</td>
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<td>FDL</td>
<td>Forum on specification and Design Languages</td>
<td>Barcelona, Spain</td>
<td>Program Committee</td>
<td>BORRIONE D.</td>
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<td>PIERRE L.</td>
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<tr>
<td>ICM</td>
<td>27th IEEE International Conference on Microelectronics</td>
<td>Casablanca Morocco</td>
<td>Publicity Chair Program Committee</td>
<td>SIMEU E.</td>
</tr>
<tr>
<td>IDT</td>
<td>10th IEEE International Design &amp; Test Symposium</td>
<td>Dead Sea, Jordan</td>
<td>Program co-chair</td>
<td>MIR S.</td>
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<td>Program Committee</td>
<td>STRATIGOPOULOS H.</td>
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<tr>
<td>IMSTW</td>
<td>20th International Mixed-Signal Testing Workshop</td>
<td>Paris, France</td>
<td>Program committee</td>
<td>BARRAGAN M.</td>
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<td>Finance chair</td>
<td>FOURNERET-ITIÉ A.-L.</td>
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<td>IOLTS</td>
<td>21st IEEE International On-Line Testing Symposium, Halkidiki, Greece</td>
<td>Steering committee: MIR S.</td>
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<td>General chair: STRATIGOPOULOS H.</td>
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<tr>
<td>ISVLSI</td>
<td>IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2015), Montpellier, France</td>
<td>Program committee: ANGHEL L.</td>
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<td>Topic Chair: ANGHEL L.</td>
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<td>ITC</td>
<td>IEEE International Test Conference, Anaheim, CA, USA</td>
<td>Program Committee: STRATIGOPOULOS H.</td>
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<tr>
<td>LASCAS</td>
<td>6th IEEE Latin American Symposium on Circuits and Systems, Montevideo, Uruguay</td>
<td>Program Committee: MIR S.</td>
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<td>LATS</td>
<td>Latin-American Test Symposium, Puerto Vallarta, Mexico</td>
<td>Program Committee: LEVEUGLE R.</td>
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<td>NANOARCH</td>
<td>IEEE International Symposium on Nanoscale Architectures, Boston, MA, USA</td>
<td>Program Committee: ANGHEL L.</td>
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<tr>
<td>NEWCAS</td>
<td>13th IEEE International NEWCAS Conference, Grenoble, France</td>
<td>IEEE liaison: FESQUET L.</td>
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<td>Finance chair: FOURNERET-ITIÉ A.-L.</td>
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<td>Publicity: POSSAMAI BASTOS R.</td>
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<tr>
<td>PowerMEMS</td>
<td>The 15th Int. Conference on Micro and Nanotechnology for Power Generation and</td>
<td>Program Committee: S. BASROUR</td>
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<td></td>
<td>Energy Conversion Applications, Boston (MA) USA</td>
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<td>TVHSAC</td>
<td>4th IEEE International Workshop on Test and Validation of High Speed Analog</td>
<td>Program chair: BARRAGAN M.</td>
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<td></td>
<td>Circuits, Anaheim (CA), California</td>
<td>Program Committee: STRATIGOPOULOS H.</td>
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<td>VARI</td>
<td>European Workshop on CMOS Variability, Salvador, Brazil</td>
<td>Program Committee: STRATIGOPOULOS H.</td>
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<tr>
<td>VLSI-SoC</td>
<td>IFIP/IEEE International Conference on Very Large Scale Integration, Daejeon,</td>
<td>Working group chair: BORRIONE D.</td>
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<td>Korea</td>
<td>Steering committee chair: MIR S.</td>
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<td>Program Committee: MAISTRI P. PIERRE L.</td>
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<td>WTS</td>
<td>IEEE VLSI Test Symposium, Napa (CA) USA</td>
<td>Program chair: ANGHEL L.</td>
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<td>Steering committee: NICOLAIDIS M.</td>
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<td>Program Committee: STRATIGOPOULOS H.</td>
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</tbody>
</table>
Participation to Societies and Working Groups in 2015

Co-Chair of IEEE European Computer Society Test Technology Technical Council (L. Anghel)
Chair of IFIP 10.5 Working Group (D. Borrione)
Member of IFIP 10.5 Working Group (S. Mir)
Member of the IEEE P1687 Working Group (M. Portolan)
Member of the IEEE System JTAG initiative (M. Portolan)
Global Coordinator for the TTTC's E. J. McCluskey Doctoral Thesis Award (M. Portolan)
TTTC Award Co-Chair (M. Portolan)
IEEE Solid-State Circuits Chapter Chair (L. Fesquet)
Chair of the IEEE Computer Society Test Technology Technical Council (M. Nicolaidis)

Awards and distinctions in 2015

Best Paper Award at Design Automation and Test in Europe Conference (DATE’2015)
Title: Digital circuits reliability with in-situ monitors in 28nm fully depleted soi
Authors: Marine Saliva¹, Florian Cacho¹, Vincent Huard¹, Xavier Federspiel¹, Damien Angot¹, Ahmed Benhassain¹, Alain Bravaix² and Lorena Anghel³ (¹STMicroelectronics, ²IM2NP-ISEN, ³TIMA)

Best Paper Award at the 20th IEEE European Test Symposium (ETS 2015)
Title: High frequency jitter estimator for socs
Authors: H. Le Gall¹, R. Alhakim², M. Valka², S. Mir², H.G. Stratigopoulos², E. Simeu² (¹STMicroelectronics, ²TIMA)

Best Paper Award at “48th International Symposium on Microelectronics (ISM 2015)
Title: Line coding methods for high speed serial links
Authors: Abdelaziz Goulahsen¹, Julien Saadé², Frédéric Pétrot² (¹STMicroelectronics, ²TIMA Laboratory)

Best Poster Award at " 6th Micromechanics and Microsystems Europe workshop" (MME 2015)
Title: Characterization of a smartphone size haptic rendering system based on thin-film ALN transduction on glass
Authors: F. Bernard¹², F. Casset³, J.S Danel³, C. Chappaz², S. Basrour¹
¹TIMA, ²STMicroelectronics, ³CEA-LETI

Best Special Session Award at “IEEE 33rd VLSI Test Symposium” (VTS’15)
Title: Special session on statistical test methods
Educational tasks

Dealing with problems risen by advanced technologies and proposing advanced design and test methodologies, TIMA members are, as a matter of fact, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people.

Open Seminars at TIMA

In addition to internal seminars, the Laboratory regularly publicises talks given by our visiting researchers. Grenoble academic and industrial researchers had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>SPEAKER</th>
<th>INSTITUTION</th>
<th>DATE</th>
<th>THEME</th>
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<tr>
<td>Etienne Le Coarer, Mathieu Barthelemy</td>
<td>Université Joseph Fourier - IPAG (Institut de Planétologie et d’Astrophysique de Grenoble)</td>
<td>29/01/15</td>
<td>Présentation du Centre Spatial Universitaire</td>
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<tr>
<td>Mejid Kebaili</td>
<td>Laboratoire TIMA - Equipe AMfoRS</td>
<td>04/05/15</td>
<td>Verification of multi-clock systems</td>
</tr>
<tr>
<td>Simon Pontié</td>
<td>Laboratoire TIMA - Equipe AMfoRS</td>
<td>08/06/15</td>
<td>Robustness of unified operations in elliptic curve cryptography</td>
</tr>
<tr>
<td>Michele Portolan</td>
<td>Laboratoire TIMA - Equipe AMfoRS</td>
<td>03/07/15</td>
<td>Complex test scheduling based on IEEE 1687</td>
</tr>
<tr>
<td>Antonio José Gines Arteaga</td>
<td>TIMA Laboratory, RMS team,</td>
<td>15/10/15</td>
<td>Advanced Computer Aided Design Methodology for RF @ AMS (Analogue Mixed-signal) Circuits and Systems</td>
</tr>
<tr>
<td>Negin Javaheri</td>
<td>Laboratoire TIMA - Equipe AMfoRS,</td>
<td>16/10/15</td>
<td>Synthèse automatique de circuits numériques à partir de spécifications temporelles</td>
</tr>
<tr>
<td>Dr. Rongxiang Wu</td>
<td>School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu</td>
<td>17/11/15</td>
<td>More than Moore: Integrated Inductors for Monolithic Power Management</td>
</tr>
<tr>
<td>Dr. Rongxiang Wu</td>
<td>School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu</td>
<td>23/11/15</td>
<td>More than Moore: Micro-Transformers for Integrated Galvanic Isolation</td>
</tr>
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</table>
Seminars and invited talks given by TIMA members

Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions:

<table>
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<tr>
<th>INSTITUTION</th>
<th>LOCATION</th>
<th>DATE</th>
<th>SPEAKER</th>
<th>TITLE OR CONTENT</th>
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<tr>
<td>Ecole d’hiver Francophone sur les Technologies de Conception des Systèmes embarqués Hétérogènes (FETCH’2015)</td>
<td>Louvain-la-Neuve, Belgique</td>
<td>7-9/01/2015</td>
<td>Laurence Pierre</td>
<td>Runtime verification of embedded systems requirements throughout the design flow</td>
</tr>
<tr>
<td>Engineering science doctoral day</td>
<td>Casablanca, Morocco</td>
<td>18/04/2015</td>
<td>Emmanuel Simeu</td>
<td>Invited Tutorial on Energy Efficiency and Control</td>
</tr>
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<td>Universita di Brescia</td>
<td>Brescia – Italy</td>
<td>00/04/2015</td>
<td>S. Basrour</td>
<td>Microsystems research activities at TIMA Laboratory</td>
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<tr>
<td>Brown Univ.</td>
<td>Providence, USA</td>
<td>30/11/2015</td>
<td>L. Rufer</td>
<td>Resonant MEMS for Applications in Acoustics and Power Harvesting</td>
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<tr>
<td>The 27th International Conference on Microelectronics</td>
<td>Casablanca, Morocco</td>
<td>20/12/2015</td>
<td>Emmanuel Simeu</td>
<td>Invited Tutorial on Indirect Test and Control of Analogue/RF Circuits</td>
</tr>
</tbody>
</table>
Publications

International journals

AMfoRS


Dependable Multicore Architectures at Nanoscale: The View From Europe
*University of Rome, **University of Athens, ***Politecnico di Milano, ****University of Cyprus, *****Karlsruhe Institute of Technology, ******Université Antonio de Nebrija, *******University of Tuebingen, ********Semcon, *********Ridgetop Europe, **********Erasmus Medical Center, ***********Delft University of Technology, Computer Engineering, The Netherlands

2 Morin-Allory K., Javaheri N., Borrione D.
Efficient and Correct by Construction Assertion-Based Synthesis
Transactions on Very Large Scale Integration (VLSI) Systems, Volume: PP, pp. 1-12, 2015

CDSI


Calibration of high frequency MEMS microphones and pressure sensors in the range 10 kHz–1 MHz
*Laboratoire de Mecanique des Fluides et d'Acoustique, **Ecole Centrale de Lyon

4 Kachroudi A., Basrour S., Rufer L., Sylvestre A.*, Jomni F.**

Dielectric properties modelling of cellular structures with PDMS for micro-sensor applications
Smart Materials and Structures, Volume: 24, pp. 125013, 2015
*Laboratoire de Génie Electrique de Grenoble, **Laboratoire Matériaux, Organisation et Propriétés

5 Tounsi F., Mezghani B.*, Rufer L., Masmoudi M.*

Electroacoustic Analysis of a Controlled Damping Planar CMOS-MEMS Electrodynamic Microphone
*Groupe de Recherche en Microtechnologie et Système sur puce

6 Rolloff O., Possamai Bastos R., Fesquet L.

Exploiting reliable features of asynchronous circuits for designing low-voltage components in FD-SOI technology

7 Rufer L., De Pasquale G.*, Esteves J., Randazzo F., Basrour S., Somà A.*

Micro-acoustic Source for Hearing Applications Fabricated with 0.35 μm CMOS-MEMS Process
Procedia Engineering, Volume: 120, pp. 944-945, 2015
*Politecnico di Torino

RIS

8 Nicolaidis M.
Double-Sampling Design Paradigm - a Compendium of Architectures

9 Papavramidou P., Nicolaidis M.
Test Algorithms for ECC-based Memory Repair in Ultimate CMOS and Post-CMOS
10 Barragan M., Leger G.*
A Procedure for Alternate Test Feature Design and Selection
*IMSE, Instituto de Microelectronic de Sevilla

11 Beznia K.*, Bounceur A.*, Euler R.*, Mir S.
A tool for analog/RF BIST evaluation using statistical models of circuit parameters
*Université de Bretagne Occidentale

12 Laraba A., Stratigopoulos H., Mir S., Naudet H.*
Exploiting pipeline ADC properties for a reduced-code linearity test technique
*STMicroelectronics

13 Barragan M., Leger G.*, Vazquez D.*, Rueda A.*
On-chip sinusoidal signal generation with harmonic cancelation for analog and mixed-signal BIST applications
*IMSE, Instituto de Microelectronic de Sevilla

14 Dimakos A., Stratigopoulos H., Siligaris A.*, Mir S., De Foucauld E.*
Parametric Built-In Test for 65nm RF LNA Using Non-Intrusive Variation-Aware Sensors
*CEA-LETI, Laboratoire d'Electronic de Technologie de l'Information

Dynamic many-process applications on many-tile embedded systems and HPC clusters: The EURETILE programming environment and execution platform
*Istituto Nazionale di Fisica Nucleare, **RWTH Aachen University, ***École polytechnique fédérale de Zurich

16 Ferro L., Pierre L., Chabot M., Bel Hadj Amor Z.
ISIS version 2.1.1
Logiciel N° IDDN.FR.001.500008.001.S.P.2010.000.00000, delivered on Mar 01, 2015

17 Pierre L., Mazet K., Ziane-Cherif A.
OSIRIS version 1
Logiciel N° IDDN.FR.001.120039.000.S.C.2015.000.00000, delivered on Mar 01, 2015

18 Thalayssat J.*, Cleyet-Merle S.*, Schwambach V.
Procédé et dispositif de génération d’une représentation multi-résolutions d’une image et application à la détection d’objet utilisant une fenêtre de détection
Brevet N° 1553461, delivered on Apr 17, 2015
*STMicroelectronics
Invited conference talks

AMfoRS

19 Anghel L.  
Reliability Measurements with In Situ Aging Monitors in FDSOI Technology  
International Test Conference (ITC’15), 2015

CDSI

20 Al Khatib C., Gana M., Aktouf C.*, Fesquet L.  
A new methodology for implementing a distributed clock management system for low-power design  
Workshop on High Performance Embedded Systems (HiPEAC’15), 2015  
*Defacto technologies

RIS

21 Velazco R.  
Efectos de radiaciones en circuitos integrados digitales: orígenes, técnicas de mitigación y test experimentales  
Reunión de trabajo en Procesamiento de la Información y Control (RPIC’15), 2015

22 Velazco R.  
Effects of radiation in digital integrated circuits: origins, mitigation technics and experimental tests  
IEEE WESCIS (Education Society and Computer Intelligence Society), 2015

23 Velazco R.  
Error rate prediction for programmable circuits: methodology, tools and studied cases  
Workshop on the Effects of Ionizing Radiation on Electronic and Photonic Components for Aerospacial applications (WERICE’15), 2015

24 Velazco R.  
Estudio de la robustez frente a SEUs de algoritmos auto-convergentes  
Conferencias de Investigación para Posgrado, Facultad de Informatics, Universidad Complutense, 2015

25 Velazco R.  
Robustness of intelligent control with respect to radiation induced faults. Estudio de la robustez del "control inteligente" frente a fallos inducidos por las radiaciones, Seminaire in the frame of "Post-graduate Research Conferences"  
Conferencias de Investigación para Posgrado, Facultad de Informatics, Universidad Complutense de Madrid , 2015

International conferences

AMfoRS

26 Papadimitriou A.*, Hély D.*, Beroulle V.*, Maistri P., Leveauge R.  
Analysis of laser-induced errors: RTL fault model versus layout locality characteristics  
Third Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE'15), 2015  
*LCIS, Laboratoire de Conception et d'Intégration des Systèmes

27 Rehman Saif-Ur, Benabdenbi M., Anghel L.  
Application-independent testing of multilevel interconnect in mesh-based FPGAs  
IEEE 10th International Conference on Design and Technologies for Integrated System in Nanoscale (DTIS’15), pp. 1-6, 2015

28 Chabot M., Mazet K., Pierre L.  
Automatic and Configurable Instrumentation of C Programs with Temporal Assertion Checkers  
Digital circuits reliability with in-situ monitors in 28nm fully depleted SOI
Design, Automation & Test in Europe Conference & Exhibition (DATE’15), pp. 441-446, 2015
*STMicroelectronics

30. Kebaili N., Morin-Allory K., Brignone J.C.*, Borrione D.
Enabled-Based Synchronizer Model for Clock Domain Crossing static Verification
Forum on specification & Design Languages (FDL’15), 2015
*-

Impact of Gate Oxide Breakdown in Logic Gates from 28nm FDSOI CMOS technology
*STMicroelectronics, **Tohoku University, Japan

Polynomial multipliers for Fully Homomorphic Encryption on FPGA
International Conference on ReConFigurable Computing and FPGAs (ReConFig’15), 2015
*IF, Institut Fourier

33. Javaheri N., Morin-Allory K., Borrione D.
Revisiting Regular Expressions in Synthorus2: from PSL SEREs to Hardware
Forum on specification & Design Languages (FDL’15), 2015

34. Pierre L.
Towards a Toolchain for Assertion-Driven Test Sequence Generation
Forum on specification & Design Languages (FDL’2015), 2015

35. Pontié S., Maistri P., Leveugle R.
Tuning of randomized windows against simple power analysis for scalar multiplication on elliptic curves
Third Workshop on Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE’15), 2015

Validation of RTL laser fault injection model with respect to layout information
IEEE International Symposium on Hardware Oriented Security and Trust (HOST’15), pp. 78-81, 2015
*LCIS, Laboratoire de Conception et d'Intégration des Systèmes

CDSI

1. Design of thin-film AlN actuators for 4-inch transparent plates for haptic applications
16th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE’15), pp. 1-4, 2015
*CEA-LETI, Laboratoire d'Electronique de Technologie de l'Information, **STMicroelectronics, ***--

A Generic Clock Controller for Low Power Systems: Experimentation on an AXI Bus
IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC’15), 2015
*CIME, INPG, Grenoble, ***Defacto technologies, ***CEA

39. Arslan C., Poujaud J., Fesquet L.
A method to automatically determine the Level-Crossing thresholds in non-uniform sampling and Processing
1st IEEE International Conference on Event-Based Control, Communication and Signal Processing (EBCCSSP’15), 2015

40. Cherkaoui A., Fesquet L., Fischer V.*, Aubert A.*
A Self-timed Ring based True Random Number Generator with Monitoring and Entropy Assessment
University Booth at DATE 2015, pp. session UB02.1, 2015
*LHC, Laboratoire Hubert Curien

Characterization of a smartphone size haptic rendering system based on thin-film ALN transduction on glass
26th Micromechanics and Microsystems Europe workshop (MME’15), pp. 1-4, 2015
*CEA-LETI, Laboratoire d'Electronique de Technologie de l'Information, **STMicroelectronics
42 Bonnau O.*, Fesquet L.
Communicating and Smart Objects: multidisciplinary topics for the innovative education in microelectronics and its applications
14th International Conference on Information Technology Based Higher Education and Training (ITHET'15), pp. 1-5, 2015
*Institut d'Electronique et de Télécommunications de Rennes, Université de Rennes 1 – Institut National des Sciences Appliquées (INSA Rennes) – SUPELEC, France

43 Simatic J., Fesquet L., Bidegaray-Fesquet B.*
Correctly Sizing FIR Filter Architecture in the Framework of Non-uniform Sampling
11th International Conference on Sampling Theory and Applications (SampTA’15), pp. 269-273, 2015
*Laboratoire Jean Kuntzmann

44 Beyrouthy T., Fesquet L., Rolland B.*
Data Sampling and Processing: Uniform vs. Non-Uniform Schemes
1st IEEE International Conference on Event-Based Control, Communication and Signal Processing (EBCCSSP’15), 2015
*CIME, INPG, Grenoble

45 Trioux E., Rufer L., Monfray S.*, Skotnicki T.*, Muralt P.**, Basrour S.
Electrical characterization of a buckling thermal Energy harvester
The 15th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS’15), 2015
*STMicroelectronics, **EPFL

Evaluation of Bulk Built-In Current Sensors Detecting Multiple Transient Faults
IEEE Asian Test Symposium (ATS’15), 2015
*Ecole Nationale Supérieure des Mines de Saint-Etienne, **LIRMM, Laboratoire d’Informatique de Robotique et de Microélectronique de Montpellier

Experimental validation of diaphragms for acoustic micro-transducers
Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP’15), pp. 1–4., 2015
*

48 Rolloff O., Possamai Bastos R., Fesquet L.
Exploiting reliable features of asynchronous circuits for designing low-voltage components in FD-SOI technology
26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF’15), 2015

49 Melo J.G.M.*, Torres F.S.*, Possamai Bastos R.
Exploration of Noise Robustness and Sensitivity of Bulk Current Sensors for Soft Error Detection
International Workshop on CMOS Variability (VAR’15), 2015
*Fed. Univ. of Minas Gerais, Dept. of Electron. Eng., Belo Horizonte, Brazil

50 Trioux E., Monfray S.*, Skotnicki T.*, Muralt P.**, Basrour S.
Fabrication of bilayer plate for a micro thermal energy harvester
IEEE SENSORS’14, pp. 2171 - 2174, 2015
*STMicroelectronics, **EPFL

Guidelines on 3D VLSI design regarding the intermediate BEOL process influence
IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2015
*

High frequency calibration of MEMS microphones using spherical N-waves
RECENT DEVELOPMENTS IN NONLINEAR ACOUSTICS: 20th International Symposium on Nonlinear Acoustics including the 2nd International Sonic Boom Forum, pp. 1685, 2015
*Laboratoire de Mecanique des Fluides et d’Acoustique

53 Rufer L., De Pasquale G.*, Esteves J., Randazzo F.*, Basrour S., Somà A.*
Micro-acoustic source for hearing applications fabricated with 0.35μm CMOS-MEMS process
Eurosensors 2015, pp. 944-947, 2015
*Politecnico di Torino
54 Kachroudi A., Basrour S., Rufer L., Jomni F.*
Piezoelectric cellular microstructure PDMS material for micro-sensors and energy harvesting
The 15th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS’15), 2015
*Laboratoire Matériaux, Organisation et Propriétés

55 Darwish A., Fesquet L., Sicard G.*
RTL Simulation of an Asynchronous Reading Architecture for an Event-driven Image Sensor
1st IEEE International Conference on Event-Based Control, Communication and Signal Processing (EBCCSP’15), 2015
*CEA

56 Fesquet L., Darwish A., Sicard G.*
Sampling circuits for 1D and 2D sensors for low-power purpose
11th International Conference on Sampling Theory and Applications (SampTA’15), pp. 430-434, 2015
*CEA-LETI, Laboratoire d’Electronique de Technologie de l’Information

57 Bonnaud O.*, Fesquet L.
Towards multidisciplinarity for microelectronics education: a strategy of the French national network
*Institut d’Electronique et de Télécommunications de Rennes, Université de Rennes 1 – Institut National des Sciences Appliquées (INSA Rennes) – SUPELEC, France

RIS

58 Souari A.*, Thibeault Cl.*, Blaquière Y.**, Velazco R.
An Automated Fault Injection for Evaluation of LUTs Robustness in SRAM-Based FPGAs
IEEE East-West Design & Test Symposium (EWDTS’15), 2015
*ETS, Ecole de Technologie Supérieure, Département de génie électrique, **UQAM, Université du Québec à Montréal

Evaluating SEU fault-injection on parallel applications implemented on multicore processors
*~

60 Papavramidou P., Nicolaidis M.
Low-power memory repair for high defect densities

61 Nicolaidis M., Papavramidou P.
Memory repair for high defect densities
33rd IEEE VLSI Test Symposium (VTS’15), pp. 1-4, 2015

62 Charif A., Zergainoh N.-E., Nicolaidis M.
MUGEN: A High-Performance Fault-Tolerant Routing Algorithm for Unreliable Networks-on- Chip

Neutron-Induced Single Events in a COTS Soft-Error Free SRAM at Low Bias Voltage
*Universidad Complutense de Madrid, Spain, **Laboratoire de Physique Subatomique et de Cosmologie, ***ONERA/DES

64 Souari A.*, Thibeault Cl.*, Blaquière Y.**, Velazco R.
Optimization of SEU emulation on SRAM FPGAs based on sensitiveness analysis
*ETS, Ecole de Technologie Supérieure, Département de génie électrique, **UQAM, Université du Québec à Montréal

Sensitivity to Neutron Radiation of a 45 nm SOI Multi-Core Processor
Radiation and Its Effects on Components and Systems (RADECS’15), 2015
*ONERA/DES, **Laboratoire de Physique Subatomique et de Cosmologie, ***Universidad Complutense de Madrid, Spain
Statistical Anomalies of Bitflips in SRAMs to Discriminate MCUs from SEUs
*Universidad Complutense de Madrid, Spain, **Laboratoire de Physique Subatomique et de Cosmologie, ***ONERA/DESP, ****Cypress Semiconductor

RMS

67 Renaud G., Barragan M., Mir S.
Design of an on-chip stepwise ramp generator for ADC static BIST applications
IEEE International Mixed-Signal Testing Workshop (IMS3TW'15), pp. 1-6, 2015

68 Malloug H., Barragan M., Mir S.
Evaluation of harmonic cancellation techniques for sinusoidal signal generation in mixed-signal BIST
IEEE International Mixed-Signal Testing Workshop (IMS3TW'15), 2015

69 Stratigopoulos H., Barragan M., Mir S., Le Gall H.*, Bhargava N.*, Bal A.*
Evaluation of low-cost mixed-signal test techniques for circuits with long simulation times
IEEE International Test Conference (ITC’15), 2015
*STMicroelectronics

70 Liaperdos J.*, Stratigopoulos H., Abdallah L., Tsiatouhas Y.*, Arapoyanni A.**, Li X.*
Fast Deployment of Alternate Analog Test Using Bayesian Model Fusion
Design, Automation and Test in Europe Conference (DATE'15), 2015
*CEID, Department of Computer Engineering and Informatics, **DIT, Department of Informatics & Telecommunications

71 Barragan M., Leger G.*
Feature selection for alternate test using wrappers: application to a LNA case study
Design Automation and Test in Europe Conference (DATE'15), 2015
*IMSE, Instituto de Microelectronica de Sevilla

72 Le Gall H.*, Alhakim R., Valka M., Mir S., Stratigopoulos H., Simeu E.
High Frequency Jitter Estimator for SoCs
20th IEEE European Test Symposium (ETS'15), 2015
*STMicroelectronics

Horizontal-FPN fault coverage improvement in production test of CMOS imagers
33rd IEEE International VLSI Test Symposium (VTS'15), 2015
*STMicroelectronics

74 Pastorelli C.*, Mellot P.*, Mir S., Tubert C.*
Piece-wise-linear ramp ADC for CMOS imager sensor and calibration techniques
International Image Sensor Workshop (IISW’15), 2015
*STMicroelectronics

Special session: Hot topics: Statistical test methods
VLSI Test Symposium (VTS), 2015 IEEE 33rd, pp. 1-2, 2015
*IMSE, Instituto de Microelectronic de Sevilla, **LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier, ***Carnegie Mellon University, ****Mentor Graphics Corporation, *****Auburn University

76 Dimakos A., Andraud M., Abdallah L., Stratigopoulos H., Simeu E., Mir S.
Test and calibration of RF circuits using built-in non-intrusive sensors
IEEE International Computer Society Annual Symposium on VLSI (ISVLSI'15), 2015

SLS

77 Vincent L., Mancini S., Charles H.P.*, Lesecq S.*
Adaptive Data Prefetching for High Performance Processors
Workshop at the HIPEAC Conference High Performance Embedded Systems (HPES'15), 2015
*CEA-LETI, Laboratoire d'Electronique de Technologie de l'Information
78 Bourge A., Muller O., Rousseau F.
A Novel Method for Enabling FPGA Context-Switch
ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pp. 261, 2015

79 Bourge A., Muller O., Rousseau F.
Automatic High-Level Hardware Checkpoint Selection for Reconfigurable Systems
Field-Programmable Custom Computing Machines (FCCM’15), 2015

80 Cunha M., Fournel N., Pétrot F.
Collecting traces in dynamic binary translation based virtual prototyping platforms
Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO’15), pp. 1-6, 2015

81 Payet M., Fresse V.*, Rousseau F.
Dynamic Data Flow Analysis for NoC Based Application Synthesis
IEEE International Symposium on Rapid System Prototyping (RSP’15), pp. 61-67, 2015
*LHC, Laboratoire Hubert Curien

82 Schwambach V., Cleyet-Merle S.*, Issard A.*, Mancini S.
Estimating the Potential Speedup of Computer Vision Applications on Embedded Multiprocessors
*STMicroelectronics

83 Schwambach V., Cleyet-Merle S.*, Issard A.*, Mancini S.
Estimation rapide et précise de l’accélération d’applications séquentielles sur des multiprocesseurs embarqués
Conférence en Parallélisme, Architecture et Système (ComPAS’2015), 2015
*STMicroelectronics

84 Faravelon A., Fournel N., Pétrot F.
Fast and accurate branch predictor simulation

85 Schwambach V., Cleyet-Merle S.*, Issard A.*, Mancini S.
Fast Parallel Application and Multiprocessor Design Space Exploration from Sequential Code
International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2015
*STMicroelectronics

86 Schwambach V., Cleyet-Merle S.*, Issard A.*, Mancini S.
Image Tiling for Embedded Applications with Non-Linear Constraints
Design & Architectures for Signal & Image Processing (DASIP 2015), 2015
*STMicroelectronics

87 El-Antably A., Fournel N., Rousseau F.
Integrating Task Migration Capability in Software Tool-Chain for Data-Flow Applications Mapped on Multi-tiled Architectures

88 Goulahsen A.*, Saade J., Pétrot F.
Line coding methods for high speed serial links
*STMicroelectronics

89 Saade J., Goulahsen A.*, Picco A.*, Huloux J.*, Pétrot F.
Low overhead, DC-Balanced and run length limited Line Coding
IEEE 19th Workshop on Signal and Power Integrity (SPI’15), pp. 1-4, 2015
*STMicroelectronics

90 Fresse V.*, Combes C.*, Payet M., Rousseau F.
Methodological Framework for NoC Resources Dimensioning on FPGAs
International Workshop on Design and Performance of Networks on Chip (DPNoC’15), 2015
*LHC, Laboratoire Hubert Curien

91 Schwambach V., Cleyet-Merle S.*, Issard A.*, Mancini S.
Parana: Fast Parallel Application and Multiprocessor Design Space Exploration from Sequential Code
Design Automation Conference (DAC) Work-in-Progress Session, 2015
*STMicroelectronics
92 El-Antably A., Gruber O.*, Fournel N., Rousseau F.
Transparent and Portable Agent Based Task Migration for Data-Flow Applications on Multi-tiled Architectures
*LIG (CNRS-INPG-UJF), Grenoble, France

Book chapters

AMfoRS

Laser-induced fault effects in security-dedicated circuits
VLSI-SoC: Internet of Things Foundations, IFIP Advances in Information and Communication Technology, pp. 220-240, 2015
*LCIS, Laboratoire de Conception et d'Intégration des Systèmes, **STMicroelectronics, ***LIRMM, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier, ****ONERA/CERT, Toulouse, France

CDSI

94 Fesquet L., Bidegaray-Fesquet B.*
Digital Filtering with non-uniformly sampled data: from the algorithm to the implementation
*Laboratoire Jean Kuntzmann

RMS

95 Stratigopoulos H., Kaminska B.*
Analog and Mixed-Signal Test
*Simon Fraser University, Canada

Design of an energy efficient ZigBee transceiver
Mixed-Signal Circuits, 2015
**IMSE, Instituto de Microelectronica de Sevilla

97 Bentobache M.*, Bounceur A.*, Euler R.*, Mir S., Kieffer Y.*
Minimizing test frequencies for linear analog circuits: new models and efficient solution methods
in VLSI-SoC: At the Crossroads of Emerging Trends, IFIP Advances in Information and Communication Technology, pp. 188-207, 2015
*Université de Bretagne Occidentale

98 Dubois M., Stratigopoulos H., Mir S., Barragan M.
Statistical evaluation of digital techniques for Sigma-Delta ADC BIST

Edited Books

RIS

99 Nicolaidis M.
Design for Reliability and Yield for Ultimate CMOS Technologies
IEEE Transactions on Device and Materials Reliability, IEEE, 2015
National journals

CDSI

100 Fesquet L., Morin-Allory K., Robin R.*
Un projet de microélectronique numérique original : Contrôle autonome d'un micro-drone par caméras externes
J3eA – Journal sur l'enseignement des sciences et technologies de l’information et des systèmes,
Volume: 14, pp. 9, 2015
*CIME, INPG, Grenoble

SLS

101 Sarrazin G., Fournel N., Gerin P., Pétrot F.
Simulation native basée sur le support matériel à la virtualisation cas des systèmes many-cœurs spécifiques

National conferences

CDSI

102 Rufer L.
Approche "fabless" de fabrication des micro-transducteurs électroacoustiques
CFA/VISHNO 2016, pp. 826-831, 2015

103 Kachroudi A., Basrour S., Jomni F.*
A Predictive model for the effective dielectric permittivity of micro-structured polymer as ferroelectret material for micro-sensors applications
International Meeting on Advanced Materials (MAM'15), 2015
*Laboratoire Matériaux, Organisation et Propriétés

104 Rendon A., Basrour S.
Study of a piezoelectric microgenerator thermo-magnetically triggered
5èmes Journées Nationales sur la Récupération et le Stockage d’Energie pour l’Alimentation des Microsystèmes Autonomes (JNRSE’15), 2015

SLS

105 Schwambach V., Cleyet-Merle S.*, Issard A.*, Mancini S.
Estimating the Potential Speedup of Computer Vision Applications on Embedded Multiprocessors
18ème Journées Nationales du Réseau Doctoral en Micro- nanoélectronique (JNRDM’15), 2015
*STMicroelectronics

106 Payet M., Fresse V.*, Rousseau F., Rémy P.*
Extraction du parallélisme à l'exécution pour la synthèse d'applications basées sur un NoC
Conférence en Parallélisme , Architecture et Système (ComPAS’15), 2015
*LHC, Laboratoire Hubert Curien

Other communications

AMfoRS

107 Pontié S.
Attaque par analyse de la puissance consommée contre un crypto-processeur basé sur les courbes Jacobi quantiques
Journées Codage et Cryptographie 2015, Toulon, FRANCE
108 Bel Hadj Amor Z., Borrione D., Javaheri N., Morin-Allory K., Pierre L.
Design Understanding - At What Abstraction Level is the Pain Most Intense?
Workshop on Design Automation for Understanding Hardware Designs (DUHDe Friday Workshop
DATE 2015), Grenoble, FRANCE

109 Pierre L.
Runtime Verification of Embedded Systems Requirements throughout the Design Flow
Ecole d'hiver Francophone sur les Technologies de Conception des Systèmes embarqués Hétérogènes
(FETCH'2015), Louvain-La-Neuve , BELGIUM

SLS

110 Pétrot F.
A Few Open Problems in Vertically-Partially-Connected 3D-NoC
15th International Forum on MPSoC for Software-defined Hardware, Ventura Beach Marriott, CA,
UNITED STATES

PhD theses

AMfoRS

112 Gang Yi
Design of a Network on chip (NoC) that tolerates multiple static and dynamic faults
These de Doctorat, Université de Grenoble, spécialité "Micro et Nano Electronique", Nov 05, 2015

113 Javaheri N.
Automatic synthesis of digital circuits from temporal specifications
These de Doctorat, Université de Grenoble, spécialité "Nanoélectronique et Nanotechnologies", Oct 01,
2015

114 Rehman Saif-Ur
Development of test and diagnosis techniques for hierarchical mesh-based FPGAs
These de Doctorat, Université de Grenoble, spécialité "Nanoélectronique et Nanotechnologies", Nov 06,
2015

115 Saliva M.
Dedicated circuits to aging mechanisms study in advanced CMOS technology nodes: Design and
measurements
These de Doctorat, Université de Grenoble, spécialité "Micro et Nano Electronique", Oct 02, 2015

CDSI

116 Le Pelleter T.
A digitalization method adapted to an event-driven logic for ultra-low power purpose: Application to
physiological signal pattern recognition
These de Doctorat, Université de Grenoble, spécialité "Micro et Nano Electronique", May 13, 2015

117 Trioux E.
Micro-générateurs piézoélectriques pour des applications de récupération d'énergie
These de Doctorat, Université de Grenoble, spécialité "Nanoélectronique et Nanotechnologies", Nov 25,
2015

RIS

118 Costenaro E.
Techniques for the evaluation and the improvement of emergent technologies' behaviour facing random
errors
These de Doctorat, Université de Grenoble, spécialité "Micro et Nano Electronique", Dec 09, 2015
RMS

119 Fei R.
Alternative solution to improve the production test of optical sensors in CMOS technology
These de Doctorat, Université de Grenoble, spécialité "Micro et Nano Électronique", Oct 13, 2015

120 Stratigopoulos H.
Test techniques for Analog Circuits and Systems
HDR, Université de Grenoble, spécialité "micro et nano électronique", Jul 17, 2015

SLS

121 Alcantara O.
Synthesis of NoC emulation platforms for embedded systems: toward the next-generation of NoCs
These de Doctorat, Université de Grenoble, spécialité "Sciences, Ingénierie, Santé", Sep 09, 2015

122 El-Antably A.
Study of task migration in a multi-tiled architecture - Automatic generation of an agent-based solution
These de Doctorat, Université de Grenoble, spécialité "Nanoélectronique et Nanotechnologies", Dec 16, 2015
Social life

TIMA picnic on July 2015