Chips are the heart of professional and commodity objects that need to be always smaller, faster and more versatile. At one end of the spectrum, micro and nano systems (MEMS/NEMS) provide sensors for multiple kinds of applications, among which the most prominent and socially significant ones include medicine (chirurgical devices, implants, analysis and surveillance of human health based on chemical, sound or visual sensors) or environment (measurement of air/water quality, observation of eco-systems). At the other end, the processing of large data is at the basis of consumer and professional electronic equipment: computers, cell phones, digital cameras, numerical TV, tablets, games, etc.

The rapid evolution of chip fabrication technology results in a correspondingly rapid obsolescence of designs, and in growing users expectations on the characteristics of the circuits. Active CMOS components are now measured in nano-meters, which raises unprecedented problems such as variability of process, voltage and temperature, or power leakage. Circuits are embedded in a wide variety of applications, some of which demand strict security, availability, safety, mobility and power consumption requirements. For all these reasons, hardware and hardware-dependent software architectures have to be reconsidered, together with their design and test methods, models and tools. More specifically, results in the following research topics have a strategic importance to the European microelectronics and embedded systems industry.

- **Multiprocessors on a chip (MPSOC):** current systems already hold several processor cores on a chip. Hundreds are announced by 2010, over a thousand by 2020 (source: ITRS 2009). How to organize processors and memories into subsystems, and ensure efficient (on chip and off chip) communications is an open problem, both logically and topologically (3D integration).

- **Heterogeneous architectures** include analog devices (sensors, actuators, antennas, energy scavenging), digital computations, AC/DC converters; synchronous cores and asynchronous communications; hardware components and several software layers. The number of possible combinations explodes with the increasing number of components on a chip. **Efficient design space exploration** methods and **performance evaluation** tools are needed. **Verification and test generation models** for such designs require memory and computing resources that grow exponentially with the size of the simulated architecture.

- **Design of innovative components:** while processor cores tend to be standardized to a few instruction sets and be provided as IP by industry, there is still room for academic research to invent, design, characterize and test advanced analog components for emerging applications, among which: **micro-sensors** for sound, ultrasound, pressure (**medical imaging and instruments**), smart vision and toxic chemicals (**industrial and severe environments**). Additional components are aimed at ensuring greater **energy autonomy** to the system, such as low frequency piezoelectric micro-generators.

- **Taking efficient advantage of the parallelism of the hardware architecture** will need the development of special purpose additional logic, and a hardware dependent software layer that should facilitate the development of the OS, taking into account the various types of cores and the existence of NoCs. Problems to be solved include the non uniform processing time of tasks by different cores, the non uniform access to memory, task migration, cache coherence, power management, fault management, etc

- **Robustness:** systems that include a large number of components on large area chips will have fabrication defects. With the miniaturization of devices, process variations will result in voltage and temperature variations inducing timing faults. Alternative design approaches (e.g. based on advanced asynchronous techniques) enable the design of robust circuits to process variability, voltage or temperature. Acceptable yields will require that circuits be tested both after manufacturing and during operation (self test), and that advantage be taken of the redundancy of MPSOC architectures to increase fault tolerance, possibly at the cost of performance. New methods are needed to perform **dynamic monitoring** and **reconfiguration** of the hardware, with implications on the **dynamic reallocation** of software tasks and data, and **adaptive routing** of the communications.

- **Safety, reliability:** the smaller size of devices has a negative impact on the consequences of natural radiations and circuit aging. Real life experiments in commercial airplanes have shown that a single particle may upset several bits in a memory, even in a single word, so that the current single event upset
(SEU) hypothesis is no longer realistic. The complexity of models and counter measures to face multiple bit upsets (MBU), grows exponentially with the number of simultaneous faults. Faults may also be the result of malicious attacks (to extract or substitute confidential information) that can take various forms: fault injection, power consumption analysis, application of electro-magnetic fields, or their combination. Providing counter-measure to the more complex ones is an open problem. New “attack resistant” architectures are needed; asynchronous architectures are very promising.

- **Ultra low power consumption: at all levels of design**, power efficiency has become a priority requirement. From the circuit level (low voltage transistors, energy scavenging devices) and the block level (libraries of low power component, power gating, reduced clock frequency, power interruption) to the synchronization primitives (asynchronous protocols) and activity monitoring and reporting, low power consumption must be planned early in the hardware design flow, so that the first level of software API may provide primitives to energy aware operating systems and algorithms.

TIMA is a public research laboratory sponsored by Centre National de la Recherche Scientifique (CNRS), Grenoble Institute of Technology (Grenoble INP) and Université Joseph Fourier (UJF), where all the above challenges are addressed. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end. The current Activity Report volume covers the activities of the laboratory for 2009 and 2010. During that period, TIMA was composed of six research groups: **Architectures for Robust and complex Integrated Systems** (ARIS), **Concurrent Integrated Systems** (CIS), **Micro and Nano Systems** (MNS), **Reliable Mixed-signal Systems** (RMS), **System Level Synthesis** (SLS), **Verification and modeling of Digital Systems** (VDS). These research groups are largely autonomous in managing their students and grants, but they also jointly cooperate in many large projects. By the end of the reporting period, some reorganization took place, and TIMA is now structured into four research themes. Yet, it was found more natural to report according to the structure that did the work. The next six chapters are the scientific activity report and achievements of the groups.

Chapters 7 to 10 are the list of the Laboratory members, trainees and visitors who were present during all or part of the reported period. The members, listed in alphabetical order in Chapter 7, are presented in more details in Chapters 8 to 10, according to their category (academics and permanent researchers, PhD students, staff).

A large part of the research is financed by research grants and contracts, most of which are large cooperative projects with industrial and academic partners, at the national, European or world level. Chapter 11 gives an overview of these contracts.

Members of TIMA have established scientific agreements with universities and research laboratories worldwide. They contribute yearly to many national and international events, as members of the Organizing and/or Program Committee. At the national level, they are coordinators of 3 of the 6 themes of the CNRS GDR SOC-SIP. At the international level, they created several yearly events (FDL, IOLT, LATW) and assume the responsibilities of PC Chair or General Chair in prominent conferences of the domain area. In 2009 and 2010, members of TIMA chaired or co-chaired LATW in Buzios and Corfu, SEE in San Diego, SAMPTA in Marseille, RSP in Paris, IOLT in Lisbon and Corfu, FDL in Nice, and DRV in Austin. The details of these involvements are given in Chapter 12. Other contributions to the scientific community include high-level courses and tutorials, given in addition to the normal teaching obligations of the academic members. These are the topic of Chapter 13.

This report ends with the results obtained by the researchers. Chapter 15 lists the publications, classified according to their category and thematic areas. Patents have been obtained on a variety of inventions: embedded sensors diagnosis, a 3D serial asynchronous link, an adaptive artificial urinary sphincter, a medical needle instrumentation, a micro-fluidic device etc. Innovative circuits have been fabricated, such as the first secured asynchronous FPGA against side channel attacks, or a new non-coherent Impulse radio UWB communication technique. Works on circuit hardening were selected among the most influential papers for the DATE 10th anniversary book. Finally, all the research results are quickly transferred to industry: recent achievements include the creation of a new spin-off company by a graduated PhD from the MNS group, the adoption by Thales Communication of the Rabbits hardware/software exploration environment, or the integration by Dolphin Integration of the HORUS verification technology based on assertions in their mixed-signal simulator.
Yannick Monnet was awarded the "Thesis Prize" in Micro and Nano Electronics by Grenoble INP in 2009, with special mention for its impact and industry transfer. And Hamid Lamraoui obtained the "Thesis Prize 2010" from the French Society for Biological and Medical Engineering.

Finally, we like to close this report with some illustrations of the special events and recognitions, and mention the social gatherings that cement TIMA as a human community.

Dominique Borrione

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1. Micro and Nano Systems (MNS)

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- J. Delamare,
- P. Cinquin,
- R. Tourki,
- A. Soudani,
- D. Favier,
- G. Chagnon,
- P. Mozer

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Topics:

In recent years, a very large amount of scientific work has been achieved around Micro-Electro-Mechanical Systems (MEMS). Some industrial success stories (accelerometers, gyroscopes and MOEMS) have shown their maturity. MEMS are now starting to take place around us in our everyday life as the microelectronic did 20 years ago. However, a lot of effort is still needed for the integration of ICs and MEMS. Nearly every kind of sensor or actuator has been successfully developed with MEMS technologies whereas a very little work has been done on integration of MEMS devices with complex integrated circuits. An important part of the MNS group research activity is centred on integrated MEMS with the vision of “Systems-On-Chip embedding MEMS” as target. We believe that the future of MEMS is beside millions of transistors in large mixed signal Systems-On-Chip. These integrated MEMS devices will act not only as sensors but also as actuators or electric devices like switches and filters.

Since 2003, the group is strongly involved in the miniaturization of nodes for wireless sensor networks. In this topic we address the problem of the energy, and its management which can increase drastically the autonomy of such tiny devices. Our approach is based on scavenging the environmental energy surrounding the node into electrical power which can supply it. We explore the design, fabrication and characterization of new microgenerators. We have investigated ultra low power approaches for the energy management circuits. Finally, we develop several hierarchical models associates with the different subsystems involved in a node. These models are implemented in different simulation languages and CAD tools used for the global simulation of a node.

1 CEA – Leti, 2 ST Microelectronics, 3 GE2Lab, 4 TIMC, 5 LEM, 6 3SR, 7 Groupe Hospitalier Pitié-Salpêtrière
In the last decade the MNS group has developed several demonstrators using well established microfabrication techniques available from several IC foundries. More recently, we carry on with the investigation concerning the integration of microresonators with advanced CMOS technologies based on SOI substrates. These topics are developed in collaboration with CEA-LETI and ST Microelectronics.

In 2007 we started a new topic of research concerning the Microsystems for health. In tight collaboration with TIMC-IMAG and 3SR laboratories in Grenoble, we are investigating innovative ways for the miniaturisation and integration of different functionalities of an implantable and autonomous urinary sphincter in a human body and for the integration of microsensors in surgical tools. A spin off has been created to commercialize the urinary artificial sphincter which has been developed during a PhD thesis.

1.1 Autonomous Microsystems

1.1.1 Introduction:

Over the recent years a growing interest in the field of miniature sensor nodes has be seen. A wide range of applications is already planned for their integration; from embedded sensors in buildings to medical implants. Despite the considerable effort of research in this domain, one area was left with little attention – the energy source powering the device. Until now, the majority of such systems was running on an electrochemical battery. This approach has a primary drawback – the device lifetime is directly linked to the battery size. Considering millimetre size devices, it is hard to extend lifetime beyond one year. A solution to this problem is to take advantage from the very low power consumption of current electronics; indeed such a device can be powered by harvesting energy of the surroundings. Recent projects like SMARTDUST, WINS or SAND have used photovoltaic and thermoelectric principles, and thus have shown that scavenging energy from the environment is possible.

Mechanical energy is a promising solution since several natural mechanical sources exist: vibration, deformation, variation of constraint. The main advantage of this solution is the abundance of mechanical energy in the environment and their relatively high power. Another important point is that the device needs only to be coupled mechanically through its package with the environment, the microsystem itself is then isolated. One of the drawbacks is that classical sources of mechanical energy operate at frequencies below 200 Hz when natural frequencies of MEMS structures are very high.

Since 2003, we have explored the design, fabrication and characterization of new microgenerators which convert the mechanical energy into electricity. At first, this research topic has been developed in the frame of the European research project called VIBES. VIBES stands for Vibration Energy Scavenging and is a Specific Targeted Research Project (STREP) of the 6th Framework Program of the European Union (EU). The project was led by University of Southampton; the rest of consortium is composed of public research laboratories (TIMA, Tyndall, University of Southampton, FEMTO-ST and EPFL) and companies (MEMSCAP, 01db METRAVIB and PHILIPS).

During this project, we have fabricated MEMS piezoelectric microgenerators with very promising results and proposed innovative ultra-low-power electronic circuits for managing the power produced by these devices. Beyond the VIBES project, we are exploring new MEMS components at low frequencies in the framework of three projects. The first one is SESAM supported by the ANR-2009, and the second is µSEMPEE supported by the cluster MNS-2010 from the Rhône-Alpes Regional Council. HBS is the last and it is supported by the Fonds Unique Interministériel (FUI – 2010).

Moreover, new approaches were developed, still with a strong focus on energy scavenging. The first one was the investigation of new generators based on flexible sheets of electro-active polymers. This work was done in collaboration with the CEA-LETI. The second one opened a totally new road since it was based on temporal temperature variation. The project was created in collaboration with the Magnetic Actuators and MicroSystems team from G2Elab (Grenoble).

1.1.2 Seismic Piezoelectric Microgenerators

Members: S. Basrour, M. Defosseux, M. Allain

The goal of our work is to develop and demonstrate that a micro power generator is able to scavenge mechanical vibrations and motions from the surrounding (like building, machines, human body). This device will produce electrical power (in the range of µW) in order to supply an autonomous microsystem. The microsystem will embed an Ultra Low Power controller, a low power RF communication module, several MEMS sensors and an energy storage unit (micro battery or supercapacitor). Figure 1.1 shows a schematic of the architecture of the autonomous microsystem.
 Among the transduction principle based on piezoelectricity, electromagnetic induction or electrostatic effect, we decide to investigate more in details a piezoelectric transducer. The reason is that piezoelectricity allows high output power density and that some piezoelectric materials can be deposited by techniques that are compatible with CMOS microfabrication techniques.

Piezoelectricity is the property of some materials to generate electrical charges on their surfaces when they are subject to a mechanical stress, as shown in Figure 1.2. These materials are widely used either for actuation (where mechanical stress is induced by applied voltage – indirect effect) or for sensing (electrical charge appears when mechanical stress is applied – direct effect). The best bulk piezoelectric materials available are able to transfer mechanical energy to electrical energy with 80% efficiency.

During the VIBES project (2004-2007), we have designed, modelled and fabricated several piezoelectric micro power generators. The device, as shown in Figure 1.3a is composed of a seismic mass made of Silicon 500µm thick connected to the substrate by a thin cantilever beam. When excited at its resonance frequency, the system moves according to its fundamental vibration mode. During the movement, a piezoelectric layer deposited on the cantilever is compressed and elongated. In consequence, thanks to the piezoelectric effect, electrical charges appear on the surface and are collected by the metallic electrodes. The generated alternative electrical signal is sent to an electrical load or to an Energy Harvesting Circuit that we describe in the next section.

The device was fabricated using MEMS microfabrication techniques that include piezoelectric thin layer deposition. This work was performed in cooperation with MEMSCAP, FEMTO-ST and EPFL. Basically, the process is composed of Deep Reactive Ion Etching (DRIE) steps on both sides of a Silicon On Insulator (SOI) wafer. We have used two materials for the piezoelectric layer. The first one is Aluminium Nitride (AlN), a material relatively easy to deposit by sputtering and environmentally friendly, but having low electromechanical coupling coefficient. The other is PZT (Lead Zirconate Titanate), much more difficult to create as a thin layer (Sol-gel technique), but with remarkable piezoelectric properties. Despite its lower piezoelectric coefficient AlN has a better mechanical factor and a permittivity 100 times lower than PZT. Therefore by taking into account piezoelectric coefficients and permittivity ratios, for a given stimulus, AlN exhibits an output voltage ten times higher than PZT for a power harvested in the same order of magnitude. This has a huge impact on the collected energy as voltage is the preferred mode of energy collection (using diode rectifier). Figure 1.3b shows an SEM photo of a PZT microgenerator.
We have fabricated and tested several such devices. A standard electrode layout covering the entire surface of the beam was used, presented in Figure 1.3, as well as some innovative solutions aiming at raising the output voltage and coupling coefficient. They consist either of implementing several piezoelectric capacities on one device, which is supposed to raise the output voltage, or integrating of interdigitated electrodes that permit to use the more energetically effective $K_{33}$ mode of operation of the piezoelectric layer.

In the first place we have evaluated the output power dissipated on a matched resistive load. The device was excited using a controlled vibration source – a shaker, controlled by a function generator and a custom LabVIEW application (see Figure 1.4). The results for PZT devices are presented in the Figure 1.5. Powers ranging from 0.9µW to 1.4µW per device can be obtained with one device excited at the anti-resonance with 2g excitation amplitude at 875 Hz. An important gain in power output can be obtained with the use of IDT devices. The output voltages at high excitation levels are sufficient for rectification and further use in an energy scavenging circuit.

Figure 1.4 Test bench setup used for the electromechanical characterization of the devices and a close-up view of the tested device mounted on a shaker
In case of absence of sufficient vibration source, several devices can be used together in order to provide power needed. We have estimated that power less than 400nW is required to power a simple wireless sensor node with a duty cycle of operation of about 1%. Therefore, our generators with conjunction with an energy scavenging circuit and an energy storage unit (a supercapacitor) can be used as a power source and replace the commonly used batteries. The figure of merit (FOM) of our devices was among the best published for this kind of structures and frequencies.

Since 2009, we are involved in the SESAM project (Smart multi-source Energy Scavenger for Autonomous Microsystems). This project is leaded by ESIEE-Paris; the rest of consortium is composed of laboratories TIMA, LIP6, and CEA-Leti laboratories. In this project we focused our attention on low frequency vibrating structures working at frequencies close to 200 Hz and working efficiently at very low levels of acceleration. The goal of this project is to prove that is is possible to harvest energy efficiently at lower frequencies. The devices are fabricated locally using the same flow chart used previously with AlN thin films. According to the performances and the CMOS compatible process (PZT sol-gel deposition process is not CMOS compatible), we choose to use 2µm thick AlN piezoelectric layer. We report in the Figure 1.6, a view of clamped-free and clamped-clamped structures.

![Figure 1.5](image1.png)

**Figure 1.5** Power output of one piezoelectric generator versus the excitation vibration amplitude, for a standard device (a) and for a device with interdigitated electrodes (b)

![Figure 1.6](image2.png)

**Figure 1.6** Piezoelectric microgenerators on a 4” substrate (a), and a SEM picture of a clamped-free device (b)
This device allows us to harvest 0.62µW at 214 Hz for 0.17g RMS for a volume of less than 3mm$^3$ (Figure 1.7). Under vacuum, at a given input acceleration the power harvested is more than doubled. Compared to literature, this device presents, under vacuum, the best figure of merit.

![Figure 1.7](image)

**Figure 1.7** Power generated versus acceleration applied to the device (a), and electrical behaviour of the device versus the resistive load (b)

These MEMS devices exhibit very high mechanical quality factors (typically $Q_m > 300$) and in this way their bandwidth is very narrow. The main problem for harvesting efficiently the mechanical vibrations concerns the adaptability of the microgenerators resonance frequencies to the source main frequency. We have proposed an innovative approach to achieve a completely passive, wide band adaptive system by employing mechanical nonlinearities. We have developed analytical analysis of the underlying idea and in the Figures 1.8 a) and b) we can see the emergence of the nonlinear behaviour of the MEMS resonator when the device is excited at high acceleration levels. This behaviour is exerted for high quality factors.

![Figure 1.8](image)

**Figure 1.8** Numerical simulation of system response in the frequency domain for different input acceleration amplitudes (a), Numerical simulation of frequency response of the system with different quality factors $Q$ for an input acceleration amplitude of 2g (b)
In Figure 1.9 we report experimentally verified frequency adaptability of over 36% for a clamped-clamped beam device at 2g input acceleration. We believe that the proposed solution is perfectly suited for autonomous industrial machinery surveillance systems, where high amplitude vibrations that are necessary for enabling this solution, are abundant.

![Figure 1.9 Nonlinear frequency response of the CC structure for 3 acceleration amplitudes, for both positive and negative frequency sweeps with visible amplitude "jumps" (a), Peak voltage and power generated on a matched resistive load of 290kΩ for positive and negative frequency sweeps versus the excitation amplitude for the CC beam (b)](image)

In 2010, we started two new projects. In the framework of µSEEMPE project (µ-Sources Energie Electrique Matériaux Piezo Emergents) we are working on the integration of new piezoelectric materials deposited by thin film techniques on top of silicon substrates. The target of this work is to provide different technologies for the fabrication of seismic piezoelectric generators. The HBS project (Heart Beat Scavengers) concerns the design, fabrication and characterization of tiny generators exhibiting ultra low resonant frequencies.

### 1.1.3 Energy Harvesting Circuit

The goal of the power management module is to transfer the energy produced by the micro power generator to the energy storage module, i.e., the micro battery. In order to charge the battery, a stable DC voltage is needed with a specific voltage that depends on the battery characteristics. On the other hand, the signal coming from the microgenerator is generally alternative (AC) and the voltage can be very low (few mV). By consequence, some operations such voltage rectification and elevation are required. In addition, these operations must be made with the best efficiency and the circuit must have very low power consumption.

Figure 1.10 shows the standard architecture of the power management module. The Energy Harvesting Circuit (EHC) is composed of an AC/DC circuit for the rectification, and of a DC/DC circuit for the elevation of the voltage. The DC/DC circuit is managed by a digital controller which maximises the energy transfer from the power generator to the micro battery.

![Figure 1.10 Architecture of the Energy Harvesting Circuit](image)
In the framework of the VIBES project, we have proposed several original approaches to overcome the problem of low voltages and power provided by the microgenerator. At first, we have designed a passive circuit based on a voltage multiplier (VM), which plays the role of AC/DC and DC/DC converters. It accepts tenth of mV as input. This multiplier uses diodes with very low threshold voltage. The second approach deals with the design of an ultra low power (ULP) AC/DC converter (tenth of nanowatt) able to rectify signals down to few mV.

**Voltage Multiplier (VM)**

A voltage multiplier with 6 stages is implemented with STMicroelectronics CMOS 0.12 (HCMOS9). The system composed of the ASIC voltage multiplier and the MEMS generator connected on the chip level was tested (Figure 1.11). It is up to now the smallest MEMS microgenerator with its power management module.

![Figure 1.11 A System in a Package composed by a MEMS microgenerator and a voltage multiplier](image)

**Figure 1.12** presents the open circuit output voltage of the system for different input acceleration amplitudes at resonance of 1511 Hz. These experimental results show that a 1V output voltage can be obtained for very low excitation amplitude of about 50 mg applied on the generator.

![Figure 1.12](image)

**Figure 1.12** presents the process of charging of a 1 µF capacitor connected to the output of our system for different input acceleration levels. The harvested energy on this kind of load reaches 5.3 µJ after 250 seconds. It is clear that we can store more energy if we connect in series these circuits or if we wait more time. The efficiency of this kind of circuit is poor around 20% and depends strongly on the characteristics of the excitation signal (amplitude and frequency) and the number of stages implemented. We have shown that this circuit can be used successfully with a piezoelectric microgenerator and can be adapted easily to the electromagnetic one designed by or partners in the VIBES project.
The ULP AC/DC
The AC/DC converter based on ULP comparators is implemented using the technology Austria Microsystems CMOS 0.35. The layout of this circuit is reported in Figure 1.13.

![Layout of the ULP AC/DC converter (Austria Microsystems CMOS 0.35)](image)

**Figure 1.13** Layout of the ULP AC/DC converter (Austria Microsystems CMOS 0.35)

The electrical characterizations of this circuit have shown that it can rectify input signals with very small amplitude. Moreover this circuit can be polarized down to 2V and in this case its consumption is close to 1nW.

Autonomous power management system
The total efficiency of this ULP AC/DC circuit can reach 95% but it needs a voltage source. To overcome this problem we have proposed to supply the AC/DC with the voltage multiplier as shown in Figure 1.14.

![Schematic of an ULP AC/DC supplied with a voltage multiplier](image)

**Figure 1.14** Schematic of an ULP AC/DC supplied with a voltage multiplier

As a proof of concept we have performed the above-mentioned circuit with $C_{\text{aim}}$ equals 1µF and $C_{\text{recolte}}$ equals to 80nF. The transient response of this system is reported on Figure 1.15 when the input signal, 140 mV peak, is provide by our piezoelectric microgenerator resonating at 1500 Hz.
Thanks to this configuration, we succeeded in harvesting the ultra low power signal given by the microgenerator in an efficient way without the need of an external power supply. In a future work, we propose to cascade several modules in order to obtain the desired voltage for the miniature sensor node.

1.1.4 Global simulation and co-simulation of Energy Harvesting Circuits

Members: H. Boussetta, S. Basrour, A. Soudani, R. Tourki

The study case is an integrated power harvesting circuit used for supplying power to nodes in wireless sensor networks. The system is composed of a MEMS structure (in our case a microgenerator) and an electrical circuit which boosts and rectifies the low amplitudes AC signals delivered by such generators. This electrical circuit is based on a voltage multiplier composed with ultra low threshold voltage diodes. The classical validation of such systems by separate simulation of each element: FEM analysis for mechanical part and traditional circuit-simulators for electrical part does not offer the possibility to predict the behaviour of the complete system. To overcome such limitations, we propose to use a simulation environment based on VHDL-AMS and SPICE languages.

Concerning the modelling of the microgenerator, we start from one dimensional system where only the general behaviour of such transducer is presented. The model was kept intentionally simple to focus on the functionality of the piezoelectric transduction. Then, an enhanced model of the piezoelectric generator developed on our research group is introduced in order to better predict the real behaviour of such system. The design of the enhanced structure is based on the microfabrication techniques of the SOI substrate. Several important considerations are taken into account especially the important size of the mass compared to the one of the beam, the rigidity of the mass and its rotational inertia. It is also important to consider that the acceleration is applied to the mass and not to the end of the beam.

Described models are parameterized using generic interface lists in entity declarations. This way of coding makes our models good candidates for reuse just by changing constants that define physical and geometric parameters. Then, those numbers of degrees of freedom (geometric and physical) multiply analysis possibilities and so greatly cut down the simulation time compared to the FEM computation. Thus, the proposed enhanced model can be used to obtain several valuable results. First, we will study the impact of the piezoelectric properties of the material used on the model by keeping the same dimensions of both devices and just changing the piezoelectric material layer. The used piezoelectric materials can be either Aluminum Nitrite (AlN) or Lead Zirconium Titanate (PZT) thin layers. To study the microgenerator with AlN layer, we just have to substitute the generic parameters responsible of physical properties of the used material (PZT) in the entity declaration of the previous model by AlN ones. A sinusoidal acceleration of 1g was used to simulate the submodel of the microgenerator. A seismic mass of 400 µm by 400 µm and a beam of 400 µm length in an SOI wafer (410 µm thick) were used. An AC analysis was first carried out to study the behaviour of the system versus frequency. As shown in Figure 16, we have noted lower amplitude and higher resonant frequency for the AlN material. This result was expected because of the poor coupling coefficient of AlN material compared to PZT one.
To model the power management circuit described in section 1.1.4, we chose SPICE language. In fact, instead of trying to equal SPICE compact models, we decided to use parameterized SPICE models given by the tool. Thus, we had to select the appropriate model of transistor. The Level1 MOS was selected in order to decrease simulation time. In fact, this model is a basic MOSFET model generally used for discrete components especially in power electronics but it is a good compromise between accuracy and time in system level simulations. To improve the accuracy of the model, BSIM4-V4 (level 54 in Smash™ 8.0 – Dolphin Integration) can be then used. This model takes into account the effects of device geometry and process parameters. It enables us to better predict the real behaviour of such system but it notably slows down simulation time. Global simulation results are presented on Figure 1.17. The simulated model consists on a structural connection between the parametric microgenerator with AlN layer connected with a structural model of a six stages voltage multiplier.

**Figure 1.17** Simulation results curves of 1µF capacitor charge for two different values of input acceleration amplitude.

### 1.1.5 New generators based on electro-active polymers

*Members: C. Jean-Mistral, J.J. Chaillout, S. Basrour*

Electro-active polymers (EAP) include electronic polymers (piezoelectric, dielectric, conductive polymers) and ionic polymers (IPMC, ionic gels…). A complete state of art has led us to select four polymer families: dielectric, IPMC, electrostrictif and piezoelectric polymers.

For each polymer type, an electromechanical model have been developed to characterize the behaviour of a simple structure (plate) according to a specific mechanical load (quasi-static or dynamic solicitation under
100Hz). According to our simulations the best promising electro-active polymers in terms of energy scavenging density are dielectric polymers. Their maximum energy density is about 1.21J/g. But in the worst case (high pre-strain), energy density can decrease down to 0.026J/g, value already close to the best ones available for piezoelectric materials. In Figure 1.18 is plotted the scavenging cycle for dielectric polymer.

![Deformation mode](image)

**Figure 1.18 Dielectric generator cycle**

First prototypes named A, B and C on Figure 1.19 have been realized and characterized to validate our analytical model.

![Flexible frame](image)

**Figure 1.19 Dielectric polymer prototype (a) and the output power harvested (b)**

Various experiments have been performed: with different pre-stretch for the film, with different size for the dielectric generator. We obtain the same kind of curves with relative error between 10% and 30%. The improvement of the model is necessary. Dielectric characterizations have been performed to test the influence of temperature, frequency and pre-strain on dielectric constant, conductivity for example. First results show us a dielectric constant higher than the expected one at room temperature and at very low frequency. Moreover, mechanical contactless characterizations have been carried out to improve the model.

The model developed in this study is complete and validated by various experiments at room temperature. It takes into account a lot of parameters and can be used to design power generators based on dielectric polymers. The maximum energy density scavenged with this technique is about 1.21J.g^{-1} for one cycle at
constant charge Q. We are developing an innovating application for the scavenge energy from human walking. This system is a patch placed first in a knuckle and able to scavenge 100µW to supply autonomous device for medical or sport applications. First prototype characterizations are under investigation. In the near future, new power management circuits and miniaturized n-stacks structures will be studied.

1.1.6 Thermal energy scavenging

Members: L. Carlioz¹,³, J. Delamare³, S. Basrour¹

¹ TIMA, ³ GE2Lab

Before anything else, let's just start by explaining what we intend by thermal harvesting. Classically, thermal is a synonym of spatial gradient of temperature, that is to say a difference of temperature between two physical points. Such a gradient is commonly used in thermoelectronics where industrial micro generators are already a reality.

Our approach is somehow different since we focused our attention on temporal change of temperature, i.e. the evolution of temperature along the time. This field was not really documented and some state of the art was necessary in order to determine the various solutions available to answer this problematic.

One of the first considerations before starting this part was to choose the variation of temperature that will be considered. We selected the range from a human environment (some °C in one hour) to an industrial one (e.g. a car engine with a change of a few tens of °C in 5 s). Of course, the lower the temperature's change the better it is for an easy adaptation in every situation.

The preliminary research underline the fact that several possibilities existed that can be divided into two different routes: direct conversion (thermal to electric conversion) and indirect one. Pyroelectricity and magnetization change were part of the first group whereas shape memory alloys and hybridization of soft magnetic materials and piezoelectric belonged to the second one.

Shape memory was quickly discarded because it was too much dependent of the temperature evolution along time. This effect could have been counteracted by using magnetic shape memory alloys for example. But those materials were quite a new discovery and thus not yet fully characterized. Consequently the knowledge on how to use them and how to prepare them was too difficult to obtain.

Magnetization change materials had also the same problem. In order to obtain a sufficient magnetic flux variation, the change of magnetization should occur across a time span as short as possible. This implies important variations of temperature during a small amount of time. This is impossible considering our initial requirements.

Pyroelectricity was then studied, with a special focus on PVDF (PolyVinylidene DiFluoride) since some samples were already available. A first model based on the literature was elaborated in order to determine how much energy could be generated using pyroelectric effect. The amount of energy harvested by this technique is very weak.

Finally the last way explored was the one of the hybridization of piezoelectricity and magnetism. The system is composed of a bimorph of PZT upon which is glued a hard magnet (Figure 1.20). This magnet is attracted by a soft magnetic material when the temperature is below the Curie temperature. This is the default position of the generator. When the temperature overcomes T_C, the soft material is deactivated and the beam oscillates back to the neutral position. Changing from one state to the other is decoupled from the temperature temporal evolution due to the fact that the magnetic force is highly non linear. An off the shelf prototype has been built as a concept proof. Now the model has to be detailed and the optimisation of the geometry could then be developed. Some macro prototypes have been developed and some encouraging results have been obtained (100 µJ with a variation of T between 38°C and 48°C).
1.2 Design and technologies for Integrated Micro and Nano Systems

MEM Resonator Frequency Compensated, NACRE Nano 2012

*Members: S. Basrour, Y. Civet, F. Casset, J.F. Carpentier*

\[^1\] TIMA, \[^2\] ST Microelectronics, \[^3\] CEA LETI

The performance of our electronic systems is generally limited by the accuracy and stability of the clocks or frequency references they use. Micro-Electro-Mechanical resonators (MEM) offer a promising alternative to industrial Quartz crystal time references thanks to size reduction, low cost, CMOS integration and multifrequency applications. However, since MEM resonator frequency is linked to device dimensions, manufacture mismatch induces frequency deviations. This work proposes to investigate an “in-line” trimming by compensation holes filling or localized deposition. Flexural beam and bulk mode (Plate & Disk) resonators have been studied with compensation holes smartly localized onto microresonators. Because of compensation holes, frequency is shifted either up or down depending on holes distribution. Figure 1.21 shows SEM view of a wine-glass mode disk resonator with 40nm electrode to resonator gap (a) and frequency shift of clamped-clamped microbeam (b).

Further electrical measurements are under progress onto holed bulk mode resonators to observe frequency shift. We propose then to fill holes after an initial measurement, allowing to fix the required compensation material volume needed. Analytical model has been developed and reports drop of 350ppm (10nm Silicon epitaxied) and shift up of 4000ppm for 50nm Silicon epitaxied.

We also investigate localized correction without holes for fine tuning. Indeed, accuracy of few ppm is typically required for industrial prospects. Further developments are on going to check the relevancy of this technique and the achievable resolution.
1.3 BioMEMS

1.3.1 Introduction

The progress in MEMS is being applied to biomedical applications and has become a new field of research unto itself, known as BioMEMS. MEMS technology has enabled low-cost, high-functionality devices in some commonly used areas. BioMEMS applies these technologies and concepts to diverse areas in biomedical research and clinical medicine. BioMEMS is an enabling technology for ever-greater functionality and cost reduction in smaller devices for improved medical diagnostics, therapies and surgery. With its knowledge and research in MEMS, our group is positioned to investigate and develop BioMEMS. Furthermore, the research environment in Grenoble provides the necessary multidisciplinary collaboration that will be required for the implementation of novel ideas into BioMEMS. The inherent characteristics of BioMEMS promise the production of miniature, smart, and low-cost biomedical devices that could revolutionize clinical applications such as implantable devices, surgical instruments and diagnostic tools.

1.3.2 Artificial Urinary Sphincter

*Members*: H. Lamraoui, A. Bonvilain, P. Mozer, P. Cinquin, S. Basrour

Members: H. Lamraoui, A. Bonvilain, P. Mozer, P. Cinquin, S. Basrour

1 TIMA, 4 TIMC, 7 Groupe Hospitalier Pitié-Salpêtrière

These research works at TIMA laboratory in collaboration with TIMC-IMAG laboratory and an urologist physician at the hospital la Pitié Salpêtrière in Paris propose to solve the problem of urinary incontinence with a new adaptive autonomous artificial urinary sphincter.

Urinary incontinence is defined as the involuntary leakage of urine and there are several surgical methods to alleviate. In the event of a major leak, the establishment of an artificial urinary sphincter can give patients a normal social life. At the moment, there is only the prosthesis developed by the American Medical System company (*Figure 1.22*) which remedies severe incontinence.

*Figure 1.22 Artificial urinary sphincter AMS 800* (a) cuff (b) balloon (c) pump

This technology, patented is to replace the manual pump mechanism used by many patients worldwide by a mechatronics device. So far the device consisted of a fluid-filled cuff placed around the urethra, like a ring. It is connected to a pump implanted in the scrotum (*Figure 1.22*). When the patient wants to empty his bladder, he presses the pump that drives water from the cuff to a balloon. The urethra is no more compressed and release urine. Although improving significantly the patient continence, the existing system suffers from significant shortcoming. Indeed, maintaining high pressure on the urethra, which is essential during physical activities but useless in a supine position for example, can eventually cause atrophy or erosion of the urethra, thus requiring the withdrawal of apparatus. In addition, the location and the size of the hand pump make handling difficult, particularly for elderly or suffering from other disabilities.
The prototype developed in these researches (Figure 1.23) allows better control by the user to adjust the pressure to the patient even if the device is already implanted and perform dynamic control of pressure based on the activity and the posture of the patient.

![Prototype of the new patented artificial urinary sphincter](image)

**Figure 1.23** Prototype of the new patented artificial urinary sphincter

A spin-off UroMEMS is created in 2011 with the objective of commercializing a first product in 2013. The scheme is aimed at first to men who underwent radical prostatectomy due to cancer of the prostate. The market represents approximately 10,000 prostheses per year worldwide.

In these works, we propose a study on a dynamics control of the system that improves its efficiency by adjusting the behaviour of the system to the patient and his lifestyle. We developed also a communication between the implant and the outside world via a RF link.

Our work lies in the choice of microsensors allowing the monitoring of the activity and the posture of the patient, the development of a command and in the study of energy consumption. The prototype consists of micro-actuators commanding by microsensors and an electronics control which treat the physiological signals. The energy consumption necessary for a long enough functioning device is defined, in order to provide the most appropriate solution.

At first, we do a feasibility study of a new implantable urethral occlusion system for treating urinary incontinence by severe sphincter deficiency. This system is based on an electromechanical actuator that allows the occlusion of the urethra and functions that provide electronic data processing, two-way communication, an ergonomic setup and control the actuator based on the measured information patient. Sensors are indeed embedded in the system to apply a urethral occlusion pressure adequately. We see that the theoretical autonomy of the system, based on power consumption of standard components, is more than 4 years.

The processing of signals from measurements performed on the patient and the extraction of various relevant information for the adaptation of occlusive pressure of the artificial urinary sphincter has been performed. We developed the methodologies used to help assess particular activity, posture and intra-abdominal pressure of the patient. The detection algorithm designed to be implemented in the artificial urinary sphincter is then established.

Experiments in 16 healthy volunteers in the context of a clinical trial protocol were conducted to evaluate the detection algorithm of artificial urinary sphincter activity, and to compare the characteristics of the measure mechanomyographic (MMG) compared to those of electromyography (EMG) (Figure 1.24), considered today as the reference method. It was shown that the detection performances of our algorithm in the recording conditions are satisfactory, since the 8 activities to be detected by the algorithm using only the accelerometer were detected successfully in over more than 78% of cases. We then see that the
measurement of muscle activity by the accelerometer (measuring MMG) from the EMG, this poorer performance in terms of activation time at events involving a sudden increase in intra-abdominal pressure (IA). Finally, we see that the study on the correlation of 2 signals during the Valsalva maneuver does not allow us to affirm that MMG signal can be used to estimate the IA pressure.

![Figure 1.24 MMG and EMG signals after treatment during coughing](image)

Finally we designed and tested the prototype of the artificial urinary sphincter. It incorporates a mechatronic system for compressing the urethra with a predetermined pressure at a distance by the user through a graphical interface developed for the control and configuration of the prototype. The mechatronic system and functionality of the device were then evaluated and validated in vitro (Figure 1.25), then in a second time in vivo (Figure 1.26) in an animal (a female dog). An example of detection of events involving leaks from the urinary incontinent patient is then tested with the recorded measurements in healthy volunteers, included in the prototype. Finally, the power consumption of each system function was measured and the autonomy of the prototype was evaluated at 2.8 years for a constant occlusion pressure. The autonomy of theoretical prototype is then recalculated with the electromagnetic motor offer a higher yield. We will see that it is about 11 years for a cumulative change in pressure of 1000 cmH2O per day.

![Figure 1.25 In vitro experiments](image)
Actually, we work on the use of piezoelectric actuator in order to make the prosthesis MRI compatible. At last we envisage using Biopile developed at TIMC-IMAG laboratory like a good candidate to power the device. And after, the critical elements that must be taken into account concern the packaging and the biocompatibility (for implantable devices).

1.3.3 Deformation measurements of a cylinder : particular case of a medical needle

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\textsuperscript{1}TIMA, \textsuperscript{4}TIMC, \textsuperscript{6}3SR

These research works at TIMA laboratory in collaboration with TIMC-IMAG and 3SR laboratories propose to solve the problem of knowing the precise position of the tip of a flexible cylinder inserted in a non-transparent environment.

Percutaneous medical procedures for diagnostic or therapeutic, guided or not by imaging (ultrasound, fluoroscopy imaging, resonance imaging magnetic, etc.) are to introduce, through the skin, an instrument that can be deformed, to a target previously identified. Different types of instruments are commonly used in everyday medical practice for such interventions, in particular, needles. To facilitate the implementation of these procedures, tools for tracking and navigation were specifically developed for twenty years to see, in real time and in a virtual environment, the representation of the reality of the relevant interventional procedure: the target, a three-dimensional model of the instrument and its actual and projected path. The assistance provided by these systems, increasingly used in practice daily, allows the therapist to guide the instrument toward the target more precisely with decreased morbidity.

While these tools have really helped revolutionize medical practices, they suffer from several limitations among which two are specifically identified: the cost and the assumption of the dimensional stability of the instrument used. Indeed, the interaction of deformable instrument with human tissue is the source of its deformations that can cause failure of interventional medical procedure.

This work is focused on the integration of microsensors on the deformable tool to allow the monitoring in real time of its deformations.

We first conducted a feasibility study by developing a macroscopic prototype consisting in a medical needle to which we glued manually commercial gauges. Experiments of this first prototype have allowed us to validate the analytical and numerical models developed and to determine the accuracy of the measured position of the tip of the needle that is 0.5 mm.

So we looked to integrate microgauges directly on the body of the needle. For this, the substrate and the material of the needle being unconventional to perform microfabrication, it is the lock to overcome. So to adapt the shape of the substrate on the equipment, we designed and built a support (Figure 1.27). This support has the same shape than a 5’ wafer but it is made by steel and is very thick (5mm). There is round grooves just under the surface which are opened on the top of the support. So the needles surpass (about 50µm) the top of the support, which will make difficult the coating of the resist.
We determine the dimensions and the constitution of the microgauges with the help of the previous analytic and numeric modeling. Then we determined the process of microfabrication of the microgauges on the needles (Figure 1.28). The needles used are of two types: steel and nickel-titanium (NiTi) which is a shape memory alloy (SMA). Because of the particularities of the needle (shape and material), we must be careful with the different temperatures during the fabrication process.

Polysilicon must be better piezoresistif material for the microgauges, but we use Ge, because it allows us to minimize the temperature of the annealing. It gives a less gauge factor than polySi, but Ge is more usually used for flexible substrates thanks to its low temperature of annealing.

After determining the parameters of achievement, we have made a first photolithography. This one is made difficult by the shape of the substrate (needles surpassing the top) and the annealing temperature of the resist that is poorly controlled because of the thickness of the support that generates a significant thermal inertia. For example, the use of a negative resist is not possible because of the intermediate annealing which is too critical. However, after making the masks, we can achieve with a thick resist a photolithography (Figure 1.29) in anticipation of a lift-off. We test after the lift off with aluminum (Figure 1.30).
With these results, we have shown that it is possible to integrate microsensors on the body of a surgical tool directly by microfabrication if it is possible to adapt it on the clean room equipment. It will open a new way to monitor deformable tools inserted in non transparent environment.

We can now consider the fabrication of microgauges on needles using the process developed. The next way is to integrate several microgauges on three generatrix of the needle at 120°. It will take into account the connections along the needle.
2. Concurrent Integrated Systems (CIS)

Group Leaders: Laurent Fesquet, Gilles Sicard
(e-mail: Laurent.Fesquet@imag.fr; Gilles.Sicard@imag.fr)


<table>
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<th>Research areas</th>
<th>Contracts</th>
<th>Partners</th>
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<td>ST Microelectronics, France Telecom R&amp;D, CEA-Leti, CEA-LITEN, E2V Semiconductors, Tiempo, Coronis Systems, INRIA, Thalès, Dolphin, Telecom ParisTech</td>
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<td>Smart CMOS Vision Sensors:</td>
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<td>High Dynamic Range, Adaptive sensors,</td>
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</tr>
<tr>
<td>Smart Read-out systems</td>
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2.1 Asynchronous circuits and systems

2.1.1 Introduction

The global synchronization strategy of synchronous circuits was introduced in the early 70s because at that time, it was a satisfactory answer to design needs and technological potentials. This initial choice of an implementation strategy, drove and is still driving the design of algorithms/architectures, languages and CAD tools. Today, integration potentials of advanced technologies are going beyond design productivity, and one can wonder whether the synchronous circuit style is still relevant. Asynchronous circuits which were introduced in the mid 50s, receive now increasing interest. What significant benefits are they likely to offer? Can they contribute to improve design productivity in the future? Our motivation is to answer these questions, investigating what impact asynchronous circuits may have on the design of integrated systems and how to take advantage of this circuit style at different levels: circuit level, architectural/algorithmic level, specification level, and system level? Because asynchronous circuits provide more flexible, robust and reliable synchronization and communication mechanisms, they give rise to alternative and innovative solutions that have to be analyzed and evaluated.

At the circuit level, asynchronous logic enables the design of delay insensitive circuits which do not require accurate and costly delay characterization. In fact delay insensitivity guarantees a correct functional behavior independently of the propagation delays in the basic components (gates, interconnects...). Delay insensitive asynchronous circuits are for example insensitive to some emerging problems like delay fault due to crosstalk or process variations. The delay insensitivity property makes asynchronous circuits very promising to exploit advanced CMOS and nanometric technologies. Eliminating the global clock, which synchronizes all parts of circuit in synchronous logic, provides more flexibility to design system architectures. In fact, the control is naturally distributed rather than centralized. Hence, communications as well as synchronization through «rendezvous» for example, are easily implemented by a collection of independent and local finite state machines, which do not require knowing the state of the whole system. Data to be computed by the system flow in the architecture as fast as they can accord resources’ availability and hardware implementation. The processing cost (in terms of delay and power consumption) is exactly the image of what is specified by the algorithm, given the chosen hardware implementation. It means that speed and power consumption may depend on the data processed. The data-flow behavior of asynchronous circuits, at any level of granularity, is the source of significant improvements in terms of speed/power optimizations and ease of design. Moreover, this approach can be fruitfully coupled to an event-based non-uniform signal processing which provides drastic power reduction, thanks to an dedicated signal processing theory.
Finally, asynchronous circuits also bring flexibility at the system level. Complex, highly concurrent image processing applications naturally take advantage of the locality and modularity of clock-less circuits. Because they don’t need a global synchronization signal, modularity is a major property of asynchronous circuits which enables the design of complex integrated systems by simply assembling functional blocks. Design time is thus reduced and reusability increased. As an example, the design of locally-synchronous globally-asynchronous SoCs bring a solution to the problem of communications between distant parts using long interconnects. Without requiring drastic change in terms of tools and methodologies, synchronous parts of SoCs may be interconnected using advanced and robust asynchronous interfaces.

The potentials of asynchronous circuits are being investigated through the design of mobile systems (from smart-card to multimedia terminal). There are three main properties of asynchronous circuits that can improve such systems and/or make their design easier: electromagnetic compatibility, low power, power management and flexible interfacing capabilities. Interfacing digital asynchronous circuits with analog parts (RF front-end, sensors, actuators, etc.) is also a major field of interest. It is in fact essential if we expect to successfully design SoCs that may integrate various kinds of digital and analog parts.

2.1.2 CAD tools and design flow

A design flow has been developed at TIMA since 2000. The first step was to build a tool (TAST) for synthesizing asynchronous circuits. TAST stands for TIMA Asynchronous digital circuit Synthesis Tools. This is a design environment which is gathering researches carried out in the group on asynchronous circuits design methods and associated CAD tools. This work has been concluded in 2007 by the creation of a spin-off company, Tiempo.

The group is now focused on specific CAD tools in order to target non functional specifications such as:
- lower area and higher speed
- ultra-low power,
- security driven synthesis to get power attack resistant and fault tolerant circuits,
- EMI (Electro Magnetic Interference) driven synthesis,
- formal verification of models and circuits (collaboration with the VDS group).

2.1.2.1 SystemC add-on

SystemC is a Hardware Description Language (HDL) based on C++ allowing describing a system at different levels of abstraction. SystemC provides a set of predefined ports and channels which enables communication between entities. An open source simulator allows simulating and testing a system modeled in SystemC. The SystemC library and simulator were designed for modeling synchronous circuits and thus have some limitations for modeling asynchronous circuits. We have defined a new subset of SystemC called ASC (Asynchronous SystemC) allowing to accurately modeling asynchronous circuits. This SystemC subset is based on a set of ports and channels primitives offering the same communication primitives as the common languages used for asynchronous circuits modeling (CHP, Tangram or Balsa). ASC also offers some new operators and statements allowing to accurately modeling the basic components of an Asynchronous Network on Chip. We are also doing some modifications on the SystemC simulator kernel for efficiently simulating the models described with ASC. Our final goal is to be able to synthesize these ASC models with the TAST framework. We are currently formally defining the semantic of the ASC library for being able to efficiently synthesize ASC based models.

2.1.2.2 The TAL Libraries

TAL-130 stands for TIMA Asynchronous Library; it has been designed using the standard CMOS 130nm process from STMicroelectronics in collaboration with the LIRMM laboratory. The library contains around 170 standard cells that we unfortunately do not find into conventional synchronous standard cell libraries. About 30 different functionalities implementing various kinds of C-elements and combination of C-elements have been included in the library. All the cells of TAL are layout compatible with the standard cell library provided by ST so that the designer can mix the use of conventional and TAL cells in his/her design. Moreover, TAL can be use in all the standard design tools such as Cadence, Synopsys, Modelsim, ... The aim of TAL is to enable the design of asynchronous circuits that are smaller, faster and which consume less power than those obtained using conventional synchronous standard cell libraries. To evaluate the performance gains brought by the library, two cryptographic circuits (AES) have been designed and fabricated using TAL-130. The next table presents a comparison between an AES design with the TAL library and a previous version of the same circuits exclusively designed with conventional standard cells.
A new version of TAL 130 has been designed. The aim of this version is to propose low-power cells in terms of dynamic consumption and static consumption. This library can also be used with low-Vdd values. This library is compliant with the core standard cells available in ST 130nm design kit.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Description</th>
<th>Core Area / Total Area / Nb of equivalent gates</th>
<th>Placement density</th>
<th>Number of IO</th>
<th>Key Length</th>
<th>Cyphering time (ns)</th>
<th>Energy (nJ)</th>
<th>Current (mean) mA</th>
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<td>AES component 1</td>
<td>Standard cells</td>
<td>0.648 mm² / 1.55 mm² / 70247 gates</td>
<td>63%</td>
<td>42</td>
<td>128</td>
<td>1025</td>
<td>12.5</td>
<td>12.3</td>
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<td>AES component 2</td>
<td>TAL cells</td>
<td>0.507 mm² / 1.217 mm² / 60336 gates</td>
<td>60%</td>
<td>42</td>
<td>128</td>
<td>928</td>
<td>10.42</td>
<td>11.23</td>
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TAL-65 is a library with asynchronous cells, designed using STMicroelectronics 65 nm CMOS process. The library contains about 150 cells all compliant with the core standard cells available in ST design kits. The TAL-65 library also includes some specific cells required for the design of asynchronous network on chips. TAL-45 is a library which is fully compliant with the 45 nm ST CMOS standard cells. This library contains about 40 cells. Notice that a TAL library is also available for Altera FPGA. The group started to investigate a TAL library dedicated to flexible organic electronic.

### 2.1.2.3 Synthesis method for low-power QDI state machines

In order to target low-power circuits, a complete direct mapping synthesis method from a state machine graph model has been developed. The Method covers the synthesis of sequential QDI controllers and shows a major enhancement in circuit performance compared to HDL-based synthesis method. Such controllers makes possible to apply local optimization techniques at gates level, especially for reducing power. We demonstrated the synthesized circuit performance enhancements compared to HDL based synthesis method by electric simulations. Two examples are synthesized and simulated using 130 nm CMOS technology. The results show enhancements in terms of power consumption, area and circuit latency. A circuit example has been synthesized (with TAST and our methods) and simulated using Synopsys Nanosim (see Table 1). The circuit is a configurable shift register sequential controller (27 states) and is implemented using the TAST synthesis method and our method (with an optimized flavor too).

<table>
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<tr>
<th>Controller (27 actions)</th>
<th>Number of transistors</th>
<th>Dynamic power (uW)</th>
<th>latency (ns)</th>
<th>Dynamic energy(pJ)</th>
<th>Static power(nW)</th>
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<td>7992</td>
<td>115</td>
<td>4918</td>
<td>566</td>
<td>724</td>
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<td>2170</td>
<td>69</td>
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<tr>
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**Table 1**

### 2.1.2.4 Asynchronous assertion monitors

This work has been done in cooperation with the VDS group and deals with assertion based verification techniques. The idea is to generate asynchronous monitors from a normalized property description language such as PSL (Property Specification Language) or SVA (System Verilog Assertions). PSL is a standard formal language to specify logic and temporal properties in a declarative style, under the form of assertions. We defined a library of components, and an interconnection method to automatically synthesize hardware monitors that can be linked to a prototype of the design under verification, thus providing an efficient debugging platform. The existing tool produces asynchronous on-line checkers that are connected to the monitored design. The on-going work aims at snooping the design with monitors built from asynchronous modules. The monitors are thus reliable in the case of truly asynchronous events, and become applicable to a wider range of verification tasks, notably the communications among globally asynchronous modules.
Monitor synthesis principles

PSL distinguishes four satisfaction levels for a property: hold strongly, hold, pending, fail. Moreover, due to the composition of elementary properties to form complex ones, we have to face these two requirements:
- some sub-properties have significance only after some “starting” event has been observed (e.g., right-hand-side of a temporal or logic implication)
- some sub-properties of an “always” invariant property may be “restarted” before the result of a previously started evaluation is known, and this restart should not abort the on-going evaluation.

The monitors we build reflect these requirements. When implemented in hardware, the monitor outputs display the property satisfaction level, and the indication that the answer is no longer pending may be used as an interrupt to trigger further actions. A monitor for a property P is built as a module that takes as inputs the reset, the synchronization signals (Start, Ack_out, Checking, Ack_in), a signal Start that triggers the evaluation, and the signals of the design under verification (DUV) that are operands of the temporal operators in P (see Figure above). The three monitor outputs have the following significance:
- Checking: a 1 indicates that output Valid is effective;
- Valid: provides the evaluation result;
- Pending: a 1 indicates that the monitor has been started and that the satisfaction result is pending; this is significant for strong operators.

The synthesis method relies on:
- A library of asynchronous primitive monitors, one for each PSL operator of the “foundation language”. The asynchronous library elements are designed with a Quasi-Delay Insensitive (QDI) style. This class of asynchronous (or clockless) circuits has the advantages to be robust (due to the delay insensitivity), scalable and reusable. Moreover, this design style is compatible with the standard FPGAs and it allows the prototyping of asynchronous or mixed (sync./async.) circuits on clocked FPGAs.
- A systematic connection procedure to build complex monitors from primitive ones, based on the PSL expression syntax tree. The Figure above illustrates the construction of the monitor for property P defined as:
  Property P is always (A ->B before! C));

These asynchronous monitors are well-suited to check properties in GALS communication systems and to online monitor critical safety systems.

2.1.3 Asynchronous circuit design

2.1.3.1 Secure circuit design and smart-cards

DES and AES crypto processors

DES and AES crypto processors were designed to evaluate the benefits brought by asynchronous logic to improve circuits’ resistance against power analysis attacks. DES prototypes (see Figure 2.1) were jointly designed by TIMA, LETI and STMicroelectronics within the Esp@ss-is Medea+ European project. The goal of this work is to study the introduction in smart-card IC design of an innovative hardware technology, namely Asynchronous Logic, and to evaluate how it can improve security.

A test board is under development to enable us to perform Differential Power Analysis and measure the ability of this technology to resist against such attacks.
Fault tolerant QDI asynchronous circuits

Differential Fault Analysis (DFA) is a well-known method for cryptanalysis. With DFA it is possible to retrieve secret cryptographic keys by analysing the results of correct and erroneous cryptographic computations. A successful DFA attack depends on two conditions. First: the algorithm must be known and vulnerable. Second: it must be possible to induce faults on the hardware platform. The procedure of DFA depends on the cryptographic algorithm. Successful attacks were done on the Data Encryption Standard (DES).

QDI asynchronous circuits are attractive to design fault resistant systems against a large class of faults. We show that the fault resistance of a circuit can be improved by exploiting QDI asynchronous logic properties. A secure fault tolerant DES prototype was designed to evaluate the hardening techniques we apply against fault injection (see Figure 2.2). The secure circuit is only 7% larger and about 20% slower than the non-secure initial circuit. Both the reference and the secure circuits are to be tested under a laser fault injection system within the Duracell RNRT project (see Figure 2.3).

The counter-measures implemented in the secure version have been evaluated and validated. The fault tolerance of the protected modules was improved by 2.5 and all the faults injected were either filtered by the counter-measures or detected by alarm cells. Thus a DFA appeared impracticable on the secure version.
It is worthwhile to mention that the proposed techniques to harden the QDI circuits against faults do not alter the counter measures that can be applied for PA. Therefore, this technology enables us to jointly harden circuits against fault and power attacks.

2.1.3.2 Asynchronous Programmable Logic

Introduction
The integrated systems today require flexibility, performance and reconfigurability. The trends in this domain lead to integrate on a single chip different processing cores, communication units and reconfigurable logic. Therefore the Systems on Chip (SoC) can embed programmable logic. In order to challenge the reconfigurability paradigm for special issues such as communication, synchronization or security, the asynchronous logic is a very promising approach. Nevertheless, the standard programmable logic blocks are not well-suited to map asynchronous circuits. The goal of this study is to define a more adequate programmable structure to implement asynchronous designs on SoCs embedding a reconfigurable part. This project aims the design of a Programmable Logic Device dedicated to the implementation of clockless circuits.

PLD Architecture
The group has investigated a novel Programmable Logic Device (PLD) architecture for implementing and prototyping various styles of clockless or asynchronous circuits. Many classes of asynchronous circuits exist, depending on the timing assumptions that are made at the logical level and the adopted handshake communication protocols. This work aims to break the dependency between the PLD architecture dedicated to asynchronous logic and the logic style. Indeed, the existing PLDs dedicated to asynchronous logic are always style-oriented. The proposed programmable structure is flexible enough to be used with different logic styles and asynchronous design flows.

Many asynchronous circuits are constructed with Muller gates. In order to support this specificity, a new Look-Up Table (LUT) architecture, which is well-adapted to the Muller gate implementation, has been designed.

This new LUT (see Figure 2.4) allows the combination of a single memory-point with combinational logic. This programmable memory is realized thanks to an optional feedback structure. This architecture has been evaluated in CMOS, Pass-Transistor Logic and 3-state logic which is a non-conventional way to design LUTs. The simulations demonstrate that, at equivalent power consumption, a higher speed is observed for the 3-state logic.

This work is also associated to the TAST project in order to efficiently map and prototype multi-style logic asynchronous circuits.

An asynchronous e-fpga for security applications
With the growing security needs of applications such as homeland security or banking, the frequent updates in cryptographic standards and the high ASIC costs, the ciphering algorithms on an asynchronous embedded FPGA co-processor are becoming a viable alternative. A novel asynchronous e-FPGA has been designed and fabricated (Figure 2.5).
This architecture is natively robust against side channel attacks such as simple and differential power analysis or clock based fault attacks. Many countermeasures are already implemented in ASICs to prevent SPA, DPA, EMA and FAs. The approaches using QDI asynchronous circuits appear to be very promising and this work aims at transposing these methods in an e-FPGA context. The challenge is first to make the asynchronous FPGA natively robust against SPA and DPA while being very flexible. Afterwards, countermeasures against other SCAs and FAs can be easily explored and experimented. The e-FPGA is expected to provide the following advantages for security:

**Balanced power consumption** — QDI circuits which generally use 1-of-n encoding (for example: dual-rail, triple-rail, etc.) can be balanced to reduce the power consumption dependency with the processed data. Indeed, the bit encoding ensures that the data are transmitted and computations are performed with a constant Hamming weight. This is important since the leakage of the Hamming weight or distance can be exploited by SPA, DPA, and EMA.

**Absence of a global clock signal** — No clock means that FAs based on clock are removed. Moreover, DPA and SPA attacks without global clock signal are expected to be much more difficult. Indeed, the clock absence will make very complicated the synchronization of the DPA and SPA signatures.

**Environment variation tolerance** — QDI circuits adapt to their environment such as voltage and temperature variations, which means that they tolerate many forms of fault injection (power glitches, thermal gradients, etc.). These QDI circuits can be easily combined with other countermeasure to efficiently counteract FAs.

**Redundant data encoding** — QDI circuits typically use a redundant encoding scheme (1-of-n). For example, the dual-rail encoding (a bit is encoded onto two wires) provides a mean to encode an alarm signal to counteract FAs.

To validate the e-FPGA native robustness against SPA and DPA attacks, an electrical simulation campaign has been carried out on a Programmable Logic Bloc (PLB) of the e-FPGA which is designed in CMOS 65 nm technology. Remind that, to be robust against SPA and DPA, the PLB should have the same current profiles and a constant running time whatever the manipulated data.

During the simulation, for a given secret key and the DES algorithm, random plaintext vectors have been processed.

The corresponding current profiles are shown on the Figure above. Whatever the manipulated data are, the current profiles are very similar. In other words, the power consumption is data independent. Moreover, the
observation of output variations shows that they are completely superposed. This means that the e-FPGA running time is data independent. This drastically increases the circuit robustness against SCAs exploiting the running time variations. In conclusion, with data independent power consumption and a constant running time, the proposed asynchronous e-FPGA architecture is natively robust against SPA, DPA and timing attacks.

2.1.4 Asynchronous blocks for SoC design

2.1.4.1 Asynchronous Self-Timed Rings for high speed serial links

In the industry of semiconductor, we can see a clear trend towards the use of high speed serial links between RF transceivers and baseband digital signal processing circuits. This type of relationship requires often generating a high frequency clock featuring high performances in terms of jitter and phase noise. These performances seem to be incompatible with conventional architectures of ring oscillators. Furthermore, the use of an LC oscillator has many disadvantages for these applications (surface, sensitivity to radiation and therefore EM pollution ...).

Oscillators are basic blocks in almost all designs: they are part of PLLs, clock recovery systems and frequency synthesizers. The design of low phase-noise multi-phase clock circuitry is crucial especially when a large number of phases is required. With the advanced nanometric technologies, it is required to deal with the process variability, stability and phase noise. Various applications have demonstrated that asynchronous circuits have great potential for low-power and high-performance design.

Self-timed rings (STR) are promising approach for designing high-speed serial links and clock generators. Indeed, the architecture of STR presents well-suited characteristics for managing process variability and offering an appropriate structure to limit the phase noise. Therefore, self-timed rings are considered as promising solution for generating Multiphase clocks. Moreover, self-timed rings can easily be configured to change their frequency by just controlling their initialization at reset time. At the opposite, inverter rings are not programmable.

A ring oscillator topology for high-speed multiphase oscillators based on self-timed ring oscillators has been developed. STR allows us to achieve a higher speed with a large number of multiphase outputs. Thanks to its architecture, based on request and acknowledgement signals, STR oscillation frequency is controlled by the STR initialization (number of tokens and bubbles). A comparison between STR and inverter rings shows clear advantages to STR. They efficiently increase the number of phases without frequency loss. Moreover, STR is able to efficiently scale the output resolution for matching the application requirements. Moreover, the configurability of the STRs allows us to reduce the phase noise by simply doubling the number of stages without changing the oscillation frequency. This work shows that STRs are a promising solution for the high resolution high-speed low-phase noise oscillators.

A test chip has been designed, fabricated and tested in STMicroelectronics CMOS65nm technology in order to verify our theoretical claims and validate our simulation results.

![Figure 2.7 STR die and STR under test (at ST Microelectronics, Crolles)](image)

2.1.4.2 Asynchronous clock generators for nanometric technologies

With the upcoming nanometric technologies, integrated system performances after fabrication will not be fully predictable. Indeed, the process variations really become huge at the chip scale. This implies to consider global management strategies in order to respect energetic and real-time constraints. Therefore performance estimation and management are today key points in new integrated systems. Solutions such as dynamic voltage and frequency scaling (DVFS) have to be considered, they have been explored and have shown to provide significant energy savings. The power reduction is a quadratic function of the voltage $V_{dd}$ and a linear function of the clock frequency $f$. As a result, Dynamic Voltage Scaling (DVS) can be used to efficiently manage the SoC energy consumption. Supply voltage can be reduced whenever slack is
available. This reduces the system speed which implies the use of Dynamic Frequency Scaling (DFS), to keep correct system behavior. The addition of DFS to DVS results in additional linear power savings. The application of DFS to a system requires the use of a source for generating adjustable clocks. For example these clocks can be derived from analog voltage controlled oscillators (VCO), which are a part of a phase locked loop (PLL). However, VCO have a limited operating range and a required stabilization time when changing the frequency. Another solution is to use a standard clock divider, but this will make the time resolution coarser, due to counting integer periods of the input frequency. In addition, they give regular time step which implies irregular frequency step (usually frequency step follows “1/x” curve).

Self-timed rings are considered promising solution for generating clocks. They can be efficiently used to generate high-resolution timing signals. They are robust against process variability in comparison to inverter rings. Moreover, for a given number of stages self-timed rings can be reconfigured easily their initial state, while in the contrary, inverter-ring frequency is fixed. The group investigates the design of Programmable/Stoppable Oscillators which are based on self-timed ring to exploit their interesting characteristics. Through a handshaking protocol, the oscillator is communicating with the synchronous processor to insure a proper switching from one frequency to another. The oscillator is designed in order to avoid the presence of glitches and truncated clock periods.

![Self-timed ring schematic](image)

Figure 2.8 Self-timed ring schematic

### 2.1.5 Non-uniform Digital Signal Processing and Sampling

#### 2.1.5.1 Analog-to-Digital Converters Based on Non-Uniform Sampling

This work is a contribution to a drastic change in standard signal processing chains: Analog-to-Digital Converters (ADCs), digital processing circuits, Digital-to-Analog Converters (DACs)... Integrated Smart Devices and Communicating Objects are the important applications targeted by this study. The main objective is to reduce their power consumption by one or two orders of magnitude, by completely rethinking their architectures and the associated signal processing theory.

Most of integrated systems bring signals with interesting statistical properties into operation, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, electro-cardiograms, speech signals...) are almost always constant and may vary significantly only during brief moments. Thus, classical regular sampling systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. The new idea of this work consists in realising an adaptive sampling scheme of the analog input signal based on its amplitude variations, and implementing an architecture only driven by the samples occurrences. The sampling scheme is based on “level-crossing” that provides a non equi-repartition of the samples in time. Quantization levels are regularly disposed along the amplitude range of the signal. A sample is taken only when the analog input signal crosses one of them (cf. Figure 2.9). Samples are not regularly spaced out in time, because it depends on the signal variations. This kind of sampling is the dual case of Nyquist sampling: the amplitude of samples is perfectly known but their time instants are quantized.

In this context, we propose a new class of ADCs, based on this non-uniform sampling and on an asynchronous hardware implementation (without any global clock). The term A-ADC for “Asynchronous ADC” is now used. Contrary to previous works carried out in other laboratories, not only does the term “asynchronous” define the design mode but also the sampling scheme. The architecture of the A-ADC is a tracking loop enslaved on the analog signal (cf. Figure 2.10). It is composed of a difference quantifier, an up/down counter, a Digital-to-Analog Converter (DAC), and a timer delivering the time intervals. No external signal as a clock is used to trigger the conversion. To preserve the same state of mind, an asynchronous structure is chosen for the circuit. The information transfer is locally managed with a bi-directional control signaling between senders and receivers (requests and acknowledgements).

The theory associated with the A-ADC is completely different from classical Nyquist ADCs. The Signal-to-Noise Ratio (SNR) only depends on the resolution of the local timer and not on the number of quantization levels. A very low hardware resolution can also be implemented insuring a high SNR i.e. a high Effective Number Of Bits (ENOB). The silicon area and the power consumption can thus greatly be reduced. We have
elaborated a methodology to enable the designers to precisely calculate the design parameters of an A-ADC, given a target application. The input parameters are the analog signal characteristics and the desired ENOB, from which the four parameters characterizing an A-ADC are computed: the number of quantization levels, the loop delay, the timer period, and the number of bits for the timer. The following input signal characteristics must be perfectly known: Power Spectral Density, bandwidth, dynamic, and probability density. This method also determines the design constraints on the analog blocks of the loop.

We designed an A-ADC according to this theory, using the standard CMOS 0.12µm process from STMicroelectronics, for a speech application and an effective resolution of 10-bit. The converter has been implemented with a three stage micro-pipelined architecture, and a 4-phase handshake protocol. The photography of the die is given in Figure 2.11.

The maximum input frequency of the converter is: \( f_{\text{max}} = 160\text{kHz} \). This is much higher than the bandwidth of a speech signal, but this fact will not cause extra useless activity, nor extra power consumption for the converter. When the chip is running at its maximum speed, a power consumption lower than 180µW is measured. Lastly, the targeted resolution of 10-bit is reached for a frequency of the timer lower than 1MHz. The comparison of the A-ADC with standard Nyquist ADCs is done using the following Figure of Merit:

\[
\text{FoM} = \frac{\gamma \text{ENOB}^2 f_{\text{max}}}{P_m S},
\]

where \( P_m \) is the average dissipated power in Watts, \( f_{\text{max}} \) is the maximum frequency of the input signal in Hertz, and \( S \) the area of the core of the circuit in m². The FoMs of ADCs coming from recent publications have been computed or estimated. The best converters verify: \( \text{FoM} < 10^{19} \), and most of them: \( 10^{17} < \text{FoM} < 10^{18} \). Considering the characteristics of the A-ADC, the FoM of the A-ADC is: \( \text{FoM} = 2.10^{19} \), that is twice higher than the best ADC.

These interesting performances have been achieved by reducing the activity of the converter thanks to the non-uniform sampling scheme and its asynchronous hardware implementation. These two aspects constitute very promising ways of investigation in order to significantly reduce the power consumption of complex systems such as Communicating Objects or Smart Devices for Sensor Networks and/or ad-hoc networks applications.

**2.1.5.2 Non uniformly sampled digital signal processing**

According to the asynchronous digital signal processing chain defined in Section 2.2.8 and to the expected gain on power consumption, this work focuses on the signal theory of non-uniform sampling schemes and on possible implementations/architectures of such a non uniformly sampled signal processing.

It is well known that asynchronous designs exhibit interesting properties like low-power, low-voltage, low-EMI, etc. This kind of design has been used in a few publications to improve the performances of Nyquist ADCs such as: immunity to metastable behavior, reduction of the electromagnetic interference, speed, and power consumption savings. Moreover, most of the systems using ADCs imply signals with interesting statistical properties, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, pressure sensors, electro-cardiograms, speech signals...) are almost always constant and may vary significantly only during short moments. Thus, classical regular sampling and converting systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. It has been proved that ADCs using a non equi-repartition of the samples in time leads to interesting power savings compared to Nyquist ADCs. The new class of ADCs presented in Section 2.2.8 uses both the “level-crossing” sampling scheme and an asynchronous implementation of the circuit (no global clock).

This work follows this previous contribution, joining up the A-ADC to an asynchronous implementation of a circuit processing the non uniform samples (Figure 2.12).
Figure 2.12 Dual Approaches of Signal Processing Chains

Our new approach of signal processing is to combine asynchronous designs with signal event triggered processes in order to reduce dynamic activity. This work is dedicated to low-power applications especially in the area of Smart Devices and Communicating Objects.

Many studies deal with non uniform signal theory but are limited to mathematical aspects like recovery of additive-random or jittered sampling process. We decided to study the sampling scheme of the level-crossing sampling technique. Indeed, a sampled signal is obtained in the time domain by the multiplication between the analog signal and a function called “sampling function”. This implies in the frequency domain that the spectrum of the analog signal is convolved by the Fourier Transform of the sampling function: the sampling scheme. Usually in the uniform case, as the sampling function is a Dirac comb, the sampling scheme is also a Dirac comb. So the band base spectrum is duplicated around each multiple of the sampling frequency (the Shannon theorem is a consequence of the duplications). In the level-crossing non uniform case the sampling function depends on the signal. Thus the classical Discrete Fourier Transform (DFT) commonly employed for the spectral analysis of uniformly sampled signals is useless. In order to analyse the non-uniformly sampled signal scheme a new spectral analysis technique is devised. The idea is to combine the features of both uniform and non-uniform signal processing chains in order to obtain a good spectrum quality with low computational complexity. The proposed technique shows significant improvements in terms of spectrum quality and computational complexity if we compare it to the General Discrete Fourier transform or the Lomb’s algorithm, which are used with some non-uniform sampling schemes. Moreover, a linear interpolated Digital-to-Analog conversion can reconstruct the signal from its non-uniform samples according to the time-interval values. This also allows spectral analysis by computing the Continuous Fourier Transform on the interpolated functions.

Among all the digital processes, Finite Impulse Response (FIR) filters have been chosen for their stability and convergence properties to illustrate this work. The convolution operator is formalized in the non uniform sampling context in order to define an algorithm for the FIR filtering computation of non-uniformly sampled signals. An asynchronous iterative architecture is also proposed to implement the algorithm. It is formally proven that the computational complexity of the asynchronous FIR filter can be far lower than the computational complexity of the synchronous FIR filter, provided that the signal statistics are well exploited. It has demonstrated that the computational requirements, and hence the energy, can be reduced by more than one order of magnitude when compared to the standard uniform sampling scheme. This gain is due to the reduction of the number of samples processed. It should be noted that the gain could even be higher for other applications (medical, monitoring…).

A IIR filtering chain, which processes directly the non-uniform samples without resampling in a regular scheme, has also been studied. The non-uniformity in the sample times lead to choose a state representation for the filters. The stability of such systems is an issue and the performance of different numerical schemes (Euler, Bilinear, Runge-Kutta, …) used to implement the filters in this representation...
have been studied and compared in terms of stability, complexity and filtering quality when applied to classical filters as Butterworth, elliptic or Chebyshev filters. Euler schemes are to be rejected, the explicit one for being unstable and the implicit one for being in a sense too stable, i.e. too dissipative. The three other studied schemes (bilinear, RK23 and RK4) give qualitatively good results. If applied to N-order filters, only RK4 is effective (no matrix inversion), but if 1- and order decompositions are used, the complexity study does not allow to rank one of them clearly first. For RK23 and RK4, some oversampling is needed for inactive inputs to ensure stability, while this is unnecessary for the bilinear scheme.

Another developed approach is an efficient online processing technique for non-uniformly sampled signals which smartly combines the features of uniform and non-uniform signal processing. This has been applied to spectrum analysis and filtering. For filtering, the idea is to perform an adaptive rate sampling (relevant number of samples to process) along with an adaptive and optimal filter order (relevant number of operations per output sample) without an online filter calculation. This leads to minimize the computational load and enhance the power efficiency. Indeed the sampling is triggered when the input signal crosses one of the pre-specified threshold levels defined in the amplitude domain. As a result, the relevant and active signal parts are locally over-sampled in time. More the signal varies rapidly more it crosses the thresholds in a given time period. Contrary no sample is taken for the static signal parts. The approach is especially well-suited for the low activity sporadic signals. This smart sampling reduces the system activity and at the same time improves the accuracy of signal acquisition processes. In order to only process the active signal parts, an Activity Selection Algorithm (ASA) is used to window the relevant signal parts. ASA displays interesting features with AADC which are not available in the classical case. It correlates the length of selected window with the signal activity. In addition, it also provides an efficient reduction of the spectral leakage phenomenon in the case of transient signals. This is done by avoiding the signal truncation problem – which occurs in the classical case – with a simple and efficient algorithm instead of employing a smoothening window function. The selected data obtained at the output of the ASA can be used directly for further digital processing. However, in the studied cases, the non-uniform selected data are uniformly resampled. In these conditions, it is possible to apply a FFT or a classical filter to the selected data. For instance, in the filtering case, the data at the output of the ASA are decimated in order to once again reduce the processing activity. This leads to a drastic reduction of the processed sample number and to a significant decrease of the computational load.

To conclude, the digital signal processing chain using a level crossing sampling scheme behaves like the classical regularly sampled chain: an analog signal measured by a sensor can be sampled, processed and reconstructed in order to provide to an actuator a new analog signal. The difference between the standard technique and ours lies in the reduced number of samples taken for low-active signals. The level crossing scheme and the proposed signal processing theory implemented using asynchronous hardware lead to a significant reduction of power consumption making this technology very attractive for the low power SoC era.

2.2 Smart CMOS Imagers

Since 2003, researches on smart Image Sensors have done in CIS Group. The aims of these researches are to improve current CMOS Imagers on several ways:

- To obtain CMOS imagers with a High Dynamic Range (Works done before 2009, funding by the “PICS” Medea+ project, with ATMELE Grenoble, now e2v semiconductors Grenoble)
- To implement adaptive systems in order to obtain ideally the same image of a scene whatever external conditions. Currently, light adaptive systems and temperature problems are addressed.
- To reduce the huge amount of data at the output of the sensor: this research is focused on the design of dedicated readout structures in order to avoid the data extraction of a static pixel.

All these research works have the same technical constraints:

- Minimize the number of transistors in the pixel (up to 15) and the pixel silicon area
- Optimize the image processing chain allocation between pixel, column amplifier and the entire circuit in order to optimize the electronic behavior and the silicon area.
- Preserve, as possible, the behavior of a standard, industrial CMOS imager in term of electronic biasing capabilities, timing diagram, etc.

2.2.1 Light Adaptive Systems

A test chip, called “Imagyne 2” has been designed and focused on a very simple light adaptive system. It includes an array of 128x128 standard 3T pixels and an array of 64x64 2T logarithmic pixels. These two arrays are designed together: one Log. Pixel and four standard pixels are drawn together. The goal of this logarithmic array is to provide continuously the mean illumination value. With this information, we can perform the optimized integration time value of the standard pixels array at each image. This anti blooming system requires few transistors (+0.5 / pixel) and induces a reduced silicon overhead (less than 20%) in relation to the state of the art. This chip uses the 0.35um CMOS technology from AMS via CMP. Experimental results are shown in Figure 2.13.
Figure 2.13 Results of imagine 2 CMOS Imager. A) when light condition is modified (B and D cases), a basic sensor provides saturate images. B) With Imagyne 2 sensor, the integration time value is always the optimized one.

2.2.2 Temperature Compensation

CMOS vision sensors, as all electronic systems, are very sensitive to temperature variation. Mainly, this sensitivity limits their DC electrical behaviour. Figure 2.14 presents the temperature effect on the two main architectures of CMOS imagers: “Standard” imager (integration of the photocurrent) and “logarithmic” imager (continuous logarithmic response to the photocurrent).

Figure 2.14 Temperature effect on CMOS Imagers for low, medium and high values. A) “Standard” imager B) “Logarithmic” Imager

A strong variation of temperature, as shown in Figure 2.14 (like in automotive applications), implies saturation effect in the electronic image processing chain.
So far, no elegant integrated solution of this shortcoming has been proposed in the state of the art. In this work, we propose to find smart integrated solutions in order to preserve the DC behavior of the entire imager. Most solutions have been explored: Feedback loop, Zero Temperature Coefficient (ZTC) point and bandgap techniques. 

Figure 2.15-A shows simulation results obtain with ZTC solution on a standard imager. We reduce the variation of the output voltage by 98% of the total variation. This solution has been integrated in a test chip. Figure 2.15-B shows simulation results obtain with Bandgap technique on a logarithmic imager. We have reduced the output voltage variation of the sensor at most 96% and at least 78%.

![Figure 2.15](image)

**Figure 2.15** Temperature effect on CMOS Imagers for low, medium and high values. A) “Standard” imager B) “Logarithmic” Imager

This work is on-going and it’s supported by the “Vis-Imalogic” Minalogic project.

### 2.2.3 Smart Read-out Systems

Classical image processing is based on the evaluation of data delivered by a vision sensor in the form of images. These sensors with conventional clocks, receive visual information from the scene sequentially. Each array of data that is transmitted, recorded and that requires generally a post processing, carries the information of all pixels of the matrix without considering the constancy of some values. Therefore, this method leads us, depending on the dynamic content of the scene, to a high level of data redundancy. In this case of sequential reading, the output bandwidth of the sensor is shared equally among all the pixels in the matrix.

This work is focused on the implementation in a CMOS imager of a new control architecture which reduces the dataflow that goes through the ADC and that must be transmitted all the way after the converter. This architecture is based on the principle of the suppression of x-axis spatial redundancy. First work adds dedicated X-spatial event detector just before the global ADC. This scheme gives “Go-noGo” information and allows the pixel data to reach the ADC input or not. Due to this, a substantial gain is expected in term of power consumption or data flow rate.

Figure 2.16 shows Matlab results of this data flow reduction method. For this, we are looking to evaluate, in a certain scene, the number of pixels that have the same value of their precedent neighbour compared to the total number of pixels in the scene.

![Figure 2.16](image)

**Figure 2.16** Matlab results of the application of the algorithm on 2 photos
Results obtained are very promising. Note that the implementation of this dataflow reduction method doesn’t imply silicon overhead on the pixel. The photosensitive array is a standard one. This work is on-going and data flow reduction methods using temporal and/or spatial redundancy are under studying.
3. Reliable Mixed-signal Systems (RMS)

Group Leader: S. Mir
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<th>Research areas</th>
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</tbody>
</table>

3.1 Computer-Aided-Test techniques for AMS/RF circuits

3.1.1 Test metrics estimation using density estimation

Members: H. Stratigopoulos and S. Mir

Parametric test escape (e.g. the probability of a defective device passing the manufacturing test) and yield loss (e.g. the probability of a functional device failing the manufacturing test) constitute the major industry-relevant metrics for grading any test. The current practice for testing analog circuits nowadays is specification-based testing, where the performances that are promised in the data sheet are measured sequentially and compared to their specifications. This approach effectively controls the undesired parametric test escape and yield loss. However, the implicated cost is too high because it requires long test times and sophisticated test equipment. This high cost has sparked off intensified efforts to identify robust and low-cost alternative tests that could effectively replace the standard specification-based tests. Nevertheless, the progress that has been made is very limited. One of the primary reasons is the lack of tools to evaluate in advance and during the design stage test metrics, such as parametric test escape and yield loss, resulting from applying alternative tests.

Ideally, test metrics can be estimated during the design stage if we can afford to simulate the circuit a very large number of times, that is, one million times if we desire to estimate test metrics with parts per million (PPM) accuracy. However, this is practically infeasible as it requires immense computational efforts. Therefore, electrical simulations need to be replaced by statistical simulations in order to generate the large volume of data that are needed. There are several fast statistical simulation methods that can come to the rescue, including density estimation, response surface modelling combined with design of experiments, behavioural modelling, etc. However, they all suffer from limitations, which can lead to inaccurate estimates. More specifically, density estimation suffers from inaccurate fitting of the tails where the rare events that give rise to test escape and yield loss mostly occur. Response surface and behavioural models are approximate models of the actual circuit, thus it is very unlikely that they will capture all the dominant effects at the circuitual level that give rise to rare events.

In this work, we propose a method to estimate test escape and yield loss with the desired PPM accuracy when a single alternate test replaces a single specification-based test. The method is based on Extreme Value Theory (EVT) and statistical blockade. EVT is used to model the tail of the distributions of the alternate test and the performance where the rare events occur. Statistical blockade aims to speed up the simulation for generating the required samples to fit the extreme value model. The underlying idea behind statistical blockade is to bias the Monte Carlo analysis and block the simulations that will likely result in a circuit that is not extreme.
The method is applied to evaluate the test escape and yield loss resulting when an alternative oscillation-based test replaces the standard test used to measure the maximum attenuation in the pass band of a high-Q switched-capacitor band-pass filter (see Figure 3.1). The true values of test escape and yield loss are 64 PPM and 101 PPM, respectively. The method produces estimates that are very close, that is, 61 PPM for the test escape with a 95% confidence interval [25 PPM, 96 PPM] and 96 PPM for the yield loss with a 95% confidence interval [22 PPM, 166 PPM]. Figure 3.2 shows how the statistical blockade works. We first run a Monte Carlo simulation with a number of passes that we can afford and we create two sets, one containing circuits in the main lobe of the distribution (black circles in Figure 3.2(a)) and a second set containing extreme circuits (red filled circles in Figure 3.2(a)). Then we train a classifier to separate these sets in the space of design parameters. Subsequently, we generate circuit instances by sampling design parameters from their distribution defined in the design kit and the derived separation boundaries in Figure 3.2(a) are used to allow the simulation of instances (see Figure 3.2(b)) that are likely to be extreme.

3.1.2 Hierarchical test metrics estimation for complex circuits

Members: M. Dubois, H. Stratigopoulos, S. Mir

An expected way to reduce testing costs is the implementation of a test strategy during the design phase. However, the lack of methods for evaluating different testing techniques (BIST, DFT…) slows down the industrial implementation. In particular, parametric defect level and yield loss due to the BIST approach are never evaluated. In this work, we have proposed to evaluate test metrics of different BIST techniques for complex hard-to-simulate circuits by generating a large population of circuits described by their performances and corresponding test measurements. The methodology proposed follows six steps illustrated in Figure 3.3:

1. A few electrical MonteCarlo simulations of subcircuits that constitute the behavioral model are used for propagating the correlation of low-level process and design parameters to the behavioral space.
2. A joint probability density function (PDF) of the behavioral parameter space is estimated using a non-parametric law. This density characterizes the statistical distribution of each behavioural parameter and the dependencies between them.
3. An uniform sampling of the joint PDF is performed to obtain k samples (typically 10000) of the behavioural parameters, and each sample is simulated using an electrical behavioural level simulator.
We obtain this way $k$ samples of the output parameter space formed by the specified performances and test measurements of the overall CUT.

4. From the $k$ samples of the behavioural parameter space and the $k$ samples of the output parameter space we build a regression function using neural networks from the behavioural parameter space to each output parameter of the standard test and the DFT/BIST approach.

5. The joint PDF of the behavioural parameters is randomly sampled to obtain $N>>1$ million samples, and for each sample we use the regression functions to calculate the output parameters. Thus, we obtain this way $N$ samples of the output parameter space.

6. Test metrics are estimated from this large sample using relative frequencies. A good circuit has all performances within specifications whereas a bad one fails at least one of them. The test measures are evaluated with respect to their ability to discriminate between good and bad circuits. The test limits are fixed according to the test metrics such as yield loss and defect level.

Figure 3.3. Methodology for statistical evaluation of parametric test metrics for AMS/RF circuits

This technique is being demonstrated for the case of digital BIST techniques for a $\Sigma\Delta$ converter. The first part of the work has considered the reduction of the converter simulation time using a behavioural model in Simulink®. Thereafter, the generated population is used to compare the quality of the BIST techniques. Figure 3.3(a) shows the correlation of the open-loop gain and the unity frequency of the operational amplifier designed for the modulator under test while Figure 3.3(b) shows a test limit evaluation according to the test escape and yield loss of a BIST technique using a binary sequence as test stimulus. Future works are oriented to improve the BIST implementation in order to optimize test metrics.

Figure 3.3 (a) Openloop gain versus unity frequency of the operationnal amplifier distributions, (b) estimated yield loss and test escape as a function of test limits of the BIST technique

3.1.3 Analog diagnosis using machine-learning-based techniques

Members : K. Huang, H. Stratigopoulos and S. Mir

Accurate diagnostic methods of Integrated Circuits (ICs) are useful to (a) reduce design iterations in IC prototypes, (b) analyze the failure mechanisms from high-volume production data so as to enhance yield for future IC generations, and (c) identify the root-cause of failure in cases where the IC is part of a larger safety-critical system (e.g. automotive, aerospace) so as to improve safety features. Understanding the failure mechanism is necessary to construct a list of realistic faults for diagnosis purposes. In a production
environment, ICs can fail due to global multiple process deviations, such as poor temperature control, mask misalignments, etc. These deviations can be readily detected at wafer-level by supply current tests or by process control monitors in the scribe lines. Thus, global multiple deviations are typically not considered in the context of diagnosis. Another failure mechanism is local process variations that can lead to mismatch in critical device pairs and, thereby, to performance degradation. Such local process variations could be due to fabrication, but they can also be induced in the field due to aging phenomena or over-stressing. This type of defects is referred as parametric faults. The third failure mechanism is local spot defects. They can take forms of missing or extra materials and they are often modeled by open and short circuits. This type of defects is referred as catastrophic faults.

3.1.3.1 A unified catastrophic/parametric fault diagnosis approach based on machine learning

The proposed diagnosis flow is illustrated in Figure 3.4(a). We propose a unified catastrophic/parametric fault diagnosis approach based on an assemblage of learning machines that are trained beforehand to guide us through diagnosis decisions. The central learning machine is a defect filter that distinguishes failing devices due to catastrophic faults from failing devices due to parametric faults. Two types of diagnosis can be carried out according to the decision of the defect filter: catastrophic faults are diagnosed using a multi-class classifier, whereas parametric faults are diagnosed using inverse regression functions.

The defect filter relies on a non-parametric estimate \( \tilde{f}(m) \) of the joint probability density function \( f(m) \), where \( m \) is the diagnostic measurements vector. If \( \tilde{f}(m) = 0 \), the device is considered to contain a catastrophic fault. A multi-class classifier is used to diagnose this catastrophic fault. If \( \tilde{f}(m) > 0 \), the device is considered to contain a parametric fault. We then use nonlinear regression functions to predict parametric deviations.

The proposed approach is demonstrated on an RF Low Noise Amplifier (LNA) with a high diagnostic rate. Figure 3.4(a) shows the diagnosis flow. Figure 3.4(b) shows the projection of diagnostic measurements of devices with catastrophic faults (dots with different colours) and devices with parametric deviations (black
dots) in the top three principal components. Figure 3.4(c) shows two examples of prediction of parametric deviations in cases where the two parameters deviate ±40% from their nominal values.

3.1.3.2 Fault diagnosis based on non-parametric density estimation

According to several reports and anecdotal evidence, local spot defects represent the majority of defects that are met in production, in incoming inspection by costumers, and in the field of operation. Thus, we focus on local spot defects to build defect models.

We consider a non-idealized defect model by taking into account the impact of resistive behavior of defects. We consider non parametric kernel density estimation to model the likelihoods and defect probabilities, thus revoking the assumption of normal distributions. A high level description of the diagnosis flow is illustrated in Figure 3.5(a). Deriving likelihoods also allows us to analyze the misdiagnosed circuits and the resulting ambiguity groups. This is not possible using the standard fault dictionary approach since it provides a deterministic diagnosis decision. We first generate n defect locations $F_i$, $i = 1,...,n$ through a failure analysis. Then, we estimate the probability density function of resistance $r$ associated with each defect. This density is denoted by $p(R|F)$ and is fitted to data using non parametric kernel density estimation. Once the density $p(R|F)$ is estimated, we can sample it to generate N different scenarios for defect location $F_i$. In other words, we can generate N different “instances” of the defect $F_i$, i.e. N different combinations of resistive behaviors. These N defect instances are injected at the layout level during a post-layout Monte Carlo simulation to obtain the corresponding diagnostic measurements $m$.

During the Monte Carlo simulation, N instances of the circuit and the associated defect are sampled. This simulation includes process and mismatch deviations in the design and random values of the defect
parameters $r$. This way, we collect enough samples to estimate the likelihood $p(m|F)$. As before, this estimation is carried out using non parametric kernel density estimation. Once all likelihoods $p(m|F)$ are estimated, we can readily use them to diagnose the most probable defect that gave rise to a faulty DUT, given the pattern $m$.

The same case study as in Section 3.1.3.1 (shown in Figure 3.5(b)) is used to evaluate the proposed diagnosis flow using post-layout simulation. Figure 3.5(c) shows the layout of the LNA. Defects are injected at the layout level as shown in Figure 3.5(d). We are now applying the proposed approach to diagnose the faulty TJAJ1050 High speed CAN transceivers used in automobiles from our industrial partner NXP Netherlands.

3.1.4 Power control using parameter estimation

Members: R. Khereddine, E. Simeu, S. Mir, L. Abdallah and F. Cenni

An efficient management of energy consumption is of paramount importance for battery-operated wireless devices. The autonomy and life span of these devices directly depends on procedures aimed at saving energy. The total power consumption is largely determined by the radio frequency (RF) front-end, in particular the power amplifier (PA) and the low noise amplifier (LNA) that are found, respectively, in the transmission and reception paths. Achieving high energy efficiency for these components, while maintaining a high degree of linearity, has been a major issue in low power wireless communications from a hardware design standpoint. Energy savings can also be obtained using a software-based control. Most typically, energy hungry components are switched off during idle times.

This activity has studied further energy savings that can be obtained by considering different performance modes for each RF circuit and controlling the required power supply. Each performance mode of a Circuit Under Control (CUC) has a different power consumption associated with it. The sequence and time duration of performance modes must be scheduled by the underlying application or by demand from the communication network. The implementation of such an approach is not straightforward. A major challenge is to guarantee the performance level during each CUC mode by just controlling the power supply during all the operational life of the device. In fact, for each CUC, parameter variability, ageing mechanisms and operation disturbances can make difficult to guarantee the required performance level while only power supply is controlled.

Figure 3.6 presents the proposed closed loop logical control scheme to adjust the power consumption of an RF CUC according to the required performance mode. Since the CUC performances are not directly available for measurement, the controller must estimate them, regardless of the RF input and output signals of the CUC which are down-converted using embedded RF sensors. The control algorithm compares the estimated performances with the target performances of the desired mode, and acts accordingly on the CUC power supply. The controller takes as input the signals coming from embedded sensors placed at the CUC input and output. These signals are used in a recursive real-time parameter identification algorithm to extract the coefficients of an input/output behavioural model. Regression functions stored in the controller map the behavioural model coefficients to CUC performances.

The logical control is not intended to be permanently on. It is activated when the application sets a new performance mode for the CUC which requires a different CUC power supply. The control follows an iterative algorithm that starts with the CUC power supply set at the maximum value. During each iteration, the behavioural parameters ($\hat{\theta}$) are estimated by the LMS recursive algorithm and used by the regression equations to predict the CUC performances ($\hat{P}$). These are in turn compared with the specifications.
required by the new performance mode. If the specifications are met, the power supply of the CUC is reduced by a pre-defined value ($\Delta V_{dd}$) and a new iteration is considered. Otherwise, if the specifications are not met, the power supply is incremented by a value ($\Delta V_{dd}$) and the control stops.

The control technique has been evaluated for an RF LNA case-study that uses as an embedded sensor an envelope detector placed at its output. The CUC input stimulus is obtained by mixing a Gaussian signal with an average amplitude of 150mV, sampled at 10 MHz, with a carrier signal at 2.4 GHz. Figure 3.7 shows the accuracy of the identified behavioural model. Table 3.1 illustrates the evolution of the control algorithm. The target CUC mode is defined in the second raw of this Table. Each subsequent raw indicates the performances predicted and the reduction of CUC power consumption at each level of power supply voltage. The target performance mode is obtained with the power supply controlled at 2,301V, with a power consumption reduction of 54%.

![Figure 3.7. Accuracy of the identified behavioural model](image)

Table 3.1. Evolution of predicted performances

<table>
<thead>
<tr>
<th>Vdd (V)</th>
<th>Saved Power (%)</th>
<th>$N^C$</th>
<th>$S_{11}$</th>
<th>$S_{12}$</th>
<th>Gain</th>
<th>IIP1</th>
<th>IIP3</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1V</td>
<td>-14</td>
<td>1.70</td>
<td>-12.46</td>
<td>-43.65</td>
<td>10.41</td>
<td>-19.29</td>
<td>1.92</td>
</tr>
<tr>
<td>2.9V</td>
<td>-26</td>
<td>1.74</td>
<td>-12.30</td>
<td>-43.23</td>
<td>10.06</td>
<td>-17.09</td>
<td>1.06</td>
</tr>
<tr>
<td>2.7V</td>
<td>-38</td>
<td>1.99</td>
<td>-12.23</td>
<td>-42.99</td>
<td>8.97</td>
<td>-18.58</td>
<td>0.66</td>
</tr>
<tr>
<td>2.5V</td>
<td>-49</td>
<td>2.25</td>
<td>-11.96</td>
<td>-42.68</td>
<td>7.86</td>
<td>-19.70</td>
<td>0.39</td>
</tr>
<tr>
<td>2.3V</td>
<td>-54</td>
<td>2.39</td>
<td>-11.35</td>
<td>-42.90</td>
<td>7.16</td>
<td>-19.73</td>
<td>0.22</td>
</tr>
</tbody>
</table>

3.1.5 Test compaction using density estimation

Members: N. Akkouche, S. Mir, E. Simeu

Although the area occupied by analog circuits on a SoC typically ranges from 5% to 30%, the test cost for a mixed-signal SoC is higher than that for a digital SoC. It is approaching almost 40% of the total manufacturing cost. This is due to the capital cost associated with expensive mixed-signal automatic test equipment (ATE), as well as the high test times for analog cores. In the industry, analogue circuits are tested by explicit functional tests that measure directly the set of the circuit performances and compare them with their specifications, defined by the designer. Thus, the circuit is classified as functional if all the specifications are satisfied. Otherwise, it is faulty. This process is very expensive in terms of test time and equipment.

This activity studies an approach for ordering and elimination of analog specification (or functional) tests that is based on a statistical estimation of parametric defect level. A statistical model of $n$ specification tests is obtained by applying a density estimation technique to a small sample of data (obtained from the initial phase of production testing or through Monte-Carlo simulation of the design). The statistical model is next sampled to generate a large population of synthetic devices from which specification tests can be ordered according to their impact on defect level ($D$) by means of feature selection techniques. An optimal order can be obtained using the Branch and Bound method when $n$ is relatively low. However, for larger values of $n$, heuristic methods such as genetic algorithms and floating search must be used which do not guarantee an optimal order. Since the value of $n$ can reach several hundreds for advanced analog integrated devices, we have studied a heuristic algorithm (Figure 3.8) that considers combinations of subsets of the overall test set. These subsets are easier to model and to order and a heuristic approach is used to form an overall order.

This approach has been illustrated for the fully differential operational amplifier in Figure 3.9. Table 3.2 shows the tests considered and their statistical parameters. These tests approximately follow a multivariate normal distribution, that is, each test has a Gaussian distribution and all tests are linearly correlated. Table 3.3 illustrates the test order obtained by applying the algorithm of Figure 3.8. Since the size of the test set is relatively small (11 tests), the results are obtained without considered subsets (called the reference) and with subsets. The test order obtained in both cases is very similar, with very little impact on defect level when the order differs.

For production testing, it may then be possible to eliminate those tests that have the smallest impact on parametric defect level. However, devices with catastrophic defects are not considered in this analysis. These need to be filtered with a defect filter. For illustration purposes, we show in Table 3.4 the impact of analog test ordering for catastrophic fault coverage (FC) where a large set of catastrophic faults have been simulated.
In the future, we plan to address case-studies for which the multinormal model is not valid using parametric density estimation techniques, in particular the use of Copulas theory. The application to a case-study from IBM with 117 analog tests is targeted.

### Table 3.2. Parameters and specifications of the tests

<table>
<thead>
<tr>
<th>Test</th>
<th>μ</th>
<th>σ</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. A_D</td>
<td>76.60dB</td>
<td>0.493dB</td>
<td>74.53dB +∞</td>
</tr>
<tr>
<td>2. GBW_D</td>
<td>330MHz</td>
<td>18.14MHz</td>
<td>250.47MHz +∞</td>
</tr>
<tr>
<td>3. Phase Margin</td>
<td>63.33°</td>
<td>0.45°</td>
<td>61.34° +∞</td>
</tr>
<tr>
<td>4. CMRR (Gm0)</td>
<td>-42.76dB</td>
<td>1.02dB</td>
<td>-38.44dB +∞</td>
</tr>
<tr>
<td>5. PSRR (VDD)</td>
<td>-29.99dB</td>
<td>3.65dB</td>
<td>-14.78dB +∞</td>
</tr>
<tr>
<td>6. PSRR (Vmn)</td>
<td>-28.21dB</td>
<td>3.75dB</td>
<td>-12.56dB +∞</td>
</tr>
<tr>
<td>7. THD</td>
<td>66.19dB</td>
<td>2.38dB</td>
<td>55.07dB +∞</td>
</tr>
<tr>
<td>8. I_DD</td>
<td>2.48mA</td>
<td>0.21mA</td>
<td>3.5mA +∞</td>
</tr>
<tr>
<td>9. Intermodulation</td>
<td>67.57dB</td>
<td>1.09dB</td>
<td>62.35dB +∞</td>
</tr>
<tr>
<td>10. SR</td>
<td>73.14V/µs</td>
<td>5.55V/µs</td>
<td>45.37V/µs +∞</td>
</tr>
<tr>
<td>11. Noise</td>
<td>39.22µV</td>
<td>0.5µV</td>
<td>41.68µV +∞</td>
</tr>
</tbody>
</table>

### Table 3.3. Test ordering for the fully differential amplifier

<table>
<thead>
<tr>
<th>Test</th>
<th>Multinormal reference</th>
<th>Multinormal With subsets</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Order</th>
<th>Test</th>
<th>Multinormal reference</th>
<th>Multinormal With subsets</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>0.4</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2.4</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>9.8</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>16.8</td>
<td>0.4</td>
</tr>
<tr>
<td>6</td>
<td>9</td>
<td>24.4</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>11</td>
<td>32.7</td>
<td>0.2</td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>41.1</td>
<td>0.4</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>49.6</td>
<td>0.2</td>
</tr>
<tr>
<td>10</td>
<td>8</td>
<td>58.1</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>66.7</td>
<td>0</td>
</tr>
</tbody>
</table>

### Table 3.4. Catastrophic fault coverage of the ranking test

<table>
<thead>
<tr>
<th>Elimination order</th>
<th>Multinormal reference</th>
<th>Multinormal With subsets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>all tests</td>
<td>98.13</td>
</tr>
<tr>
<td>1</td>
<td>PSRR (Gm0)</td>
<td>98.13</td>
</tr>
<tr>
<td>2</td>
<td>GBW_D</td>
<td>98.13</td>
</tr>
<tr>
<td>3</td>
<td>CMRR</td>
<td>98.13</td>
</tr>
<tr>
<td>4</td>
<td>THD</td>
<td>98.13</td>
</tr>
<tr>
<td>5</td>
<td>PSRR (Vmn)</td>
<td>98.13</td>
</tr>
<tr>
<td>6</td>
<td>Intermodulation</td>
<td>97.5</td>
</tr>
<tr>
<td>7</td>
<td>Noise</td>
<td>97.5</td>
</tr>
<tr>
<td>8</td>
<td>Phase Margin</td>
<td>97.5</td>
</tr>
<tr>
<td>9</td>
<td>A_D</td>
<td>97.5</td>
</tr>
<tr>
<td>10</td>
<td>I_DD</td>
<td>93.75</td>
</tr>
<tr>
<td>11</td>
<td>SR</td>
<td>95.63</td>
</tr>
</tbody>
</table>

---

**Figure 3.8. Flowchart of the test ordering algorithm**

**Figure 3.9. Fully differential amplifier**
3.2 Design-for-test of AMS/RF circuits

3.2.1 ΣΔ converter BIST technique using a ternary stimulus

Members: M. Dubois, H. Stratigopoulos, S. Mir

The BIST technique aims at the measurement of the Signal-to-Noise and Distortion Ratio (SNDR) of a ΣΔ converter. In a preliminary step, the digital test stimulus is encoded by simulating an ideal ΣΔ modulator excited with an analog sinusoidal signal. Thereafter, the binary sequence is injected through a 1bit ADC directly at the input of the modulator under test. Previous work using this technique shows limitations such as a reduced input dynamic range testing and the lack of capability to detect harmonic distortions. Thus, an improvement of the test stimulus has been developed to tackle these problems.

The proposed solution is based on the sum of a N-length binary sequence \( b = \{b_0, b_1, ..., b_N\} \) with a delayed version of itself \( b_\delta = \{b_\delta, b_\delta + 1, ..., b_N + \delta, b_0, b_1, ..., b_{\delta - 1}\} \). According to the shift theorem, the power spectrum density \( B_\delta \) of \( b_\delta \) is equal to

\[
B_\delta(k) = B(k) \cdot e^{-j\frac{2\pi k \delta}{N}}, \quad f \text{ or } k, \delta = 0, 1, ..., N - 1,
\]

where \( B(k) \) is the power density of the initial binary sequence \( b \). The power spectral density of their sum is given by

\[
T(k) = B(k) \cdot \cos\left(\frac{\pi k \delta}{N}\right), \quad f \text{ or } k, \delta = 0, 1, ..., N - 1,
\]

This results in a ternary signal whose performances depend on the initial binary sequence and the delay \( \delta \). The main impact is a reduction of the test stimulus power which allows to enlarge the input dynamic range test of the modulator. Moreover, the amplitude \( A_T \) and phase \( \Phi_T \) of the signal encoded in the ternary sequence are related to the amplitude \( A_B \) and the phase \( \Phi_B \) of the binary counterpart according to

\[
A_T = A_B \cdot \cos\left(\frac{\pi \delta}{N}\right),
\]

\[
\Phi_T - \Phi_B = -\frac{\pi \delta}{N},
\]

Figure 3.10(a) shows the power spectral density of the binary and the ternary stimulus with their corresponding cumulative spectral power. The ternary test stimulus power is almost half of its binary counterpart for a delay equal to one. Figure 3.10(b) represents SNDR performance evaluation by performing behavioral simulations of the model of a modulator under test. The SNDR estimation starts to decrease at \(-10\)dBFS for the binary test signal while its value is still close to the reference until \(-6\)dBFS for the ternary test stimulus.

![Figure 3.10(a)](image-url-a)

![Figure 3.10(b)](image-url-b)

Figure 3.10. (a) Power spectral density of a binary and a ternary test stimulus, (b) SNDR simulation of a behavioral model excited with analog signal, binary and ternary digital tests.
The on-chip implementation of the ternary signal requires a few logic gates for implementing the sum of the two bit streams and the same register necessary to implement a binary test stimulus. The injection of the ternary signal for a differential modulator does not require any extra component compared to the binary implementation. Future work is aimed at validating this technique in a silicon prototype.

### 3.2.2 Sensors for machine-learning-based RF test

*Members: L. Abdallah, H. Stratigopoulos, S. Mir*

This work addresses the development of embedded sensors for RF devices aiming at reducing production test costs (i.e. tester instrumentation and test time) without sacrificing test quality. We propose a new type of non-intrusive sensors that are placed very close to the DUT, without being physically connected to it. The fundamental of the idea can be summarized as follows: each step in IC fabrication is subject to imperfections that in the long run result in variations in process parameters. Variations are categorized as inter-die (e.g. lot-to-lot, wafer-to-wafer, across the wafer variations) or intra-die (e.g. across the die). An analysis of these inter-die variations reveals each two neighboring structures within the die are similarly affected, implying that their parameters are likely to be highly correlated. However, this correlation can be corrupted due to intra-die variations, since such variations affect neighboring structures differently. For mature technologies, intra-die variations are very small compared to inter-die variations, thus their negative impact on the correlation can be minimized by taking layout precautions. Based on the above observations, we have experimented with some process sensors that we call dummy circuits and process control monitors.

For an RF LNA case-study, we have studied two types of dummy circuits, namely a typical bias circuit with a current mirror and MOS gain stages with different geometries. These particular dummy circuits offer a vectorless test: they are biased by a DC voltage generated on-chip and provide DC output voltages that correspond to different gain parameters. In addition, they incur a very small area overhead since they do not include layout-hungry inductors and capacitors. In addition, process control monitors (PCM) are basic layout components (e.g. capacitor, transistor) aimed at measuring directly a low level process parameter (e.g. capacitance per unit area, reverse saturation current for BJTs). We propose to include PCMs on the die with the aim to monitor variations across the DUT during production test. For our case-study, we have considered a metal-insulator-metal (MIM) capacitor that mimics the geometry and layout of a capacitor in the DUT. The MIM capacitor can be measured by using its I-V characteristic by connecting one conductive plate to ground and the other one to a capacitor.

The dummy circuits and the PCMs can detect large process variations but they cannot detect the presence of a random defect in the DUT since they do not tap into its signal path. So we have exploited other types of sensors that are related to the signal path. The simplest yet efficient way to monitor the DUT is through DC probes that can be set up by connecting a large resistor at a critical node, such that the current flow within the DUT is unaffected. Their main drawback is that they are unresponsive to variations related to L, C components. For this purpose, we have developed an envelope detector and a current sensor. The envelope detector is formed by two stages. The first stage is a half-wave rectifier of the current delivered at the input. Thereafter, this current is converted to voltage and low-pass filtered to the output in the second stage. Another possibility to extract RF signature, is to use a current sensor to extract a signature of the dynamic power supply current. Herein, we adapt the radiometric current sensor proposed in the literature which takes advantage of the small parasitic resistor of the line that connects the core of the DUT to the power supply pad. The output RF current of the sensor which is proportional to the RF power supply current is switched to the input of the envelope detector which outputs the RMS value of Imeas.

Figure 3.11 and Figure 3.12 illustrate the schematic and the layout of the chip including the LNA and the various sensors. It is realized using the 0.25-μm Qubic4+ process design kit provided by NXP Semiconductors.

In order to predict the performances of the LNA using regression functions, we use a set of 1000 LNA instances that we generate through a post-layout Monte Carlo simulation that considers global variations and mismatch. Out of the 1000 instances, 700 are used to train the regression functions and 300 are used to validate their generalization accuracy. Table 3.5 shows the errors in predicting the performances using different combination of sensors. Specially, the second line shows the errors when considering only the non-intrusive sensors which are acceptable. In addition, we have injected 23 catastrophic faults at the layout level. After injecting a catastrophic fault, we extract all the parasitics. Out of the 23 catastrophic faults, 17 are detected by the DC probes. The remaining 6 faults are detected by the envelope detector. Consequently, given the catastrophic fault model used, the current sensor is deemed unnecessary since all catastrophic faults are detected by the less-intrusive envelope detector (see Table 3.5). Finally, for the purpose of completeness, we assess the prediction accuracy using the four selected BIT structures. The result is shown in the last line of Table 3.6.
A device that passes successfully the manufacturing testing step might fail in the field during its normal operation. This could be due to electromagnetic interference, particle strikes in radiation intense environments, crosstalk, heat dissipation, thermal cycling, negative bias temperature instability (NBTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), etc. These phenomena are becoming more prominent as the channel length is reduced and as the density of integration is increased to include heterogeneous circuits on a single die. Thus, in cases where a device is part of a larger safety critical, mission-critical, and/or remote-controlled system, it needs to be self-testing, i.e. it needs to monitor itself and report errors that might occur. Self-testing can be performed on-line during idle times or in parallel with normal operation to enable concurrent error detection. Self-testing is key property of devices that are used in avionics, biomedical instrumentation, implanted chips, automotive, space applications, nuclear reactors, etc.

We envision a built-in self-test (BIST) architecture, as shown in Figure 3.13. In the self-test mode, the device under test (DUT) is connected to a test stimulus generator which enables a self-excitation of the DUT. A set of non-intrusive on-chip sensors is used to extract a DC measurement pattern which is thereafter presented to the neural network. The neural network maps this measurement pattern to an one-bit output, which indicates whether the measurement pattern is a valid or invalid code-word, that is, whether the DUT complies to its specifications or not. The training of the neural network is carried out off-line on a sample set of fabricated chips. The training phase results in an appropriate topology for the neural network and it also determines the weights of the internal synapses which are stored in a local memory. In the self-test mode, the weights are downloaded to the neural network.

### Table 3.5. LNA performances

<table>
<thead>
<tr>
<th></th>
<th>LNA alone</th>
<th>LNA with ED</th>
<th>LNA with BICS</th>
<th>Co-Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11</td>
<td>-13.5</td>
<td>+0.01</td>
<td>-0.09</td>
<td>+0.1</td>
</tr>
<tr>
<td>S12</td>
<td>-42.4</td>
<td>-0.02</td>
<td>+0.7</td>
<td>+0.6</td>
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<tr>
<td>S21</td>
<td>11.9</td>
<td>+0.02</td>
<td>-2.18</td>
<td>-0.07</td>
</tr>
<tr>
<td>S22</td>
<td>-8.9</td>
<td>-0.25</td>
<td>-8.8</td>
<td>-0.4</td>
</tr>
<tr>
<td>NF</td>
<td>1.5</td>
<td>0.1</td>
<td>+0.27</td>
<td>+0.07</td>
</tr>
<tr>
<td>IIP1</td>
<td>-11</td>
<td>-0.21</td>
<td>-1</td>
<td>+0.01</td>
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<tr>
<td>IIP3</td>
<td>5.9</td>
<td>+0.2</td>
<td>-0.5</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

### Table 3.6. RMS prediction errors (%)

<table>
<thead>
<tr>
<th></th>
<th>S11</th>
<th>S12</th>
<th>S21</th>
<th>S22</th>
<th>NF</th>
<th>IdB</th>
<th>CP</th>
<th>IIP 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALL BIT</td>
<td>1.3</td>
<td>0.4</td>
<td>0.7</td>
<td>2.9</td>
<td>1.2</td>
<td>1.4</td>
<td>3.1</td>
<td></td>
</tr>
<tr>
<td>Dummy PCM</td>
<td>1.7</td>
<td>0.4</td>
<td>0.9</td>
<td>3.3</td>
<td>2</td>
<td>1.8</td>
<td>3.4</td>
<td></td>
</tr>
<tr>
<td>Dummy PCM, ED DCprobe</td>
<td>1.4</td>
<td>0.4</td>
<td>0.8</td>
<td>3.1</td>
<td>1.7</td>
<td>1.6</td>
<td>3.2</td>
<td></td>
</tr>
</tbody>
</table>

3.2.3 Neuromorphic BIST

*Members: D. Maliuk*, H. Stratigopoulos, H. Huang*, Y. Makris*

(*Yale University, USA*)
In this work, we have designed and fabricated a neural network as a single chip (see Figure 3.14) using a 0.5 µm digital CMOS process available through MOSIS. We have chosen an analog implementation since, compared to its digital counterpart, it has superior time response and computational density in terms of silicon mm² per operations per second and, in addition, it consumes extremely low power. The neural network is fully configurable with 10 neurons and 100 synapses, which allows us to study various topologies that can implement classification boundaries of increased non-linearity.

The chip is put to the test to learn to classify RF low noise amplifier (LNA) instances based on a measurement pattern which is obtained by exercising the RF LNA with two single-tone sinusoidal stimuli of different powers and by recording the outputs of two amplitude (or power) detectors placed at the input and output ports of the RF LNA. To train the chip, we have used simulation data enhanced with synthetic data in order to create an overall information-rich training data set. We use a chip-in-the-loop training approach based on the parallel weight perturbation with simulation annealing algorithm. An arbitrarily large set of synthetic devices is also used as a validation set to assess classification rate of the trained neural network with PPM accuracy.

We have demonstrated that the hardware classifier achieves similar classification rates to its ideal software counterpart.

3.2.4. Pipeline converter test evaluation

Members: A. Laraba, M. Dubois, C. Forel, H. Stratigopoulos, S. Mir, H. Naudet*  
(*ST Microelectronics, HED, Grenoble)

In production testing, ADCs are tested for static and dynamic performance. Dynamic test consists in applying a sinusoidal signal and analyzing the Fourier Transform, whilst the static performances are obtained by applying a ramp or a slow sinusoidal signal to the ADC and using the histogram method, which requires the collection of a very important volume of data. With the increasing resolution of converters, the static test time is increasing exponentially, and is becoming excessive regarding the area of silicon that is being tested or the test time of the other parts of the circuit. This forces the test engineers to reduce the test time at the expense of a lower precision, which generates test instabilities which could lead up to rejecting good circuits (yield loss) or accepting bad ones (test escape).

Many alternative test/calibration techniques are proposed in the literature, but most of them are not actually used in an industrial context. One of the reasons is that the economic loss due to the test errors would be more important than the cost reduction made possible by the new test technique. That is why the evaluation of the test metrics at the design stage is important before implementing an alternative test method. Test metrics are generally estimated with parts-per-million accuracy. In order to obtain such a precision, a large sample of circuits needs to be generated, which would take a very long time, especially for complex circuits like ADCs.

In this activity, we are using the test metrics estimation methodology described in Section 3.1.2 for the evaluation of test techniques for pipeline ADCs. This methodology allows the generation of a large sample of circuits within a reasonable time for complex hard-to-simulate circuits. We have started the evaluation of a test method proposed in the literature that consists in measuring only some specific codes of the transfer characteristic of the ADC. These codes reflect the static behavior of the whole converter, so that the linearity performance is estimated within a very reduced test time compared to the traditional linearity testing with the histogram method.
The technique has been evaluated on an industrial ADC design of STMicroelectronics. The blocks of the ADC have been simulated at the transistor level to extract the statistical distribution of the behavioral parameters of the converter (~1000 Monte Carlo instances). In the next step of the evaluation flow, regression functions have been built using a sample of behavioral level circuits (~5000 instances) that have been simulated using Matlab. These functions have next been used to generate a random sample of 1 million circuits that has been used to compare the static parameters (Differential Non Linearity and Integral Non Linearity) obtained by the new test method against the ones obtained by the classic histogram method. These results are shown in Figure 3.15. The biggest errors in the estimation of INL and DNL occur when the circuit under test presents large values of DNL and INL. We are currently analyzing the eventual causes of these errors in the estimation of INL and DNL.

![Simulation results of the estimation of DNL and INL for a sample of 4900 pipeline ADCs](image)

**Figure 3.15.** Simulation results of the estimation of DNL and INL for a sample of 4900 pipeline ADCs

### 3.3 Modeling with SystemC-AMS and control

#### 3.3.1 CMOS image sensor modeling with SystemC-AMS

**Members: F. Cenni*, S. Scotti*, E. Simeu**  
*(ST Microelectronics & TIMA, * ST Microelectronics, Grenoble 2 SAS)*

The market of embedded electronics has shown a sharp increase in the complexity of the systems provided. The validation of the overall functioning of these systems is crucial as such needs to be performed as soon as possible during the design flow by means of simulations. That is why, in general terms, a validation through simulations of virtual prototypes of complex systems shrink time-to-market by anticipating many phases of the design-to-market flow. Notably, these phases are architecture exploration, early validation of the overall specifications, embedded software development and bug-fixing.

An image acquisition system is typically composed by three main blocks: an image sensor followed by an image signal processor (ISP), the whole controlled by a central processing unit (CPU). This work focuses on the development of a reliable and accurate model of a ST Microelectronics image sensor with the purpose to simulate its functioning within its surrounding environment. Nowadays, the stand-alone ISP algorithms are normally tested in the development phase by means of images sets issued by a real sensor. Since the ISP must also be able to control the sensor parameters, the interoperability between sensor and ISP is normally checked by connecting a board with the sensor chip and the ISP implemented on FPGA to the PC-hosted instruction set simulator (ISS) of the target CPU through an interface board. A SystemC-AMS/SystemC-TLM
virtual prototype of the overall system is being developed with the purpose to avoid, at early design stages, the use of boards for a first validation of the system. This would also allow validating the ISP algorithms at simulation-level by tuning them and stressing them up to determine their limit working conditions.

With respect to an image sensor, many physical domains are concerned. Analogue and digital electrical signals are involved together with analogue optical values. SystemC-AMS is an analog and mixed signal (AMS) extension of the SystemC framework, both C++ based libraries, that aims at creating a complete design environment for the modeling and simulation of heterogeneous systems at a high level of abstraction.

The SystemC-AMS framework has been chosen in order to model and simulate the heterogeneity of physical domains concerned here. The timed data flow (TDF) model of computation (MoC) has been used. The model takes into account the distortion of the light’s angle of incidence due to the lens effect, the Bayer filter adsorption effect, the electronic rolling shutter (ERS) effect, a linear discharge of the photodiodes, hot pixels effect and the controllable integration time. The SystemC-AMS model of the video sensor is integrated in a SystemC-TLM 2.0 proof-of-concept platform (Figure 3.16) by wrapping it in a SystemC-TLM module with an initiator socket for the transmission of the video stream and a target socket for controlling its parameters (e.g. integration time). The platform also contains a SystemC-TLM simple model of the ISP that provides the output image by means of an interpolation. It also estimates the light of the output image and decides whether the control parameters of the sensor have to be updated or not (e.g. integration time for the auto-exposure feature). Both the input and output images are sent to the comparator unit.

Future works will enrich the SystemC-AMS model of the sensor with other non-idealities such as the dark signal non-uniformity (DSNU) and the photo response non-uniformity (PRNU).

**Figure 3.16.** SystemC-TLM platform and intermediate images: synthesized input image, Bayer image output by the sensor, output image recovered by the ISP and the comparison image calculated through equation and legend on the bottom right

### 3.3.2 Power consumption modelling at system level

**Members:** L. Bousquet, E. Simeu, F. Cenni*, L. Fesquet*, K. Morin-Allory*

*ST Microelectronics & TIMA, "Group CIS, "Group VDS"

The market of embedded electronics has shown a sharp increase in the complexity of the systems provided. The equipment that these systems integrate offers more and more features. This constant growth of complexity and diversity of applications lead designers to integrate components of different physical natures on a single chip. Thus, systems become multiprocessors, and also heterogeneous, the digital and analog functions are mixed. SystemC-AMS is an analog and mixed signal (AMS) extension of the SystemC framework, both C++ based libraries, that aims at creating a complete design environment for the modeling and simulation of heterogeneous systems at a high level of abstraction. The extension of SystemC with SystemC-AMS provides a complete environment for fast simulation of the heterogeneous systems at the architectural level. This helps to dimension the digital and AMS resources required and to validate the architectural choices. **Figure 3.17** illustrates the place of SystemC-AMS in the mixed design flow. SystemC-AMS provides three Models of Computation (MoC): TDF (sampled) and LSF (continuous) are high level MoCs whereas ELN is a low level MoC that works with predefined analog components instantiations.
Providing information on global power consumption during the architectural level simulation is becoming a decisive advantage for system designers who would like to have an estimation of the consumption of each part of a system early in the design process. Unfortunately, information on energy consumption of AMS and RF blocks is only available at lower level after the implementation choices have been made.

With this goal in mind, we are developing a method that can be used to automatically extract relevant power consumption information from a low-level description (netlist or ELN) of a linear circuit, and to integrate this information in the high level model so that it is propagated during simulation. Thus, during each simulation cycle, it will be possible to extract the supply electric currents associated with each component of the system and to use the result in order to estimate the power consumption of the overall system. The first step starts from a block transfer function (high level) and refines it in order to build the electrical circuit (low level) corresponding to a given implementation solution candidate. This part has not been studied, since existing analog refinement tools can be used in this step. Our work focuses on the reverse step that consists on finding automatically the state space representation of the electrical circuit. The output vector of the state space representation can contain the input current. Once the input current is known, the multiplication with the voltage input is enough to obtain the instantaneous power consumption.

Figure 3.18 shows two different implementations of a given transfer function. The input currents of these circuits have been computed using our automatic state space extraction method. The result shows two different levels of power consumption.

Ultra Wide Band (UWB) has emerged as a promising technique for indoor wireless communications, localization applications, sensor network, etc…The advantage of UWB lies in many valuable properties: low power consumption and low circuit cost, good time resolution, spectrum compatibility with existing narrowband systems, rich multipath diversity, enhanced penetration capability and high user-capacity. However, timing synchronization is one of the critical issues in UWB system. That is because UWB system has a dense multipath channel, and its pulses are narrow (typically at nanosecond scale) with low power
density under the noise floor. Therefore, the objective of our work is to maintain the satisfactory synchronization and tracking between the received signal \( r(t) \) and the generated reference signal \( y(t) \) (by minimizing the timing offset error). We have used the delay locked loop (DLL) technique, shown in Figure 3.19, for tracking purpose and for estimating the offset time \( \tau \) between the received and reference signal and compensate it by shifting the reference signal position, to \( y(t - \hat{\tau}) \) where \( \hat{\tau} \) denotes the DLL estimate of \( \tau \).

The tracking output error \( e \) depends on the offset time \( \tau \). It plays the role of a correction signal which is then used to drive the offset decision block and to generate the compensation parameter \( \hat{\tau} \). The output error \( e \) may be expressed by:

\[
e(\tau) = S(\tau) + N_{\text{DLL}} + \epsilon = \tau - \hat{\tau}
\]

where \( S(\tau) \) is the loop discriminator (S-curve) characteristic and \( N_{\text{DLL}} \) is the equivalent additive noise. A simplified model of the DLL tracking system could be approximated by the equivalent diagram shown in Figure 3.20(a).

![Delay-Locked Loop Diagram](image)

**Figure 3.19.** Delay-Locked Loop Diagram

Our aim in this work is to design a fit offset decision which is used to adjust and update the current estimate of offset time \( \hat{\tau} \). We have employed a novel control strategy in the communication domain, called Internal Model Control (IMC) method. The IMC structure consists of two blocks: the first (Model Block) should match perfectly the tracking system and the second (Control Block) represents the inverse model of the system. Figure 3.20(b) illustrates the equivalent DLL tracking diagram including the IMC regulation loop. We evaluate the performance of the modified DLL tracking with Matlab simulations. Figures 3.21(a) & (b) show the estimated offset time \( \hat{\tau} \) (solid line) for SNR=3 dB. The time offset \( \tau \) (dashed line) in Figure 3.21(a) is constant, but it increases in Figure 3.21(b) linearly with the time (Doppler Effect). The system model and control are empirically estimated using an identification process. Sufficient accuracy was obtained for a polynomial model of order 3 with a determination coefficient \( R^2 \) high enough (\( R^2>99 \)). The Least-Squares estimation algorithm method is applied for seeking the optimal function coefficients for the model and the control block. Table 3.7 and Table 3.8 show the structure and the coefficients for the model & control blocks, the identification performance ( \( R^2 \)), and the tracking performance. We observe that the tracking performance using our approach is slightly degraded with the presence of the Doppler Effect. Therefore, the perspective of our research study is to improve the estimation accuracy by modifying the IMC structure, using an adaptive control loop.
3.4 Design of Microsystems

3.4.1 Polymer-based MEMS sensors for ORL surgery

(*Institut Jean Lamour, Univ. Henri Poincaré Nancy, **LMOPS, Univ. de Savoie, Chambéry, ***CHU Grenoble)

In this project we aim at the development of a micromachined vibration sensor working in the audible frequency range from 1 to 5 kHz to be used during an ORL (Oto-Rhino-Laryngology) surgery. The sensor will give the surgeon feed-back concerning consequences of his intervention on the middle ear acoustic transmission properties by measuring the amplitude of vibration of ossicles constituting the transmission chain. Since vibration amplitudes and mechanical impedances of ossicles are very low (vibrations from 10 to 100nm, impedances lower than 1Nsm⁻¹), high sensitivity and low mechanical impedance are required to the sensor. An ergonomic probe containing the sensor, held by surgeon’s hand, thus allowing precise and easy positioning on small ossicles (millimeter scale) will be a result of the project.

A MEMS based vibration sensor is convenient for the task especially due to the small size of the ear ossicles. The sensor is composed of an elastic pillar which tip is placed in contact with the vibrating ossicle to transmit vibrations to a suspended base composed of a circular membrane. Membrane deformation will be converted into electrical signal by means of planar capacitive strain gauges (Figure 3.22(a)) providing information on the pillar tip vibration magnitude. Silicon is too stiff and brittle to satisfy both low displacement and low impedance requirements and to withstand imprlicable hand movements. Polymer materials which became widely used in MEMS field, due to interesting mechanical and electrical properties are considered for this project. For example, a SU-8 negative resin has been chosen to realize the sensor membrane because of its good mechanical properties. The SU-8 confers good rigidity and high failure strain to the membrane, allowing high frequency resonance and robustness to the sensor.

With the introduction of an electroactive polymer such as PVDF-TrFE the sensitivity of gauges to a mechanical strain will be increased while keeping high structure compliance. With this approach, the presence of gauges will not disturb the sensor mechanical behavior and the modeling and the design process will become easier. Analytical modeling of the pillar tip has proven that the introduction of an elastomer material which presents glass transition behavior in the low frequency range (~100Hz) could improve sensor robustness. Such a material could avoid the device saturation that can occur if a high magnitude of hand shaking movements (~100µm) is superposed to the measurement signal.

A complete modeling of the sensor mechanical behavior and an optimization study of its design has been realized. SU-8 membranes have already been realized. PDMS pillars have been realized by a molding technique (Figure 3.22(b)) We are currently optimizing in order to extend it to epoxy resins. Gauges integration would soon result from an in-progress collaboration work with the Institut Jean Lamour from Nancy in order to obtain high quality PVDF-TrFE layers with a thickness inferior to 10 microns. In collaboration with the LMOPS laboratory from Chambéry an intensive selection work of the pillar material has been done and a characterization of the acoustic properties on the material samples will be carried out.

<table>
<thead>
<tr>
<th>Table 3.7. The control and system model for the IMC loop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model $\dot{z} = 3.5 \cdot \dot{z} - 1.1 \cdot \dot{z}^3$  &amp; $R^2 = 1$</td>
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<td>Control $\dot{z} = 0.2 \cdot E + 0.02 \cdot E^3$           &amp; $R^2 = 0.998$</td>
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<table>
<thead>
<tr>
<th>Table 3.8. The tracking performance</th>
</tr>
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<tr>
<td>Without Doppler effect $\tau = 0.6$ &amp; With Doppler effect $\tau = 0.1 + 0.01 \cdot t$</td>
</tr>
<tr>
<td>estimation of the error variance 0.0027 &amp; 0.096</td>
</tr>
</tbody>
</table>

Figure 3.21 (a) Evolution of the Modified DLL Tracking without Doppler effect ($\tau = 0.6$), and (b) evolution of the Modified DLL Tracking with Doppler Effect $\tau = 0.1 + 0.01 \cdot t$
3.4.2. GaN-based piezoelectric sensors

*Members: L. Rufer, S. Vittoz, T. Lalinsky*

(* Slovak Academy of Sciences, Institute of Electrical Engineering, Bratislava, Slovak Republic)

Gallium nitride (GaN) is known as a wide band gap semiconductor used mainly in optoelectronics but it is also a good piezoelectric material with high stiffness coefficients. As such, GaN and III-V nitrides (III-N) materials as a whole are of great interest in the field of sensors. From gas to radiation sensors, this material is particularly well studied. III-N materials have also great chemical and thermal stability enabling applications in chemical sensors and biosensors.

Harsh environments are defined by high temperature (> 600°C) and high pressure (> 10 atm) and especially corrosive atmosphere. The particular properties of III-N materials made them good candidates for applications in such environments, where silicon based electronics cannot function properly. For instance, AlGaN/GaN based High Electron Mobility Transistors (HEMT) operate up to 750°C. By coupling such electronic devices with cantilevers constituted of III-N heterostructures, mechanical sensing structure can be obtained to monitor parameters such as pressure, strain or acceleration in harsh environments.

The aim of the project is to accomplish detailed modeling of electrical and mechanical behavior of different structures used for pressure for harsh environment. Electro-mechanical behavior of different layers composing these structures will be simulated in order to predict basic features of these sensors. Piezoelectric effects in these structures will be studied. The modeling will be based on the Finite Element Analysis and on an analytical approach.

This work is done in the frame of the European project MORGaN (Materials for Robust Gallium Nitride). The detailed analysis of GaN structures as cantilevers and membranes fabricated with different technologies by other partners of the project will be done. At this stage, we are studying a cantilever structure made of a III-N materials multilayer. This cantilever is coupled with a high mobility transistor (HEMT) that is obtained by epitaxial growth of III-V nitride alloy (AlGaN) on the GaN layer (see Figure 3.23(a)). The same principle has been used to fabricate a membrane sensing structure based on III-N multilayer stack grown on a sapphire substrate (see Figure 3.23(b)).

The sensing principle of this structure is based on the variation of the electrical behavior of the transistor due to a mechanical load. The mechanical load exerted at the free end of the cantilever or by the pressure on the AlGaN/GaN membrane creates a mechanical stress in the structure that affects the piezoelectric surface charge density at the AlGaN/GaN interface (or interface resulting polarization). Simultaneously, it will modify the threshold voltage of the HEMT.

Analytical and numerical modeling of the mechanically-induced polarization have been established for the cantilever structure. The subsequent coupled-physics modeling of the sensing HEMT is ongoing. The model of the membrane-based sensor is based on the same principle as the cantilever-based sensors and is already underway. Test chips of the membrane based sensors have been obtained thanks to the MORGaN project. Test and characterization of these structures is shared with partners and is currently in progress.
3.4.3 High frequency aeroacoustic sensor

*a*a

Aero-acoustics, a branch of acoustics which studies noise generation via either turbulent fluid motion or aerodynamic forces interacting with surfaces, is a growing area and has received fresh emphasis due to advances in air, ground and space transportation. Compared with all other working principles, due to its simple fabrication process, measurement circuit, packaging issues and application requirements, piezoresistive type microphones are well suited for aero-acoustic measurements.

Single-crystalline silicon (sc-Si) has larger gauge factor than poly-crystalline silicon (poly-Si), which is a suitable material property for piezoresistive sensing elements. Recently, some kinds of sc-Si based aero-acoustic microphone were demonstrated by using bonding technology to form a sc-Si layer on an amorphous dielectric layer. These devices demonstrated a good acoustic performance due to using high gauge factor material and a good electrical performance due to the dielectric diaphragm electrical isolating property. However, the bonding technology involved in the fabrication process either requires chemical mechanical polishing (CMP) before bonding or etching back process after bonding. All these increase the cost and prevent the real commercialization.

A piezoresistive aero-acoustic microphone with four-corner-supported diaphragm is demonstrated here. A 0.1µm thick thermal oxide mask layer is grown on a (100) P-type silicon wafer. After photolithography, oxide layer is removed by buffered oxide etchant (BOE) and bulk silicon is etched by TMAH solution to form the dimple shape. After stripping the first oxide mask layer, thermal oxide/amorphous silicon two sacrificial layer system are grown and deposited with the thickness of 0.3µm and 0.1µm, respectively. The second photolithography and etching process is used to define the diaphragm area. Then, the first 0.15µm thick low stress silicon nitride (SiN) layer is deposited. Sensing piezoresistors are placed on the diaphragm supporting cantilever beam and formed by the re-crystallized metal-induced-lateral-crystallization (RC-MILC) poly-Si. Reference resistors are placed outside the diaphragm and the resistor value will keep constant during the working period. After piezoresistor doping, the second 0.15µm thick low stress SiN layer is deposited to protect sensing resistor during wet etching in the later step. After etching hole opening and metal contact hole opening, the Cr/Au metal line is formed by lift-off process with the thickness of 50nm and 1µm, respectively. Finally, the diaphragm is released by a 60°C TMAH/BOE/room temperature TMAH etching sequence.

The successfully fabricated aero-acoustic microphone is shown in Figure 3.24. The major advantages of this technology are: 1) simple fabrication process with poly-Si; 2) poly-Si gauge factor increased by RC-MILC technique; 3) the cavity is opened in the front side with three etching sequences which reduces the device size compared with backside etching technique and makes the cavity depth independent with the diaphragm area; 4) the dimple structure on the diaphragm prevent stiction even when the cavity depth is around 5µm with the diaphragm area of 500µm×500µm.

The preliminary microphone characterization was carried out. The static responses of different diaphragm dimensions were obtained by nano-indentation with HP4155A semiconductor parameter analyzer (Figure 3.25). The resonant frequency of 100µm diaphragm was 580 kHz, which is measured by laser vibrometer (Figure 3.26).
3.4.4 CMOS-MEMS technology for acoustics and ultrasonics

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Recently, different works showing the feasibility of MEMS using CMOS technology followed by surface micromachining without mask have been published. Unlike the older approach where suspended MEMS components were obtained by silicon substrate etching, the proposed technology consists in etching oxide layers resulting from the CMOS process and thus releasing metallic layers of the same CMOS technology. Works based on standard CMOS 0.35 µm processes using AMS or TSMC foundries available in the literature do not give information concerning either the mechanical properties of materials or the design rules which are essential for the microsystem conception.

This project is divided into two parts. In the first part, it will be necessary to develop a technological process: determine the etching type, etching time, as well as the feasible extreme dimensions for simple structures in CMOS technology. The second part of the work will be dedicated to the validation of the CMOS-MEMS process by the development of MEMS acoustics devices. Two different sorts of devices will be considered:

- Capacitive microphone
- Capacitive micromachined ultrasonic transducer (CMUT) for biomedical applications. This transducer will be of use to diagnosis and medical imaging in places difficult to access by traditional instruments.

The electronic circuits for the signal processing (preamp, ADC…) and these MEMS devices will be integrated on the same chip for better performances and to decrease noise.

At this stage, we have developed a model for the MEMS capacitive microphone with lumped-parameters as shown in Figure 3.27(a). Finite Element Analysis, with CoventorWare, helps us too in the microphone modeling. A layout, with the AMS CMOS 0.35 µm process, has been sent for microphones fabrication. MEMS structures like cantilever, bridges, and membranes have been fabricated thanks to the vapor phase fluoridric acid (HF) etching as shown in Figure 3.27(b). The next step is the characterization of the MEMS capacitive microphone.

![Figure 3.24. Plan-view optical micrograph of a fabricated sensor](image)

![Figure 3.25. Static sensor response with different diaphragm dimensions](image)

![Figure 3.26. Resonant frequency measurement](image)

![Figure 3.27. (a) Microphone structure with his equivalent circuit and (b) bridges fabricated using AMS CMOS 0.35 µm technology](image)
4. System Level Synthesis (SLS)

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4.1 Main trend for embedded systems design: Multiprocessor SoC

We define an embedded computing system as an application specific electronic subsystem used in a larger device such as an appliance, an instrument or a vehicle. The embedded system functions of digital electronics are usually realized using both software running on CPUs and specialized hardware accelerators. The evolution of technologies is enabling the integration of complex hardware platforms in a single chip: called System-on-Chip, SoC. Modern SoC may include one or several CPU subsystems to execute software and sophisticated interconnect in addition to specific hardware accelerators.

Mastering the design of these high programmable and parallel embedded systems is a technical and scientific challenge. It requires new design methods, new design tools, new system modeling strategies to allow for concurrent hardware and software design.

100% of new ASICs include several CPU in 65nm technology. Mobile and Multimedia platforms are multi-processor system on chip (SoC) using different kinds of programmable processors (e.g. DSPs and microcontrollers). Heterogeneous cores are exploited to meet the tight performance and cost constraints. Tomorrow's SoCs are composed of multiple, possibly highly parallel, processors for applications such as mobile terminals, set top boxes, gaming consoles, graphic cards, and network processors. Moreover, these chips contain sophisticated communication networks-on-chips (NoC) to sustain the ever increasing bandwidth requirements. So mastering a huge task level parallelism is the next SoC design challenge. As a result, design methodologies must change their focus to the selection, specialization and usage of processors—either programmable or dedicated—as basic components rather than the logic modules. Compared with conventional ASIC design, such a multi-processor SoC is a fundamental change in chip design.

The SLS group is working on both hardware and software architectures for MPSoC systems, and therefore develops CAD tools and methods. This includes low level software to efficiently support the applications, and eases the reuse of legacy code on these complex architectures. Regarding architectures we take benefit from the integration, both because technological evolution, such as 3D integration, or because the number of transistors becomes huge (1.6M Transistors per 1mm² in 45 nm technology).
4.2 Methods and tools for computer aided design


The CAD activities mainly cover the following themes: Modeling, Simulation and Debug and Profiling. Simulation of large scale integrated, potentially heterogeneous, multiprocessor platforms is a long lasting theme of the SLS group. This work is of primary necessity as the number of processors in integrated circuits is rising, and therefore the simulation times are increasing constantly. As a result, the execution of the software on Instruction Set Simulators during simulation (making the processor the ultimate hardware/software interface) is not viable anymore. Several innovative approaches have been defined and demonstrated, and the years 2008-2010 have been particularly fruitful on this topic.

4.2.1 Native simulation strategies

For several years, the so called native simulation approach has been seen as the implementation of the low level software functions of an Operating System using a simulator API. This has become specifically popular with the wide dissemination of SystemC, as it provides many API functions similar to the ones of an OS. The idea is thus to model the system as a stack of layers, and each upper layer can rely on the functions provided by the lower level layers. If the abstraction is coarse, then several layers can be merged to provide at a low execution cost the functions (usually realized on top of an operating system or a high level hardware abstraction such as SystemC TLM), if the abstraction is fine grain, then the “real” realization (some OS code for example) is provided, and the hardware can be described more accurately at the cycle level. One of the abstractions that can be made is illustrated on Figure 4.1. The leftmost part of the figure represents an abstract view of a platform, then details the CPU subsystem that contains one or several CPUs but that share the same operating system (SMP) and software layers. Finally, the hardware view of the subsystem is abstracted.

Figure 4.1 Software stack representation

The modeling approach is mainly useful for simulating systems at different levels of abstraction. Going high into the abstraction can lead to purely functional information. Addresses may even be hidden behind programming level constructs such as array or variable definitions. However, these approaches have the clear drawback that it is impossible to model operations as frequent and as simple as the copy of data from a hardware IP into a software allocated buffer, because the software buffer is allocated into the Unix process in which SystemC runs, whereas the hardware IP addresses are relative to the target platform. This clearly means that the usage of these approaches is intrinsically limited to trivial platforms. Our main contribution in native simulation has been to define an approach that allows to simulate a multiprocessor system (whose software enforce the use of the HAL API) using the host machine instead of interpreting the instructions. Figure 4.2 illustrates the approach that relies on the use of the memory of the simulator (in the Unix process) as the memory of the simulated system. This allows avoiding remapping techniques that are not able to handle some situations at the price of a strict adherence to an API (that is very often necessary for porting matters but that may not be used in legacy codes). In order to provide estimations of the execution time, an LLVM based framework is being developed to generate “host code” based on the exact “cross-compiled” code to provide additional information at run time. This approach is however not perfect, as it requires to adhere strictly to a HAL, and to modify the target platform IP's. This first
step was a necessity to understand the problem, but this solution only goes half-way. A new approach has been researched, and the work on that topic is still ongoing.

4.2.2 Dynamic Binary Translation (DBT) based simulation strategies

As far as processor simulation is concerned, the use of dynamic recompilation techniques is very promising from a speed perspective. However, these techniques do not currently provide accurate speed and/or power estimates of the code execution, because the approach “forgets” the original code inherently. Also, the so-called “emulators” are currently fully integrated with their environments, and do not provide the level of modularity that is necessary in the SoC domain. Therefore, we have worked on integrating a DBT engine (QEMU) into SystemC. This has required the definition of a lightweight addition of timing (and/or power) information during dynamic translation, at the basic-block level, as the main issue here is the correct synchronization and time advance between the event-driven simulator and the DBT engine. This also leads to the definition of cache modeling strategies that happened to be quite efficient and accurate. The principle of Dynamic Binary Translation is shown in Figure 4.2. Our contribution has been to generate not only functional calls, but also call allowing to first synchronize with the event driven simulator and second to advance the time.

![Figure 4.2 Dynamic binary translation principle](image)

In order to further increase the speed of simulation for multimedia applications, we have defined an intermediate representation that takes into account SIMD extension, in order to be able to execute target SIMD instructions while benefiting from host SIMD instructions. Using this simple yet innovative approach, we have shown a clear speedup on synthetic benchmarks.

4.2.3 Debug and Profiling

We started an activity in debugging by looking at the bugs in concurrent programs running on simulation platforms to ensure first non-intrusiveness and second potential access to all the resources. Profiling benefits from the same infrastructure, with the goal of automatically detecting hot spots from the traces, and pointing out the sources of the hot spots. This work relies on a trace generation infrastructure suited for virtual prototypes, that requires minimal modifications of the models for tracing but changes neither the model behavior nor its timing.

Multiprocessor debug shall not be considered like “usual” debug, i.e. launching a debug process per actual process to follow the flow of computation. As there may be hundreds of cooperating processes, the real problem is to identify wrong data sharing, race conditions and inappropriate understanding of the consistency issues. A formal approach to these issues would be ideal, but unfortunately it is clearly not possible to handle actual programs with these techniques. So we choose a more practical approach in which we analyze execution traces.

Concerning race conditions, as the traces are obtained per processor, they are first reassembled in order to produce a trace per process, and then the communication operation (i.e. load/store, barriers, sync, etc) are ordered (without a notion of global time, but still requiring the memories to be synchronized if the accesses occur on different physical memory banks). Using partial orders instead of total orders (as it would be if we would rely on a global clock for all events) allows to relax the comparison between events, and even though the analysis is trace based, a correct execution can still be detected as leading to a potential race condition. The detection algorithm is exponential, but behaves well in practice if the processes synchronize often, as
these synchronizations are indeed limiting the number of events to be considered which are parallel. Figure 4.3 illustrates the intervals that can be built from a trace.

![Figure 4.3](image)

**Figure 4.3** Interleavings of memory accesses, the black dot represent the synchronizations

As far as consistency violation is concerned, we believe that virtual prototyping allows releasing constraints on what can be verified today. Indeed, the consistency check on actual parallel machines relies on the fact that, among others, each write must be done with a different value in order to be able to know which process or processor produced it. NP completeness of these checks can possibly (it is still to be proved) be made polynomial by adding information that the virtual prototype may be able to produce. Up to now, we have been working on sequential consistency, but we plan to extend the approach to other memory consistency models.

Profiling is another issue. The question is “how in this mass of traces can I identify weak points”, such as phases of a parallel program producing a lot of cache misses, hot spots due to concurrent accesses to the same target, and so on.

This problem occurs now very often and we have started cooperation with colleagues from the computer science lab of Grenoble to benefit from their research in data mining. The idea is to automatically identify repeated or costly patterns in the traces and then analyze these patterns, which is a much simpler operation, to identify what leads to the specifically occurring problem. We have started experiments on both performance and power consumption profiling with first interesting results. For example, the tool automatically identified a call to a function to lead to high latencies due to the fact that floating point computations were performed by software in a library. To summarize, we apply here existing data-mining strategies to our traces to detect the occurrence of events that occur either very often or very rarely, and then let the designer analyze the identified points himself. We believe that due to the specific structure of the traces, more efficient algorithms than the general purpose ones can be proposed.

This area is supported by the following projects: OpenTLM, SPRINT, LoMoSA, Comcas, HOSPI, iGlance, SoftSoC, Decopus, Damocles, DMSoCProfile.

### 4.3 Low level software


The low level software is the intermediate software layer between the hardware architecture and the software application layer. This low level software, also called Hardware dependent Software (HdS) includes three main parts:

- The Operating System (OS), which manages the sharing of resources. It is responsible for the initialization and management of the application tasks and communication between them. It provides services such as tasks scheduling, context switching, and so on. The relationship with the hardware is tenuous, and mainly through the implementation of drivers.
- The communication layer, which is responsible for managing the I/O operations and more generally the interactions with the hardware components and the other subsystems. This communication layer implements the different communication primitives used for task communication (intra or inter processor).
- The HAL is a thin software layer, which totally depends on the type of processor that executes the software stack, but also depends on the hardware resources interacting with the processor. The HAL performs the processor related accesses on which the device drivers are based to implement the interface for the communication with the device.
To contribute in this field, we have developed a small embedded operating system that has been ported on top of a few typical processors (MIPS, ARM, SPARC, Microblaze, NIOS, x86, …). This OS serves as basic component for a software design flow able to produce binary code for all computing units of a multiprocessor architecture. The design approach is component-based, static, and very low cost. This design approach is the main contribution in the last 2 years. This allows specifically tailoring the OS regarding the services required by an application, which corresponds to the constraints that an integrated system has to meet. In terms of communication layer, a set of platform specific device drivers has been developed. However, sharing the device drivers development knowledge is complex, and writing drivers is an error prone and a time consuming activity. Therefore, we are currently working on automatic driver generation from high level hardware and software description. From a practical point of view, this would simplify this task much.

A device driver interface can be separated into four parts (see Figure 4.4). The driver requires kernel services like memory allocation, and also offers services (e.g., hardware initialization) to the kernel. b) User application sends general commands to the driver using exported driver interface, while c) libraries provide some services to the driver like string manipulation. d) Lastly, the hardware abstraction layer (HAL) accommodates hardware access methods, which are used by the driver.

One of the most elementary pieces of information about a device and the driver that manages it, is what function the device accomplishes. Different devices carry out different tasks and need information at different semantic levels to work out. There are devices that play sound samples, devices that read and write data on a magnetic disk, and still other devices that display graphics to a video screen, and so on. Thus, because of the various and interrelated sources of information, driver generation is intrinsically complex. A method, called Me3D, is currently under investigation to help in driver generation. Step by step, information is requested from the designers (IP-XACT model of the platform or device, behavior of the driver, …) for the final generation. A set of tools is also available, called ADDAX (http://tima-sls.imag.fr/www/research/addax/addax-setup/). Methods and tools are today related to DNA-OS, but will be extended to other OS.

This axis is supported by the following projects: SHAPES, EURETILE, SoftSoC, SoCLib, Ciloé, and HOSPI.

4.4 Future MPSoC Architectures


In our view, the future SoC architectures will be massively parallel, and tend to be more homogeneous (more likely based on identical CPU cores and on coarse grain reconfigurable cores) and will be organized around a network on chip. As a consequence, they will tend to be as hard to program as the parallel machines (shared memory or message passing). One key challenge is to provide support to make their programming easier, specially for memory access. Beside the programming model, the efficiency of MPSoC architectures strongly relies on the efficiency of its cores. Therefore, we are also focused on application specific architectures. The last key challenge is to provide efficient and scalable communication structures, such as 3D-NoC, for these highly parallel architectures. These three key challenges will be described in the following paragraphs.
4.4.1 Memories and programming model

Our work on improving and hiding memory access is focused specifically on shared memory multiprocessor machines, as it has been a widely used approach to concurrent programming. It is also quite natural in integrated systems as the memory bandwidth can be very high, thanks to the use of Networks on Chips. This leads to several choices, detailed now.

- **Make the memory hierarchy transparent and efficient**: this means that caches will be used globally, requiring coherency. This also means that the internal memory will be spread over the chip to ensure a high bandwidth. To optimize the handling of data and instructions, we are currently working on hardware managed page migration techniques to put the necessary information closer to the processors that use it.

- **Optimize the accesses to external RAM**: the access patterns are fundamental to benefit from the highest possible bandwidth for external DRAM accesses. The current memory controllers try to optimize the accesses by building packets of data belonging to the same page, but the memory controller has only a local view of the incoming packets. We try to take benefit from some knowledge available at the Network level, usually available as QoS or priority on virtual channels, in the hope that including this high level information will minimize the latencies and maximize bandwidth.

- **Optimize atomic accesses**: The use of spin-locks has been shown theoretically to be a suboptimal solution to the problem of having synchronized parallel execution progress, and to lead to deadlocks. The introduction of the couple linked load/store conditional or compare and swap has been the advocated solution for years (even though the implementation is not that straightforward). Recently, the introduction of the concept of transactional memories is regarded as an other, more general solution, to the handling of atomicity. Supporting this abstraction requires the implementation of a system called TM, often complex, either software or hardware. In order to investigate the applicability of TM in SoCs, as the support of parallel programming paradigms, we have compared several hardware TM systems based on different architecture choices (cache coherence protocol) and on different conflict resolution policies (i.e. actions undertaken when two or more transactions try to access the same pieces of data). Additionally, since existing TM systems do not ensure starvation freedom, we have also proposed an innovative and efficient conflict resolution policy bringing this guarantee when no cache overflow occurs inside a transaction.

- **Support for unusual concurrent programming paradigms**: POSIX Threads and MPI are the two well known representatives of shared memory versus message passing programming paradigms. For some time, the work stealing idea has been introduced. The principle is that each processor executes its own task until it becomes idle, and then steals a fraction of the remaining work on a randomly chosen busy processor. We have evaluated several implementations of adaptive work stealing and architectural choices to enhance the

![Figure 4.5 Hardware support to distributed memory architectures for work-stealing](image-url)
performances of work-stealing. We have shown that simple architectural support and wise copy of data can provide up to a 20% performance increase compared to a static parallelization.

4.4.2 Application Specific Processors

As previously stated, it is worth developing efficient supports to ease the programmability and to hide memory management inside highly parallel architectures only if cores themselves use efficiently the silicon area. For years ago the market is already lead by this goal through drastic constraints in terms of time to market and design quality, e.g. embedded systems for telecommunication or multimedia, to develop heterogeneous multiprocessor architectures with application specific processors in order to achieve computation and communication performances.

Therefore, we are working on application specific architectures in two different fields: flexible design radio and 3DTV. As an example, by working on a prototype of 3DTV decoder, we have developed a fixed-point version of a free-view point algorithm, i.e. the 3DTV user can choose its own view point on the 3D scene. The developed version was the entry point of a commercial compilation flow that synthesizes the application-specific processor on FPGA. Additionally, we are currently targeting dynamically reconfigurable hardware (some processors or IP can be reconfigured on the fly to achieve a different task), since this elegant paradigm enables to have an homogeneous architecture for the silicon point of view, while achieving better efficiency than CPU-based architectures. More precisely, we are currently focusing two solutions to abstract and manage the reconfigurable hardware.

The first solution proposes a hardware manager to control reconfiguration and allocation. The hardware manager is seen as a peripheral by the OS. The second solution is dedicated to flexible design radio, where the manager can additionally take advantage of information sent by the protocol layers to improve the scheduling of reconfiguration.

4.4.3 Three-Dimensional Networks-on-Chip (3D-NoCs)

Three-Dimensional Integration (3DI) is becoming an appealing solution for integration of MP²SoCs (Massively Parallel Multi-Processor Systems-on-Chip). 3D-Integration results in a considerable reduction in the length and the number of long global wires which are the dominant factors on delay and power consumption, and allows stacking dies of different technologies (e.g. DRAM, CMOS, MEMS, RF) in a single package. The incorporation of the third dimension in the design of the integrated systems allows the exploitation of three dimensional topologies which result in a major improvement in network on chip (NoC) performance. Supposing a NoC with a complete 3D-Mesh topology, the number of vertical channels is equal to $2(N - \sqrt[3]{N})$, where $N$ is the number of network nodes. As generally each channel of a NoC consists of tens and even in some architectures hundreds of physical wire links, such a network with a large number of nodes requires a huge number of physical vertical interconnections. Through-Silicon-Via (TSV) has the potential to offer a great vertical interconnect density and features an extremely small inter-wafer distance. Even though 3D-Integration using TSVs introduces a whole new set of application possibilities, it also introduces new architecture level design issues. The TSV interconnect pitch (mainly due to its pads) imposes a larger area overhead than the corresponding horizontal wires and a TSV consumes all layers in the upper die in addition to the top layer in the lower die. Additionally, fabricating a 3D integrated circuit using TSV technology involves several extra and costly manufacturing steps, and each extra step adds a risk for defects, resulting in potential yield reduction. The yield is an exponential function of defect frequency and the number of TSVs, and thus, exponentially decreases when the number of TSVs goes beyond a certain value. Keeping a homogeneous topology (the same size and shape) for all tiers of heterogeneous chips and using a regular 3D network topology (e.g. fully connected cube) is extremely hard and probably often impossible. Delivering clock to each die and dealing with clock synchronization is another critical problem in the design of the 3D integrated circuits. Furthermore, the run-time temperature variations and stresses and the thermal concerns, which are significant issues of 3D integration, will introduce additional uncontrollable, time-varying clock skew.

To tackle these problems of 3D-Integration technology, we categorize our research on 3D-NoC based system architectural design into three areas:

1) In order to support the network topology heterogeneity of tiers and reduce the number of vertical links (TSVs) used by the network, we have focused on vertically partially connected 3D-NoCs in which the usual planar topologies (normally regular and fully connected, e.g. 2D-Meshes) are partially connected together by only some vertical links and each tier could have its own planar topology independent from other tiers. There are two types of routers: 2D-routers (for example with a switch degree of 5, connected to the four coplanar neighbor routers plus the local subsystem) and 3D-routers (for example with a switch degree of maximum 7, connected to the four coplanar neighbor routers,
plus the local subsystem, plus other neighbor routers placed in the upper and/or lower stages). The goal is not to determine some fixed places for 3D-Routers to construct a fixed 3D-Topology, but to give the system designer flexibility in arranging 2D and 3D routers in any order and any combination as he decides. In other words, the aim is to have no hypothesis and no constraint on the location and connection of vertical links: any node of a tier can be connected to any node of the upper or lower stage. In such irregular 3D topologies the main problem is to define the packet routing strategy (i.e. selecting a path in the network between a source and a destination), as the usual simple algorithmic routings are not applicable. Routing strategies have to provide different guarantees, mainly the freedom from blockage. Deadlock, the situation in which two or more packets are each waiting permanently for another to release a shared channel in a circular dependency, is the most critical blockage. While developing a deadlock free routing algorithm in regular topologies is well understood, proposing a distributed deadlock free routing strategy parameterized by the topology and applicable in irregular topologies is a difficult research topic. By proposing a deadlock-free distributed routing algorithm we have provided a general solution to this issue. We have shown that independently of the size of 2D networks and of the number and placement of the vertical links, the proposed routing algorithm is deadlock and livelock free. We have also developed SoCLib-compatible SystemC model of a router using this routing algorithm. Currently in order to generalize the vertically partially connected topologies to be used in general purpose systems (rather than application specific ones) we are proposing a method to algorithmically determine the place of vertical links.

Figure 4.6  An example of vertically partially connected 3D-NoC

2) In order to overcome the problem of clock skew between layers the use of GALS (Globally Asynchronous Locally Synchronous) approaches is advocated by many 3D integrated systems. A GALS system is divided into several physically independent clusters and each cluster is clocked by a different clock signal. The GALS paradigm also enables the implementation of various forms of DPM (Dynamic Power Management) and DVFS (Dynamic Voltage and Frequency Scaling) methods which, because of heat extraction and energy dissipation, are essential in future 3D-SoCs. Since one obvious way to eliminate the problem of clock skew is the utilization of asynchronous logic, a network with a fully asynchronous circuit design is a natural approach to construct GALS architectures. A large number of locally planar synchronous islands can communicate together via a global three-dimensional asynchronous network. Each link of an asynchronous network works with its own speed as fast as possible, as opposed to the synchronous approach in which the slowest element determines the highest operating frequency. Asynchronous circuits automatically adjust their speed of operation according to the actual local environmental conditions and they are not restricted by a fixed clock frequency. In a 3D-NoC this property offers the opportunity of totally exploiting the potentially high bandwidth of TSVs. This fact that in an asynchronous 3D-NoC the nominal average load of a link is much less than its maximum capacity, especially in GALS systems which the flit injection rate (by synchronous cores) is much lower than the network throughput, encouraged us to search for solutions that make a more efficient usage of TSVs. Serializing the data communication of vertical links is an innovative solution for better utilization of these high-speed connections in an asynchronous 3D-NoC, particularly because 3D integrated circuits are strictly TSV limited to ensure an acceptable yield and area overhead. The serialization allows minimizing the number of die-to-die interconnects and simultaneously maximizing the exploitation of the high bandwidth of these vertical connections, hence
addressing the cost-efficiency trade-off of 3D-Integration using TSV technologies. Additionally, reducing the number of TSVs to be exploited allows for hardware redundancy that is often used to improve the yield. As the principal cause of TSV defects is the misalignments, a simple and effective way to add redundancy and improve yield is to use larger pads. Serialization and consequently using fewer TSVs leads to increase the vertical interconnection pitches and so in the same area we can use square pads larger than standard pads. Another efficient example of hardware redundancy is the use of redundant TSVs which can be used to replace defected TSVs. However the serialization has a direct impact on the network performance. If the serialization degrades the vertical throughput to a value much lower than that of horizontal links, these serial vertical links may become bottlenecks for all paths crossing them. As a consequence, the circuit design optimization of the serializer and deserializer plays a key role. It is also very important to properly determine the optimum serialization level. Hence, our primary desire when designing the serializer and deserializer was to optimize the communication throughput. We have patented our (De)Serializer circuits based on self-controlled (de)multiplexors in 2009.

Figure 4.7 Inter-Router Vertical Connections using Asynchronous link of \( n \) bits divided into \( p \) segments of \( m \) bits serialized to one bit

3) In a successful manner, 3D-Integration leads to integrate billions of transistors in a single chip containing a complete large MP$^2$SoC. But the integration of many processing cores in a single system aggravates the inter-core communication traffic congestions and memory organization becomes an issue as it has a great impact on the overall performance of the system. In a 3D-MP$^2$SoC, most of the vertical data communications are due to the request/responses between processors and their blocks of (shared) memory (which could be SRAM, DRAM or NVRAM). Therefore accessing points of vertical links on logic dies perform hotspots of the 3D-SoC which may lead to highly congested areas and thus unpredictable latency, particularly when combining with our two other solutions for 3D-NoCs (i.e. vertically partially connected topologies and serialized vertical links). By providing two complementary approaches, we are analyzing the performance of a 3D-MP$^2$SoC due to different location of memory interfaces over logic dies, location and number of vertical links, and number and location of serialized vertical links as well as serialization level. First, by using a fast analytical method we obtain the performance metrics (such as end-to-end packet/message latency, saturation point, mean buffer utilization, router delay components and the probability of contention, etc) due to different architectural parameters. After the fast exploration of the design space (by the help of our analytical technique) and choosing the most practical combinations (of memory organization and architectural parameters), we use the SoCLib (SystemC) CABA simulation environment to evaluate the performance of selected solutions in a more precise manner.

This area is supported by the following projects: SOCLib, Sceptre, Ciloé, iGlance, 3DIM3
4.5 PhD topics

1. Bahmani Maryam, “Architectural Exploration of 3D-NoCs”
2. Chagoya-Garzon Alexandre, “Abstraction methods for multiprocessor code generation”
3. Chen Hui, “Models and code generation approaches for HW/SW IP integration”
4. Dubois Florentine, “A compositional approach based on analytical formulations for energy and power analysis of NoC architectures”
5. ElMrabti Amin, “Abstract modeling of architectures and applications for system generation”
7. Gligor Marius, “Programming for low power on MPSoC platforms”
8. Guérin Xavier, “Kernels for heterogeneous MPSoC architectures”
9. Guironnet de Massas Pierre, “Transparent Integration of memory hierarchies in MPSoC architectures”
12. Hedde Damien, “Debug of concurrent programs using non intrusive simulation techniques”
15. Lagraa Sofiane, “SoC profiling based on data-mining tech”
16. Meunier Quentin, “HW support for Parallel programming : work stealing and transactional memories”
17. Prost-Boucle Adrien, “Automatic Generation of hardware accelerators on reconfigurable target using high-level synthesis”
19. Shen Hao, “Models for the estimation and analysis of performances of SoC architectures using flexible processors”
20. Tan Jun-Yan, “NoC prototyping”
21. Xu Yan, “Light software services for dynamical reconfiguration”
5. Verification and modeling of Digital Systems (VDS)

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**Engineers:** F. Pancher (part time), J. Sester

**Interns:** Z. Bel Hadj Amor, C. Deschamps, D. Enéas, J. Fischer

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<td>SFINCS (ANR), FME² (ANR), SoCKET (Pôles de compétitivité), Beyond DREAMS (MEDEA+), Nano 2012</td>
<td>Dolphin Integration, STMicroelectronics, Thales, EADS Astrium, Airbus</td>
<td>LIP6 (Université Pierre et Marie Curie, Paris), Radboud University (Nijmegen, NL), McGill University (Montréal, Canada), Royal Institute of Technology (Stockholm, Sweden)</td>
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The VDS group is mainly concerned by the correctness of the hardware design, from its early specification levels to the "register transfer" level (RTL). The research of the VDS group aims at providing verification solutions based on formal or semi-formal methods. In both cases, the expected behaviour is expressed as a formal specification (roughly speaking, a statement in a formal language or logic). Formal verification makes use of static analysis techniques to prove that this statement holds for the hardware design, while semi-formal verification enables its verification during simulation. In the activities of the VDS group, formal verification is related to the application of deduction-based methods, through the use of theorem provers or proof assistants; semi-formal verification is identified with the construction and use of assertion checkers.

Depending on the size and the characteristics of the design under verification, one of these solutions is more advantageous than the other one. In particular, theorem proving is interesting for reasoning on very abstract (algorithmic) descriptions or for developing general-purpose theories (meta-models for general problems), and runtime verification using assertion checkers is beneficial for more concrete hardware descriptions of large size systems (for which static analysis methods such as model-checking are deficient). These aspects are developed in the following sections, where we describe our work on:

- the assertion-based verification and assertion-based design for IP blocks, using the notion of property checkers and test generators,
- the assertion-based verification of SoC’s at the system level (described in SystemC TLM),
- a meta-model based solution for the formal verification of communication infrastructures in Networks on Chip (NoCs),
- the application of theorem proving techniques to the verification of robustness properties, using a formal representation of fault models.

### 5.1 Assertion-Based Design at RT Level


Assertion based verification (ABV) has raised a real interest over the past few years, and a large diffusion in the industry. Two IEEE standards have been defined to write temporal properties: PSL (Property Specification Language) and SVA (SystemVerilog Assertions). The main CAD tools available on the market provide the designer with furnished toolboxes combining ABV features with simulation: Questa, Verdi, NCSim etc.
Most often, ABV consists in synthesizing properties into hardware or software monitors. These components analyze the design, and detect any behavior violating the corresponding properties. More recent works have addressed the test vector generation from temporal properties. A property is synthesized into a component called generator. It produces signal sequences complying with the associated property. If the environment is described by a set of properties, an environment model can be obtained by combining the corresponding generators.

Our on-going works go beyond this concept, to achieve Assertion-Based Compilation (ABC). In this context, the following question is raised: is it possible to automatically produce a hardware module from a declarative specification composed of temporal properties? This problem is part of the following research domain: automatic synthesis of correct-by-construction circuits from specifications.

5.1.1 Automatic Compilation of Properties into Synchronous Monitors

The Horus tool1 that we developed, based on formally proven correct methods, provides a unified support to assertion-based design, between the specification and the test phases. Given a set of logical and temporal properties written in PSL, Horus automatically constructs a test environment for the design. This construction is fast, correct, and produces efficient monitors and generators. Horus covers the whole PSL “simple subset”, and the whole verification flow: from the simulation to the on-line testing. It can relieve the test engineer from the tedious work of writing correct test benches. When synthesized on FPGA, the instrumented design under test can execute at full speed.

The principles of the automatic compilation of PSL properties into synthesizable monitors have been described in previous reports. As a basic principle, the monitors are assembled following the syntactic tree of the PSL formulas, using as building blocks a library of primitive components. The library elements follow a systematic structure, and present a generic interface. The interconnection procedure is proven correct by induction, in higher order logic.

The status of each property in the instrumented design (strongly hold, hold, pending, fail), displayed on the pending and valid outputs of each monitor, can be traced at each clock cycle. In case of a failed property, the signals involved and the precise temporal origin of their sub-trace are identified. User-friendly post-processing debugging aids, such as graphical trace displays, are not available in our University prototype, but are planned in an industrial development in cooperation with Dolphin Integration.

Integration in SMASH and SLED

This Horus technology is now integrated in EDA tools of Dolphin Integration: SMASH (simulator) and SLED (schematic editor)2. The first release of Dolphin’s mixed signal simulator SMASH integrating Horus based support for PSL was SMASH 5.13.0 and was released in June 2009. Support for PSL was close to the full simple subset concerning FL operators, and only a few SERE operators were supported.

In SMASH 5.14.0 (released in December 2009), support for PSL sequences was improved: all operators are now supported, and the simulation model is generated instantly and is faster. SMASH 5.14.0 also introduces breakpoints on PSL properties which makes debugging a lot easier. Released in December 2009 as well, Dolphin’s schematic link editor SLED 1.5.0 can create verification cells from PSL files, and makes it possible to instantiate and connect them to the design under test. It also customizes (i.e. renames signal names when necessary, which works around the lack of support for port mapping for vunits in PSL) the PSL verification units and generates appropriate SMASH directives when generating the netlist for SMASH, so that instantiated PSL properties are verified during simulation.

Additionally, the SLED SDG (Synthesizable Detector Generator) option, which makes it possible for the user to seamlessly generate PSL verification units as synthesizable VHDL or Verilog monitors, makes it possible to bring Assertion Based Verification into FPGA emulation, or to use PSL as a design language for safety related parts of critical applications.

An industrial case study has been used to assess this integration of the Horus technology in SMASH. The IP, provided as a RTL VHDL description, in an interface that implements the HDLC protocol. The HDLC (High-level Data Link Control) is a synchronous serial protocol used in data communications systems. The goal of the study was to analyze the protocol in order to express the specification (parts of the IP requirements) in PSL form. Thirteen properties related to the transmitter and the receiver parts of the

1 http://timia.imag.fr/vds/Horus/
interface were written and analyzed. This allowed validating and suggesting improvements of this HDLC design.

**Rewrite Rules**

This work has been performed jointly with Marc Boulé and Zeljko Zilic from McGill University, Montreal, Canada. The McGill group had developed their own checker generator tool, concurrently with our development of Horus. Comparisons between the two approaches showed similar results, despite the fact that the internal algorithmics are quite different: their work is based on automata and rewrite rules. A cooperation was established, with the support of a Jacques Cartier grant.

The use of rewrite rules was motivated by the richness of PSL. The rewrite rules were defined to convert various assertion forms into regular expression implications, for further use by simulation or formal verification engines. We have shown how an automated theorem prover can be used to ensure the correctness of assertion language equivalences and rewrite rules. We have implemented the higher-order semantic definition of PSL in the logic of PVS, and used the PVS proof assistant to mechanize the formal reasoning. This was applied to three sets of rewrite rules found in the literature, attempting to prove that they were well founded and semantically correct. We have shown that some of the published rules were actually incorrect. Of the more than fifty rewrite rules, two were not provable because of language semantics issues, nine were shown not to hold on empty traces, and four were shown to be false.

As witnessed in our proof results, we have also shown how certain simple subset guidelines must be changed in order to create behaviors that are better suited to dynamic verification with PSL. We have formally justified the guidelines for writing a simulation friendly PSL.

**Low Power Monitors**

In the first Horus prototype, and in most equivalent published works, the main figures of merit have been the speed and area of the synthesized monitors. If online checking is considered, monitors also have to be designed for power efficiency.

A new library of primitive monitors has been designed, using the clock gating principle, in order to reduce the dynamic power consumption. This technique is of interest only for the primitive monitors that contain 3 or more registers. The low power library has been proven equivalent to the original one, using conventional equivalence checking tools.

A set of benchmark properties has been synthesized in 350 nm and 65 nm, both for the standard and the low power libraries. The essential results are a set of curves showing the frequency of monitor activation for which low power monitors are beneficial in terms of power consumption. In all cases, a price must be paid in terms of area and frequency.

**5.1.2 Test Sequence Generation for Accelerating ABV**

The hardware monitors built using the Horus technology are used during simulation (or FPGA emulation) to check whether their representative properties are satisfied by the design. In that context, guaranteeing that the property is not verified **vacuously** is crucial. Generation of test sequences for the simulator cannot be performed purely randomly: test sequences must be designed to ensure a good coverage of the monitor's activation conditions.

Consider as a trivial example a property of the form $\text{always } (A \rightarrow B)$. If the testbench is such that $A$ never holds, then the property is always verified, but verified vacuously i.e., without having actually been checked. The goal of this study is therefore to develop methods that can either determine that satisfying $A$ is impossible, or produce test sequences that will force infinitely often the satisfaction of $A$. In the general case, properties under consideration may not be already in the implication form, and express requirements that involve primary outputs.

After studying existing solutions (ATPG methods, techniques for code coverage analysis, some results about the production of test sequences related to temporal properties,...), it was clear that none of them was actually adapted to our needs. We thus started the development of a specific method, first under the hypothesis that the circuit has already been synthesized as a netlist of gates and memory elements. In the general case, we transform the PSL property into a SERE (Sequential Extended Regular Expression) implication, using the rewrite rules mentioned in the previous section, then we focus on the left hand side of this implication. Each "letter" of this SERE has to be characterized in terms of the primary inputs and internal registers. To that goal, an algorithm has been specified and implemented; it has been tested on some simple examples. Obtaining such a characterization will allow the application of our Horus test generators to this test sequence generation issue.
5.1.3 Automatic Compilation of Properties into Synchronous Generators

In contrast to assertions that are turned into monitors to check if the design is compliant with the corresponding property, assumptions are used to constrain the behavior of the environment, i.e. restrict the set of possible input vectors. By not considering test vectors that are not compliant with the design input specifications, the test can be more efficient. Modeling the environment of the design with formal assumptions is recent. In this research, we focus on this specific problem: automatically build a simplified model of the environment that feeds the design under verification with test vectors that satisfy a set of assumptions. This model is a (test vectors) generator.

Two versions of the compiler of assumptions into synchronous RTL generators have been implemented:

- A modular construction based on the principles of the monitor compilation. The elaboration of this first prototype was described in previous reports.
- An automata-based construction, built according to the principles of the MBAC tool from McGill University. This second prototype, developed in 2009, is now described.

Generators and monitors are symmetrical concepts: a monitor recognizes the language of a property (actually its complement) while a generator produces the language of the property. It is thus a natural idea to use the same central automaton construction technique to produce property monitors and generators. Since the monitors built by MBAC are of low complexity, we decided to reuse the MBAC approach and automaton construction mechanism to produce synthesizable generators.

Figure 5.1 illustrates the two steps required to build a generator from a temporal property. First the MBAC tool elaborates the checker’s automaton. Then the MBAC_GEN module turns it into a generator automaton that describes all the traces compliant with the corresponding property. Finally the back-end tool extracts the synthesizable HDL description for the generator. In particular, as several traces can satisfy the property, more than one path may lead to an accepting final state: a pseudo-random block is used to randomly choose one transition in the states that exhibit non-deterministic transitions.

A benchmark of 60 generators has been synthesized with Quartus II 7.2 on a Cyclone II EP2C35 FPGA. Measures taken after synthesis have shown that, in contrast to the generators produced by the first prototype, the complexity is related to the automaton, but not to the property. It is then very hard to forecast the size of the generator from the structural complexity of the property: which Boolean and temporal operators are used is a prevalent criterion.

5.1.4 Automatic Compilation of Properties into Synthesizable Designs

Combining the monitor and generator viewpoints above, one arrives to Assertion Based Compilation (ABC). A property is seen as the specification of the module to be designed, where some operand variables are input to the module, and others are outputs. The objective is then to directly produce the RTL design from its assertions.

Following the previous approach, the compilation method is modular: it is based on the interconnection of elementary library modules for the simple PSL operators, according to the syntactic structure of the property. For ABC, we introduce a third type of component: the reactant. A reactant is a RTL design automatically generated from a specification written under the form of an asserted temporal property. A reactant has
inputs and outputs that are operands in the PSL formula that defines the property at hand; it reacts to the input values and produces output values so that the property holds. The construction method is again based on the proven correct interconnection of proven correct elementary reactants, but also elementary monitors and generators.

One reactant is produced for each property. In the general case, the specification has more than one property, and a same variable may appear in several distinct properties. A difficult problem to be solved is the elaboration of a method, and its formal justification, for deciding which properties monitor the variable, and which properties generate its value. Moreover, if a variable is an output for several reactants, these are combined with a special kind of component named solver, to produce the final design.

Our ABC method has been implemented in a prototype software tool called SyntHorus. The compilation complexity is linear in the number of operators of the specification. SyntHorus can process complex specifications that hold hundreds of properties, and produces the final circuit in a few seconds. The size of the resulting RTL circuit is also proportional to the size of the specification.

FPGA experiments have been done on complex circuits: crossbar controller, GenBuf, Net-Maker etc. They showed that automatically synthesized designs are globally more complex than the corresponding hand coded ones. We have demonstrated that the overhead is directly linked to the number of multi-source signals present in the specification. In their absence, no hardware resolution mechanism needs to be embedded and the resulting design is slightly larger than the original one.

![Figure 5.2](image)

**Figure 5.2 Comparison of synthesis results on FPGA between an original Conmax IP and the model compiled with Synthorus**

As an example, Figure 5.2 shows the comparison between a manually designed Conmax IP and the automatically generated design with Synthorus, for 4 masters, using two priority levels, connected to a number of slaves varying from 1 to 16. LCs overhead is clearly visible and remains linear when the number of slaves increases. The main part of this overhead is due to the use of the Solvers. The FFs overhead is noticeably less important.

Our current works aim at removing the weaknesses of the first Synthorus prototype, both in terms of area efficiency, and with regards to the currently non-automatic determination of the (observed/generated) direction of the internal signals.

### 5.2 Assertion-Based Design with an Asynchronous Technology

**Members:** A.Porcher, K.Morin-Allory

The work reported here is realized in cooperation with the CIS group. Similarly to synchronous monitors, asynchronous monitors can be employed for logical simulation or emulation onto a FPGA board. While in synchronous circuits a clock globally controls the activity, the asynchronous circuit activity is locally
controlled using communicating channels that detect the presence of data at their inputs and outputs. This is consistent with the so-called handshaking or request/acknowledge protocol. One transition on a request signal activates another module connected to it. Therefore, signals must be valid at all times. Asynchronous circuit synthesis must be hazard-free. In order to have very reliable monitors, we choose to implement Quasi-Delay Insensitive (QDI) circuits. Indeed, these circuits are very robust to Process, (strong) Voltage and Temperature (PVT) variations. Moreover, they offer nice properties such as modularity and low-power consumption.

Like in the synchronous case, the monitor construction mimics the structure of the property. It is based on a library of primitive monitors (one for each PSL operator) and on a syntax directed interconnection scheme. Figure 5.3 illustrates the construction of the monitor for property:

PSL property P1 is always A -> (B before C);

A monitor observing a synchronous design takes as inputs the Reset, the Clock and the signals (A, B and C) of the design that are operands in the property. The monitor outputs the signal Valid (coded in dual-rail) that provides the evaluation result (‘1’ on the second rail means error, otherwise it means absence of error). To comply with the handshake protocol, the signal Valid is acknowledged. To avoid any behavioral modification in the design under verification, the observed signals and the synchronization signal are not acknowledged. Each synchronous observed signal is turned into a signal that respects the 4-phases protocol via a Synchronizer. This synchronizer has been formally proven correct and fully characterized.

Monitors have been implemented on both an ALTERA DE2 EP2C35 FPGA board and on a library of standard Muller cells in a CMOS 65nm technology from ST Microelectronics. As it is shown in the following Table, the monitor area is very small and so induces a very low over-cost for monitoring an integrated system. Furthermore, the area grows linearly with the complexity of the asynchronous monitor.

![Figure 5.3 Asynchronous monitor for property P1](image)

### 5.3 Assertion-Based Verification at System Level

*Members: L. Ferro, L. Pierre, Z. Bel Hadj Amor*

With the increasing SoC complexity and time-to-market pressure, *platform-based design* is becoming a new paradigm for the design and analysis of embedded systems. Among its advantages, this methodology favors design reuse, architecture exploration, and early software development. It allows to raise the abstraction
level to ESL (Electronic System Level), thus improving the efficiency of various activities such as validation. In that ESL context, SystemC TLM (Transaction-Level Modeling) is perceptibly being adopted, and TLM specifications tend to become golden reference models. Their reliability is therefore capital, and guaranteeing their correctness is compelling.

To that goal, we have developed a solution for the *runtime verification of PSL assertions for TLM specifications*. At that level, assertions express properties regarding communications i.e., properties associated with transactional actions (for instance, data are transferred at the right place in memory, a transfer does not start before the completion of the previous one, etc.). Our verification solution makes use of: (1) a method for the construction of SystemC checkers (monitors) from PSL assertions which is an adaptation of the Horus technique, and (2) a framework for the observation of communication actions. This solution has been implemented in a prototype tool with a graphical user interface, ISIS\(^3\). PSL assertions can be captured through the GUI and:

- the tool performs the automatic construction of the corresponding monitors,
- then the SystemC code of the design under verification is instrumented to relate the variables involved in the properties (formal variables) to actual components of the design.

The monitors are thus linked to the design under test through the observation mechanism, and it remains to run the SystemC simulator on the system made of this combination of modules. Any property violation during simulation is reported by the monitors.

Through its Modeling layer, PSL gives the possibility to use auxiliary variables in assertions. To illustrate the usefulness of this feature at the transactional level, let us consider the example of a Motion-JPEG decoding platform\(^4\). The following property \(P\) can be used to check the reliability of its communication channel: *the data that are displayed (written on the RAMDAC) are exactly the ones that have been transmitted by the EU (processing unit)*.

The expression of this property requires the memorization of the data that are transmitted by the EU, to be compared to the data subsequently written on the RAMDAC:

```c
/* Modeling layer */
unsigned int req_data;    // auxiliary variable
// When the EU transmits data, they are stored into req_data:
if (eu.write_CALL())
    req_data = eu.write.p2;
/* Assertion */
// Every time the EU transmits data, the data subsequently written on the RAMDAC
// will be identical to those previously transmitted data:
assert ALWAYS (eu.write_CALL() -->
    NEXT_EVENT(rdac.write_CALL()(req_data == rdac.write.p2));
```

The Modeling layer allows the declaration of auxiliary variables. In the statement part, statements of the underlying language (C++ here) can be used to initialize and update these extra variables. Here \(req_{\text{data}}\) is a variable that memorizes the transmitted data; it is updated when \(eu\) executes its method \(write\), the term \(eu.write.p2\) denotes in ISIS the second parameter of function \(write\). The assertion states that, each time \(eu\) writes in the communication channel then, next time data will be written on the RAMDAC, these data will be identical to \(req_{\text{data}}\). Memorization is mandatory because the moment when the comparison \(req_{\text{data}} == rdac.write.p2\) is performed is concomitant to \(rdac.write\_CALL()\) but subsequent to \(eu.write\_CALL()\).

To implement this notion in the ISIS tool, we have proposed a formal (operational) semantics of PSL endowed with the Modeling layer, and we have refined it to fit the transactional level.

It is worth noticing that, in property \(P\) above, only one auxiliary variable \(req_{\text{data}}\) was necessary. Indeed, the communication channel does not process several communications simultaneously. Therefore we memorize the transmitted data when the communication starts, and we can use this value to check the data written on the RAMDAC when it ends.

In the case where *several communications can occur concurrently*, using only one global auxiliary variable is no more sufficient. Several verifications of the same assertion, for different values of one or more variables, can overlap on the same evaluation cycles. In other words, we need to enable reentrancy for the PSL assertions.

Therefore we have proposed, and implemented in ISIS, a solution to support reentrant assertions (i.e., different instances of a same assertion evaluated on overlapping evaluations cycles), through the use of multiple checker instances, with local variables. We have extended the PSL syntax with an appropriate syntactical construct, and we have adapted the semantics accordingly.

\(^3\) [http://tima.imag.fr/vds/isis/](http://tima.imag.fr/vds/isis/)
\(^4\) provided by the SLS group
5.4 Formal verification of NoC communication infrastructures

Members: A. Helmy, L. Pierre, D. Borrione

The current technology allows the integration on a single die of complex systems-on-chip (SoC's) that are composed of manufactured blocks (IP's), interconnected through specialized networks on chip (NoCs). IP blocks have usually been validated by diverse techniques (simulation, test, formal verification) and the key problem remains the validation of the communication infrastructure. The work reported in this section addresses the formal verification of NoCs by means of a mechanized proof tool, the ACL2 theorem prover.

In the context of platform-based design, the trend in the design flow is to raise the level of abstraction of the initial phase and to ground the flow on verified parameterized library modules. Yet, on-chip communications are not supported by a general and formal theory, which is necessary to obtain verified parameterized communication modules. Our objective was to provide a formal foundation to the verification of on-chip communication networks, spanning from their initial design specifications to their RTL implementation.

As a first step toward this objective, we proposed the generic network on chip model (GeNoC)\(^5\). It consists of a metamodel of on-chip communication architectures and its implementation in the logic of a theorem proving system. The peculiar aspect of this model is to represent a large class of systems. It is a highly generic and parameterized object. While performing the proofs, parameters such as the size of the network or the length of messages need not to be instantiated. Its implementation in a theorem proving system provides mechanized support and partial automation in the verification effort. The model is implemented in the ACL2 theorem prover. An important feature of ACL2 is to denote both a powerful theorem proving system and an execution engine in the same environment. The theorem proving system has a high degree of automation. ACL2 specifications are written in an applicative subset of Common Lisp and are thus executable.

Our first versions of the model contained unrealistic simplifying hypotheses, concerning the granularity of moves and the time when messages were introduced in the network. As a consequence, while the final result of the communications was correctly portrayed, the intermediate steps were abstracted away: where and when a message is temporarily delayed by the presence of other messages in the network could not be shown. The enhanced formalization proposed as a second step constitutes a significant progress, both mathematically simpler and offering a much larger expressive power:

(i) the current metamodel covers a network specification from the transport layer to the data link layer of the OSI model;
(ii) the progression of the messages in the network is specified step by step instead of considering their transfer atomically from their source to their destination, thus allowing a great variety of scheduling policies (circuit, wormhole, priority, etc.);
(iii) new messages may enter the model at arbitrary times and arbitrary nodes;
(iv) the same model can be used for formal verification and for simulation.

This metamodel represents the transmission of messages on a generic communication architecture, with an arbitrary network characterization (topology and node interfaces), routing algorithm, and switching technique. The main function of this model, called GeNoC, is recursive. Each recursive call represents one step of execution, where messages progress by at most one hop. Such a step defines our time unit.

A first correctness theorem is associated with function GeNoC. It states that for all topology T, interfaces I, routing algorithm R, and scheduling policy S that satisfy specific constraints \(P_1, P_2, P_3 \) and \(P_4\), GeNoC fulfills the following correctness property: every message arrived at some node \(n\) was actually issued at some source node \(s\) and originally addressed to node \(n\), and it reaches its destination without modification of its content.

The proof of this correctness property is derived from constraints (proof obligations) \(P_1, P_2, P_3 \) and \(P_4\), without considering the actual definitions of the constituents. Consequently, the global correctness of the network model is preserved for all particular definitions satisfying the constraints. Following the same principles, a second meta-theorem has been proven, it is concerned with the fact that there is no loss of messages under given constraints (proof obligations).

Proving that a particular NoC is a valid instance of GeNoC amounts to:

- defining the functions that describe the network topology,
- defining all the functions associated with the communications,
- discharging the proof obligations for these functions.

\(^5\) http://tima.imag.fr/vds/GeNoC/genoc.html
This technique has been applied to various NoCs:
- the Hermes NoC (PUCRS, Brazil): http://www.inf.pucrs.br/~gaph/Projects/Hermes/Hermes.html,
- the Spidergon NoC from STMicroelectronics,
- the Nostrum NoC (Royal Institute of Technology, Stockholm): http://www.ict.kth.se/nostrum/.

5.5 Application of formal methods to fault-tolerance

Members:  R.Clavel, L.Pierre

The work reported here is performed in the framework of the FME$^3$ project, in cooperation with the ARIS group. Designing dependable circuits requires in particular evaluating, at each step in the design flow, the achieved level of robustness against various types of faults or errors. In critical systems, an erroneous piece of information may lead to dramatic consequences in terms of human lives. In those cases, errors are generally the consequence of natural phenomena such as particle impacts, electromagnetic perturbations, electrical noise or degradations due to aging. The causes of errors, called faults, were usually modeled in digital systems as single bit-flips or signals stuck either at 1 or at 0. With the evolution of technologies, circuits are increasingly sensitive to transient faults that have therefore become the main concern for designers. Also, faults increasingly lead to multiple-bit errors that are more difficult to detect or tolerate in the system. We target the development of new methodologies for analyzing the robustness of circuits described in VHDL at the Register Transfer (RT) level, with respect to errors caused by transient faults. Our goal is to take advantage of formal methods to get accurate and efficient solutions that would complement existing fault-injection techniques.

In a first solution, we intended to take advantage of the high level of automation of the ACL2 theorem prover. We defined and then formalized in ACL2 the fault model that corresponds to the presence of a single or multiple-bit error in a single register of the circuit. This model characterizes the fault-injection function $\text{inject}$ as a function that satisfies the following conjunction of properties:
- it takes as parameter a state $s \in S$ and returns a state $\text{inject}(s) \in S$
- $\text{inject}(s)$ is different from $s$
- only one memorizing element (n-bit register) differs from $s$ to $\text{inject}(s)$.

In other words, the injection function belongs to the following set:
$$E = \{\text{inject} : S \rightarrow S \mid \forall s \in S, \exists \ i, (\text{inject}(s))_i = f(s)_i\}$$

Encoding such a formulation in a theorem prover would require the presence of quantifiers and the possibility of specifying functions by characteristic properties instead of using a function definition. Despite the fact that ACL2 is first-order and does not support the explicit use of quantifiers, there are solutions to mimic certain kinds of originally higher-order or quantified statements. For instance, the encapsulation mechanism allows to introduce new function symbols that are constrained to satisfy certain axioms, without providing function definitions that uniquely determine the functions's behavior. Using this principle, it was possible to encode the model above in ACL2. However the main problem with this implementation is not the use of the “encapsulate” construct, but the fact that the implementation of the third property (“only one state component differs from $s$ to $\text{inject}(s)$”) in the error model had to be expressed by a theorem that explicitly enumerates every possible error location, thus leading ACL2 to enumerate all the corresponding subgoals. CPU times could become prohibitive with real-size systems. The conclusion was that it is possible to find a way of encoding our models and associated robustness properties in ACL2, but that it may result in a lack of efficiency for performing proofs.

We thus decided to adopt a less automated proof tool, that provides a more powerful logic. One of the candidates was PVS. Its logic and inference mechanisms are powerful enough, without requiring too much effort for realizing proofs. We can take advantage of several PVS features:
- the possibility to parameterize PVS theories,
- the possibility to define predicate functions that make use of universal and existential quantifiers,
- the possibility to override a function definition, by means of the WITH construct. The result of an overridden function is exactly the same as the original, except that at the specified arguments it takes the new values.

The fault model was encoded in PVS, thus making explicit the fault function $f$, and enabling the

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$^6$ http://timagi.imag.fr/vds/FME3/
characterization of a parameterized set of injection functions:

\[ E(F) = \{ \text{inject} : S \rightarrow S \mid \forall s \in S, \exists i, \exists f \in F, (\text{inject}(s))^i = f(s) \} \]

where \( F \) is a set of fault functions. Choosing different instances for this parameter \( F \) easily allows considering the same circuit with several fault models for its registers.

We also defined an extension of this model to characterize the presence of a single or multiple bit error in several registers of the circuit.

These formalizations and the corresponding representations of robustness theorems were applied to examples such as a cash withdrawal system, a FIR filter, and a CAN interface.

A toolchain has been created to automatically generate the PVS source code from the original VHDL RTL description (see Figure 5.4). Using our tool VSYML, we parse the original VHDL RTL code, perform symbolic execution, and we get an XML representation of the transition and output functions. Templates of robustness theorems have been encoded in a library, xml2pvs. The intermediate format produced by VSYML is processed, together with the properties to be verified and the patterns of xml2pvs, by the tools xsltproc\(^7\) and html2text\(^8\) in order to produce a PVS file that contains both the design description and the theorems to be proved in the presence of soft errors. Proof strategies dedicated to the various types of robustness properties have been defined. They enable the mechanization of the proof process.

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\(^7\) [http://xmlsoft.org/XSLT/xsltproc2.html](http://xmlsoft.org/XSLT/xsltproc2.html)

6. Architectures for Robust and complex Integrated Systems (ARIS)

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Research areas
- Design of robust complex integrated systems for nanotechnologies.
- Hardware/Software dependability analysis from RT-Level descriptions.
- Secure digital implementations.
- RT-Level design for reliability/safety/availability and/or security.
- Methodology, tools and experimentation for the study the sensitivity to radiation of integrated circuits and systems
- Methods and tools for fault injection
- Mitigation techniques for the effects of radiation in integrated circuits and systems
- Design and exploitation of experiments on-board satellites and high altitude balloons
- Design for test, yield and reliability in nanometric memories
- Concurrent error detection in nanometric designs
- Circuit self-regulation under variability, circuit degradation and application constraints
- Fault-tolerant, power-aware task scheduling and allocation
- Error recovery architectures for massively parallel processors
- Design for test, yield and reliability in 3D interconnects
- Fault-tolerant 2D and 3D NOC routing algorithms

Contracts
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- PARACHUTE
- MINALOGIC
- ARAVIS
- ASTER
- SOCKET
- SHIVA

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- RECORE (Netherlands)
- ST Microelectronics (France)
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6.1 Summary

The ARIS group was created in 2007 as a continuation and extension of past activities performed in the RIS (Reliable Integrated Systems) and the QLF (QuaLiFication of circuits) groups of TIMA. Research activities of ARIS deal with two main areas: the design of robust architectures for ultimate technologies and the study of the behavior of integrated circuits and systems under intentional attacks or in harsh environments. Indeed, different types of interferences and parasitic effects affect the reliability of modern electronic systems. Nanometer circuits, micro-electronics, micro-system technology and power electronic systems are already part of our daily life. However, these systems may encounter many problems with natural and artificial interferences coming from various sources (e.g. particle radiation effects, electromagnetic interferences, etc.). Another related area is the new threat on secure systems, related to fault-based attacks.

Recent research areas of the group include fault tolerant architectures for mitigating the flaws of nanometric CMOS (variability, accelerated circuit aging and parasitic effects); fault tolerant
architectures for high defect densities targeting post CMOS nanotechnologies; and Computing architectures for nanotechnologies.

A last research area of the ARIS group concerns the design of robust (high-yield, high- reliability, low-power) architectures for ultimate CMOS and post-CMOS technologies. Silicon-based CMOS technologies are approaching their ultimate limits. By approaching these limits, power dissipation, fabrication yield, and reliability are steadily worsening, thus making nanometric scaling increasingly difficult. In particular, process, voltage and temperature variations (PVT) affect parametric yield and reliability. Reliability is also increasingly affected by soft-errors, electromagnetic interferences, and accelerated circuit aging. Low power, a stringent requirement in nanometric technologies, is increasingly difficult to meet with further nanometric scaling. It is also conflicting with reliability requirements as voltage reduction increases dramatically circuit sensitivity to failures.

These problems are becoming increasingly hard to treat as we move down to the ultimate CMOS nodes. They risk becoming showstoppers, unless a new design paradigm able to maintain acceptable levels of power dissipation, yield and reliability is introduced. These issues are further exacerbated by unprecedented complexity levels as the integration of tera-device ICs is expected to become a reality within one decade. Research in ARIS group concerns a variety of approaches spanning from circuit level up to OS, including: design for test, yield and reliability for embedded memories and interconnects (2D and 3D); fault tolerant 2D and 3D routing algorithms; circuit-level concurrent error detection techniques; self-regulation of circuit parameters in response to variability, aging and varying application constraints; fault-tolerant and power-aware task scheduling and allocation; error recovery in multiprocessor systems. These activities culminate to the development of a comprehensive platform enabling designing robust (high-yield, high-reliability and low-power) single-chip massively-parallel tera-device processors fabricate in ultimate-CMOS and post-CMOS technologies affected by high defect densities. In particular, this approach is expected to achieve reliable operation in massively parallel processor arrays where all links, routers and nodes may include faults affecting their temporal behaviour (e.g. delay faults and clock skews), most of them include faults affecting their logical behaviour, and new destructive failures may affect the array links, routers and nodes with high frequency (e.g. MTBF of the order of few days).

Concerning researches related with the operation of integrated circuits in harsh environment, the main stress considered is radiation of nuclear and space environments, but it is interesting to mention that particles reaching the Earth’s surface from the Sun, up to now innocuous for microelectronics circuits, have sufficient energy to flip bits in memories or corrupt the logic of parts manufactured with less than 0.25 μm and supply voltages drop to less than 2.2 Volts. This constitutes a threat to avionics control systems and even to systems operating at sea level.

One of the significant issues of these researches is the prediction of error rates a studied system (circuit, architecture, software ...) will have in the final environment it will operate. The refinement of forecasting error rate strategies needs both to perform ground tests by means of simulated radiation environment (particle accelerators,…), and to compare ground test results to data obtained from experiments aboard of spacecrafts, balloons, satellites or while installed at high altitude.

Another research field concerns the development of innovative methods and tools dedicated to the predictive analysis, validation and qualification of integrated electronic systems using fault injections. The sensitivity predictive analysis platform covers the development of multilevel fault injection methods and tools to be applied at different system abstraction levels from RTL level to gate level descriptions.

The activities of the ARIS group concern both natural and intentional faults in integrated systems. Activities are also on-going on the design of secure circuits protected against fault-based attacks. These activities include the analysis of the circuit robustness against a whole panel of attacks (DFA, DPA, EMA) and the evaluation of protection techniques. Common approaches are developed to analyze the dependability level and protect circuits against both types of faults (natural and intentional), taking into account their different characteristics.
6.2 Design of robust integrated systems under high failure rates


Silicon-based CMOS technologies are approaching their ultimate limits. By approaching these limits, power dissipation, fabrication yield, and reliability are steadily worsening, making nanometric scaling increasingly difficult. In particular, as process parameters variations increasingly spread out with nanometric scaling, the probability that a complex SoC die includes timing faults increases drastically at each new process generation. Timing is also increasingly affected by variations of voltage (due to IR drop) and temperature (due to local hot spots etc). Thus, process, voltage and temperature (PVT) variations may create unpredictable timing behaviour and affect parametric yield and reliability. Reliability is also increasingly affected by soft-errors, electromagnetic interferences (like cross talk), and accelerated circuit aging. Low power, a stringent requirement in nanometric technologies, is increasingly difficult to meet with further nanometric scaling. It is also conflicting with reliability requirements as voltage reduction increases dramatically circuit sensitivity to failures. These problems are becoming increasingly hard to treat as we move down to the ultimate CMOS nodes. They risk to become showstoppers, unless a new design paradigm able to maintain acceptable levels of power dissipation, yield and reliability, is introduced. These issues are further exacerbated by unprecedented complexity levels as the integration of tera-device ICs is expected to become a reality within one decade.

An important research axis in ARIS group concerns the development of techniques for designing robust complex integrated systems. These techniques are spanning from circuit level up to OS, including:

- Low-cost circuit-level concurrent error detection in logic designs covering the whole set of failures affecting nanometric technologies.
- Self-regulation for adapting circuit parameters to variability and circuit degradation.
- New approaches for efficient BIST, self-repair, and ECC implementation in memories.
- Fast memory ECC design.
- Self-test and self-repair for 2D and 3D interconnects.
- Differential Voltage Frequency Scaling at processor-level and array-level.
- Fault-tolerant, variability aware and power-aware task scheduling and allocation algorithms.
- Coherent check-pointing and error recovery at array-level.
- Check-pointing-free error recovery at array-level.
- Fault-tolerant, congestion-free, and deadlock-free 2D and 3D routing algorithms.

Each of these techniques addresses at the most appropriate level some of the major issues concerning yield, power, and reliability in nanometric technologies. Furthermore, several of these techniques are combined into an integrating framework enabling the implementation of robust (high-yield, high reliability, and low-power) single-chip massively parallel tera-device processors, in highly defective technologies. These activities are supported by three CATRENE projects (OPTIMISE, TOETS and 3DIM3) and by the ARAVIS/Minalogic project.

6.2.1 Low-cost highly versatile memory BIST for advanced nanometric nodes and/or 3D systems

In modern SoCs embedded memories concentrate the majority of defects. In addition, defect types are becoming more complex and diverse and may escape detection during fabrication test, leading to field failures due to the use of faulty components in final products. As a matter of fact, memories have to be tested by test algorithms achieving very high fault coverage for a comprehensive set of faults. Fixing the test algorithm during the design phase may not be compatible with this goal, as unexpected failures not covered by this algorithm may occur during production. Also, having the possibility to select the memory test algorithm after fabrication is very important during the initial phase of introduction of a new process node (both process debug and production ramp-up). Finally, in 3D systems, logic (processor) dies can be stacked with memory dies coming from various sources, and using different memory sizes in different versions of a product. Thus, memory BIST integrated in the logic die should be adaptive to the various memory sizes used in the final product and fault models corresponding to the various memory-die sources. In this context, programmable BIST approaches, allowing selecting after fabrication a large variety of memory tests, are desirable but may lead on
unacceptable area cost. In this work we develop a flexible memory BIST approach enabling full programmability in silicon of all three components of memory test (test algorithm, test data, and address sequencing), as well as of the size of the memory under test.

6.2.2 Eliminating speed penalty in ECC protecting memories

One of the major drawbacks in implementing error control codes (ECC) in memories is the performance penalty associated to the code generation and error detection and correction circuitries. In this work, we developed innovative architectures enabling complete elimination of this penalty. The proposed concept and its evaluation to an experimental design is described in a paper presented at DATE 2011. This solution is generic and can be implemented in any SoC architecture. Current work concerns an automation tool able to insert and optimize our solution at RTL for any SoC design, comprising any number of memories.

6.2.3 Self-test and self-repair for 2D and 3D interconnects.

In this work we address Design for Yield of 3D interconnects. These interconnects are realized by means of through silicon vias (TSVs) and represent an important challenge in producing 3D systems, as TSVs exhibit very high failure rates. To cope with this issue we develop efficient self-repair architectures using TSV reconfiguration circuitry that replaces faulty TSVs by fault-free spare ones. However, when we have to repair very large numbers of TSVs and/or when the defect density exceeds a certain level, this approach requires adding a large number of TSVs, resulting in high area penalty and high fabrication cost. In these situations, we have developed an alternative solution in which we transform a parallel transmission link that includes faulty TSVs, into a link that uses only the fault-free TSVs to transmit messages serially. The serialization architectures include two approaches. In the Configurable fault-tolerant Serial Links (CSLs), presented at IOLTS 2010, the serialization circuitry is programmed by an external tester. In the I-BIRAS architecture (Interconnect Built-In Self-Repair and Adaptive Serialization for Inter-Die Communication in 3D Integrated Systems), both the serialization circuitry and its control are integrated in the dies to be stacked. This enables performing serialization not only after fabrication but also in the field to cope with product-life failures. Some results of this ongoing work can be found in our publications at IOLTS 2010 and ETS 2011.

6.2.4 Low-cost circuit-level concurrent error detection in logic designs

Traditional fault-tolerance using massive redundancy (e.g. duplication and TMR) induces very high area and power penalties and has unacceptable impact on hardware resources and power dissipation. In our past work we introduced the double-sampling approach (VTS 1999, DATE 2000), which drastically reduces area and power penalties. While this approach has found significant adoption by both industrial R&D and the academia, it employs redundant sequential elements (a shadow latch per circuit flip-flop) and results in significant power penalty. As a consequence, this approach is often used to protect only the critical paths of a design. Our recent work introduces a combination of the double-sampling technique with latch-based design, in an architecture referred as GRAAL (presented in a chapter of the book “Soft Errors in Modern Electronic Systems”, M. Nicolaidis, Springer 2011). With this architecture, concurrent error detection is achieved by adding just an XOR gate per circuit latch, resulting in a low-area and low-power concurrent error detection scheme. A first implementation of this scheme, using the CSEM icyflex1 processor, shows an area penalty of 17% and a power penalty of 8.4% (ETS 2011) for complete protection of all circuit paths. Current work concerns an improved implementation targeting less than 13% extra area and less than 5% extra power for complete circuit protection.

Work on double-sampling in flip-flop based designs targets a new approach enabling trading error detection capabilities with circuit speed, in a manner that the circuit adapts its operation on the fly to changing reliability requirements and/or severity of environmental conditions.
6.2.5 Self-regulation for adapting circuit parameters to variability, circuit degradation and application context

In this work, we monitor the rate of error detections provided by the concurrent error detection circuitry, in order to determine optimal operating frequencies and voltage levels and adapt accordingly clock frequency and Vdd to PVT variability, circuit degradation during product life, and varying computing-power requirements due to changing application contexts. Power dissipation/reliability constraints are used to select the operating clock frequency and Vdd level of the circuit according to the computational constraints (task deadlines) required by the application. Aggressively low Vdd is used for tight power-dissipation constraints, relaxed Vdd is used in reliability-tight constraints. Interactions between hardware and OS are used, as reliability and power-dissipation constraints, and application deadlines are provided by the OS, while the final selection of Vdd and clock frequency is done at the hardware level.

6.2.6 Fault-tolerant, congestion-free and deadlock-free 2D and 3D routing algorithms

This work targets single-chip, massively parallel processors. Conventional fault tolerant routing uses routing tables and determines fault-free routes in a static manner. Unfortunately, in a complex network, this approach will lead to frequent congestions as statically pre-established routes can not take care of the actual network traffic. To cope with this issue, we have developed a distributed algorithm in which the routing decisions are taken locally and opportunistically (i.e. the routing path is modified according to congested or faulty node/router/link that a message can encounter during its transmission). This approach can tolerate failures of high multiplicity and avoid congestions, but deadlocks become possible. We achieve deadlock freedom by using virtual channels and pertinent routing rules acting at the local level. The algorithm was shown efficient in networks comprising thousands nodes and affected by high defect levels. Some results of this ongoing work can be found in our papers published at 2010 IEEE Network Computing and Applications and at DATE 2011. These algorithms have been extended to cover 3D networks. Some results of this extension can be found in NORCHIP 2009 MICPRO 2010, IOLTS 2010.

6.2.7 Variability, aging and power-aware task scheduling and allocation

In this work we develop algorithms for performing task scheduling and allocation that minimizes power, under constraints related to variability and to aging-induced circuit degradation. In our approach we consider the application to be organized into tasks, task clusters and groups of task clusters. The approach acts in three steps. The two first steps are done off-line.

The first step performs local static allocation: it determines the number of execution cycles of each group of tasks clusters and their sum (giving a rough estimation of time and power). This step is easy to perform (low computation complexity).

The second step performs global static scheduling. It determines a set of optimal operating points (time-power) for each group of task clusters. Due to the high computational complexity, we perform this step by means of a genetic algorithm.

The third step (on-line scheduling), uses the results of the second step to select the points that minimize the energy of the active groups of tasks while respecting their deadline. This approach targets a global optimization and is computationally intractable for large processor arrays. The results obtained leaded us to the development of local, non-deterministic approaches using opportunistic decision rules.

6.2.8 Coherent check-pointing and error recovery at array-level

This work concerns check-pointing and rollback recovery in single-chip multiprocessor arrays. The challenges we faced in this domain are twofold. First, when rollback is executed in some parts of the system, we have to maintain coherence with the tasks executed by other parts. Second, check-points have to be saved in reliable (thus external to the chip) memory. But as the single-chip multiprocessor I/Os are limited, they may be easily congested by check-pointing. To cope with these issues we developed innovative coordinated check-pointing algorithms that enable performing coherent rollback in a simple manner. Furthermore, in large processor arrays, intelligent broadcast techniques and partitioning are used to reduce the number of broadcasts and the size of checkpoints. Some results of
this ongoing work have been published in IOLTS 2008, ISCAS 2008, DELTA 2008, and MICPRO 2010.

In a more recent approach, we use a hierarchical (parent-child) task distribution approach and maintain the hierarchy until successful execution. In case of a failure occurring in some node when it executes some part of the application, its parent node distributes this part to other fault-free nodes of the array. This way, error recovery is achieved without performing check-pointing, thus avoiding the associated performance penalties and possible I/Os congestions. The approach is shown to be robust to multiple node failures, as we can go up to the parent-child tree until a fault-free parent node.

The two approaches are complementary as in some applications storing intermediate states for performing check-pointing require less memory space than maintaining the task distribution hierarchy while in some other applications the inverse is true.

6.2.9 Integrated fault-tolerant routing, power-aware task scheduling and allocation, rollback recovery and circuit parameter regulation

In the first part of this work we developed an innovative algorithm integrating fault-tolerant routing, power-aware task scheduling and allocation and rollback recovery in single-chip massively parallel multiprocessors. We resolve the complexity of fault tolerant routing and task scheduling and allocation in complex arrays by adopting a distributed non-deterministic approach, taking local decisions in opportunistic manner. This algorithm uses a hierarchical (parent-child) task distribution approach. It maintains this hierarchy until successful execution of the current tasks. In case of failure in some array node its parent node distributes the failed part of the application to new nodes of the array, as described in the previous section. This way, error recovery is achieved for multiple failed nodes without performing check-pointing, thus avoiding storing check-points to an external memory and the associated performance penalties and I/Os congestions. The fault tolerant and error recovery capabilities of the algorithm were validated in arrays comprising thousands of processing nodes and including up to 20% failed routers /links /nodes, executing streaming applications.

The above algorithm was further extended to perform circuit parameters regulation adaptive to PVT variability, circuit degradation due to aging, and changing reliability, power-dissipation and computing power requirements of the application. To cope with the intractable complexity associated with the management of these requirements in complex processor arrays, we chose a hierarchical approach which adopts the task distribution hierarchy described earlier. Regions, sub-regions and nodes of the array are selected by the different levels of the task allocation hierarchy, by taking into account power-dissipation and speed distributions over the array nodes induced by variability and aging. This approach enables efficient power and deadline aware task scheduling and allocation at reasonable computation time.

Furthermore, in the proposed approach, each task encapsulates deadline constraints and power dissipation/reliability constraints. These constraints are used by the node selected for executing the task to determine its operating frequency and Vdd level.

6.2.10 Designing robust single-chip massively parallel tera-device processors

The above approaches are integrated in a framework aimed at designing robust single-chip massively parallel tera-device processors, comprising thousands of processing nodes and fabricated in ultimate CMOS or post-CMOS technologies affected by high defect densities. Our platform combines several of the approaches described above in an innovative manner that enables their optimal cooperation and allows handling high defectivity while achieving low-power operation. Particularly, this approach is able to achieve reliable operation in arrays where all links, routers and nodes include faults affecting their temporal behaviour (e.g. delay faults and clock skews), most of them include faults affecting their logical behaviour, and new destructive failures may affect with high frequency (e.g. MTBF of the order of few days) the array links, routers and nodes.
6.3 Hardware/Software dependability analysis from RT-Level descriptions

Members: R. Leveugle, P. Maistri, P. Vanhauwaert, J.B. Ferron, M. Anghel, M. Ben-Jrad, S. Bergaoui, R. Clavel (VDS), L. Pierre (VDS)

Significant effort was targeted during the last years on developing efficient techniques to analyze, at design time and early in the design flow, the functional consequences of soft errors. The goal is to precisely identify the soft errors leading to unacceptable application disturbances, in spite of all the possible masking effects due to the circuit architecture (redundancy, performance-oriented features, etc.) or to the application characteristics (meaningless computations in a parallel structure, meaningless precision of some data, etc.). Targeted circuits have essentially been synchronous digital circuits. Most of the techniques, developed since more than ten years in the team, start from synthesizable RTL descriptions. Such descriptions are already close to the final hardware in terms of cycle accuracy and in terms of memory cells identification. Higher level descriptions may in some cases be used, with limited representation of soft error locations and reduced accuracy in terms of propagation analysis. Software is also taken into account in the case of systems based on microprocessors. Robustness evaluations may aim at (1) classifying the soft errors with respect to their functional impact (2) identifying error propagation paths (3) identifying critical locations or registers (4) ensure that a given set of behavioural properties always hold for a given set of soft errors (e.g., a given maximum multiplicity of erroneous bits). Classification may be used to compute derating factors on the application failure probability. Critical locations are hardened in priority when trade-offs have to be made. The efficiency of the hardening techniques implemented at RT-Level can be validated as well during such analyses.

A whole set of techniques has been developed to cover the wide range of analysis objectives and circuit characteristics. Most of the studied approaches concern the optimisation of fault injection techniques. One cornerstone has been for a long time the length of the experimental campaigns. Most efforts were therefore targeted to the performance optimisation, but without forgetting the need for flexibility with respect both to the type of circuit and the analysis aims. In addition, techniques have been studied to (1) reduce the number of soft errors to inject (2) analyze the criticality of variables and registers for embedded software and (3) propose alternatives for cases in which fault injection is not adequate, such as the need of guarantee of a given behaviour in spite of all assumed soft errors.

Concerning the acceleration of the fault injection experiments, we proposed more than ten years ago to take advantage of hardware emulation. A few years ago, we proposed efficient injection platforms based on SoPCs (System on Programmable Chip). Such platforms take advantage of the processor core integrated in the SoPC to reduce the quantity of data exchanges with the host computer, thus accelerating the experiments, while maintaining the largest flexibility with respect to the type of possible dependability analyses. The platform has still been improved with new optimizations published in 2010 at LASCAS. Unfortunately, even with such accelerations, exhaustive fault injections often remain unaffordable in a reasonable time.

Another approach has also been used, based on the partial reconfiguration capabilities of some FPGAs. In that case, it is possible to avoid any instrumentation of the circuit under evaluation; soft errors are injected by reconfiguring the contents of flip-flops. The same approach can be used to study the effect of configuration errors in SRAM-based FPGAs. We have also improved the injection environment by adding a database of realistic error patterns in order to improve the precision of the analyses. The patterns can be obtained once from device characterizations under a given perturbation source. The obtained patterns can then be used to analyze the robustness of several versions of a design or several designs, without resorting each time to costly perturbation sources such as particle accelerators or lasers. This is especially powerful to study regular structures since the patterns obtained on a small area of the chip can be abstracted and relocated on similar areas in other parts of the chip. This has been exploited for example in FPGAs to study the effect of configuration errors. The approach has been published at IICECS in 2010.

Due to time limitations, only partial analyses can be performed in most cases. They are based on a randomly (and often arbitrarily) selected set of faults or errors. Such a statistical fault injection (SFI) has been very extensively used in the literature but the margin of error on the results given on such a basis was unknown. We have therefore proposed and validated an approach to quantify the errors on the results with a given confidence level, or conversely to evaluate the number of injections to perform
in order to achieve a given error/confidence level. The method has been presented at the DATE Conference in 2009.

SFI can then be very useful in doing quick classification or derating factor estimations, with a controlled margin of error. Unfortunately, this approach does not address all possible expected outcomes of a fault injection campaign. In the case of a large number of potential errors and workload cycles, only a very small proportion of the registers are actually perturbed at a few cycles. This means that such results cannot help in identifying the most critical registers or clock cycles. Flip-flop grading remains possible when the random selection is only used to reduce the number of injection cycles in each flip-flop; however, in that case, the efficiency of SFI is noticeably reduced and the required number of experiments remains very large. Error propagation paths are also only partially exercised, so decisions on the best hardening positions are hard to make. Finally, SFI cannot guarantee that a given property always holds; this can at best be assessed with a given margin of error. Several complementary approaches have therefore been studied in order to more efficiently obtain some expected outcomes and will be summarized hereafter.

An approach based on Timed Petri Net models has been proposed and evaluated. It has been shown that this type of model can efficiently identify some harmless errors even in the case of architectures difficult to analyze with classical fault pruning techniques. Such models can therefore be used to reduce the number of injection experiments. They can also help in grading the criticality of the flip-flops in a circuit. The results have been presented at IOLTS in 2009.

For embedded software, identifying critical variables or registers is very important before fault injections are started. An improved algorithm for critical register identification has been proposed and implemented in the Gcc compiler; this has been published in the IEEE Transactions on Nuclear Science in 2010. Effects of compilation options on the register and memory criticality have been analyzed and presented at LASCAS 2010 and DELTA 2011. The study also pointed out the strong impact of micro-architectural features (such as dependency management) on the actual criticality of internal processor registers. As a consequence, an algorithm was developed to improve the precision of the lifetime analysis; this algorithm is currently under evaluation for the Leon3 processor.

The specific case of configuration errors in SRAM-based FPGAs was also addressed by developing a tool performing static analyses at design time to evaluate the criticality of the various bits in the configuration file. Such analyses are less precise than fault injections because the dynamic behaviour of the application cannot be captured, but they can be very short (a few minutes, while fault injections may require days or weeks). The SEFEA-ProD tool developed in the team was used to analyze the robustness of designs in Xilinx Virtex II and Atmel AT40K devices. Comparisons have been made with experimental results based on laser fault injections and proton ground tests, showing very good correlations. Results have been published at SCS in 2009.

Another study aims at proving properties even in presence of soft errors. This follows 2005 experiments based on formal property checking and published at IOLTS. Work was done in collaboration with the VDS group in TIMA and the LIP6 laboratory, in the frame of the FME3 project, supported in the period 2008-2010 by the French national research agency (ANR). Model checking techniques and theorem provers (ACL2, then PVS) were used and extended to efficiently model the effect of single or multiple bit errors and prove properties in presence of such errors. The resilience of systems was in particular analyzed, i.e. their capability, after a disturbance due to a soft error, to recover a correct behaviour. The work is continued in the frame of the SHIVA project, to prove the efficiency of some protection techniques against fault-based attacks on cryptoprocesors.

6.4 RT-Level design for reliability/safety/availability and/or security

Members:  R. Leveugle, P. Maistri, G. Canivet, V. Maingot, S. Bergaoui

Protecting a design against natural perturbations or malicious attacks can be done at several levels. We mostly focus here on approaches that can be applied at RT-Level, therefore quite early in the design flow and easy to synthesize on several physical targets (several ASIC technologies, FPGAs ...). Approaches studied in the past also included operating system or software modifications but we focused these last years on hardware protection techniques. Some protections aim at improving reliability, safety and/or availability against natural perturbations (radiations, particles, electromagnetic fields) and other disturbances caused by for example process, voltage and temperature (PVT) variations. Some others are dedicated at improving security against malicious attacks, either passive
(based on power or electromagnetic measures) or active (laser-based, glitch-based or electromagnetic-based perturbations).

The main part of the work is on the development and validation of robust cores including new protection schemes against malicious attacks. Processor cores are extended with dependability-oriented features (Leon2 some years ago, currently Leon3) and cryptographic coprocessors are designed (especially for the AES and RSA encryption/decryption algorithms). This activity is part of several projects, including SHIVA (Minalogic) and EMAISec (ANR). The coprocessors developed in the frame of SHIVA have strong throughput expectations in addition to fault-based attack protection. The versions developed within EMAISec aim at demonstrating protections against electromagnetic attacks.

After analyzing the realistic error patterns obtained due to laser-based and power glitch attacks onto SRAM-based FPGAs (publications at IOLTS 2008 and VTS 2009), it was shown that an efficient protection or "countermeasure" against fault-based attacks on a ASIC implementing an AES crypto-processor (published in IEEE Transactions on Computers in 2008) was not efficient on SRAM-based FPGAs due to the remanent errors induced in the configuration. An improved countermeasure was therefore implemented and validated; this has been published at ASAP 2010 and in the Journal of Cryptology (Springer). Additional protections have been designed and are under evaluation against electromagnetic attacks.

In addition to the development of hardening techniques and hardened IPs, a study has aimed at evaluating the impact of fault-oriented protections on leakage information. As a matter of fact, in the security context, it is useless to protect a circuit against only one type of attack, since a hacker could use several approaches to obtain secret information. The last results on this study were published at SCS 2009.

Recently, a study was started on the use of Graphics Processing Units (GPUs) to implement cryptographic functions. GPUs are many-core structures that can be well suited to implement high-performance cryptographic applications at low cost. The study is currently focused on performances but will be extended in the near future towards countermeasures for robust implementations.

Due to the increasing spatial multiplicity of error patterns, protecting a circuit with information redundancy is more and more difficult. This is particularly true when malicious attacks are concerned, but the problem exists also for natural perturbations. Another approach consists in using functional checks. In this context, we have developed in 2008 a new control-flow checking technique that has been improved in 2010. This technique is non-intrusive and does not require a modification of the initial microprocessor-based system. Checks include not only the control flow itself, but also the integrity verification of critical data, with several possible trade-offs between overheads and error detection. No assumption is made on the error multiplicity. The approach is compatible with the norms requiring a complete separation between the nominal functions and the checking features (e.g. for automotive applications). A first prototype has been developed including (1) a specific watchdog processor (or infrastructure IP I-IP) and (2) development tools. The watchdog program is automatically generated at compile time by a modified version of the Gcc compiler. Additional tools have been recently developed to cope with linkage constraints. The current prototype is currently optimized and will be validated in 2011 by fault injection campaigns. It will be used as a basis for security management in the SHIVA project and to validate the approach against radiation impacts in the CATRENE OPTIMISE project.

Finally, studies are on-going on the problems related to configuration errors in SRAM-based FPGAs. The goal is to propose specific design techniques to achieve robustness at lower cost than the classical massive redundancy approach. A first approach is under evaluation for detecting configuration errors in Atmel AT40K devices by taking advantage of unused resources for a given design.
6.5 Radiation Hardened memory cells

Members: L. Anghel, M. Nicolaidis, R. Velazco

Radiation-induced transient effects in silicon CMOS circuits are essentially charge collection and transport phenomena resulting from direct ionization. The collected charges may inadvertently change, for short time intervals, the internal node voltages of the circuit (single event upset). These transients may change the electrical behavior of the MOS transistors in digital and analog circuits.

Design hardening techniques at circuit level can be developed to achieve immunity to upsets. A lot of hardened-by-design memory elements have been proposed in the last years. In 1994 and 1997 were developed two hardened cells in TIMA laboratory, so-called, HIT (Heavy Ion Tolerant cell) and DICE (Dual Interlocked Cell) respectively. The philosophy was to strengthen the feedback of the cell in order to restore the data potentially corrupted by the impact of a charged particle. However, the price to pay is an increase of the cell area and a higher power consumption. In 2010 the HIT cell was included in the DARE (Design Against Radiation Effects) library and is presently considered to be transferred to many industrial partners to be used for the development of commercial radiation hardened circuits.

6.6 Study by real life experiments of the effects of natural radiation on the operation of submicronic integrated circuits

Members: P. Peronnard, W. Mansour, G. Foucard, R. Velazco

Ionization resulting from charged particles and atoms present in the substrate of CMOS circuits, may modify memory cell's content or provoke a transient pulse within a combinational circuit. This phenomenon which until recently was only considered to be a treat for space applications is nowadays a major concern for avionic equipments and even for any application operating at ground level. Thus it constitutes a potential obstacle to the reliable operation of circuits manufactured from future deep submicronic processes.

We have developed experimental boards, so-called SRAMCheckers including a 1 Gigabit SRAM memory built from successive generations (130 nm and 90 nm) of COTS (Commercial Off The Shelf) SRAM circuits. The boards are exposed to the effects of natural atmospheric radiation both during commercial long-haul flights and in high altitude balloons. The goal of these experiments is to get objective data about error rates and errors features (multiplicity for instance) in the real life environment, this with the final goal of predicting the conjecture will face the future of submicronic components. The sensitive to the considered errors of SRAMs selected for these real life experiments was also predicted using a tool developed at ONERA DESP. This tool, so-called MUSCA SEP³ (MUlti-SCAleS Single Event Phenomena Predictive Platform (MUSCA SEP³)) consists in sequentially modelling all these various physical mechanisms likely to lead to a SEE occurrence in integrated circuits. MUSCA SEP³ inputs include a device description, i.e., the semiconductor active zones, the passivation metallization layers and the package. When the tested circuit is a SRAM, the elementary cell (layout) is described and so the rules of translation allowing modelling the whole memory plan.

The SRAM Checker boards were activated during many commercial flights and balloons (in the frame of BALLTRAP project with ONERA) putting in evidence the occurrence of MCU (Multiple Cell Upsets) and MBU (Multiple Bit Upsets) which are of high concern for applications requiring high reliability. Indeed, many of the faults detected proved that as the impact of a single neutron may perturb the content of 3 bits of a word. In 2009 the results obtained in flights were presented at IOLTS 09 (International On-Line Test Symposium), and a work confronting predicted error-rate to obtained measures was presented at NSREC and published at IEEE TNS.
6.7 Development of a generic and flexible test bed suitable for the qualification of integrated circuits devoted to operate in harsh environment

Members: R. Velazco, G. Foucard, P. Peronnard, W. Mansour

With the miniaturization, integrated circuits become more and more sensitive to perturbations resulting from the effects of the environment (temperature, radiation, EMC...). This activity concerns the design and HW/SW improvements of a test system which facilitates the realization and exploitation of qualification tests for all kind of circuits, from a simple register bench to complex components such as processors.

Screening tests are mandatory to predict error rates in many fields. In the case of radiation, they consist in exposing the studied parts, eventually operating in vacuum, to particles representative of the ones that will be encountered in the operational environment. The hardware and software developments related with such tests must take into account the random nature of event occurrence, both in time and space. On one hand this entails on-line error detection, on the other hand this makes mandatory the need for development of ad hoc hardware mechanisms related with the detection and recovering from destructive errors, such as SEL (Single Event Latchups), which are power/ground short circuits provoked by the activation of a parasitic thyristor present in bulk-CMOS circuits impact of a single particle; or critical errors (sequencing loss, system crashes) that may occur circuits such as processors, system on chips,....

In the past we have prototyped different versions of a dedicated test system having the following characteristics:

The last version of such a platform, called ASTERICS (Advanced System for the TEst under Radiation of Integrated Circuits and Systems), was designed to deal with the following requirements:

- The whole system must have a size allowing to entirely fitting it in enclosures commonly used for environmental qualification tests.
- The DUT must be tested on-line, operating in nominal conditions.
- The system should allow to exercise as many circuits (among candidates to a given project for instance) as possible, to avoid waste of time/money consequence of delays provoked by operating the facilities used to simulate the studied environment.
- Capability for the tester to be remotely controlled anywhere in the world through the internet network.

The new ASTERICS test platform constitutes a powerful tool with generic capabilities for the qualification under radiation of digital circuits. The idea is to implement the whole DUT board architecture by means of an FPGA whose configuration is obtained from compiling the description of key features of the DUT in a hardware description language such as VHDL or Verilog. In this way, there is only a minor hardware development, limited to wiring the DUT pins to the ones of the tester connector. The architecture of ASTERICS is mainly composed of:
• A Xilinx Virtex4FX FPGA, containing a PowerPC hardware processor, having in charge the following tasks: it controls the circuit under test, runs on and off the test sequences and monitors the latchup circuit. It is also able to transfer test programs and to gather test results from the component being studied to/from the PC user interface via an Ethernet 10/100/1000 link. A second FPGA used as a chipset and several static and dynamic memory banks are also included in the board: a 32Mb SRAM memory organized in 2 banks of 512k*32bits (which should allow the test of advanced 64-bits processors) and 512Mb of DDR-SDRAM (16Mx32bits) to enable fast and efficient processor tests. To cope with a wide range of DUTs, all these memory banks are managed by the FPGA of ASTERICS’s motherboard, a Virtex4LX FPGA from Xilinx, which is optimized for high-performance logic. It is multi-volt Input/Outputs compliant, that means it can drive signals in 3.3, 2.5, 1.8, 1.5 and 1.2 Volts, reducing the number of components required to interface the DUT.

• The DUT board comprises exclusively the component to be tested and, in some cases voltage regulators.

The last enhancement of ASTERICS was the proof of its remote use, through the ETHERNET connection. Such a feature may allow significantly reduce the cost of radiation testing campaigns, as they may be performed without requiring the presence of the experimenter. The demonstration of this remote use of ASTERICS was done in the 2009 and 2010 editions of SERESSA (international School on Radiation Effects on Systems for Space Applications) performing on-line laser tests remotely monitored. ASTERICS was transferred to the CRC (Cyclotron Research Center) of UCL (Université Catholic de Louvain-la-Neuve, Belgium) to be used in the future as the basic platform for radiation ground testing performed in various radiation ground test facilities.

![Figure 6.2 ASTERICS: a generic test platform for radiation ground testing and fault injection](image)

### 6.8 Predicting SEU error rates from Radiation Ground Testing and Fault Injection

**Members:** R. Velazco, P. Peronnard, G. Foucard

When estimating the sensitivity to radiation of an integrated circuit the goal is to evaluate the average number of impinging particles required to provoke a fault. Main considered non destructive faults for advanced ICs are SE (Single Event Upset), MBU (Multiple Bit Upset), MCU (Multiple Cell Upset and SEFI (Single Event Functional Interrupt). The consequences of this in the operation of a circuit or a system can be studied by means of fault injection techniques performed according different strategies, which depend basically of the available circuit model (SPICE, RTL, ….). To evaluate the error rate of a circuit/system it is in all the cases is required a measure of the intrinsic sensitivity, so-called cross-section, of the target circuit/system to the considered Single Event. 

σ is called the interaction cross-section and is a direct measure of the IC sensitivity and is calculated as the number of particles required to provoke one Single Event. Its unit is the cm² or it is expressed in barn (1 barn = 10⁻²⁴ cm²). Generally σ is given as an interaction cross-section per device (or per bit).
As a consequence, the end-product of a radiation ground testing will be a plot of the interaction cross-section versus particle energy (measured in terms of Linear Energy Transfer (LET) which is the energy transferred to the Silicon by the impinging particle.

Processors are included in most of the architectures devoted to embedded systems. The determination of SEU cross-section of microprocessor’s memory elements requires the use of a so-called static test which consists in exposing the device to a suitable particle flux while the content of the DUT’s registers and memory elements are observed. This is usually attained by executing a test program in charge of initializing these memories and dumping their content after a given period of time. The usually obtained measure, called cross-section (the number observed bit flips divided by the number of incident particles) is used to predict the final error-rate of the tested device in a given harsh environment. However it has been shown that the measured static cross-section can significantly overestimate the one the circuit while it executes a real application. The reason is simple: while a test program is written to maximize the number of errors observed, a real application is not. Moreover, many memory bits are not used, or are refreshed so often that SEUs in these regions have no impact on the system's behavior.

Fault injection may helps in predicting the behavior of a real program which would be used for the final application. It was demonstrated by many experiments that the final cross section of an application executed by a processor can be obtained by multiplying the static cross-section by the error rate obtained during fault injection. The key point is how to perform a fault injection campaign where instants and location of injected faults suitably match the ones of faults occurring when the application will operate in the final environment.

Fault Injection strategies can be classified in two families: software based and hardware based. Among software based ones, depending on the available DUT description level, can mentioned:
- SPICE based fault injection, if a SPICE net-list is available;
- VHDL / Verilog fault injection when a behavioral or RTL description does exist;
- ISS based fault injection if an Instruction Set Simulator is available.

Hardware based fault injection requires a physical device, and faults can be injected using:
- FPGA based fault injection, if a RTL description is available and mapped to an FPGA;
- The CEU (Code Emulated Upset) method, based in the random activation of interrupt signals.

The CEU approach, initially proposed by ARIS and published in 2000 consists in triggering, at a randomly chosen clock cycle and while the processor is running, an asynchronous interrupt. When the DUT receives the interrupt, it transfers the control from the executed benchmark to a trap handler. This handler then flips the content of a randomly chosen bit and resumes the benchmark execution. Obtained results proved that the predicted error rate fits very well the measured ones. The last years the CEU approach was extended to complex processors, to make possible to target cache memories as well as register files. This new concept was explored in the frame of SCADRI project and applied to two advanced processors: the Power PC 7447 and 7448. The main contribution of these experiments was the validation of the CEU error-rate prediction approach for an advanced and complex processor while it executed a program issued from a real space application, an Attitude and Orbital Control Systems (AOCS) provided by CNES (French government space agency).

Fault injection sessions and radiation ground testing campaigns were performed using the ASTERICS test platform. Radiation ground testing results were gathered during experiments performed at Louvain-La-Neuve heavy ions facility. We used the resulting cross-sections and flux settings as inputs to our fault injection set-up. Outputs of the fault injection experiments were analyzed with exactly the same tools used to analyze the radiation ground test results. At the 95% confidence level, there was no disagreement. The test set-up cannot see significant differences between the rates of SEU induced by radiations and those issued from SEU-like faults injected. In the tables 1 and 2 below are provided, for two selected heavy ions, results proving the accuracy of the proposed approach to predicted SEU rates.
Table 1: Predictions vs. Measures for the PPC 7448 when data cache is deactivated

<table>
<thead>
<tr>
<th>Ion</th>
<th>$\sigma_{\text{SEU \ predicted}}$</th>
<th>$\sigma_{\text{SEU \ measured}}$</th>
</tr>
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<tbody>
<tr>
<td>Argon</td>
<td>1.96E-06</td>
<td>1.84E-06</td>
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<tr>
<td>Krypton</td>
<td>3.82E-06</td>
<td>3.56E-06</td>
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</table>

Table 2: Predictions vs. Measures for the PPC 7448 when data cache is activated

<table>
<thead>
<tr>
<th>Ion</th>
<th>$\sigma_{\text{SEU \ predicted}}$</th>
<th>$\sigma_{\text{SEU \ measured}}$</th>
</tr>
</thead>
<tbody>
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<tr>
<td>Krypton</td>
<td>3.24E-05</td>
<td>3.17E-05</td>
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</table>

6.9 Evaluation of the sensitivity to radiation of SRAM-based FPGAs

Members: G. Foucard, A. Bocquillon, R. Velazco

The increasing popularity of low-cost safety-critical computer-based applications in a large scope of areas (such as space and avionics, automotive, biomedical, telecontrol, etc.) requires the availability of new circuits and methods for designing dependable systems. In particular, in the areas where computer-based dependable systems are currently being introduced, the cost (and hence the design and development time) is often a major concern, and the adoption of commercial reconfigurable hardware, such as SRAM-based FPGAs (Field Programmable Gate Arrays) is a common practice. As a result, software implemented fault tolerance is an attractive solution for this class of applications, since it allows the implementation of dependable systems without incurring the high costs coming from designing custom hardware or using hardware redundancy.

Despite these attractive characteristics, designers are reluctant to use these components for critical applications due to their sensitivity to Single Event Upsets (SEUs) provoked by radiation. All SRAM-based FPGA resources are controlled by its configuration memory, an SEU in this area may thus change the original behaviour of the application. Moreover a fault affecting this memory is permanent until the device is configured again.

Quantifying the sensitivity of the configuration memory is therefore mandatory in order to evaluate the sensitivity of a specific application. These researches focused on the methods and tools to evaluate the potential weaknesses of fault-tolerant applications when implemented in SRAM-based FPGAs. A TMR (Triple Modular Redundancy) architecture of a crypto-processor was selected and implemented in a Virtex II. The HIF (Heavy Ion Facility) cyclotron of UCL was used to put in evidence the significant contribution of the SRAM configuration memory to the sensitivity of any application implemented on a SRAM-based FPGA. The static cross-section was obtained and combined with the results of fault injection experiments, this to predict the error-rates of the implemented fault-tolerant crypto-processor which were classified in three main families of outputs: error detected, falsely detected error (the result was correct but the TMR output corresponds to detected an error) and undetected errors (the TMR issued an error not seen by the voter).

The final results of these experiments, presented in 2010 at NSREC and published at IEEE TNS, are depicted in Table 3 and show that the maximum underestimation factor being less than 2. This difference might be the result of MBUs not being considered in the fault injection campaign. Falsely detected errors follow a reverse trend: the prediction overestimates the measure by a factor close to 5. This could be explained by the small number of errors of this type observed during radiation ground testing. It is important to note that in such a case, the prediction is certainly closer to the reality than the measure.
Table 3. Measured vs. predicted error rates for the TMR implemented in the studied FPGA

<table>
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<tr>
<th>Error rate</th>
<th>Particles</th>
<th>Detected errors</th>
<th>Falsely detected errors</th>
<th>Undetected errors</th>
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<tr>
<td>Measured</td>
<td>Carbon</td>
<td>1.04x10^-4</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td></td>
<td>Argon</td>
<td>2.84x10^-7</td>
<td>6.67x10^-6</td>
<td>7.78x10^-5</td>
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<tr>
<td>Predicted</td>
<td>Carbon</td>
<td>9.53x10^-5</td>
<td>1.55x10^-6</td>
<td>2.09x10^-6</td>
</tr>
<tr>
<td></td>
<td>Argon</td>
<td>1.94x10^-5</td>
<td>3.16x10^-5</td>
<td>4.25x10^-5</td>
</tr>
</tbody>
</table>

The TMR crypto-core application was implemented in an experiment, so-called COTS, accepted to be included in the payload of the LWS (Living With a Star) satellite of NASA. The results obtained in flight, launch scheduled October 2012, will be confronted to those issued from radiation ground testing and fault injection experiments as well as to those predicted by MUSCA SEP3 simulator. Figure 6.3 depicts the flight version of the SET (Space Environment Testbed), in which the one of the left is the COTS experiment developed at TIMA/ARIS around the TMR crypto-core implemented in the Virtex II FPGA experiment.

Figure 6.3  The SET experiment included in the payload of NASA LWS (Living With a Star) satellite
7. Members of TIMA

Table 1 lists researchers, Ph D. students, engineers and clerical staff present in the TIMA Laboratory in 2009 and 2010. Table 2 lists the invited researchers. Table 3 lists the interns and trainees, including MSc students.

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Table 2 – Visitors (for 2009 and 2010)

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<td>GAUDE</td>
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<td>France</td>
<td>6 months</td>
</tr>
<tr>
<td>GRONDIN</td>
<td>Jérôme</td>
<td>France</td>
<td>3 months</td>
</tr>
<tr>
<td>HAMAYUN</td>
<td>Mian Muhammad</td>
<td>Pakistan</td>
<td>7 months</td>
</tr>
<tr>
<td>IDBAHMANE</td>
<td>Soufiane</td>
<td>Morocco</td>
<td>6,5 months</td>
</tr>
<tr>
<td>IGA</td>
<td>Rodrigo</td>
<td>Chili</td>
<td>5 months</td>
</tr>
<tr>
<td>JULLIEN</td>
<td>Audrey</td>
<td>France</td>
<td>2 months</td>
</tr>
<tr>
<td>KUMAR</td>
<td>Kavita</td>
<td>France</td>
<td>2 months</td>
</tr>
<tr>
<td>LARABA</td>
<td>Asma</td>
<td>Algeria</td>
<td>5,5 months</td>
</tr>
<tr>
<td>LETONDEUR</td>
<td>Loic</td>
<td>France</td>
<td>2,5 months</td>
</tr>
<tr>
<td>MAALI</td>
<td>Abderraouf</td>
<td>Tunisia</td>
<td>3,5 months</td>
</tr>
<tr>
<td>MALLE</td>
<td>Anthony</td>
<td>France</td>
<td>5 months</td>
</tr>
<tr>
<td>MASSON</td>
<td>Florian</td>
<td>France</td>
<td>5 months</td>
</tr>
<tr>
<td>MICHEL</td>
<td>Luc</td>
<td>France</td>
<td>4 months</td>
</tr>
<tr>
<td>MISHINA</td>
<td>Anna</td>
<td>Russian</td>
<td>2 months</td>
</tr>
<tr>
<td>NOVOTNY</td>
<td>Filip</td>
<td>Czech Republic</td>
<td>5 months</td>
</tr>
<tr>
<td>PATASKAR</td>
<td>Vishal</td>
<td>India</td>
<td>4,5 months</td>
</tr>
<tr>
<td>POSTE</td>
<td>Nicolas</td>
<td>France</td>
<td>3 months</td>
</tr>
<tr>
<td>PROLONGE</td>
<td>Romain</td>
<td>France</td>
<td>2 months</td>
</tr>
<tr>
<td>PROST-BOUCLE</td>
<td>Adrien</td>
<td>France</td>
<td>5 months</td>
</tr>
<tr>
<td>REYMOND</td>
<td>Vincent</td>
<td>France</td>
<td>4 months</td>
</tr>
<tr>
<td>RIBEIRO</td>
<td>Jérémy</td>
<td>France</td>
<td>3 months</td>
</tr>
<tr>
<td>ROCTON</td>
<td>Benjamin</td>
<td>France</td>
<td>3 months</td>
</tr>
<tr>
<td>SINGH</td>
<td>Abhinav</td>
<td>India</td>
<td>3,5 months</td>
</tr>
<tr>
<td>SOREZ</td>
<td>Clément</td>
<td>France</td>
<td>6 months</td>
</tr>
<tr>
<td>YANG</td>
<td>Bo</td>
<td>China</td>
<td>5 months</td>
</tr>
<tr>
<td>YAO</td>
<td>Ziqing</td>
<td>China</td>
<td>6 months</td>
</tr>
<tr>
<td>ZORGATI</td>
<td>Mohamed</td>
<td>Bechir</td>
<td>Tunisia</td>
</tr>
</tbody>
</table>

Table 3 – Trainees (for 2009 and 2010)
8. Academic and research members

AMBLARD Paul

Position: Associate Professor (Maître de Conférences) at University Joseph Fourier, Grenoble, UFR Informatique et Mathématiques Appliquées.
He passed away December 15, 2010

Education
1984 PhD Computer Science
1976 Master of Science in Mathematics

Past activities
October 1997 Joined TIMA Laboratory
From 1984 Associate Professor at University Joseph Fourier
From 1973 to 1982 Teacher of Mathematics in secondary school

ANGHEL Lorena

Position: Professor at Grenoble Institute of Technology, Phelma(Physique-Electronique- Matériaux)

Education
1996 : Microelectronic Engineering degree - at Polytechnic University of Bucharest, Romania
1997 : MS degree in Microelectronics – UPB, Romania
2000 : PhD in Microelectronics (INP Grenoble)
2007 : Diploma of "Habilitation à Diriger des Recherches" in EEATS

Past activities
Assistant Professor (ATER) at UJF (Université Joseph Fourier Grenoble) in 2000
Visitor researcher in Zenasis Technologies, USA, July-October 2005
Visitor Researcher in Intel Corp, USA, July-October 2005

Research interests
Test and On Line testing, Defect and fault tolerant techniques, computer architecture, nanotechnologies

Current responsabilities
Researcher in the ARIS group,
Coordinator of ACI-SI project VENUS in collaboration with IMS (Bordeaux, France), 2004-2007.
Scientific Coordinator of Catrene Optimise roject 2009-2013
Scientific Leader of TIMA in MEDEA+ Parachute European program 2004-2009
Scientific Leader of TIMA in Catrene 3DIM3 European program 2009-2012
General Co Chair of European Test Symposium, May 2011, Trondheim, Norway
University Booth Chair DATE 2011, Grenoble, France
Program Chair of Design of Circuits and Integrated Systems (DCIS 2008), November, 2008, France
Program Chair of IEEE Design for Reliability and Variability (DRVW 2008), October 2008, USA
Program Chair of 4th Summer School on Radiation Effects, December 2008, Florida, USA
Program Chair of 3rd Summer School on Radiation Effects, Novembre 2007, Buenos Aires, Argentina
Program Chair of 2nd Summer School on Radiation Effects, Novembre 2006, Sevilla, Spain
General Chair of 11th International On Line Testing Symposium July 2005, France
BASROUR Skandar

Position: Professor in Electronics and Microsystems at Ecole Polytechnique de l’Université de Grenoble (Polytech’G). Electrical Engineering Department (3I)

Education
1987-1990: PhD in Microelectronics – Université Joseph Fourier de Grenoble
1986-1987: DEA in Microelectronics – Université Joseph Fourier de Grenoble
1982-1986: Graduated from Ecole Normale Supérieure of Tunisia (Physics and Chemistry)

Past activities
2001: Assistant Professor in Electronics and Microsystems at the Université de Franche-Comté (Topics Contribution to the development of the X ray LIGA technique in France. Development and improvement of the UV LIGA Techniques for the realization of original Microsystems)
1991-992: Postdoctoral situation at the Laboratoire de Microstructures et Microélectronique CNRS – Bagneux (Topics: Fabrication and characterization of submicron gated TEGFET’s)

BENABDENBI Mounir

Position: Associate Professor at Grenoble-INP PHELMA (Physique-Electronique- Matériaux) since 2009

Education
2002: PhD in Microelectronics, University Pierre and Marie Curie (UPMC) in Paris
1998: DEA degree in Computer Science, University Montpellier 2

Past activities
2003-2009: Associate Professor at University Pierre and Marie Curie (UPMC) in Paris. Head of VLSI Test related research activities at LIP6 laboratory (Laboratoire d’Informatique de Paris 6)
2002-2003: Researcher at the LIP6 laboratory

Research interests
Test and On Line testing, Defect and fault tolerant techniques, computer architecture, nanotechnologies

Current responsibilities
Participation since 2008 to the French program ANR ADAM (Adaptive and Dynamic Architecture for MP²SoC). Participation since 2009 to the European Catrène Project 3DIM3 related to the design and Test of stacked 3D chips.

Miscellaneous
Has served in many Conference and Workshop Committees

BONVILAIN Agnès

Position: Associate Professor (Maître de Conférences) in electronics at Ecole Polytechnique de l’Université Joseph Fourier de Grenoble (Polytech’G), Electrical Engineering Department (3I and E2I).

Education
2002: PhD in control and informatics – Université de Besançon
1988: DEA in Control, Informatics and robotics – Université de Besançon

Past activities
September 2005: Joined TIMA Laboratory
From 1997 to 2002: Researcher in microrobotics at LAB laboratory, Besançon
From 1993 to 2005: Teacher in electronics in secondary school
From 1988 to 1993: Engineer head of service in two companies

Research interests: BioMEMS
BORRIONE Dominique

Position: Professor at Université Joseph Fourier, Grenoble
Director of TIMA Laboratory since January 2007

Education
1981: Doctorat d’Etat in Computer Science, University of Grenoble
1976: PhD in Computer Science, University of Grenoble
1971: DEA in Computer Science, University of Grenoble
1970: B. S. in Applied Mathematics, Aix-Marseille University

Past activities
Director of the ARTEMIS Laboratory (1991-1995)

Miscellaneous
Has served in many Conference and Workshop Committees
IFIP Silver Core

FESQUET Laurent

Position: Associate Professor (Maître de conférence) at Grenoble INP

Education
2008: HDR in microelectronics – Grenoble Institute of technology
1997: PhD in Electronics – Paul Sabatier University – Toulouse
1994: Agrégation (teaching degree) in applied physics, Ecole Normale Supérieure de Cachan
1993: Engineering degree in Physics, Ecole Nationale Supérieure de Physique de Strasbourg
1993: DEA degree in Photonics – Louis Pasteur University – Strasbourg

Past activities
Research:
1995-1999: Researcher at LAAS-CNRS in Toulouse
Teaching:
1998-1999: Teacher in charge of physics, electrotechnics and power electronics curses in BTS - Brive
1995-1998: Teacher in electronics at the ENSAE (Sup'Aéro) and at the Paul Sabatier University - Toulouse
1994-1995: Teacher at the French Navy instruction center in Toulon in charge of electronics and inertial navigation systems lectures

Current responsibilities
Deputy Director of the CIME-Nanotech
Head of the « Concurrent Integrated Systems » research group (CIS)
Founder and Chair of the french IEEE-SSCS Chapter (Solid-State Circuit Society)

Miscellaneous
Co-program chair of SampTA in 2011
Tutorial Chair of IEEE ASYNC in 2010
Co-general chair of SampTA in 2009
Member of the ASYNC, DATE, SampTA and DCIS program committees
As served in many conference organizations
GASCARD Eric

**Position:** Associate Professor with TIMA Laboratory since September 1st, 2003

**Education**
Ph.D. in Computer Science from University Provence (Aix-Marseille 1), France, 3 July 2002

**Current responsibilities**
Associate Professor University Joseph Fourier (Grenoble 1), UFR, Polytech'Grenoble, France, since September 1, 2003

LEVEUGLE Régis

**Position:** Professor at Grenoble INP (Phelma), vice-director of TIMA laboratory

**Education**
1987 - Engineer Degree from ENSERG (INPG)
1987 - DEA Degree in Microelectronics (Grenoble)
1990 - PhD in Microelectronics (INPG)
1995 - Habilitation à Diriger des Recherches (French National Degree for Research Supervising)

**Past activities**
Director of Studies at the INPG Telecommunications Department between 2001 and 2003

**Research interests**
Computer architecture, VLSI design methods, dependability analysis, fault-tolerant architectures, concurrent checking, secure circuits

**On-going research activities and collaborations**
- Projects on multi-level fault injections and high level dependability analysis of complex VLSI circuits and FPGAs. Collaborations with STMicroelectronics, EADS, Airbus, Atmel (several national and industrial projects). Participation to the ANR-07-SESU-006 project FME3 on formal approaches in collaboration with LIP6 (Paris, France), 2008-2010.
- Project on the hardening of digital circuits, SRAM-based FPGA designs and embedded systems by modification of high level hardware descriptions and/or operating system functions. Collaborations with EADS, Airbus, Atmel (CATRENE European project "Optimise").
- Projects on secure chip design and cryptographic IPs resistant to attacks. Collaborations with CS-SI (national projects).

**Miscellaneous**
- Authored or co-authored more than 150 scientific papers in journals, books, conferences and workshops.
- Served in more than 70 conference committees - General co-Chair for DFT'02, vice General Chair for IOLTW'02, Program co-Chair for DFT'01, IOLTS'04 and IOLTS'06, and vice Program Chair for IOLTS'03, IOLTS'05 and IOLTS'07.
### MAISTRI Paolo

**Position**: Chargé de Recherche CNRS (French National Center for Scientific Research) since 2008  

**Education**  
2001 – Master of Science in Computer Science and Electrical Engineering at University of Illinois at Chicago (UIC), Chicago (IL), USA  
2001 – Master of Science in Computer Engineering at Politecnico di Milano, Milan, Italy  
2006 – PhD in Computer Engineering at Politecnico di Milano, Milan, Italy  

**Past activities**  
Contract researcher at Politecnico di Milano, Milan, Italy from 2002 to 2003  
Post-Doc researcher at TIMA Laboratory from 2006 to 2008  

**Research interests**  
Cryptographic implementations, secure design, countermeasures against side-channel fault analysis  

**Miscellaneous**  
Member of the ARIS group.  
Author or co-author of about 27 scientific papers in journals, books, conferences and workshops.

### MANCINI Stéphane

**Position**: Associate Professor at TIMA/Grenoble INP-ENSIMAG  

**Education**  
− 2000 : Phd in Electronics and Telecommunication – Telecom Paris, France  
− 1996 : Engineering degree in Electronics and Telecommunication – Telecom Paris, France  
− 1996 : DEA (Master) degree in Computer Science – Université Pierre et Marie Curie, Paris, France  

**Past activities**  
2001-2010 Associate professor at GIPSA Lab/Grenoble INP-ENSIMAG  

**Research interests**  
SoC architecture, Memory hierarchy, ESL & CAD Tools, AAA (Algorithm Architecture Adequacy/matching), Embedded multimedia systems (3D, vision)  

**Current responsibilities**  
Researcher in the SLS(System Level Synthesis) group  

**Miscellaneous**  
- Member of the DASIP conference steering committee  
- Has organized the first DASIP conference at GRENOBLE, in 2008

### MIR Salvador

**Position**  
CNRS Research Director (French National Center for Scientific Research); Vice-director of TIMA Laboratory; Leader of the RMS Group at TIMA (Reliable Mixed-signal Systems)  

**Education**  
2005: Habilitation à diriger des recherches, Institut National Polytechnique de Grenoble, France  
1993: Ph.D. degree - Computer Science, University of Manchester, United Kingdom  
1989: Master degree - Computer Science, University of Manchester, United Kingdom  
1987: Industrial Engineering degree - Electrical, Polytechnic University of Catalonia, Barcelona, Spain  

**Publications**  
Over 150 scientific papers in international journals and conferences
Editor of two books on silicon Microsystems

Conference organization
- General chair of IFIP/IEEE VLSI-Soc’06, IEEE IMSTW’05
- Program chair of IFIP/IEEE VLSI-Soc’11
- Program co-chair of IEEE IMS3TW’08, IEEE IMSTW’04
- Local Arrangements chair of IEEE DATE’11, IEEE WTW’05
- Member of the Executive Committee of IEEE DATE (2011)
- Chair of the Steering Committee of IFIP/IEEE VLSI-Soc (2010-2011)
- Member of the Steering Committee of IFIP/IEEE VLSI-Soc (2007-2010)

Miscellaneous
- Member of IEEE, IEEE Computer Society and IEEE Circuits and Systems Society
- Member of the IFIP Working Group 10.5
- Participation in the European projects SMART, JESSI-COMMON-FRAME, ARCHIMEDES, AMATIST, PROFIT, TECHNOBAT, PICS, NANOTEST, TOETS
- Regular reviewer for International Journals and Conferences and Government agencies (NSF-USA, ANVAR-France, ANEP-Spain, AGAUR-Spain …)

Distinctions
- Best paper award in 18th IFIP/IEEE International Conference on VLSI (VLSI-Soc’10, acceptance rate < 30%)
- Best paper award in 14th IEEE European Test Symposium (ETS’09, acceptance rate < 25%)
- Award of excellence Jean-Pierre Noblanc 2006 in recognition of outstanding work on the MEDEA+ Project A406 PICS
- Award from Association of Industrial Engineers of Catalonia, Spain, to the best Work Graduation Dissertation in Industrial Engineering, Barcelona, 1988

MORIN-ALLORY Katell

Position: Associate Professor (Maître de conférence) at ENSERG (Ecole Nationale Supérieure d'Electronique et Radioélectricité de Grenoble)

Education
- 2004: PhD in Computer Science, Université de Rennes 1, France
- 2000: DEA degree in Computer Science, Université de Rennes 1, France
- 2000: Magistère of Mathematic Modelisation and Computer Science Method, Université de Rennes 1, France

Current responsibilities
- Researcher in the VDS (Verification and Modeling of Digital Systems) group

MULLER Olivier

Position: Associate Professor at Ensimag (École Nationale Supérieure d'Informatique et de Mathématiques Appliquées) of the Grenoble Institute of Technology

Education
- 2007: PhD in Computer Science, Université de Bretagne-Sud and ENST Bretagne, France
- 2004: DEA degree in electronics, ENST Bretagne, France
- 2004: Engineer Degree from ENST Bretagne, France

Current responsibilities
- Researcher in the SLS(System Level Synthesis) group
NICOLAIDIS Mihail

Position: Research Director at the French National Research Centre

Education
Doctor-Engineer degree - Design of self-testing integrated circuits for analytical failures hypotheses 1986

Miscellaneous
Michael Nicolaidis is research Director at the CNRS and co-leader of the ARIS group (Architectures for Complex and Robust Integrated Systems) at TIMA Laboratory.
His research interests include VLSI testing, DFT, on-line testing, fault tolerant design, design for yield, reliability, variability and low-power in nanometric technologies, fault tolerant approaches for nano-technologies, design of robust single-chip massively parallel tera-device processors, and computational physics.
He has 204 Cited Publications and 3568 Citations (Google Scholar citations gadget).
He is author of one book and editor of two books and several journal special issues.
He authored 21 international patents and developed the memory BIST synthesis approach and the programmable memory BIST architecture licensed to two EDA industry leaders.
He is member of the editorial board of the IEEE Design & Test of Computers since 2005.
He was Program Chair and General Chair of the IEEE VLSI Test Symposium and is currently member of its Steering Committee.
He founded the IEEE International On-Line Testing Symposium and was his General Co-chair from 1995 to 2011.
He was Vice-Chair of the Test Technology Technical Council (TTTC) of the IEEE Computer Society at 2009 and 2010.
He received twice the Best Paper Award of the Design and Test in Europe Conference, and once the Best Paper Award of the IEEE VLSI Test Symposium.
One of his papers was selected among the most influential papers of the 10 years of DATE.
He received the Meritorious Service Award of the IEEE Computer Society and is a Golden Core member of the IEEE Computer Society.
He is founder of iRoC Technologies.
- He is co-founder of iRoC Technologies.

PÉTROT Frédéric

Position: Professor in Computer Architecture at the École Nationale Supérieure d'Informatique et de Mathématiques Appliquées (ENSIMAG) of the Institut Polytechnique de Grenoble

Education
2003: Habilitation à Diriger des Recherches - Université Pierre et Marie Curie, Paris, France
1994: PhD in Computer Science - Université Pierre et Marie Curie, Paris, France
1989: DEA (Master) degree in Computer Science - Université Pierre et Marie Curie, Paris, France

Current responsibilities
Head of the System Level Synthesis group.

Past activities
1994-2004 : Associate Professor at Université Pierre et Marie Curie (Paris VI), France. Major contributor to the Alliance CAD System and to the Disydent digital system design environment.
### PIERRE Laurence

**Position:** Professor in Computer Science at Université Joseph Fourier, Grenoble

**Education**
- 1999 : HDR ("Habilitation à Diriger des Recherches"), Université de Provence, Marseille, France
- 1990 : PhD in Computer Science, Université de Provence, Marseille, France
- 1986 : DEA degree in Computer Science, Université de Provence, Marseille, France

**Current responsibilities**
Leader of the VDS (Verification and Modeling of Digital Systems) group

**Past activities**
- 1991-2002 : Associate Professor at Université de Provence, Marseille
- 2002-2008 : Professor at Université de Nice Sophia-Antipolis

### ROUSSEAU Frédéric

**Position:** Professor at UJF (Joseph Fourier University), Grenoble, researcher at TIMA lab

**Education**
- 2005: “Habilitation à diriger des recherches”, TIMA lab, University Joseph Fourier, France
- 1997: Ph.D. in computer science from the University of Evry, France
- 1992: DEA degree in Computer Science, INPG, Grenoble, France
- 1991: DEA degree in Microelectronics, University Joseph Fourier,
- 1991: Master degree, computer science and electrical engineering (3i), University Joseph Fourier, Grenoble, France,

**Past activities**
- 1999 – 2007 Assistant professor at UJF (Joseph Fourier University), Grenoble, researcher at TIMA lab
- 1996 – 1999 Teacher – Researcher at the engineer school of Marseille (ESIM), France in the computer science and electrical engineering department.

**Current responsibilities**
Researcher in the « System Level Synthesis » group (SLS) in the following fields:
- Hardware/software communication interface design
- Low level software and HW/SW interface

### RUFER Libor

**Position:** Researcher / Expert in Microsystems and Test with TIMA

**Education:**
- 2007: Habilitation à Diriger des Recherches - Joseph Fourier University, Grenoble
- 1993: Diplôme d'Etudes Approfondies en Acoustique - Ecole Centrale de Lyon
- 1984: Ph.D. in Acoustics - Czech Technical University, Prague
- 1974: Engineer degree - Faculty of Electrical Engineering, Prague

**Past activities:**
- 1994 - 2004: Associated Professor, Joseph Fourier University, Grenoble
- 1997 - 1999: Invited Researcher, Acoustics Laboratory of School for Building, Concordia University, Montreal, Canada
1992 - 1993: Invited Researcher, Centre Acoustique, Ecole Centrale de Lyon
1980: Research Fellow, Acoustics Laboratory, Danish Technical University, Lyngby
1976 - 1993: Associated Professor, Czech Technical University, Prague

Current responsibilities:
- PHC - PROCORE project leader (partner: Hong Kong University of Science and Technology), 2009-2010.
- PHC - STEFANIK, project leader (partner: Academy of Science, Institute of Electrical Engineering, Slovak Republic), 2010-2011.
- FP7 - MORGaN, UJF partner leader (24 partners), 2008-2011.

Research interests:
MEMS-based sensors and actuators, electro-acoustic and electro-mechanical transducers modelling and design, RF MEMS.

Miscellaneous:
Memberships: IEEE (Senior Member), Audio Engineering Society (USA), Société Française d'Acoustique.

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SHEIBANYRAD Abbas (Hamed)

Position : CNRS Research Fellow since 2009, SLS Team

Education
2008: PhD in Microelectronics, LIP6 (UPMC), Paris
2004: Masters (DEA) in Microelectronics, UPMC, Paris
2000: Computer Hardware Engineering, Tehran Polytechnic University, Tehran

Past activities
2008-2009: Postdoctoral Research Fellow, TIMA Laboratory, Grenoble
2000-2003: R&D Research Engineer, Vaf Corp., Tehran

Research interests
SoC (System-on-Chip) Architecture, NoC (Network-on-Chip) Design, 3D-Integration and 3D Topologies, GALS Approaches and Asynchronous Circuit design

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SICARD Gilles

Position : Associate Professor (Maître de conférence HDR) at UJF (Joseph Fourier University), Grenoble

Education
1999 : PhD in Microelectronics, INPG.
1994 : DEA degree in Microelectronics, INPG.

Past activities
Contractual teacher (ATER) at ENSERG (Ecole Nationale Supérieure d'Electronique et Radioélectricité de Grenoble) and researcher at LIS Laboratory (Laboratoire des Images et des Signaux), Grenoble, 1999.

Current responsabilities
Co-Leader of the « Concurrent Integrated Systems » research group (CIS)

Current Research Interests:
New architectures of CMOS Vision Sensors (with High Dynamic range capability, or Light adaptive systems)
- Electromagnetic Compatibility in integrated circuits (Design of Asynchronous circuits with low-emission capability and a high immunity)
- Low-Power Asynchronous circuits (Design of Low-power and low-leakage corelib for asynchronous circuits)

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**SIMEU Emmanuel**

**Position:**
Associate Professor at École Polytechnique de l'Université de Grenoble (Polytech’G); Director of CIM (Computer Integrated Manufacturing) Platform of API-PRIMECA Dauphiné Savoie

**Education**
- 2005 DHDR (Diplôme d'Habilitation à Diriger des Recherches) in Physics, Joseph Fourier University of Grenoble
- 1992 Ph.D in Automatic Control and System Theory, Institut National Polytechnique de Grenoble
- 1988 DEA degree in Automatic Control and Signal Processing, Institut National Polytechnique de Grenoble
- 1987 Electrical Engineer Degree - University of Casablanca (Morocco)

**Current responsibilities**
Member of the Reliable Mixed -signal Systems (RMS) Group

**Past Activities**
- 1992-1995: Associate Professor at ISAR (Institut Supérieur d'Automatique et de Robotique de Valence)
- 1988-1995: Researcher in LAG (Laboratoire d'Automatique de Grenoble)
- 1989-1992: Researcher in CNET-CNS Grenoble (SITAR Project)

**Miscellaneous**
Pedagogic responsibility in the department of industrial risk management of Polytech’Grenoble.
Courses and lectures at of Polytech’Grenoble on Reliability Analysis Tools
- Automatic Control
- Statistic Methods
- Supervision and Statistical Process Control
- Multivariate Data Analysis

**STRATIGOPOULOS Haralampos**

**Position:** Chargé de Recherche CNRS (French National Center for Scientific Research) since 2007

**Education**
- Ph.D., Yale University, USA, Engineering and Applied Science Department, Dec 2006
- M.S. in Electrical Engineering, Yale University, USA, Engineering and Applied Science Department, May 2003
- Diploma in Electrical and Computer Engineering, National Technical University of Athens, Greece, June 2001

**Current responsibilities**
Member of the Reliable Mixed -signal Systems (RMS) Group

**Research Interests**
Analog/Mixed-Signal/RF circuit design and test, machine learning, neuromorphic solid-state circuits, built-in self-test, concurrent error detection, computer-aided design

**Miscellaneous**
- Program Chair at IEEE TVHSAC ‘10 and IEEE IMS3TW’11
- TPC member at DATE, IMS3TW, IOLTS
- Member of the Test Technology Technical Council (TTTC) Student Activities Group
- Guest Editor of the 2011 Special Issue on Analog, Mixed-Signal, RF, and MEMS Testing published at the Springer Journal of Electronic Testing: Theory & Applications (JETTA)
- Best Paper Award at IEEE ETS’09
VELAZCO Raoul

Position: Research Director at the French National Research Agency (CNRS); Researcher with TIMA laboratory since 1996

Education:
1990 Dr. ès Sciences from INPG (Institut National Polytechnic of Grenoble)
Test and diagnosis of programmable integrated circuits
1982 Doctor-Engineer Degree from INPG:
Génération Automatique de programmes de test de microprocesseurs (INPG)
1979 Engineer degree
1976-1979 National School for Informatics and Applied Mathematics (ENSI MAGIC) Grenoble

Research Activities:
Radiation effects on integrated circuits and systems, methods and tools for the study of the sensitivity to radiation of complex integrated circuits, mitigation techniques, real-life (balloons, planes, satellites) experiments.

Current Responsibilities:
- Co-Leader of the ARIS research group of TIMA laboratory
- Member of the Scientific Committee of TIMA since 1998
- Responsible of the design of a flight experiment included on board a scientific satellite: NASA Project LWS/SET (Living With a Star / Space Environment Testbed).
- Expert Radiation at CNRS

Miscellaneous:
- He was leader at TIMA of the Circuit Qualification (QLF) research group until the end of 2000.
- Author or co-author of more than 180 scientific publications 35 at IEEE Transactions on Nuclear Sciences.
- He developed and patented a new memory cell (HIT cell) robust with respect to the transient effects of radiation, licensed to an industrial leader of the radiation hardened circuits.
- Coordinator from 2006 to 2010 of European ALFA (Amérique Latina Formación Académica) “NICRON” Project.
- Co-founder in 2000 of iRoC Technologies and of PULSCAN in 2008

ZERGAINOH Nacer-Eddine

Position: Associate Professor (Maître de Conférences) in Computer Engineering and architecture, Ecole Polytechnique (Polytech’G), Joseph Fourier University, Grenoble

Education
1984 Baccalaureat degree, Mathematics
1989 Engineer degree, Telecommunication. National School of telecommunication
1990 DEA degree, Signal Processing & Control, Signals and Systems Laboratory, Supélec.
1996 PhD degree, Computer Engineering, INRIA & Paris XI University, France
Methods and tools-aided design of reactive systems. Distributed Real-time Operating System for an embedded obstacle detection system.

Past activities
Participated to the European Esprit-Polyglot Project.
Participated to the European Prometheus Project.
Teacher in telecom and computer (ESIGITEL, EPITA, Paris XIII University).
Contractual engineer of research with LIMSI-CNRS Laboratory Gif/Yvette.  

**Current responsibilities**  
Researcher in System Level Synthesis Group of TIMA Laboratory.  
His research interests include system-level design and CAD issues, multiprocessor architectures modeling, and real-time operating system. Currently, his research focuses on multiprocessor architectures exploration, RTOS, and interface Synthesis.

**Miscellaneous**  
Has authored or co-authored several scientific papers.  
Has served in many program committees of conferences and workshops  
Has served as a reviewer of many journals and conferences
9. Staff members

BEN TITO Laurence

Position: Executive Secretary at TIMA Laboratory since March 2010

Education:
2002: Certificate in Advanced English » (Cambridge University Diploma, evening courses)
1994: BTS Executive Secretary (= 2-year technical degree)
1991: DEUG of Philosophy (= second-year University Diploma)
1989: Bac A1

Current responsibilities:
Executive Secretary

CHEVROT Frederic

Position: Contracted technician with TIMA Laboratory since March 2003

Education:
1998: DEUG Technologie Industrielle, Université Joseph Fourrier.
1995: BAC S Tec

Current responsibilities:
Assistant System Engineer

CORREARD Julie

Position: In charge of communication on part-time training since September 2009 to obtain a master degree in communication.

Education:
2010: Licence en marketing and DEESMA, ECORIS, Chambéry
2008: BTS Communication des entreprises, WESFORD, Grenoble
2005: BAC STT, Grenoble

Past Activities:
September 2008 to July 2010: Administrative and multimedia coordinator on ALFA NICRON Project at TIMA.

Current responsibilities:
Communication and web tasks at TIMA Laboratory since September 2009.
Special event management.
FOURNERET-ITIE Anne-Laure

**Position**: Personnel officer since September 2003

**Education**:
2004-2006: Diplôme CNAM (DESS) « Responsable de l’administration et de la gestion du personnel »
1997: Licence d’Administration Publique, UPMF, Saint Martin d’Hères

**Current responsibilities**:
Personnel officer and special event manager

GARNIER Nicolas

**Position**: Contractual Engineer at TIMA Laboratory since February 2006 and Engineer CNRS since December 2007

**Education**:
2005: Formation Sécurité des Systèmes et Réseaux, CNRS, Grenoble
2003: Maîtrise d’informatique, Université de Savoie, Le Bourget du Lac

**Past Activities**:
November 2004 to February 2006: System Engineer at Laboratoire Modélisation et Calculs, Grenoble

**Current responsibilities**:
System Engineer at TIMA Laboratory

KHALID Ahmed

**Position**: Contractual technical officer at TIMA Laboratory since September 1996; technical officer INPG since 1999 and Technical Assistant Grenoble INP since 2007

**Education**:
2007: Bac (DAEU option B) option Mathematical
1995: BEP ACC (business administration and accounting)

**Current responsibilities**:
System Technician at TIMA Laboratory

MARTINEAU Sophie

**Position**: Accountant specialized in Travelling/Missions and French teacher

**Education**:
2008: DAEFLE, Alliance Française Paris
1997: BTS Assistant de Direction, lycée Edgar Quinet, Bourg en Bresse

**Current responsibilities**:
In charge of all the Missions/Travelling administrative points and french teacher for foreign PhD students
<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Education</th>
<th>Past Activities</th>
<th>Current responsibilities</th>
</tr>
</thead>
<tbody>
<tr>
<td>PANCHER Fabrice</td>
<td>CNRS Research Engineer at TIMA since June 2010</td>
<td>1997: Engineering degree in Industrial Computer Science and Instrumentation (Polytech Grenoble)</td>
<td>2008-2010: Software Technical Leader at Texas Instruments (Monterrey, Mexico)</td>
<td>Software developments for TIMA’s research groups</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1994: Preparation to engineering schools</td>
<td>1998-2007: Research engineer at Laboratoire de Physique Subatomique et de Cosmologie (CNRS-IN2P3) (Grenoble, France)</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>1997-1998: Software engineer at Snaketech (Voiron, France)</td>
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</tr>
<tr>
<td>RAJAB Youness</td>
<td>Technician at TIMA Laboratory since September 2008</td>
<td></td>
<td></td>
<td>In charge of all accounting expenses of TIMA laboratory</td>
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<tr>
<td>SALIZZONI Marie-Christine</td>
<td>Accountant ADR at TIMA since January 2000</td>
<td>1983 : DESE (Diplôme d’Etudes Supérieures en Economie) CNAM Grenoble, spécialité comptabilité et gestion</td>
<td></td>
<td>Accounting of TIMA Laboratory; budgets; contracts</td>
</tr>
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</tr>
</tbody>
</table>
TORELLA Lucie

Position: Adjoint Technique de Recherche et de Formation (UJF) at TIMA since 1997.

Education:
BEP Secrétariat

Current responsibilities:
Secretary / Publications

VITRY Gérard

Position: "Ingénieur d'Etudes" at CNRS. He retired in July 2010

Education:
1973: "Programmeur Expert en Systèmes Informatiques" – Grenoble

Current responsibilities:
System Engineer; Web administrator
10. Ph. D. candidates

- **ABBAS, Hassan**
  - Title of thesis: Design of CMOS color image sensors inspired by human vision
  - Expected date of defense: 2014
  - Previous degrees: M2R Micro-NanoElectronique (MNE)

- **ABDALLAH, Louay**
  - Title of thesis: Built-In Self-Test of RF front-ends
  - Expected date of defense: 2011
  - Previous degrees: Master 2 Micro Nano Électronique - Université Joseph Fourier; Master 1 Électronique - Université Libanaise – Liban

- **ABOUZEID, Fady**
  - Title of thesis: Subthreshold architecture and digital circuits study in submicron CMOS technology
  - Completed in November 18, 2010
  - Previous degrees: Master Micro Nano Électronique (2007)

- **AKKOUCHE, Nourredine**
  - Title of thesis: Techniques of statistical modelling of analogue and mixed circuits for the optimization of the production test
  - Expected date of defense: 2011
  - Previous degrees: Master in Applied Mathematics

- **ALHAKIM, Rshdee**
  - Title of thesis: Optimisation des Performances de Réseaux de Capteurs Dynamiques par la Contrôle de Synchronisation dans les Systèmes Ultra Large Bande
  - Expected date of defense: 2012
  - Previous degrees: Master (2007)

- **ALSAYEG, Khaled**
  - Title of thesis: Clockless microcontrol
  - Completed in September 01, 2010
  - Previous degrees: Master 2 Research "Micro and nano electronics (MNE)". INPG-UJF, Grenoble, France (2006); Engineer in electronics, Damascus university, Syria (2001)

- **AMHAZ, Hawraa**
  - Title of thesis: Low level image processing integrated in a CMOS image sensor
  - Expected date of defense: 2011
  - Previous degrees: Master 2 "Micro and Nano Electronics" (UJF Grenoble)

- **ARTHAUD, Yoann**
  - Title of thesis: Design and realisation of a monitoring micro-system for help during middle ear surgery operations
  - Expected date of defense: November 2010
  - Previous degrees: Master in Micro and Nano Electronics

- **ASQUINI, Anna**
  - Title of thesis: Auto test circuit development for frequency synthesizers and RF power amplifiers based on fault modelling
  - Completed in January 22, 2010
  - Previous degrees: Master in Electronic Engineering, "Roma Tre" Universitity, Rome, Italy

- **BAHMANI, Maryam**
  - Title of thesis: The architecture of Networks and Integrated Memory for 3 Dimensional Integrated Circuits
  - Expected date of defense: 2013
  - Previous degrees: M.Sc. (2 years) in Computer Architecture, 2006- 2008; Thesis Title: "Corona: A new Ring-Based interconnection for NoC"
BEL HADJ AMOR, Zeineb
- Title of thesis: Formal verification of complex Systems on Chip from the Transaction level to the Register Transfer Level
- Expected date of defense: 2013
- Previous degrees: Master 2 Micro-nano electronic

BEN HASSINE, Nizar
- Title of thesis: Baw devices reliability for RF applications
- Completed in October 29, 2009
- Previous degrees: Master degree in micro and nano technologies

BEN JRAD, Mohamed
- Title of thesis: Robustness improvement by designing circuits implemented on SRAM FPGAs and validation by fault injection
- Expected date of defense: 2012
- Previous degrees: Software engineer

BERGAOUI, Salma
- Title of thesis: Behavioral surveillance for systems and embedded software by disjoint signature monitoring
- Expected date of defense: 2012
- Previous degrees: Software engineer (INSAT Tunisia)

BEYROUTHY, Taha
- Title of thesis: Asynchronous Programmable Logic for Secure Embedded Systems
- Completed in November 2, 2009
- Previous degrees: System Integration" Engineering Degree of the Telecommunication School of Engineering of Bretagne : ENST Bretagne (2005-2006); Masters degree in Micro technology : "M.A.R.S “ (Micro technologie Architecture Réseaux systèmes ) from the Telecommunication School of Engineering of Bretagne : ENST Bretagne ; Masters degrees in Physics - Department of Physics- Faculty of Fundamental and Applied Sciences, Lebanese University , Lebanon (2000-2004)

BIZOT, Gilles
- Title of thesis: A global system issue from power management inside the OS down to silicon process for Reconfigurable and Massively parallel Multi-core Architectures
- Expected date of defense: 2011
- Previous degrees: Master of Science in Micro and Nano Electronic (EEATS - UJF); Electronic Engineer (specialized in System on Chip) (ENSERG - INPG)

BOCQUILLON, Alexandre
- Title of thesis: Fault injection in SRAM based FPGA: production, propagation and consequences
- Completed in October 02, 2009
- Previous degrees: Master diploma : ESPCI ; Engineer diploma : ENSICAEN

BONNOIT, Thierry
- Title of thesis: Hardware/Software Codesign for Low-power and Reliability of Nanoscale configurable Multiprocessors system on chip for Software-defined radio applications
- Expected date of defense: 2011-2012
- Previous degrees: Masters

BOUGEROL, Antonin
- Title of thesis: Study of single event functional interrupts induced by natural radiation environment on memory based complex devices
- Expected date of defense: 2011

BOUSQUET, Laurent
- Title of thesis: Heterogeneous systems modeling and simulation: SystemC-AMS library extension
- Expected date of defense: 2012
- Previous degrees: Master MNE (2009, Marseille) , Ingenieur ISMIN (2009, Saint-Etienne)
BOUSSETTA, Hela
- Title of thesis: Modelling and Global Simulation of self powered Microsystems
- Completed in February 20, 2010
- Previous degrees: Master titled New Technologies of Dedicated information Systems –option systems conception obtained in ENIS (The high school of National Engineering of Sfax-Tunisia) (2002-2004); Master’s diploma (May 2004); Electric Genius to the ENIS–Tunisia (2000-2003); Engineer's Diploma (June 2003)

CANIVET, Gaëtan
- Title of thesis: Analysis of faulted-based attack effects and secure design on a reconfigurable platform
- Completed in September 23, 2009
- Previous degrees: Ingénieur Electricien, Master Recherche Spécialité Génie Electrique

CARLIOZ, Louis
- Title of thesis: Piezoelectric generator thermo-magnetically triggered
- Completed November 27, 2009
- Previous degrees: Master Nanotech, INPG-Polito-EPFL (2006); Licence d'Ingénierie Franco Italienne (LIFl), INPG-Polito (2004)

CENNI, Fabio
- Title of thesis: Modeling of heterogenous systems, analog/digital interfacing and MoC integration
- Expected date of defense: 2012
- Previous degrees: Electronic Engineer Degree, specialized in “Electronic Systems for the Elaboration of the Information” at “Università di Bologna - Facoltà di Ingegneria Elettronica”; First Level Degree at “Università di Bologna - Facoltà di Ingegneria Elettronica”; Maturità Scientifica, diploma (equivalent to a baccalaureate) obtained at “E.Fermi” Technical high school for the Industries (I.T.I.S.) with specialization “electronics and telecommunication” in Faenza, Italy

CHAGOYA-GARZON, Alexandre
- Title of thesis: Communication synthesis in a binary code generation flow targeting heterogeneous multi-tile architectures
- Completed in March 12, 2010
- Previous degrees: April 2007: "Dispense de DEA/Master"; September 2003: Engineer Diploma from the Telecommunication Department of the INPG (Grenoble); 1998: Scientific Baccalaureate Diploma, option mathematics

CHAIX, Fabien
- Title of thesis: Fault-tolerant Deadlock-free adaptive routing for Many Cores chips
- Expected date of defense: 2012
- Previous degrees: Master Micro and Nano Electronics, Engineer Diploma at INPG-ESISAR

CHEFI, Ahmed
- Title of thesis: Design of a CMOS image sensor with low power consumption for Wireless Sensor Networks
- Expected date of defense: 2012
- Previous degrees: Master degree in Electrical Engineering; Engineering degree in Electrical Engineering; Higher technician certificate in telecommunications; Bachelor’s degree

CHEN, Hui
- Title of thesis: Method and aided tools for driver generation in the context of MPSoC
- Expected date of defense: 2012
- Previous degrees: Master of Science in Electrical Engineering and Information Technology (Munich University of Technology); Bachelor of Science in Engineering (Zhejiang University)

CIVET, Yoan
- Title of thesis: MEMS Resonator Frequency Compensation by "in-line" trimming
- Expected date of defense: 2012
- Previous degrees: Master Nanotech (Micro & Nano technologies) (Grenoble-INP, Politecnico di Torino, EPFL), Master recherche MNE (UJF)
• CLAVEL, Renaud
  - Title of thesis: Formal methods for the analysis of errors caused by transient faults
  - Expected date of defense: 2011
  - Previous degrees: Master II EEATS (Grenoble); Master ENS Cachan; Agregation in electronic

• COSTA MARQUES, Greicy
  - Title of thesis: Study and validation of fault-tolerance software techniques to deal with errors induced by natural radiation in architectures based in advanced processors
  - Expected date of defense: 2012
  - Previous degrees: Master in electrical engineering (Federal University of Rio de Janeiro - UFRJ); Engineering Electrician (Federal University of Amazonas - UFAM)

• DAMRI, Laila
  - Title of thesis: Test vectors generation for assertions acceleration
  - Expected date of defense: 2012
  - Previous degrees: Master of Microelectronics System from Montpellier

• DEFOSSEUX, Maxime
  - Title of thesis: Design and characterisation of piezoelectric microgenerators for autonomous microsystems
  - Expected date of defense: 2011
  - Previous degrees: Master’s degree with honours in Electronics Engineering option Micro and Nano Electronics in University Joseph Fourier; "Agrégation" of physics, option applied physics, a highly selective national teaching exam; Bachelor of science with honours in Electronics Engineering at the Ecole Normale Supérieure de Cachan

• DUBOIS, Florentine
  - Title of thesis: Network-on-Chips Static Analysis
  - Expected date of defense: 2013
  - Previous degrees: Master degree in Computer Science from Institut National Polytechnique de Grenoble (school: ENSIMAG)

• DUBOIS, Matthieu
  - Title of thesis: Optimization of Converter Testing Using Statistical Techniques
  - Expected date of defense: 2011
  - Previous degree: DEA degree "Systèmes Automatiques et Microélectroniques" Université de Montpellier 2 (2003); Engineer degree "Microélectronique et Automatisme" Polytech'Montpellier (2003)

• EKOBO AKOA, Brice
  - Title of thesis: Detection and error concealment within a video decoder: Using techniques based on statistic analysis
  - Expected date of defense: 2014
  - Previous degrees: Master 2 Micro and Nano Electronics

• ELISSATI, Oussama
  - Title of thesis: Ring oscillators and asynchronous delay lines: applications to PLLs and “Clock recovery” systems
  - Expected date of defense: 2011
  - Previous degrees: Engineer degree "Informatique Industrielle et Instrumentation" Polytech’Grenoble (2007)

• ELMRABTI, Amin
  - Title of thesis: Methods and tools for code generation for multi-core platforms based on high-level description of applications and architectures
  - Completed in December 08, 2010
  - Previous degrees: Software Engineer diploma, computing master degree
- FALL, Diarga
  - Title of thesis: Fault tolerant techniques for the design of reliable circuits in advanced process nodes
  - Expected date of defense: 2012
  - Previous degrees: Masters in electronics, computing science and instrumentation, Polytech Grenoble, France

- FERRO, Luca
  - Title of thesis: Verification of temporal properties for SystemC TLM specifications
  - Expected date of defense: 2011
  - Previous degrees: Master's degree in Embedded Systems

- FERRON, Jean-Baptiste
  - Title of thesis: Modeling faults in SRAM FFPGA and appropriate protections
  - Expected date of defense: 2011
  - Previous degrees: Engineer degree ENSERG (Grenoble) 2006, M2R MNE UJF (Grenoble) 2007

- FOUCARD, Gilles
  - Title of thesis: Radiation error rate for applications implemented in SRAM-based FPGA: prediction versus measures
  - Completed in June 11, 2010
  - Previous degrees: Master Pro Conception des systèmes intégrés numériques et analogiques, INPG (2003-04); Maîtrise Electronique, Electrotechnique et Automatique UFR de Physique, UJF, Grenoble (2002-03); Licence Ingénierie Electrique, UFR de Physique, UJF, Grenoble (2001-02); DUT Génie Electrique et Informatique Industrielle IUT1, UJF, Grenoble (1999-01)

- GERIN, Patrice
  - Title of thesis: Simulation models for software validation and architecture exploration of Multi-Processors System On Chip
  - Completed in November 30, 2009
  - Previous degrees: Master Recherche Microelectronics Grenoble, France

- GLIGOR, Marius
  - Title of thesis: Fast Simulation Strategies and Adaptive DVFS Algorithm for Low Power MPSoCs
  - Completed in September 09, 2010

- GUERIN, Xavier
  - Title of thesis: An efficient embedded software development approach for multiprocessor system-on-chips
  - Completed in May 12, 2010
  - Previous degrees: DEUG MIAS (2003); Licence d'informatique (2004); Maîtrise d'informatique (2005); DEA / Master informatique (2006)

- GUIRONNET DE MASSAS, Pierre
  - Title of thesis: Study of methods and mechanisms for software-seamless data accesses in a multiprocessor system-on-chip
  - Completed in November 12, 2009

- HAMAYUN, Mian Muhammad
  - Title of thesis: Fast and Accurate Performance Estimation in High Level Multiprocessor System Simulation Platforms
  - Expected date of defense: 2012
  - Previous degrees: Master Computer Science (Informatique), Master Software Engineering
HAMON, Jérémie
- Title of thesis: Asynchronous oscillators and architectures for UWB impulse radio signal processing
- Completed in October 15, 2009
- Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005)

HASSAN, Khaldon
- Title of thesis: Efficient Memory Access for MPSoC NoC-based
- Expected date of defense: 2011
- Previous degrees: Microelectronics Engineer (ENSERG - Grenoble INP)

HEDDE, Damien
- Title of thesis: Use of simulation for development and debugging of parallel programs on MPSoC (multiprocessor system-on-chip)
- Expected date of defense: 2011
- Previous degrees: Engineer in Applied Mathematics and Computer Science

HELMY, Amr
- Title of thesis: Implementation of automatic demonstration techniques for formal verification of NoCs
- Completed in April 30, 2010
- Previous degrees: Master Recherche Microelectronics, Grenoble, France (2006)

HORREIN, Pierre-Henri
- Title of thesis: Integration of cross-layer protocols in a flexible radio environment
- Expected date of defense: 2011
- Previous degrees: Master Degree (Engineer)

HUANG, Ke
- Title of thesis: Fault Modeling and diagnostics for nanometric mixed-signal/RF circuits
- Expected date of defense: 2011
- Previous degrees: Master Research Micro and Nano Electronics

KHEREDDINE, Rafik
- Title of thesis: Embedded Diagnosis of RF and AMS Components: Regression based Methods
- Expected date of defense: 2011

KOCH-HOFER, Cedric
- Title of thesis: Modeling, Validation and Presynthesis of Asynchronous Circuits in SystemC
- Completed in March, 26, 2009
- Previous degrees: Engineer in Computer Science at ENSIMAG (INPG) Grenoble (2004)

KOUDAIRA MOSTEFAOUI, Abdellah Medjadji
- Title of thesis: Flexible architecture for HW/SW interfaces
- Completed in August 24, 2009
- Previous degrees: Master Computer science, University of Versailles, Saint-Quentin-en-Yvelines, France, 2005

LAGRAA, Sofiane
- Title of thesis: New MP-SoC profiling tools based on data mining techniques
- Expected date of defense: 2013
- Previous degrees: Master 2; engineer

LAMRAOUI, Hamid
- Title of thesis: Autonomous microsystem design and integration for an artificial urinary sphincter control
- Expected date of defense: 2011
- Previous degrees: ESIL Engineering degree (master degree equivalence) in Biomedical Engineering; Master’s degree in Automation (INPG)
MAINGOT, Vincent
- Title of thesis: Fault attacks vs. side channel attacks
- Completed in June 09, 2009
- Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005); Engineering in Telecommunication, Grenoble, France (2005)

MANSOUR, Wassim
- Title of thesis:
- Expected date of defense:
- Previous degrees:

MEUNIER, Quentin
- Title of thesis: Study of two solutions for parallel programming support in integrated multiprocessors: work-stealing and transactional memories
- Completed in October 29, 2010
- Previous degrees: Engineer in Applied Mathematics and Computer Science, Master of Research (Major Mathematics, Computer Science)

MIAN QAISAR, Saeed
- Completed in May 05, 2009
- Previous degrees: Masters SIPT (Signal Image Parole et Telecoms) France (2005)

NGUYEN, Hoang Nam
- Title of thesis: Design for test of RF MEMS components and microwave acoustic devices
- Completed in June 06, 2009
- Previous degrees: Master Instrumentation and Microelectronics at Henri Poincare University (Nancy 1) (2004)

ODDOS, Yann
- Title of thesis: Semi-Formal Verification and Automatic Synthesis from PSL to VHDL
- Completed in November 27, 2009
- Previous degrees: Master Recherche Microelectronics, Grenoble, France (2006)

OUCHET, Florent
- Title of thesis: Analogical proof of the synthesis of robust asynchronous circuits. Application to the security of embedded systems in aeronautics
- Expected date of defense: 2011
- Previous degrees: Master EEATS - MNE

PAPAVRAMIDOU, Panagiota
- Title of thesis: Yield and Reliability in Memories for Late CMOS Technologies
- Expected date of defense: 2013
- Previous degrees: Diplome de Physique, Mastère spécialisé Electronique Physique

PASCA, Vladimir
- Title of thesis: Hardware/Software Fault Tolerance Techniques for Reconfigurable 3D Integrated Circuits
- Expected date of defense: 2012
- Previous degrees: Master of Engineering in Computer Engineering from the University of Limerick, Ireland.

PAUGNAT, Franck
- Title of thesis: Study and development of a AMS design-flow in SytemC: semantic, refinement and validation
- Expected date of defense: 2012
• PERONNARD, Paul  
  o Title of thesis: Study of the atmospheric effects on a complex microprocessor  
  o Completed in October 02, 2009  
  o Previous degrees: Master Recherche Microelectronics, Grenoble, France; DEST Electronique (CNAM) (2005); DUT GEII (2001)

• PORCHER, Alexandre  
  o Title of thesis: Proven generation of robust asynchronous checkers-Application to safe embedded systems  
  o Expected date of defense: 2011  
  o Previous degrees: ENSERG Ingineer and Master 2 MNE graduate

• POSSAMAI BASTOS, Rodrigo  
  o Title of thesis: Transient-Fault Robust Systems Exploiting Quasi-Delay Insensitive Asynchronous Circuits  
  o Completed in July 09, 2010  
  o Previous degrees: Electrical Engineer at UFRGS, Brazil; Master in Computer Science at UFRGS, Brazil

• PROST-BOUCLE, Adrien  
  o Title of thesis: Génération automatique d'accélérateurs matériels sur cible reconfigurable via la synthèse d'architecture  
  o Expected date of defense:  
  o Previous degrees: Master's Degree in Micro and Nano Electronics

• RAHMOUNI, Khaled  
  o Title of thesis: Optimisation of the electronic/software design flow in the context of critical embedded systems targeting circuit breakers for medium voltage electrical networks  
  o Completed in December 07, 2010  
  o Previous degrees: Mastère spécialisé Productique et Informatique Avancée, Ecole Centrale de Lille

• RASLAN, Zahy  
  o Title of thesis: Design, fabrication and characterization of microactuators based on carbon nanotubes  
  o Completed in December 17, 2009  
  o Previous degrees: Master’s degree in Advanced Technologies for communication and mobility; Master’s degree in Computer and electrical engineering

• RUIZ AMADOR, Dolly  
  o Title of thesis: Ageing simulation of complexes CMOS circuit  
  o Expected date of defense: 2011  
  o Previous degrees: Master in Micro and nanoelectronic (INPG-UJF)

• RUSU, Claudia  
  o Title of thesis: Multi-Level Fault-Tolerance in Networks-on-Chip  
  o Completed in September 10, 2010  

• SAHNINE, Chawki  
  o Title of thesis: Reconfigurable, high throughput and low power VLSI architecture for advanced OFDM digital processing  
  o Completed in January 30, 2009  
  o Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005); Bachelor in Electrical Engineering, Ecole polytechnique de Montréal, Montréal, Canada (2004)
SHEN, Hao
- Title of thesis: Contribution to a modeling approach and an exploration flow targeted to heterogeneous MPSoC architectures based on configurable processors
- Completed in November 03, 2009
- Previous degrees: Master, Computer Science and Technology, Shanghai Jiao Tong University, Shanghai, P.R.China, 2005

TAN, Junyan
- Title of thesis: Automatic generation of efficient architectures for algorithms of multispectra image processing
- Expected date of defense: 2012
- Previous degrees: Engineer's degree ISTASE and master's degree INSA-lyon.

TONGBONG, Jeanne
- Title of thesis: Design and evaluation of a bist technique for RF LNA
- Completed in July 12, 2009
- Previous degrees: Master Optics and Microwaves, INSERG-INPG, Grenoble, France, (2005)

TOUNSI, Farès
- Title of thesis: MEMS Electrodynamic Microphone in CMOS technology: design, modeling and realization
- Completed in March 22, 2010
- Previous degrees:

VITTOZ, Stéphane
- Title of thesis: Pressure/Vibrations microsensors based on AlGaN/GaN substrate for harsh conditions environments
- Expected date of defense: 2011
- Previous degrees: Master Degree in Micro Nano Electronics from Grenoble Joseph Fourier University of Science (2008); Graduate in Device Physics from Grenoble Institute of Technology (2008)

YAHYA, Eslam
- Title of thesis: Performance Modeling, Analysis and Optimization of Multi-Protocol Asynchronous Circuits
- Completed in September 12, 2009
- Previous degrees: Master of Science/Electrical Engineering, Benha High Institute of Technology, Egypt, (2004)

YANG, Wenbin
- Title of thesis: Design and integration of microsystems in a medical needle for deformation measurement and insertion guidance
- Expected date of defense: 2011
- Previous degrees: Master of science (research) in Micro and Nano Systems, Paul Sabatier University, Toulouse (2008); Bachelor of science in electronic engineering, Zhejiang University, China (2005)

YU, Hai
- Title of thesis: Fault Tolerant Architecture for Mitigating the Variability Issues in Nanometric Technologies
- Expected date of defense: 2011
- Previous degrees: Master

ZAKARIA, Hatem
- Title of thesis: Integrated asynchronous regulation for decananométric technologies: application to an embedded reconfigurable parallel system
- Expected date of defense: 2011
- Previous degrees: Master of Science (Optimal power control of CDMA mobile networks), September 2006, Benha University
ZIMOUCHE, Hakim
- Title of thesis: High Dynamic Range CMOS Image Sensor with no sensibility to disturbance
- Expected date of defense: 2010
- Previous degrees: Master2 Recherche (DEA) en ESM (Electronique, Signal et Microsystèmes)
11. Contracts

TIMA has a long tradition of international cooperation, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2009 - 2010.

European Projects ongoing in 2009 and 2010

IST PROJECTS

- **SHAPES**: (Scalable software Hardware Architectures Platform for Embedded Systems) 01/01/06-30/06-2009 prolongation until 31/12/2009.
  Partners: ADR/TIMA, France; Eidgenoessische Technische Hochschule, Switzerland; Rheinisch-westfaelische Technische Hochschule, Germany; Istituto Nazionale di Fisica Nucleare, Italy; Target Compiler Technologies, Belgium; ST Microelectronics SA, France; Universita di Pisa, Italy; Universita Degli Studi di Cagliari, Italy; Fraunhofer Gesellschaft zur Foerderung der Angewandten Forschung, Germany; Medcom Gesellschaft fuer Medizinische Bilvererbeitung, Germany; PIE Medical Equipment BC, The Netherlands; THALES Communication, France.
  Future computing architectures for Embedded DSP and Control are strategic and deserve adequate research efforts. Tiled architectures suggest a possible HW path: “small” processing tiles connected by “short wires”. Tiled Architectures will cover a significant share of 10+ year embedded applications. The SHAPES project will set a new density record with multi-Teraops single-board computers and multi-Petaops systems, and will be based on a groundbreaking HW/SW architecture paradigm. The heterogeneous SHAPES tile is composed of a VLIW floating-point DSP, a RISC, on chip memory, and a network interface. It includes a few million gates, for optimal balance among parallelism, local memory, and IP reuse on future technologies. The SHAPES routing fabric connects on-chip and off-chip tiles, weaving a distributed packet switching network. 3D next-neighbours toroidal engineering methodologies will be used for off-chip networking and maximum system density.

- **SPRINT**: (Open SoC Design Platform for Reuse and Integration of IPs) 01/01/2006-31/12/2008 prolongation until 31/03/2009.
  Partners: ADR/TIMA, France; FROSILOG SA, France; Universitaet Pederborn, Germany; KEESDA, France; Philips Semiconductor BV, The Netherlands; KUNGLIA TEKNISKA HOEGSKOLAN, Sweden; SPIRATECH Ltd, France; EUROPEAN ELECTRONIC CHIPS & SYSTEMS DESIGN INITIATIVE, France; ARM Ltd, United Kingdom; LAUTERBACH DATENTECHNIK; Germany.
  The SPRINT project aims at enabling Europe to be the leader in design productivity and quality in System-on-Chip (SoC) design, by mastering the SoC design complexity with effective standards and design technology for reuse and integration of Intellectual Property (IP) modules. Designer productivity is the main obstacle to efficient implementation of complex SoCs. Using standards to support the efficient reuse and exchange of IP modules is the way to enhance productivity. The SPRINT consortium performs a rigorous integrated research activity to obtain a breakthrough in technology for reuse and integration of IP modules within and across companies, so that IP from various sources can be combined quickly and efficiently. The key SPRINT objectives are: 1. To align the approaches of the European key players in the SoC domain towards IP reuse and to drive the identification and development of open interface standards for IP integration. 2. To create an open SoC design platform, consisting of standards and a SoC design methodology, with matching tools and IP modules. Such design platform provides the basis for SoC design environments that support the efficient development and integration of interoperable and reusable IP modules, including debug and verification of SoCs. 3. To enable European companies to be the first in the world to demonstrate and subsequently exploit the new standards-based SoC design environments in an interoperable way in order to improve on design productivity and the quality in SoC design.

FP7-Cooperation COLLABORATIVE PROJECT

- **MORGAN**: Materials for Robust Gallium Nitride – 01/11/2008-30/10/2011
Industrial Research and Development Corporation, Sweden, Research Institute for Technical Physics and Materials Science MFA Hungary, MicroGaN GmbH MG Germany, SIFAM Fibre Optics SFO UK, Slovak University of Technology in Bratislava, STU Slovakia, Universität Ulm TUU Germany, Technische Universität Wien TUW Austria, University of Bath UoB UK, Vivid Components Ltd.

This project will study GaN based structures with goals going from material fabrication and optimisation to applications in thermal heat spreaders, interconnection, packaging, power devices, and sensors. All these studies will be realised in the frame of a large consortium capable of realizing deep materials studies, physical and electrochemical simulation and modelling, and to engage studies on the degradation phenomena. The materials development will be compatible to 100mm or even 150mm diameter wafers, that could be later required for implementation in industrial manufacturing plant. Evidently such manufacturing development would be developed elsewhere. The participation of SME and leading companies in diamond materials, epitaxial growth, sensors and power microwave electronics insures potential use in case of success. These materials development will create novel materials for extreme environments. They will increase the product durability (energy production, microwave power, aerospace telecommunication) and, through sensors that will improve process control, decrease the risk of industrial hazards and increase safety.

The role of the TIMA Laboratory is to accomplish detailed modelling of electrical and mechanical behaviour of different structures used for pressure and chemical sensors for harsh environment. Electro-mechanical behaviour of different layers composing these structures will be simulated in order to predict basic features of these sensors. Piezoelectric and piezo-resistive effects in these structures will be studied.

- **EURETILE Project ; “European REference TILed Architecture Experiment” Programme**
  - **ICT(Information an Communication Technologies) – 01/10_30/06/13**
    - Partners : INFN(Istituto Nazionale di fisica nucleare) ITALY, CoordinatorRWTH(Rheinisch-Westfaelische Technische Hochschule Aachen) GERMANY, ETHZ(Eidgenoessische Technische Hochschule Zuerich) SWITZERLAND ATTEL ROMA S.R.L. (ITALY) TARGET COMPILER TECHNOLOGIES NV (BELGIUM) UJF/TIMA (France).
    - EURETILE investigates and implements brain-inspired foundational innovations to the system architecture of massively parallel tiled computer architectures and the corresponding programming paradigm. The execution target is a many-tile HW platform, equipped with a many-tile simulator. A set of SW process - HW tile mapping candidates are generated by the holistic SW tool-chain using a combination of analytic and bio-inspired methods. The Hardware dependent Software is then generated, providing OS services with maximum efficiency/minimal overhead. The many-tile simulator collects profiling data, closing the loop of the SW tool chain. Fine-grain parallelism inside processes is exploited by optimized intra-tile compilation techniques. The elementary HW tile is a multi-processor, which includes a Distributed Network Processor (for inter-tile communication), a floating-point VLIW processor (for numerical intensive computations), and a RISC processor (for control, user interface and sequential computations). Furthermore, EURETILE investigates and implements the innovations for equipping the existing full-European elementary HW tile with high-bandwidth, low-latency brain-like inter-tile communication (emulating 3 levels of connection hierarchy, namely neural columns, cortical areas and cortex). The innovations will secure a 15+ year HW road-map of low-power and fault-tolerant excellence. EURETILE leverages on the working SW and HW prototypes of the innovative multi-tile HW paradigm and SW tool-chain developed by the FET-ACA SHAPES Integrated Project (2006-2009). This background knowledge includes working tile silicon and board, a multi-tile simulator (running up to eight tiles), and a complete SW tool-chain including a parallel programming and an automatic mapping/optimization environment (Distributed Operation Layer), a specialized OS (DNA-OS automatically generated for both RISC and VLIW) integrated with Linux RT, and an optimizing compiler co-designed with the HW tile.

**MEDEA+ PROJECTS**

- **Medea+ 2A 701 : PARACHUTE : (Parasitic Extraction and Optimisation for Efficient Microelectronic Design and Application) 2006-2008 prolongation until 31/03/2009**
  - Partners : MINEFI/DGE/STSI, France ; EADS-CGR, France ; EADS Space Transportation, ATTEL Nantes, France ; AIRBUS, France ; IROC Technologies, France ; TIMA/UJF, France ; Univ. of Madrid, Spain ; Univ. Palma de Majorca, Spain ; Alcatel Espacio, Spain.
  - This project addresses the increasing problem of interference that together with the parasitic effects of new IC processes are affecting the reliability of modern electronic systems. Nanometer circuits, micro-electronics, micro-system technology and power electronic systems are already part of our daily life. However, these systems encounter many problems with natural and artificial
interferences coming from various sources i.e. those circuits are becoming sources of interference to themselves. Considerable steps forward have to be made to improve the "Reliability of Applications based on these Electronic Systems". Reliability will be defined here as the securing of the system function regardless the presence of "interference" and these "Parasitic Effects". The one that will especially be considered are:

- Electromagnetic effects due to the presence of electromagnetic parasitic fields: Electromagnetic Compatibility (EMC), Signal Integrity, Short Electrical Transient, electrostatic discharges;
- Particle Radiation effects: particles naturally present in the atmosphere are able to ionise silicon and induce some parasitic currents: these effects are named /Single Event Upset and Single Event Transients.

- **Médéa+ 2A 708 : LOMOSA** (Low-power expertise for Mobile & multi-media System Applications) 2006-2008 prolongation until 30/06/2009
  Partners: MINEFI/DGE/STSI, France; STMicroelectronics, France; THOMSON R&D, France; PHILIPS, France; THALES Communications, France; CEA/LETI, France; CEA/LIST, France; TIMA/UJF, France; Univ. of Cantabria, Spain; ALARI, Switzerland; Diseño de Sistemas en Silicio, SA, Spain; Royal Philips Electronics, The Netherlands.
  The LoMoSA+ project aims at the creation of a low-power expertise for mobile and multimedia applications by initiating the development of a European low-power System-on-Chip (SoC) platform, consisting of an interacting combination of (architectural) models, design flows and methodologies, hardware design components, embedded software and test-benches. A special work package investigates the impact on power, scalability and performance of future multiprocessor SoC infrastructures based on on-chip communication solutions. The concept of hardware-dependent software (HdS) allows building efficient hardware-software interfaces and thus enables keeping power consumption under control for these novel architectures. The LoMoSA+ consortium consists of world-class experts from the industry (Philips, STM, Infineon, Thales, Thomson), a number of university research labs and institutes (CEA, TIMA, Universities of Braunschweig, Kaiserslautern, Paderborn, Munich, Berlin, Cantabria) and 2 SME’s (DS2, and Target). The contribution of TIMA in this project is the definition of a hardware dependent software API and a set of tools to support the optimized implementation of hardware/software interfaces based on a user-defined library of heterogeneous components.

- **Médéa+ 2A717 : Beyond DREAMS** 01/06/2008-31/05/2011
  Partners: STMicroelectronics (Grenoble) SAS, MAGILLEM Design Services, CEA/LETI, Université PARIS VI PIERRE et MARIE-CURIE.
  Design Refinement of Embedded Analogue and Mixed-Signal Systems (DREAMS) is a joined effort of the European semiconductor companies, together with leading European Universities and research institutes, to address the design issues for these mixed-signal systems. The overall objective of the Beyond DREAMS project is to improve the competitiveness of European industries in the domain of embedded mixed-signal system design by reducing the entire design time and cost of heterogeneous SoC and SiP. To achieve this overall objective, DREAMS will improve the design refinement process of EAMS by providing a methodology, a simulation and modelling framework, standardized languages, libraries and modeling formats that guide and instruct designers to perform architectural refinement of analogue/mixed-signal/RF sub-system design in the context of digital HW/SW co-design. It offers a modeling and simulation platform to validate communication and network protocols, architectures, analogue/RF subsystem specification or properties of the physical implementation in the early design space exploration phases.
  The objective is to develop modelling techniques that will be donated to the standardization bodies, and the proof-of-concept implementation developed in the project must be freely available as open-source software. In addition, a design environment facilitating IP integration, modeling and simulation is required. This unified design framework, which should be based on standardized meta-data model descriptions, should bring the different design disciplines together, enabling design/IP reuse and interfacing with third-party design and simulation tools.

- **Medea+ 2A714 : SOFTSOC** 01/01/2008-31/03/2011
  Partners: THALES Communications SA, THOMSON R&D France, CEA/LETI.
  SoftSoC aims at solving the main SoC productivity bottleneck by providing Hardware Dependant Software (HDS) solutions to enable SoC designers to aggregate multiple HW IP with their associated HDS into efficient design.
  SoftSoC solutions will enable Europe to maintain its leadership in key strategic markets by increasing the capacity of SoC designers to build larger and better quality systems in less time.
The consortium involves European leaders in system and SoC design interested in the exploitation of the results.

- **Medea+ iGLANCE** *(Interactive Genius Look At Numerous Contemporary Events)* 01/07/2008-30/06/2011
  Partners: STMicroelectronics(Grenoble) SAS, 4D WIEW Solution, LOGICA IT SERVICES France, INRIA.
  High-Definition Television (HDTV) is close to mass-market development in Europe, as the most important key component, i.e. the flat screen display, has become affordable for consumers, and besides this, media and standards for HDTV content distribution are available (BD, HD-DVD, H.264 video coding). In fact, experiments with HD displays have revealed that three-dimensional TV (3DTV) for consumers may be implemented at low cost by extending the display with a lenticular lens coating and a feasible 3D rendering engine. A next-generation processing chip for HDTV receivers should therefore not only upgrade the existing generation of chips in terms of performance of high-definition AV quality, but also prepare for the development of a new innovative application. Simultaneously, the breathtaking growth of the Internet and the increasing use of cameras is pushing innovations in AV content distribution, user content creation such as a YouTube channel, and remote information sharing. Therefore, the broadcasting market is experimenting with new forms of video distribution, like IPTV. These developments call for a TV chip design which innovates in the direction of 3DTV, featuring so-called multi-view decoding. This allows interactive selection of viewpoints within a scene between the available camera viewpoints (Free-Viewpoint TV). This viewing mode also appears in medical analysis applications. Furthermore, the healthcare market provides interesting cases 3DTV, since 3D data is common for many medical imaging modalities (e.g. CT, MR, 3D/4D ultrasound, 3D X-ray), and the visualization of such data could inherently benefit from 3D display devices and advances in the underlying techniques.

The iGLANCE project brings a strong partner in advanced imaging with the European market leader of TV chips together in their ambition to realize new innovations in digital TV platforms. This embedded system will be implemented by developing an innovative chipset and the corresponding software and architecture, where

1. the system can offer the ultimate HDTV AV quality to serve the European mass-market application of HDTV, and by
2. establishing a flexible architecture extension providing the additionally required computation power for 3D multi-view decoding, requiring the processing of several HDTV channels.

**LATIN AMERICA HIGHER EDUCATION PROJECTS** *(Amérique Latine Formation Académique : ALFA)*

  Partners: Universidade Federal do Rio Grande do Sul (UFRGS), Brazil; Instituto Nacional de Tecnologia Industrial (INTI), Argentine; Universidad del Valle (UV), Colombia; Pontificia Universidad Catolica de Peru (PUCP), Peru, Universidad de la Republica (UR), Uruguay; Instituto Nacional de Astrofísica, Optica y Electronica (INAOE), Mexico; Politecnico di Torino (POLITO), Italy; Instituto Superior Tecnico (IST), Portugal; Ecole Nationale Supérieure d'Electronique, Informatique et Radiocommunications (ENSEIRB), Bordeaux, France; IMSE-CNMIstitut National Polytechnique de Grenoble (INPG/TIMA), France.
  The constant progress accomplished in microelectronic circuits manufacturing technologies entails a significant increase of their sensitivity to different parasitic phenomena induced by the environment, making mandatory the use of fault tolerant techniques to guarantee the final system reliability/safety. The proposal goals are to support students and researchers mobility among a net of Latin American and European Universities having well-recognized skills in this area. Thanks to both the complementary experience of the network members, and the novelty of problems and proposed solutions, the offered training activities represent a precious vehicle in the diffusion of fault-tolerant design techniques in the participating countries.
MARIE-CURIE Outgoing International Fellowships (OIF)  
Support for Training and Career development of researchers

- **Contract “RESPONS”**: Multiple-Valued application of negative differential resistance devices in asynchronous circuits design. 31/01/2007-30/01/2010  
  Partners: CEE/TIMA-INPG/ASU Fulton School of engineering (Arizona State University)  
  The project targets the post-CMOS era technologies. It focuses on the digital logic applications of negative-differential resistance (NDR) semiconductor nanodevices. NDR property appears in nanometer scale devices due to quantum resonant tunnelling or Coulomb blockade effects and inherently introduces strong binary and multi-valued processing capacities of the devices like resonant-tunneling diodes (RTD), single-electron transistors (SET), carbon nanotubes (CNT).

  This project aims to develop test strategies for mixed-signal/radio-frequency (RF) integrated devices using machine learning. The proposed efforts will be directed to two main areas, namely (a) the on-line test of mixed-signal/RF circuits when they are embedded in a System-on-Chip (SoC) or a System-in-Package (SiP) that demands high reliability and (b) the testing of RF micro-electro-mechanical systems (MEMS). The key novelty of this interdisciplinary project lies in very large-scale integration (VLSI) design and test, in order to address emerging and open-ended test challenges.

CATRENE PROJECTS

- **3DIM3 project**: 3D – TSV Integration pour application Multimedia et Mobile -01/02/2009-31/01/2012  
  Partners: STMicroelectronics (Grenoble2) SAS, NXP SEMICONDUCTORS France EADS DEFENCE and SECURITIIY SYSTEMS SA CADENCE DESIGNE SYSTEMS R3 LOGIC France - CEA GRENOBLE - ECOLE CENTRALE de LYON, INP/TIMA.  
  3D TSV integration technology allows the stacking of different chips and devices in a single package. The maximum benefit is obtained from the use of heterogeneous and highly specialized technologies, and the possibility to make the optimal partitioning early in the design process. This project aims at providing novel system design methodologies, new design tools and system architecture solutions to handle this emerging 3D TSV integration technology. This project will therefore enable the efficient design, from system level to layout, of 3D integrated Multimedia and Mobile products with higher performances, lower power, and smaller size/form factor at lower cost.

- **COMCAS project**: COmmunication-centric heterogeneous Multi-Core ArchitectureS. 01/03/2009-29/02/2012  
  Partners: STMicroelectronics (Grenoble2) SAS, CEA-CENTRE de SACLAY, THALES CommunicationsSA, STMicroelectronics WIRELESS SAS CEA-CENTRE de GRENOBLE, UNIVERSITE de NICE, ST-NXP WIRELESS France INP/TIMA.  
  This project “COMCAS” aims at breakthrough low-power design solutions for (data) communication-centric heterogeneous multi-core architectures targeting 45nm and 32nm CMOS technologies. These architectures will be exploited in a number of future applications e.g. the next generation of programmable multi-processor mobile phones and mobile digital entertainment devices. COMCAS investigations concern the complete low-power design hierarchy looking at all aspects from system level choices, modeling of applications (algorithms, protocols) and architectures, maximize the reuse of existing IPs using the most appropriate tool chains, partitioning and mapping, cycle-accurate and bit-true virtual prototyping, minimal power design blending semi- and full custom circuit designs at transistor level in technologies of 45 nm and beyond.

- **OPTIMISE project**: OPTImisation of Mitigation for Soft firm and hard Errors. 01/07/2009-30/06/2013  
  Partners: EADS France, AIRBUS OPERATIONS, ATMEL NANTES SA, STMICROELECTRONICS (TOURS) SAS, VALEO Etudes Electroniques, CONTINENTAL AUTOMOTIVE France, REGIENOV, IROC TECHNOLOGIES, CEA, INSTITUT POLYTECHNIQUE DE BORDEAUX CNRS (Marseille).  
  This project aims at developing optimized mitigations for advanced digital and power electronic systems in order to solve the major issue of their reliability against the increasing problem of soft, firm and hard errors. To reach this goal, end-users, semiconductor manufacturers are associated with technology developers and European academic partners.
The expected deliverables are a set of validated mitigation techniques from layout to applications architecture levels, customized mitigations for given applications and a strong effort in standardization.

The expected benefits will be the capability to use advanced electronics in critical end-user applications, and ensure reliability of consumer electronic, especially for low power.

**TOEST Project**: “TOESTS” is the Dutch word for TESTS : 01/04/09-31/03/12

Partners: STMicroelectronics (Crolles 2) SA, NXP SEMIONDUC- TORS France, CEA, ATMEL ROUSSET SAS, STMICROELECTRONICQ GRENOBLE 2, CEA centre de Saclay), INFINEON TECHNOLOGIES France, IRoC TECHNOLOGIES, SUPELEC, E2V SEMICONDUCTORS France, TEMENOTO SYSTEMS, CNRS Délégation Languedoc Roussillon, OPHTIMALIA.

Testing takes an increasingly significant proportion of total production costs for advanced semiconductor devices as miniaturisation and integration levels rise. For system-on-chip and system-in-package designs, such testing can be up to 20% of the total cost of chip design and manufacture – and this is increasing drastically as complexity and functionality grow. Yet often, 80 to 90% of this testing concentrates on the analogue, mixed analogue-digital signal and embedded radio-frequency parts of the design. The TOETS project focuses on developing new methods to bring down the cost of such testing, and is addressing the challenge at application, chip architecture and transistor technology levels.

**NATIONAL PROJECTS**

In addition, TIMA is a partner in a variety of national cooperative research actions, which are listed below:

- **ANR projects**:

  1. **ARESA** : (Système Enfoui et Réseaux de Capteur) 13/12/2005-12/12/2008 prolongation until 31/12/2009
   
   Partners: France Telecom R&D/TECH/IDEA - LSR IMAG VERIMAG - CITI EA - CORONIS SYSTEMS

   Wireless sensor networks (WSN) are expected to become the support for new services benefiting citizen, businesses and communities alike. In these networks composed of large numbers of small embedded communicating devices, energy is a precious resource. In order to accelerate technical and commercial viability of long-lived WSN-based services, ARESA set out to research system architectures, hardware technologies and communication protocols that substantially reduce WSN power consumption compared to prior art.

   After setting a few application frameworks and spelling out their operating constraints, we simultaneously tackled the aspects of global system modeling and building blocks optimization.

   We produced a formal model encompassing the sensor network and the physical world, with accurate account of nodes power consumption. We explored the scalability issues when the network grows to a huge number of nodes.

   We architected the sensor node and studied its hardware-software partitioning, then proposed energy-optimized hardware blocks and communication protocols.

   To validate our research work, we both ran full system software simulations and deployed a field demonstrator comprised of about forty nodes.

   Throughout the project, we have published our results in scientific journals and conferences, applied for patents, accelerated market maturity by contributing to standardization, improved our industrial partners’ technology and we now hand out hardware building blocks, software building blocks and a great deal of expertise to further research projects.

  2. **SoCLib** : (Plate-forme de Prototypage pour Applications Logicielles Embarquées sur Puce) 01/12/2006-30/11/2009 prolongation until 31/03/2010

   Partners: Université Paris VI (Pierre et Marie Curie) coordinating, THOMSON R&D France SNC, STMicorelectronics S.A, THALES Communications SA, CEA/Centre d’études Nucléaires SACLAY, INSA Lyon, Groupe des Ecoles des Télécommunications, INRIA, Univ de Bretagne Sud, MAGILLEM DESIGN Services, TURBOCONCEPT, CEA Grenoble, SILICOMP-AQL

  3. **FME** (programme SESUR) : Enhancing the Evaluation of Error consequence using Formal Methods – 01/01/2008-31/12/2010

   Partners: LIP6 (Laboratoire Paris 6)
The aim of the FME3 project (Enhancing the Evaluation of Error consequences using Formal Methods) is to develop and evaluate a new methodology for analyzing the robustness of circuits described at the RT level, with respect to errors caused by transient faults. We propose to improve efficiency and accuracy by combining fault injection techniques and formal methods. The cornerstone of our approach will be a functional modeling of both the device and the fault models. Such a formalization will fit the capabilities of model checking tools as well as of theorem provers, thus giving the possibility to consider various kinds of circuit descriptions, including parameterized ones.

- **SFINCS** (programme ARFU) : Semi-Formal INstrumentation for Circuits and Systems
  01/01/2008-31/12/2010
  Partners : DOLPHIN, THALES
  The SFINCS project (Semi-Formal INstrumentation for Circuits and Systems) investigates and develops new technologies for SoC validation. SFINCS addresses Assertion-Based Verification (ABV). The aim of this project is to develop and integrate methodologies to apply ABV to a variety of hardware systems, using a uniform approach founded on a technology conceived in the TIMA Laboratory. We target the following designs:
  - synchronous IPs described at the RT level
  - pseudo-synchronous, mixed functions and GALS systems (Globally Asynchronous Locally Synchronous)
  - HW/SW system aspects described at the SystemC TLM (transactional) level
  - application to complex, mixed SoC and to safety critical systems.

- **HOSPI** (Programme ARFU) : HOmogeneous SPecification for Platform Integration
  01/01/2008-31/12/2010
  Partners : CEA/LETI-DCIS, MAGILLEM Design Services (MDS).
  The objective of the HOSPI project is to define innovative methods, and implement the associated tools, to ease the mapping of data-streaming applications on heterogeneous platforms. From a practical point of view, it implies to reduce the gap that exists between the application description, i.e. high level specification that does not make any assumption on the implementation, and the platform description, that includes pieces of hardware and pieces of software to support the actual implementation. We propose a 3 steps process: /a)/ use a general-purpose environment to describe and parallelize the application. This environment will be based on Process Networks (PN) to express the coarse grain parallelism of the application, /b)/ provide an abstract view of the platform, both on communications and computations sides, based on an XML view. The target formalism will be inspired from the existing IP-XACT schema, but will require many still to be identified add-ons to express the platform capabilities and parameters, and /c)/ define relationships between these two views in order to automate the way the application can be mapped from its PN representation onto the HW platform. These relationships will be used to express the mapping choices, and be supported by tools to automate the generation (or parameterization) of the HW and SW.

- **SESAM** (programme ARPEGE : Systèmes Embarqués et Grandes Infrastructures).
  Partners : CHAMBRE de COMMERCE et d'INDUSTRIede PARIS - Ecole Supérieure d'ingénieurs en Electronique et Electrotechnique (ESIEE); CEA de GRENOBLE: Université Paris VI Pierre et Marie-Curie
  This project is lead by ESIEE-Paris. In this project we focused our attention on low frequency vibrating structures working at frequencies close to 200 Hz and working efficiently at very low levels of acceleration. The goal of this project is to prove that is possible to harvest energy efficiently at lower frequencies.

- **EMAISeCi** (programme ARPEGE) : Analyse et Injection Electromagnétiques sur circuits sécurisés.
  01/10/10-29/01/14
  Partners : Université de Montpellier II (Sciences Techniques du Languedoc), Ecole Nationale Supérieure des Mines de Saint Etienne, Université de Saint Etienne.
  The security constitutes a crucial component of Media and Communication technologies. Among the threats, the vulnerability of the electronic material which implements cryptography is perhaps most important. Among the most known attacks, those called by "side channels" (or observation), exploit the correlation between the handled data and the consumption or the electromagnetic radiation of the component. Another type of attacks, called by "injection of faults" circumvents protections intended to protect sensitive information, while modifying the operation of the component.
  The objective of the EMAISeCi project is to allow a theoretical comprehension of the influence of EM (for the observation or the injection of faults) on integrated circuits. This comprehension will
later on make it possible to build counter measures dedicated to the emergent threats on security based on the exploitation of the EM channel.

- **DGE projects, competitiveness cluster MINALOGIC:**

  - **SCEPTRE** : Optimisation Partitionnement, Modélisation et Compilation des SOC Multiprocesseurs  
    STMicroelectronics Divisions STS et HEG, INRIA Equipes MOAIS, Mescal, Arenaire et Compys,  
    IRISA Equipe CAPS, TIMA Equipe SLS, UJF (Verimag), CAPs Entreprise

  - **OPEN-TLM** : Open Transaction Level Modeling)  
    CEA/LETI, INRIAAlpes, Keesa, Silicomp, STMicroelectronics, TIMA, Thomson, UJF (Verimag)

  - **ASTER** : Architectures pour mémoires STAtiques haute pErformance  
    STMicroélectronics SA coordinating, Defacto Technologies, TIMA/INPG

  - **VIS-IMALOGIC** : E2V SEMICONDUCTORS SAS coordinating, CEA/LETI; TIMA/UJF

  - **ARAVIS** : Architecture avancée Reconfigurable et Asynchrone pour Vidéo et radio logicielle Intégréée  
    STMicroélectronics SA coordinating, INRIA, CEA/LETI, France Telecom

  - **SOCKET** : SoC toolKIT for Critical Embedded systems  
    Partners : ASTRIUM SAS, STMicroelectronics (Grenoble) SAS, THALES Research & Technology France,  
    AIRBUS, France, MAGILLEM Design Services, SCHNEIDER, ELECTRIC INDUSTRIE SAS, CEA/LETI,  
    Université de Bretagne Sud, Centre National d'Etudes Spatiales  
    The SoCKET project (SoC toolKit for critical Embedded systems) gathers industrial and academic  
    partners from the Aerospace Valley (http://www.aerospace-valley.com/en/) and Minalogic  
    (http://www.minalogic.com/en/) pôles to address the issue of design methodologies for critical  
    embedded systems. The main goals are the following:  
    • to define a "seamless" design flow which integrates qualification and certification, from  
      the system level to integrated circuits and to software  
    • to apply the SoC’s design methodologies to critical embedded systems  
    • to reduce design time (by enabling concurrent hardware and software development) and to  
      optimize SoC-based design  
    • to disseminate these methodologies through the Aerospace Valley and Minalogic pôles.

  - **SHIVA** : "Secured Hardware Immune Versatile Architecture",  
    Partners : CS - Systèmes d'Information Netheos, CEA/LETI, INRIA, INPG/TIMA  
    SHIVA ("Secured Hardware Immune Versatile Architecture") is a MINALOGIC project supported by  
    French national research founding in the period 2009-2012. The aim is developing secured blocks  
    for high performance network infrastructures. TIMA contribution is threefold: (1) developing  
    high performance (over 10 Gbps) hardware crypto-processors for AES and RSA encryption and  
    decryption; these crypto-processors, especially the AES one, include several countermeasures  
    against fault-based and side-channel attacks (2) proving the efficiency of some of these  
    countermeasures by means of formal verification techniques and (3) developing new True Random  
    Number Generators based on asynchronous structures. Three groups of TIMA (ARIS, VDS, CiS)  
    collaborate within this project with several industrial and academic partners.

- **Other National Projects:**

  - **ASTEC** : Asynchronous TECnology and components for ultra low power embedded and  
    secured systems.  
    Partners : CEA Centre de Grenoble, TiEMPO, UJF/TIMA.  
    The aim of the Minalogic ASTEC project is to design a new family of Low power Asynchronous  
    components (IP of 16 and 32bits micro controller core). These components will be dedicated to  
    Low Power embedded systems and security applications. In order to demonstrate the  
    performances of these asynchronous IPs, two microcontrollers will be designed and tested (With  
    Tiempo SAS and TIMA Labs): A 16bits version for Low Power applications and a 32bits for  
    security applications. The 16bits microcontroller will be used in several prototypes of low power  
    embedded systems for medical and sport applications (with Cyberfab SARL and Tracedge SARL).  
    The 32bits microcontroller will be validated in a security application (with CESTI LETI)
- CROLLES III « NANO-2012 » DECOPUS and ASSERTIONS Projects: 01/09/2008-31/12/2010

Partners: Alcatel Vacuum Technology France, CCI de PARIS, CEA centre de Saclay, CEA centre de Grenoble, CNRS, (CEMEE, CRHEA, IEMN, IM2NP, LAAS, LCC), Ecole Centrale de Lyon, ENSEA, ENSIERB/IMS, IBM, INPG/IMEP, INPG/SIMAP, INPG/TIMA, INRIA (Grenoble), Rennes, Sophia Antipolis, Institut Supérieur d’Electronique du Nord (ISEN), MASA GROUP, ST Microelectronics (Crolles), (Grenoble & Wireless), Univ.MontpellierII (GES), Univ. d’Orléans (GREMI), Univ.PARIS SUD ORSAY (IEF), Univ.PIERRE & Marie CURIE (LIP 6), Univ.de TOURS François RABELAIS(LMP), Univ.de SAVOIE.

Subproject "Test sequence generation for assertion acceleration" (VDS team)

The global goal of this subproject is to develop an assertion-based methodology for testing embedded systems. In our approach, starting from PSL assertions, we generate synthesizable VHDL or Verilog descriptions of hardware checkers. These components can be connected to the device under test and used during simulation or hardware emulation to check whether the temporal properties expressed by the PSL assertions are satisfied. In that context, test sequence generation is a crucial issue. Using constrained random test generation can lead to a low coverage rate for the checkers’ activation conditions, and checking can thus be irrelevant. The goal of this project is to propose new methods for generating test sequences constrained by temporal properties.

- CROLLES III « NANO-2012 » NACRE (NANO Composants REsonants en réseau) 2009 - 2012

Partners: ST SA, MSA Group, CNRS/CRHEA, CEA/LIST, INRIA Bretagne, CNRS 31/CEMEE, CNRS 59/IAEMN, CNRS 31/LAAS, Univ.MontpellierII/GES, Univ.Orléans/GREMI, Univ.Tours/LMP, AVTF, INPG/SIMAP, Ecole centrale de Lyon, INRIA Sophia Antipolis, ST Microelectronics 2 (Grenoble), IBM, UJF/TIMA, ASML

The aim of this project concern the design fabrication and characterization of Micro Electromechanical Resonators used as time references. These devices offer a promising alternative to industrial Quartz crystal time references thanks to size reduction, low cost, CMOS integration and multi-frequency applications. These devices are fabricated on standard 12 inches SOI substrates.

- Rhône-Alpes (Regional projects)


  Partners: iRoc Technologies, E2V Grenoble, CNES, INPG/TIMA coordinating

  - CLUSTER II « ISLES » SEMBA project 2009 et 2010

  Partners: TIMA and Citi coordinating, VERIMAG, LCIS, INL, LIP, LHC, LAMA, LIG, GIPSA, INRIA-Planete

  Title: Systèmes EMBArqués

  To produce competitive embedded systems for the consumer electronics market is a constant challenge, due to the rapid technological evolutions in micro and nano-electronics, and the fast obsolescence of the products that include them. Low cost and power consumption, fast design, manufacturing and test, and system reliability are essential conditions for success; it is important to be able to formally specify, predict and control them.

  The SEMBA project, follow-up of the EMSOC Research project, aims to federate public research laboratories of the Rhône-Alpes region in the field of embedded systems. The project is organised around 3 thematic areas:

  1. Architecture and design
     key-words: software/hardware architectures, components, synthesis
  2. Evaluation of the quality of embedded systems
     key-words: validation, test, reliability, performance, quality of service
  3. Software and communication infrastructures for embedded systems
     key-words: protocols, OS, middleware, sensors networks, safety, networks-on-chip

  - CLUSTER I « microélectronique, nanosciences » µSEEMPE (µ-Sources Energie Electrique Matériaux Piezo Emergents) 2010 – 2013

  Partners: TIMA, INL, LGEF, CEA-Leti

  With our partners we are working on the integration of new piezoelectric materials deposited by thin film techniques on top of silicon substrates. The target of this work is to provide different technologies for the fabrication of seismic piezoelectric generators. The resonant frequencies of such devices are below 200Hz.

  - CILOE: Calcul Intensif pour les LOgiciels de CAO Electronique et les applications embarquées.

  Pôle de compétitivité MINALOGIC. 13/06/2008-12/07/2011

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Partners: BULL, INRIA (équipe Mescal et Moais), CEA/LETI, 3 PME (EDXACT, INFINISCALE, PROBAYES)

CILOE is a project involving Grenoble Universities (UJF-TIMA), other academic partners (INRIA, CEA-LETI), Small industries (SC, EDXact) and big industries (BULL, CS). It received the label MINALOGIC. The main goal is to study and experiment High-Performance Computing in the field of Computer Aided Design of Electronics and in embedded applications. The contribution of TIMA (one man-year) is about the CELL processor.

  
  Methods, tools and models for the development, the test and the qualification of fault tolerant multiprocessor platforms
  
  The main goal of this project is the development of new models, methods and tools for the prediction of the reliability and the dependability of fault tolerant multi-processor systems (FTMPS), particularly with respect to faults induced by ionizing radiation. This research is focused in FTMPS implemented by means of FPGA (Field Programmable Gate Arrays) and devoted to real-time signal processing, the final goal being the analysis of the possibility to use commercially available FPGAs for the control of intelligent antennas devoted to operate on-board satellites.

- HBS (Heart Beat Scavengers) 2010-2013
  
  Partners: TIMA, Sorin CRM, CEDRAT, Tronics, EASII-IC, TRONICS and CEA-Leti
  
  This project is leaded by SORIN CRM group. It concerns the design, fabrication and characterization of tiny generators exhibiting ultra low resonant frequencies. These devices are powered by the heart beats.

LOCAL PROJECTS

- MISTIC Project: TATIE (Technologie Asynchrone et Traitement des signaux Irrégulièrement Echantillonnés) 2009-2011
  
  Partners: TIMA, LJK, Gipsa-Lab
  
  Le développement de nouvelles techniques de conversion analogique–numérique basées sur un échantillonnage irrégulier en temps conduisent à repenser complètement les chaînes de traitement numérique. Ce paradigme se traduit également par une refonte des méthodes de calcul numérique usuellement adoptées en traitement du signal et des technologies d’automatique discrète. Cette étude associant des chercheurs de TIMA, du LJK et de Gipsa-Lab vise à développer un cadre théorique au traitement des systèmes numériques à échantillonnage non uniforme, asservis ou non, permettant de réaliser des systèmes matériels embarqués faiblement consommateurs et rayonnants.
12. International activities

This section gives an overview of national and international activities in which the members of the Laboratory participated.

International cooperation agreements

The Laboratory is engaged or has been recently engaged in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations took various forms, e.g. extended visits of researchers at the cooperative location, organization of joint research, organization of workshops, etc.

- Politecnico di Torino, Italy (2006-2009)
  This cooperation takes place in the framework of ALFA NICRON project; between France and Italy. The project deals with validation of an automated technique for the realization of robust software devoted to high-safety applications with the Dipartamento di Automatica e Informatica, M. Sonza Reorda.

- University of Montreal, Canada (2006-2009)
  This cooperation with the group of Pr. El Mostapha Aboulamid, includes the exchange of staff and students. It is directed by F. Rousseau and F. Pétrot at TIMA.

- McGill University, Montréal, Canada (2008-2009)
  This cooperation with the group of Prof. Zilic started in the framework of a “Centre Jacques Cartier” project. It focused on the assertion-based verification, debug and on-line monitoring techniques. Researcher exchanges lead to three common publications. The cooperation is directed by D. Borrione and K. Morin-Allory at TIMA.

- Sharif University, Tehran, Iran (2008-2009)
  This cooperation, under the framework of a Gundishapur PHC program (Egide), focuses on the signal processing systems based on a non-uniform sampling scheme. The cooperation is directed by Prof. Farokh Marvasti from the Sharif University and L. Fesquet at TIMA.

- Tallinn University, Estonia (2008-2010)
  This cooperation includes the exchange of students. The cooperation contact is Pr. Raimund Ubar in Tallin, Paul Amblard at TIMA.

- The Hong Kong University of Science and Technology (HKUST), Department of Electronic and Computer Engineering, Clear Water Bay, Kowloon, (2009-2010)
  Title: Integrated Wireless Capacitive Micromachined Ultrasonic Transducer for Bio-medical Applications

- Yaounde University, Cameroun (2009-2011)
  This cooperation with the team of Prof. Maurice Tchuenté of Yaounde I University in Cameroon includes the exchange of staff, the co-supervision and the exchange of students and it is directed by Emmanuel Simeu at TIMA.

- University of Oradea, Romania (2009-2011)
  This cooperation consists in PhD exchange students and takes place in the framework of an ERASMUS project; between France and Romania. Representatives: L. Anghel and D. E.Popescu.

- University of Malaga and Cidetec, San Sebastian, Spain (2009-2012)
  Title: Design and Application of Smart Sensors Based on Piezoresistive Principles
  Programme: TEC2009-14446-C02, Ministry of Science and of Innovation of Spain
  Leaders: F. Vidal Verdú (Univ. Malaga), L. Rufer (TIMA)
- **Academy of Science, Institute of Electrical Engineering, Slovak Republic (2010-2011)**
  
  Title: Advanced GaN mechanical sensors for extreme conditions
  
  Programme: PHC (Partenariats Hubert Curien) STEFANIK, Sponsor: The French Ministry of Foreign Affairs and the French Ministry of Education and Research. Leaders: Tibor Lalinsky (IEE) and Libor Rufer (TIMA).

- **Institute of Electronics and Computer Science (IECS), Riga, Latvia (2010-2011)**
  
  This project ADSP-NoA, under the framework of the Osmose program (Egide), focuses on the signal processing systems based on a non-uniform sampling scheme. This cooperation also targets the architecture and implementation levels and is directed by Dr. Modris Greitans, Head of the IECS and L. Fesquet at TIMA.

- **Yale University, USA (2010-2011)**
  
  This cooperation includes the exchange of students and it is directed by Prof. Yiorgos Makris from Yale University and Haralampos Stratigopoulos from TIMA. A Ph.D. student from Yale University visited TIMA for a period of 3 months in 2010.

- **Aristote University of Thessaloniki, Greece (2010-2011)**
  
  This cooperation takes place in the framework of the LLP/ERASMUS 2010-2011 program. The academic responsible persons are Prof. Alikiviades Hatzopoulos from Aristotle University of Thessaloniki and Emmanuel Simeu and Haralampos Stratigopoulos from TIMA. A Ph.D. student from Aristotle University of Thessaloniki will be visiting TIMA for a period of 6 months in 2011.

- **University of São Paulo, Polytechnic School, Microelectronics Laboratory (LME), Brazil (2011-2014)**
  
  Title: Développement et miniaturisation de filtres, antennes et lignes de propagation intelligentes
  
  Programme: CAPES-COFECUB, Leaders: I. Pereyra (USP), Ph. Ferrari (IMEP), L. Rufer (TIMA)

### Organisation of International Conferences, Workshops, Forums

In the following 2 tables, TIMA researchers were General or Program chair or co-chairs for the listed events.

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<thead>
<tr>
<th>ACRONYM</th>
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<th>LOCATION</th>
<th>ROLE</th>
<th>NAME</th>
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<tr>
<td>DATE 2009</td>
<td>International Conference on Design Automation and Test in Europe</td>
<td>Nice</td>
<td>Special Day Organizer</td>
<td>L. Anghel</td>
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<td>DCIS 2009</td>
<td>Design of Circuits and Integrated Systems Conference</td>
<td>Zaragoza, Spain</td>
<td>Technical Program Co Chairs</td>
<td>L. Anghel</td>
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<td>DRV 2009</td>
<td>2nd Wkshp on Design for Reliability &amp; Variability</td>
<td>Austin, TX, USA</td>
<td>General Chair Co-general chair</td>
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<td>FDL 2009</td>
<td>12th Forum on specification and Design Languages</td>
<td>Nice, France</td>
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### International activities

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<td>MTRE 2010</td>
<td>Workshop on mitigation techniques against space radiation effects on Ics 2010</td>
<td>Estec, Netherlands</td>
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<td>PATMOS 2010</td>
<td>20th Power and Timing Modeling, Optimization and Simulation International Workshop</td>
<td>Grenoble, France</td>
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<td>SERESSA 2010</td>
<td>6th Int. School on the Effects of Radiation on Embedded Systems for Space Applications</td>
<td>Sao José dos Campos, Brazil</td>
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<td>TVHSAC 2010</td>
<td>2nd Workshop on Test and Validation of High Speed Analog Circuits</td>
<td>Austin, Texas</td>
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### Participation to Committees for International Conferences and Symposia

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<td>ASAP 2009</td>
<td>International Conference on Application-specific Systems, Architectures and Processors</td>
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<td>AE 2010</td>
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<td>International Conference on Application-specific Systems, Architectures and Processors</td>
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<td>ASYNC 2010</td>
<td>IEEE International Symposium on Asynchronous Circuits its and systems</td>
<td>Grenoble, France</td>
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<td>DATE 2010</td>
<td>International Conference on Design Automation and Test in Europe</td>
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<td>DCIS 2010</td>
<td>Design of Circuits and Integrated Systems Conference</td>
<td>Lanzarote, Spain</td>
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<td>DELTA 2010</td>
<td>IEEE International Symposium on Electronic Design, Test &amp; Applications</td>
<td>Ho Chi Minh City, Vietnam</td>
<td>Program Committee</td>
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<td>DFT 2010</td>
<td>IEEE International Symposium Defect and Fault Tolerance in VLSI Systems</td>
<td>Kyoto, Japan</td>
<td>Technical Program Committee</td>
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## Participation to Committees for Regional Conferences, International Workshops and Research Schools

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<td>DDECS 2009</td>
<td>IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems</td>
<td>Liberec, Czech Republic</td>
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<td>DTIS 2009</td>
<td>IEEE Design and Technology of Integrated Systems</td>
<td>Cairo, Egypt</td>
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<td>FDL 2009</td>
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<td>Lausanne, Suisse</td>
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<td>IMS3TW 2009</td>
<td>IEEE International Mixed-Signals, Sensors and Systems Test Workshop</td>
<td>Phoenix, Arizona, USA</td>
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<td>IWASI 2009</td>
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<td>Paris, France</td>
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<td>SPIE VLSI 2009</td>
<td>SPIE Microtechnologies for the New Millenium, Very Large</td>
<td>Dresden, Germany</td>
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<td>CARI 2010</td>
<td>African Conference on Research in Computer Science and Applied Mathematics</td>
<td>Yamoussoukro Côte d'Ivoire</td>
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<td>DASIP 2010</td>
<td>Conference on Design and Architectures for Signal and Image Processing</td>
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<td>DSN 2010</td>
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<td>FDL 2010</td>
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<td>HLDVT 2010</td>
<td>IEEE International High Level Design Validation and Test Workshop</td>
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<td>IDT 2010</td>
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<td>IMS3TW 2010</td>
<td>IEEE International Mixed-Signals, Sensors and Systems Test Workshop</td>
<td>La Grand Motte, France</td>
<td>Publicity Chair Publication Chair S. Mir H. Stratigopoulos</td>
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<td>LASCAS 2010</td>
<td>IEEE IEEE Latin American Symposium on Circuits and Systems</td>
<td>Iguazu, Brazil</td>
<td>Program Committee S. Mir</td>
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<td>MNM 2010</td>
<td>SPIE Microtechnologies for the New Millenium, VLSI Circuits and Systems II</td>
<td>Dresden, Germany</td>
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<td>MPSOC 2010</td>
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<td>Savannah, GA, USA</td>
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<td>PdeS 2010</td>
<td>IFAC Workshop on Programmable Devices and Embedded Systems</td>
<td>Pszczyna, Poland</td>
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<td>RSP 2010</td>
<td>IEEE Rapid Prototyping Workshop</td>
<td>Fairfax, Virginia, USA</td>
<td>Steering Committee F. Rousseau</td>
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<td>WTW 2010</td>
<td>IEEE Wireless Test Workshop</td>
<td>Santa Cruz, CA, USA</td>
<td>Program Committee Publicity Chair S. Mir</td>
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**Participation to Societies and Working Groups**

- Member of IEEE European Test Technology Technical Committee (S.Mir)
- Chair of IFIP 10.5 Working Group (D. Borrione)
- Member of IFIP 10.5 Working Group (S. Mir)
- Chapter Chair of the IEEE Solid-State Circuit society (Laurent Fesquet)
- Member of the Scientific Committee Council of the ENIAC (F. Pétrot)
Awards and distinctions

2009

- Best Paper Award at ASAP 2009 Conference (X. Guérin and F. Pétrot)
- Best Paper Award at FDL 2009 Conference (L. Ferro and L. Pierre)
- 2009 CISCO Award Recipient (Régis Leveugle)
- Elevation of L. Fesquet to the IEEE Senior Member grade, 2009
- Best Paper Award at 14th IEEE European Test Symposium 2009 (H. Stratigopoulos, S. Mir, E. Acar and S. Ozev)

2010

- Best Paper Award at VLSI-SoC 2010 (R. Khereddine, L. Abdallah, E. Simeu, S. Mir and F. Cenni)
- Best Paper Award at 8th IEEE International NEWCAS Conference 2010 (G. Waltisperger, C. Condemine, S.Basrou)
- Best Paper Award at the 9th Annual IEEE Conference on Sensors 2010 (Zhou Z. J., Rufer L., Wong M.)
13. National activities

Organisation of Workshops and open scientific project meetings

<table>
<thead>
<tr>
<th>ACRONYM</th>
<th>TITLE</th>
<th>LOCATION</th>
<th>ROLE</th>
<th>NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANR 2009</td>
<td>SESUR 2007 program (intermediate review of projects)</td>
<td></td>
<td>Member of the scientific committee</td>
<td>R. Leveugle</td>
</tr>
<tr>
<td>SEmba 2010</td>
<td>Journées Scientifiques SEmba</td>
<td>Autrans, France</td>
<td>Organizer</td>
<td>R. Echahed (LIG), D. Borrione, E. Simeu, F. Pétrot</td>
</tr>
<tr>
<td>SoCKET 2010</td>
<td>Présentation du projet SoCKET (Minalogic, Aerospace Valley)</td>
<td>Grenoble, France</td>
<td>Organizer</td>
<td>L. Pierre</td>
</tr>
<tr>
<td>ANR 2010</td>
<td>One project proposal in the &quot;White&quot; program</td>
<td></td>
<td>Reviewer</td>
<td>R. Leveugle</td>
</tr>
<tr>
<td>GDR 2010</td>
<td>&quot;Test and Fault Tolerance&quot; working group for the GDR SoC-SiP since 2007</td>
<td></td>
<td>Co-chair</td>
<td>R. Leveugle</td>
</tr>
</tbody>
</table>

Awards and distinctions

2009

- Distinction « Chevalier dans l’Ordre des Palmes Académiques » June 2009 (R. Leveugle)
- Prix de Thèse Grenoble-INP 2009 (Yannick Monnet)

2010

- Prix de Thèse Grenoble-INP 2010 (Pierre Guironnet de Massas)
- Prix de Thèse de doctorat 2010 mention innovation de EMB (Engineering in Medecine and Biology)
- IEEE France Section – SFGBM (Société Française de Génie Biologique et Médical) – AGBM avec le soutien du GDR STIC-Santé (Hamid Lamraoui)
14. Educational tasks

Dealing with problems risen by advanced technologies and proposing advanced design and test methodologies, TIMA members are, as a matter of fact, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into three categories: courses and tutorials, seminars, direction of Ph.D. students employed by French industrial companies (CIFRE program).

Courses and tutorials

The following table lists courses and tutorials that have been organized and given by members of the Laboratory, at different institutions request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA researchers or externally.

<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Speakers</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sup Télécom Bretagne</td>
<td>Grenoble, France</td>
<td>Jan. 09</td>
<td>4h</td>
<td>L. Fesquet</td>
<td>Thinking and Designing Different The Asynchronous Circuits</td>
</tr>
<tr>
<td>MIDEP</td>
<td>INP Grenoble France</td>
<td>March/09</td>
<td>8h</td>
<td>S. Basrour</td>
<td>Conception des microsystèmes</td>
</tr>
<tr>
<td>MIDEP</td>
<td>INP Grenoble</td>
<td>Dec. 09</td>
<td>8h</td>
<td>L. Anghel</td>
<td>VLSI Design</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>INP Grenoble</td>
<td>Feb/09 &amp; March/09</td>
<td>17h30</td>
<td>D. Borrione</td>
<td>Specification and verification</td>
</tr>
<tr>
<td>Ecole Nationale Supérieure des Mines de Saint-Étienne</td>
<td>Gardanne, France</td>
<td>Jan./09</td>
<td>18h</td>
<td>E. Simeu</td>
<td>Test and Fault Tolerance</td>
</tr>
<tr>
<td>University of Yaoundé I Mathematics and Computers department</td>
<td>Yaoundé Cameroon</td>
<td>July /09</td>
<td>20h</td>
<td>E. Simeu</td>
<td>Embedded Systems and Automatic Control</td>
</tr>
<tr>
<td>University of Mountains Sciences and Techniques Department</td>
<td>Banganté Cameroon</td>
<td>July /09</td>
<td>16h</td>
<td>E. Simeu</td>
<td>Embedded Control</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>INP Grenoble</td>
<td>Nov/09</td>
<td>20 h</td>
<td>G. Sicard</td>
<td>Conception de Circuits Analogiques</td>
</tr>
<tr>
<td>Sup Télécom Bretagne</td>
<td>Grenoble, France</td>
<td>Jan. 09</td>
<td>6h</td>
<td>L. Anghel</td>
<td>Test de circuits numériques</td>
</tr>
<tr>
<td>Sup Télécom Bretagne</td>
<td>Grenoble, France</td>
<td>Jan 10</td>
<td>4h</td>
<td>L. Fesquet</td>
<td>Thinking and Designing Different The Asynchronous Circuits</td>
</tr>
<tr>
<td>SERESSA 2009 (Summer School)</td>
<td>Takasaki, JAPON</td>
<td>Dec./09</td>
<td>2h</td>
<td>R. Velazco</td>
<td>Soft Error rate prediction</td>
</tr>
<tr>
<td>Máster de Sistemas Electrónicos Avanzados</td>
<td>Univ. Carlos III, Leganés, Spain</td>
<td>May-June 2009</td>
<td>10 h</td>
<td>R. Velazco</td>
<td>Reliability, validation and test of digital systems</td>
</tr>
<tr>
<td>IEEE International Conference on Signals, Circuits &amp; Systems (SCS)</td>
<td>Djerba, Tunisie</td>
<td>Nov/09</td>
<td>3h</td>
<td>R. Leveugle</td>
<td>Integrated and embedded systems security: hardware-based threats and solutions</td>
</tr>
<tr>
<td>MATRI Project Tutorial</td>
<td>INPG, Grenoble France</td>
<td>Dec/09</td>
<td>6h</td>
<td>D. Borrione</td>
<td>Formal and Semi-Formal Verification</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>Inp Grenoble</td>
<td>Jan-March 2010</td>
<td>14h</td>
<td>D. Borrione</td>
<td>Specification and verification</td>
</tr>
</tbody>
</table>
Open Seminars at TIMA

In addition to internal seminars, the Laboratory regularly publicises talks given by our visiting researchers. Grenoble academic and industrial researchers had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. Marvasti</td>
<td>Université Sharif de Téhéran</td>
<td>06/01/09</td>
<td>Sparse Signal Processing</td>
</tr>
<tr>
<td>Dr. Abel Soudani</td>
<td>Université de Monastir, Tunisie</td>
<td>02/06/09</td>
<td>Transport des images et qualité du service dans les réseaux de capteurs sans fil</td>
</tr>
<tr>
<td>Prof. I. Koren</td>
<td>University of Massachusetts, Amherst</td>
<td>10/06/09</td>
<td>Managing Resources for High Performance and Low Energy in General-Purpose Processors</td>
</tr>
<tr>
<td>Prof. George Jie YUAN</td>
<td>Hong Kong University of Science &amp; Technology</td>
<td>02/07/09</td>
<td>Mixed-signal IC Techniques for Bio-Medical Applications</td>
</tr>
<tr>
<td>Dr. Przemysław Śliwiński</td>
<td>Institute of Engineering Cybernetics, Wroclaw University of Technology, Poland</td>
<td>04/02/10</td>
<td>Wavelets and their applications to autofocusing and asynchronous analog-to-digital conversion</td>
</tr>
<tr>
<td>Prof. Joseph ALTET</td>
<td>Universitat politècnica de Catalunya, Spain</td>
<td>19/05/10</td>
<td>Thermal Coupling in Integrated Circuits : Applications to the Test and Characterization of Analogue and Digital Circuits</td>
</tr>
<tr>
<td>Prof. Mark C. REED</td>
<td>Australian National University (ANU), Canberra</td>
<td>31/05/10</td>
<td>WCDMA Femtocell Research: Challenges with real-time FPGA realization</td>
</tr>
<tr>
<td>Prof. Kees GOOSSENS</td>
<td>Faculty of Electrical Engineering, Eindhoven University of Technology (Netherlands)</td>
<td>09/09/10</td>
<td>MPSOC Performance Virtualisation for enhanced robustness and performance verification</td>
</tr>
<tr>
<td>Prof. Alkis HATZOPoulos</td>
<td>Aristotle University of Thessaloniki, Greece</td>
<td>16/09/10</td>
<td>Analog design, modeling, and testing</td>
</tr>
<tr>
<td>Dr Modris Greitans</td>
<td>IECS, Riga, Latvia</td>
<td>12/10/10</td>
<td>Non uniform Sampling : Architecture and Signal Processing</td>
</tr>
</tbody>
</table>
### Seminars and invited talks given by TIMA members

Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions:

<table>
<thead>
<tr>
<th>Institution</th>
<th>Location</th>
<th>Date</th>
<th>Speaker</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMSA (Univ. Mayor de San Andrés)</td>
<td>La Paz, Bolivia</td>
<td>11/05/10</td>
<td>R. Velazco</td>
<td>Effects of Radiation on Integrated Circuits: origins, mitigation techniques, test and real-life experiments</td>
</tr>
<tr>
<td>Universidad Nacional del Altiplano (UNA)</td>
<td>Trujillo, Peru</td>
<td>19/09/10</td>
<td>R. Velazco</td>
<td>Effects of Radiation on Integrated Circuits: origins, mitigation techniques, test and real-life experiments</td>
</tr>
<tr>
<td>Carengie Mellon University, ECE</td>
<td>Pittsburgh</td>
<td>30/10/10</td>
<td>L. Anghel</td>
<td>NOC Fault Tolerant Design</td>
</tr>
<tr>
<td>Pontificia Universidad Católica de Chile</td>
<td>Santiago, Chile</td>
<td>16/11/10</td>
<td>S. Mir</td>
<td>Built-in-self-test techniques for analog/mixed-signal/RF/MEMS: design and evaluation</td>
</tr>
<tr>
<td>Universidad de Chile</td>
<td>Santiago, Chile</td>
<td>17/11/10</td>
<td>S. Mir</td>
<td>Built-in-self-test techniques for analog/mixed-signal/RF/MEMS: design and evaluation</td>
</tr>
<tr>
<td>Universidad Técnica Federico Santa María</td>
<td>Valparaiso, Chile</td>
<td>18/11/10</td>
<td>S. Mir</td>
<td>Built-in-self-test techniques for analog/mixed-signal/RF/MEMS: design and evaluation</td>
</tr>
<tr>
<td>Universidad de Concepción</td>
<td>Concepción, Chile</td>
<td>19/11/10</td>
<td>S. Mir</td>
<td>Built-in-self-test techniques for analog/mixed-signal/RF/MEMS: design and evaluation</td>
</tr>
<tr>
<td>UNPSJB (Universidad Nacional de la Patagonia San Juan Bosco)</td>
<td>Puerto Madryn, Argentina</td>
<td>07/12/10</td>
<td>R. Velazco</td>
<td>Error Prediction in programmable circuits: Methodology, tools and studied-cases</td>
</tr>
<tr>
<td>UNPSJB (Universidad Nacional de la Patagonia San Juan Bosco)</td>
<td>Puerto Madryn, Argentina</td>
<td>07/12/10</td>
<td>R. Velazco</td>
<td>A Software approach to deal with soft-errors in applications implemented in programmable circuits</td>
</tr>
</tbody>
</table>
University/industry joint research programs

A French national program, called CIFRE, allows French companies to host Ph.D. students. The thesis director must belong to a French University or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company.

TIMA researchers have been asked by companies to direct several Ph.D. theses in the CIFRE framework. The most recent ones are listed in the table below.

<table>
<thead>
<tr>
<th>Company / Institute</th>
<th>Student</th>
<th>Ph D. Advisor</th>
<th>Dur.</th>
<th>Research Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>STMicroelectronics</td>
<td>N. Ben Hassine</td>
<td>S. Basrour</td>
<td>Oct. 2009</td>
<td>Reability of BAW resonators</td>
</tr>
<tr>
<td>EADS</td>
<td>A. Bocquillon</td>
<td>R. Velazco</td>
<td>Oct. 2009</td>
<td>Evaluation de la sensibilité des FPGAS SRAM-BASED face aux erreurs produits par les radiations naturelles</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>F. Abouzeid</td>
<td>M. Renaudin / G. Sicard</td>
<td>Sept. 2010</td>
<td>Subthreshold architecture and digital circuits study in 45 &amp; 32nm CMOS technology</td>
</tr>
<tr>
<td>STE</td>
<td>O. Elissati</td>
<td>L. Fesquet</td>
<td>Feb. 2011</td>
<td>Low-phase noise asynchronous oscillators</td>
</tr>
<tr>
<td>EADS</td>
<td>A. Bougerol</td>
<td>R. Leveugle</td>
<td>Sept. 2011</td>
<td>Study of failure modes induced par natural radiative environment on memory based complex devices</td>
</tr>
<tr>
<td>EADS</td>
<td>S. Houssany</td>
<td>R. Leveugle</td>
<td>Fev. 2013</td>
<td>Evaluation methodology of microprocessor sensitivity to cosmic radiations</td>
</tr>
</tbody>
</table>
15. Publications

PEER-REVIEWED JOURNAL ARTICLES (ACL)

THEME 1: Architectures for robust and complex integrated systems

2009

1. PERONNARD P., VELAZCO R., HUBERT G.
   Real-life SEU experiments on 90nm SRAMs in Atmospheric Environment: measure vs. predictions done by means of MUSCA SE3P platform

2010

2. BERGAOUI S., VANHAUWAERT P., LEVEUGLE R.
   A new critical variable analysis in processor-based systems
   IEEE Transactions on Nuclear Science, Vol. 57, No. 4, part 1, August 2010

3. CANIVET G., MAISTRI P., LEVEUGLE R., CLE DIERE J.*, VALETTE F.*, RENAUDIN M.***
   Glitch and laser fault attacks onto a secure AES implementation on a SRAM-based FPGA
   Journal of Cryptology, Springer, published online October 26, 2010 (paper version pending)
   * CESTI/CEA-LETI, France; ** DGA/CELAR, France; *** Tiempo, France

4. IDRISS T., ZIADE H., AYOUBI R., VELAZCO R.
   A new fault injection approach to study the impact of bitflips in the configuration of SRAM-based FPGAs
   International Arab Journal on Information Technology (IAJIT), in press, accepted

THEME 2: Design of integrated devices, circuits and systems

2009

5. BEN HASSINE N.*,**, MERCIER D.*, RENAUX PH.*, PARAT G.*, BASROUR S., WALTZ P.*, CHAPPAZ C.*, ANCEY P.*, BLONKOWSKI S.*
   Dielectric properties of Metal-Insulator-Metal Aluminium Nitride structures: measurement and modeling
   *CEA-LETI/MINATEC, DRT/DIHS, Grenoble, France; **STMicroelectronics, Crolles, France

6. HAMON J., FESQUET L., MISCOPEIN B.*, RENAUDIN M.**
   Constrained Asynchronous Ring Structures for Robust Digital Oscillators
   * Orange Labs, France Telecom, Meylan, France; ** Tiempo SAS, Montbonnot St Martin, France

   Surface Acoustic Wave Excitation on SF6 plasma treated AlGaN/GaN heterostructure
   Vacuum Journal (Elsevier), Vol.84, No.1, pp.231-234, 2009
   * Institute of Electrical Engineering of the Slovak Academy of Sciences, Bratislava, Slovakia; ** Slovak University of Technology, Faculty of Electrical Engineering and Information Technology, Department of Microelectronics, Bratislava, Slovakia; *** International Laser Center, Bratislava, Slovakia

8. MARZENCKI M.*, DEFOSSÉUX M., BASROUR S.
   MEMS energy harvesting device with passive resonance frequency adaptation capability
   * CiBER Laboratory, Simon Fraser University, Burnaby, Canada; ** CEA-LETI, Minatec, Grenoble, France

155
9 QAISAR S.-M., FESQUET L., RENAUDIN M.
A Signal Driven Adaptive Resolution Short-Time Fourier Transform

10 QAISAR S.-M., FESQUET L., RENAUDIN M.
Signal Driven Sampling and Filtering : A Promising Approach for Time Varying Signals Processing

11 QAISAR S.-M., FESQUET L., RENAUDIN M.
Adaptative Rate Sampling and Filtering based on level crossing sampling
Eurasip Advances in Signal Processing, Accepted 14th April 2009

12 TERRASSON G., BRIAND R., BASROUR S.
A Design Technique for Power Constrained CMOS Low-Noise Amplifier Dedicated to Wireless Sensor Networks
Journal of Low Power Electronics (JOLPE), Vol. 5, N° 2, August 2009

13 TOUNSI F., MEZGHANI B.*, RUFE R., MASMoudi M.*, MIR S.
Electromagnetic Investigation of a CMOS MEMS Inductive Microphone
* Groupe de Recherche en Microtechnologie et Système sur puce, Sfax, Tunisia

2010

14 ALLAIN M.*, BERTHIER J.*, BASROUR S., POUTEAU P.*
Electrically actuated sacrificial membranes for valving in microsystems
Journal of Micromechanics and Microengineering, Vol. 20, N°3, 035006 (7pp), March 2010
*CEA-LETI, Grenoble, France

15 BOUSSETTA H., MARZENCKI M.*, BASROUR S., SOUDANI A.**
Efficient Physical Modeling of MEMS Energy Harvesting Devices With VHDL-AMS
ISSN: 1530-437X. Digital Object Identifier: 10.1109/JSEN.2010.2044786
* CIBER Laboratory, Simon Fraser University, Burnaby, BC, Canada; Electronic and Microelectronic Laboratory (EµE), Faculté de Sciences de Monastir, Avenue de l’environnement 5019 Monastir, Tunisia

16 CENNI F., CAZALBOU J., MIR S., RUFE R. L.
Design of a SAW-based chemical sensor with its microelectronics front-end interface

17 FESQUET L., BIDÉGARA Y B.
IIR Digital Filtering of Non-uniformly Sampled Signals via State Representation

18 JEAN-MISTRAL C.*, BASROUR S., CHAILLOUT J.J.*
Comparison of electroactive polymers for energy scavenging applications
Smart Materials and Structures, 19(8):085012, 2010
* CEA-LETI, Grenoble, France

19 JEAN-MISTRAL C.*, BASROUR S., CHAILLOUT J.J.*
Modelling of dielectric polymers for energy scavenging applications
Smart Materials and Structures, 19(10):105006, 2010
* CEA-LETI, Grenoble, France

20 JEAN-MISTRAL C.*, BASROUR S., CHAILLOUT J.J.*
Dielectric properties of polycrylate thick films used in sensors and actuators
Smart Materials and Structures, 19(7):075019, 2010
* CEA-LETI, Grenoble, France
Development of a Novel Artificial Urinary Sphincter: a Versatile Automated Device
IEEE/ASME Transactions on Mechatronics, D.O.I 10.1109/TMECH.2010.2056927, 3 Aug. 2010
* Hôpital CHARLES-FOIX - JEAN-ROSTAND – APHP, Service Médecine physique et réadaptation, Ivry sur Seine, France; Laboratoire TIMC, IMAG, La Tronche, France

22 POSSAMAI BASTOS R.*, SICARD G., KASTENSMIDT F.*, RENAUDIN M.**, R. REIS*
Asynchronous circuits as alternative for mitigation of long-duraction transient faults in deep-submicron technologies
* UFRGS, Instituto de Informática, PGMicro/PPGC, Porto Alegre, RS, Brazil; ** Tiempo, 38330 Montbonnot Saint Martin, France

Step toward robust and reliable amorphous polymer field-effect transistors and logic functions made by the use of roll to roll compatible printing processes
* CEA-LETI, Grenoble, France

THEME 3 : Design and verification of System-on-Chip architectures

2009

24 BORRIONE D., HELMY A., PIERRE L., SCHMALTZ J.*
A Formal Approach to the Verification of Networks on Chip
EURASIP Journal on Embedded Systems, Volume 2009, Article ID 548324, 14 pages, 2009,
* Institute for Computing and Information Sciences, Radboud University, Nijmegen, The Netherlands

Gradual Refinement for Application Specific MPSoC Design from Simulink Model to RTL Implementation
Journal of Zhejiang University SCIENCE A co-published with Springer-Verlag GmbH, Zhejiang University Press, ISSN 1862-1775, Volume 10, Number 2, February 2009
* Institute of Vlsi Design, Zhejiang University, China; ** Seoul National University, South Korea; *** CEAS-LETI, Grenoble, France; **** Informatics Institute, Federal University of Rio Grande do Sul, Brazil

Simulink(R) based Heterogeneous Multiprocessor SoC Design Flow for Mixed Hardware/Software Refinement and Simulation Integration, the VLSI Journal (Elsevier), Vol. 42, No. 2, February 2009
* Seoul National University, South Korea; **Informatics Institute, Federal University of Rio Grande do Sul, Brazil; *** CEA-LETI, Grenoble, France; **** Institute of Vlsi Design, Zhejiang University, China

2010

28 GUIRONNET DE MASSAS P., PETROT F.
Evaluation of the implementation cost of cache coherence protocols using omniscient actions
29 MEUNIER Q., PETROT F.
Lightweight Transactional Memory systems for NoCs based architectures: Design, implementation and comparison of two policies

30 MEUNIER Q., PETROT F., ROCH J.-L.*
Hardware/software support for adaptive work-stealing in on-chip multiprocessor
* LIG, INP Grenoble and INRIA, Montbonnot Saint-Martin(38), France

31 MULLER O., BAGHDADI A.*, JÉZÉQUEL M.*
Parallelism Efficiency in Convolutional Turbo Decoding
EURASIP Journal on Advances in Signal Processing, vol. 2010, Article ID 927920, 11 pages,
*Institut Telecom, Telecom Bretagne, Université Européenne de Bretagne, UMR CNRS 3192
Lab-STICC, Technopôle Brest iroise, CS 83818, 29238 Brest, France

32 MORIN-ALLORY K., BOULÉ M., BORRIONE D., ZILIC Z.
Validating Assertion Language Rewrite Rules and Semantics with Automated Theorem Provers
IEEE Trans. on CAD, Vol 29, N° 9, September 2010

THEME 4 : Reliable Mixed-signal / RF circuits and systems

2009

33 DHAYNI A., MIR S., RUFER L., SIMEU E., BOUNCEUR A.
Pseudorandom BIST for test and characterization of linear and nonlinear MEMS

34 STRATIGOPOULOS H., MIR S., BOUNCEUR A.
Evaluation of analog/RF test measurements at the design stage

2010

35 STRATIGOPOULOS H., DRINEAS P., SLAMANI M., MAKRIS Y.
RF Specification Test Compaction Using Learning Machines
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.18, No.6, June 2010

ARTICLES IN PEER-REVIEWED CONFERENCE PROCEEDINGS (ACT)

THEME 1 : Architectures for robust and complex integrated systems

2009

36 BAARIR S.*, BRAUNSTEIN C.*, CLAVEL R., ENCRENAZ E.*, ILIE J.-M.*, LEVEUGLE R.,
MOUNIER I.*, PIERRE L., POITRENAUD D.*
Complementary formal approaches for dependability analysis
The 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,
* LIP6, France

37 BERGAOUI S., VANHAUWAERT P., LEVEUGLE R.
A new critical variable analysis in processor-based systems
European Conference on Radiation Effects on Components and Systems (RADECS'09),
Bruges, Belgium, September 14-18, 2009
38 BERGAOUI S., LEVEUGLE R.
IDSM: An improved control flow checking approach with disjoint signature monitoring
Conference on Design of Circuits and Integrated Systems (DCIS), Zaragoza, Spain, pp. 249-254, November 18-20, 2009

39 CANIVET G., LEVEUGLE R., CLEDIERE J.*, VALETTE F.**, RENAUDIN M.***
Characterization of effective laser spots during attacks in the configuration of a Virtex-II F
27th IEEE VLSI Test Symposium (VTS'09), Santa Cruz, california, USA, May 3-7, 2009
* CESTI/CEA-LETI, France; ** DGA/CERAR, France; *** Tiempo, France

40 FERRON J.B., ANGHEL L., LEVEUGLE R., BOCCULLION A.*, MILLER F.*, MANTELET G.**
A methodology and tool for predictive analysis of configuration bit criticality in SRAM-based
FPgas: experimental result
3rd International Conference on Signals, Circuits & Systems (SCS), Djerba, Tunisia, November 6-8, 2009
* EADS IW, France; ** Atmel, France

41 FERRON J.-B
Predictive Analysis of Configuration Bit Criticality in SRAM-Based FPgas. Methodology, tool, and
results
RADFAC’09, Grenoble, France, April 9, 2009

42 FERREYRA P.*, BRAC E.*., VELAZCO R., MARQUES C.*
Test and Qualification of a Fault Tolerant FPGA Based Active Antenna System for Space
Applications
Proc.of Latin American Test Workshop (LATW’09), Buzios,Brazil, March 3-5, 2009
* Facultad de Matematica Astronomica y Fisica de la Univ. Nacional de Cordoba, Argentina

43 FERREYRA P.*, BRAC E.*., VELAZCO R., MARQUES C.*
A New Automatic VHDL Fault Injection Tool: A case studied
* Facultad de Matematica Astronomia y Fisica de la Univ. Nacional de Cordoba, Argentina

44 HUBERT G., VELAZCO R., PERONNARD P.
A generic Plateform for Remote accelerated tests and high altitude SEU experiments on
Advanced ICS
International On-Line Test Symposium (IOLTS’09), Sesimbra (Portugal), pp. 180, June 24-26, 2009

45 IDRISS T., ZIADE H., AYOUBI R., VELAZCO R.
MSI: A Multiple SEU Injection Method for FPgas
International Conference on Information Science, Technology and Applications (ISTA’09), Kuwait,
March 20-22, 2009

Enhanced Self-Configurability and Yield in Multicore Grids
15th IEEE International On-Line Testing Symposium (IOLTS’09), Sesimbra-Lisbon, Portugal,
June 24-27, 2009
*Department of Informatics, University of Piraeus, Greece; **LAAS-CNRS, Toulouse, France; ***Dep.
of Microelectronics and Computer Science, Technical University of Lodz, Poland

47 LEVEUGLE R., CALVEZ A., VANHAUWAERT P., MAISTRI P.
Precisely Controlling the Duration of Fault Injection Campaigns: a Statistical View
4th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale
Era (DTIS’09), 2009

48 LEVEUGLE R., CALVEZ A., MAISTRI P., VANHAUWAERT P.
Statistical Fault Injection: Quantified Error and Confidence
Design, Automation and Test in Europe (DATE ’09), 2009

49 LEVEUGLE R., PIERRE L., MAISTRI P., CLAVEL R. (Commun)
Soft Error Effect and Register Criticality Evaluations: Past, Present and Future
Proc. IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE’09), Stanford (CA),
March 24-25, 2009
50 MAINGOT V., LEVEUGLE R.
Influence of error detecting or correcting codes on the sensitivity to DPA of an AES S-Box
3rd International Conference on Signals, Circuits & Systems (SCS'09), Djerba, Tunisia,
November 6-8, 2009

51 MAISTRI P., LEVEUGLE R.
Toward automated fault pruning with Petri nets
15th IEEE International on-line Testing Symposium (IOLTS'09), June 24-26, 2009

52 MAISTRI P., LEVEUGLE R.
Early pruning of soft errors and transient faults with Petri nets
Electronic Symposium Digest of 14th IEEE European Test Symposium, Sevilla, Spain, May 25-29,
2009

53 MAISTRI P.
Pruning Single Event Upset Faults with Petri Nets
10th IEEE Latin-American Test Workshop (LATW’09), Armacao de Buzios, Brazil, March 2-5,
2009

54 NICOLAIDIS M.
Simulating Time
Proceedings Computing and Philosophy Symposium, AISB 2009 Convention (Adaptive &
Emergent Behaviour & Complex Systems), April 6-9, Edinburgh, UK

55 NICOLAIDIS M.
Computational Space, Time and Quantum Mechanics
7th European Computing and Philosophy Conference, (ECAP’09), Barcelona, Spain, July 2-4
2009

56 NICOLAIDIS M.
Emergence of Relativistic Space-Time in a Computational Universe
7th European Computing and Philosophy Conference, (ECAP’09), Barcelona, Spain, July 2-4,
2009

57 PERONNARD P., VELAZCO R., CABANILLAS E., AL FALOU W., ZIADE H.
Evaluation of the soft error rate of a space application executed by a real time operating system
MESM 2009, Beyrouth, Liban, September 27-29, 2009

58 PERONNARD P., SILVA CARDENAS C., FERNANDEZ S., VELAZCO R.
High altitude experiments to evaluate SEU sensitivity of advanced SRAMs

59 PERONNARD P., VELAZCO R., HUBERT G.
Real-life SEU experiments on 90nm SRAMS in Atmospheric Environment : measure vs.
predictions done by means of MUSCA SEP3 platform,
IEEE Nuclear and Space Radiation Effects Conference (NSREC’09), Québec City, Canada,
July 20–24, 2009

60 PIERRE L., CLAVEL R., LEVEUGLE R. (Commun)
ACL2 for the Verification of Fault-Tolerance Properties: First Results
International Workshop on The ACL2 Theorem Prover and Its Applications (ACL2’09), Boston
(MA), USA, May 11-12, 2009

61 RUSU CL., ANGHEL L., AVRESKY D.*
Message routing in 3D networks-on-chip
NORCHIP Conference 2009, Trondheim, Norway, November 16-17
* IRIANC

62 TORRELLAS S., NICOLESCU B., VALDERAS M. G., VELAZCO R., SAVARIA Y.
Validation by fault injection of a Software Error Detection Technique dealing with critical Single
Event Upsets
Proceedings of Latin American Test Workshop (LATW’06), pp.111-116, Buenos Aires, Argentine,
March 26-29 2006
63 RUSU C.L., ANGHEL L., AVRESKY D.*
Message routing in 3D networks-on-chip
NORCHIP Conference 2009, Trondheim, Norway, November 16-17
* IRIANC

64 VANHAUWAERT P., LEVEUGLE R.
Efficiency of probabilistic testability analysis for soft error effect analysis: a case study
Design and Technology of Integrated Systems (DTIS’09), Cairo, Egypt, April 6-7, 2009

65 YU H., NICOLAIDIS M., ANGHEL L.
An effective approach to detect logic soft errors in digital circuits based on GRAAL
10th International Symposium on Quality of Electronic Design (ISQED’09), San Jose, CA, USA,
March 16-18, 2009

2010

66 BERGAOUI S., LEVEUGLE R.
Impact of compilation options on the criticality of registers in a microprocessor-based system
1st IEEE Latin American Symposium on Circuits and Systems (LASCAS’10), Iguaçu Falls, Brazil,
February 24-26, 2010, pp. 216-219

67 BOUGEROL A.*, MILLER F.*, GUIBBAUD N.**, LEVEUGLE R., CARRIERE T.***, BUARD N.*
Experimental demonstration of pattern influence on DRAM SEU & SEFI radiation sensitivities
11th European Conference on Radiation and its Effects on Components and Systems (RADECS),
Längelfeld, Austria, September 20-24, 2010
* EADS IW, Suresnes, France; ** APTUS, France; *** EADS Astrium Space Transportation, Les
Mureaux, France

68 CANIVET G., MAISTRI P., LEVEUGLE R., VALETTE F.*, CLÉDIÈRE J.**, RENAUDIN M.***
Robustness evaluation and improvements under laser-based fault attacks of an AES crypto-
processor implemented on a SRAM-based FPGA
15th IEEE European Test Symposium, Prague, Czech Republic, May 24-28, 2010, pp. 251
* DGA/CERAl, France; ** CESTI/CEA-LETI, France; *** Tiempo, France

69 CANIVET G., MAISTRI P., LEVEUGLE R., VALETTE F.*, CLEDIERE J.**, RENAUDIN M.***
Dependability analysis of a countermeasure against fault attacks by means of laser shots onto a
SRAM-based FPGA
21st IEEE International Conference on Application-specific Systems, Architectures and Processors
(AASP'10), Rennes, France, July 7-9, 2010
* DGA/CERAl, France; ** CESTI/CEA-LETI, France; *** Tiempo, France

70 CHAIX F., AVRESKY D., ZERGAI NOH N. E., NICOLAIDIS M.
Fault-Tolerant Deadlock-Free Adaptive Routing for Any Set of Link and Node Failures in Multi-
Cores Systems
9th IEEE International Symposium on Network Computing and Applications (NCA10), Cambridge,
MAE, July 15-17, 2010

71 KOLONIS E., NICOLAIDIS M.
Simulating Time with Computers: implementation and experimentations
8th European Conference on Computing and Philosophy (ECAP’10), Munich, Germany, October
4-6 2010, pp. 496-501, Verlag Dr. Hut, ISBN 978-3-86853-546-4

72 LEVEUGLE R., PROST-BOUCLE A.
A new automated instrumentation for emulation-based fault injection
1st IEEE Latin American Symposium on Circuits and Systems (LASCAS’10), Iguaçu Falls, Brazil,
February 24-26, 2010, pp. 220-223

73 LEVEUGLE R., BEN JRAD M.
A new methodology for accurate predictive robustness analysis of designs implemented in SRAM-
based FPGAs
IEEE International Conference on Electronics, Circuits and Systems (ICECS’10), Athens, Greece,
December 12-15, 2010
74 NICOLAIDIS M.
Simulating Time with Computers
North American Computing And Philosophy Conference (NACAP’10), Carnegie Mellon University, Pittsburgh, Pennsylvania, July 24-26, 2010

75 NICOLAIDIS M., PASCA V., ANGHEL L.
Interconnect Built-In Self-Repair and Adaptive-Serialization (I-BIRAS) for 3D Integrated Systems
16th IEEE International On-Line Testing Symposium (IOLTS’10), Corfu, Greece, July 5–7, 2010

76 PASCA V., ANGHEL L., BENABDENBI M.
Fault Resilient Intra-die and Inter-die Communication in 3D Integrated Systems.
Proceedings of PhD Research in Microelectronics and Electronics Conference (PRIME’10), Berlin, Germany, July 18-21, 2010

77 PASCA V., ANGHEL L., RUSU C., BENABDENBI M.
Configurable Serial Fault-Tolerant Link for Communication in 3D Integrated Systems
Proceedings of International On-Line Test Symposium (IOLTS’10), Corfu, Greece, July 3-7, 2010

78 PASCA V., ANGHEL L., BENABDENBI M.
Fault Tolerant Communication in 3D Integrated Systems.
Proceedings of DSN Workshop on Dependable Systems and Networks (WDSN’10), Chicago, USA, June 28, 2010

79 PASCA V., ANGHEL L., RUSU C., BENABDENBI M.
Non-regular 3D mesh Networks-on-Chip
Proceedings of DAC Workshop on Diagnostic Services in Network-on-Chips (DSNoC’10), Anaheim, USA, June 13, 2010

80 PASCA V., ANGHEL L., RUSU C., BENABDENBI M.
Configurable Fault-Tolerant Link for Inter-die Communication in 3D on-Chip Networks
European Test Symposium (ETS’10), Prague, Czech Republic, May 24-28, 2010

81 PASCA V., ANGHEL L., RUSU C., LOCATELLI R., COPPOLA M.
Error Resilience of Inter-Die and Intra-Die Communication with 3D Spidergon STNoC
Design Automation and Test in Europe Conference, (DATE’10), Dresden, Germany, March 8-12, 2010

82 RUSU C., ANGHEL L., AVRESKY D.*
RILM: Reconfigurable inter-layer routing mechanism for 3D multi-layer networks-on-chip.
Proceedings of International On-Line Testing Symposium (IOLTS’10), Corfu, Greece, July 3-7, 2010
* IRIANC

83 RUSU C., ANGHEL L.
Checkpoint and rollback recovery in network-on-chip based systems
Student forum at 15th Asia and South Pacific Design Automation Conference (ASP-DAC’10), Taipei, Taiwan, January 18-21, 2010

THEME 2 : Design of integrated devices, circuits and systems

2009

84 ABOUZEID F., CLERC S., RENAUDIN M., SICARD G.
Ultra-Low Voltage from 65nm to 32nm
8èmes Journées Faible Tension Faible Consommation (FTFC’09), Neuchatel, Switzerland, June 3-5, 2009
*CEA-LETI, Minatec, Grenoble, France
85 ABOUZEID F.*, CLERC S.*, FIRMIN F.*, RENAUDIN M.*, SICARD G.
A 45nm CMOS 0.35V-Optimized Standard Cell Library for Ultra-Low Power Applications IEEE The International Symposium on Low Power Electronics and Design (ISLPED'09), San Francisco, USA, August 19-21, 2009
* STMicroelectronics, Crolles, France; ** TIEMPO SAS, Grenoble, France

86 ALLAIN M.*, BERTHIER J., BASROUR S., POUTEAU P.*
Sacrificial membranes for serial valving in Microsystems Nanotech 2009 Conference, Houston, TX, May 03-07, 2009, 343-346
*CEA-LETI, Minatec, Grenoble, France

87 ALSAYEG K., FESQUET L., SICARD G, RIOS D., RENAUDIN M.*
Optimizing speed and consumption of QDI controllers using direct mapping synthesis NEWCAS 2009, Toulouse, France, June 28-July 1, 2009
* TIEMPO SAS, Grenoble, France

*STMicroelectronics, Crolles Cedex, France
** CEA-LETI/MINATEC, Grenoble Cedex, France
***Ecole Nationale Supérieure des Mines de Saint-Etienne, Saint-Etienne, France

89 BEN HASSINE N., MERCIER D.*, RENAU PX P.*
SMR Under High Power Study For Reliability 5th International Conference on Ph.D. Research in Microwtronics & Electronics 5PRIME 2009, Cork, Ireland, 12-17 July 2009
* CEA-LETI/MINATEC, Grenoble Cedex, France

90 BEYROUTHY T., FESQUET L.
DPA robust S-BOX implementation on a secure asynchronous FPGA Cryptarchi Conference, June 24-27, 2009, Prague, Poland

91 BIDEGARAY-FESQUET B., FESQUET L.
A fully nonuniform approach to FIR filtering Sampling Theory and Applications (SampTA’09), Marseille, France, May12-18, 2009

92 CARLIOZ L., DELAMARE J., BASROUR S.
Temperature Threshold Tuning Of A Thermal Harvesting Switch The 15th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers'09), Denver Colorado, June 21-25, 2009

93 CUGAT O., BASROUR S., DELAMARE J., JEAN-MISTRAL C., DEFOSSEUX M.*, CARLIOZ L., MARZENCKI M.,
* CEA-LETI, Minatec, Grenoble, France; ** CIBER Laboratory, Simon Fraser University, Burnaby, Canada

94 DEFOSSEUX M.*, MARZENCKI M.*, BASROUR S.
Piezoelectric vibration harvesting device with automatic resonance frequency tracking capability Material Research Society - Fall MEETING, Boston, USA, November 30 - December 4, 2009
* CEA-LETI, Minatec, Grenoble, France; ** CIBER Laboratory, Simon Fraser University, Burnaby, Canada

95 ELISSATI O., YAHYA E., FESQUET L., RIEUBON S.

96 GHANDOUR S.*, DESPESSE G.*, BASROUR S.
Theoretical Analysis of A New Memes Approach To Build A High Efficiency Fully Integrated DC-DC Converter 20th Micromechanics Europe Workshop (MME’09), Toulouse, France, September 20-22, 2009
Updates on the Potential of Clock-Less Logics to Strengthen Cryptographic Circuits against Side-  
Channel Attacks  
IEEE International Conference on Electronics and Systems (ICECS’09), Hammamet, Tunisia,  
December 13-16, 2009  
*Télécom Paris Tech

98 MURALT P.*, MARZENCKI M.**, BELGACEM B.*, CALAME F.*, BASROUR S.  
Vibration Energy Harvesting with PZT Micro Device  
Proceedings of The Eurosensors XXIII Conference, Procedia Chemistry, Volume: 1, Issue: 1,  
Lausanne, Switzerland, Sept. 6 - 9, 2009, 1191-1194  
* Ceramics Laboratory, EPFL, Lausanne, Switzerland*; ** CiBER Laboratory, Simon Fraser  
University, Burnaby, Canada

99 MURALT P.*, MARZENCKI M.**, BELGACEM B.*, CALAME F.*, BASROUR S.  
Vibration Energy Harvesting with PZT Micro Device  
* Ceramics Laboratory, EPFL, Lausanne, Switzerland*; ** CiBER Laboratory, Simon Fraser  
University, Burnaby, Canada

100 POSSAMAI BASTOS R., MONNET Y., SICARD G., KASTENSMIDT F., RENAUDIN M.*, REIS R.  
Comparing Transient-Fault Effects on Synchronous and on Asynchronous Circuits  
15th IEEE International On-Line Testing Symposium (IOLTS’09), Sesimbra-Lisbon, Portugal,  
June 24-27, 2009

101 POSSAMAI BASTOS R., MONNET Y., SICARD G., KASTENSMIDT F., RENAUDIN M.*, REIS R.  
A Methodology to Evaluate Transient-Fault Effects on Asynchronous and Synchronous Circuits  
14th IEEE European Test Symposium (ETS’09), Sevilla, Spain, May 25 -29, 2009

102 POSSAMAI BASTOS R., MONNET Y., SICARD G., KASTENSMIDT F., RENAUDIN M., REIS R.  
Comparing Transient-Fault Effects on Synchronous and on Asynchronous Circuits  
15th IEEE International On-Line Testing Symposium (IOLTS’09), Sesimbra-Lisbon, Portugal,  
June 24-27, 2009

103 QAISAR S. M., FESQUET L., RENAUDIN M.  
Effective Resolution of an Adaptive Rate ADC  
Sampling Theory and Applications (SampTA’09), Marseille, May 12-18, 2009

104 RASLAN A., BASROUR S., LE POCHE H.  
Design and Fabrication of Electromechanical Tweezers based on CNT Ropes  
Nanotech 2009 Conference, Houston, TX, May 03-07, 2009, 425-428

105 THABUIS T., VILLARD P., BELLEVILLE M., SICARD G., PISTONE F., MAILLART P., DECAENS G.  
(Commun)  
A comparative study of on chip decorrelation schemes for low power, high resolution Infrared  
sensors  
iIEEE NEWCAS – TAISA’09 Conference, Toulouse, France June 28-July 1, 2009

106 TERRASSON G.*, BRIAND R.*, BASROUR S., DUPE V.*  
A Top-Down Approach for the Design of Low-Power Microsensor Nodes for Wireless Sensor  
Network  
Forum on specification & Design Languages (FDL’09), Sophia Antipolis, France, Sept. 22-24,  
2009  
*LIPSI, ESTIA, France

107 TERRASSON G.*, BRIAND R.*, BASROUR S., DUPE V.*, ARRIJURIA O.*  
Proceedings of The Eurosensors XXIII Conference, Procedia Chemistry, Volume: 1, Issue: 1,  
Lausanne, Switzerland, Sept. 6 - 9, 2009, 1195-1198  
*LIPSI, ESTIA, France

108 TOUNSI F., MEZGHANI B., RUFER L., MIR S., MASMOUDI M.  
Electromagnetic modelling of an integrated micromachined inductive microphone.  
Design and Technology of Integrated Systems (DTIS’09), Cairo, Egypt, April 6-7, 2009
109 TOUNSI F., RUFER L., MEZGHANI, BMASMOUDI M., MIR S.
Highly Flexible Membrane Systems for Micromachined Microphones – Modeling and Simulation
3rd IEEE International Conference on Signals, Circuits and Systems, (SCS’09), DJerba, Tunisia, November 6-8, 2009

110 WALTISPERGER G.*, CONDEMINE C.*, BASROUR S.
Power Path Optimization for Autonomous Microsystems
*CEA-LETI, Minatec, Grenoble, France

111 YAHYA E., ELISSATI O., ZAKARIA H., FESQUET L., RENAUDIN M.
Programmable/Stopable Oscillator Based on Self-Timed Rings
IEEE ASYNC 2009 Conference, UNC Chapel Hill - USA, May 17-20, 2009

112 YAHYA E., FESQUET L., RENAUDIN M.*
Asynchronous High-Speed Modeling and Optimization tool Set (AHMOSE)
Design, Automation and Test in Europe Conference (DATE’09) (University Booth) Nice, France, April 20-24, 2009
*TIEMPO SAS, Grenoble, France

113 YAHYA E., FESQUET L.
Asynchronous Design: A Promising Paradigm for Electronic Circuits and Systems
IEEE International Conference on Electronics and Systems (ICECS’09), Hammamet, Tunisia, December 13-16, 2009

114 ZHOU Z.J., RUFER L., WONG M.
Aero-Acoustic Microphone with Layer-Transferred Single-Crystal Silicon Piezoresistors
15th Int. Conf. on Solid-State Sensors, Actuators and Microsystems (Transducers’09), Denver, USA, June 21-25, 2009

2010

115 AMHAZ H., SICARD G.
X-axis Spatial Redundancy Supression : Contribution to the Integration of Smart Reading Techniques in a Standard CMOS Vision Sensor
17th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2010), Athens, Greece, December 12-15, 2010

116 AMHAZ H., SICARD G.
A high output voltage swing logarithmic image sensor designed with on chip FPN reduction
6th IEEE Conference on Ph.D. Research in Microelectronics & Electronics (PRIME 2010), Berlin, Germany, July 18 – 21, 2010

117 ARTHAUD Y., RUFER L., MIR S.
Study of a 3D MEMS-based tactile vibration sensor for the use in the middle ear surgery
International Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP’10), Sevilla, Spain, May 5-7, 2010

Frequency shift of MEMS electromechanical resonators induced by process variation
21st Micromechanics and Microsystems Europe Workshop (MME’10), Enschede, The Netherlands, September 26-29, 2010
*CEA-LETI, Grenoble, France; **STMicroelectronics, France

MEMS resonator temperature compensation
11th International Conference on Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE 2010), Bordeaux, France, April 26-28, 2010
*CEA-LETI, Grenoble, France; **STMicroelectronics, France
120 CIVET Y., CASSET F.*, CARPENTIER JF.**, DECOSSAS S., HACCART T., BASROUR S. MEMS resonator frequency compensation by “in-line” trimming” 11th International Symposium on RF MEMS and RF Microsystems (Memswave’10), Otranto, Italy, June 28-29-30, 2010 *CEA-LETI, Grenoble, France; **STMicroelectronics, France

121 CLERC S.*, ABOUZEID F.*, HEINRICH V.*, JAIN A.*, VEGGETTI A.*, CRIPPA D.*, ROCHE P.*, SICARD G. A 40nm cmos, 1.27nj, 330mv, 600khz, bose chaudhuri hocquenghem 252 bits frame decoder IEEE International Conference on Integrated Circuit Design and Technology (ICICDT’10), Grenoble, France, June 2-4, 2010 *STMicroelectronics, Grenoble, France

122 DEFOSSEUX M.*, ALLAIN M.*, BASROUR S. Comparison of different beam shapes for piezoelectric vibration energy harvesting The 10th International Workshop on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS’10), Leuven, Belgium, November 30 – December 3, 2010 * CEA-LETI, Minatec, Grenoble, France

123 ELISSATI O., YAHYA E., RIEUBON S., FESQUET L. A High-Speed High-Resolution Low-Phase Noise Oscillator Using Self-Timed Rings 18th IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC’10), Madrid, Spain, September 27-29, 2010

124 ELISSATI O., YAHYA E.*, RIEUBON S.**, FESQUET L. A novel High-Speed Multi-Phase Oscillator on Asynchronous Rings IEEE International Conference on Microelectronics (ICM’2010), December 19-22, 2010, Cairo, Egypt * Higher Institute of Technology, Banha University, Egypt; ** ST-Ericsson, Grenoble, France

125 ELISSATI O., YAHYA E.*, RIEUBON S.**, FESQUET L. Optimizing and Comparing CMOS Implementations of the C-element in 65nm technology: Self-Timed Ring Case International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS 2010), Grenoble, France, September 7-10, 2010 * Higher Institute of Technology, Banha University, Egypt; ** ST-Ericsson, Grenoble, France


128 GHANDOUR S.*, DESPESSE G.*, BASROUR S. Design of a New MEMS DC/DC Voltage Step-down Converter 8th IEEE International NEWCAS conference, Montréal, Canada, June 20 - 23, 2010 * CEA-LETI, Grenoble, France

129 HAMON J., FRISTOT V., ROLLAND R.* Implementation of a real time multi-resolution edge detection video filter 8th European Workshop on Microelectronics Education (EWME’10), Darmstadt, Germany, May 10-12, 2010 *CIME-Nanotech, Grenoble

131 POSSAMAI BASTOS R.*, SICARD G., KASTENSMIDT F.L.*, RENAUDIN M.**, REIS R.*
Evaluating Transient-Fault Effects on Traditional C-element s Implementations
16th IEEE International On-Line Testing Symposium (IOLTS’10), Corfu island, Greece,
July 5-7, 2010
"UFRGS, Instituto de Informática, PGMicro/PPGC, Porto Alegre, RS, Brazil; "Tiempo, 38330
Montbonnot Saint Martin, France

132 POSSAMAI BASTOS R.*, SICARD G., KASTENSMIDT F.*, RENAUDIN M.**, R. REIS*
Asynchronous circuits as alternative for mitigation of long-duration transient faults in deep-
submicron technologies
15th IEEE European Test Symposium (ETS’10), Prague, Czechoslovakia, May 24-28, 2010
"UFRGS, Instituto de Informática, PGMicro/PPGC, Porto Alegre, RS, Brazil; "Tiempo, 38330
Montbonnot Saint Martin, France

133 REHDER G.P., MIR S., RUFER L., SIMEU E., NGUYEN H.N.
Low frequency test for RF MEMS switches.
In 5th IEEE International Symposium on Electronic Design, Test and Applications (DELTA),
Ho Chi Minh City, January 2010

134 WALTISPERGER G.*, CONDEMIN C.*, BASROUR S.
Photovoltaic Energy Harvester for Micro-Scale Applications
8th IEEE International NEWCAS conference. June 20 - 23, 2010, Montréal, Canada
* CEA-LETI, Grenoble, France

135 YAHYA E., HAMON J., FESQUET L.
AHMOSE: Asynchronous High-Speed Modelling and Optimization Tool-Set
Tutorial given at the 16th IEEE International Symposium on Asynchronous Circuits and Systems
(ASYNC), May 3-6, 2010

136 YAHYA E., HAMON J., FESQUET L.
AHMOSE: Asynchronous High-Speed Modelling and Optimization Tool-Set
Tutorial given at the 16th IEEE International Symposium on Asynchronous Circuits and Systems
(ASYNC), May 3-6, 2010

137 YANG W., BONVILAIN A., ALONSO T.*, MOREAU-GAUDRY A.**, BASROUR S.
Modelling and Characterization of an Instrumented Medical Needle in Sight of New Microsensor
Design for its Insertion Guidance
32nd Annual International Conference of the IEEE Engineering in Medicine and Biology
(EMBC’10), Buenos Aires, Argentina, August 31 - September 4, 2010
* Laboratoire 3SR (CNRS-UJF-INPG), Grenoble, France; ** Laboratoire TIMC-IMAG (CNRS-
UJF), La Tronche, France

138 ZIMOUCHE H., SICARD G.
Temperature Compensation Method for Logarithmic CMOS Vision Sensor Using CMOS Voltage
Reference Bandgap Technique
17th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2010),
Athens, Greece, December 12-15, 2010

139 ZIMOUCHE H., SICARD G.
Integrated Temperature Compensation Scheme for a Standard Linear CMOS Vision Sensor
6th IEEE Conference on Ph.D. Research in Microelectronics & Electronics (PRIME 2010),
Berlin, Germany, July 18 – 21, 2010

140 ZIMOUCHE H., SICARD G.
Standard Linear CMOS Image Sensor Insensitive to Temperature Variations
The 8th IEEE International NEWCAS 2010 Conference, Montreal, Canada, June 20 - 23, 2010
THEME 3 : Design and verification of System-on-Chip architectures

2009

141 ALSAYEG K., MORIN-ALLORY K., FESQUET L.
   RAT-based formal verification of QDI asynchronous controllers
   Forum on specifications and Design Languages (FDL’09), Sophia Antipolis, France,
   September 22 - 24, 2009

142 BOUCHHIMA A., GERIN P., PÉTROT F.
   Automatic instrumentation of embedded software for high level hardware/software co-simulation
   Asia and South Pacific Design Automation Conference (ASP-DAC’09), pages 546-551,
   Yokohama, Japan, January 19-22, 2009

143 CHAGOYA-GARZON A., GUERIN X., ROUSSEAU F., PETROT F., ROSSETTI D.*, LONARDO A.*,
   VICINI P.*, PAOLUCCI P.S.**
   Synthesis of communication mechanisms for multi-tile systems based on heterogeneous Multi-
   processor System-on-Chips
   20th IEEE/IFIP International Symposium on Rapid System Prototyping(RSP’09), Paris, France,
   June 23-26 2009
   *INFN Roma ; **Atmel Roma, INFN

144 EL MRABTI A., F. PÉTROT, A. BOUCHHIMA
   Extending IP-XACT to support an MDE based approach for SoC design
   Design Automation and Test in Europe (DATE’09), Nice, France, April 20-24, 2009

145 EL MRABTI A., SHEIBANYRAD H., ROUSSEAU F., PETROT F., LEMAIRE R.*, MARTIN J.*
   Abstract Description of System Application and Hardware Architecture for Hardware/Software
   Code Generation
   12th Euromicro Conference on Digital System Design (DSD’09), Patras, August 27-29, 2009
   *CEA-LETI, Grenoble, France

146 FERRO L., PIERRE L.
   ISIS: Runtime Verification of TLM Platforms
   Proc. Forum on specification & Design Languages (FDL’09), Sophia-Antipolis (France),
   September 2009 (Best Paper Award)

147 GERIN P., HAMAYUN M.-M, PÉTROT F.
   Native MPSoC Co-Simulation Environment for Software Performance Estimation
   In Proceedings of the 7th IEEE/ACM International Conference on Hardware/Software-Co-Design
   and System Synthesis, pages 403–412, Grenoble, France, October 2009

148 GLIGOR M., FOURNEL N., PÉTROT F.
   Adaptive Dynamic Voltage and Frequency Scaling Algorithm for Symmetric Multiprocessor Architec
   ture
   Euromicro Conference on Digital System Design Architectures, Methods and Tools (DSD’09),
   Patras, Greece, August 27-29, 2009

   COPPOLA M.**
   Practical Design Space Exploration of an H264 Decoder for Handheld Devices Using a Virtual
   Platform
   Power and Timing Modeling, Optimization and Simulation (PATMOS’09), Delft, Netherlands,
   September 9-11, 2009
   * Thales Communications, France ; ** STMicroelectronics, Crolles, France

150 GLIGOR M., FOURNEL N., PÉTROT F.
   Using Binary Translation in Event Driven Simulation for Fast and Flexible MPSoc Simulation
   International Conference on Hardware-Software Codesign and System Synthesis
   (CODES+ISSS’09), Grenoble, France, October 11-16,2009

151 GUÉRIN X., PÉTROT F.
   A System Framework for the Design of Embedded Software Targeting Heterogeneous Multi-Core
   SoCs
   20th IEEE International Conference on Application-specific Systems, Architectures and
   Processors, Boston (Ma), USA, July 7-9, 2009
<table>
<thead>
<tr>
<th>Publication ID</th>
<th>Author(s)</th>
<th>Title</th>
<th>Conference/Location</th>
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</thead>
<tbody>
<tr>
<td>152</td>
<td>GUIRONNET-DE-MASSAS P., PETROT F.</td>
<td>Migration de données dans les MPSoC : une solution matérielle</td>
<td>13ème Symposium d'architecture de machines, 12 p., Toulouse, France, Septembre 2009</td>
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<td>*CEA-LETI; **CIME-Nanotech; ***LIG laboratory</td>
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<tr>
<td>155</td>
<td>MEUNIER Q., PETROT F.</td>
<td>Lightweight Transactional Memory Systems for Large Scale Shared Memory MPSoCs</td>
<td>NEWCAS – TAISA’09 Conference, Toulouse, France June 28-July 1, 2009</td>
</tr>
<tr>
<td>156</td>
<td>MEUNIER Q., PETROT F.</td>
<td>LightTM : Une Mémoire Transactionnelle conçue pour les MPSoCs</td>
<td>Symposium en Architecture de machines (SympA’13), Toulouse, France, September 9-11, 2009</td>
</tr>
<tr>
<td>157</td>
<td>ODDOS Y., BOULÉ M.<em>, MORIN-ALLORY K., BORRIONE D., ZILIC Z.</em></td>
<td>MYGEN: Automata-based On-line Test Generator for Assertion-based Verification</td>
<td>19th Great Lakes Symposium on VLSI (GLSVLSI’09), Boston (MA), May 10-12, 2009</td>
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<td>*McGill University, Montréal, Canada</td>
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<tr>
<td>158</td>
<td>ODDOS Y., MORIN-ALLORY K., BORRIONE D.</td>
<td>Synthoros: Highly Efficient Automatic Synthesis from PSL to HDL</td>
<td>Proc. IFIP/IEEE International Conference On Very Large Scale Integration (VLSI-SoC’09), Florianopolis (Brazil), October 2009</td>
</tr>
<tr>
<td>159</td>
<td>OUCHET F., BORRIONE D., MORIN-ALLORY K., PIERRE L.</td>
<td>High-level symbolic simulation for automatic model extraction</td>
<td>IEEE Symposium on Design and Diagnostics of Electronic Systems (DDECS’09), Liberec (Czech Republic), April 15-17, 2009</td>
</tr>
<tr>
<td>160</td>
<td>PIERRE L., CLAVEL R., LEVEUGLE R. (Commun)</td>
<td>ACL2 for the Verification of Fault-Tolerance Properties: First Results</td>
<td>International Workshop on The ACL2 Theorem Prover and Its Applications (ACL2’09), Boston (MA), USA, May 11-12, 2009</td>
</tr>
<tr>
<td>161</td>
<td>POPOVICI K., JERRAYA A.*</td>
<td>Flexible and Abstract Communication and Interconnect Modeling for MPSoC</td>
<td>Asia and South Pacific Design Automation Conference (ASP-DAC’09), Yokohama, Japan, January 19-22, 2009</td>
</tr>
<tr>
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<td>*CEA – LETI, Grenoble, France</td>
</tr>
<tr>
<td>163</td>
<td>SHEN H., PÉTROT F.</td>
<td>Novel Task Migration Framework on Configurable Heterogeneous MPSoC Platforms</td>
<td>14th Asia and South Pacific Design Automation Conference (ASP-DAC’09), Yokohama, Japan, January 19-22, 2009</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>*CEA-LETI, MINATEC; **Magillem Design Services</td>
</tr>
</tbody>
</table>
165 FERRO L., PIERRE L.
Formal Semantics for PSL Modeling Layer and Application to the Verification of Transactional Models
Proc. Of Design, Automation and Test in Europe (DATE’10), Dresden (Germany), March 9-11, 2010

166 HELMY A., PIERRE L., JANTSCH A.
Theorem Proving Techniques for the Formal Verification of NoC Communications with Non-Minimal Adaptive Routing
Proc. IEEE Symposium on Design and Diagnostics of Electronic Systems, Vienna (Austria), April 2010

167 LEFFTZ V.¹, BERTRAND J.², CASSE H.³, CLIENTI C.⁴, COUSSY P.⁵, MAILLET-CONTOZ L.⁶, MERCIER P.⁷, MOREAU P.⁸, PIERRE L., VAUMORIN E.⁹
A Design Flow for Critical Embedded Systems
¹Astrium (Toulouse, FR), ²CNES (Toulouse, FR), ³IRIT (Toulouse, FR), ⁴Thales R&T (Palaiseau, FR), ⁵LESTER, Lorient, France; ⁶STMicroelectronics (Grenoble, FR), ⁷PSI (Grenoble, FR), ⁸Airbus (Toulouse, FR), ⁹Magillem (Paris, FR)

168 OUCHET F., MORIN-ALLORY K., FESQUET L.
Delay insensitivity does not mean slope Insensitivity!
16th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC’10), May 3-6, 2010

169 PIERRE L., FERRO L.
Enhancing the Assertion-Based Verification of TLM Designs with Reentrancy

170 PORCHER A., MORIN-ALLORY K., FESQUET L.
Synthesis of Asynchronous Monitors for Critical System
IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS’10), Vienna, Austria, April 14-16, 2010

171 RAHMOUNI K., PÉTROT F.
Improving the tests coverage of a medium voltage protection device using system simulation approaches

172 SHEN H., PÉTROT F.
A Flexible Hybrid Simulation Platform Targeting Multiple Configurable Processors SoC.

THEME 4 : Reliable Mixed-signal / RF circuits and systems

2009

173 ASQUINI A., BOUNCEUR A., MIR S., BADETS F., CARBONERO J.L., BOUZAIDA L.
DFT technique for RF PLLs using built-in monitors
Design and Technology of Integrated Systems (DTIS’09), Cairo, Egypt, April 6-7, 2009

174 CENNI F., MIR S., RUFER L. (Commun)
Behavioral modeling and simulation of a chemical sensor with its microelectronics front-end Interface
3rd IEEE International Workshop on Advances in Sensors and Interfaces (IWASI’09), Trani, Italy, June 25-26, 2009

175 CENNI F., SIMEU E., MIR S.
Macro-modeling of analog blocks for SystemC-AMS simulation: A chemical sensor case-study
17th IFIP International Conference on Very Large Scale Integration (VLSI-SoC’09), Florianopolis, Brazil, October 12-14, 2009
176 DUBOIS M., STRATIGOPoulos H.-G., MIR S.
Hierarchical parametric test metrics estimation: A ΣΔ converter BIST case-study
27th IEEE International Conference on Computer Design (ICCD’09), Lake Tahoe, California, USA, October 2009, pp. 78-83.

177 KHEREDDINE R., SIMEU E., MIR S.
Parameter identification of RF transceiver blocks using regressive models.
IFAC Workshop on Programmable Devices and Embedded Systems (PDeS’09), Roznov pod Radhostem, Czech Republic, February 10-12, 2009

178 LIZARRAGA L., MIR S., SICARD G.
Experimental validation of a BIST technique for CMOS active pixel sensors
27th IEEE VLSI Test Symposium (VTS’09), Santa Cruz, USA, May 3-7, 2009

179 STRATIGOPoulos H., MIR S., ACAR E., OZEV S.
Defect filter for alternate RF test
European Test Symposium (ETS’09), Sevilla, Spain, May 25-29, 2009

180 STRATIGOPoulos H., MIR S., MAKRIS Y.
Enrichment of limited training sets in machine-learning-based analog/RF Test.
Design, Automation and Test in Europe Conference (DATE’09), Nice, France, April 20-24, 2009

2010

181 ABDALLAH L., STRATIGOPoulos H., KELMA C.*, MIR S.
Sensors for built-in alternate RF test
IEEE European Test Symposium (ETS’10), Prague, Czech Republic, pp. 49-54, May 24-28, 2010
*NXP Semiconductors, Caen, France

182 ABDALLAH L., STRATIGOPoulos H., KELMA C.*, MIR S.
Capteurs embarqués pour le test alternatif des circuits RF
Journées GDR SoC-SIP, Paris, France, June 9-11, 2010
*NXP Semiconductors, Caen, France

183 ALHAKIM R., RAOOF K.*, SIMEU E.
A Novel Fine Synchronization Method for Dirty Template UWB Timing Acquisition
* GiPSA-LAB, CNRS – Grenoble University

184 AKKOUCHE N., MIR S., STRATIGOPoulos H., SIMEU E.
Ordering of analog specification tests based on parametric defect level estimation
26th IEEE VLSI Test Symposium, Santa Cruz, USA, April 2010

185 DUBOIS M., STRATIGOPoulos H., S. MIR.
Evaluation des métriques de test pour des circuits analogiques/mixtes complexes
Journées GDR SoC-SIP, Paris, France, June 9-11, 2010

186 HUANG K., STRATIGOPoulos H., S. MIR.
Fault diagnosis of analog circuits based on machine learning
Design, Automation and Test in Europe Conference, Dresden, Germany, March 8-12, 2010

187 HUANG K., STRATIGOPoulos H., S. MIR.
Diagnostic de fautes de circuits analogiques basé sur l’apprentissage automatique
Journées GDR SoC-SIP, Paris, France, June 9-11, 2010

188 HUANG K., STRATIGOPoulos H., S. MIR.
Bayesian fault diagnosis of RF circuits using nonparametric density estimation
IEEE Asian Test Symposium (ATS’10), Shanghai, China, December 1-4, 2010
189 KHEREDDINE R., ABDALLAH L., SIMEU E., MIR S., CENNI F.
Adaptive Logical Control of RF LNA performances for efficient energy consumption
18th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Madrid,

190 MALIUK D.*, STRATIGOPOULOS H., HUANG H., MAKRIS Y.
Analog neural network design for RF built-in self-test
IEEE International Test Conference (ITC), Austin, TX, USA, October 31-November 05, 2010
* Yale University, USA

191 STRATIGOPOULOS H., S. MIR.
Analog test metrics estimates with PPM accuracy
IEEE International Conference on Computer-Aided Design (ICCAD), San Jose, USA,
November 7-11, 2010

192 TONGBONG J., ABDALLAH L., MIR S., STRATIGOPOULOS H.
Evaluation of built-in sensors for RF LNA response measurement
16th IEEE International Mixed-signals, Sensors and Systems Test Workshop (IMS3TW), La Grande
Motte, France, June 7-9, 2010

INVITED CONFERENCE PRESENTATIONS (INV)

THEME 1 : Architectures for robust and complex integrated systems

2009

193 ALEXANDRESCU D., WEN S.J., NICOLAIDIS M.
Dealing with Soft Errors in Complex Electronic Systems
Invited talk in 18th Annual Single Event Effects Symposium, April 20-22, 2009, San Diego CA

194 ALEXANDRESCU D., WEN S.J., NICOLAIDIS M.
Complex Electronic Systems Soft Error Rate (SER) Management
Invited presentation in 14th IEEE European Test Symposium, May 25-29, 2009, Sevilla, Spain

Ensuring High Testability without Degrading Security
Embedded Tutorial, European Test Symposium (ETS'09), Seville (Spain), May 26-28, 2009
* LIRMM, France

196 R. VELAZCO
Single Event Effects on Digital Integrated Circuits: Origins and Mitigation Techniques
INTERCON 2009, Arequipa, Peru, August 10-14, 2009

197 R. VELAZCO
Advances in the study of the effects of radiation in integrated circuits
Section IEEE du Pérou et le Chapitre Technique Circuits et Systèmes, Colegio de Ingenieros del
Peru, August 17, 2009

2010

198 LEVEUGLE R.
Integrated systems security: hardware-based threats and solutions
Embedded tutorial, IEEE Latin American Symposium on Circuits and Systems (LASCAS’10),
Iguacu Falls, Brazil, February 24-26, 2010

199 LEVEUGLE R.
Early robustness evaluation of digital integrated systems
13th Forum for Design Languages (FDL), Southampton, UK, September 14-16, 2010

200 VELAZCO R.
Single Events on Digital Integrated Circuits
Invited Conference, BETCON: Bolivian Engineering and Technology Congress, Univ. Mayor de San
Andrés, La Paz, Bolivia, May 10-14, 2010
201 VELAZCO R.
Effects of natural radiation on integrated circuits: origins, mitigation techniques and experiments in the natural environment
Invited conference at CONEIMERA (Congreso Nacional de Estudiantes de Ingenieria Mecanica, Electronica Electrica, y Ramas Afines), Trujillo (Peru) September 20-25, 2010

202 VELAZCO R.
Error Rate Predictions for Programmable Circuits: Methodology, Tools and Studied Cases.
Invited conference at 9th RASEDA : International Workshop on Radiation Effects on Semiconductor Devices for Space Applications), Takasaki, Japan, October 27-29, 2010

THEME 2 : Design of integrated devices, circuits and systems

2009

203 FESQUET L., ZAKARIA H.
Controlling Energy and Process Variability in System-on-Chips: needs for control theory
3rd IEEE Multi-conference on Systems and Control (MSC’09), Saint Petersburg, Russia, July 8-10, 2009

THEME 4 : Reliable Mixed-signal / RF circuits and systems

2009

204 STRATIGOPOULOS H.
Checkers for on-line monitoring of analog circuits
Invited talk, CMOS Emerging Technologies Workshop, Vancouver, Canada, September 23-25, 2009

2010

205 MIR S., STRATIGOPOULOS H., DUBOIS M., BOUNCEUR A.
Evaluation of parametric test metrics for mixed-signal/RF DFT solutions using statistical techniques
Invited Talk, Catrene European Nanoelectronics Design Technology Conference (DTC’10), Grenoble, June 23-24, 2010

206 MIR S., STRATIGOPOULOS H., BOUNCEUR A.
Density estimation for analog/RF test problem solving
Invited Talk, 28th IEEE VLSI Test Symposium, Santa Cruz, USA, pp. 41, April 2010

207 SIMEU E.
Embedded Test and Control of Analogue/RF Circuits Using Intelligent Resources
11th Latin America Test Workshop, Invited embedded tutorial, March 28-31, 2010, Punta del Este, Uruguay

INVITED CONFERENCE TALKS WITHOUT PAPER (COM)

THEME 3 : Design and verification of System-on-Chip architectures

2009

208 GUIRONNET DE MASSAS P., PETROT F.
Optimized and Transparent Data Accesses in Homogeneous MPSoC
209 BORRIONE D., MORIN-ALLORY K., ODDOS Y.
Automatic synthesis of simulation and test environments from assertions
3ème école d’hiver francophone sur les Technologies de Conception des Systèmes embarqués
Hétérogènes, Chexbres, Suisse, 12-14 janvier 2009

210 PETROT F., GERIN P.
Estimation de performance du logiciel embarqué utilisant une technique d’annotation du code natif
3ème école d’hiver francophone sur les systèmes hétérogènes, Chexbres, Suisse, janvier 2009

211 PÉTROT F., FOURNEL N., GLIGOR M.
A Power Aware Transactional Level Multi-processor SoC Simulation Environment.

212 PETROT F., MEUNIER Q.
Design and Use of Transactional Memory in MPSoCs.
9th International Seminar on Application Specific Multiprocessor SoC, Savannah, Georgia, USA,
August 2009

2010

213 BORRIONE D.
Fast and correct by construction control prototyping from PSL: an extension of the assertion-based
verification paradigm
4ème école d’hiver francophone sur les systèmes hétérogènes (FETCH’10), Chamonix, France,
January 11-13, 2010

214 PETROT F., GUIRONNET DE MASSAS P.
De l’accès transparent et optimisé aux données dans les systèmes multiprocesseurs intégrés
4ème école d’hiver francophone sur les systèmes hétérogènes (FETCH’10), Chamonix, France,
January 11-13, 2010

215 PÉTROT F., FOURNEL N., GLIGOR M.
Annotation within dynamic binary translation for fast and accurate system simulation
10th International Forum on Embedded MPSoC and Multicore, Gifu city, Gifu, Japan, June 28 - July 2
2010

THEME 4: Reliable Mixed-signal / RF circuits and systems

2010

216 MIR S.
The role of test in the evolution and maturation of emerging technologies
Panel at 16th IEEE International Mixed-signals, Sensors and Systems Test Workshop (IMS3TW),
La Grande Motte, France, June 7-9, 2010

217 STRATIGOPOULOS H.
Adaptive analog test: feasibility and opportunities Ahead
Panel organization at 26th IEEE VLSI Test Symposium (VTS), Santa Cruz, USA, April 2010

218 STRATIGOPOULOS H.
On-Line monitoring for analog and sensor-based systems
Special session organisation, 16th IEEE International On-Line Testing Symposium (IOLTS), Corfu,
Greece, June 2010
POSTER PRESENTATION IN CONFERENCE (AFF)

THEME 1: Architectures for robust and complex integrated systems

2009

219 FERRON J. B., ANGHEL L., LEVEUGLE R.
Predictive analysis of configuration bit criticality in SRAM-based FPGAs – Methodology, tools, and Results
3ème Colloque du GdR SoC-SiP, Paris, France, June 10-12, 2009

2010

220 BEN JRAD M., LEVEUGLE R.
Injection de fautes par reconfiguration partielle - Application à un FPGA Virtex II Pro
13èmes Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM), Montpellier, France, 7-9 Juin 2010

221 BERGAOUI S., LEVEUGLE R.
Nouvelle méthode de vérification de flot de contrôle avec signatures disjointes
13èmes Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM), Montpellier, France, 7-9 Juin 2010

222 DETTENBORN R.
RTL Analysis Based on Signal Reliability
IVième Colloque national du GDR SoC-SiP, Paris-Cergy, France, June 09-10-11, 2010

THEME 2: Design of integrated devices, circuits and systems

2009

223 ALSAYEG K., FESQUET L., SICARD G., RIOS D., RENAUDIN M.
Direct mapping of sequential QDI controllers
PhD Forum DATE 2009, Nice, France, April 20-24, 2009

224 BEYROUTHY T., FESQUET L.
A secure asynchronous FPGA for an embedded system
PhD Forum DATE, Nice, April 20-24, 2009

225 ZIMOUCHE H., SICARD G.
Capteur de vision CMOS à réponse insensible à la température
Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’09), Bordeaux, May 14-16, 2009

2010

226 YANG W., BONVILAIN A., BASROUR S.
Modélisations et Expérimentations d’une Aiguille Médicale Instrumentée pour le Guidage de son Insertion
Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’10), Montpellier, Juin 7-9, 2010

227 CIVET Y., CASSET F., CARPENTIER JF., BASROUR S.
Compensation de la fréquence des résonateurs MEMS par ajustement in-line
Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’10), Montpellier, Juin 7-9, 2010
THEME 3 : Design and verification of System-on-Chip architectures

2009

228 CHAGOYA-GARZON A., GUERIN X., ROUSSEAU F
Outils de Génération du Logiciel pour les Systèmes sur Puce Multi-Processeur Hétérogènes
Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’09), Bordeaux, May 14-16, 2009

THEME 4 : Reliable Mixed-signal / RF circuits and systems

2009

229 ABDALLAH L., TONGBONG J., STRATIGOPOULOS H.-G., MIR S.
Alternate LNA testing using an envelope detector
Journées GDR SoC-SiP, Paris, France, June 10-12, 2009

BOOK CHAPTERS (OS)

THEME 1 : Architectures for robust and complex integrated systems

2010

230 ENTRENA L.*, LÓPEZ ONGIL C.*, GARCÍA VALDERAS M.*, PORTELA GARCÍA M.*, NICOLAIDIS M.
Hardware Fault Injection
* Electronic Technology Department, Carlos III University of Madrid, Spain

231 NICOLAIDIS M., KOLONIS E.
Computational Opportunities and CAD for Nanotechnologies

232 NICOLAIDIS M.
Computational Space, Time and Quantum Mechanics

233 NICOLAIDIS M.
Circuit-level Soft-Error Mitigation

234 VELAZCO R., FOUCARD G., PERONNARD P.
Integrated circuit qualification for Space and Ground-level Applications: Accelerated test and Error-Rate Prediction
THEME 2 : Design of integrated devices, circuits and systems

2009

235 GOULIER J.*, ANDRE E.*, RENAUDIN M.
A new analytical approach of the impact of jitter of the continuous time delta sigma converters
Chapter in books series IFIP International Federation for Information Processing, VLSI-SoC: Advanced Topics on Systems on a Chip; eds. R. Reis, V. Mooney, P. Hasler; (Boston: Springer), pp 1-16, Volume 291/2009
* St Microelectronics, Crolles, France

2010

236 ELISSATI O., YAHYA E., RIEUBON S., FESQUET L.
Optimizing and Comparing CMOS Implementations of the C-element in 65nm technology: Self-Timed Ring Case

237 SICARD G., LABONNE E., ROLLAND R.
A Standard 3.5T CMOS Imager, Including a Light Adaptive System for IntegrationTime Optimization

238 ZAKARIA H., YAHYA E., FESQUET L.
Self Adaption in SoCs

THEME 3 : Design and verification of System-on-Chip architectures

2009

239 BORRIONE D., HELMY A., PIERRE L., SCHMALTZ J.*
Formal Verification of Communications in Networks-on-Chips
Chapter in "Networks-on-Chips: Theory and Practice", F.Gebali, H.Emiligi and M. Watheq El-Kharashi editors, CRC Press (Taylor and Francis group), March 2009
* Institute for Computing and Information Sciences, Radboud University, Nijmegen, The Netherlands

240 POPOVICI K., JERRAYA A.*
Hardware Abstraction Layer – Introduction and Overview
Chapter 4 in "Hardware dependent Software, Concept, Tools and Applications", edited by Wolfgang Ecker, Wolfgang Miller, Rainer Domer, February 2009
* CEA-LETI, Grenoble, France

241 PÉTROT F., GERIN P.
Simulation at Cycle Accurate and Transaction Accurate Levels
242 POPOVICI K., JERRAYA A.*
   Hardware Abstraction Layer – Introduction and Overview
   Chapter 4 in “Hardware dependent Software, Concept, Tools and Applications”, edited by
   Wolfgang Ecker, Wolfgang Miller, Rainer Domer, February 2009
   * CEA-LETI, Grenoble, France

243 DUBOIS M., ROUSSEAU F., ABOULHAMID E. M.*
   An Introduction to Cosimulation and Compilation Methods
   Chapter in System Level Design with .NET Technology, CRC Press, September 2009,
   * University of Montreal, Canada

2010

244 FERRO L., PIERRE L.
   ISIS: Runtime Verification of TLM Platforms
   Chapter in Advances in Design Methods from Modeling Languages for Embedded Systems and
   Soc’s (Selected Contributions from FDL’09), Lecture Notes in Electrical Engineering, Vol. 63,
   Springer, May 2010

245 GUÉRIN X., PÉTROT F.
   Operating System Support for Applications targeting Heterogeneous Multi-Core System-on-Chips
   In Multi-Core Embedded Systems, Series: Embedded Multi-Core Systems George Kornaros,
   editor. Chapter 9, 24 p., Avril 2010, CRC Press

246 PIERRE L., FERRO L.
   Dynamic Verification of SystemC Transactional Models
   Chapter in "Model-Based Testing for Embedded Systems" (Series "Computational Analysis,

247 SHEIBANYRAD H., PÉTROT F.
   Asynchronous 3D-NoCs
   In 3D-Architectures and Networks-on-Chip, Hamed Sheibanyrad, Frédéric Pétrot et Axel Jantsch
   (éditeurs), Springer, December 2010

EDITED BOOKS (DO)

THEME 3 : Design and verification of System-on-Chip architectures

2009

248 ABOULHAMID E.M.*, ROUSSEAU F. (Eds.)
   System Level Design with .NET Technology
   * University of Montreal, Canada

2010

249 BORRIONE D. (editor)
   Advances in Design Methods from Modeling Languages for Embedded Systems and SoC’s
   Revised selected contributions from FDL’09, Series “Lecture Notes in Electrical Engineering”,

250 POPOVICI K.*, ROUSSEAU F., JERRAYA A.**, WOLF W., Ed.
   Embedded Software Design and Programming of Multiprocessor System-on-Chip: Simulink and
   *MathWorks (Boston, EU), **CEA/LETI; ***GeorgiaTech, Embedded System Lab, (Atlanta, EU)
THESES (TH)

THEME 1: Architectures for robust and complex integrated systems

2009

252 Vincent MAINGOT
Secure Design against fault attacks and side-channel attacks
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – June 09, 2009

253 Gaetan CANIVET
Analysis of faulted-based attack effects and secure design on a reconfigurable platform
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – September 23, 2009

254 Alexandre BOCQUILLON
Evaluation de la sensibilité des FGPA SRAM-based face aux erreurs induites par les radiations natur
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – October 02, 2009

255 Paul PERONNARD
Methods and tools for the evaluation of the sensitivity to natural radiations of advanced integrated cir
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – October 02, 2009

256 Nizar BEN HASSINE
Bulk Acoustic Wave devices reliability for Radio Frequency applications
Thèse de Doctorat UJF, spécialité Micro et Nano électronique – October 29, 2009

2010

257 Gilles FOUCARD
Radiation error rate for applications implemented in SRAM-based FPGA: prediction versus
measures
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – June 11, 2010

258 Claudia RUSU
Multi-Level Fault-Tolerance in Networks-on-Chip
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – September 10, 2010

THEME 2: Design of integrated devices, circuits and systems

2009

259 Cedric KOCH-OFER (Commun)
Modélisation, Validation et Présynthèse de Circuits Asynchrones en SystemC
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – March 26, 2009

260 Saeed MIAN QAI SAR
Signal Driven Sampling and Processing: A Promising Approach for Adaptive Rate Computationally
Efficient Solutions
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – May 05, 2009
261 Jérémy HAMON
Asynchronous oscillators and architectures for UWB impulse radio signal processing
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – October 15, 2009

262 Taha BEYROUTHY
Asynchronous programmable logic for secured embedded systems
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – November 2, 2009

263 Louis CARLIOZ
Piezoelectric generator thermo-magnetically triggered
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – November 27, 2009

264 Yann ODDOS
Semi-Formal Verification and Automatic Synthesis from PSL to VHDL
Thèse de Doctorat UJF, spécialité Micro et Nano électronique – November 27, 2009

265 Eslam YAHYA
Performance Modeling, Analysis and Optimization of Multi-Protocol Asynchronous Circuits
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – December 09, 2009

266 Z. RASLAN
Design, Fabrication and characterization of microactuators based on carbon
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – December 12, 2009

2010

267 R. POSSAMAI BASTOS
Systèmes Robustes aux Fautes Transitoires Exploitant la Logique Asynchrone Quasi-Insensible aux
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – July 09, 2010

268 Hela BOUSSETTA
Modelling and global simulation of self powered microsystems
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – February 20, 2010

269 Khaled ALSAYEG
Synthesis of low power QDI sequential controllers proved correct
Thèse de Doctorat INPG, spécialité Micro et Nano électronique September 01, 2010

THEME 3 : Design and verification of System-on-Chip architectures

2009

270 Cedric KOCH-OFER (Commun)
Modélisation, Validation et Présynthèse de Circuits Asynchrones en SystemC
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – March 26, 2009

271 Chawki SAHININE
Reconfigurable, high throughput and low power VLSI architecture for advanced OFDM
digital processing

272 Hao SHEN
Contribution to a modeling approach and an exploration flow targeted to heterogeneous MPSoC
architectures based on configurable processors
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – March 11, 2009

273 Abdellah KOUADRI MOSTefaoui
Flexible Architectures for Networks-On-Chip Validation and Exploration
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – August 24, 2009
274 Pierre GUIRONNET DE MASSAS
Study of methods and mechanisms for software-seamless data accesses in a multiprocessor system-on-chip
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – November 12, 2009

275 Yann ODDOS
Semi-Formal Verification and Automatic Synthesis from PSL to VHDL
Thèse de Doctorat UJF, spécialité Micro et Nano électronique – November 27, 2009

276 Patrice GERIN
Simulation models for software validation and architecture exploration of Multi-Processors System On Chip
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – November 30, 2009

2010

277 Amr HELMY
Implementation of automatic demonstration techniques for formal verification of NoCs
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – April 30, 2010

278 Xavier GUERIN
An efficient embedded software development approach for multiprocessor system-on-chips
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – May 12, 2010

279 Marius GLIGOR
Fast Simulation Strategies and Adaptive DVFS Algorithm for Low Power MPSoCs
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – September 09, 2010

280 Quentin MEUNIER
Study of two solutions for parallel programming support in integrated multiprocessors: work-stealing and transactional memories
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – October 29, 2010

THEME 4: Reliable Mixed-signal / RF circuits and systems

2009

281 Hoang-Nam NGUYEN
Alternative test technique for RF MEMS switch
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – July 06, 2009

282 Rabeb KHERIJI
Optimisation du test de production pour des amplificateurs faible bruit RF
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – September 09, 2009

283 Jeanne TONGBONG
Conception et évaluation d’une technique de DfT pour un amplificateur faible bruit RF
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – December 07, 2009

2010

284 Anna ASQUINI
A BIST technique for RF frequency synthesizers
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – January 22, 2010

285 Farès TOUNSI
MEMS Electrodynamic Microphone in CMOS technology: design, modeling and realization
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – March 22, 2010
SOFTWARE AND PATENTS

THEME 1 : Architectures for robust and complex integrated systems

2009

286 NICOLAIDIS M., BOUTOBZA S.
A multi-port memory device
US patent application filed April 2009

THEME 2 : Design of integrated devices, circuits and systems

2009

287 ALLAIN M.*, BASROUR S., BERTHIER J.*, POUTEAU P.*
Vanne microfluidique à usinage unique
Brevet N° FR2945097 Année de dépôt et d’obtention: 2009, (UJF, INP, CNRS, ou industriel)
CEA.
* CEA, Grenoble, France

THEME 3 : Design and verification of System-on-Chip architectures

2009

288 BORRIONE D., FERRO L., FESQUET L., MORIN-ALLORY K., ODDOS Y., PIERRE L.
Logiciel "HORUS"
enregistré au Répertoire IDDN le 27/05/2009, N° : IDDN.FR.001.220016.000.S.P.2009.000.31500

289 PETROT F., SHEIBANYRAD H.
Architecture de communication à base de sérialiseur asynchrone entre circuits déposés sur des
substrats de silicium empilés.
Brevet français n°09/53637, juin 2009

THEME 4 : Reliable Mixed-signal / RF circuits and systems

2010

290 DUBOIS M., MIR S., STRATIGOPOULOS H.
Convertisseur analogique-numérique sigma-delta muni d’un circuit de test
Demande de brevet FR No. 10/02741 déposée le 30 juin 2010
16. Press articles and special events in 2009/2010

Summary

► Régis Leveugle nommé Chevalier dans l'Ordre des Palmes Académiques
  Distinction remise lors d'une cérémonie par Paul Jacquet, Administrateur Général de Grenoble INP
  March 3, 2009

► Traquer et limiter les défaillances
  « à savoir, Grenoble INP », April 27 – May 2009

► Le Prix de Thèse de Grenoble INP
  « En ligne de Grenoble INP »
  Semaine du lundi 18 mai 2009 N°167

► TIMA - SLS sur un stand à ESWEek
  WTC, October 14-15, 2009

► Le Prix de Thèse de Doctorat 2010 par la Société Française de Génie Biologique et Médical
  April 13, 2011
Régis Leveugle nommé Chevalier dans l’Ordre des Palmes Académiques.....
Distinction remise lors d’une cérémonie par Paul Jacquet, Administrateur Général de Grenoble INP le 3 mars 2009
« à savoir, Grenoble INP », N° 83 Bi-mensuel du 27 avril au 7 mai 2009
Rubrique : À explorer - Traquer et limiter les défaillances

Traquer et limiter les défaillances

Régis Laureau,
professeur à
Grenoble INP
et chercheur au laboratoire TIMA, vient de nous faire part d’une découverte surprenante. En effet, lors de ses recherches sur les circuits intégrés, il a constaté que certains composants électroniques, lorsqu’ils sont mis sous tension, peuvent provoquer des défaillances dans les circuits. Ces défaillances peuvent être le résultat de parasites électromagnétiques ou de défauts dans les connexions des composants.

La miniaturisation des composants électroniques fait apparaître des failles de sécurité qui peuvent ensuite faire l’objet d’attaques par des personnes malveillantes dans le but d’entrer dans des systèmes informatiques.

Comment vous y prémunissez-vous ?

R.L. : Nous avons des collaborateurs en longue date sur ce thème avec des industriels comme ST Microelectronics, qui a développé des processus de simulation, qui permettent d’avoir un niveau de robustesse des circuits lors de leur conception. Autrement dit, il s’agit de modéliser et d’utiliser de la physique pour faire une chaine de parasites sur le circuit gérant une défaillance. C’est ce que nous en somme prospère d’hommes en 10 ans, que l’on appelle aussi “Failure in Time”, ou FIT. Parallèlement,

nous intégrons si nécessaire des circuits de dispositifs de surveillance, destinés à commander le bon déroulement de l’application en cours de fonctionnement. Dans certains cas, ces dispositifs peuvent contenir une erreur en temps réel. Une fois les protocoles bâtis, nous avons ensuite développé en laboratoire des techniques de qualification dans différents environnements. Cet objectif est d’être le plus écologique et de protéger au mieux les clients, il leur faut prévenir les événements les plus critiques de leurs utilisateurs afin de les protéger de manière efficace et d’améliorer le meilleur compromis coût/bénéfice. Les méthodes que nous développons peuvent être utilisées pour améliorer la sécurité des systèmes informatiques.

Grenoble INSTITUTE OF TECHNOLOGY
Le Prix de thèse de Grenoble INP

Le Prix de Thèse est organisé par le Collège Doctoral depuis 1990. Parmi les 200 thèses soutenues chaque année, un certains nombre d’entre elles sont récompensées par ce prix qui illustre d’une part l’importance que l’établissement accorde à la recherche et d’autre part, il révèle l’importance de cette recherche pour les entreprises.

Le lauréat (Doctorant à TIMA dans le groupe CIS)

Yannick MONNET (Micro&Nano Electronique)

Prix Spécial

Ce travail de thèse a porté sur la modélisation et la conception de circuits asynchrones (circuits sans horloge) résistants aux attaques par injection de fautes. Les contributions scientifiques théoriques sont l’analyse de la sensibilité aux fautes des circuits asynchrones et le développement de contre-mesures permettant d’améliorer leur résistance et leur tolérance à l’injection de fautes. Ces contributions ont été évaluées avec succès en pratique par l’attaque de circuits cryptographiques asynchrones à l’aide d’un laser. Publiés dans les conférences et revues spécialisées, ces résultats uniques valident les analyses théoriques et les contre-mesures proposées. Cette technologie a été transférée à la jeune société TIEMPO, qui l’exploite dans des produits destinés à des applications de transactions sécurisées.
WTC les 14 et 15 Octobre 2009 présence de TIMA -SLS sur un stand à ESWEEK
Hamid Lamraoui received the 2010 PhD. Award for innovation EMB (Engineering in Medicine and Biology) and IEEE France Section – SFGBM (Société Française de Génie Biologique et Médical) for his work on Design of an implantable urethral occlusion active system for treatment of severe urinary incontinence.
17. Social life

The Laboratory had the pleasure to congratulate some of its members for births.

Born children of Laboratory's members:

- Yannis ZERGAINOH 16 November 2010
- Alice HAMON 14 November 2010
- Alexia GASCARD 06 November 2010
- Cristina MAISTRI 06 August 2010
- Alexia Hao SHEN January 2010
- Samuel PERONNARD January 2010
- Rosemary GUERIN 11 November 2009
- Gabriel ANGHEL 10 August 2009
- Maëlisse KHEREDDINE 17 February 2009
- Wendelin MORIN-ALLORY 21 January 2009
Pictures 1:
TIMA picnic on June 19, 2009
Pictures 1:
TIMA picnic on June 19, 2009
Pictures 1:
TIMA picnic on June 19, 2009
Pictures 2:
Christmas party for the children on December 09, 2009
TIMA picnic on June 29, 2010
Pictures 3:
TIMA picnic on June 29, 2010
pictures 4:
F. paugnat distributing presents as Santa Klauss
Christmas party for the children on December 08, 2010
Pictures 4:
Christmas party for the children on December 08, 2010