Techniques de l'Informatique et de la Microélectronique pour l'Architecture des systèmes intégrés

Techniques of Informatics and Microelectronics for integrated systems Architecture
Foreword

TIMA Laboratory addresses the wide spectrum of the “Techniques of Informatics and Microelectronics for integrated systems Architecture”. TIMA is a public research laboratory sponsored by Centre National de la Recherche Scientifique (CNRS), Grenoble Institute of Technology (Grenoble INP) and Université Joseph Fourier (UJF). The research topics cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog devices to multiprocessor systems on a chip.

The research projects and perspectives of TIMA can be analysed along three main research themes, characterized by their long term objectives, scientific domain of expertise and research community. From physical sciences to computer science, these themes include:

Theme 1: design of integrated devices
Theme 2: test, dependability, security, and qualification of circuits and integrated systems.
Theme 3: design and verification methods and tools for system on chip architectures.

The laboratory is further composed of six research groups, each covering one or more themes: Architectures for Robust and complex Integrated Systems (ARIS), Concurrent Integrated Systems (CIS), Micro and Nano Systems (MNS), Reliable Mixed-signal Systems (RMS), System Level Synthesis (SLS), Verification and modeling of Digital Systems (VDS). These research groups are largely autonomous in managing their students and grants, but they also jointly cooperate in many large projects. Indeed, the interactions between the groups have grown in the past years: it is a policy of the Laboratory to offer a global research expertise while building cooperative projects with industrial and academic partners, in France, in Europe and in the world. In 2008, TIMA has contributed a record number of contracted projects, signed with public authorities (Rhône-Alpes Region, Agence Nationale pour la Recherche, Pôles de Competitivité, European Commission) as well as industrial partners. The abstracts of the largest cooperative projects are listed in Chapter 10, while their results are detailed in the scientific chapters of the groups, Chapters 1 to 6.

Dissemination of knowledge and research results is a constant effort. Chapter 13 provides the full references of the 115 refereed articles in international journals and conferences, 11 defended PhD’s, as well as other scientific productions. In particular, Yannick Monnet was awarded the "Thesis Prize" in Micro and Nano Electronics by Grenoble INP, with special mention for its impact and industry transfer.

Several other achievements in 2008 deserve special mention. The CIS group produced the world first secure asynchronous FPGA, in CMOS 65 nm technology; this reconfigurable circuit is natively protected against power and electromagnetic side-channel attacks (see section 2.11). The RMS group invented and filed a patent for a method to diagnose faults in embedded sensors for aeronautical applications (see section 3.4). The VDS group developed the VSYML (VHDL Symbolic Simulator in CAML) software, which has been made open source in the first trimester 2009 (see section 5.4). The ARIS group performed experiments at high altitude by means of stratospheric balloons successfully launched (see section 6.2).

Most of the permanent researchers of TIMA are academics. They teach in undergraduate and postgraduate courses, in University and Engineering curricula, mostly in Physics, Electrical Engineering and Computer Science. Moreover many of them are involved in continuous education programs, and contribute to research level summer schools and conference tutorials. In 2008, members of TIMA organized the SERESSA 2008 summer school on the Effects of Radiation on Embedded Systems for Space Applications, in Miami.

It is a tradition in TIMA to not only contribute papers in conferences, but also be active in their program committees and organization. In 2008, members of TIMA participated in the committees of 32 international conferences and workshops, among which they chaired or co-chaired DTIP in Nice, IOLTS in Rhodes, DCIS in Grenoble, DECIDE in Mexico, IMS3TW in Vancouver and DRVW in Santa Clara. The details of these activities and other international cooperation and participation to working groups are given in Chapter 11.

This annual report should provide our readers with a better understanding of our objectives, projects and achievements. It is available in electronic form on CD and on the web at: http://tima.imag.fr/

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1. Micro and Nano Systems (MNS)

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| - Design and technologies for Integrated Micro and Nano Systems  
- Micro power generators for autonomous microsystems  
- Wireless Sensor Network  
- Microsystems for health | - European: VIBES (IST)  
- National: BQR INPG  
- Industrial: CIFRE ST CEA-LETI  
- Memberships: GDR Micro Nano Systèmes | - STMicroelectronics  
- CEA - LETI  
- METRAVI 01db  
- MEMSCAP  
- Start-up company created: MEMSCAP (France). | - FEMTO-ST, France  
- G2E Lab, France  
- INL, France  
- LIPSI ESTIA, France  
- U. of Southampton, UK  
- Tyndall, Ireland  
- EPFL, CH  
- TIMC, France  
- LEM, Tunisia |

**Topics:**

In recent years, a very large amount of scientific work has been achieved around Micro-Electro-Mechanical Systems (MEMS). Some industrial success stories (accelerometers, gyroscopes and MOEMS) have shown their maturity. MEMS are now starting to take place around us in our everyday life as the microelectronic did 20 years ago. However, a lot of effort is still needed for the integration of ICs and MEMS. Nearly every kind of sensor or actuator has been successfully developed with MEMS technologies whereas a very little work has been done on integration of MEMS devices with complex integrated circuits. An important part of the MNS group research activity is centred on integrated MEMS with the vision of “Systems-On-Chip embedding MEMS” as target. We believe that the future of MEMS is beside millions of transistors in large mixed signal Systems-On-Chip. These integrated MEMS devices will act not only as sensors but also as actuators or electric devices like switches and filters.

Since 2003, the group is strongly involved in the miniaturization of nodes for wireless sensor networks. In this topic we address the problem of the energy, and its management which can increase drastically the autonomy of such tiny devices. Our approach is based on scavenging the environmental energy surrounding the node into electrical power which can supply it. We explore the design, fabrication and characterization of

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new microgenerators. We investigate ultra low power approaches for the energy management circuits and RF transceivers. Finally, we develop several hierarchical models associates with the different subsystems involved in a node. These models are implemented in different simulation languages and CAD tools used for the global simulation of a node.

In the last decade the MNS group has developed several demonstrators using well established microfabrication techniques available from several IC foundries. More recently, we carry on with the investigation concerning the integration of nano-accelerometer with advanced CMOS technologies based on SOI substrates. Since 2006, we have started the design and the fabrication of new Carbon Nano Tube based Nano-Electro-Mechanical Systems. Even more the electrical behaviour and reliability of acoustic devices (BAW) deposited on silicon substrates are under investigation. These topics are developed in collaboration with CEA-LETI and ST Microelectronics.

In 2007 we started a new topic of research concerning Microsystems for health. In tight collaboration with TIMC laboratory, we are investigating innovative way for the miniaturisation and integration of different functions for an autonomous urinary sphincter implanted in a human body.

1. 1  Miniature sensor nodes for wireless network

1.1.1  Introduction: wireless Microsystems

Over the recent years a growing interest in the field of miniature sensor nodes has be seen. A wide range of applications is already planned for their integration; from medical implants to embedded sensors in buildings. Despite the considerable effort of research in this domain, one area was left with little attention – the energy source powering the device. Until now, the majority of such systems was running on an electrochemical battery. This approach has a primary drawback – the device lifetime is directly linked to the battery size. Considering millimetre size devices, it is hard to extend lifetime beyond one year. A solution to this problem is to take advantage from the very low power consumption of current electronics; indeed such a device can be powered by harvesting external energy. Recent projects like SMARTDUST, WINS or SAND have used photovoltaic and thermoelectric principles, and thus have shown that scavenging energy from the environment is possible.

Mechanical energy is a promising solution since several natural mechanical sources exist: vibration, deformation, variation of constraint. The main advantage of this solution is the abundance of mechanical energy in the environment and their relatively high power. Another important point is that the device needs only to be coupled mechanically through its package with the environment, the microsystem itself is then isolated. One of the drawback is that classical sources of mechanical energy operate at frequencies below 100 Hz.

Since 2003, we have explored the design, fabrication and characterization of new microgenerators which convert the mechanical energy into electricity. At first, this research topic has been developed in the frame of the European research project called VIBES. We have fabricated MEMS piezoelectric microgenerators with very promising results and proposed innovative ultra-low-power electronic circuits for managing the power produced by these devices. Beyond the VIBES project, new approaches were developed, still with a strong focus on energy scavenging. The first one was the investigation of new generators based on flexible sheets of electro-active polymers. This work was done in collaboration with CARE one of the CEA-LETI laboratories. The second one opened a totally new road since it was based on temporal temperature variation. The project was created in collaboration with the Magnetic Actuators and MicroSystems team from G2EElab (Grenoble).

1.1.2  The VIBES project

Members: S. Basrour, Y. Ammar, M. Marzencki

VIBES stands for Vibration Energy Scavenging and is a Specific Targeted Research Project (STREP) of the 6th Framework Program of the European Union (EU). The project is leaded by University of Southampton; the rest of consortium is composed of public research laboratories (TIMA, Tyndall, University of Southampton, FEMTO-ST and EPFL) and companies (MEMSCAP, 01db METRAVIB and PHILIPS).

The goal of this project is to develop and demonstrate a micro power generator able to scavenge mechanical vibrations and motions from the surrounding (like building, machines, human body). This device will produce electrical power (in the range of µW) in order to supply an autonomous microsystem. The microsystem will embed an Ultra Low Power controller, a low power RF communication module, several
MEMS sensors and a micro battery for energy storage. The project will focus on piezoelectric and electromagnetic transduction principles implemented with MEMS microfabrication techniques. Figure 1 shows a schematic of the architecture of the autonomous microsystem in development within the VIBES project.

![Figure 1. Architecture of an autonomous microsystem including a vibration micro power generator](image)

1.1.3 Piezoelectric micro power generators

From the two initial transduction principle, piezoelectricity and electromagnetic induction, we decide to investigate more in detail a piezoelectric transducer. The reason is that piezoelectric materials are deposited by sputtering techniques and then are compatible with CMOS microfabrication techniques.

**Piezoelectricity**

Piezoelectricity is the property of some materials to generate electrical charges on their surfaces when they are subject to a mechanical stress, as shown in Figure 2. These materials are widely used either for actuation (where mechanical stress is induced by applied voltage – indirect effect) or for sensing (electrical charge appears when mechanical stress is applied – direct effect). The best bulk piezoelectric materials available are able to transfer mechanical energy to electrical energy with 80% efficiency.

![Figure 2. Schematic of the piezoelectric effect in a material subjected to a mechanical strain, electrical charges appear depending on the direction of the strain with different coefficient](image)

**Piezoelectric Microgenerator**

We have designed, modelled and fabricated several piezoelectric micro power generators. The device, as shown in Figure 3a is composed of a seismic mass made of Silicon 500µm thick connected to the substrate by a thin cantilever beam. When excited at its resonance frequency, the system moves according to its fundamental vibration mode. During the movement, a piezoelectric layer deposited on the cantilever is compressed and elongated. In consequence, thanks to the piezoelectric effect, electrical charges appear on the surface and are collected by the metallic electrodes. The generated alternative electrical signal is sent to an electrical load or to an Energy Harvesting Circuit that we describe in the next section.

The device is fabricated using MEMS microfabrication techniques that include piezoelectric thin layer deposition. It was created in cooperation with MEMSCAP, FEMTO-ST and EPFL. Basically, the process is composed of Deep Reactive Ion Etching (DRIE) steps on both sides of a Silicon On Insulator (SOI) wafer. We have used two materials for the piezoelectric layer. The first one is Aluminium Nitride (AlN), a material relatively easy to deposit by sputtering and environmentally friendly, but having low electromechanical coupling coefficient. The other is PZT (Lead Zirconate Titanate), much more difficult to create as a thin layer,
but with remarkable piezoelectric properties. Figure 3b shows an SEM photo of a PZT microgenerator.

![Figure 3](image)

**Figure 3.** Schematic of the mass/cantilever piezoelectric micro power generator (a) and SEM picture of the fabricated device (b)

**Performances**

We have fabricated and tested several such devices. A standard electrode layout covering the entire surface of the beam was used, presented in Figure 3, as well as some innovative solutions aiming at raising the output voltage and coupling coefficient. They consist either of implementing several piezoelectric capacities on one device, which is supposed to raise the output voltage, or integrating of interdigitated electrodes that permit to use the more energetically effective k33 mode of operation of the piezoelectric layer.

In the first place we have evaluated the output power dissipated on a matched resistive load. The device was excited using a controlled vibration source – a shaker, piloted by a function generator and a custom LabVIEW application (see Figure 4). The results for PZT devices are presented in the Figure 5. Powers ranging from 0.9µW to 1.4µW per device can be obtained with one device excited at antiresonance with 2g excitation amplitude. An important gain in power output can be obtained with the use of IDT devices. The output voltages at high excitation levels are sufficient for rectification and further use in an energy scavenging circuit.

![Figure 4](image)

**Figure 4.** Test setup used with a zoom on the tested device mounted on a shaker
Figure 5. Power output of one piezoelectric generator versus the excitation vibration amplitude, for a standard device (a) and for a device with interdigitated electrodes (b).

In case of absence of sufficient vibration source, several devices can be used together in order to provide power needed. We have estimated that power less than 400nW is required to power a simple wireless sensor node with a duty cycle of operation of about 1%. Therefore, our generators with conjunction with an energy scavenging circuit and an energy storage unit (a supercapacitor) can be used as a power source and replace the commonly used batteries.

1.1.4 Energy Harvesting Circuit

The goal of the power management module is to transfer the energy produced by the micro power generator to the energy storage module, i.e. the micro battery. In order to charge the battery, a stable DC voltage is needed with a specific voltage that depends on the battery characteristics. On the other hand, the signal coming from the µPG is generally alternative (AC) and the voltage can be very low (few mV). By consequence, some operations such voltage rectification and elevation are required. In addition, these operations must be made with the best efficiency and the circuit must have very low power consumption.

Figure 6 shows the standard architecture of the power management module. The Energy Harvesting Circuit (EHC) is composed of an AC/DC circuit for the rectification, and of a DC/DC circuit for the elevation of the voltage. The DC/DC circuit is managed by a digital controller which maximises the energy transfer from the power generator to the micro battery.

In the framework of the VIBES project, we have proposed several original approaches to overcome the problem of low voltages and power provided by the microgenerator. At first, we have designed a passive circuit based on a voltage multiplier (VM), which plays the role of AC/DC and DC/DC converters. It accepts tenth of mV as input. This multiplier uses diodes with very low threshold voltage. The second approach deals with the design of an ultra low power (ULP) AC/DC converter (tenth of nanowatt) able to rectify signals down to few mV.

Figure 6. Architecture of the Energy Harvesting Circuit
Voltage Multiplier (VM)
A voltage multiplier with 6 stages is implemented with STMicroelectronics CMOS 0.12 (HCMOS9) and the layout is reported in (Figure 7).

![Figure 7. Voltage multiplier integrated circuit](image)

This integrated circuit is assembled with a piezoelectric microgenerator as shown in Figure 8. It is up to now the smallest MEMS microgenerator with its power management module.

![Figure 8. A System in a Package composed by a microgenerator and a voltage multiplier](image)

The results of characterization show that we can obtain up to 1 volt at the output of the VM for very weak accelerations (50mG) (Figure 9). The resonant frequency of the microgenerator is close to 1500 Hz.

![Figure 9. Output voltage of the VM versus acceleration (1G = 9.8 ms⁻²)](image)

Another set of experimental results for this circuit is presented in Figure 10. We can see the transient evolution of the output voltage when a capacitor of 1μF is used as a load.
The harvested energy on this kind of load reaches 5.3 µJ after 250 seconds. It is clear that we can store more energy if we connect in series these circuits or if we wait more time. The efficiency of this kind of circuit is poor around 20% and depends strongly on the characteristics of the excitation signal (amplitude and frequency) and the number of stages implemented.

We have shown that this circuit can be used successfully with a piezoelectric microgenerator and can be adapted easily to the electromagnetic one designed by our partners in the VIBES project.

**The ULP AC/DC**

The AC/DC converter based on ULP comparators is implemented using the technology austriamicrosystems CMOS 0.35. The layout of this circuit is reported in Figure 11.

![Figure 11. Layout of the ULP AC/DC converter (austriamicrosystems CMOS 0.35)](image)

The electrical characterizations of this circuit have shown that it can rectify input signals with very small amplitude. Moreover this circuit can be polarized down to 2V and in this case its consumption is close to 1nW.

**Autonomous power management system**

The total efficiency of this ULP AC/DC circuit can reach 95% but it needs a voltage source. To overcome this problem we have proposed to supply the AC/DC with the voltage multiplier as shown in Figure 12.

![Figure 12. Schematic of an ULP AC/DC supplied with a voltage multiplier](image)
As a proof of concept we have performed the above-mentioned circuit with $C_{\text{alm}}$ equals 1µF and $C_{\text{recolte}}$ equals to 80nF. The transient response of this system is reported on Figure 13 when the input signal, 140 mV in amplitude, is provided by our piezoelectric microgenerator resonating at 1500 Hz.

![Figure 13. Transient response of the voltage on the output capacitor $C_{\text{recolte}}$.](image)

Thanks to this configuration, we succeeded in harvesting the ultra low power signal given by the microgenerator in an efficient way without the need of an external power supply. In a future work, we propose to cascade several modules in order to obtain the desired voltage for the miniature sensor node.

### 1.1.5 New generators based on electro-active polymers

**Members: C. Jean-Mistral, J.J. Chaillout, S. Basrour**

Electro-active polymers (EAP) include electronic polymers (piezoelectric, dielectric, conductive polymers) and ionic polymers (IPMC, ionic gels...). A complete state of art has led us to select four polymer families: dielectric, IPMC, electrostrictif and piezoelectric polymers.

For each polymer type, an electromechanical model has been developed to characterize the behavior of a simple structure (plate) according to a specific mechanical load (quasi-static or dynamic solicitation under 100Hz). According to our simulations the best promising electro-active polymers in terms of energy scavenging density are dielectric polymers. Their maximum energy density is about 1.21J/g. But in the worst case (high pre-strain), energy density can decrease down to 0.026J/g, value already close to the best ones available for piezoelectric materials. In Figure 14 is plotted the scavenging cycle for dielectric polymer.

![Figure 14. Dielectric generator cycle](image)
First prototypes (named A, B and C on the right figure) have been realized and characterized to validate our analytical model.

![Image of prototype](image_url)

**Figure 15. Dielectric polymer prototype and the output power harvested**

Various experiments have been performed: with different pre-stretch for the film, with different size for the dielectric generator. We obtain the same kind of curves with relative error between 10% and 30%. The improvement of the model is necessary. Dielectric characterizations have been performed to test the influence of temperature, frequency and pre-strain on dielectric constant, conductivity for example. First results show us a dielectric constant higher than the expected one at room temperature and at very low frequency. Moreover, mechanical contactless characterizations have been carried out to improve the model.

The model developed in this study is complete and validated by various experiments at room temperature. It takes into account a lot of parameters and can be used to design power generators based on dielectric polymers. The maximum energy density scavenged with this technique is about 1.21 J.g\(^{-1}\) for one cycle at constant charge Q. We are developing an innovating application for the scavenge energy from human walking. This system is a patch placed first in a knuckle and able to scavenge 100 μW to supply autonomous device for medical or sport applications. First prototype characterizations are under investigation.

In the near future, new power management circuits and miniaturized n-stacks structures will be studied.

### 1.1.6 Thermal energy scavenging


Before anything else, let's just start by explaining what we intend by thermal harvesting. Classically, thermal is a synonym of spatial gradient of temperature, that is to say a difference of temperature between two physical points. Such a gradient is commonly used in thermoelectronics where industrial micro generators are already a reality.

Our approach is somehow different since we focused our attention on temporal change of temperature, i.e. the evolution of temperature along the time. This field was not really documented and some state of the art was necessary in order to determine the various solutions available to answer this problematic.

One of the first considerations before starting this part was to choose the variation of temperature that will be considered. We selected the range from a human environment (some °C in one hour) to an industrial one (e.g. a car engine with a change of a few tens of °C in 5 s). Of course, the lower the temperature's change the better it is for an easy adaptation in every situation.

The preliminary research underline the fact that several possibilities existed that can be divided into two different routes: direct conversion (thermal to electric conversion) and indirect one. Pyroelectricity and magnetization change were part of the first group whereas shape memory alloys and hybridization of soft magnetic materials and piezoelectric belonged to the second one.

Shape memory was quickly discarded because it was too much dependent of the temperature evolution along time. This effect could have been counteracted by using magnetic shape memory alloys for example.
But those materials were quite a new discovery and thus not yet fully characterized. Consequently the knowledge on how to use them and how to prepare them was too difficult to obtain.

Magnetization change materials had also the same problem. In order to obtain a sufficient magnetic flux variation, the change of magnetization should occur across a time span as short as possible. This implies important variations of temperature during a small amount of time. This is impossible considering our initial requirements.

Pyroelectricity was then studied, with a special focus on PVDF (PolyVinylidene DiFluoroide) since some samples were already available. A first model based on the literature was elaborated in order to determine how much energy could be generated using pyroelectric effect. The amount of energy harvested by this technique is very weak.

Finally the last way explored was the one of the hybridization of piezoelectricity and magnetism. The system is composed of a bimorph of PZT upon which is glued a hard magnet (Figure 16). This magnet is attracted by a soft magnetic material when the temperature is below the Curie temperature. This is the default position of the generator. When the temperature overcomes $T_C$, the soft material is deactivated and the beam oscillates back to the neutral position. Changing from one state to the other is decoupled from the temperature temporal evolution due to the fact that the magnetic force is highly non linear. An off the shelf prototype has been built as a concept proof. Now the model has to be detailed and the optimisation of the geometry could then be developed. Some macro prototypes have been developed and some encouraging results have been obtained (100 µJ with a variation of $T$ between 38°C and 48°C)

1.2 Global simulation and co-simulation of heterogeneous systems

Since a few years, we can see the development of SoC that includes several technologies in the same substrate. For example, recent SoC includes digital, analogue and RF electronic circuits but also memory blocks (SRAM, MRAM), and specially MEMS parts. This fact leads to a certain amount of heterogeneity that has an effect on the design and validation aspects.

Until now, every technology has its dedicated design and validation tools based on different levels of description (from system to device) and process of simulation (for example event or time driven). A very active research effort has been spent on the development of Co-design tools that can manage the design of both hardware and software parts of a digital system. With the addition of analogue, RF, optoelectronics and MEMS parts, there is still a lot of work to build a design environment that can manage the validation of every part of an heterogeneous system within the same framework.

The goal of this work is to develop both design methods and tools for the validation of heterogeneous systems. In this specific project, we focus on the design of an autonomous microsystem.

This work is divided in two main tasks which are:

- Modelling at different abstraction level and with a hierarchical approach of the different blocks of a system,
- Global simulation and co-simulation
1.2.1 Modelling of the Energy Harvesting Circuit
The models are described using analytical expressions or by equivalent electrical circuit. Our case study is
the whole system reported in Figure 18 and includes:
- a piezoelectric micro power generator,
- an Energy Harvesting Circuit (§ 1.1.4),
- a microbattery,
- and a digital controller.

![Diagram of the autonomous microsystem used for the simulation](image)

**Figure 18.** Block diagram of the autonomous microsystem used for the simulation

Simulink is an environment of Matlab which supports the heterogeneous modelling (multi domains, mixed
signals, multi languages) of our microsystem. Within this environment, the piezoelectric microgenerator,
Energy Harvesting Circuit and the micro battery have been modelled at circuit level using electrical
components available in the SimPOWER toolbox. At first, the controller is described with analytical equations
and then a VHDL implementation was done in order to be simulated with SMASH\(^1\) or MODELSIM\(^2\)
simulators.

1.2.2 Global Simulation and co-simulation with the Matlab-Simulink environment
*Members: A. Zenati, S. Basrour*

**Figure 19** shows the different parts of the global model. It is composed (on the top) of the hardware parts of
the microsystem and on the bottom of the two different representation of the digital controller (analytical
equations and VHDL).

---

\(^1\) Dolphin Integration

\(^2\) MENTOR Graphics
The global simulation has been performed with Simulink only. On the other hand, the co-simulation has been realized using both Simulink and SMASH or Modelsim simulators.

Figure 20 presents the comparison of the $I_{\text{bat}}(t)$ curves (current reaching the microbattery) obtained with different simulation methods and the experimental results.

The simulation results are very close whatever the simulation methods. These results show the same qualitative behaviour compared with the experimental data. Quantitative discrepancy comes from a mismatch on several physical parameters like MOSFET transconductance or battery capacity.

At the moment, simulations have been carried out with electrical equivalent models for both the $\mu$PG and the battery. These simple models will be replaced in a near future by more complex descriptions models.
Concerning the µPG, the electrical equivalent model will be replaced by a behavioural model based on an analytical description taking into account several shape factors and material parameters. In addition, a model order reduction technique will be employed to produce a compact model from a complex finite element analysis.

1.2.3 Modelling and simulation of a RF Transceiver with Matlab-Simulink

Members: G. Terrasson\textsuperscript{1,2}, R. Briand\textsuperscript{3}, S. Basrour

Recent advancements in microelectronics and micromechanics have enabled the development of microsensors. This device embeds a controller, several sensors, a communication module and an energy supply. However, the development of microsensors is limited by lifetime constraints imposed by the energy supplies. In this device, the communication module contributes the most to the global consumption. So, purpose of several research projects is to develop new communication protocols and increase communication module energy efficiency.

In this context, the goal of our research is to develop a new approach to conceive a transceiver with power consumption constraint. Firstly we have to choose a transceiver architecture which seems to be a good compromise for microsensor applications. Then, we adopt a top-bottom method.

The first step consists to model the overall system to determine all functional block parameters. The transceiver model takes into account all the particularities of electronics devices and transceiver architecture like noise, substrate coupling and non-linearity.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Figure21.png}
\caption{First transceiver model with MATLAB-Simulink (Version 7.0.1)}
\end{figure}

\textbf{Figure 21. First transceiver model with MATLAB-Simulink (Version 7.0.1)}

\textbf{Figure 21} illustrates the first transceiver model develop with MATLAB-Simulink. The second step is to model and optimize functional blocks. The first block modelled is the Low Noise Amplifier (LNA). The goal is to implement in a LNA topology parameters obtained in the first step and to determine components parameters (gate width of transistor, value of resistance, inductance..). To validate the model, a comparison between Matlab-Simulink and Cadence simulations is used. \textbf{Figure 22} demonstrates that Matlab-Simulink LNA model we developed is near to the Cadence model. However, Matlab-Simulink simulation is faster than Cadence simulation.

\begin{itemize}
\item \textsuperscript{1} TIMA
\item \textsuperscript{2} GE2 Lab
\item \textsuperscript{3} LIPSI
\end{itemize}
Figure 22. Simulink and Cadence simulations

Using the functional block model, the next objective of our research is to optimize the topology to obtain weak consumption with better performances (gain, noise, linearity).

Finally, these models will be reused in the global simulation of a node.

1.2.4 Global Simulation and co-simulation: the VHDL-AMS approach

Members: H. Boussetta, S. Basrour, A. Soudani, R. Tourki

In parallel with this block modelling approach, we proposed a novel top/down methodology for behavioural and structural modelling of multi domain microsystems. The study case is an integrated power harvesting circuit used for supplying power to nodes in wireless sensor networks. The system is composed of a MEMS structure (in our case a microgenerator) and an electrical circuit which boosts and rectifies the low amplitudes AC signals delivered by such generators. This electrical circuit is based on a voltage multiplier composed with ultra low threshold voltage diodes. The classical validation of such systems by separate simulation of each element: FEM analysis for mechanical part and traditional circuit-simulators for electrical part does not offer the possibility to predict the behaviour of the complete system. To overcome such limitations, we propose to use a simulation environment based on VHDL-AMS and SPICE languages.

Concerning the modelling of the microgenerator, we start from one dimensional system where only the general behaviour of such transducer is presented. The model was kept intentionally simple to focus on the functionality of the piezoelectric transduction. Then, an enhanced model of the piezoelectric generator developed on our research group is introduced in order to better predict the real behaviour of such system. The design of the enhanced structure is based on the microfabrication techniques of the SOI substrate. Several important considerations are taken into account especially the important size of the mass compared to the one of the beam, the rigidity of the mass and its rotational inertia. It is also important to consider that the acceleration is applied to the mass and not to the end of the beam.

Described models are parameterized using generic interface lists in entity declarations. This way of coding makes our models good candidates for reuse just by changing constants that define physical and geometric parameters. Then, those numbers of degrees of freedom (geometric and physical) multiply analysis possibilities and so greatly cut down the simulation time compared to the FEM computation. Thus, the proposed enhanced model can be used to obtain several valuable results. First, we will study the impact of the piezoelectric properties of the material used on the model by keeping the same dimensions of both devices and just changing the piezoelectric material layer. The used piezoelectric materials can be either Aluminum Nitrite (AlN) or Lead Zirconium Titanate (PZT) thin layers. To study the microgenerator with AlN layer, we just have to substitute the generic parameters responsible of physical properties of the used material (PZT) in the entity declaration of the previous model by AlN ones. A sinusoidal acceleration of 1g was used to simulate the submodel of the microgenerator. A seismic mass of 400 \( \mu \text{m} \) by 400 \( \mu \text{m} \) and a beam of 400 \( \mu \text{m} \) length in an SOI wafer (410 \( \mu \text{m} \) thick) were used. An AC analysis was first carried out to study the behaviour of the system versus frequency. As shown in Figure 23, we have noted lower amplitude and higher resonant frequency for the AlN material. This result was expected because of the poor coupling coefficient of AlN material compared to PZT one.
To model the power management circuit described in section 1.1.4, we chose SPICE language. In fact, instead of trying to equal SPICE compact models, we decided to use parameterized SPICE models given by the tool. Thus, we had to select the appropriate model of transistor. The Level1 MOS was selected in order to decrease simulation time. In fact, this model is a basic MOSFET model generally used for discrete components especially in power electronics but it is a good compromise between accuracy and time in system level simulations. To improve the accuracy of the model, BSIM4-V4 (level 54 in Smash™ 8.0) can be then used. This model takes into account the effects of device geometry and process parameters. It enables us to better predict the real behaviour of such system but it notably slows down simulation time. Global simulation results are presented on Figure 24. The simulated model consists on a structural connection between the parametric microgenerator with AlN layer connected with a structural model of a six stages voltage multiplier.

![Graph showing comparison between PZT and AlN materials](image1)

**Figure 23. Comparison between the piezoelectric microgenerators with the same mass but based on PZT and AlN materials**

![Graph showing simulation results curves](image2)

**Figure 24. Simulation results curves of 1µF capacitor charge for two different values of input acceleration amplitude.**
1.3 Design and technologies for Integrated Micro and Nano Systems

1.3.1 Nano-accelerometer on thin SOI

*Members: S.Basrour, T. Baron\textsuperscript{1,2,3}, E. Ollier\textsuperscript{2}, X. Gagnard\textsuperscript{3}*

Thin SOI technology is capable to push forward the possibilities by offering the ability of “In-IC” integration of NEMS (Nano-Electro-Mechanical Systems) structures. The benefits are size and cost reduction for sensors and increase of functionalities for ICs. This situation is also an opportunity to benefit from the attributes of NEMS. In particular, this approach is attractive for low cost accelerometers. This work proposes to investigate thin SOI accelerometers based on a nano-beam resonator, the acceleration being detected thanks to a frequency shift.

Q factors related to this kind of nano-structures have been calculated by taking into account thermo elastic damping, support losses and also surface damping. Figure 25 presents the theoretical Q factors for our structures 160 nm thick with a length on width ratio of 100. A typical Q value is 2140 for a nano-beam 100 nm wide and 6 µm long. We also see that the main losses are due to anchor and surfaces.

![Figure 25. SEM pictures of a nano-beam resonator (L = 6 µm, W = 100 nm, g = 200 nm) (a) and Theoretical Q factor for nano-beams 160nm thick and length/width ratio=100 (b)](image)

The small dimensions of these devices produce very weak electrical signals very difficult to detect with standard characterization techniques. To measure electrical signal, an “In-IC” integration of NEMS process is under development with CEA-LETI and ST Microelectronics. To characterize nanostructures for understanding physic behaviour in these sizes, some characterization tools are also developed with these partners

\textsuperscript{1}TIMA
\textsuperscript{2}ST Microelectronics
\textsuperscript{3}CEA LETI
1.3.2 Nano-Electro-Mechanical Systems based on carbon nanotubes

*Members: Z. Raslan, S. Basrour, A. Ghis.*

Nanoelectromechanical systems (NEMS) are a novel approach to nanotechnology where strong coupling between electrical and mechanical degrees of freedom is utilized to design new devices with a typical length scale in the nanometer range. The field is rapidly expanding and the potential for applications is high. The interest is largely due to the potential of NEMS to operate at high frequencies with ultra-low power and small dissipation. The extraordinary properties of carbon nanotubes (CNTs) make them ideal candidates for building blocks of NEMS. Different devices based on CNT as actuators, resonators, RF filters, sensors, electromechanical transistor and memory have been investigated in literature.

Our research interests in the coupling of electromagnetic signal with vertical CNT array in the GHz range for telecommunication systems. We aim to develop a RF filter based on mechanical resonance phenomenon of carbon nanotubes arrays. We expect according to Drude-Lorentz theory that carbon nanotubes at their eigen-frequency oscillate with maximum deformation and absorb the energy of the input signal leading to a band-rejection filter. The picture (here after) shows a nanotube array and the conditions on the electrical field which is needed to allow the vibration of nanotubes and the wave propagation.

![Sens de propagation](image)

*Figure 26.*

To explore this mechanism we propose to make the growth of carbon nanotubes on a coplanar microwave line.

![Figure 27.](image)

*Figure 27.*

We are currently collaborating with different departments of LETI and LITEN for realizations and electrical tests. We start by some realizations to extract mechanical and electrical features of nanotubes and arrays. Theses features are needed for the design of the filter. Other structures based on horizontal carbon nanotubes are under test, interesting results are already observed.
1.3.3 BAW devices for RF application reliability

Members: N. Ben Hassine\textsuperscript{1,2,3}, S. Basrour\textsuperscript{3}, D. Mercier\textsuperscript{2}, P. Renaux\textsuperscript{2}, C. Chappaz\textsuperscript{1}, P. Waltz\textsuperscript{1}

The Micro Electro Mechanical Systems (MEMS) market is growing steadily with time, providing the automotive, telecommunications or space industry with components such as accelerometers, pressure sensors, and gyros, and also RF filters. Among these latter components; Bulk Acoustic Wave Resonators (BAW) (Figure 28) are developed and investigated at the CEA-LETI.

![Figure 28. BAW resonator structure](image)

As MEMS achieve maturity, reliability concerns become of paramount importance. The successful marketing of MEMS requires preliminary identification and elucidation of possible failure mechanisms, in order to evaluate the probability of the component to perform the required functions over its lifetime.

![Figure 29. Measurement bench setup for RF power tests](image)

As a consequence, the objective was to contribute to a better understanding of the failure mechanisms occurring during BAW components operation especially when RF power is applied to the device (Figure 28) which generates internal heat that is enable to impact key parameters of BAW resonator. Some finite element simulations using ANSYS (Figure 29) were done.

Since BAW resonators are in the simplest case Metal-Insulator-Metal (MIM) capacitors, measurement under bias of Mo-AlN-Mo capacitances was performed as well as leakage and relaxation current in order to predict bias impact in BAW devices and to give a physical and theoretical explanation for the observed phenomenon. In particular, a deep study of electrostrictive effect in AlN was carried out.

\textsuperscript{1}STMicroelectronics
\textsuperscript{2}CEA-LETI
\textsuperscript{3}TIMA
1.4 Dynamics electronic urinary sphincter

*Members: H. Lamraoui, A. Bonvilain, P. Cinquin, S. Basrour*

Urinary incontinence is defined as the involuntary leakage of urine and there are several surgical methods to alleviate. In the event of a major leak, the establishment of an artificial urinary sphincter can give patients a normal social life. At the moment, there is only the prosthesis developed by the American Medical System company which remedies severe incontinence.

We propose a study on a dynamics regulatory system that improves its efficiency by adjusting the behaviour of the system to the patient and his lifestyle. We envisage also a communication between the implant and the outside world via a RF link (Figure 31).

Our work lies in the development of command and in the study of energy consumption. The command consists of micro-actuators, microsensors and an electronics control. The energy consumption necessary for a long enough functioning device is defined, in order to provide the most appropriate solution. One demonstrator is currently under realisation, and the experimental results allow us to verify energy consumption forecast and consider in the longer term the fuller integration of the device.

In this work, the critical elements that must be taken into account concern biocompatibility (for implantable elements), the operating voltages, and the effective temperature.
2. Concurrent Integrated Systems (CIS)

Group Leaders: Laurent Fesquet, Gilles Sicard
(e-mail: Laurent.Fesquet@imag.fr; Gilles.Sicard@imag.fr)


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* With VDS

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2.1 Introduction: asynchronous circuits and systems

The global synchronization strategy of synchronous circuits was introduced in the early 70s because at that time, it was a satisfactory answer to design needs and technological potentials. This initial choice of an implementation strategy drove and is still driving the design of algorithms/architectures, languages and CAD tools. Today, integration potentials of advanced technologies are going beyond design productivity, and one can wonder whether the synchronous circuit style is still relevant. Asynchronous circuits which were introduced in the mid 50s, receive now increasing interest. What significant benefits are they likely to offer? Can they contribute to improve design productivity in the future?

Our motivation is to answer these questions, investigating what impact asynchronous circuits may have on the design of integrated systems and how to take advantage of this circuit style at different levels: circuit level, architectural/algorithmic level, specification level, and system level? Because asynchronous circuits provide more flexible, robust and reliable synchronization and communication mechanisms, they give rise to alternative and innovative solutions that have to be analyzed and evaluated.

At the circuit level, asynchronous logic enables the design of delay insensitive circuits which do not require accurate and costly delay characterization. In fact delay insensitivity guarantees a correct functional behavior independently of the propagation delays in the basic components (gates, interconnects,...). Delay insensitive asynchronous circuits are for example insensitive to some emerging problems like delay fault due to crosstalk. The delay insensitivity property makes asynchronous circuits very promising to explore and exploit advanced CMOS and future technologies.

Eliminating the global clock, which synchronizes all parts of circuit in synchronous logic, provides more flexibility to design system architectures. In fact, the control is naturally distributed rather than centralized. Hence, communications as well as synchronization through «rendezvous» for example, are easily implemented by a collection of independent and local finite state machines, which do not require knowing the state of the whole system. Data to be computed by the system flow in the architecture as fast as they can accord resources' availability and hardware implementation. The processing cost (in terms of delay and power consumption) is exactly the image of what is specified by the algorithm, given the chosen hardware implementation. It means that speed and power consumption may depend on the data processed. The data-flow behavior of asynchronous circuits, at any level of granularity, is the source of significant improvements in terms of speed/power optimizations and ease of design.
Today, one of the main challenges is the design of efficient and convenient CAD tools for asynchronous circuits. This is currently one of the priorities of our research work. We have adopted a CSP based language, called CHP, as the specification language (introduced by Alain Martin - Caltech). The specification and development of a design framework for asynchronous/synchronous circuits is in progress. This work follows two main motivations: 1) to provide the asynchronous circuit designers with a powerful execution/simulation framework, mixing high-level CHP descriptions, HDL programs and gate level descriptions, 2) to give to synchronous designers familiar with existing HDL-based top-down design flows, the opportunity to include clock-less circuits in their designs. The main challenge is to efficiently synthesize behavioral descriptions written in CHP into gates. One of our goals is to provide a synthesis tool that would target different styles of circuit, QDI and Micropipeline circuits, thus enabling designers to compare the merits of different approaches.

Finally, asynchronous circuits also bring flexibility at the system level. Complex, highly concurrent image processing applications naturally take advantage of the locality and modularity of clock-less circuits. Because they don’t need a global synchronization signal, modularity is a major property of asynchronous circuits which enables the design of complex integrated systems by simply assembling functional blocks. Design time is thus reduced and reusability increased. As an example, the design of locally-synchronous globally-asynchronous SoCs bring a solution to the problem of communications between distant parts using long interconnects. Without requiring drastic change in terms of tools and methodologies, synchronous parts of SoCs may be interconnected using advanced and robust asynchronous interfaces.

The potentials of asynchronous circuits are being investigated through the design of portable systems (from smart-card to multimedia terminal). There are three main properties of asynchronous circuits that can improve such systems and/or make their design easier: electromagnetic compatibility, low power and free power management, flexible interfacing capabilities. Interfacing digital asynchronous circuits with analog parts (RF front-end, sensors, actuators, etc.) is also a major field of interest. It is in fact essential if we expect to successfully design SoCs that may integrate various kinds of digital and analog parts.

2.2 The TAST design environment

TAST stands for TIMA Asynchronous digital circuit Synthesis Tools. This is a design environment which is gathering researches carried out in the group on asynchronous circuits design methods and associated CAD tools.

It consists of a compiler/synthesizer with the capability of targeting several outputs from a high level description language. We have adopted a high level description language derived from CHP (Communicating Hardware Processes introduced by Caltech) with specific features to cope with communication protocols, data encoding, arbitrary precision arithmetic, non-determinism, hierarchy, project management, and traceability. All these features make our CHP a very practical system description language to develop with. It also makes scalability and modularity easy to manage.

The flow (Figure 1) is organized around an intermediate form based on Petri Nets (PNs) associated to Data Flow Graphs (DFGs). Such models have been used for years to model synchronous circuits and systems and find a particularly adequate application in the field of asynchronous digital circuits and systems design.

CHP models can be simulated using our non-deterministic simulator which fully supports the semantic of the TAST CHP language. The simulator includes powerful commands to trace code execution, compute statistics along simulation runs, perform code coverage, watch process variables, etc... Petri Nets animation is also provided to enable didactic analysis of CHP model behaviors.

CHP synthesis into asynchronous digital circuits is based upon the DTL (Data Transfer Logic) specification we have defined. It provides a set of rules to guarantee that PN-DFG graphs are synthesizable into asynchronous digital circuits. DTL CHP programs are compiled into M-ary Decision Diagrams (MDDs) which are reduced, factorized and synthesized into QDI circuits. It is theoretically proven that all these steps preserve the Quasi Delay Insensitivity of the circuits.

Technology mapping is finally applied to enable the designer to freely choose its preferred target. He/she can choose between conventional synchronous standard cell libraries, dedicated libraries including C-elements for example (like TAL), or even FPGAs.

Current research is carried out in the CIS group to improve TAST in the following areas:
- get better performance of synthesized circuits in terms of area, speed and power,
- security driven synthesis to get power attack resistant and fault tolerant circuits,
- EMI (Electro Magnetic Interference) driven synthesis,
- testability and ATPG,
- formal verification of models and circuits (collaboration with the VDS group).
SystemC add-on
SystemC is a Hardware Description Language (HDL) based on C++ allowing describing a system at different levels of abstraction. SystemC provides a set of predefined ports and channels which enables communication between entities. An open source simulator allows simulating and testing a system modeled in SystemC. The SystemC library and simulator were designed for modeling synchronous circuits and thus have some limitations for modeling asynchronous circuits. We have defined a new subset of SystemC called ASC (Asynchronous SystemC) allowing to accurately modeling asynchronous circuits. This SystemC subset is based on a set of ports and channels primitives offering the same communication primitives as the common languages used for asynchronous circuits modeling (CHP, Tangram or Balsa). ASC also offers some new operators and statements allowing to accurately modeling the basic components of an Asynchronous Network on Chip. We are also doing some modifications on the SystemC simulator kernel for efficiently simulating the models described with ASC. Our final goal is to be able to synthesize these ASC models with the TAST framework. We are currently formally defining the semantic of the ASC library for being able to efficiently synthesize ASC based models.

2.3 The TAL Libraries
(Collaboration with Tiempo)

TAL-130 stands for TIMA Asynchronous Library; it has been designed using the standard CMOS 130nm process from STMicroelectronics in collaboration with the LIRMM laboratory. The library contains around 170 standard cells that we unfortunately do not find into conventional synchronous standard cell libraries. About 30 different functionalities implementing various kinds of C-elements and combination of C-elements have been included in the library. All the cells of TAL are layout compatible with the standard cell library provided by ST so that the designer can mix the use of conventional and TAL cells in his/her design. Moreover, TAL can be use in all the standard design tools such as Cadence, Synopsys, Modelsim, …

The aim of TAL is to enable the design of asynchronous circuits that are smaller, faster and which consume less power than those obtained using conventional synchronous standard cell libraries. To evaluate the performance gains brought by the library, two cryptographic circuits (AES) have been designed and fabricated using TAL-130. The next table presents a comparison between an AES design with the TAL library and a previous version of the same circuits exclusively designed with conventional standard cells.

A new version of TAL 130 has been designed. The aim of this version is to propose low-power cells in term of dynamic consumption and static consumption. This library can also be used with low-Vdd values. This library is compliant with the core standard cells available in ST 130nm design kit.
TAL-65 is a library with asynchronous cells, designed using STMicroelectronics 65 nm CMOS process. The library contains about 150 cells all compliant with the core standard cells available in ST design kits. The TAL-65 library also includes some specific cells required for the design of asynchronous network on chips. TAL-45 is currently a library under design which is fully compliant with the 45 nm ST CMOS standard cells. This library contains about 40 cells.

2.4 CMOS Imagers with High Dynamic Range
(Collaboration with E2V Semiconductors)

Novel applications require the study of a new class of CMOS imager which has to work within a hard light condition. One of the goals of The PICS Medea+ European project is to explore the possibility to design such CMOS sensors while being compliant with industrial constraints. The critical conditions and properties this work has to tackle are:

- Light conditions: This kind of vision system has to work within a hard light condition. A wide input dynamic range is expected for the sensor together with an efficient anti-blooming system.
- The pixel cannot exceed 100µm² which limits the maximum number of transistors and requires choosing between full-PMOS or full-NMOS transistor circuits.

Therefore, the imager has to provide a high input dynamic range (up to 100dB) and an instantaneously image acquisition (Global Shutter system) whereas currently available CMOS imagers provide an input dynamic range around 65dB and implement sequential image acquisition (Rolling Shutter system). Using a CCD sensor which provides around 80dB of Dynamic Range is not possible due to the fact that the imager could be integrated in a System on Chip.

A first circuit has been designed in collaboration with Atmel with a dedicated advanced imaging technology. The pixel architecture respects the main constraints of the PICS project: Area under 100µm², global shutter, and an expected Dynamic Range up to 100dB. This test-chip was fully tested (Figure 2).

A second test chip, called “Imagyne 2” is being designed and focused on light adaptive system. It includes an array of 128x128 standard pixels and an array of 64x64 2T logarithmic pixels. These two arrays are designed together: one Log. Pixel and four standard pixels are drawn together. The goal of this logarithmic array is to provide continuously the mean illumination value. With this information, we can perform the ideal integration time value of the standard pixels array at each image. This anti blooming system requires few transistors (0.5 / pixel) and induces a reduced silicon overhead (less than 20%) in relation to the state of the art. This chip uses the 0.35µm CMOS technology from AMS via CMP. Experimental results are shown in figure 3.
Figure 3. Results of imagine 2 CMOS Imager. A) when light condition is modified (B and D cases), a basic sensor provides saturate images. B) With Imagine 2 sensor, the integration time value is always the optimized one.

2.5 Secure circuit design and smart-cards

2.5.1 Integrated system for contact less smart-cards

(Collaboration with France Telecom R&D & STMicroelectronics)

We have designed MICABI a Contactless Smart-Card Chip which integrates an on-chip coil connected to a power reception system and an emitter/receiver module compatible with the ISO 14443 standard, together with the MICA 8-bit microcontroller described above (see Figure 4). Beyond the contactless smart-card application field, this new chip demonstrates that System on Chip integrating power reception and management, radio-frequency communication and signal processing are feasible. The chip, fabricated in a CMOS 6 metal layers 0.25 µm technology from STMicroelectronics, associates analog/digital parts as well as synchronous/asynchronous logic.

Power reception and data transmission are performed using a modulated magnetic field emitted by the reader. The antenna was integrated on silicon (on-chip coil), using 5 metal layers, to suppress interconnect issues and decrease card cost. Computation power in the card-chip is provided by the MICA quasi delay insensitive microcontroller in order to limit power consumption, noise, and sensitivity to supply voltage variations. The 8-bit microcontroller core integrates a 32 Kbytes RAM and a 2 Kbytes ROM containing a BIST (Built In Self Test) and a boot program.

The power-supply reception system is designed in order to allow operation of the micro-controller while in reception or in emission. A voltage regulation system decouples the micro-controller voltage supply and the RF front end voltage supply which transmits data. This regulation ensures correct operation of the RF front-end while the micro-controller is in operation at its own speed according to its data treatment and received current. In normal mode of operation its supply-voltage is regulated to 2 volts. At this voltage level the microcontroller delivers 18.6 Mips on average and consumes about 13.3 mW. At 1 volt, the core still delivers 4.3 Mips and consumes only 800 µW.

A dedicated interface between the asynchronous processor core and the ISO 14443 compliant analog emitter/receiver module was designed. This interface implements a handshake-based protocol which ensures minimum power consumption and noise when the chip is receiving or emitting data.
2.5.2 Secure circuits design

The goal of this research is to propose new design methods and tools to improve circuit resistance against non-invasive attacks such as timing attacks, PA (Power Analysis), EMA (ElectroMagnetic Analysis) and FA (Fault Analysis). Today, cryptography and cryptanalysis are both evolving very rapidly opposing hackers and secure systems providers. The smart card market is the primary concerned, but e-commerce, e-banking and data ciphering in general are all sensitive to attacks. Searching for new counter measures against such attacks, jointly at the software and the hardware levels, is becoming a major issue.

DPA attacks consist in measuring current consumption or electromagnetic emission of a running circuit in order to extract secret or private information. Glitch attacks are methods to disrupt circuit execution by applying sharp signal changes to the clock signals or to the power supply lines.

The asynchronous technology provides a means for designing DPA resistant circuits. In fact, it can be shown that quasi delay insensitive circuits can be designed so that the execution time and power consumption do not vary with the data processed. Thus, the electric and electromagnetic signatures of a running circuit are data independent making DPA type attacks inefficient.

In this field, the challenge is to get the best of asynchronous circuits to improve security at the smallest cost as possible. Today, known solutions are rather costly in terms of area. Current works carried out in the CIS group are focused on low-complexity secure asynchronous circuits.

Glitch attacks in particular and DFA (Differential Fault Analysis) in general, are also important issues that we are currently investigating theoretically.

MICA processor

On the practical side, we have recently performed DPA on the MICA microprocessor (see section 2.13). Results obtained when performing power analysis on the MICA 8-bit QDI asynchronous micro-controller reveal that the processor resists to standard DPA attacks. These results practically demonstrate the relevancy of using the asynchronous technology to design new secure circuits for smartcards and cryptographic applications (Figure 5).
Figure 5. Photography of the hardware system used to perform DPA measurements. The curves were obtained averaging the current consumed by the processor over 10000 runs of two different programs: (load FF, load 00, FF xor 00) and (load 00, load 00, 00 xor 00). The current consumption remains the same, and appears then not to be data dependent.

DES and AES crypto processors
DES and AES crypto processors were designed to evaluate the benefits brought by asynchronous logic to improve circuits’ resistance against power analysis attacks. DES prototypes (Figure 6) were jointly designed by TIMA, LETI and STMicroelectronics within the Esp@ss-is Medea+ European project. The goal of this work is to study the introduction in smart-card IC design of an innovative hardware technology, namely Asynchronous Logic, and to evaluate how it can improve security. A test board is under development to enable us to perform Differential Power Analysis and measure the ability of this technology to resist against such attacks.

Figure 6. QDI DES crypto processor

Fault tolerant QDI asynchronous circuits
Differential Fault Analysis (DFA) is a well-known method for cryptanalysis. With DFA it is possible to retrieve secret cryptographic keys by analysing the results of correct and erroneous cryptographic computations. A successful DFA attack depends on two conditions. First: the algorithm must be known and vulnerable. Second: it must be possible to induce faults on the hardware platform. The procedure of DFA depends on the cryptographic algorithm. Successful attacks were done on the Data Encryption Standard (DES). QDI asynchronous circuits are attractive to design fault resistant systems against a large class of faults. We show that the fault resistance of a circuit can be improved by exploiting QDI asynchronous logic properties. A secure fault tolerant DES prototype was designed to evaluate the hardening techniques we apply against fault injection (Figure 7). The secure circuit is only 7% larger and about 20% slower than the non secure initial circuit. Both the reference and the secure circuits are to be tested under a laser fault injection system within the Duracell RNRT project (Figure 8).
The counter-measures implemented in the secure version have been evaluated and validated. The fault tolerance of the protected modules was improved by 2.5 and all the faults injected were either filtered by the counter-measures or detected by alarm cells. Thus a DFA appeared impracticable on the secure version.

It is worthwhile to mention that the proposed techniques to harden the QDI circuits against faults do not alter the counter measures that can be applied for PA. Therefore, this technology enables us to jointly harden circuits against fault and power attacks.

### 2.6 Modeling and design of asynchronous priority arbiters for on-chip communication systems

The design of complex arbitration modules, like those required in SoC communication systems is addressed. Clock-less, delay-insensitive arbiters are studied in the perspective of making easier and more practical the design of future GALS or GALA SoCs. The work focuses on high-level modeling and delay-insensitive implementations of fixed and dynamic priority arbiter. Gate-level electrical simulations show that arbiters which are able to process several hundreds mega requests per second can be designed using the 0.18 µm CMOS process of STMicroelectronics.

One of the critical components of a SoC is the communication system, commonly named on-chip bus. Such an on-chip communication system has to be very flexible to interface in-house and external virtual components, providing high bandwidth, low latency, low power, arbitration mechanisms and routing capabilities.

In a SoC the on-chip bus connects the components to each other and dynamically allocates a path from one block to another. Several blocks running concurrently may require accessing the same resource leading to contentions. In this case, an arbiter is needed to solve the conflicts and to ensure that only one block is accessing the resource. The choice is done with the help of priorities affected to each request.

Several arbitration algorithms were proposed in the past to solve the problem of accessing a unique resource from an arbitrary number of blocks. These algorithms can be classified according to the characteristics of their corresponding hardware implementation. To mention a few, arbitration structures can be distributed or centralized, can be linear like daisy-chain arbiters, or ring-based like token-ring and round-robin arbiters.

Most on-chip communication systems and the arbitration modules they include are today designed with synchronous circuits. In this paper, delay-insensitive asynchronous arbiters are considered, to be part of future on-chip busses of GALA (globally asynchronous locally asynchronous) or GALS (globally asynchronous locally synchronous) SoCs.
In the SoC design perspectives, delay-insensitive arbiters have this main advantage of being hundred-percent reliable (enough time is given to resolve metastability). Today, reliability of on-chip communication systems is a major issue since the increasing transaction rate is drastically reducing the so-called Mean Time Before Failure characterizing clocked synchronizers.

As far as power consumption is concerned, such event driven communication/arbitration structures have a minimal electrical activity. Indeed, unlike clocked circuits, power consumption of delay-insensitive asynchronous arbiters is proportional to access rates. Furthermore, delay insensitivity enables the design of fast “long distance” communication busses. Finally yet importantly, such delay-insensitive communication systems are fully autonomous blocks, which can easily be reused in complex SoC architectures as soft, firm or hardware virtual components, hence decreasing design time and complexity.

Based on these motivations, this work contributes to two fundamental issues: arbitration algorithms are modeled using a high-level description language called CHP (Communicating Hardware Processes), and the delay-insensitive arbiter architectures are derived from these CHP specifications.

Three fixed priority arbiters were designed, daisy-chain, binary-tree and parallel-request-sampler as well as a dynamic priority arbiter based on the parallel-request-sampler algorithm.

This work demonstrates that it is today possible to cleanly and formally model and design delay-insensitive arbiter modules that are reliable, modular and fast. It also defines the fundamentals of an automated synthesis process devoted to arbiters. Finally, it constitutes an enabling factor for the asynchronous technology to be increasingly adopted in the design of SoCs.

Prospective works will be focused on the automation of the synthesis process within TAST, and the improvement of arbiter architecture and circuit performances. “n initiators to p receivers” fixed or dynamic priority routers will also be investigated to address the design of complex on-chip routing systems.

2.7 Lowering electromagnetic disturbances with asynchronous circuits

2.7.1 Asynchronization method

Asynchronization method was elaborated in order to exploit low EMI benefits of asynchronous circuits. It consists in obtaining asynchronous circuits from Register Transfer Level description of synchronous ones. This method suggests replacing identified synchronous structures (clock control) by equivalent asynchronous ones (handshake communications) inside the circuit. Cycle compatibility is respected in order to validate the circuit functionality.

This method was validated on a 4 coefficient Finite Impulse Filter reducing significantly the level of the spectrum.

2.7.2 A Current shaping methodology for lowering EM disturbances in asynchronous circuits

This work proposes a design methodology aiming at reducing peak-currents in asynchronous digital circuits. The method exploits the flexibility brought by handshake based communication mechanisms implemented in asynchronous circuits. It starts from a structural description of the circuit, which is then refined according to the communication protocol used, and annotated with operator latencies and current consumption. Force Directed Scheduling is then applied on the refined and annotated structural model of the circuit to determine the set of delays that have to be inserted in the handshaking protocols in order to minimize the peak-current without increasing the latency of the critical path.

It is important to mention that the method is general and can be applied to any asynchronous circuits, based on different protocols and different logic styles. Evaluated on a micropipeline asynchronous FIR filter, the method enabled a 20% reduction of the maximum peak-current (Figure 9).

Future work will be focused on including the method in the TAST framework and applying it to different asynchronous circuit styles in order to define which asynchronous circuit style is the best suited to low EMI circuit design.
2.7.3 Quasi Delay Insensitive Asynchronous Circuits for low EMI

This approach proposes a new design alternative for controlling/reducing electromagnetic emissions of integrated circuits. Our design approach is based on the exploitation of Quasi Delay Insensitive Asynchronous logic properties. In fact, by using a four-phase protocol combined with 1 to N encoded data, we demonstrate how QDI circuits can be used for tuning and lowering electromagnetic emissions. The investigation is based on the characterisation of two DES crypto-processors: an asynchronous and a synchronous version. The spectra of the measured currents show a significant reduction of the EMI of the asynchronous DES when compared to the synchronous one (Figure 10).

Figure 9. Current spectrum of synchronous FIR filter and asynchronous FIR filter

2.8 Analog-to-Digital Converters Based on Non-Uniform Sampling

This work is a contribution to a drastic change in standard signal processing chains: Analog-to-Digital Converters (ADCs), digital processing circuits, Digital-to-Analog Converters (DACs)... Integrated Smart Devices and Communicating Objects are the important applications targeted by this study. The main objective is to reduce their power consumption by one or two orders of magnitude, by completely rethinking their architectures and the associated signal processing theory.

Most of integrated systems bring signals with interesting statistical properties into operation, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, electro-cardiograms, speech signals...) are almost always constant and may vary significantly only during brief moments. Thus, classical regular sampling systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. The new idea of this work consists in realising an adaptive sampling scheme of the analog input...
signal based on its amplitude variations, and implementing an architecture only driven by the samples occurrences. The sampling scheme is based on “level-crossing” that provides a non equi-repartition of the samples in time. Quantization levels are regularly disposed along the amplitude range of the signal. A sample is taken only when the analog input signal crosses one of them (cf. Figure 11). Samples are not regularly spaced out in time, because it depends on the signal variations. This kind of sampling is the dual case of Nyquist sampling: the amplitude of samples is perfectly known but their time instants are quantized.

In this context, we propose a new class of ADCs, based on this non-uniform sampling and on an asynchronous hardware implementation (without any global clock). The term A-ADC for “Asynchronous ADC” is now used. Contrary to previous works carried out in other laboratories, not only does the term “asynchronous” define the design mode but also the sampling scheme. The architecture of the A-ADC is a tracking loop enslaved on the analog signal (cf. Figure 12). It is composed of a difference quantifier, an up/down counter, a Digital-to-Analog Converter (DAC), and a timer delivering the time intervals. No external signal as a clock is used to trigger the conversion. To preserve the same state of mind, an asynchronous structure is chosen for the circuit. The information transfer is locally managed with a bi-directional control signaling between senders and receivers (requests and acknowledgements).

The theory associated with the A-ADC is completely different from classical Nyquist ADCs. The Signal-to-Noise Ratio (SNR) only depends on the resolution of the local timer and not on the number of quantization levels. A very low hardware resolution can also be implemented insuring a high SNR i.e. a high Effective Number Of Bits (ENOB). The silicon area and the power consumption can thus greatly be reduced. We have elaborated a methodology to enable the designers to precisely calculate the design parameters of an A-ADC, given a target application. The input parameters are the analog signal characteristics and the desired ENOB, from which the four parameters characterizing an A-ADC are computed: the number of quantization levels, the loop delay, the timer period, and the number of bits for the timer. The following input signal characteristics must be perfectly known: Power Spectral Density, bandwidth, dynamic, and probability density. This method also determines the design constraints on the analog blocks of the loop.

We designed an A-ADC according to this theory, using the standard CMOS 0.12µm process from STMicroelectronics, for a speech application and an effective resolution of 10-bit. The converter has been implemented with a three stage micro-pipelined architecture, and a 4-phase handshake protocol. The photography of the die is given in Figure 13.

The maximum input frequency of the converter is: \( f_{\text{max}} = 160kHz \). This is much higher than the bandwidth of a speech signal, but this fact will not cause extra useless activity, nor extra power consumption for the converter. When the chip is running at its maximum speed, a power consumption lower than 180µW is measured. Lastly, the targeted resolution of 10-bit is reached for a frequency of the timer lower than 1MHz. The comparison of the A-ADC with standard Nyquist ADCs is done using the following Figure of Merit:

\[
\text{FoM} = \frac{2^{\text{ENOB}} \cdot 2 \cdot f_{\text{max}}}{P_m \cdot S},
\]

where \( P_m \) is the average dissipated power in Watts, \( f_{\text{max}} \) is the maximum frequency of the input signal in Hertz, and \( S \) the area of the core of the circuit in m². The FoMs of ADCs coming from recent publications have been computed or estimated. The best converters verify: \( \text{FoM} < 10^{19} \), and most of them: \( 10^{17} < \text{FoM} < 10^{18} \). Considering the characteristics of the A-ADC, the FoM of the A-ADC is: \( \text{FoM} = 2 \cdot 10^{19} \), that is twice higher than the best ADC.

These interesting performances have been achieved by reducing the activity of the converter thanks to the non-uniform sampling scheme and its asynchronous hardware implementation. These two aspects constitute very promising ways of investigation in order to significantly reduce the power consumption of complex
systems such as Communicating Objects or Smart Devices for Sensor Networks and/or ad-hoc networks applications.

2.9 Non uniformly sampled digital signal processing

According to the asynchronous digital signal processing chain defined in Section 2.2.8 and to the expected gain on power consumption, this work focuses on the signal theory of non-uniform sampling schemes and on possible implementations/architectures of such a non uniformly sampled signal processing.

It is well known that asynchronous designs exhibit interesting properties like low-power, low-voltage, low-EMI, etc. This kind of design has been used in a few publications to improve the performances of Nyquist ADCs such as: immunity to metastable behavior, reduction of the electromagnetic interference, speed, and power consumption savings. Moreover, most of the systems using ADCs imply signals with interesting statistical properties, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, pressure sensors, electro-cardiograms, speech signals...) are almost always constant and may vary significantly only during short moments. Thus, classical regular sampling and converting systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. It has been proved that ADCs using a non equi-repartition of the samples in time leads to interesting power savings compared to Nyquist ADCs. The new class of ADCs presented in Section 2.2.8 uses both the “level-crossing” sampling scheme and an asynchronous implementation of the circuit (no global clock).

This work follows this previous contribution, joining up the A-ADC to an asynchronous implementation of a circuit processing the non uniform samples (Figure 14).

Our new approach of signal processing is to combine asynchronous designs with signal event triggered processes in order to reduce dynamic activity. This work is dedicated to low-power applications especially in the area of Smart Devices and Communicating Objects.

Many studies deal with non uniform signal theory but are limited to mathematical aspects like recovery of additive-random or jittered sampling process. We decided to study the sampling scheme of the level-crossing sampling technique. Indeed, a sampled signal is obtained in the time domain by the multiplication between the analog signal and a function called “sampling function”. This implies in the frequency domain that the spectrum of the analog signal is convolved by the Fourier Transform of the sampling function: the sampling scheme. Usually in the uniform case, as the sampling function is a Dirac comb, the sampling scheme is also a Dirac comb. So the band base spectrum is duplicated around each multiple of the sampling frequency (the Shannon theorem is a consequence of the duplications). In the level-crossing non uniform case the sampling function depends on the signal. Thus the classical Discrete Fourier Transform (DFT) commonly employed for the spectral analysis of uniformly sampled signals is useless. In order to analyse the non-uniformly sampled
signal scheme a new spectral analysis technique is devised. The idea is to combine the features of both uniform and non-uniform signal processing chains in order to obtain a good spectrum quality with low computational complexity. The proposed technique shows significant improvements in terms of spectrum quality and computational complexity if we compare it to the General Discrete Fourier transform or the Lomb’s algorithm, which are used with some non-uniform sampling schemes. Moreover, a linear signal to Analog conversion can reconstruct the signal from its non-uniform samples according to the time interval values. This also allows spectral analysis by computing the Continuous Fourier Transform on the interpolated functions.

Among all the digital processes, Finite Impulse Response (FIR) filters have been chosen for their stability and convergence properties to illustrate this work. The convolution operator is formalized in the non-uniform sampling context in order to define an algorithm for the FIR filtering computation of non-uniformly sampled signals. An asynchronous iterative architecture is also proposed to implement the algorithm. It is formally proven that the computational complexity of the asynchronous FIR filter can be far lower than the computational complexity of the synchronous FIR filter, provided that the signal statistics are well exploited. It has demonstrated that the computational requirements, and hence the energy, can be reduced by more than one order of magnitude when compared to the standard uniform sampling scheme. This gain is due to the reduction of the number of samples processed. It should be noted that the gain could even be higher for other applications (medical, monitoring…).

A IIR filtering chain, which processes directly the non-uniform samples without resampling in a regular scheme, has also been studied. The non-uniformity in the sample times lead to choose a state representation for the filters. The stability of such systems is an issue and the performance of different numerical schemes (Euler, Bilinear, Runge-Kutta, …) used to implement the filters in this representation have been studied and compared in terms of stability, complexity and filtering quality when applied to classical filters as Butterworth, elliptic or Chebyshev filters. Euler schemes are to be rejected, the explicit one for being unstable and the implicit one for being in a sense too stable, i.e. too dissipative. The three other studied schemes (bilinear, RK23 and RK4) give qualitatively good results. If applied to N-order filters, only RK4 is effective (no matrix inversion), but if 1- and order decompositions are used, the complexity study does not allow to rank one of them clearly first. For RK23 and RK4, some oversampling is needed for inactive inputs to ensure stability, while this is unnecessary for the bilinear scheme.

Another developed approach is an efficient online processing technique for non-uniformly sampled signals which smartly combines the features of uniform and non-uniform signal processing. This has been applied to spectrum analysis and filtering. For filtering, the idea is to perform an adaptive rate sampling (relevant number of samples to process) along with an adaptive and optimal filter order (relevant number of operations per output sample) without an online filter calculation. This leads to minimize the computational load and enhance the power efficiency. Indeed the sampling is triggered when the input signal crosses one of the pre-specified threshold levels defined in the amplitude domain. As a result, the relevant and active signal parts are locally over-sampled in time. More the signal varies rapidly more it crosses the thresholds in a given time period. Contrary no sample is taken for the static signal parts. The approach is especially well-suited for the low activity sporadic signals. This smart sampling reduces the system activity and at the same time improves the accuracy of signal acquisition processes. In order to only process the active signal parts, an Activity Selection Algorithm (ASA) is used to window the relevant signal parts. ASA displays interesting features with AADC which are not available in the classical case. It correlates the length of selected window with the signal activity. In addition, it also provides an efficient reduction of the spectral leakage phenomenon in the case of transient signals. This is done by avoiding the signal truncation problem – which occurs in the classical case – with a simple and efficient algorithm instead of employing a smoothening window function. The selected data obtained at the output of the ASA can be used directly for further digital processing. However, in the studied cases, the non-uniform selected data are uniformly resampled. In these conditions, it is possible to apply a FFT or a classical filter to the selected data. For instance, in the filtering case, the data at the output of the ASA are decimated in order to once again reduce the processing activity. This leads to a drastic reduction of the processed sample number and to a significant decrease of the computational load.

To conclude, the digital signal processing chain using a level crossing sampling scheme behaves like the classical regularly sampled chain: an analog signal measured by a sensor can be sampled, processed and reconstructed in order to provide to an actuator a new analog signal. The difference between the standard technique and ours lies in the reduced number of samples taken for low-active signals. The level crossing scheme and the proposed signal processing theory implemented using asynchronous hardware lead to a significant reduction of power consumption making this technology very attractive for the low power SoC era.
### 2.10 Real-time dynamic voltage scheduling: embedded asynchronous systems outperform embedded synchronous systems

Power consumption is becoming a major issue for embedded system design such as cellular phones, personal digital assistants (PDA's) and “Internet appliances”. In these systems, there is a trend towards high performance computation and service integration which increases power demand. Reducing power consumption is required to keep autonomy and weight reasonable in these battery powered devices, to ensure reliability, and to reduce heat dissipation and system cost. A number of research efforts have recently investigated aspects of energy-efficient dynamic voltage scaling. This technique allows processors to dynamically change their voltage and speed at run-time under the control of voltage scheduling algorithms. However, there is no study that deals with asynchronous processors. This work introduces a new power reduction technique that combines an asynchronous processor and voltage scheduling algorithms. The asynchronous processor that we have designed is a CMOS standard-cell Quasi-Delay-Insensitive processor. It is ideal for embedded applications: it is low power and functional within a wide supply voltage range from 2.5 VDC down to 0.65 VDC. In cooperation with voltage scheduling algorithms that we developed, the operating system adjusts the performance level of the processor to the task requirements at run-time by controlling the processor operating voltage. This scheme exploits the ability of the asynchronous processor to self-regulate its processing speed with respect to the supply voltage.

Real-time embedded systems have often to manage periodic and sporadic tasks. While periodic tasks are commonly used to process sensor data and update the current state of the system, sporadic tasks are required to process asynchronous events. However, most of the voltage scheduling schemes presented in the literature considers systems with periodic tasks only. No attention has been dedicated to a system with sporadic tasks. We consequently consider in this work both periodic and sporadic tasks and propose 3 voltage scheduling algorithms. The first algorithm, Sporadic Tasks Voltage Scheduling, considers a case where only sporadic tasks arrive to the system. The second algorithm, Periodic Tasks Voltage Scheduling, assumes that all tasks are periodic. The last algorithm, Periodic and Sporadic Tasks Voltage Scheduling, deals with both periodic and sporadic tasks. This voltage scheduling is based on the two previous algorithms.

These algorithms determine the required processor speed to regulate the processor operating voltage and so the computational power at run-time. The processor speed is computed considering workload and task deadlines and updated whenever a task is added to or removed from the system. This ensures minimum energy consumption.

Simulation results, based on real measurements performed with an asynchronous processor mother board supplied with different voltages show that low power voltage scheduling – asynchronous processor combination reduces drastically power consumption in a real-time embedded system. Further, the inefficiency of dynamic voltage scaling in synchronous systems is pointed out. Since asynchronous processor can instantly be stopped and woken up without any time overhead and the computation can continue during the voltage switching, all tasks meet their deadlines. In synchronous systems this technique is less efficient. Because sporadic tasks have random arrival times, it is difficult to predict the future idle times. Furthermore shutting down, waking up and switching voltage and frequency of synchronous processors cause a time and energy overhead. Thus, tasks can miss their deadlines and voltage scheduling overhead is much higher.

### 2.11 Asyncronous clock generators for nanometric technologies

With the upcoming nanometric technologies, integrated system performances after fabrication will not be fully predictable. Indeed, the process variations really become huge at the chip scale. This implies to consider global management strategies in order to respect energetic and real-time constraints. Therefore performance estimation and management are today key points in new integrated systems. Solutions such as dynamic voltage and frequency scaling (DVFS) have to be considered, they have been explored and have shown to provide significant energy savings. The power reduction is a quadratic function of the voltage √d and a linear function of the clock frequency f. As a result, Dynamic Voltage Scaling (DVS) can be used to efficiently manage the SoC energy consumption. Supply voltage can be reduced whenever slack is available. This reduces the system speed which implies the use of Dynamic Frequency Scaling (DFS), to keep correct system behavior. The addition of DFS to DVS results in additional linear power savings. The application of DFS to a system requires the use of a source for generating adjustable clocks. For example these clocks can be derived from analog voltage controlled oscillators (VCO), which are a part of a phase locked loop (PLL). However, VCO have a limited operating range and a required stabilization time when changing the frequency. Another solution is to use a standard clock divider, but this will make the time resolution coarser, due to counting integer periods of the input frequency. In addition, they give regular time step which implies irregular frequency step (usually frequency step follows “1/X” curve).

Self-timed rings are considered promising solution for generating clocks. They can be efficiently used to generate high-resolution timing signals. They are robust against process variability in comparison to inverter
rings. Moreover, for a given number of stages self-timed rings can be reconfigured easily their initial state, while in the contrary, inverter-ring frequency is fixed. The group investigates the design of Programmable/Stoppable Oscillators which are based on self-timed ring to exploit their interesting characteristics. Through a handshaking protocol, the oscillator is communicating with the synchronous processor to insure a proper switching from one frequency to another. The oscillator is designed in order to avoid the presence of glitches and truncated clock periods.

Figure 15. Self-timed ring schematic

2.11 Asynchronous Programmable Logic

Introduction
The integrated systems today require flexibility, performance and reconfigurability. The trends in this domain lead to integrate on a single chip different processing cores, communication units and reconfigurable logic. Therefore the Systems on Chip (SoC) can embed programmable logic. In order to challenge the reconfigurability paradigm for special issues such as communication, synchronization or security, the asynchronous logic is a very promising approach. Nevertheless, the standard programmable logic blocks are not well-suited to map asynchronous circuits. The goal of this study is to define a more adequate programmable structure to implement asynchronous designs on SoCs embedding a reconfigurable part. This project aims the design of a Programmable Logic Device dedicated to the implementation of clockless circuits.

PLD Architecture
The group has investigated a novel Programmable Logic Device (PLD) architecture for implementing and prototyping various styles of clockless or asynchronous circuits. Many classes of asynchronous circuits exist, depending on the timing assumptions that are made at the logical level and the adopted handshake communication protocols. This work aims to break the dependency between the PLD architecture dedicated to asynchronous logic and the logic style. Indeed, the existing PLDs dedicated to asynchronous logic are always style-oriented. The proposed programmable structure is flexible enough to be used with different logic styles and asynchronous design flows.

Many asynchronous circuits are constructed with Muller gates. In order to support this specificity, a new Look-Up Table (LUT) architecture, which is well-adapted to the Muller gate implementation, has been designed.

This new LUT (Figure 16) allows the combination of a single memory-point with combinational logic. This programmable memory is realized thanks to an optional feedback structure. This architecture has been evaluated in CMOS, Pass-Transistor Logic and 3-state logic which is a non-conventional way to design LUTs. The simulations demonstrate that, at equivalent power consumption, a higher speed is observed for the 3-state logic.

This work is also associated to the TAST project in order to efficiently map and prototype multi-style logic asynchronous circuits.

An asynchronous e-fpga for security applications
With the growing need of applications such as homeland security or banking, the frequent updates in cryptographic standards and the high ASIC costs, the ciphering algorithms on an asynchronous
embedded FPGA co-processor are becoming a viable alternative. A novel asynchronous e-FPGA has been designed and fabricated.

Figure 17. The e-FPGA Layout

This architecture is natively robust against side channel attacks such as simple and differential power analysis or clock based fault attacks. Many countermeasures are already implemented in ASICs to prevent SPA, DPA, EMA and FAs. The approaches using QDI asynchronous circuits appear to be very promising and this work aims at transposing these methods in an e-FPGA context. The challenge is first to make the asynchronous FPGA natively robust against SPA and DPA while being very flexible. Afterwards, countermeasures against other SCAs and FAs can be easily explored and experimented. The e-FPGA is expected to provide the following advantages for security:

**Balanced power consumption** — QDI circuits which generally use 1-of-n encoding (for example: dual-rail, triple-rail, etc.) can be balanced to reduce the power consumption dependency with the processed data. Indeed, the bit encoding ensures that the data are transmitted and computations are performed with a constant Hamming weight. This is important since the leakage of the Hamming weight or distance can be exploited by SPA, DPA, and EMA.

**Absence of a global clock signal** — No clock means that FAs based on clock are removed. Moreover, DPA and SPA attacks without global clock signal are expected to be much more difficult. Indeed, the clock absence will make very complicated the synchronization of the DPA and SPA signatures.

**Environment variation tolerance** — QDI circuits adapt to their environment such as voltage and temperature variations, which means that they tolerate many forms of fault injection (power glitches, thermal gradients, etc). These QDI circuits can be easily combined with other countermeasure to efficiently counteract FAs.

**Redundant data encoding** — QDI circuits typically use a redundant encoding scheme (1-of-n). For example, the dual-rail encoding (a bit is encoded onto two wires) provides a mean to encode an alarm signal to counteract FAs.

To validate the e-FPGA native robustness against SPA and DPA attacks, an electrical simulation campaign has been carried out on a Programmable Logic Bloc (PLB) of the e-FPGA which is designed in CMOS 65 nm technology. Remind that, to be robust against SPA and DPA, the PLB should have the same current profiles and a constant running time whatever the manipulated data.

During the simulation, for a given secret key and the DES algorithm, random plaintext vectors have been processed.

Figure 18. Current profiles of the e-FPGA PLB
The corresponding current profiles are shown on the Figure above. Whatever the manipulated data are, the current profiles are very similar. In other words, the power consumption is data independent. Moreover, the observation of output variations shows that they are completely superposed. This means that the e-FPGA running time is data independent. This drastically increases the circuit robustness against SCAs exploiting the running time variations. In conclusion, with data independent power consumption and a constant running time, the proposed asynchronous e-FPGA architecture is natively robust against SPA, DPA and timing attacks.

2.12 Asynchronous assertion monitors
This work has been done in cooperation with the VDS group and deals with assertion based verification techniques. The idea is to generate asynchronous monitors from a normalized property description language such as PSL (Property Specification Language) or SVA (System Verilog Assertions). PSL is a standard formal language to specify logic and temporal properties in a declarative style, under the form of assertions. We defined a library of components, and an interconnection method to automatically synthesize hardware monitors that can be linked to a prototype of the design under verification, thus providing an efficient debugging platform. The existing tool produces asynchronous on-line checkers that are connected to the monitored design. The on-going work aims at snooping the design with monitors built from asynchronous modules. The monitors are thus reliable in the case of truly asynchronous events, and become applicable to a wider range of verification tasks, notably the communications among globally asynchronous modules.

Monitor synthesis principles
PSL distinguishes four satisfaction levels for a property: hold strongly, hold, pending, fail. Moreover, due to the composition of elementary properties to form complex ones, we have to face these two requirements:
- some sub-properties have significance only after some “starting” event has been observed (e.g. right hand-side of a temporal or logic implication)
- some sub-properties of an “always” invariant property may be “restarted” before the result of a previously started evaluation is known, and this restart should not abort the on-going evaluation.

The monitors we build reflect these requirements. When implemented in hardware, the monitor outputs display the property satisfaction level, and the indication that the answer is no longer pending may be used as an interrupt to trigger further actions. A monitor for a property P is built as a module that takes as inputs the reset, the synchronization signals (Start, Ack_out, Checking, Ack_in), a signal Start that triggers the evaluation, and the signals of the design under verification (DUV) that are operands of the temporal operators in P (see Figure above). The three monitor outputs have the following significance:
- Checking: a 1 indicates that output Valid is effective;
- Valid: provides the evaluation result;
- Pending: a 1 indicates that the monitor has been started and that the satisfaction result is pending; this is significant for strong operators.

The synthesis method relies on:
- A library of asynchronous primitive monitors, one for each PSL operator of the "foundation language". The asynchronous library elements are designed with a Quasi-Delay Insensitive (QDI) style. This class of asynchronous (or clockless) circuits has the advantages to be robust (due to the delay insensitivity), scalable and reusable. Moreover, this design style is compatible with the standard FPGAs and it allows the prototyping of asynchronous or mixed (sync./async.) circuits on clocked FPGAs.
- A systematic connection procedure to build complex monitors from primitive ones, based on the PSL expression syntax tree. The Figure above illustrates the construction of the monitor for property P defined as:
  Property P is always (A ->B before C);
These asynchronous monitors are well-suited to check properties in GALS communication systems and to online monitor critical safety systems.

2.13 Asynchronous Processors

2.13.1 ASPRO Microprocessor

(Collaboration with France Telecom R&D & STMicroelectronics)

We have designed a CMOS standard-cell Quasi-Delay-Insensitive (QDI) 16-bit asynchronous microprocessor using a 0.25 µm technology (see Figure 19). ASPRO-216 has been developed for embedded applications. It can be customized both at the hardware and software levels to fit specific application requirements. It is a scalar processor which issues instructions in-order and completes their execution out-of-order. Its architecture extensively uses an overlapping pipelined execution scheme involving de-synchronized units. ASPRO owns four bi-directional serial links with 50 Mb/s throughput, two 16-bit parallel ports, 16 Kwords program memories on chip, and 64 Kbytes data memories on chip. ASPRO operates with a power supply between 0.8V and 2.5V. The performance of ASPRO-216 is 140 Mips, 0.5 Watt, at 2.5 Volts and 24 Mips, 27 mW, at 1V (see Table 1 for a comparison with other asynchronous processors).

<table>
<thead>
<tr>
<th></th>
<th>mw</th>
<th>Mips</th>
<th>Supply (V)</th>
<th>mw/Mips</th>
<th>Techno.</th>
<th>Circuit style</th>
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<td>QDI, std-cell</td>
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</tr>
</tbody>
</table>

Table 1. ASPRO compared to other asynchronous processors

The design flow we set-up to design ASPRO is described in Figure 20. The specification language used is a CSP like language called CHP (from Caltech). The processor is first described by a high level sequential
CHP program which is automatically translated into VHDL and validated by simulation. This program is then refined by process decomposition and transformed to get a parallel structural version.

![Diagram of the flow used to design ASPRO](image)

**Figure 20. Synoptic of the flow used to design ASPRO**

The synthesis phase is constrained by cycle time and latency specifications. When every part of the processor is available at the gate level, an optimization of the whole architecture is performed to get maximum performance (pipeline balancing, slack matching) according to the pipeline depths and latencies of each block (see 2.2.1.d. for details on the design flows and associated tools).

Software development tools, C compiler, assembler, linker and simulator are available for the development of applications using the ASPRO processor. We have also developed a motherboard to demonstrate the capabilities of the microprocessor. The board includes an ASPRO, flash memories for the boot, reset / interrupt logic, four communication links and a parallel interface to connect peripheral boards. Three peripheral boards have been designed, one is based on LED and Switches (see Figure 21), another one includes an RF interface and the last one is a digital camera. Experiments performed with the mother board shows that the processor is running correctly down-to 0.65 volt (nominal supply voltage is 2.5 Volts).

![ASPRO motherboard and a peripheral daughter board](image)

**Figure 21. The ASPRO motherboard and a peripheral daughter board**

An example of a system built using the boards we have designed is presented in Figure 22. This is a multiprocessor system based on two ASPRO processors, a camera and an RF interface. The application consists in capturing an image, processing it and transmitting the result through the radiofrequency. This prototype enables us to carry on experimentation on multiprocessor systems, low power Operating System implementing a dynamic voltage scheduling strategy.
Figure 22. Multiprocessor system for image processing with wireless communication

2.13.2 **MICA micro-controller**
(Collaboration with France Telecom R&D & STMicroelectronics)

**Figure 23. The MICA micro-controller**

MICA is a QDI asynchronous 8-bit micro-controller CISC machine, based on a dedicated “luxurious” micro-architecture (see Figure 23). In order to facilitate the design of a “C” compiler and also to limit memory accesses, we decided to integrate two different register-files: eight 8-bit registers are devoted to data, and eight 16-bit registers are devoted to pointers (including the program counter and the stack pointer). Specific arithmetic units are associated with each register file enabling concurrent computations of data and addresses. A dedicated unit is managing the standard status bits Z, N, V and C. A peripheral unit is also included, supporting six 8-bit parallel ports (1 input, 4 outputs and 1 bi-directional used to control external flash memories and the synchronous/asynchronous interface) and four serial links (using a two-phase delay insensitive protocol compatible with our high performance RISC asynchronous ASPRO processor — described above -). Moreover, the micro-controller integrates 16 Kbytes RAM and 2 Kbytes ROM. The latter includes a **Built-In-Self-Test** which is executed at reset according to the boot mode selected (eight modes are available). It is a 350 assembly instruction routine which performs a complete stuck-at-fault test, thanks to the QDI asynchronous logic. The BIST routine computes a signature written on the fly, on one of the parallel port to report on self-test progress.

- **Instruction set**

The eight 8-bit data registers are named r0 to r7, and the eight 16-bit index registers i0 to i7, where i6 and i7 are the stack-pointer and the program-counter respectively. The controller implements the common arithmetic and logic instructions. All instructions are encoded within one word (16 bits). Four basic addressing modes are available (immediate, register, indexed with displacement, indexed post-incremented or pre-decremented) which can be used in conjunction with data or index register operands. Lastly, the controller implements a maskable interrupt mechanism and a “wait for interrupt” instruction (Wfi). **Table 2** summarizes the instruction set, note the “copy” (Cp) and the “Puch&Load” (Pl) instructions. A complete software development suite of tools is currently under development including a “C” compiler, an assembler, a linker and a simulator.
The micro-controller core is designed using the so-called Quasi Delay Insensitive (QDI) logic. A four-phase protocol is used in conjunction with an n-rail encoding. This chip has been a vector for developing new skills in the design of standard-cell based QDI asynchronous circuits. The design of MICA was focused on two correlated concerns: designing distributed asynchronous finite state machine and designing for low power.

In order to reduce the power consumption of the micro-controller we have worked on minimizing the number and the energy-cost of communication actions occurring during the execution of each instruction, and minimizing the number of sequential steps to perform each instruction. In other words, instead of designing the architecture around a big central sequencer, we have tried to distribute the sequencing implementation all over the architecture as much as possible. The asynchronous logic is particularly well suited to satisfy such a design approach since by nature the sequencing of an asynchronous circuit is performed by multiple local sequencers implementing handshaking communications and local treatments.

Thus, the architecture of MICA has been designed as a distributed system, each part providing specific services. For example, the two register-files, the status register and the memory integrate local units which manage the memory resources. These modules implement functions such as "read", "write", "read then write back" or even more complex function like : read a byte, increment/decrement the pointer/address and read the corresponding byte (Cp and Pl instructions for examples use these features). Adopting such an approach significantly simplifies the design of the main sequencer of a CISC microprocessor like MICA. It then minimizes the power consumed by the main sequencer, the consumption associated with each instruction being the direct image of its complexity. In fact, complex instruction implementation does not penalize simple instruction implementation at the main sequencer level. Moreover, such a distributed approach minimizes the power consumed by communications since the minimum number of transactions occurs through busses (memory accesses for example).

Because of the low-power constraint and because computational power was not a priority for the targeted applications, a minimum number of pipeline stage was introduced. This does not prevent parallel execution of instruction sub-parts, but simply means that parallel execution of instructions is not supported. In some cases however, subsequent instructions may partially overlap.

Finally, at the signal level, communication channels are using a low power data encoding. Instead of using dual-rail coding, we have implemented N-rail coding (also called "One Hot"), i.e. one out of the N wires is active during a transaction (instead of one out of two with dual-rail). The different parts of the architecture are all controlled by the main sequencer through channels using 5-rail to 1 rail data encoding which minimizes the number of transitions per communication action, and hence minimizes the dynamic power consumption. The data paths (8-bit and 16-bit) are entirely designed with 4-rail encoded data, requiring radix-4 logic/arithmetic processing units. The register files are also designed with 4-rail encoded data. Instead of bit-registers they are built of digit-registers, each digit representing 4 values.

<table>
<thead>
<tr>
<th>Arithmetic/logic</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add, Addc, Sub, Subb, Inc, Dec, Neg</td>
<td></td>
</tr>
<tr>
<td>And, Or, XOR, Not, Cbn (clear bit n), Sbn (set bit n), Tbn (test bit n)</td>
<td></td>
</tr>
<tr>
<td>Rol, Ron, Rcl, Rcr (rotate without and with carry)</td>
<td></td>
</tr>
<tr>
<td>Shl, Shr, Shsr (shift left, shift right unsigned and signed)</td>
<td></td>
</tr>
<tr>
<td>Index</td>
<td></td>
</tr>
<tr>
<td>Addx, Subx</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Load/Store</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ld, Ldp, Stp (load, store peripheral), St</td>
<td></td>
</tr>
<tr>
<td>Cp (copy from memory to memory is available)</td>
<td></td>
</tr>
<tr>
<td>Pl (push &amp; load)</td>
<td></td>
</tr>
<tr>
<td>Psh, Pshsr (push, push status register), Pop</td>
<td></td>
</tr>
<tr>
<td>Index</td>
<td></td>
</tr>
<tr>
<td>Pshx, Popx</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Control flow</th>
<th>Rti, Rts, Jmp, Jsar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bcc, Bsrcc (cc = a, eq, ne, cc, cs, l, le, lt, lte, g, ge, gt, gte, vc, vs)</td>
<td></td>
</tr>
</tbody>
</table>

| Misc | Nop, Wfi, Eint, Dint (enable and disable interrupt) |

Table 2. The MICA microprocessor Instruction set

- Architecture design

The micro-controller core is designed using the so-called Quasi Delay Insensitive (QDI) logic. A four-phase protocol is used in conjunction with an n-rail encoding. This chip has been a vector for developing new skills in the design of standard-cell based QDI asynchronous circuits. The design of MICA was focused on two correlated concerns: designing distributed asynchronous finite state machine and designing for low power.

In order to reduce the power consumption of the micro-controller we have worked on minimizing the number and the energy-cost of communication actions occurring during the execution of each instruction, and minimizing the number of sequential steps to perform each instruction. In other words, instead of designing the architecture around a big central sequencer, we have tried to distribute the sequencing implementation all over the architecture as much as possible. The asynchronous logic is particularly well suited to satisfy such a design approach since by nature the sequencing of an asynchronous circuit is performed by multiple local sequencers implementing handshaking communications and local treatments.

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Micro-controller performance

A test chip has been designed, fabricated and tested. The micro-controller has been easily tested thanks to the BIST, and was **fully functional at first silicon** between 3 Volts down to 0.8 Volt (2.5 Volts is the nominal voltage of the .25µm CMOS technology used). **Table 3** gives the Mips (mean number of instructions executed per second when running the BIST program), Power and Mips/watt figures at different voltages (based on the total current consumed by the core, the memory and the pads). It is noticeable that the chip only consumes 800 µW at 1 volt, still delivering a computational power of 4.3 MIPS. At 0.8 volt, the chip consumes less than 400 µW.

<table>
<thead>
<tr>
<th>Supply(V)</th>
<th>Mips</th>
<th>Current (mA)</th>
<th>Power(mW)</th>
<th>Mips/Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>4.3</td>
<td>0.8</td>
<td>0.8</td>
<td>5503.6</td>
</tr>
<tr>
<td>1.5</td>
<td>11.9</td>
<td>3.1</td>
<td>4.7</td>
<td>2560.2</td>
</tr>
<tr>
<td>2.0</td>
<td>18.6</td>
<td>6.7</td>
<td>13.3</td>
<td>1398.0</td>
</tr>
<tr>
<td>2.5</td>
<td>23.8</td>
<td>11.2</td>
<td>28.0</td>
<td>850.3</td>
</tr>
</tbody>
</table>

Table 3. MICA measured performances

We have developed a mother board to demonstrate the capabilities of the MICA microprocessor. The board includes a MICA processor, a flash memory for the boot (and also programmable), reset / interrupt logic, four communication links and a peripheral interface. The same peripheral board developed for the ASPRO processor can be used. This system enabled us to show that the processor is running correctly down-to 0.65 volt (see **Figure 24**).

![Figure 24. The MICA motherboard](image-url)
3. Reliable Mixed-signal Systems (RMS)

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L. Lizarraga*, S. Mohsen, N. Nguyen, L. Rufer, E. Simeu, H. Stratigopoulos,  
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*ST Microelectronics & TIMA, &TIMA & Université Européenne de Bretagne, *RMS and CIS Groups, €Ecole  
Ingénieurs Sfax (Tunisie).

<table>
<thead>
<tr>
<th>Research areas</th>
<th>Contracts</th>
<th>Industrial Partners</th>
</tr>
</thead>
<tbody>
<tr>
<td>Computer-Aided-Test (CAT) techniques for AMS/RF circuits</td>
<td>NANO TEST (MEDEA+, 2005-2008)</td>
<td>ST Microelectronics</td>
</tr>
<tr>
<td>Design-for-Test of AMS/RF/MEMS devices and systems</td>
<td>VIS-IMALOGIC (MINALOGIC, 2007-2009)</td>
<td>E2V</td>
</tr>
<tr>
<td>Design of AMS/RF/MEMS devices and systems</td>
<td>MARIE CURIE (CEC, 2007-2011)</td>
<td>NXP</td>
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<tr>
<td></td>
<td>Eurocopter (2007-2009)</td>
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<td></td>
<td>B-DREAMS (MEDEA+, 2008-2011)</td>
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<tr>
<td></td>
<td>CARNOT LSI (ANR, 2008)</td>
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<td></td>
<td>MORGAN (CEC, 2008-2011)</td>
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</table>

3.1 Computer-Aided-Test techniques for AMS/RF circuits

3.1.1 Density estimation for AMS/RF BIST evaluation

Members:  A. Bounceur*, S. Mir, H. Stratigopoulos, Y. Fellah  
(* TIMA & Université Européenne de Bretagne)

A major hurdle when dealing with mixed-signal/RF Built-In-Self-Test (BIST) techniques is the difficulty to  
evaluate them at the design stage. This evaluation is typically seen in terms of incurred costs, such as those  
due to the silicon overhead, the degradation of performances in the circuit under test, and the probabilities of  
test errors. These probabilities allow the definition of test metrics such as defect level (probability that a  
device that passes the test is defective) and yield loss (probability that a good device fails the test). A BIST  
circuitry with its associated test limits must be designed so that it results in a minimum additional parametric  
yield loss while detecting a maximum of bad devices. The direct calculation of parametric test metrics from  
Monte Carlo circuit simulations is misleading since there is insufficient data to represent properly faulty  
devices (or devices out of the specifications). In order to get a precision of parts-per-million (ppm), it is  
necessary to generate a population of at least one million devices from an initial small population. To this  
end, the focus in this task has been the development of an evaluation toolbox based on principles from  
statistical theory. In the past, we have considered the use of a multivariate Gaussian model and the use of  
non-parametric density estimation for estimating the joint probability density function (PDF) of the circuit  
performances and the test measures (see Figure 1).

![Figure 1. Statistical models for the estimation of parametric test metrics](image-url)
During 2008, we have investigated the use of Copulas theory as a means to generate the joint statistical model of the Circuit Under Test (CUT) performances and BIST measures. Once the model is estimated, it can be readily simulated to obtain the amount of test data necessary to achieve ppm accuracy. The basic idea is that, for any multivariate distribution function, the univariate marginals and their dependence structure can be separated, with the latter completely described by a unique Copula function. Thus, the problem boils down to the identification of the Copula function. Although this is a difficult problem to solve, an approximation can be made by choosing from existing Copula functions. The method was shown in the case of an RF Low Noise Amplifier (LNA) with a single BIST measurement. The BIST measurement is the RMS output of an integrated cell that computes the cross-correlation between the output of the LNA and the current drawn by its current supply. It is shown that a multivariate Gaussian Copula is a good choice for this case study. Once the Copula is calibrated, we can readily employ it to obtain as many samples as necessary from the original multivariate distribution function of the CUT and BIST. These samples correspond to synthetic instances which can be thereafter used for test metrics estimation. Figure 2(a) shows instances generated by circuit simulation and by Copulas generation. As can be observed, the two distributions match very well illustrating that computational intensive circuit simulation can be substituted with the much faster model based on Copulas. One can use this model to generate one million instances so as to compute parametric yield loss and defect level with ppm accuracy, given the limits of the BIST measurement (Figure 2(b)). Furthermore, the test limits can be optimized to achieve a desired trade-off between test metrics.

Figure 2. (a) Application of the Copulas model to a case-study LNA with a BIST technique, and (b) setting of test limits as a trade-off between parametric defect level and yield loss

A Computer-Aided-Test (CAT) tool has been developed for automating the statistical modeling task using Copulas. Figure 3 illustrates the graphical interface of this tool that has been integrated in the CATLAB toolbox of the mixed-signal CAT platform developed in the Group (see Section 3.1.5). Panel one in Figure 3 allows the definition of statistical parameters for the marginal laws and the Copula of the multivariate PDF. Panel two is used for sampling the model and for the generation of over 1 million new instances. Finally, panel 3 is used for the estimation of the parametric test metrics.
3.1.2 Machine-learning-based test techniques

Members: H. Stratigopoulos, S. Mir, Y. Makris*  
(*Yale University, USA)

The machine-learning-based test technique employs a low-cost test configuration to extract a test measurement pattern and subsequently maps this pattern to one of three possible classifications: the device is good, the device is faulty or a test decision is prone to error. The mapping is established by a classifier which consists of a committee of two neural networks. In a training phase, the classifier learns to allocate guard-bands in the test measurement space, as shown in the left-hand part of Figure 4 and in Figure 5. The good (faulty) guard-band “guards” the good (faulty) population, i.e. it has all good (faulty) training devices on one side. In essence, the guard-bands create a trichotomy in the alternate measurement space: two regions outside the guard-banded zone that are dominated by either good or faulty training devices and the guard-banded zone which contains a mixed population. If a new device out of production falls outside the zone, then it is assigned to the dominant class, otherwise, if it falls within the zone, it is considered to have ambivalent status (N_r % of all devices) and, thus, it is forwarded to standard specification-based testing, in order to reach a final accurate decision.

Predicting the label of new devices through the guard-bands entails two types of errors: the pattern of a faulty device might be interwoven in the “good” region giving rise to test escapes (T_E), or the pattern of a good device might be interwoven in the “faulty” region giving rise to yield loss (Y_L). It is evident that the wider the guard-banded zone is, i.e. the more the guard-bands are pushed away of each other into the “clean” regions, the less the test error and, of course, the larger the percentage N_r of retested devices. The trade-off can be explored by two parameters, namely $\lambda_g$ and $\lambda_f$, which define the position of the good and faulty guard-band, respectively. When both are zero, the two guard-bands collapse to a single classification boundary (i.e. N_r=0). When $\lambda_g$ ($\lambda_f$) increases, then the good (faulty) guard-band is pushed into the “faulty” (“good”) region, thus widening the guard-banded zone and decreasing Y_L (T_E).
The test accuracy heavily depends on the information that is available during the training phase. The training set should include a balanced population between faulty and good devices such that one population does not overshadow the other. Second, the training devices must be representative of the manufacturing process such that they “fill up” the test measurement space. Most importantly, the training set must contain “critical” devices that are marginally-in-the-specification and marginally-out-of-the-specification bounds such that the true separation boundaries are approximated. The problem lies in that such training sets with numerous faulty and “critical” devices are not readily available during the test development phase since brute-force Monte Carlo analysis samples only the statistically likely cases.

To this end, we have developed a method based on non-parametric density estimation to generate synthetic data that respect the distribution of experimental data. The resulting enhanced data set contains all the relevant information needed for training and, in addition, its volume can be arbitrarily large, allowing us to express the test error in ppm accuracy. The method has been demonstrated on an UHF receiver front-end. The chosen single low-cost test configuration, shown in Figure 6, relies on the modulation-demodulation principle. $N_t - T_E$ curves for approximately constant $Y_L$ are shown in Figure 7. One can identify interesting trade-off points, for example $T_E = 110$ppm and $Y_L = 0$ppm if we choose to retest $N_r = 3.4\%$ of the devices. This results in an overall test cost reduction of 64% without sacrificing test accuracy.
3.1.3 Parameter identification for test and control of AMS/RF circuits

Members: R. Khereddine, E. Simeu, S. Mir

AMS and RF circuits are required in many different applications (i.e. network sensors, multimedia, telecommunications, etc.). In SoC/SiP devices, AMS and RF components coexist with digital ones like microprocessors, and memories. These embedded resources can be used to test or control the system. In the case of an RF transceiver, the embedded microprocessor in the digital part can be used to generate the test stimuli for the RF front-end and to treat a low frequency signal response of the system. This signal can be extracted from different points situated in the high frequency part using embedded sensors (i.e. envelope detector, peak detector, etc.) as shown in Figure 8.

Figure 8. Embedded sensors for transceiver test

Our approach for test and control of AMS/RF blocks consists of building a complete behavioural input/output model of the system under test using a generic modelling approach applicable for very large classes of both linear and nonlinear input/output behaviours and obtain the structure and the different parameters of the model. Next, a subset of parameters which are best correlated with our objectives is easily estimated and used in the test and/or control process. Other parameters and the structure of the model are inherited from the nominal model.

The Situation-Dependent Auto Regressive with eXogenous variable (SDARX) model is a multivariate nonlinear function used to represent a large number of behaviours. This model is expressed as:

\[ y(t) = \varphi_0 (\gamma(t)) + \sum_{i=1}^{n_u} \varphi^y_i (\gamma(t)) y(t-i) + \sum_{i=1}^{n_y} \varphi^u_i (\gamma(t)) u(t-i) + v(t) \]

where: \( \gamma(t) = [y(t-1), y(t-2), ..., y(t-n_y), u(t), ..., u(t-n_u+1)]^T \). The basic idea of the SDARX model is to achieve the local linearization of the general NARX model by introducing a locally linear ARX model with situation-dependent coefficients \( \varphi^y_i (\gamma(t)) \) given by:

\[ \varphi_0 (\gamma(t)) = c_0^0 + \sum_{k=1}^{m_0} c_k^0 e^{-\rho_k^0} \left| (t)-Z_k^0 \right|^2 \]

\[ \varphi^y_i (\gamma(t)) = c_{i,0}^y + \sum_{k=1}^{m} c_{i,k}^y e^{-\rho_k^y} \left| (t)-Z_k^y \right|^2 \]

\[ \varphi^u_i (\gamma(t)) = c_{i,0}^u + \sum_{k=1}^{m} c_{i,k}^u e^{-\rho_k^u} \left| (t)-Z_k^u \right|^2 \]

The parameter estimation strategy consist of a combination of two parameter estimation methods. The linear parameters \( \{c_{i,k}^y/k=1,..,m_i;i=1,..,n_u/ny;d=0,u,y\} \) are calculated with the Least Mean Squares method and the nonlinear parameters \( \{\rho_k^d,Z_k^d/k=1,..,m_d;d=u,y\} \) are estimated with a descent method (Levenberg-Marquardt).

The identification strategy for test purposes contains two phases. In the design phase we find the nominal model of the system, and we fix the structure and some parameters of the nominal model. Then we select the best correlated linear parameter subset (\( \Theta_{test} \)) with our objectives. Using Monte Carlo simulation we build a regression equation or a classifier to be used for test decision. In the application phase we use recursive least squares algorithm to estimate \( \Theta_{test} \), and we decide if the circuit is good or faulty.

As an example case-study, we have considered an RF LNA. This device implements a nonlinear function of a third degree given by: \( y(t)=a_0 + a_1 u(t)+a_2 u(t)^2+a_3 u(t)^3 \). In this simple case, LNA performances are directly
calculated from the model parameters as: \( \text{Gain} = a_1, \text{IP2} = a_1/a_2, \text{IP3} = (4a_1/3a_3)^{1/2}. \) Figure 9 illustrates the accuracy of performance estimation for the LNA.

Figure 9. LNA performance estimation

3.1.4 Analogue functional test compaction using density estimation

Members: N. Akkouche, S. Mir, E. Simeu, H. Stratigopoulos

The RF functions in a complex System-on-Chip are characterized by a large number of performances. Testing all performances results in lengthy test times and requires expensive test instrumentation. Our aim in this work is to identify and test the most relevant subset of performances, while making sure that the defect level (proportion of faulty devices that pass the test) remains below a certain threshold. For example, Figure 10 illustrates a case-study LNA design for which our intention is to rank its performances according to the impact on parametric defect level.

To achieve this, we estimate the joint probability density function (PDF) of performances using non-parametric kernel density estimation. The estimated PDF is sampled thereafter to rapidly generate data corresponding to one million devices. This allows us to estimate defect level with ppm accuracy. We have implemented three different feature selection algorithms to search in the power-set of performances, namely branch and bound, floating search, and a genetic algorithm. The branch and bound algorithm results in the optimal order of elimination. However, it is exhaustive and can be applied only in the case when the dimensionality is low. The other algorithms perform a much faster search but the result is, in general, suboptimal. For our case study in Figure 10, all algorithms resulted in the same order of elimination, as shown in Figure 11.

Figure 10. LNA schematic and list of performances with corresponding specification limits

<table>
<thead>
<tr>
<th>NF</th>
<th>( S_{11} )</th>
<th>Gain</th>
<th>1-dB CP</th>
<th>IP3</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \leq 1.3 \text{ dB} )</td>
<td>( \leq -9 \text{ dB} )</td>
<td>( \geq 17 \text{ dB} )</td>
<td>( \geq -11.3 \text{ dBm} )</td>
<td>( \geq -5.1 \text{ dBm} )</td>
</tr>
</tbody>
</table>
3.1.5 Test generation for AMS circuits

Members: S. Mohsen, A. Bounceur, S. Mir

A Computer-Aided-Test (CAT) platform has been integrated in the Cadence Design Framework Environment for the evaluation of AMS/RF test techniques. It comprises tools for statistical modelling of circuit performances and test measures, fault simulation, test generation and test optimization. Figure 12(a) illustrates a simplified architecture of the platform. The platform is constantly updated with refinements and new algorithms that are gaining increasing acceptance in our community.

Work in this activity has targeted the improvement of an analogue test pattern generation tool. This tool which is included in the OPTEGEN toolbox allows the generation of multifrequency test vectors for maximum coverage and diagnosis of structural faults in AMS/RF circuits. This tool has been improved in order to consider process deviations in the definition of the fault-free and faulty behaviours. Frequency regions for the detection of a fault can thus consider parametric tolerances. For example, Figure 12(b) shows two regions of detection of a fault: a first region between 1 and 1.4 GHz and a second region between 1.9 and 2.1 GHz. The tolerance band of good behaviour is comprised between the curves (c) and (d). The tolerance band under the presence of a certain fault is comprised between the curves (a) and (b). The CAT platform is able to automatically inject a set of pre-defined faults, to determine the regions of detection of each fault in the frequency spectrum considering process deviations, and to generate an optimized multifrequency test stimulus with maximum fault coverage and diagnosis.
3.2 Design-for-test of AMS/RF/MEMS devices and systems

3.2.1 Self-calibrating ΣΔ modulator using a BIST technique

Members: M. Dubois, N. Chouba*, M. Ben Mbarka*, S. Mir
(* ST Microelectronics)

With the continuous shrinking of transistor size for ever more complex SoC devices, testing costs of mixed-signal parts increase while their yields decrease. With the use of an embedded built-in-self-test (BIST) solution, test cost reduction is obtained by avoiding the use of expensive mixed-signal testers while yield improvement is made possible by using a self-calibration function. We have demonstrated this technique for a case-study stereo sigma-delta converter. The application of this work may be especially interesting for the self-calibration of nanometric converters.

The BIST technique aims at the measurement of the Signal-to-Noise and Distortion Ratio (SNDR) of the converter. In a calibration phase, five external biasing voltages that define the circuit operating point are swept consecutively with digitally programmable potentiometers for finding the best value of the SNDR.

A hardware prototype to demonstrate this technique is shown in Figure 13(a). An FPGA is used for implementing the calibration algorithm, the digital filter of the converter and the protocol required for programming the digital potentiometers. A graphical interface shown in Figure 13(b) has been developed in C++ language. The user can use this software to program the biasing voltages manually using cursors before running a test sequence. Moreover, three different calibration modes were programmed: software calibration (SNDR computation and calibration algorithm made by the software), BIST calibration (computation of the SNDR using the implemented algorithm) and on-chip calibration (all functionalities of the FPGA used).

Figure 13(c) shows the SNDR measured in the calibration phase as a function of the common voltage of the output amplifier. The best value obtained for Vcm=2.165V is recorded and then a second calibration phase was done moving simultaneously 2 different voltages (Figure 13(d)). As expected once the optimal working point is reached by changing an important parameter, the modulator is stable even if we vary the other voltages in a large range. The uncertainty of the measurement (around 2dB) is mainly due to the noise.
contributed by the use of external circuits. The absolute value of the SNDR obtained is well under the theoretical value but this noise problem would not occur if the complete calibration system was on chip.

### 3.2.2 CMOS imager BIST

*Members: L. Lizarraga*, S. Mir, G. Sicard†, H. Stratigopoulos
(* RMS and CIS Groups, †CIS Group)*

In this work we have evaluated a BIST technique for the pixel matrix of a CMOS imager. The BIST technique is based on applying electrical stimuli to avoid some optical tests that are performed when testing such devices. Standard and logarithmic pixel structures have been used to evaluate the BIST technique by simulation. The BIST technique has also been evaluated experimentally for a logarithmic pixel matrix fabricated in an AMS 0.35µm CMOS technology.

**Figure 14** shows the logarithmic pixel structure and **Figure 15** shows the test sequence applied to the pixel. First, an electrical pulse is applied to the calibration transistor PR in order to apply a reference voltage to the node Vph. Then an electrical pulse is applied to the photodiode anode. This originates an increase on the Vph voltage as it can be observed from **Figure 15**. Two test measures are taken from the test sequence: VA and VB. Since the pixel performances and the test measurements are dependent on the pixel structure (i.e. technological parameters, electrical faults, etc) a significant correlation exists between pixel performances and pixel test measures.

**Figure 14. Logarithmic pixel architecture**

**Figure 15. BIST test sequence**

The experimental results have been obtained on a 128 x 128 logarithmic pixel matrix. **Figure 16** shows the test environment. It is mainly composed by an analogue card, a digital card and a visual interface (PC). The analogue card contains the CMOS imager and converts the analogue signals into digital values through an ADC. The analogue card communicates with the digital card which contains an FPGA where a mini-MIPS has been implemented. The digital card gives the row and column addresses to the pixel matrix and it communicates with the PC. The visual interface allows to visualise the image and to obtain each pixel value in a hexadecimal mode in an excel file. From this file we can calculate the performances and obtain the test measures.

The total number of pixels measured experimentally is 16384 (i.e. 128 x 128 pixels). To calculate the test metrics with ppm precision, we fit a nonparametric statistical model on the 16384 pixels sample. Next, the statistical model is sampled in order to generate 1 million pixels. Test metrics such as pixel false acceptance (FA) and pixel false rejection (FR) are calculated for the sample obtained experimentally and for the sample obtained by simulation. Specifications limits are set at 5σ. The test measurement limits are set for the case FA=FR which results in the limits being placed at 4.4 σ. **Table 1** shows the test metrics. No faulty pixels are found from the population that has been generated by sampling the estimated density of the experimental

<table>
<thead>
<tr>
<th>Metric</th>
<th>Experimental data</th>
<th>Simulation data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yield</td>
<td>1 million</td>
<td>999941</td>
</tr>
<tr>
<td># defective pixels</td>
<td>0</td>
<td>59</td>
</tr>
<tr>
<td>Test yield</td>
<td>1 million</td>
<td>999945</td>
</tr>
<tr>
<td>FA</td>
<td>0</td>
<td>55</td>
</tr>
<tr>
<td>FR</td>
<td>0</td>
<td>59</td>
</tr>
</tbody>
</table>

**Table 1. Parametric test metrics**
data. On the other hand, 59 faulty pixels are found when the simulation data is used. This difference may be explained by the imprecision of the statistical model of the design kit parameters or noise during experimental measurements.

3.2.3 LNA DFT

Members: J. Tongbong, L. Abdallah, S. Mir, H. Stratigopoulos

This work addresses the development of design-for-test (DFT) techniques for LNAs aiming at reducing production test costs (i.e., tester instrumentation and test time) without sacrificing test quality. The proposed DFT technique is based on the use of embedded detectors as shown in Figure 17(a). Our case study is an 1.9 GHz LNA, shown in Figure 10, which has been designed using a ST Microelectronics 0.25µm BiCMOS technology.

Initially, we have performed a statistical evaluation of parametric test metrics for a range of different test measures, such as current consumption, output power, etc. Fault simulation has also been performed for single catastrophic and parametric faults in order to evaluate the different test measures. This initial analysis allowed us to focus on a DFT technique using two sensors: a Built-in Current Sensor and an Envelope detector. The outputs of both sensors are DC signals that can be easily measured on-chip and they are highly correlated with circuit performances that are not measurable on-chip.

For the current sensor, a 10Ω resistor is placed between the power supply and the circuit under test. This induces a voltage drop that is converted and amplified through a differential Operational Transconductance Amplifier (OTA). This current sensor has a [1mA-8mA] dynamic range, with a linear gain of 270mV/mA and 2mW power consumption. The RF envelope detector designed is shown in Figure 17(b). It is made of three stages. First, a single transistor voltage-to-current converter is used. Transistors P1 and P2 are amplifying the signal while current mirrors M3-M6 assume a subtractor function reducing the DC current flowing through the capacitor C1. Next, a half-wave class AB rectifier is followed by a low pass filter at the output stage. The envelope detector main characteristics are a [20mV-150mV] peak voltage dynamic range, a voltage gain of 17 dB and 6mW power consumption.

Figure 17(c) shows a figure of the layout of the LNA with embedded sensors. A prototype chip has been sent for fabrication. The evaluation of the BIST technique at the design stage using post-extract simulations and the experimental tests are currently underway.
3.2.4 DFT for RF MEMS switches

Members: H.N. Nguyen, R. Khereddine, E. Simeu, S. Mir, L. Rufer, P. Cauvet*
(*NXP Caen, France)

This work aims at finding a fast and low-cost test technique for RF MEMS switches embedded in SiP (System-in-Package). The complexity of RF SiP requires a test strategy leading to a design-for-test (DFT) solution that helps to overcome the necessity of sophisticated test equipment, as well as the access difficulties to measure embedded points. The proposed approach uses the principle of alternate test that replaces conventional specification-based testing procedures. The basic idea is to extract the high frequency characteristics of the switch from the signal envelope of the response. Features such as rise-time, fall-time, actuation voltage and on/off capacitance ratio can be extracted from this low frequency signal. These features are then used in a regression process to predict RF conventional specifications like S-parameters.

A test set-up was configured and used to evaluate some samples of a commercial switch. Experimental measures are executed with an industry-developed evaluation board and a developer’s kit. The commercial Teravicta RF MEMS switch (model TT712) and its evaluation board are shown in Figure 18(a). Low frequency measures like ON and OFF transition times and the ratio between peak amplitude of RF input and output signals are used as regressors. These low frequency characteristics shown in Figure 18(b) provide important data for the multivariate regression algorithm that builds a nonlinear mapping between the low frequency switch features and the RF performances. Thus, conventional performances, such as S-parameters, are predicted from these measurements by the nonlinear regression. The results exhibited a good correlation between low frequency and RF measurements. The experimental validation has only been performed for a reduced population sample (Figure 18(c)). Simulation results have also been used to evaluate this correlation (Figure 18(d)).

![Figure 18](image_url)

**Figure 18.** (a) Commercial RF MEMS switch and test kit, (b) measured actuation control signal (green line) and extracted rise-time, fall-time (blue line), (c) predicted vs. measured insertion loss ($S_{21\text{ON}}$), and (d) predicted vs. simulated isolation ($S_{21\text{OFF}}$)
### 3.2.5 PLL BIST

Members: A. Asquini#, F. Badets*, S. Mir, J.L. Carbonero*,
(“ST Microelectronics & TIMA, *ST Microelectronics)

RF PLL specifications are critical, mostly when they are embedded in high speed digital communication systems. Often, reduced test resources (time, cost, and speed) limit the number of performances that are actually tested in production. In this work, we are studying a BIST solution based on taking low-cost on-chip measures that are highly correlated with circuit performances that are not measurable on-chip. Sensors are embedded in relevant points of the RF PLL. They provide test measures aimed at replacing traditional performance measurements, since most of these can no longer be carried out either with dedicated RF testers and/or on-chip for the new devices operating at ever increasing speed. The BIST technique proposed is made up of three sensors, two of which are applied to the Voltage Controlled Oscillator (VCO) and one to the Phase Frequency Detector (PFD) output (based on the Veriner-Delay-Lines principle), as shown in Figure 19.

![PLL with embedded BIST monitors](image)

Figure 19. PLL with embedded BIST monitors

All sensors have been designed and simulated. The final layout has been carried out for some sensors. Parametric test metrics for individual components such as the VCO and the charge pump have been calculated using a statistical model. Two of the sensors test limits have been set as for the required specifications. For the third sensor (RF power sensor) test limits have been placed using the statistical model as shown in Figure 20(a). Next, single catastrophic faults have been simulated and fault coverage figures are obtained as a function of tests limits as shown in Figure 20(b). At 4.1σ almost all faults that are not detected by performances are not detected by the test measures either. Setting defect level equal to yield loss (blue line in Figure 20(a)), the statistical model gives a value of 9 ppm. This sets the limit for test measures at x = 4.4 approximately, which results in a catastrophic fault coverage (CFC) of 67.6%. Considering as acceptable to have a parametric yield loss ten times larger than defect level (red line in Figure 20(a)), the statistical model gives a defect level of approximately 9 ppm, yield loss of 85 ppm, and CFC always of 67.6% with the test measures limits set at x = 3.9. In this specific case, the rule of ten is not worth while using since it only adds yield loss without improving either fault coverage or defect level. In generic cases, choice of test limits has to be made according to product and customer requirements on test metrics.

![Figure 20](image)

Figure 20. VCO results: a) setting of test limits for the RF power sensor based on parametric test metrics, and (b) catastrophic fault coverage as a function of test limits of this sensor
3.3 Design of AMS/RF/MEMS devices and systems

3.3.1 Acoustic sensor for ORL surgery

Members: Y. Arthaud, L. Rufer, S. Mir, S. Schmerber*, N. Noury**
(*CHU Grenoble, **TIMC Grenoble)

In this project we aim at the development of a micromachined tactile vibration sensor working in the audible frequency range from 1 to 5 kHz to be used during an ORL (Oto-Rhino-Laryngology) surgery. The sensor will give the surgeon feedback concerning consequences of his intervention on the middle ear’s acoustic transmission properties by measuring the ear ossicles amplitude of vibration. Since vibration amplitudes and forces exerted by ossicles are very low (from 100 to 10 nm), high sensitivity and low mechanical impedance are required for the device. The device will be held by hand to allow precise and easy positioning on the small ossicles (millimeter scale). A mechanical filtering system eliminating the low frequency component of the vibration spectrum will avoid device saturation under the high magnitude hand's shaking movements (~100µm). The use of such a device could be extended to all type of hand-held vibration measuring tool where a low mechanical impedance and high sensitivity is required.

A MEMS based vibration sensor is convenient for the task especially due to the small size of the ear ossicles. The sensor is composed of a pillar with a tip that is placed in contact with the vibrating ossicle to transmit vibrations to a suspended base composed of four “arms”. Arm deformation will be converted into electrical signal by means of piezoresistive gauges (Figure 21(a)) providing information on the pillar tip vibration magnitude. Silicon is too stiff and brittle to satisfy low displacement and low impedance requirements and to withstand hand's movements. Polymer materials which became widely used in MEMS field, present good mechanical properties and its electrical behavior can be tuned by adding various types of particles like metals particles or carbon nanotubes.

For example, SU-8 negative resins presents good mechanical properties (high flexibility and fracture strains), and allows precise and easy patterning which can be useful for the sensor base fabrication. Realization of test structures has been done and characterization is in progress.

An analytical modeling demonstrate the ability of beams constituted of elastomer materials (such as polyurethane (PU), and polydimethylsiloxane (PDMS)) to absorb low frequency stimulations (Figure 21(b)). We aim at realizing such pillars by a molding technique. The mold has been done and in the near future the realization and measurement stages should confirm the modeling result presented below.

An in progress bibliographic study has allowed us to establish the promising potential of nano-composites as electrically strain sensitive materials. These materials consist in carbon nanotubes soaked in a polymer matrix providing to it good piezoresistive properties as well as keeping polymer flexibility. A potential supplier for strain sensitive materials has been identified and we are currently working on gathering data that are necessary for the design of the nano-composites based piezoresistive gauges.

![Figure 21. Schematic view of the sensor structure (a), transmission properties of a viscoelastic beam (material properties based on Soundcoat Dyad601 PU) (b)](image-url)
3.3.2 High frequency aeroacoustic sensor

* Hong Kong University of Science and Technology, ** Ecole Centrale de Lyon

Microphone is a sensor for measuring acoustic pressure variation. Most of them are developed for audio applications with the frequency ranges from 20 Hz to 20 kHz and the pressure level ranges from 20 µPa to 60 Pa. These specifications are inadequate for aero-acoustic applications that require bandwidths from hundreds of kHz to a few MHz and pressure levels from 10 Pa to 1 kPa, such as a model-based characterization of the “N-waves” generated during supersonic flights. Piezoresistive microphones are uniquely suited for such relatively wide bandwidth and high pressure levels.

Due to the difficulty in forming single-crystal silicon (sc-Si) on amorphous dielectric thin films, polycrystalline Si (poly-Si) piezoresistors on Si nitride (SiN) membranes were used in early demonstrations of aero-acoustic microphones. Technologies for replacing such low gauge-factor poly-Si with sc-Si have been proposed, based on the bonding and etch-back of Si-on-oxide or bulk wafers. These technologies are relatively complicated and time-consuming or the doping concentration is not optimized for the piezoresistors.

An aero-acoustic microphone technology based on layer-transferred sc-Si on SiN is presently demonstrated. A 1 µm thick low-pressure chemical vapor deposited (LPCVD) SiN layer is formed on a p-type handle wafer with patterned sacrificial islands. A separate donor wafer is implanted with hydrogen. The two wafers are subsequently bonded at 300°C in air. Exfoliation at the peak of the hydrogen implant profile and layer-transfer of lightly doped sc-Si from the donor to the handle wafer is accomplished with a heat-treatment at 550°C for 30 mins. The transferred Si is thinned by thermal oxidation and implanted with boron to obtain the optimal gauge factor. It is patterned to form the piezoresistors. A second layer of LPCVD SiN is formed, patterned and etched to form the contact holes. Si exposed in the contact holes is heavily doped to reduce the contact resistance. The piezoresistors are connected to form a Wheatstone bridge. The metallic interconnects are resistant to extended 85°C aqueous potassium hydrogen (KOH) based Si etch. Finally, the microphone cavity is formed and the sensing membrane is released in KOH. Shown in Figure 22(a) is a photograph of a finished microphone. The cavity depth is 140µm.

Compared with earlier aero-acoustic microphone technologies, the advantages of the presently proposed technology are: 1) replacement of poly-Si with higher gauge-factor sc-Si; 2) fabrication of sc-Si piezoresistors with optimal doping concentration; 3) uniform layer-transfer versus time-consuming full-wafer etch-back; 4) reduction of device size and better control of diaphragm dimension due to the front-side cavity etch for diaphragm release.

An optical vibrometer is used to measure frequencies and shapes of vibration modes. The shape of the fundamental mode at 520 kHz is shown in Figure 22(b).

![Figure 22. Planview photograph of the microphone (a), Measured first vibration mode of the microphone membrane (b)](image)
3.3.3 CMOS integrated micromachined inductive microphone

Members: F. Tounsi*, L. Rufer, M. Masmoudi**, B. Mezghani**, S. Mir
(*ENIS & TIMA, **ENIS, Sfax, Tunisia)

MEMS-based products utilize robust processes from the IC’s industry to make a wide variety of electronic devices smaller, more reliable and cheaper to manufacture. During the past decade, silicon micromachining techniques have been successfully applied to the fabrication of miniature microphones on silicon wafer. Silicon microphones based on different principles, e.g. piezoelectric, piezoresistive, and capacitive have been investigated. Most of the silicon microphones presented in the literature are based on the capacitive principle because of the high sensitivity, flat frequency response, and low noise level. However, capacitive microphones present some potential issues such as electrostatic pull-in instability and output signal attenuation due to the parasitic capacitance. In addition they require deposition, etching and/or bonding processes, which are not directly compatible with integrated circuit (IC) technology. Furthermore, only few integrated microphones have been suggested, which were made by merging micromachining and IC processing. But they still use a specific material and fabrication technology. This will limit the affordability of these types of microphones and make them more expensive.

In this project we are studying a more flexible approach in which the microphone can be produced. An inductive micromachined microphone, shown in Figure 23(a), has been designed. A standard CMOS 0.6µm micromachining process enables its monolithic integration with the electronics. The inductive microphone consists of an internal inductor L2 fabricated on top of a flexible suspended thin plate, over a cavity, and a fixed external inductor L1 on the top of the substrate. Depending on sensitivity requirements, either or both inductors may be driven with either a DC or AC signal. The induced signal on the recipient inductor, relates to the displacement current induced by the moving B-field, generated by the external inductor L1. The induced voltage is then amplified and treated with the nearby electronics integrated on the same chip.

![Figure 23. Structure of the inductive microphone (a), SEM photo of the fabricated microphone (b)](image)

We have built the linear analogy model of the inductive microphone as well as its 3D finite elements model. The obtained simulation results predict the dynamic behavior of the microphone as well as the basic microphone characteristics that are satisfying the requirements for audio applications. The microphone sensitive element, thin plate, is suspended over a cavity with the aid of springs. Several kinds of springs, such as Crab-leg spring, U-spring, serpentine spring, and folded flexure spring have been studied to achieve the desired resonance frequency of the structure. The B-field is evaluated for two cases. In the case of a DC signal in the primary coil the signal is induced as a function of distance separating the two plans of the inductors. In the case of an AC signal, an extra term (and hence higher sensitivity) associated with induced E-field leads to higher output signal. The estimated induced voltage is in the µV range.

The first microphone sample has been fabricated in the 0.6µm CMOS technology (Figure 23(b)). Experimental work on this sample is on going. This work was originally initiated, at 2002, by the EMC Research Group from 'Ecole Nationale d'Ingénieurs de Sfax' (ENIS), Tunisia. One PhD thesis on this topic was defended (February 2008) and a second PhD is being conducted in collaboration with the RMS Research group.
3.3.4 Self-adaptive architecture for a chemical wireless sensor node

Members: S. Mir, L. Rufer, E. Simeu, R. Kheredinne, J. Tongbong

Two of the most critical challenges in the design of the nodes of a wireless sensor network (WSN) are power management and reliability. Guaranteeing the safe and reliable operation of a WSN has so far been addressed by building dependability features at the network level. This projects aims at studying self-monitoring techniques that can be implemented at each network node. These techniques will not only help to boost the network reliability but also provide efficient means of power management.

A wise use of the energy stored in a WSN node requires adapting power consumption as a function of the node performances. These performances are subject to constant variations for multiple reasons such as changes in node locations or environmental conditions. Built-in self-test functions for the estimation of node performances can lead to optimal power management. Such functions could also allow a node to respond to specific performance demands from the network. This is not possible in today’s WSNs for which the power consumption of a node is independent from the actual data that is being required by the network. In addition, performance data can allow for fault detection, accurate diagnosis and fault-tolerant capabilities within the node. Network reliability can then be significantly boosted by building dependability features at this level. Finally, such self-test functions can be exploited by the manufacturers during production, reducing to a great extent testing needs which have a very significant impact on final product costs.

This project is aimed at developing self-monitoring techniques for optimal performance and dependability of WSN nodes. The approach we follow is illustrated in Figure 24. The combination of design-for-test features (DFT), in particular embedded sensors, and low-cost algorithms that can be run in the embedded resources of the node are used for the identification of the parameters of the different AMS/RF blocks that constitute the node. These identification procedures are then exploited for monitoring the adequate operation of each block and for controlling their power consumption that is optimized with respect to the required performance level.

These techniques will be demonstrated for a prototype WSN node that includes chemical sensors aimed at the detection of toxic gases. There is an urgent need to develop WSNs of chemical sensors that can be quickly deployed to monitor the release of toxic chemicals into the environment stemming from industrial production or other human activities. Rapid deployment of WSNs can be extremely important to survey vast areas that can be subject to criminal chemical contamination. A description of some of the mixed-signal/RF components of this architecture can be found in other parts of this document. See Section 3.4.3 for the chemical sensor, Section 3.2.3 for blocks of the RF front-end with embedded sensors, and Section 3.1.3 for some of the parameter identification techniques. Part of this work has been carried out in the frame of a projet of the Carnot Institut LSI (Logiciel et Systèmes Intelligents).

Figure 24. Architecture of the WSN
3.3.5 GaN-based piezoelectric sensors

* Members: L. Rufer, S. Vittoz, T. Lalinsky*
  * Slovak Academy of Sciences, Institute of Electrical Engineering, Bratislava, Slovak Republic

Micro- and nano-electromechanical systems (MEMS/NEMS) and smart sensors are mainly based on silicon, which is limited by its mechanical, chemical, optical, thermal and electronic properties. Sensors in harsh environments need new semiconductor materials which are stable, especially at high temperature and in corrosive environments.

Wide band gap semiconductors such as SiC, the Group III-Nitrides (III-N) and diamond can meet this requirement. Of these, the III-N system has distinct advantages. It is the only highly polar semiconductor matrix that has ceramic-like stability and can form heterostructures. This material system having piezoelectric stress coefficients 6-7 times greater than those of GaAs is therefore ideal for piezoelectric sensors in harsh environment. The high chemical stability also results in a polarization that is stable to high temperatures.

The aim of the project is to accomplish detailed modeling of electrical and mechanical behavior of different structures used for pressure and chemical sensors for harsh environment. Electro-mechanical behavior of different layers composing these structures will be simulated in order to predict basic features of these sensors. Piezoelectric and piezoresistive effects in these structures will be studied. The modeling will be based on the Finite Element Analysis and on an analytical approach.

This work is done in the frame of the European project MORGaN (Materials for Robust Gallium Nitride), FP7-NMP-2007-Large -1, No. 214610, funded from 2008 to 2011. The detailed analysis of GaN structures as cantilevers and membranes fabricated with different technologies by other partners of the project will be done. At this stage, we are studying a cantilever structure made of Gallium Nitride (GaN) obtained by the ELOG (Epitaxial Lateral Over Growth) process. This cantilever is coupled with a high mobility transistor (HEMT) that is obtained by epitaxial growth of III-V nitride alloy (AlGaN) on the GaN layer (see Figure 25(a)).

![Figure 25. Cantilever structure with HEMT (a), simulated electrical field due to mechanical load (b)](image)

The sensing principle of this structure is based on the variation of the electrical behavior of the transistor due to a mechanical load. The mechanical load exerted at the free end of the cantilever creates a mechanical stress in the structure that affects the piezoelectric surface charge density at the AlGaN/GaN interface (or interface resulting polarization). Simultaneously, it will modify the threshold voltage of the HEMT.

As a first step, we aim at modeling the GaN cantilever in order to obtain the surface charge density distribution according to the force applied at its free end. We also study different cantilever forms (such as an L-shaped one to increase the stress at the clamped edge). First results show a linear relation between the electrical field (and so the piezoelectric polarization) and the applied force (see Figure 25(b)).
3.4 Modeling of AMS/RF/MEMS devices and systems

3.4.1 Behavioural modeling using statistical techniques

*Members: M. Dubois, K. Huang, H. Stratigopoulos, S. Mir*

An expected way to reduce testing costs is the implementation of a test strategy during the design phase. However, the lack of methods for evaluating different testing techniques (BIST, DFT...) slows down the industrial implementation. In particular, parametric defect level and yield loss due to the BIST approach are never evaluated.

In this work, we have proposed the solution illustrated in Figure 26 for evaluating parametric test metrics for AMS/RF devices. This technique is being demonstrated for the case of a $\Sigma\Delta$ converter. Since it is not possible to perform Monte Carlo simulations of the complete $\Sigma\Delta$ converter that are required for BIST evaluation, we divide the circuit in blocks for constituting a behavioural model. Monte Carlo simulation of each block becomes now feasible and we obtain the statistical distribution of the behavioural parameters. Simulations of the behavioural model are thereafter performed and give the statistical distribution of the performances and of the test criteria. A regression function mapping the behavioural parameters to the performances and test measures is then built for fast generation of a much larger population. A classification of the circuits according to their specified performances is computed using this population. A good circuit has all performances within specifications whereas a bad one fails at least one of them. The test measures are evaluated with respect to their ability to discriminate between good and bad circuits. The test limits are fixed according to the test metrics such as yield loss and defect level.

![Figure 26. Methodology for statistical evaluation of parametric BIST metrics for AMS/RF circuits](image)

The first part of the work has considered the reduction of the converter simulation time. A first assumption to overcome this issue without loss of accuracy was to simulate a combination of macro-models of the accompanying circuitry (biasing stage and clock mainly) and a transistor level description of the signal path. The advantages were to keep the environment used by designers and to take into account external parameters like temperature as illustrated by Figure 27(a) and supply voltages. The statistical model of the biasing circuit has coherent results shown in Figure 27(b) but the method was abandoned because the simulation time was still too long for doing numerous simulations in a reasonable period. So, a better trade-off between precision of the model and simulation time is currently under development using a behavioural model in Simulink®.

![Figure 27. (a) Macromodel of a bandgap circuit, (b) statistical results of transistor level and macro-model simulation using Gaussian distribution](image)
3.4.2 Statistical modeling of sensor signals for fault diagnosis

Members: E. Simeu, E. Bortolin-Argenton, A. Lefebvre*, J.P Derain*, M. Glade*
(*) EUROCOPTER Marignane, France

Helicopters are made up of several components usually needing a very high level of reliability, requiring a large number and variety of sensors not only for the flight control system, but also for monitoring of onboard equipment health status at different levels. Both tasks involve a flawless operation of the sensors. For such critical applications, sensor validation, or the ability to ascertain how well a sensor is working, is required. Signals coming from sensors are processed by the AMC ("Aircraft Management Computer") to generate information on the helicopter health status. For some failures detected by the AMC, this information may be used to locate the most likely cause of failure, i.e. what is the faulty component that has caused the signal failure. But in some cases, accurate fault localization may be impossible due to ambiguity in the fault site identification. Localization ambiguity often occurs in the case of analog sensors. When a failure is revealed, it is difficult to say whether the faulting module is the sensor, the communication medium, the pre-conditioning hardware, or the equipment on which the sensor performs the measurement.

Faced with this difficulty, our research team has collaborated with the Eurocopter Group to develop cost effective techniques to validate the sensor signals. The purpose is to exonerate or to incriminate the sensor when a fault is detected, by analyzing only the signal produced by the sensor itself, regardless of any redundancy of information. For a long time, sensor fault detection activity has focused on sensor range checking. Range checking serves to determine whether instruments are within the nominal operational bandwidth and also saturate data spikes. Range checking is very useful but is limited to the detection of high-level catastrophic events. The more subtle, gradual sensor, actuator, or process degradation due to wear, aging, fouling, and/or corrosion that lead up to catastrophic events are generally not detectable in their early stages.

In the absence of any redundant information, it is difficult to detect abnormalities in the functioning of a sensor as long as the output signal keeps within the admissible output levels defined by the sensor manufacturer. For an active sensor, driven by an external power supply, it has been demonstrated that the measurement of the sensor supply current can, under certain circumstances yield useful information in the detection and diagnosis of some sensor failures. But when this information is not accessible or when the information returned by the supply current is not sufficient, it is convenient to search for other solutions based on the analysis of the properties of the signal that carries the measurement information done by the sensor. Before being processed by necessary filtering and signal conditioning, the signals issued from a sensor are generally submitted to important fluctuations.

We have proposed to transform that difficulty into an advantage because the statistical models that govern these fluctuations are different according to the state (faulty or not) of the sensor (see Figure 28(a)). The objective is to show the ways to detect online common sensor faults and thus enhance sensor reliability. This is done by monitoring online the statistical distribution characteristics for each instrument signal. The parameters of the statistical distribution are estimated and monitored using cost effective methods to accomplish online validation of sensor signals. We refer to this technique as Univariate Statistical Process Control (USPC). An electronic hardware demonstrator of the proposed techniques was designed and built around the microprocessor DS PIC30F3013 from Microchip (see Figure 28(b)). The programs for sensor signals online validation are implemented on the demonstration card and tested successfully on several types of sensors without fault and with various types of faults.

![Figure 28. Statistical distribution of sensor signal in different functioning situations (a) and hardware demonstrator board (b)](image-url)
3.4.3 Modelling and simulation with SystemC-AMS of a chemical sensor

*F. Cenni*, E. Simeu, S. Mir, L. Rufer, A. Sani  
(*TIMA & Università di Bologna, Italy*)

The complexity of present-day's electronic systems integrated in SoC or SiP devices is having a substantial increase. Furthermore an increasing number of non-electric natures appear inside modern systems, especially with the advent of MEMS. Due to these reasons new techniques providing early functional level modelling, simulation and validation in the design flow need to be developed. That is why an AMS extension of the SystemC language standard called SystemC-AMS is in course of development. This will provide the modelling of heterogeneous systems including both continuous-time and discrete-event behaviours at architectural level. A surface acoustic wave (SAW) chemical sensor (Figure 15(a)) has been developed by the RMS group in view of its insertion in a node of a wireless sensor network (WSN).

The microelectronics interface of the sensor has been designed and simulated at transistor level, together with a Verilog-A model of the SAW device. The modelling, simulation and validation of the overall WSN node behaviour requires the facilities provided by SystemC-AMS. A SystemC-AMS model of the SAW sensor has been developed together with a method to build a SystemC-AMS model of a general component by means of the fitting of its transfer function. The blue curve in Figure 29(b) is the SAW's transfer function while the red curve is the fitting result used to generate the SAW filter model. Figure 29(c) shows the SystemC-AMS structure used in order to model a generic transfer function. Finally Figure 29(e) shows the SystemC-AMS model of the overall sensor front-end where the two PLL loops are controlled by two control signals that schedule the phases shown in Figure 29(d).
4. System Level Synthesis (SLS)

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Research areas
- CAD methods and tools for design and analysis of Multiprocessor System-on-Chip.
- Low level software for MPSoC
- Architectures for communication and memory hierarchies
- Prototyping platforms for MPSoC

Financed Projects
- ANR SoClLib
- ANR HOSPI
- Nano2012 Decopus
- Nano2012 Ipist
- Minalogic Sceptre
- Minalogic OpenTLM
- Minalogic Cilé
- MEDEA+ iGlance
- MEDEA+ LOMOSA
- MEDEA+ SoftSoc
- IST SPRINT
- IST SHAPES

Industrial Partners
- STMicroelectronics
- Thales Communications
- Schneider Electric
- Orange
- ATMEL Roma

4.1 Main trend for embedded systems design: Multiprocessor SoC

We define an embedded computing system as an application specific electronic subsystem used in a larger device such as an appliance, an instrument or a vehicle. The digital electronic embedded system functions are usually realized using both software running on CPUs and specialized hardware accelerators. The evolution of technologies is enabling the integration of complex hardware platforms in a single chip; called System-on-Chip, SoC. Modern SoC may include one or several CPUs to execute software and sophisticated interconnect in addition to specific hardware accelerators. Additionally non digital hardware, e.g. analog, RF (telecommunication applications) and micromechanical parts (sensors, actuators, energy scavenging), may be included in the same chip or package.

Mastering the design of these high programmable and parallel embedded systems is a technical and scientific challenge. It requires new design methods, new design tools, new system modeling strategies to allow for concurrent hardware and software design.

100% of new ASICs include several CPU in 65nm technology. Mobile and Multimedia platforms are multi-processor system on chip (SoC) using different kinds of programmable processors (e.g. DSPs and microcontrollers). Heterogeneous cores are exploited to meet the tight performance and cost constraints. Tomorrow's SoCs are composed of multiple, possibly highly parallel, processors for applications such as mobile terminals, set top boxes, gaming consoles, graphic cards, and network processors. Moreover, these chips contain sophisticated communication networks-on-chips (NoC) to sustain the ever increasing bandwidth requirements. So mastering a huge task level parallelism is the next SoC design challenge. As a result, design methodologies must change their focus to the selection, specialization and usage of processors —either programmable or dedicated— as basic components rather than the logic modules. Compared with conventional ASIC design, such a multi-processor SoC is a fundamental change in chip design.

The SLS group is working on both hardware and software architectures for MPSoC systems, targeting simulation models or prototypes.
4.2 CAD methods and tools


The CAD actions developed in the group covers the following themes: Modeling, Simulation, Debug and Code Generation.

The work done in modeling targets the abstract description of hardware/software multiprocessor systems. This work is of primary necessity as the number of processors in integrated circuits is raising, and therefore the simulation times are increasing constantly. As a result, the execution of the software on Instruction Set Simulators during simulation (making the processor the ultimate hardware/software interface) is not viable anymore. The idea is thus to model the system as a stack of layers, and each upper layer can rely on the functions provided by the lower level layers. If the abstraction is coarse, then several layers can be merged to provide at a low execution cost the functions (usually realized on top of an operating system or a high level hardware abstraction such as SystemC TLM), if the abstraction is fine grain, then the “real” realization (some OS code for example) is provided, and the hardware can be described more accurately at the cycle level. One of the abstraction that can be made is illustrated on the Figure 1. The leftmost part of the figure represents an abstract view of a platform, then details the CPU subsystem that contains one or several CPUs but that share the same operating system (SMP) and software layers. Finally, the hardware view of the subsystem is abstracted.

![Software stack representation](image)

The modeling approach is mainly useful for simulating systems at different levels of abstraction. Going high into the abstraction can lead to purely functional informations. Addresses may even be hired behind programming level constructs such as array or variable definitions. This is not the kind of simulation that we target: we want to abstract a hardware CPU subsystem as an API, the Hardware Abstraction Layer API (see the item 4.3 Low-Level Software). This API represents the basic hardware access that a (set of) processor(s) can do. The implementation of the API is done in SystemC, using more or less abstract (or precise) models of the underlying hardware.

Concerning simulation, the main contribution has been to define a Native Simulation approach that allows to simulate a multiprocessor system (whose software enforce the use of the HAL API) using the host machine instead of interpreting the instructions. The Figure 2 illustrates the approach that relies on the use of the memory of the simulator (in the Unix process) as the memory of the simulated system. This allows to avoid remapping techniques that are not able to handle some situations at the price of a strict adherence to an API (that is very often necessary for porting matters but that may not be used in legacy codes). In order to provide estimations of execution time, an LLVM based framework is being developed to generate “host code” based on the exact “cross-compiled” code to provide additional information at run time. As far as processor simulation is concerned, the use of dynamic recompilation techniques is very promising from a speed perspective. However, these techniques do not currently provide accurate speed and/or power estimates of the code execution, because inherently the approach “forgets” the original code. We are currently investigating the lightweight addition of information during dynamic translation, at the basic-block level, to handle this issue. This could benefit the basic-blocks analysis to be done for the native simulation.
We started an activity in debugging by looking at the bugs in concurrent programs running on simulation platforms to ensure first non-intrusiveness and second potential access to all the resources. This work will benefit from the experience gained in the participation to an international consortium that has defined an access API both for simulation models and actuals hardware devices.

The work on Code generation from high level models have been continued. A Simulink based code generation tools has been defined and implemented. The code is produced for an abstract programmable architecture that is described as a set of execution units connected by communication paths. However, code generation for embedded device does not solely consist of programs, it very often also consists of configuration files that set-up a highly parameterized device for performing a given application. The devices that make heavy use of configuration files are usually very demanding in terms of performance, and dynamic reconfiguration can occur only at very well identified time stamps. We have defined two languages to describe applications and platforms in an abstract manner, and a meta-mapping language to express the mapping capabilities. Using these high level concepts, we are able to generate, for a well identified class of platforms, all the configuration files that put the device in the right state. The handling of dynamicity is yet to be investigated, as it is quite complex to describe by structural languages.

Processors with extensible instruction sets, i.e. that have a predefined instruction set architecture that can be enhanced by specific resources (either function or registers) used by ad-hoc instructions, are currently reaching the market. A specific approach to building multiprocessor platforms based upon these core has been developed, to take benefit from the specialization while still using the general purpose core whenever possible.

This area is supported by the following projects: OpenTLM, SPRINT, LoMoSA, HOSPI, iGlance, SoftSoC, Decopus, Ipist.

4.3 Low level software


We are used to representing software by layers. Figure 2 illustrates the software stack organization in two layers: application layer and HdS (Hardware dependent Software) layer.

The application layer may be a multi-tasking description. The HdS layer represents the software layer which is directly in contact with, or significantly affected by, the hardware architecture. The HdS integrates all the software that is directly depending on the underlying hardware, such as hardware drivers or boot strategy. It also provides services for resources management and sharing, such as scheduling the application tasks on top of the available processing elements, inter-task communication, external communication, and all other kinds of resources management and control.

The operating system (OS) is the software component that manages the sharing of the resources of the architecture. It is responsible for the initialization and management of the application tasks and communication between them. It provides services such as tasks scheduling, context switch, ...

The communication layer is responsible to manage the I/O operations and more generally the interaction with the hardware components and the other subsystems. This communication layer implements the different communication primitives used for task communication (intra or inter processor).

The HAL is a thin software layer which totally depends on the type of processor that executes the software stack, but also depends on the hardware resources interacting with the processor. The HAL includes the device drivers to implement the interface for the communication with the device.
The API are well defined interfaces that allow an upper layer to use lower layer functionalities.

So we have developed a small embedded operating system (exo-kernel), called DNA-OS, that has been ported on top of all classical processors (ARM, MIPS, SPARC, Microblaze, …). This OS serves as basic component for a software design flow able to produce binary code for all computing units of a multiprocessor architecture. This software design flow is used in different projects, in order to help software application designers to port their applications on hardware architecture (simulation model or real board – see prototyping section).

This approach is being extended to generate all configurable files required in specific architecture using IP connected through a NoC. The main difficulty is to define a specification model of the architecture, of the application and of the mapping of functionalities onto hardware resources.

This area is supported by the following projects: SHAPES, LoMoSA, SoCLib, Ciloé, HOSPI

4.3 Architectures

*Contributing PhD candidates and Post-Docs : P. Guironnet de Massas, K. Hassan, D. Hedde, A. Kouadri Mostéfaoui, Q. Meunier, Ch. Sahnine, H. Sheibanyrad.*

It is our belief that the future SoC architectures will tend to be more homogeneous and, because of the high level of parallelism, will need to have support to make their programming easier. Specifically, the new platforms will be so parallel that they will tend to be as hard to program as the parallel machines (shared memory or message passing).

We focus specifically on shared memory multiprocessor machines, as it has been a widely used approach to concurrent programming. It is also quite natural in integrated systems as the memory bandwidth can be very high, thanks to the use of Networks on Chips. This leads to several choices, detailed now.

Make the memory hierarchy transparent and efficient: this means that caches will be used globally, requiring coherency. This also means that the internal memory will be spread over the chip to ensure a high bandwidth. To optimize the handling of data and instructions, we are currently working on hardware managed page migration techniques to put the necessary information closer to the processors that uses it.

Optimize access to external RAM: the access patterns are fundamental to benefit from the highest possible bandwidth for external DRAM access. The current memory controllers try to optimize the access by building packet of data belonging to the same page, but the memory controller has only a local view. We try to take benefit from some knowledge available at the Network level, usually available as QoS or priority on virtual channels, in the hope that including this high level information will minimize the latencies.

Optimize atomic accesses: The use of spin-locks has been shown theoretically to be a suboptimal solution to the problem of advancing synchronized parallel executions. The introduction of the couple *linked load/store conditional or compare and swap* has been the advocated solution for years (even though the implementation is not that straightforward). Recently, the introduction of the concept of transactional memories is regarded as an other, more general solution, to the handling of atomicity. We are investigating currently the design and applicability of transactional memories in SoC, as the support of parallel programming paradigms.

Support for unusual concurrent programming paradigms : POSIX Threads and MPI are the two well known representatives of shared memory versus message passing programming paradigms. For some time, the *work stealing* idea has been introduced. The principle is that each processor executes its own task until it becomes idle, and then steals a fraction of the remaining work on a randomly chosen busy processor. We have evaluated several implementation of adaptive work stealing and architectural choices to enhance the performances of work-stealing. We have shown that simple architectural support and wise copy of data can provide up to a 20% performance increase.
The last topic in architecture concerns 3D-NoCs. As the die stacking technologies evolve and thanks to the introduction of Through Silicon Vias, real 3D topologies can be envisioned. A work on 3D router microarchitectures is currently starting, and we also reevaluate 3D topologies in the context of 3D integration, constrained by yield, clock skew, number of TSVs and so on.

This area is supported by the following projects: SOCLib, Sceptre, Ciloé, iGlance

4.4 Prototyping


Multimedia applications impose drastic constraints in terms of time to market and design quality. Efficient hardware platforms do exist for these applications. Usually the architectures are heterogeneous multiprocessor architectures with specific I/O components in order to achieve computation and communication performances. Programming these architectures usually results in writing separate low level code for the different processors (DSP, micro-controller), implying late global validation of the overall application with the hardware platform. Hence, the key challenge is how to program efficiently such architectures, starting from a high level model and how to map an application onto such an architecture. An additional difficulty is to debug and validate the lower software layers required to map the high level application code on the architecture.

We developed a software design flow able to efficiently use the resources of the architecture and allowing to easily experiment several mappings of the application onto the platform resources. The key idea is to structure the design flow allowing incremental validation of the different software components. We use several software development platforms able to abstract a sophisticated multimedia architecture at different abstraction levels allowing separate debug of the software components.

We applied this approach on an off the shelf multimedia platform (called a tile), involving a high performance DSP and a RISC processor, to explore communication architecture and generate an efficient executable code for a multimedia application. The main objective is to be able to connect about 1000 of such tile (through a NoC) to reach $10^{15}$ FLOPS (Peta FLOPS). This deals as well with communication for inter-tile and intra-tile.

We are currently studying the architecture of the Cell processor platform, as an industrial example of heterogeneous multiprocessor platform. As programming a Cell requires a similar approach as programming the embedded platforms we have worked on, we are evaluating our low level software approach on it.

An other prototyping activity copes with NoC implementation on specific boards. The main objective is to map a generic NoC on several Virtex II pro boards, implementing the communication between boards with fast serial links. This offers then an interesting scalability for the hardware architecture and provides a good way for architecture exploration and evaluation. We introduced the notion of Network in Package (NiP) for wired-bonded Multichip modules, that is currently being extended toward real 3D-NoCs using through-silicon vias.

This area is supported by the following projects: SHAPES, Ciloé
4.5 PhD topics

1. ElMrabti Amin, “Abstract modeling of architectures and applications for system generation”
4. Chen Hui, “Models and code generation approaches for HW/SW IP integration”
5. Gerin Patrice, “Modeling of hardware/software interfaces”
6. Gligor Marius, “Programming for low power on MPSoC platforms”
7. Guérin Xavier, “Kernels for heterogeneous MPSoC architectures”
8. Guironnet de Massas Pierre, “Transparent Integration of memory hierarchies in MPSoC architectures”
9. Hassan Khaldon, “Memory controllers for NoC based MPSoC”
10. Hedde Damien, “Debug of concurrent programs using non intrusive simulation techniques”
11. Horrein Pierre-Henri, “End to end protocols for high throughput radio”
13. Meunier Quentin, “HW and SW support for Parallel programming integrated multiprocessors”
17. Senouci Benaoumeur, “Methods for automatic mapping of HW/SW models on reconfigurable prototyping platform”
18. Shen Hao, “Models for the estimation and analysis of performances of SoC architectures using flexible processors”
5. Verification and modeling of Digital Systems (VDS)

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Interns:  T. Kayrak, V. Pataskar, J. Sester

Research areas

Contracts
- SFINCS (ANR), FME³ (ANR), SoCKET (Pôles de compétitivité), Beyond DREAMS (MEDEA+)

Industrial partners
- Dolphin Integration, Thalès Communications, STMicroelectronics

Academic Partners
- LSV (ENS Cachan), Radboud University (Nijmegen, NL), McGill University (Montréal, Canada), Royal Institute of Technology (Stockholm, Sweden)

The design of first time correct systems on a chip (SoC) involves, among many other challenges, guaranteeing that the system as designed will behave according to a specified set of functionalities. The VDS group is mainly concerned by the correctness of the hardware design, from its early specification levels to the "register transfer" level (RTL). The research of the VDS group aims at providing effective specification methods, description guidelines, semantic definitions, and proof strategies, to ease the use of new verification techniques. In the following sections, we discuss three main aspects:

- assertion-based verification (ABV) of IP's using the notion of hardware property checkers (monitors) and test generators,
- assertion-based verification of SoC's specified at the transactional level (SystemC TLM),
- formal verification of the communication infrastructure in Networks on Chip (NoCs).

Another (new) aspect of our work is related to the application of formal methods to fault-tolerance (in cooperation with the ARIS group). The last section summarizes our first results.

5.1 Assertion-based verification of IP's – Horus project


Horus project. The Horus project aims at providing methodologies and tools for efficiently supporting property-based design all along the design flow. Formal properties can be expressed at the earliest specification step, experimented with, refined and complemented, using standard languages with formal semantics like PSL. Properties may express:

- the results expected from the device. These "assert" statements can be checked throughout the design flow using observation monitors.
- the characteristics of the device environment, under the form of constraints on its inputs. Input sequences satisfying these "assume" statements can be produced by test sequence generators.

From asserted and assumed properties, Horus automatically produces synthesizable source modules for the corresponding monitors and generators. It also provides a graphical user interface to support the interconnection of these modules with the design at hand. The same modules, without any adjustment, can be used for simulation, emulation, or synthesis purposes, with the objective of design verification, system integration test, and online fault detection during execution.
The Horus platform helps the user build an instrumented design to ease debugging: it can synthesize monitors and generators, connect them to the design under test (DUT) and adds a device to snoop the signals of interest. It comes with the VHDL and Verilog flavors. The Horus system has a friendly graphical user interface for the generation of the instrumented design in 4 steps:

**Step 1 - Design selection:** The DUT, with its hierarchy, is retrieved.

**Step 2 - Generators and Monitors synthesis:** Select properties or property files, define new properties, select target HDL language, synthesize monitor or generator (verification IP).

**Step 3 - Signal interconnection:** The user connects the monitors and the generators to the design. All the signals and variables involved in the DUT are accessible in a hierarchical way. The user needs only select the signals to be connected to each verification IP.

**Step 4 - Generation:** The design instrumented with the verification IPs is generated. When internal signals are monitored, the initial design is slightly modified to make these signals accessible to the monitors.

The outputs of the verification IPs are fed to an instance of a generic analyzer; this component stores the monitors outputs and sends a global status report. It also incorporates counters for performance analysis. The instrumented design has a generic interface defined for an Avalon or a Wishbone bus. If the FPGA platform is based on such a bus, the user can directly synthesize and prototype the instrumented design on it.

We have realized the application of Horus to a variety of circuits, among them a Wishbone compliant crossbar. Many properties have been verified with the Horus platform, for instance:

Assume two masters $M_j$ and $M_k$ have priorities $p_j$ and $p_k$ such that $p_k > p_j$. If $M_j$ and $M_k$ request the same slave simultaneously, then $M_k$ will get it first i.e.,

$$\text{assert always (} M_j\_cyc\_o \text{ and } M_k\_cyc\_o \text{ and } \text{CONF}[2k..2k - 1] > \text{CONF}[2j..2j - 1] \text{ and } M_j\_addr\_o[0..3] = M_k\_addr\_o[0..3] \rightarrow (M_k\_ack\_i \text{ before } M_j\_ack\_i))$$

We have compared our results with other tools: FoCs (from IBM) and MBAC (from McGill University, Montreal). This comparison has been done on monitors since no other tool that we are aware of synthesizes hardware generators for PSL properties.

- The results of Horus are equivalent to the results given by MBAC: the FPGA size, in terms of logic cells and registers, are either identical, or within a few percent for complex monitors, the result of MBAC in that case being better optimized. The positive advantage of the Horus method lies in the fact that the whole construction is formally proven correct.

- The comparison with FoCs is more difficult since the PSL subset for dynamic verification is not fully supported by FoCs, and some properties could not be synthesized. When FoCs gives results, Horus is equivalent on simple properties, and significantly better when the property is more complex.

**Asynchronous technology.** Similarly to synchronous monitors, **asynchronous monitors** can be employed for logical simulation or emulation onto a FPGA board. While in synchronous circuits a clock globally controls the activity, the asynchronous circuit activity is locally controlled using communicating channels that detect
the presence of data at their inputs and outputs. This is consistent with the so-called handshaking or request/acknowledge protocol. One transition on a request signal activates another module connected to it. Therefore, signals must be valid at all times. Asynchronous circuit synthesis must be more strict, i.e. hazard-free. In order to have very reliable monitors, we choose to implement Quasi-Delay Insensitive (QDI) circuits. Indeed, these circuits are very robust to Process, (strong) Voltage and Temperature (PVT) variations. Moreover, they offer nice properties such as modularity and low-power consumption.

Like in the synchronous case, the monitor construction mimics the structure of the property. It is based on a library of primitive monitors (one for each PSL operator) and on a syntax directed interconnection scheme. The figure below illustrates the construction of the monitor for property

**PSL property P1 is**

\[ \text{always A} \rightarrow \text{B until C}; \]

A monitor takes as inputs the reset, the synchronization signal (clock), and the signals (A, B and C) of the design under verification (DUV) that are operands of the temporal operators of the property. The monitor outputs the signal False that provides the evaluation result ('0' means absence of error, '1' means error). To respect the handshake protocol, the signal False is acknowledged. To avoid any behavioral modification in the DUV, the observed signals and the clock signal are not acknowledged.

The novelty of our approach lies in the fact that the advancement of time is seen either as a sequence of events on arbitrary signals or on occurrences of a single master clock ticks. Signal changes, or clock ticks, are considered the points in time when PSL formulas are to be evaluated.

More details can be found at http://tima.imag.fr/vds/Horus/

### 5.2 Assertion-based verification at the transactional level

**Members:** L. Ferro, L. Pierre

The first formalized functional specification of a SoC, expressed at the so-called "transaction level", is usually written in terms of algorithms and abstract communications between large macro-blocs. Designers extensively execute test cases on simulation models written in languages such as SystemC or SystemVerilog, for which no formal hardware semantics and associated formal model extraction is available. In addition, to face increasing time pressures, a design methodology called "platform-based design" is now popular in the semiconductor industry: a new SoC is built according to a generic architecture, using pre-existing parameterized virtual modules and processor cores, the simulation models of which are retrieved and interconnected, possibly using some adaptation interfaces. In that context, SystemC TLM (Transaction Level Modeling) is perceptibly being adopted. It allows to describe SoCs at a very high level of abstraction, with emphasis on the transactions (communications) between components.

The methodology we are developing enables the **dynamic verification of properties for TLM descriptions:** we check the validity of PSL assertions that express properties regarding communications i.e., properties associated with transactional events (for instance data are transferred at the right place, two communication operations with given characteristics must follow each other,…). Like in the Horus technology, the monitors are **built as the linear composition of primitive components** associated with the elementary PSL operators. These primitive components have been defined once and for all and are grouped in a library. For **monitoring SystemC transactional descriptions**, we consider that observation points are when the assertion needs to be re-evaluated i.e., each time a variable of the assertion has possibly been modified (an appropriate event...
occurs in the corresponding channel). Hence, the traces we analyze are made of the events that may enable the observation of updated values for the variables involved in the assertion. Technically, we use a model that allows to observe these transactional events in the system and to trigger the monitors when needed.

A prototype tool has been implemented as an extension of the Horus environment, it mechanizes the monitor construction and the generation of the verification-oriented description (SystemC description of the design instrumented with monitors + observation infrastructure), as pictured below.

![Diagram of testbench creation process]

This tool is equipped with a GUI as shown on the screenshot below (tab "Properties" that allows to input a PSL property expressed in terms of given transactional events, written in the SystemC flavor).

![Screenshot of GUI with PSL property]

PSL assertions are monitored during simulation and assertion violations are reported, if any. In many cases, the better chosen the stimuli, the more efficient the approach: testbenches should enable the analysis of an assortment of nominal behaviors as well as of corner cases. To that goal, our simulation/monitoring environment has been coupled with the combinatorial testing tool Tobias developed at LIG (http://www-lsr.imag.fr/Les.Groupes/PFL/Tobias/). Appropriate sequences of operation calls and proper sets of values are identified by the user and captured in test schemes, that are used to automatically generate test programs with large amounts of well-selected stimuli.
Various case studies have been developed to demonstrate the effectiveness of our approach. Among them, we have verified properties for a Motion-JPEG decoding platform developed in the SLS group. The figure below gives a screenshot that illustrates assertion violation reports during simulation. Property "the data that are written on the RAMDAC (viewer) are exactly the ones that have been transmitted by the processor" is checked, with design errors purposely introduced in the communication channel. While the image on the RAMDAC is not as expected, our monitor reports errors when detected (on the left).

More details can be found at http://tima.imag.fr/vds/Isis/

5.3 Formal verification of NoC communication infrastructure

Members: A. Helmy, L. Pierre, D. Borrione

The current technology allows the integration on a single die of complex systems-on-chip (SoC's) that are composed of manufactured blocks (IP's), interconnected through specialized networks on chip (NoCs). IP's have usually been validated by diverse techniques (simulation, test, formal verification) and the key problem remains the validation of the communication infrastructure. The work reported here addresses the formal verification of NoCs by means of a mechanized proof tool, the ACL2 theorem prover.

We use a formal meta-model that represents the transmission of messages on a generic communication architecture, with an arbitrary network characterization (topology and node interfaces), flow control mechanism, routing algorithm and switching technique. The main function of this model, called GeNoC, is recursive. In the original model (published some years ago) function GeNoC represents the transfer of messages from their source to their destination, as sketched below.

Its main argument is the list of emitted messages. It returns the list of the messages received at destination nodes. Its definition mainly relies on the following functions:

- interfaces are represented by two functions: send to inject frames on the network, and recv to receive frames,
- the routing algorithm and the topology are represented by function Routing,
- the switching technique is represented by function Scheduling.

In this original model, which mainly stands at the Network layer of the OSI stack, many simplifying hypotheses were adopted. In particular, messages are atomic, nodes are simply seen as their coordinates, and there is no explicit notion of time. The model expresses how a message travels in the network, but the granularity is the movement of the message from its source to its destination, not the time steps of this movement.
The current GeNoC version results in new modules. They contain an explicit representation of the global state of the network, and explicit time stamps for the emission of messages. Functions Routing and Scheduling are modified to enable a step-by-step simulation of the evolution of the network state. The characteristics of the new model are the following:

- a global network state representing the current status of the memory elements associated with the ports of the nodes, and an explicit notion of time,
- at the Transport layer, interfaces are still represented by two functions send and recv. Function R4D (“ready for departure”) determines which messages can be in the network at the current time,
- at the Network layer, the routing algorithm is represented by function Routing and the switching technique is represented by function Scheduling. The routing algorithm is represented by the successive application of unitary moves (e.g., routing hops). For each message, the routing function computes all possible routes from the current position to the destination. Function Scheduling returns a list of messages that have reached their destination and a list of messages that are en route to their destination. The model also allows the modeling of priorities between messages,
- at the Data Link layer, the transmission protocol can be specified.

These functions are not given explicit definitions. Rather, they are characterized by the set of properties they should satisfy, called proof obligations or constraints. It has been proven, once and for all in the GeNoC meta-model, that this set of proof obligations implies correctness theorems, which state that:
o every message arrived at some node \( n \) was actually issued at some source node \( s \) and originally addressed to node \( n \), and that it reaches its destination without modification of its content,
o no message is lost (for instance by the transmission protocol).

Proving that a particular NoC is a valid instance of GeNoC amounts to:
o defining the functions that describe the network topology,
o defining all the functions associated with the communications, in particular Routing and Scheduling,
o discharging the proof obligations for these functions.

This technique has been applied to various NoCs:
o the Hermes NoC (PUCRS, Brazil): http://www.inf.pucrs.br/~gaph/Projects/Hermes/Hermes.html,
o the Spidergon NoC from STMicroelectronics,
o the Nostrum NoC (Royal Institute of Technology, Stockholm): http://www.ict.kth.se/nostrum/.

See the web page at http://tima.imag.fr/vds/GeNoC/genoc.html

5.4 Application of formal methods to fault-tolerance


The work reported here is performed in the framework of the FME\(^3\) project, in cooperation with the ARIS group.

Designing dependable circuits requires in particular evaluating, at each step in the design flow, the achieved level of robustness against various types of faults or errors. In critical systems, an erroneous piece of information may lead to dramatic consequences in terms of human lives. In those cases, errors are generally the consequence of natural phenomena such as particle impacts, electromagnetic perturbations, electrical noise or degradations due to aging. The causes of errors, called faults, were usually modeled in digital systems as single bit-flips or signals stuck either at 1 or at 0. With the evolution of technologies, circuits are increasingly sensitive to transient faults that have therefore become the main concern for designers. Also, faults increasingly lead to multiple-bit errors that are more difficult to detect or tolerate in the system. Our project targets the development of new methodologies for analyzing the robustness of circuits described in VHDL at the Register Transfer (RT) level, with respect to errors caused by transient faults. Our goal is to take advantage of formal methods to get accurate and efficient solutions that would complement existing fault-injection techniques. We have chosen to start this work by developing a model inside the ACL2 theorem prover, devoted to the verification of fault-tolerance properties in the case of auto-correcting circuits.

First, a specialized tool called VSYML has been developed: it parses the VHDL code, performs symbolic execution, and produces an XML representation of the transition and output functions (for a Mealy machine):
\[
\delta : I \times S \to S \\
\lambda : I \times S \to O
\]

This format is easily transformed into an ACL2 representation, as illustrated below.

![Diagram of VHDl RTL description, VSYML, XML format, Characterization of errors, ACL2 macros, ACL2 code: transition and output functions + fault injection + properties]
meta-characterization of the fault injection function \( f \) as the conjunction of the following properties:
- \( f \) takes as parameter a state \( s \) and returns a state \( f(s) \)
- \( f(s) \) is different from \( s \) (injection is actual)
- only one memorizing element differs from \( s \) to \( f(s) \)

Then, considering for instance the case of a device that has a property of auto-correction in one clock cycle in the presence of single faults (e.g. a TMR architecture), we can verify theorems such as the one below:

For any initial error-free state \( S_0 \), if a fault is injected after \( n \) clock cycles \( (n > 0) \) then it will be corrected one clock cycle later i.e., the resulting state will be equivalent to the resulting state without fault injection:

\[
\delta(i, f(\delta^n(i, S_0))) = \delta(i, \delta^n(i, S_0))
\]

where \( i \) is an input sequence, and \( i \) is the current input.

The proof of such a theorem in ACL2 takes few seconds, depending on the complexity of the device.

Complex hardware systems are typically described hierarchically as the interconnection of simpler components. We can take advantage of this hierarchical construction to perform hierarchical verifications, thus considerably improving the efficiency of the method. To that goal, we reason as follows with a component \( C_1 \) enclosed in a component \( C_2 \):

From the VHDL description of component \( C_1 \), we know the sets \( I_1, O_1, S_1 \) (deduced from the input/output ports and local signals declarations), and the transition and output functions

\[
\delta_1 : I_1 \times S_1 \rightarrow S_1 \\
\lambda_1 : I_1 \times S_1 \rightarrow O_1
\]

For this component, we also have an error model specified by a function \( f_1 \). Using all these characteristics, and locally to component \( C_1 \), we determine:
- a predicate \( S_{p1} \) which is the state recognizer for \( C_1 \) i.e., \( S_{p1}(s) = \text{true} \iff s \in S_1 \)
- a predicate \( S_{reach1} \) which is the recognizer for the reachable (error-free) states of \( C_1 \). For instance, in the case of a TMR architecture, reachable states are such that the contents of the three registers are identical
- a set \( P_1 \) of fault-tolerance properties (theorems) for \( C_1 \)

The definitions of the functions are local to \( C_1 \). The outside world, in particular component \( C_2 \), only knows the existence of \( \delta_1, \lambda_1, S_{p1}, S_{reach1} \) and \( f_1 \), and can use theorems \( P_1 \) to infer other properties. Component \( C_2 \) is characterized by similar constituents, and its properties \( P_2 \) are deduced from \( P_1 \) (and possibly from the properties of all other components contained in \( C_2 \)).

CPU times are significantly optimized through hierarchical proofs.

See the web page at \( \text{http://tima.imag.fr/vds/FME3/} \)
6. Architectures for Robust and complex Integrated Systems (ARIS)

Group Leaders: M. Nicolaidis and R. Velazco
(e-mails: Michael.Nicolaidis@imag.fr, Raoul.Velazco@imag.fr)


Research areas
- Methodology, tools and experimentation for the study of the IC's sensitivity to radiation;
- Methods and tools for fault injection;
- HW and SW techniques for hardening digital/analog architectures for SOCs and NOCs;
- SEU hardened cells;
- SEL mitigation architecture;
- Fault Tolerant Architectures for mitigating the flaws of Nanometric CMOS
- Defect Tolerant Architectures targeting very high defect densities.
- Secure digital implementations;
- Robust logic implementations based on single electron transistors;
- Carbon Nanotubes Transistors characterisation, study of dispersions.
- Computing Architectures for Nanotechnologies
- Design and exploitation of experiments on-board satellites and high altitude balloons.

Contracts
- ATMEL, CNES, EADS, E2V,
- STMicroelectronics, ACI-SI Mars, IACI
- Nanosys
- MEDEA PARACHUTE
- ALFA, CLUSTER
- Aeronautique.
- FT-ORANGE
- THALES
- ARAVIS minalogic
- ASTER minalogic

Industrial Partners
- ARTISAN (USA), CEA/LETI, iROC (France), OEMPLUS (France), THALES COMMUNICATION (France), NASA GFSC (Washington, USA), AIRBUS (France), EADS-CCR (France), ATMEL, EADS-ST (France)

6.1 Summary

The ARIS group was created in 2007 as a continuation and extension of past activities performed in the RIS group (Reliable Integrated Systems) and then in the QLF group (QuaLiFication of circuits) of TIMA. Research activities of the group deal with the study of the IC behavior in harsh environment. Indeed different types of interferences and parasitic effects affect the reliability of modern electronic systems. Nanometer circuits, microelectronics, micro-system technology and power electronic systems are already part of our daily life. However, these systems encounter many problems with natural and artificial interferences coming from various sources (e.g. particle radiation effects, electromagnetic interferences, etc.). Another related area is the new threat on secure systems, related to fault-based attacks.

One of the main stress considered is radiation of nuclear and space environments, but it is interesting to mention that particles reaching the Earth's surface from the Sun, up to now innocuous for microelectronics circuits, have sufficient energy to flip bits in memories and corrupt logic inside processors for parts manufactured with less than 0.25 μm and supply voltages drop to less than 2.2 Volts. This can constitute a threat to avionics control systems (at 30,000 feet, the neutron activity is 4 to 8 times higher than the ground), and even to systems operating at sea level.

One of the important issues of these researches is the prediction of error rates of a studied system (circuit, architecture, software ...). The refinement of forecasting error rate strategies needs both to perform ground test by means of simulated radiation environment (particle accelerators) and to compare ground test results to data obtained from experiments aboard of spacecrafts. A satellite experiments developed in collaboration with CNES (French Space Agency) and NASA GFSC (Goddard Flight Space Center) aims at studying the sensitivity of
advanced FPGAs (Field Programmable Gate Arrays) to transient errors provoked by radiation, so-called Single Event Upsets (SEU). The satellite carrying this experiment, presently at the end of development phase, will be launched in 2011 in the frame of NASA LWS/SET project (Living With a Star/Space Environment Testbed). In the figure below is depicted the experiment developed at ARIS embedded in the LWS satellite carrier. The experiment includes an architecture implemented by means of a Virtex II SRAM-based FPGA in which was implemented a fault tolerant (Triple Modular Redundancy) architecture of a cryptographic application.

Figure 1. Space Environment Testbed (SET) of Living With a Star (LWS) Satellite from NASA

Another research field concern the development of innovative methods and tools dedicated to the predictive analysis, validation and qualification of integrated electronic systems using fault injections. The sensitivity predictive analysis platform covers the development of multilevel fault injection methods and tools to be applied at different system abstraction levels from RTL level to gate level descriptions.

The activities of the ARIS group concern both natural and intentional faults in integrated systems. Activities are also on-going on the design of secure circuits protected against fault-based attacks. These activities include the analysis of the circuit robustness against a whole panel of attacks (DFA, DPA, EMA) and the evaluation of protection techniques. Common approaches are developed to analyze the dependability level and protect circuits against both types of faults (natural and intentional), taking into account their different characteristics.

More recent research areas of the group include fault tolerant architectures for mitigating the flaws of nanometric CMOS (variability, accelerated circuit aging and parasitic effects); fault tolerant architectures for high defect densities targeting post CMOS nanotechnologies; and Computing architectures for nanotechnologies.

6.2 Study by real life experiments of the effects of radiation on the operation of submicronic integrated circuits

Members: P. Peronnard, R. Velazco, G. Foucard, S. Fernandez, P. Ferreyra

Ionization resulting from charged particles and atoms present in the substrate of CMOS circuits, may modify memory cell’s content or provoke a transient pulse within a combinational circuit. This phenomenon which until recently was only considered to be a treat for space applications is nowadays a major concern for avionic equipments and even for any application operating at ground level. Thus it constitutes a potential obstacle to the reliable operation of circuits manufactured from future deep submicronic processes.

A first step towards a thorough study of this problematic consists in putting in evidence the phenomenon through experimentation with suitable test vehicles and an appropriate neutron beam. In February 2000 was carried out one of the first experiments performed in France in this area. A generic and versatile test platform, the THESIC (Test for Harsh Environment Studies of Integrated Circuits) was developed at ARIS and is used to perform radiation ground test experiments to evaluate the sensitivity of integrated circuits to different kind of particles (heavy ions, neutrons, protons,…). These experiments put in evidence the need for the use of hardening techniques (design hardened memory cells, error detecting and correcting codes,….) in future deep
submicronic circuits. Indeed, the number of detected bit flips suggest that next generation of SoCs (Systems on a Chip) or high-capacity static memories may be the source of frequent errors even for systems operating at sea level.

Current researches in this area are dealing with the design and exploitation of an experiment including a very large capacity SRAM memory, which will be exposed to the effects of natural atmospheric radiation at different sites, to derive realistic error rates in real life environment of future submicronic components. Candidate SRAMs for this real life testing were evaluated using a fault simulation technique and dedicated tools (Giant 4). Obtaining real life versus accelerated test figures will help in giving trends for future technologies. This project started the experimental phase in 2007, phase that took benefit of the partnership offered by an European project, the ALFA (America Latina Formation Académica) NICRON project. The activities performed during ALFA NICRON allowed gathering preliminary results about the impact of atmospheric neutrons in advanced integrated circuits, this at different altitudes and latitudes, particularly using facilities at high altitude (available in Peru) or stratospheric balloons which will evolved in the so-called SAA (South America Anomaly) zone well known as being significantly more error prone than other regions of our planet. Three stratospheric balloons were successfully launched from an Air Force base in Uruguay (see photo depicted in Fig. 1). The short duration of the flights (around three hours) does not allow detecting SEUs, but these launches allowed to validate the electronic equipment in the payload and the logistic of such experiments. Longterm experiments (flights expected to have a duration of many weeks) using more powerful aerostatic balloons are planned to be performed in 2009. The same SRAM board was activated in different commercial flights, allowing to put in evidence the occurrence of MCU (Multiple Cell Upsets) which are of high concern for applications requiring high reliability. Indeed, one of the faults detected proved that as the impact of a single neutron the content of five memory cells (the one impacted by the particle and its four neighbours) were corrupted. Such a multiple error may constitute a harsh challenge for the detection by using state-off-the-art techniques. An experiment was also installed at high altitude (at 3800 mts in an university of Cusco, Perou) and allowed to detect some SEUs. Such experiments must have a duration of many months to get statistics that can be used to extrapolate the obtained results to error rates at

![Figure 2. Ballon launch from the Air Force base in Uruguay. The payload included a 1 Gbit SRAM](image)

An experiment to be embedded in the SARE (Satélite de imágenes de Alta Resolución) from the Argentinien Space Agency (CONAE) is presently under development at ARIS research group.
6.3 Development of a test bed suitable for the qualification of integrated circuits devoted to operate in harsh environment

Members: R. Velazco, G. Foucard, P. Peronnard

With the miniaturization, integrated circuits become more and more sensitive to perturbations resulting from the effects of the environment (temperature, radiation, EMC...). This activity concerns the design of a test system which facilitates the realization and exploitation of qualification tests for all kind of circuits, from a simple register bench to complex components such as processors.

Screening tests are mandatory to predict error rates. They consist in exposing the studied parts, eventually operating in vacuum, to simulated stress conditions. The hardware and software developments related with such tests must take into account the random nature of event occurrence, both in time and space. On one hand this entails on-line error detection, on the other hand this makes mandatory the need for development of ad hoc hardware mechanisms related with critical errors detection (sequencing loss, system crashes, latchups) and recovering. Most of commercially available functional testers have these capabilities, potentially offering a powerful solution to qualification test implementation for all circuit types. Nevertheless, two main drawbacks must be mentioned:

- Functional testers cannot fit inside most of vacuum chambers available at generally used radiation facilities. The alternative consisting in using them outside the chamber connected to the device under test (DUT) inside the enclosure, may lead to serious signal propagation problems,
- Test stimuli are defined by a set of binary patterns corresponding to circuit pins values at each clock period. For complex circuits (processors for instance) the development and debugging at this low-level of such test programs can be a difficult task. Note that these constraints may also apply for testing under other type of conditions such as temperature, magnetic perturbation, vibrations, or other type of harsh environments.

Since 1988 we have been collaborating with different European and American space agencies in projects aiming at the study of the behavior under radiation of circuits devoted to space applications. Our role was the development of the hardware and software aspects of the test under radiation of candidate circuits. Experiments were performed by means of a family of dedicated testers we designed and realized to cope with radiation testing requirements. The use of these testers for a wide range of circuits, including memories, general-purpose processors and dedicated processors, pointed out their capabilities for the qualification of complex digital ICs, but their adaptation to test a new device needs some hardware development, limited to the architecture of the Device Under Test (DUT) daughter-board. Even if such architectures are not too complex and follow quite close the basic principles of block diagrams exposed in the DUT's datasheet, the experience proved us that their development needed specialized skills constituting thus the main obstacle to easily "export" our tester concept to other teams.

In the past we have prototyped different versions of a dedicated test system having the following characteristics:

- The DUT operates in its "natural" digital environment, i.e. it is interfaced to a typical architecture. When the DUT is a processor, such architecture includes memories to store the boot and test programs, glue logic and needed power and clock circuitry. Instead of test vectors that mimic the activity of input pins at each clock cycle, during the test stimuli is applied to the processor under study as the result of the execution of a program stored in a suitable memory. Test results are stored in the memory as a byte sequence.
- An external board provides the interface with the user and controls the operation of the architecture built around the DUT.
- The whole system (DUT board and control board) communicates through a serial link with a computer for user's control of the experiment.

The last version of such a platform, called ASTERICS (Advanced System for the TEst under Radiation of Integrated Circuits and Systems), was designed to deal with the following requirements:

- The whole system must have a size allowing to entirely fitting it in enclosures commonly used for environmental qualification tests.
- The DUT must be tested on-line, operating in nominal conditions.
- The system should allow to exercise as many circuits (among candidates to a given project for instance) as possible, to avoid waste of time/money consequence of delays provoked by operating the facilities used to simulate the studied environment.
- Capability for the tester to be remotely controlled anywhere in the world through the internet network.
The ASTERICS system developed at TIMA/ARIS allows coping with these requirements. A block diagram is given in Figure 3.

The efficiency of this tester’s architecture was proved by various cooperations with space agencies aiming at performing the test under radiation of processors candidate to their applications. As a significant example, it can be mentioned the use of the previous version, the so-called THESIC+, by JPL/NASA for the study of the behavior under heavy ions of the PPC750, a complex processor candidate to be included in the electronic equipments of a satellite. This architecture has also been used to test the ATMEL AT697 radiation hardened microprocessor.

The new ASTERICS test platform constitutes a powerful tool with generic capabilities for the qualification of digital circuits. The idea is to implement the whole DUT board architecture by means of an FPGA whose configuration is obtained from compiling the description of key features of the DUT in a hardware description language such as VHDL or Verilog. In this way, there is only a minor hardware development, limited to wiring the DUT pins to the ones of the tester connector. The architecture of ASTERICS is mainly composed of:

- A Xilinx Virtex4FX FPGA, containing a PowerPC hardware processor, having in charge the following tasks: it controls the circuit to qualify, runs on and off the test sequences and monitors the latchup circuit. It is also able to transfer test programs and to gather test results from the component being studied to/from the PC user interface via an Ethernet 10/100/1000 link. A second FPGA used as a chipset and several static and dynamic memory banks are also included in the board: a 32Mb SRAM memory organized in 2 banks of 512k*32bits (which should allow the test of advanced 64-bits processors) and 512Mb of DDR-SDRAM (16Mx32bits) to enable fast and efficient processor tests. To cope with a wide range of DUTs, all these memory banks are managed by the FPGA of ASTERICS's motherboard. We have chosen for this device a Virtex4LX FPGA from Xilinx which is optimized for high-performance logic. It is multi-volt Input/Outputs compliant, that means it can drive signals in 3.3, 2.5, 1.8, 1.5 and 1.2 Volts, reducing the number of components needed to interface the DUT. The FPGA must be properly configured in order to assign the interface board resources to the device under test. The Control FPGA is also capable to configure the Chipset FPGA through its JTAG port avoiding the use of a dedicated Xilinx programmer.

- The DUT board (called “daughter-board” in the previous tester) comprises exclusively the component to test and, in some cases voltage regulators.

Obviously, a computer is also needed in ATERICS as a user’s interface. It allows the on-line control of test operations, the display of results and their storage in a mass memory in convenient formats for future analysis. It is important to notice that this computer can be located anywhere in the world, ensuring the remote control through internet. A particular effort was invested on the development of a friendly and powerful user interface capable to provide the operator with on-line test result data.
The TIMA’s ASTERICS platform will be used to test under heavy ions and neutrons, in cooperation between iRoc, CNES and E2V, a complex processor (PowerPC). This study is done in the frame of the SCADRI project performed in the frame of Rhône Alpes CLUSTER AERONAUTIQUE).

6.4 Predicting SEU error rates from Radiation Ground Testing and Fault Injection

Members: R. Velazco, P. Peronnard, G. Foucard

When estimating the sensitivity to radiation of an integrated circuit the goal is to evaluate the average number of impinging particles required to provoke a fault. Main considered faults for advanced ICs are SE (Single Event Upset), MBU (Multiple Bit Upset), MCU (Multiple Cell Upset and SEFI (Single Event Functional Interrupt). This can be achieved by means of fault injection techniques, but in all the cases is required a measure of the intrinsic sensitivity of the target circuit to the considered Single Event.

\[ \sigma \] is called the interaction cross-section and is a direct measure of the IC sensitivity. Its unit is the cm² or it is expressed in barn (1 barn = \( 10^{-24} \) cm²). Generally \( \sigma \) is given as an interaction cross-section per device (or per bit).

\[
\sigma_{dev} = \frac{\# \text{of single event recorded during the experiment}}{\text{fluence of the experiment}}
\]

\[
\sigma_{bit} = \frac{\# \text{of single event recorded during the experiment}}{\text{fluence of the experiment} \times \# \text{of bits}}
\]

As a consequence, the end-product of a radiation ground testing will be a plot of the interaction cross-section versus particle energy (measured in terms of Linear Energy Transfer or LET which is the energy transferred to the Silicon during by the particle.

Processors are included in most of the architectures devoted to embedded systems. The determination of SEU cross-section of microprocessor’s memory elements requires the use of a so-called static test which consists in exposing the device to a suitable particle flux while the content of the DUT’s registers and memory elements are observed. This is usually attained by executing a test program in charge of initializing these memories and dumping their content after a given period of time. The usually obtained measure, called cross-section (the number observed bit flips divided by the number of incident particles) is used to predict the final error-rate of the tested device in a given harsh environment. However it has been shown that the measured static cross-section can significantly overestimate the one the circuit while it executes a real application. The reason is simple: while a test program is written to maximize the number of errors observed, a real application is not. Moreover, many memory bits are not used, or are refreshed so often that SEUs in these regions have no impact on the system's behavior.

Fault injection may helps in predicting the behavior of a real program which would be used for the final application. It was demonstrated by many experiments that the final cross section of an application executed by a processor can be obtained by multiplying the static cross-section with the error rate obtained during fault injection. The key point is how to perform a fault injection campaign where instants and location of injected faults match the ones of faults occurring when the application will operate in the final environment.

Fault Injection strategies can be classified in two families: software based and hardware based. Among software based ones, depending on the available DUT description level, can mentioned:

• SPICE based fault injection, if a SPICE net-list is available;
• VHDL / Verilog fault injection when a behavioral or RTL description does exist;
• ISS based fault injection if an Instruction Set Simulator is available.

Hardware based fault injection requires a physical device, and faults can be injected using:

• FPGA based fault injection, if a RTL description is available and mapped to an FPGA;
• The CEU (Code Emulated Upset) method, based in the random activation of interrupt signals.

An extended version of the CEU fault injection methodology, published by ARIS for the first time in 2000, able to target cache memories as well as register files was explored in the frame of SCADRI project (project from Rhone-Alpes Aeronautic Cluster) targeting two consecutive generation of advanced processors: the Power PC
7447 and 7448. Basically, it consists in triggering an interrupt while the processor is running. When the DUT receives the interrupt, it transfers the control from the executed benchmark to a trap handler. This handler then flips the content of a randomly chosen bit and resumes the benchmark execution. Obtained results proved that the predicted error rate fit very well the measured ones. Radiation ground testing results were gathered during experiments performed at Louvain-La-Neuve heavy ions facility. We used the resulting cross-sections and flux settings as inputs to our fault injection set-up. Outputs of the fault injection experiments were analyzed with exactly the same tools used to analyze the radiation ground test results. At the 95% confidence level, there was no disagreement. The test set-up cannot see differences between SEU induced by radiations and SEU-like faults injected.

As a conclusion, given a cross-section measured beforehand and a particle flux, this technique allows to correctly reproducing the upsets arrival times of a real radiation ground based test. Moreover, it provides the user with an estimation of its own accuracy at the 95% confidence level. Once the underlying cross-section of the microprocessor memory elements has been obtained by radiation ground testing, this method can be used to study with a good accuracy the behavior of any other application without running it under radiation.

6.5 Design time behavioural level analysis of soft error consequences in complex digital circuits

Members: R. Leveugle, P. Maistri, P. Vanhauwaert, J. B. Ferron, L. Anghel, R. Clavel (VDS), L. Pierre (VDS)

Significant effort was targeted during the last years on developing efficient techniques to analyze at design time the functional consequences of soft errors. The goal is to precisely identify the soft errors leading to unacceptable application disturbances, in spite of all the possible masking effects due to the circuit architecture (redundancy, performance-oriented features, etc.) or to the application characteristics (meaningless computations in a parallel structure, meaningless precision of some data, etc.). Targeted circuits have essentially been synchronous digital circuits. The analysis is carried out as soon as a functional model of the circuit or system is available, so that necessary corrections can be made early in the design flow. Most of the techniques, developed since more than ten years in the team, start from synthesizable RTL descriptions. Such descriptions are already close to the final hardware in terms of cycle accuracy and in terms of memory cells identification. Higher level descriptions may in some cases be used, with limited representation of soft error locations and reduced accuracy in terms of propagation analysis.

All early robustness evaluations do not seek the same kind of answer. This point is important, because some techniques may be very efficient with respect to some outcomes, but completely inadequate with respect to others. The main types of outcomes that can be expected are:

- classification of faults/errors – Injected faults or errors are classified with respect to a list of potential effects defined by the designer. These effects may include application failure modes, error tolerance or detection (when mechanisms exist), or just nothing (silent errors, without any consequence on the application). Such a classification can be used to evaluate the intrinsic robustness level of a circuit and/or to validate the protection mechanisms implemented in the circuit.

- quantification of derating factors – Evaluating timing and architectural derating factors corresponds to identifying the fraction of the errors having no impact on the system behaviour.

- identification of error propagation paths – Classifying the errors does not give any insight into how they propagate within the circuit from their origin to the recorded effect. In order to identify the best positions in the circuit where protection must be added it is necessary to make a more detailed analysis of the error propagation from the original soft error up to the activated failure mode.

- identification of critical locations – When selective (or "pragmatic") hardening is the goal, the identification of error propagation paths allows the designer to pinpoint efficient locations where propagations can be stopped. Another possibility is to avoid using sensitive cells to implement registers that may be the origin of the most critical consequences (e.g. using specific hardened flip-flops on those locations). In that case, it is necessary to order the list of flip-flops with respect to the probability that an error in them will result in a critical event for the application. This will be called flip-flop or register grading.
proof of a given set of properties – In that case, an expected system property and/or the efficiency of detection or tolerance mechanisms must be guaranteed for all errors in the expected error set.

A lot of work was done in our team on fault injection techniques, based on simulation, then emulation. These techniques can be used for all expected outcomes. However, the main limitation is the huge amount of time required to run the experiments when many faults have to be injected in a complex circuit running a long workload. Using hardware emulation leads to noticeable time savings, and we have developed during the last years efficient injection platforms based on SoPCs (System on Programmable Chip). This platform takes advantage of the processor core integrated in the SoPC to reduce the quantity of data exchanges with the host computer, thus accelerating the experiments, while maintaining the largest flexibility with respect to the type of possible dependability analyses. Unfortunately, even with such an acceleration, exhaustive fault injections often remain unaffordable in a reasonable time.

This leads in most cases to perform only partial analyses based on a randomly (and often arbitrarily) selected set of faults or errors. Such a statistical fault injection (SFI) has been very extensively used in the literature but the margin of error on the results given on such a basis was unknown. We have therefore proposed and validated in 2008 an approach to quantify the error on the results with a given confidence level, or conversely to evaluate the number of injections to perform in order to achieve a given error/confidence level. The method will in particular be presented at the DATE Conference in 2009.

SFI can then be very useful in doing quick classification or derating factor estimations, with a controlled margin of error. Unfortunately, this approach does not address all possible expected outcomes of a fault injection campaign. In the case of a large number of potential errors and workload cycles, only a very small proportion of the registers are actually perturbed at a few cycles. This means that such results cannot help in identifying the most critical registers or clock cycles. Flip-flop grading remains possible when the random selection is only used to reduce the number of injection cycles in each flip-flop; however, in that case, the efficiency of SFI is noticeably reduced and the required number of experiments remains very large. Error propagation paths are also only partially exercised, so decisions on the best hardening positions are hard to make. Finally, SFI cannot guarantee that a given property always holds; this can at best be assessed with a given margin of error.

Several complementary approaches are therefore currently under study in order to more efficiently obtain some expected outcomes.

An approach based on Timed Petri Net models has been proposed and evaluated. It has been shown that this type of model can efficiently identify some harmless errors even in the case of architectures difficult to analyze with classical fault pruning techniques. Such models can therefore be used to reduce the number of injection experiments. They can also help in grading the criticality of the flip-flops in a circuit. At medium term, we plan to develop an environment allowing a designer to automatically generate such models from available circuit descriptions (synthesizable RTL or netlists). The extension of the approach towards error propagation analysis is also under consideration. This will be complementary to probabilistic propagation analyses, another approach under study in the team. One of the important aspects will be to make a compositional approach possible, so that results obtained at block level can be directly re-used to evaluate the dependability of a complex circuit.

Another study targets the proof of properties even in presence of faults. This follows 2005 experiments based on formal property checking. The current study is done in collaboration with the VDS group in TIMA and the LIP6 laboratory, in the frame of the FME3 project, supported in the period 2008-2010 by the French national research agency (ANR). Model checking techniques and theorem provers are currently experimented. In particular, an approach has been developed to efficiently model the effect of single or multiple bit errors and prove properties in presence of such errors with the ACL2 theorem prover.

The specific case of configuration errors in SRAM-based FPGAs is also addressed. A tool allowing a designer to analyze the effect of faults in the configuration of a Virtex II FPGA had been developed and has been extended within the MEDEA+ Parachute project to analyze Atmel FPGAs. The tool can be used to analyze the effect of attacks on such a reconfigurable platform. This has been done in particular for several attack campaigns using power glitches and several types of lasers. Such analyses lead to better understand the type of perturbations induced by attacks and to determine more realistic error models. It has also been shown on Virtex II that the probability to flip a configuration bit noticeably depends on the fault-free value of this bit (publication at VTS in 2009). For a given design, and therefore a given configuration bitstream, the configuration bits can be classified

- proof of a given set of properties – In that case, an expected system property and/or the efficiency of detection or tolerance mechanisms must be guaranteed for all errors in the expected error set.

A lot of work was done in our team on fault injection techniques, based on simulation, then emulation. These techniques can be used for all expected outcomes. However, the main limitation is the huge amount of time required to run the experiments when many faults have to be injected in a complex circuit running a long workload. Using hardware emulation leads to noticeable time savings, and we have developed during the last years efficient injection platforms based on SoPCs (System on Programmable Chip). This platform takes advantage of the processor core integrated in the SoPC to reduce the quantity of data exchanges with the host computer, thus accelerating the experiments, while maintaining the largest flexibility with respect to the type of possible dependability analyses. Unfortunately, even with such an acceleration, exhaustive fault injections often remain unaffordable in a reasonable time.

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SFI can then be very useful in doing quick classification or derating factor estimations, with a controlled margin of error. Unfortunately, this approach does not address all possible expected outcomes of a fault injection campaign. In the case of a large number of potential errors and workload cycles, only a very small proportion of the registers are actually perturbed at a few cycles. This means that such results cannot help in identifying the most critical registers or clock cycles. Flip-flop grading remains possible when the random selection is only used to reduce the number of injection cycles in each flip-flop; however, in that case, the efficiency of SFI is noticeably reduced and the required number of experiments remains very large. Error propagation paths are also only partially exercised, so decisions on the best hardening positions are hard to make. Finally, SFI cannot guarantee that a given property always holds; this can at best be assessed with a given margin of error.

Several complementary approaches are therefore currently under study in order to more efficiently obtain some expected outcomes.

An approach based on Timed Petri Net models has been proposed and evaluated. It has been shown that this type of model can efficiently identify some harmless errors even in the case of architectures difficult to analyze with classical fault pruning techniques. Such models can therefore be used to reduce the number of injection experiments. They can also help in grading the criticality of the flip-flops in a circuit. At medium term, we plan to develop an environment allowing a designer to automatically generate such models from available circuit descriptions (synthesizable RTL or netlists). The extension of the approach towards error propagation analysis is also under consideration. This will be complementary to probabilistic propagation analyses, another approach under study in the team. One of the important aspects will be to make a compositional approach possible, so that results obtained at block level can be directly re-used to evaluate the dependability of a complex circuit.

Another study targets the proof of properties even in presence of faults. This follows 2005 experiments based on formal property checking. The current study is done in collaboration with the VDS group in TIMA and the LIP6 laboratory, in the frame of the FME3 project, supported in the period 2008-2010 by the French national research agency (ANR). Model checking techniques and theorem provers are currently experimented. In particular, an approach has been developed to efficiently model the effect of single or multiple bit errors and prove properties in presence of such errors with the ACL2 theorem prover.

The specific case of configuration errors in SRAM-based FPGAs is also addressed. A tool allowing a designer to analyze the effect of faults in the configuration of a Virtex II FPGA had been developed and has been extended within the MEDEA+ Parachute project to analyze Atmel FPGAs. The tool can be used to analyze the effect of attacks on such a reconfigurable platform. This has been done in particular for several attack campaigns using power glitches and several types of lasers. Such analyses lead to better understand the type of perturbations induced by attacks and to determine more realistic error models. It has also been shown on Virtex II that the probability to flip a configuration bit noticeably depends on the fault-free value of this bit (publication at VTS in 2009). For a given design, and therefore a given configuration bitstream, the configuration bits can be classified
at design time as critical, transparent or suspect (CTS classification). Transparent bits correspond to bits whose value cannot impact the expected functionality; errors in these bits are therefore harmless. Suspect bits correspond to bits whose impact depends on the propagated data or on the configuration of other FPGA cells. Algorithms have been developed to reduce the size of this set of bits; they are currently being implemented in the tool. Results of injections by laser have been used to validate the current classification determined by the tool and the refinement obtained with the new algorithms will be evaluated in 2009. This approach is complementary to the experimental approach described in section 2.9.

6.6 Multi-level hardening of integrated embedded system for safety/availability and security

Members: R. Leveugle, P. Maistri, L. Anghel, G. Canivet, V. Maingot, J. B. Ferron

The goal of this project is to develop methods, libraries and tools to design robust integrated embedded systems. These systems must be able to cope with both natural faults and security-related fault-based attacks. Protections against fault-based attacks are evaluated with respect to their fault detection/tolerance capability, but also with respect to their potential impact on the robustness against side-channels attacks. The protection mechanisms are studied at several levels: logic, architecture, operating system and software. Complementary approaches are considered to provide a complete toolbox to a designer.

The first approach is the development of robust versions of processor or coprocessor cores. In particular, robust versions of the Leon2 processor and of an AES cryptographic coprocessor have been designed. The DDR scheme used for the AES has been published in the IEEE Transactions on Computers in 2008 and attacks on a FPGA-based prototype are on-going. Modifications of the eCoS real-time operating system had also been defined to provide low-cost fault tolerance and an embedded system demonstrator was developed, implemented on a Xilinx Virtex II Pro development board.

In addition to the development of hardening techniques and hardened IPs, a study has aimed at evaluating the impact of fault-oriented protections on leakage information. As a matter of fact, in the security context, it is useless to protect a circuit against only one type of attack, since a hacker could use several approaches to obtain secret information. Fault-based attacks are one type of threats. Another one is the use of so-called "side channels", and in particular the power consumption or the electromagnetic emissions, to infer some confidential data used during a computation. It is therefore very important to ensure that protections against fault-based attacks do not facilitate an attack using the side channels (and vice-versa). Results were obtained in the frame of the MARS project (2004-2007), part of the program "ACI Sécurité & Informatique" supported by the French Ministry of Research. Complementary experiments made in 2008 have in particular shown that the implementation of error detecting or correcting codes in a circuit does not have a very strong impact on the sensitivity to power-based (DPA) attacks. However, the code check bits can be attacked as well as the original data bits. Also, the combinatorial logic in the circuit has a significant influence on the circuit DPA sensitivity. Finally, error correcting codes may be interesting, not to achieve error correction (the probability of a correction in case of multiple errors is low) but to increase error detection and (slightly) reduce the DPA sensitivity.

Another important aspect when designing a secure circuit is the impact of the Design for Test (DfT) approaches (scanpath insertion, boundary scan, …) on the circuit robustness. DfT aims at increasing the level of observability and controllability that is just the opposite of the security constraints. We have therefore evaluated an approach based on Software-based BIST (also called SBST), to achieve better compatibility between testability and security. The main conclusion is that the approach can allow very cheap self-test of an AES core in a system including a main processor, but achieving 100% fault coverage can be difficult and the protections implemented in the cryptographic core against fault-based attacks can still reduce the achieved fault coverage.

Due to the increasing spatial multiplicity of error patterns, protecting a circuit with information redundancy is more and more difficult. Another approach consists in using functional checks. In this context, we have developed in 2008 a new control-flow checking technique. This technique is non-intrusive and does not require a modification of the initial microprocessor-based system. Checks include not only the control flow itself, but also the integrity verification of critical data, with several possible trade-offs between overheads and error detection. The approach is compatible with the norms requiring a complete separation between the nominal functions and the checking features (e.g. for automotive applications). This technique will be evaluated on a prototype in 2009.
Finally, studies are on-going on the problems related to errors in SRAM-based FPGAs. The goal is to propose specific design techniques to achieve robustness at lower cost than the classical massive redundancy approach.

6.7 Towards robust nanoelectronics design

Members: L. Anghel, T. Dang, R. Leveugle

Some work has started in 2000 on the implementation of logic circuits using nanoelectronic devices. This project had been initially defined in collaboration with CEA/LETI and aimed at taking advantage of silicon-based single-electron transistors (SETs). A study of the state-of-the-art had been performed, including the study of simple logic and arithmetic components and some expertise of the simulation approaches available for such devices. More recently, the use of carbon nanotube transistors (CNTFETs) has been considered. Between 2004 and 2007, our work in this area was part of the NANOSYS project, started in the framework of the program "ACI Nanosciences" supported by the French Ministry of Research, in collaboration with many French research teams.

The work aimed at proposing solutions to implement robust logic elements based on these components. This implies defect tolerance due to the expected high density of manufacturing defects, as well as fault tolerance to cope with other problems such as process parameter variability and transient faults. The work was based on CNTFET simulation models provided by Nanosys partners. These models have been used to compare the characteristics of a set of logic gate structures. Dispersion analysis has been done on some logic gates, showing that very small variations in the diameter of carbon nanotubes, or other physical parameter may lead to important dispersion of static characteristics of analyzed gates. Dynamic behaviour has also been studied and a tool for random defects injection has been developed. Finally, the robustness of redundant structures has been evaluated. These results have been summarized in the PhD dissertation of Trinh Dang.

6.8 Multiple Defects Tolerant Devices for Unreliable Future Nanotechnologies

Members: L. Anghel, C. Lazzari, M. Nicolaidis

Nanotechnology solutions point at the horizon with the sophistication of the chemical synthesis processes, making possible to synthesize chemically electronic components and their interconnections, to create very complex systems at low cost. These solutions are today needed to surmount technical barriers (high leakage currents, signal integrity, power density, small node storage capacities, ...) but also economical barriers (e.g. excessive cost expected for the fab-lines of future CMOS process generations). Although most of the new nanoelectronic solutions (e.g. single electron devices, quantum cellular automata, carbon nanotubes, molecular components, semiconductor nanowires, chemically assembled electronic nanocomputers (CAEN) ) are still in the research domain, significant improvements have been done in assembling them into logic gates and memory arrays to compute very complex computational systems with a much higher integration density than in nowadays CMOS, lower power consumption and higher speed. It is forecasted that these systems would integrate hundreds of billion devices in regular networks.

However, for such a densely integrated circuit to perform a useful computation, it has to deal with the inaccuracies and instabilities introduced by fabrication processes and the tiny devices themselves. Permanent faults occurring during fabrication are intimately related to the process used to fabricate the structures of a design. Different fabrication processes will result on different defect densities. For instance, if the product is fabricated by chemically synthesis of the components and interconnections, the defect densities related to such a process could be very high. On the other hand, transient faults are determined by the environment, physics and the devices operation conditions, which are not necessarily related on the way they are fabricated. Future nanoelectronic architectures have to be able to tolerate an extremely large number of defects and faults. Today it is not known which will be the nanotechnologies that will be adopted in the future to build complex computational systems, and in addition we do not know exactly which will be the causes of transient and permanent faults.

Although recent research has resulted in the development of basic logic elements and simple circuits in nanoscale, there are still debates on what logic style and architecture will be the best for nanocomputers. For most of the solutions proposed in the literature it is predicted that the defect densities could be as high as $10^2$, which could be seen as a few defective cells for every 100 memory cells.

The design of defect-tolerant architectures for the ultra-large integration of highly unreliable nanometer devices is therefore inevitable.
However, new fault tolerant design paradigm is needed, since with these high defect densities both the regular resources and the redundant ones will be affected by the defects, disabling the basic principle of traditional fault tolerance (use of a fault-free redundant unit to perform the job of a faulty regular unit). Several approaches have been proposed in the last 3 years in TIMA laboratory, dealing with self repairing memory architectures for high defect.

Today there is an increasing interest in using hardware redundancy to mask faulty behavior in nanoelectronic components. Two of improved versions of von Neumann multiplexing gates are currently under research as well as a multiple defects tolerance techniques at transistor and logic level that can apply to any logic gate including flip flops and memory elements.

6.9 Experimental radiation qualification of SRAM-based FPGAs

Members: G. Foucard , A. Bocquillon, R. Velazco

The increasing popularity of low-cost safety-critical computer-based applications in a large scope of areas (such as space and avionic's applications, automotive, biomedical, telecontrol, etc.) requires the availability of new circuits and methods for designing dependable systems. In particular, in the areas where computer-based dependable systems are currently being introduced, the cost (and hence the design and development time) is often a major concern, and the adoption of commercial reconfigurable hardware, such as SRAM-based FPGAs (Field Programmable Gate Arrays) is a common practice. As a result software implemented fault tolerance is an attractive solution for this class of applications, since it allows the implementation of dependable systems without incurring the high costs coming from designing custom hardware or using hardware redundancy.

Despite these attractive characteristics, designers are reluctant to use these components for critical applications due to their sensitivity to Single Event Upsets (SEUs) provoked by radiations. Indeed an energetic particle hitting a memory cell may induce a modification of its content (bit-flip). All SRAM-based FPGA resources are controlled by its configuration memory, an SEU in this area may thus change the original behavior of the application. Moreover a fault affecting this memory is permanent until the device is configurated again.

Quantifying the sensitivity of the configuration memory is therefore mandatory in order to evaluate the sensitivity of a specific application. This project focuses on the methods and tools to evaluate the sensitivity to radiation of applications implemented in the target FPGA. Experiments must be performed using radiation facilities (particle accelerators, laser systems,…) to inject faults in the target device and quantify the error rate of the studied application.

The Virtex II FPGA was used as a demonstrator for this project. Two complementary facilities were used: the HIF Cyclotron and a pulsed laser. The firstone allowed to put in evidence the significant contribution of the SRAM configuration memory to the sensitivity of any application implemented on a SRAM-based FPGA. The static-cross section was obtained and is presently used to explore the obtention of the dynamic cross-section by fault injection. The laser experiments allowed to identify potential single-point failures of fault tolerant techniques, this by exhaustive mapping of selected area in which faults are injected with step by step (in our case with a 1 micron step) in the configuration memory.

This project is done in collaboration with IMS laboratory (Bordeaux), EADS (Suresne).and UCL (Université Catholique de Louvain-la-Neuve).
6.10 Hardened memory cells

Members: L. Anghel, M. Nicolaidis, R. Velazco

Radiation-induced transient effects in silicon CMOS circuits are essentially charge collection and transport phenomena resulting from direct ionization. The collected charges may inadvertently change, for short time intervals, the internal node voltages of the circuit (single event upset). These transients may change the electrical behavior of the MOS transistors in digital and analog circuits.

Design hardening techniques at circuit level can be developed to achieve immunity to upsets. A lot of hardened-by-design memory elements have been proposed in the last years. In 1994 and 1997 were developed two hardened cells in TIMA laboratory, so-called, HIT2 (Heavy Ion Tolerant cell) and DICE (Dual Interlocked Cell) respectively. The philosophy was to strengthen the feedback of the cell in order to restore the data potentially corrupted by the impact of a charged particle. However, the price to pay is an increase of the cell area as well as higher power consumption. A recently developed hardened memory cell is under evaluation at TIMA/ARIS. The new architecture includes extra transistors to introduce means to delay the transient signal from the feedback path, thus avoiding the appearance of the SEU.

The performances of different kinds of SRAM cells built using the same CMOS technology will be compared.

6.11 Low-cost Single Event Latchup Mitigation Architecture for Memories

Members: M. Nicolaidis (in collaboration with CMP)

Existing single event latchup (SEL) mitigation approaches include process level mitigation, which is very often undesirable as it may costly and/or affect circuit performance; insertion of guard ring structures, which increase significantly area and may also impact performance; power recycling which removes latchup but destroys circuit state. The proposed scheme combines Error Control codes, usually used for mitigating SEUs, and sleep transistors, usually used to reduce power, in an original architecture that enables:

- latchup effect containment,
- latchup detection,
- latchup elimination,
- correction of latchup induced errors.
The resulting architecture is fully protected against SELs without affecting system operation, and induces insignificant area, performance and power penalties.

6.12 Fault Tolerant Architectures for Mitigating the Flaws of Nanometric Technologies

*Members: L. Anghel, M. Nicolaidis, C. Rusu, H. Yu, N. Zergainoh*

Silicon-based CMOS technologies are fast approaching their ultimate limits. By approaching these limits, power dissipation, fabrication yield, and reliability worsen steadily making further nanometric scaling increasingly difficult. These problems would stop further scaling of silicon-based CMOS technologies at channel lengths between 10 and 20 nm. But even before reaching these limits, these problems could become show-stoppers unless new techniques are introduced to maintain acceptable levels of power dissipation, yield and reliability. Fault tolerant design is a powerful solution for improving reliability and yield. However, traditional fault-tolerant architectures incur very high cost in terms of silicon area and power penalty. High area cost reduces their interest for commercial applications, while high power penalty makes them unacceptable in terms of battery life in portable devices and in terms of power density constraints in nanometric process nodes. In this work we develop innovative time-redundancy based fault-tolerant architectures able to mitigate the effects of faults induced by variability (process, temperature and voltage), circuit aging, EM interferences and ionizing particles. Due to their innovative principles, these architectures incur very low area and power penalty. Their combination with a dynamic frequency-voltage scaling approach allows operating at very low voltage, enabling significant power dissipation reduction.

6.13 Combining Circuit-level Fault Tolerance with OS-level Scheduling for Efficient DFVS

*Members: G. Bizot, M. Nicolaidis, N. Zergainoh*

Circuit-level error detection signals are monitored to adapt frequency, voltage and body biasing to the application requirements and circuit delay degradation induced by variability, EMI and aging.

6.14 Computing Architectures for Nanotechnologies

*Members: L. Anghel, M. Nicolaidis, N. Zergainoh*

Silicon-based CMOS technologies are predicted to reach their ultimate limits by the end of the next decade. Research on nanotechnologies is actively conducted in a world-wide effort to develop new technologies able to maintain the Moore’s law. They promise revolutionizing the computing systems by integrating tremendous numbers of devices at low cost. These trends will provide new computing opportunities and will have a profound impact on the architectures of computing systems. This work describes architectures able to exploit the extraordinary computing power promised by nanotechnologies in order to model and simulate complex natural or artificial systems composed of huge numbers of simple elements.
7. Members of TIMA

Table 1 lists researchers, Ph D. students, engineers and clerical staff present in the TIMA Laboratory in 2008. Table 2 lists the invited researchers. Table 3 lists the interns and trainees, including MSc students.

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<td>Quentin</td>
<td>Ph D. student</td>
</tr>
<tr>
<td>MIAN QAISSAR</td>
<td>Saeed</td>
<td>Ph D. student</td>
</tr>
<tr>
<td>MIR</td>
<td>Salvador</td>
<td>CR - CNRS</td>
</tr>
<tr>
<td>MORIN-ALLORY</td>
<td>Katell</td>
<td>Associate Professor – INPG/PHELMA</td>
</tr>
<tr>
<td>MULLER</td>
<td>Olivier</td>
<td>Associate Professor – INPG/ENSIMAG</td>
</tr>
<tr>
<td>NGUYEN</td>
<td>Hoang Nam</td>
<td>Ph D. student</td>
</tr>
<tr>
<td>NICOLAIDIS</td>
<td>Mihail</td>
<td>DR - CNRS</td>
</tr>
<tr>
<td>ODDOS</td>
<td>Yann</td>
<td>Ph D. student</td>
</tr>
<tr>
<td>OUCHET</td>
<td>Florent</td>
<td>Ph D. student</td>
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<tr>
<td>PAUGNAT</td>
<td>Franck</td>
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<td>PERONNARD</td>
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<tr>
<td>PETROTT</td>
<td>Frédéric</td>
<td>Professor – INPG/ENSIMAG</td>
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<tr>
<td>PIERRE</td>
<td>Laurence</td>
<td>Professor – UJF/IMA</td>
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<td>POPOVICI</td>
<td>Katalin</td>
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<tr>
<td>PORCHER</td>
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<tr>
<td>POSSAMAI BASTOS</td>
<td>Rodrigo</td>
<td>Ph D. student</td>
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<tr>
<td>RAHMOUNI</td>
<td>Khaled</td>
<td>CIFRE Ph D. student</td>
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<tr>
<td>RASLAN</td>
<td>Zahy</td>
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<tr>
<td>RIOS</td>
<td>David</td>
<td>Ph D. student</td>
</tr>
<tr>
<td>ROUSSEAU</td>
<td>Frédéric</td>
<td>Professor- UJF/POLYTECH</td>
</tr>
<tr>
<td>RUFSER</td>
<td>Libor</td>
<td>Contracted Researcher</td>
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<td>RUSU</td>
<td>Claudia</td>
<td>Ph D. student</td>
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<tr>
<td>SAHNINE</td>
<td>Chawki</td>
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</tr>
<tr>
<td>SALIZZONI</td>
<td>Marie-Christine</td>
<td>Contracted Accountant</td>
</tr>
<tr>
<td>SENOUCI</td>
<td>Benaoumeur</td>
<td>Ph D. student</td>
</tr>
</tbody>
</table>
### Members of TIMA

<table>
<thead>
<tr>
<th>NAME</th>
<th>FIRST NAME</th>
<th>COUNTRY</th>
<th>Position/Institution</th>
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<td>SHEIBANYRAD</td>
<td>Hamed</td>
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<td>Post-Doc</td>
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<td>SHEN</td>
<td>Hao</td>
<td></td>
<td>Ph D. student</td>
</tr>
<tr>
<td>SICARD</td>
<td>Gilles</td>
<td></td>
<td>Associate Prof. – UJF/UFR Physique</td>
</tr>
<tr>
<td>SIMEU</td>
<td>Emmanuel</td>
<td></td>
<td>Associate Prof. – UJF/POLYTECH</td>
</tr>
<tr>
<td>STRATIGOPoulos</td>
<td>Haralamos</td>
<td></td>
<td>CR CNRS</td>
</tr>
<tr>
<td>TAN</td>
<td>Junyan</td>
<td></td>
<td>Ph D. student</td>
</tr>
<tr>
<td>TONGBONG</td>
<td>JEANNE</td>
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<td>Ph D. student</td>
</tr>
<tr>
<td>TORELLA</td>
<td>Lucie</td>
<td></td>
<td>ADTRF – UJF/POLYTECH</td>
</tr>
<tr>
<td>VANHAUWAERT</td>
<td>Pierre</td>
<td></td>
<td>Ph D. student – Post-Doc</td>
</tr>
<tr>
<td>VELAZCO</td>
<td>Raoul</td>
<td></td>
<td>CR - CNRS</td>
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<tr>
<td>VITTOZ</td>
<td>Stéphane</td>
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<td>Ph D. student</td>
</tr>
<tr>
<td>VITRY</td>
<td>Gérard</td>
<td></td>
<td>IE - CNRS</td>
</tr>
<tr>
<td>YAHYA</td>
<td>Eslam</td>
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<tr>
<td>YANG</td>
<td>Wenbin</td>
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<td>Ph D. student</td>
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<tr>
<td>YOUSSEF</td>
<td>Mohamed Wassim</td>
<td></td>
<td>Post-Doc</td>
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<tr>
<td>YU</td>
<td>Hai</td>
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<td>ZAKARIA</td>
<td>Hatem</td>
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<tr>
<td>ZERGAIHNOH</td>
<td>Nacer-Eddine</td>
<td></td>
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<tr>
<td>ZIMOUCHE</td>
<td>Hakim</td>
<td></td>
<td>Ph D. student</td>
</tr>
</tbody>
</table>

**Table 1 – Members of the Laboratory (for 2008)**

ADTRF = «ADjoint Technique de Recherche et de Formation»
IR = «Ingénieur de Recherche»
DR = «Directeur de Recherche»
CR = «Chargé de Recherche»
IE = «Ingénieur d’Etudes»
CIFRE = Support from ANRT for Industry-University cooperation
EN = Education Nationale
ATER = «Attaché Temporaire d’Enseignement et de Recherche»

### Visitors

<table>
<thead>
<tr>
<th>NAME</th>
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<td>ABOULHAMID</td>
<td>El Mostapha</td>
<td>CANADA</td>
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<tr>
<td>REINSALU</td>
<td>Juri</td>
<td>ESTONIA</td>
<td>1 month</td>
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<tr>
<td>REINSALU</td>
<td>Uljana</td>
<td>ESTONIA</td>
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<tr>
<td>SILVA CARDENAS</td>
<td>Carlos</td>
<td>PERU</td>
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**Table 2 – Visitors (for 2008)**
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<td>Louay</td>
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<tr>
<td>AMHAZ</td>
<td>Hawraa</td>
<td>LEBANON</td>
<td>5 months</td>
</tr>
<tr>
<td>BERGAOUI</td>
<td>Salma</td>
<td>TUNISIA</td>
<td>6 months</td>
</tr>
<tr>
<td>BING</td>
<td>Xue</td>
<td>CHINA</td>
<td>7.5 months</td>
</tr>
<tr>
<td>CATHERINET</td>
<td>Benoît</td>
<td>FRANCE</td>
<td>5 months</td>
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<tr>
<td>CENNI</td>
<td>Fabio</td>
<td>ITALY</td>
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<tr>
<td>CLAVEL</td>
<td>Renaud</td>
<td>FRANCE</td>
<td>7 months</td>
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<tr>
<td>FALL</td>
<td>Diarga</td>
<td>SENEGAL</td>
<td>8 months</td>
</tr>
<tr>
<td>FELLAH</td>
<td>Youssef</td>
<td>ALGERIA</td>
<td>3 months</td>
</tr>
<tr>
<td>FU</td>
<td>Qiang</td>
<td>CHINA</td>
<td>5 months</td>
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<tr>
<td>GOSSET</td>
<td>Etienne</td>
<td>FRANCE</td>
<td>9.5 mois</td>
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<tr>
<td>HEDDE</td>
<td>Damien</td>
<td>FRANCE</td>
<td>6.5 months</td>
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<tr>
<td>HORREIN</td>
<td>Pierre-Henri</td>
<td>FRANCE</td>
<td>7.5 months</td>
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<tr>
<td>HUANG</td>
<td>Ke</td>
<td>CHINA</td>
<td>5 months</td>
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<tr>
<td>KAVUN</td>
<td>Elif</td>
<td>TURKEY</td>
<td>3 months</td>
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<tr>
<td>LABEN</td>
<td>François-Karim</td>
<td>FRANCE</td>
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<tr>
<td>LOUVAT</td>
<td>Mathieu</td>
<td>FRANCE</td>
<td>6 months</td>
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<tr>
<td>MOHSEN</td>
<td>Salah</td>
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<td>NORAZ</td>
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<td>FRANCE</td>
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<td>OUCHET</td>
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<td>PATASKAR</td>
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<tr>
<td>PORCHER</td>
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<td>FRANCE</td>
<td>3 months</td>
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<tr>
<td>POWAZNY</td>
<td>Vincent</td>
<td>FRANCE</td>
<td>6 months</td>
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<tr>
<td>RENNEVILLE</td>
<td>Guybert</td>
<td>FRANCE</td>
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<tr>
<td>SANGARE</td>
<td>Moustapha</td>
<td>GUINEA</td>
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<td>SANI</td>
<td>Awais</td>
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<tr>
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<td>Soha</td>
<td>EGYPT</td>
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<tr>
<td>SESTER</td>
<td>Jérome</td>
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<tr>
<td>SFAXI</td>
<td>Lilia</td>
<td>TUNISIA</td>
<td>6 months</td>
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<tr>
<td>SMIRI</td>
<td>Kamel</td>
<td>TUNISIA</td>
<td>1 month</td>
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<tr>
<td>TOUNSI</td>
<td>Farès</td>
<td>TUNISIA</td>
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<tr>
<td>WALZBERG</td>
<td>Alexandre</td>
<td>FRANCE</td>
<td>2 months</td>
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Table 3 – Trainees (for 2008)
8. Biographies of staff members

**AMBLARD Paul**

**Position:** Associate Professor (Maître de Conférences) at University Joseph Fourier, Grenoble, UFR Informatique et Mathématiques Appliquées

**Education**
- 1984 PhD Computer Science
- 1976 Master of Science in Mathematics

**Past activities**
- October 1997: Joined TIMA Laboratory
- From 1984: Associate Professor at University Joseph Fourier
- From 1973 to 1982: Teacher of Mathematics in secondary school

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**ANGHEL Lorena**

**Position:** Associate Professor (Maître de Conférences) at Phelma(Physique-Electronique-Matériaux) since 2001

**Education**
- 1996: Microelectronic Engineering degree - at Polytechnic University of Bucharest, Romania
- 1997: MS degree in Microelectronics – UPB, Romania
- 2000: PhD in Microelectronics (INP Grenoble)
- 2007: Diploma of “Habilitation à Diriger des Recherches” in EEATS

**Past activities**
- Assistant Professor (ATER) at UJF (Université Joseph Fourier Grenoble) in 2000
- Visitor researcher in Zenasis Technologies, USA, July-October 2005
- Visitor Researcher in Intel Corp, USA, July-October 2005

**Research interests**
- Test and On Line testing, Defect and fault tolerant techniques, computer architecture, nanotechnologies

**Current responsibilities**
- Researcher in the ARIS group,
- Coordinator of ACI-SI project VENUS in collaboration with IMS (Bordeaux, France), 2004-2007.
- Scientific Leader of TIMA in MEDEA+ Parachute European program 2004-2009
- Scientific Leader of TIMA in Catrene 3DIM3 European program 2004-2009
- Program Chair of Design of Circuits and Integrated Systems (DCIS 2008), November, 2008, France
- Program Chair of IEEE Design for Reliability and Variability (DRVW 2008), October 2008, USA
- Program Chair of 4th Summer School on Radiation Effects, December 2008, Florida, USA
- Program Chair of 3rd Summer School on Radiation Effects, Novembre 2007, Buenos Aires, Argentina
- Program Chair of 2nd Summer School on Radiation Effects, Novembre 2006, Sevilla, Spain
- General Chair of 11th International On Line Testing Symposium July 2005, France
BASROUR Skandar

**Position:** Professor in Electronics and Microsystems at Ecole Polytechnique de l'Université de Grenoble (Polytech’G). Electrical Engineering Department (3I)

**Education**
- 1987-1990: PhD in Microelectronics – Université Joseph Fourier de Grenoble
- 1986-1987: DEA in Microelectronics – Université Joseph Fourier de Grenoble
- 1982-1986: Graduated from Ecole Normale Supérieure de Tunisie (Physics and Chemistry)

**Past activities**
- 2001: Assistant Professor in Electronics and Microsystems at the Université de Franche-Comté (Topics: Contribution to the development of the X-ray LIGA technique in France. Development and improvement of the UV LIGA Techniques for the realization of original Microsystems)
- 1991-992: Postdoctoral situation at the Laboratoire de Microstructures et Microélectronique CNRS – Bagneux (Topics: Fabrication and characterization of submicron gated TEGFET's)

BONVILAIN Agnès

**Position:** Associate Professor (Maître de Conférences) in electronics at Ecole Polytechnique de l'Université Joseph Fourier de Grenoble (Polytech’G), Electrical Engineering Department (3I and E2I).

**Education**
- 2002 PhD in control and informatics – Université de Besançon
- 1988 DEA in Control, Informatics and robotics – Université de Besançon

**Past activities**
- September 2005: Joined TIMA Laboratory
- From 1997 to 2002: Researcher in microrobotics at LAB laboratory, Besançon
- From 1993 to 2005: Teacher in electronics in secondary school
- From 1988 to 1993: Engineer head of service in two companies

**Research interests**
- BioMEMS

BORRIONE Dominique

**Position:** Professor at Université Joseph Fourier, Grenoble
- Director of TIMA Laboratory since January 2007

**Education**
- 1981: Doctorat d’Etat in Computer Science, University of Grenoble
- 1976: PhD in Computer Science, University of Grenoble
- 1971: DEA in Computer Science, University of Grenoble
- 1970: B. S. in Applied Mathematics, Aix-Marseille University

**Past activities**
- Director of the ARTEMIS Laboratory (1991-1995)

**Miscellaneous**
- Has served in many Conference and Workshop Committees
- IFIP Silver Core
CHEVROT Frederic

**Position:** Contracted technician with TIMA Laboratory since March 2003

**Education**
- 2001: IUP MIAGE (Méthodes Informatiques Appliquées à la Gestion d'Entreprise). UFR IMA : (Grenoble).
- 1998: DEUG Technologie Industrielle, Université Joseph Fourrier.
- 1995: BAC S Tec

**Current responsibilities**
Assistant System Engineer

COURTOIS Bernard

**Position:** Directeur de Recherches CNRS

**Education**
- 1981: Docteur d'Etat degree
- 1976: Doctor-Engineer degree
- 1973: Engineer degree
- 1968: Baccalaureat degree – Philosophy
- 1967: Baccalaureat degree – Mathematics

**Current responsibilities**
- Director of TIMA Laboratory until December 2006
- Director of CMP Service

**Miscellaneous**
- Has authored or co-authored many scientific papers
- Has served in many Committees of Conferences & Workshops
- Has served as a reviewer of research proposals to CEC, NATO, NSF, SERC
- Doctor Honoris Causa of the Technical University of BUDAPEST
- IEEE Golden Core

FESQUET Laurent

**Position:** Associate Professor (Maître de conférence) at Grenoble INP

**Education**
- 1997: PhD in Electronics – Paul Sabatier University – Toulouse
- 1994: Agrégation (teaching degree) in applied physics, Ecole Normale Supérieure de Cachan
- 1993: Engineering degree in Physics, Ecole Nationale Supérieure de Physique de Strasbourg
- 1993: DEA degree in Photonics – Louis Pasteur University – Strasbourg

**Past activities**
- Research:
- Teaching:
  - 1998-1999: Teacher in charge of physics, electrotechnics and power electronics curses in BTS - Brive
  - 1995-1998: Teacher in electronics at Sup'Aéro and at Paul Sabatier Univeristy - Toulouse
  - 1994-1995: Teacher at the French Navy instruction center in Toulon in charge of electronics and inertial navigation systems lectures

**Current responsibilities**
- Head of the « Concurrent Integrated Systems » research group (CIS)
- Deputy Director of the CIME-Nanotech
**GARNIER Nicolas**

**Position**: Contractual Engineer at TIMA Laboratory since February 2006 and Engineer CNRS since December 2007

**Education**
- 2005 Formation Sécurité des Systèmes et Réseaux, CNRS, Grenoble
- 2003 Maîtrise d'informatique, Université de Savoie, Le Bourget du Lac

**Past Activities**
- November 2004 to February 2006: System Engineer at Laboratoire Modélisation et Calculs, Grenoble

**Current responsibilities**
- System Engineer at TIMA Laboratory

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**GASCARD Eric**

**Position**: Associate Professor with TIMA Laboratory since September 1st, 2003

**Education**
- Ph.D. in Computer Science from University Provence (Aix-Marseille 1), France, 3 July 2002

**Current responsibilities**
- Associate Professor University Joseph Fourier (Grenoble 1), UFR, Polytech'Grenoble, France, since September 1, 2003
LEVEUGLE Régis

**Position:** Professor at Grenoble INP (ENSERG), vice-director of TIMA laboratory

**Education**
- 1987 - Engineer Degree from ENSERG (INPG)
- 1987 - DEA Degree in Microelectronics (Grenoble)
- 1990 - PhD in Microelectronics (INPG)
- 1995 - Habilitation à Diriger des Recherches (French National Degree for Research Supervising)

**Past activities**
- Director of Studies at the INPG Telecommunications Department between 2001 and 2003

**Research interests**
- Computer architecture, VLSI design methods, dependability analysis, fault-tolerant architectures, concurrent checking, test, logic implementations in nanotechnology

**On-going research activities and collaborations**
- Project on the hardening of digital circuits and embedded systems by modification of high level hardware descriptions and/or operating system functions. Collaboration with Xilinx.
- Project on circuit design based on nanoelectronic devices (CNTFETs). Laboratory leader of the ACI project NANOSYS in collaboration with many French laboratories, 2004-2007.

**Miscellaneous**
- Member of the scientific committee of the French national action on "Computer and security" (ACI Sécurité & Informatique), 2003-2007.
- Authored or co-authored more than 130 scientific papers in journals, books, conferences and workshops.
- Served in more than 50 conference committees General co-Chair for DFT'02, vice General Chair for IOLTW'02, Program co-Chair for DFT'01, IOLTS'04 and IOLTS'06, and vice Program Chair for IOLTS'03, IOLTS'05 and IOLTS'07.

LOPIN Grégory

**Position:** Engineer in microelectronics with CIS Group

**Education**
- 2003-04 : Master degree in analog and digital integrated system design (DESS CSINA, INPG).
MIR Salvador

Position: Directeur de Recherche CNRS (French National Center for Scientific Research), vice-director of TIMA laboratory

Education
2005: Habilitation à diriger des recherches, Institut National Polytechnique de Grenoble, France
1993: Ph.D. degree - Computer Science, University of Manchester, United Kingdom
1989: Master degree - Computer Science, University of Manchester, United Kingdom
1987: Industrial Engineering degree - Electrical, Polytechnic University of Catalonia, Barcelona, Spain

Current responsibilities
Deputy Director TIMA Laboratory
Leader of the RMS Group at TIMA (Reliable Mixed-signal Systems) created in 2002

Miscellaneous
Has published over 100 scientific papers in international journals and conferences
Editor of two books on silicon microsystems
General chair of IMSTW'05, VLSI-SoC'06
Program co-chair of IMSTW'04, IMS3TW'08
Local chair of WTW'05
Serves in the Steering Committee of VLSI-SoC, IMS3TW
Serves in the Program Committee of DATE, ITC, ETS, DTIS, EMT-VLSI, IWASI
Regular reviewer for International Journals and Conferences and Government agencies (NSF-USA, ANVAR-France, AGAUR-Spain …)
Member of IEEE, IEEE Computer Society and IEEE Circuits and Systems Society
Participation in the European projects SMART, JESSI-COMMON-FRAME, ARCHIMEDES, AMATIST, PROFIT, TECHNODAT, PICS, NANOTEST
Award from Association of Industrial Engineers of Catalonia, Spain, to the best Work Graduation Dissertation in Industrial Engineering, Barcelona, 1988

MORIN-ALLORY Katell

Position: Associate Professor (Maître de conférence) at ENSERG (Ecole Nationale Supérieure d'Electronique et Radioélectricité de Grenoble)

Education
2004: PhD in Computer Science, Université de Rennes 1, France
2000: DEA degree in Computer Science, Université de Rennes 1, France
2000: Magistère of Mathematical Modelling and Computer Science Method, Université de Rennes 1, France

Current responsibilities
Researcher in the VDS (Verification and Modeling of Digital Systems) group

MULLER Olivier

Position: Associate Professor at Ensimag (École Nationale Supérieure d'Informatique et de Mathématiques Appliquées) of the Grenoble Institute of Technology

Education
2007: PhD in Computer Science, Université de Bretagne-Sud and ENST Bretagne, France
2004: DEA degree in electronics, ENST Bretagne, France
2004: Engineer Degree from ENST Bretagne, France

Current responsibilities
Researcher in the SLS(System Level Synthesis) group
NICOLAIIDIS Mihail

**Position**: Research Director at the French National Research Center and Chief Technical Officer in iRoC Technologies

**Education**
- 1978: Engineer degree - Mechanical-Electrical, Ecole Polytechnique de l'Université de Thessaloniki.
- 1984: Doctor-Engineer degree - Data processing

**Design of self-testing integrated circuits for analytical failures hypotheses.**

**Miscellaneous**
- He was leader of the Reliable Integrated Systems Group at TIMA Laboratory until December 31 2000.
- His research interests include VLSI testing, DFT, on-line testing, fault tolerant design, reliability issues in very deep submicron technologies, computational and fault tolerant approaches for nano-technologies, fundamental physics, and philosophy. He published more than 170 papers, edited one book and several journal special issues, and authored 18 patents.
- He developed the memory BIST synthesis approach and the programmable memory BIST architecture licensed to two leaders of the EDA industry.
- He received twice the Best Paper Award of the Design and Test in Europe Conference, and once the Best paper Award of the IEEE VLSI Test Symposium. He also received the Meritorious Service Award of the IEEE Computer Society. He is a Golden Core member of the IEEE Computer Society.
- He authored the book "Une Philosophie Numérique des Univers", proposing a unifying vision of modern physics inspired from information systems.
- He is co-founder of iRoC Technologies.

PÉTROT Frédéric

**Position**: Professor in Computer Architecture at the École Nationale Supérieure d'Informatique et de Mathématiques Appliquées (ENSIMAG) of the Institut Polytechnique de Grenoble

**Education**
- 2003: Habilitation à Diriger des Recherches - Université Pierre et Marie Curie, Paris, France
- 1994: PhD in Computer Science - Université Pierre et Marie Curie, Paris, France
- 1989: DEA (Master) degree in Computer Science - Université Pierre et Marie Curie, Paris, France

**Current responsibilities**
- Head of the System Level Synthesis group.

**Past activities**
- 1994-2004: Associate Professor at Université Pierre et Marie Curie (Paris VI), France. Major contributor to the Alliance CAD System and to the Disydent digital system design environment.
PIERRE Laurence

Position: Professor in Computer Science at Université Joseph Fourier, Grenoble

Education
1999 : HDR ("Habilitation à Diriger des Recherches"), Université de Provence, Marseille, France
1990 : PhD in Computer Science, Université de Provence, Marseille, France
1986 : DEA degree in Computer Science, Université de Provence, Marseille, France

Current responsibilities
Leader of the VDS (Verification and Modeling of Digital Systems) group

Past activities
1991-2002 : Associate Professor at Université de Provence, Marseille
2002-2008 : Professor at Université de Nice Sophia-Antipolis

RUFER Libor

Position: Researcher / Expert in Microsystems and Test with TIMA

Education:
2007: Habilitation à Diriger des Recherches - Joseph Fourier University, Grenoble
1993: Diplôme d'Etudes Approfondies en Acoustique - Ecole Centrale de Lyon
1984: Ph.D. in Acoustics - Czech Technical University, Prague
1974: Engineer degree - Faculty of Electrical Engineering, Prague

Past activities:
1994 - 2004: Associated Professor, Joseph Fourier University, Grenoble
1997 - 1999: Invited Researcher, Acoustics Laboratory of School for Building, Concordia University, Montreal, Canada
1992 - 1993: Invited Researcher, Centre Acoustique, Ecole Centrale de Lyon
1980: Research Fellow, Acoustics Laboratory, Danish Technical University, Lyngby
1976 - 1993: Associated Professor, Czech Technical University, Prague

Current responsibilities:
- Bonus Qualité Recherche (BQR), INPG project leader (partners: TIMC Laboratory and CHU, Grenoble), 2007
- PROCORE project leader (partner: Hong Kong University of Science and Technology), 2007-2008.
- Programme committee member of the IFAC Workshop 'Programmable Devices and Systems', (PDS), 2003-2007.

Research interests:
RF MEMS, MEMS-based sensors and actuators, electro-acoustic and electro-mechanical transducers and their application in acoustics and ultrasonics, associated measurement techniques, analogue and mixed-signal systems test.
SICARD Gilles

**Position:** Associate Professor (Maître de conférence HDR) at UJF (Joseph Fourier University), Grenoble

**Education**
- 1999 : PhD in Microelectronics, INPG.
- 1994 : DEA degree in Microelectronics, INPG.

**Past activities**
- Contractual teacher (ATER) at ENSERG (Ecole Nationale Supérieure d'Electronique et Radioélectricité de Grenoble) and researcher at LIS Laboratory (Laboratoire des Images et des Signaux), Grenoble, 1999.

**Current responsibilities**
- Co-Leader of the « Concurrent Integrated Systems » research group (CIS)

**Current Research Interests:**
- New architectures of CMOS Vision Sensors (with High Dynamic range capability, or Light adaptive systems)
- Electromagnetic Compatibility in integrated circuits (Design of Asynchronous circuits with low-emission capability and a high immunity)
- Low-Power Asynchronous circuits (Design of Low-power and low-leakage corelib for asynchronous circuits)

SIMEU Emmanuel

**Position:** Associate Professor at Ecole Polytechnique de l'Université de Grenoble (Polytech’G)

**Director of CIM (Computer Integrated Manufacturing) Platform of API-PRIMECA Dauphiné Savoie**

**Education**
- 2005  DHDR (Diplôme d'Habilitation à Diriger des Recherches) in Physics, Joseph Fourier University of Grenoble
- 1992  Ph.D in Automatic Control and System Theory, Institut National Polytechnique de Grenoble
- 1988  DEA degree in Automatic Control and Signal Processing, Institut National Polytechnique de Grenoble
- 1987  Engineer degree -Electrical- University of Casablanca (Morroco)

**Current responsibilities**
- Member of the Reliable Mixed -signal Systems (RMS) Group

**Past Activities**
- 1992-1995: Associate Professor at ISAR (Institut Supérieur d'Automatique et de Robotique de Valence)
- 1988-1995: Researcher in LAG (Laboratoire d'Automatique de Grenoble)
- 1989-1992: Researcher in CNET-CNS Grenoble (SITAR Project)

**Miscellaneous**
- Pedagogic responsibility in the department of industrial risk management of Polytech’Grenoble.
- Courses and lectures at of Polytech’Grenoble on reliability analysis tools, automatic control, Supervision an Statistical Process Control, Multivariate data analysis
- Courses and lectures of automatic control, Master EEA of Joseph Fourier University
### STRATIGOPOULOS Haralampos

**Position:** Chargé de Recherche CNRS (French National Center for Scientific Research) since 2007  
**Education:**  
Ph.D., Yale University, USA, Engineering and Applied Science Department, Dec 2006  
M.S. in Electrical Engineering, Yale University, USA, Engineering and Applied Science Department, May 2003  
Diploma in Electrical and Computer Engineering, National Technical University of Athens, Greece, June 2001  
**Current responsibilities:** Member of the Reliable Mixed-signal Systems (RMS) Group  
**Research Interests:** Analog/Mixed-Signal/RF design and test, machine learning, neuromorphic solid-state circuits, RF MEMS, modeling of the MOS Transistor

### VELAZCO Raoul

**Position:** "Director of Researches" at CNRS (French Research Agency); Researcher with TIMA laboratory since 1996  
**Education:**  
1990: Dr. ès Sciences from INPG  
1982: Ph.D degree from Polytechnique Institut of Grenoble (INPG)  
1979: Engineer degree  
**Current Responsibilities:**  
Leader of the "Qualification of Circuits" research group of TIMA laboratory  
Member of the Scientific Committee of TIMA since 1998  
Responsible of the design of a flight experiment included on board a scientific satellite: NASA Project LWS/SET (Living With a Star / Space Environment Testbed)  
Expert Radiation at CNRS  
**Miscellaneous:**  
General Chair of RADECS 2001 (Grenoble, France).  
General Chairman of LATW 2002 (Montevideo, Uruguay).  
Program Chair of DFT 2003 (Boston, U.S.A.).  
General Chair of EWRHE 2004 (Villard-de-Lans, France)  
General Chair of DFT 2004 (Cannes, France)  
General Chair of SERESSA summer School of Radiation and their Effects in Systems for Space Applications, 2005 (Ariau, Brazil), 2006 (Sevilla, Spain)  
Coordinator of European ALFA (America Latina Formacion Académica) "Nicron" project

### VITRY Gérard

**Position:** "Ingénieur d'Etudes" at CNRS  
**Education:**  
1973: "Programmeur Expert en Systèmes Informatiques" – Grenoble  
**Current responsibilities:**  
System Engineer; Web administrator
ZERGAINOH Nacer-Eddine

**Position**: Associate Professor (Maître de Conférences) in Computer Engineering and architecture, Ecole Polytechnique (Polytech’G), Joseph Fourier University, Grenoble

**Education**
- 1984 Baccalaureat degree, Mathematics
- 1989 Engineer degree, Telecommunication. National School of telecommunication
- 1990 DEA degree, Signal Processing & Control, Signals and Systems Laboratory, Supélec.
- 1996 PhD degree, Computer Engineering, INRIA & Paris XI University, France

  Methods and tools-aided design of reactive systems. Distributed Real-time Operating System for an embedded obstacle detection system.

**Past activities**
- Participated to the European Esprit-Polyglot Project.
- Participated to the European Prometheus Project.
- Teacher in telecom and computer (ESIGITEL, EPITA, Paris XIII University).
- Contractual engineer of research with LIMSI-CNRS Laboratory Gif/Yvette.

**Current responsibilities**
- Researcher in System Level Synthesis Group of TIMA Laboratory.
- His research interests include system-level design and CAD issues, multiprocessor architectures modeling, and real-time operating system. Currently, his research focuses on multiprocessor architectures exploration, RTOS, and interface Synthesis.

**Miscellaneous**
- Has authored or co-authored several scientific papers.
- Has served in many program committees of conferences and workshops.
- Has served as a reviewer of many journals and conferences.
9. Ph. D. candidates

- ABDALLAH, Louay
  - Title of thesis: Built-In Self-Test of RF front-ends
  - Expected date of defense: 2011
  - Previous degrees: Master 2 Micro Nano Élætronique - Université Joseph Fourier; Master 1 Électronique - Université Libanaise – Liban

- ABOUZEID, Fady
  - Title of thesis: Studies of subthreshold digital architecture and circuit in advanced CMOS technologies
  - Expected date of defense: 2010
  - Previous degrees:

- AKKOUCHE, Nourredine
  - Title of thesis: Techniques of statistical modelling of analogue and mixed circuits for the optimization of the production test
  - Expected date of defense: 2009
  - Previous degrees: Master in Applied Mathematics

- ALSAYEG, Khaled
  - Title of thesis: Clockless microcontrol
  - Expected date of defense: 2009
  - Previous degrees: Master 2 Research "Micro and nano electronics (MNE)", INPG-UJF, Grenoble, France (2006); Engineer in electronics, Damascus university, Syria (2001)

- AMHAZ, Hawraa
  - Title of thesis: Low level image processing integrated in a CMOS image sensor
  - Expected date of defense: 2011
  - Previous degrees: Master 2 "Micro and Nano Electronics" (UJF Grenoble)

- ARTHAUD, Yoann
  - Title of thesis: Design and realisation of a monitoring micro-system for help during middle ear surgery operations
  - Expected date of defense: November 2010
  - Previous degrees: Master in Micro and Nano Electronics

- ASQUINI, Anna
  - Title of thesis: Auto test circuit development for frequency synthesizers and RF power amplifiers based on fault modelling
  - Expected date of defense: 2009
  - Previous degrees: Master in Electronic Engineering, "Roma Tre" Universitity, Rome, Italy

- BARON, Thomas
  - Title of thesis: Development of inertial sensors on thin SOI
  - Completed in April 30, 2008
  - Previous degrees: Diplôme de recherche technologique, INPG, Grenoble, France (2003)

- BEN HASSINE, Nizar
  - Title of thesis: Baw devices reliability for RF applications
  - Expected date of defense: November 2009
  - Previous degrees: Master degree in micro and nano technologies

- BEYROUTHY, Taha
  - Title of thesis: Asynchronous Programmable Logic for Secure Embedded Systems
  - Expected date of defense: 2009
  - Previous degrees: System Integration" Engineering Degree of the Telecommunication School of Engineering of Bretagne - ENST Bretagne (2005-2006); Masters degree in Micro technology: "M.A.R.S " (Micro technologie Architecture Réseaux systèmes ) from the Telecommunication School of Engineering of Bretagne : ENST Bretagne ; Masters degrees in Physics - Department of Physics- Faculty of Fundamental and Applied Sciences, Lebanese University, Lebanon (2000-2004)
- **BIZOT, Gilles**
  - Title of thesis: A global system issue from power management inside the OS down to silicon process for Reconfigurable and Massively parallel Multi-core Architectures
  - Expected date of defense: 2010
  - Previous degrees: Master of Science in Micro and Nano Electronic (EEATS - UJF); Electronic Engineer (specialized in System on Chip) (ENSERG - INPG)

- **BOCQUILLON, Alexandre**
  - Title of thesis: Fault injection in SRAM based FPGA: production, propagation and consequences
  - Expected date of defense: 2009
  - Previous degrees: Master diploma: ESPCI; Engineer diploma: ENSICAEN

- **BONNOIT, Thierry**
  - Title of thesis: Hardware/Software Codesign for Low-power and Reliability of Nanoscale configurable Multiprocessors system on chip for Software-defined radio applications
  - Expected date of defense: 2011-2012
  - Previous degrees: Masters

- **BOUGEROL, Antonin**
  - Title of thesis: Study of single event functional interrupts induced by natural radiation environment on memory based complex devices
  - Expected date of defense: 2011

- **BOUSSETTA, Hela**
  - Title of thesis: Modelling and Global Simulation of self powered Microsystems
  - Expected date of defense: 2009
  - Previous degrees: Master titled New Technologies of Dedicated information Systems –option systems conception obtained in ENIS (The high school of National Engineering of Sfax-Tunisia) (2002-2004); Master's diploma (May 2004); Electric Genius to the ENIS –Tunisia (2000-2003); Engineer's Diploma (June 2003)

- **BUHRIG, Aurélien**
  - Title of thesis: Optimization of the power consumption of wireless ad-hoc sensor network nodes
  - Completed in April 29, 2008
  - Previous degrees: Engineer degree in telecommunication at the telecom department (INPG), Grenoble, in 2004; master in micro-nano electronic at the Joseph Fourier University (UJF), Grenoble, in 2004

- **CANIVET, Gaëtan**
  - Title of thesis: Analyze and protected design of reconfigurable platforms
  - Expected date of defense: 2009
  - Previous degrees: Ingénieur Electricien, Master Recherche Spécialité Génie Electrique

- **CARLIOZ, Louis**
  - Title of thesis: Microsources of energy for autonomous wireless microsystems
  - Expected date of defense: 2009
  - Previous degrees: Master Nanotech, INPG-Polito-EPFL (2006); Licence d'Ingénierie Franco Italienne (LIIF), INPG-Polito (2004)

- **CENNI, Fabio**
  - Title of thesis: Modeling of heterogenous systems, analog/digital interfacing and MoC integration
  - Expected date of defense: 2012
  - Previous degrees: Electronic Engineer Degree, specialized in “Electronic Systems for the Elaboration of the Information” at “Università di Bologna - Facoltà di Ingegneria Elettronica”; First Level Degree at “Università di Bologna - Facoltà di Ingegneria Elettronica”; Maturità Scientifica, diploma (equivalent to a baccalaureate) obtained at “E.Fermi” Technical high school for the Industries (I.T.I.S.) with specialization “electronics and telecommunication” in Faenza, Italy
- CHAGOYA-GARZON, Alexandre
  - Title of thesis: Embedded-SW repartition in a heterogenous multi-processor environment
  - Expected date of defense: September 2010
  - Previous degrees: April 2007: "Dispense de DEA/Master"; September 2003: Engineer Diploma from the Telecommunication Department of the INPG (Grenoble); 1998: Scientific Baccalaureate Diploma, option mathematics

- CHUREAU, Alexandre
  - Title of thesis: Definition of a Service-Based Intermediate Representation for Virtual Prototyping of Systems-on-Chip
  - Completed in November 12, 2008
  - Previous degrees: Master of Applied Science (Electrical Engineering), Polytechnique, Montreal, Canada (2005)

- CLAVEL, Renaud
  - Title of thesis: Formal methods for the analysis of errors caused by transient faults
  - Expected date of defense: 2011
  - Previous degrees: Master II EEATS (Grenoble); Master ENS Cachan; Agregation in electronic

- DANG, Trong Trinh
  - Title of thesis: Digital circuits based on carbon nanotubes and SETs
  - Completed in September 25, 2008
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005)

- DEFOSSÉUX, Maxime
  - Title of thesis: Design and characterisation of piezoelectric microgenerators for autonomous microsystems
  - Expected date of defense: 2011
  - Previous degrees: Master’s degree with honours in Electronics Engineering option Micro and Nano Electronics in University Joseph Fourier; "Agrégation" of physics, option applied physics, a highly selective national teaching exam; Bachelor of science with honours in Electronics Engineering at the Ecole Normale Supérieure de Cachan

- DUBOIS, Matthieu
  - Title of thesis: Optimization of Converter Testing Using Statistical Techniques
  - Expected date of defense: 2009
  - Previous degree: DEA degree "Systèmes Automatiques et Microélectroniques" Université de Montpellier 2 (2003); Engineer degree "Microélectronique et Automatisme" Polytech'Montpellier (2003)

- ELISSATI, Oussama
  - Title of thesis: Ring oscillators and asynchronous delay lines: applications to PLLs and “Clock recovery” systems
  - Expected date of defense: 2011
  - Previous degrees: Engineer degree "Informatique Industrielle et Instrumentation" Polytech’Grenoble (2007)

- ELMRABTI, Amin
  - Title of thesis: Methodology and Meta modeling environment for specification and refinement of multiprocessor system of chip systems
  - Expected date of defense: November 2010
  - Previous degrees: Software Engineer diploma, computing master degree

- FERRO, Luca
  - Title of thesis: Verification of temporal properties for SystemC TLM specifications
  - Expected date of defense: October 2010
  - Previous degrees: Master's degree in Embedded Systems
- **FERRON, Jean-Baptiste**
  - Title of thesis: Modeling faults in SRAM FFPGA and appropriate protections
  - Expected date of defense: September 2010
  - Previous degrees: Engineer degree ENSERG (Grenoble) 2006, M2R MNE UJF (Grenoble) 2007

- **FOUCARD, Gilles**
  - Title of thesis: Radiation hardening of applications designed for complex SRAM based FPGA
  - Expected date of defense: 2009
  - Previous degrees: Master Pro Conception des systèmes intégrés numériques et analogiques, INPG (2003-04); Maîtrise Electronique, Electrotechnique et Automatique UFR de Physique, UJF, Grenoble (2002-03); Licence Ingénierie Electrique, UFR de Physique, UJF, Grenoble (2001-02); DUT Génie Electrique et Informatique Industrielle IUT1, UJF, Grenoble (1999-01)

- **GERIN, Patrice**
  - Title of thesis: Generation of simulation model for Multiprocessors System-On-Chip
  - Expected date of defense: 2009
  - Previous degrees: Master Recherche Microelectronics Grenoble, France

- **GLIGOR, Marius**
  - Title of thesis: High level programming model refinement for MPSoC systems
  - Expected date of defense: 2009

- **GOULIER, Julien**
  - Title of thesis: Research on reconfigurable analog to digital converters integrated in CMOS technology. Application in multimode receivers
  - Completed in May 26, 2008
  - Previous degrees: Engineering Degree in electronics, INSA, Lyon, France, 2002; Master Degree in Microelectronics, UJF, Grenoble, France (2004)

- **GUERIN, Xavier**
  - Title of thesis: Light Operating System Networks for Widely Distributed Applications running on Heterogeneous Multiprocessor SoCs
  - Expected date of defense: 2009
  - Previous degrees: DEUG MIAS (2003); Licence d'informatique (2004); Maîtrise d'informatique (2005); DEA / Master informatique (2006)

- **GUIRONNET DE MASSAS, Pierre**
  - Title of thesis: Shared Memory based multi-processor architecture specification and implementation
  - Expected date of defense: 2009

- **HAMON, Jérémie**
  - Title of thesis: Implementation of UWB impulse radio signal processing using asynchronous logic
  - Expected date of defense: 2009
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005)

- **HASSAN, Khaldon**
  - Title of thesis: Efficient Memory Access for MPSoC NoC-based
  - Expected date of defense: 2011
  - Previous degrees: Microelectronics Engineer (ENSERG - Grenoble INP)
- HEDDE, Damien  
  - Title of thesis: Use of simulation for development and debugging of parallel programs on MPSoC (multiprocessor system-on-chip)  
  - Expected date of defense: 2011  
  - Previous degrees: Engineer in Applied Mathematics and Computer Science

- HELMY, Amr  
  - Title of thesis: Application of theorem proving techniques to the formal verification of NoCs  
  - Expected date of defense: 2009  
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2006)

- JEAN-MISTRAL, Claire  
  - Title of thesis: Scavenging energy with electroactive polymer for wireless autonomous sensors  
  - Completed in October 8, 2008  
  - Previous degrees: Engineer from ENSEEIHT Toulouse and MASTER of science in Electrical Engineering

- KHEREDDINE, Rafik  
  - Title of thesis: Embedded Diagnosis of RF and AMS Components: Regression based Methods  
  - Expected date of defense: 2009  

- KHERIJI, Rabeb  
  - Title of thesis: Structural testing of radio-frequency integrated circuits  
  - Expected date of defense: 2009  
  - Previous degrees: Mater degree and Engineer degree

- KOCHE-HOFER, Cedric  
  - Title of thesis: Modeling, Validation and Presynthesis of Asynchronous Circuits in SystemC 
  - Completed in March, 26, 2009  
  - Previous degrees: Engineer in Computer Science at ENSIMAG (INPG) Grenoble (2004)

- KOUADRA MOSTEFAOUI, Abdellah Medjadji  
  - Title of thesis: Flexible architecture for HW/SW interfaces  
  - Expected date of defense: 2009  
  - Previous degrees: Master Computer science, University of Versailles, Saint-Quentin-en-Yvelines, France, 2005

- LAMRAOUI, Hamid  
  - Title of thesis: Autonomous microsystem design and integration for an artificial urinary sphincter control  
  - Expected date of defense: October 1st, 2010  
  - Previous degrees: ESIL Engineering degree (master degree equivalence) in Biomedical Engineering; Master's degree in Automation (INPG)

- LIZARRAGUA, Livier  
  - Title of thesis: BIST technique for CMOS imagers  
  - Completed in November 11, 2008  
  - Previous degrees: Electronic Engineer (Mexico), Master Recherche Microelectronics Grenoble, France

- MAINGOT, Vincent  
  - Title of thesis: Fault attacks vs. side channel attacks  
  - Expected date of defense: 2009  
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005); Engineering in Telecommunication, Grenoble, France (2005)

- MEUNIER, Quentin  
  - Title of thesis: Platforms Abstraction Methods for System Synthesis  
  - Expected date of defense: 2010  
  - Previous degrees: Engineer in Applied Mathematics and Computer Science, Master of Research (Major Mathematics, Computer Science)
- **MIAN QAISAR, Saeed**
  - Expected date of defense: 2009
  - Previous degrees: Masters SIPT (Signal Image Parole et Telecoms) France (2005)

- **NGUYEN, Hoang Nam**
  - Title of thesis: Design for test of RF MEMS components and microwave acoustic devices
  - Expected date of defense: 2009
  - Previous degrees: Master Instrumentation and Microelectronics at Henri Poincare University (Nancy 1) (2004)

- **ODDOS, Yann**
  - Title of thesis: Correct-by-construction design of embedded tests from high-level logic and temporal specifications
  - Expected date of defense: 2009
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2006)

- **OUCHET, Florent**
  - Title of thesis: Analogical proof of the synthesis of robust asynchronous circuits. Application to the security of embedded systems in aeronautics
  - Expected date of defense: 2011
  - Previous degrees: Master EEATS - MNE

- **PAUGNAT, Franck**
  - Title of thesis: Study and development of a AMS design-flow in SytemC: semantic, refinement and validation
  - Expected date of defense: 2012

- **PERONNARD, Paul**
  - Title of thesis: Study of the atmospheric effects on a complex microprocessor
  - Expected date of defense: 2009
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France; DEST Electronique (CNAM) (2005); DUT GEII (2001)

- **POPOVICI, Katalin**
  - Title of thesis: Multilevel programming environment for heterogeneous MPSoC architectures
  - Completed in March 25, 2008
  - Previous degrees: Engineer Degree, University Oradea, Romania, 2005

- **PORCHER, Alexandre**
  - Title of thesis: Proven generation of robust asynchronous checkers-Application to safe embedded systems
  - Expected date of defense: 2011
  - Previous degrees: ENSERG Ingineer and Master 2 MNE graduate

- **POSSAMAI BASTOS, Rodrigo**
  - Title of thesis: Designing Asynchronous Circuits More Transient-Fault Robust
  - Expected date of defense: 2010
  - Previous degrees: Electrical Engineer at UFRGS, Brazil; Master in Computer Science at UFRGS, Brazil

- **RAHMOUNI, Khaled**
  - Title of thesis: Optimisation of the electronic/software design flow in the context of critical embedded systems targeting circuit breakers for medium voltage electrical networks
  - Expected date of defense: 2010
  - Previous degrees: Mastère spécialisé Productique et Informatique Avancée, Ecole Centrale de Lille
- **RASLAN, Zahy**
  - Title of thesis: Nanoelectromechanical systems based on carbon nanotubes: Realisation and test
  - Expected date of defense: 2009
  - Previous degrees: Master's degree in Advanced Technologies for communication and mobility; Master's degree in Computer and electrical engineering

- **RIOS, David**
  - Title of thesis: Low Power Asynchronous Systems
  - Completed in September 18, 2008
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2004); Engineering degree in electronics (2003)

- **RUSU, Claudia**
  - Title of thesis: Fault Tolerant Network on Chip
  - Expected date of defense: 2009

- **SAHNINE, Chawki**
  - Title of thesis: Reconfigurable, high throughput and low power VLSI architecture for advanced OFDM digital processing
  - Completed in January 30, 2009
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2005); Bachelor in Electrical Engineering, Ecole polytechnique de Montréal, Montréal, Canada (2004)

- **SENOUCI, Benaoumeur**
  - Title of thesis: Automatisation of prototyping flot, based on reconfigurable plateform for the hardware/software interface validation
  - Expected date of defense: 2009
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France

- **SHEN, Hao**
  - Title of thesis: Contribution to a modeling approach and an exploration flow targeted to heterogeneous MPSoC architectures based on configurable processors
  - Completed in March 11, 2009
  - Previous degrees: Master, Computer Science and Technology, Shanghai Jiao Tong University, Shanghai, P.R.China, 2005

- **TONGBONG, Jeanne**
  - Title of thesis: Development of BIST techniques for Radio Frequencies ICs
  - Expected date of defense: 2009
  - Previous degrees: Master Optics and Microwaves, INSERG-INPG, Grenoble, France, (2005)

- **VITTOZ, Stéphane**
  - Title of thesis: Pressure/Vibrations microsensors based on AlGaN/GaN substrate for harsh conditions environments
  - Expected date of defense: 2011
  - Previous degrees: Master Degree in Micro Nano Electronics from Grenoble Joseph Fourier University of Science (2008); Graduate in Device Physics from Grenoble Institute of Technology (2008)

- **VANHAUWAERT, Pierre**
  - Title of thesis: Fault-injection based dependability analysis in FPGA-based prototyping environment
  - Completed in April 4, 2008
  - Previous degrees: Master Recherche Microelectronics, Grenoble, France (2003); ENSERG engineer diploma (2003)
- **YAHYA, Eslam**
  - Title of thesis: Network-on-chip design using asynchronous logic
  - Expected date of defense: 2009
  - Previous degrees: Master of Science/Electrical Engineering, Benha High Institute of Technology, Egypt, (2004)

- **YANG, Wenbin**
  - Title of thesis: Design and integration of microsystems in a medical needle for deformation measurement and insertion guidance
  - Expected date of defense: 2011
  - Previous degrees: Master of science (research) in Micro and Nano Systems, Paul Sabatier University, Toulouse (2008); Bachelor of science in electronic engineering, Zhejiang University, China (2005)

- **YU, Hai**
  - Title of thesis: Fault Tolerant Architecture for Mitigating the Variability Issues in Nanometric Technologies
  - Expected date of defense: 2010
  - Previous degrees: Master

- **ZAKARIA, Hatem**
  - Title of thesis: Integrated asynchronous regulation for decananométric technologies: application to an embedded reconfigurable parallel system
  - Expected date of defense: September 2010
  - Previous degrees: Master of Science (Optimal power control of CDMA mobile networks), September 2006, Benha University

- **ZIMOUCHE, Hakim**
  - Title of thesis: High Dynamic Range CMOS Image Sensor with no sensibility to disturbance
  - Expected date of defense: October 2010
  - Previous degrees: Master2 Recherche (DEA) en ESM (Electronique, Signal et Microsystèmes)
10. Contracts

TIMA has a long tradition of international cooperations, both with industrial and academic partners in the context of multinational projects. This chapter provides a short abstract of the topics and objectives of the contracted partnerships that were active in 2008.

New European Projects or European Projects still ongoing in 2008:

IST PROJECTS

- **VIBES**: (VIBration Energy Scavenging) 01/01/2004-31/12/2006 – continuation in 2008
  Philips Electronics NV, The Netherlands; Philips Inovative Technology Solutions NV, The Netherlands-Belgium; ADR/TIMA, France; University of Southampson, United Kingdom; University of Cork, Ireland; CNRS, France; MEMSCAP, France; METRAVIB, France; Philips GmbH, Germany.
  VIBES is a Specific Targeted Research Project (STREP) of the 6th Framework Program of the European Union (EU). The goal of this project is to develop and demonstrate a micro power generator able to scavange vibrations and motions from the surrounding (like building, machines, human body). This device will produce electrical power (in the range of µW) in order to feed an autonomous microsystem. The microsystem will embed an Ultra Low Power controller, a low power RF communication module, several MEMS sensors and a micro battery for energy storage. The project will focus on piezoelectric and electromagnetic transduction principles implemented with MEMS microfabrication techniques.

- **SHAPES**: (Scalable software Hardware Architectures Platform for Embedded Systems) 01/01/06-30/06-2009
  Partners: ADR/TIMA, France; Eidgenoessische Technische Hochschule, Switzerland; Rheinisch-westfaelische Technische Horschule, Germany; Istituto Nazionale di Fisica Nucleare, Italy; Target Compiler Technologies, Belgium; St Microelectronics SA, France; Universita di Pisa, Italy; Universita Degli Studi di Cagliari, Italy; Fraunhofer Gesellschaft zur Foerderung der Angewandten Forschung, Germany; Medcom Gesellschaft fuer Medizinische Bilververbeitung, Germany; PIE Medical Equipemt BC, The Netherlands; THALES Communication, France.
  Future computing architectures for Embedded DSP and Control are strategic and deserve adequate research efforts. Tiled architectures suggest a possible HW path: "small" processing tiles connected by "short wires". Tiled Architectures will cover a significant share of 10+ year embedded applications. The SHAPES project will set a new density record with multi-Teraops single-board computers and multi-Petaops systems, and will be based on a groundbreaking HW/SW architecture paradigm. The heterogeneous SHAPES tile is composed of a VLIW floating-point DSP, a RISC, on chip memory, and a network interface. It includes a few million gates, for optimal balance among parallelism, local memory, and IP reuse on future technologies. The SHAPES routing fabric connects on-chip and off-chip tiles, weaving a distributed packet switching network. 3D next-neighbours toroidal engineering methodologies will be used for off-chip networking and maximum system density.

- **SPRINT**: (Open SoC Design Platform for Reuse and Integration of IPs) 01/01/2006-31/125/2008
  Partners: ADR/TIMA, France; FROSILOG SA, France; Universitaet Pederborn, Germany; KEESDA, France; Philips Semiconductors BV, The Netherlands; KUNGLA TEKNISSKA HOEGSKOLAN, Sweden; SPIRATECH Ltd, France; EUROPEAN ELECTRONIC CHIPS & SYSTEMS DESIGN INITIATIVE, France; ARM Ltd, United Kingdom; LAUTERBACH DATENTECHNIK, Germany.
  The SPRINT project aims at enabling Europe to be the leader in design productivity and quality in System-on-Chip (SoC) design, by mastering the SoC design complexity with effective standards and design technology for reuse and integration of Intellectual Property (IP) modules. Designer productivity is the main obstacle to efficient implementation of complex SoCs. Using standards to support the efficient reuse and exchange of IP modules is the way to enhance productivity. The SPRINT consortium performs a rigorous integrated research activity to obtain a breakthrough in technology for reuse and integration of IP modules within and across companies, so that IP from various sources can be combined quickly and efficiently. The key SPRINT objectives are: 1. To align the approaches of the European key players in the SoC domain towards IP reuse and to drive the identification and development of open interface standards for IP integration. 2. To create an open SoC design platform, consisting of standards and a SoC design methodology, with matching tools and IP modules. Such design platform provides the basis for SoC design environments that support the efficient development and integration of interoperable and reusable IP modules, including debug and verification of SoCs.
3. To enable European companies to be the first in the world to demonstrate and subsequently exploit the new standards-based SoC design environments in an interoperable way in order to improve on design productivity and the quality in SoC design.

FP7-Cooperation COLLABORATIVE PROJECT

MORGAN: Materials for Robust Gallium Nitride – 01/11/2008-30/10/2011

This project will study GaN based structures with goals going from material fabrication and optimisation to applications in thermal heat spreaders, interconnection, packaging, power devices, and sensors. All these studies will be realised in the frame of a large consortium capable of realizing deep materials studies, physical and electrochemical simulation and modelling, and to engage studies on the degradation phenomena. The materials development will be compatible to 100mm or even 150mm diameter wafers, that could be later required for implementation in industrial manufacturing plant. Evidently such manufacturing development would be developed elsewhere. The participation of SME and leading companies in diamond materials, epitaxial growth, sensors and power microwave electronics insures potential use in case of success. These materials development will create novel materials for extreme environments. They will increase the product durability (energy production, microwave power, aerospace telecommunication) and through sensors which will improve process controls decrease the risk of industrial hazards and increase safety.

The role of the TIMA Laboratory is to accomplish detailed modelling of electrical and mechanical behaviour of different structures used for pressure and chemical sensors for harsh environment. Electro-mechanical behaviour of different layers composing these structures will be simulated in order to predict basic features of these sensors. Piezoelectric and piezoresistive effects in these structures will be studied.

MEDEA+ PROJECTS

Medea+ 2A 701: PARACHUTE: (Parasitic Extraction and Optimisation for Efficient Microelectronic Design and Application) 2006-2008
Partners: MINEFI/DGE/STSI, France ; EADS-CCR, France ; EADS Space Transportation, ATMEL Nantes, France ; AIRBUS, France ; IROC Technologies, France ; TIMA/UJF, France ; Univ. of Madrid, Spain; Univ. Palma de Majorca, Spain; Alcatel Espacio, Spain.

This project addresses the increasing problem of interference that together with the parasitic effects of new IC processes are affecting the reliability of modern electronic systems. Nanometer circuits, micro-electronics, micro-system technology and power electronic systems are already part of our daily life. However, these systems encounter many problems with natural and artificial interferences coming from various sources i.e. those circuits are becoming sources of interference to themselves. Considerable steps forward have to be made to improve the "Reliability of Applications based on these Electronic Systems". Reliability will be defined here as the securing of the system function regardless the presence of "interference" and these "Parasitic Effects". The one that will especially be considered are:

- Electromagnetic effects due to the presence of electromagnetic parasitic fields: Electromagnetic Compatibility (EMC), Signal Integrity, Short Electrical Transient, electrostatic discharges;
- Particle Radiation effects: particles naturally present in the atmosphere are able to ionise silicon and induce some parasitic currents: these effects are named /Single Event Upset and Single Event Transients.
Médéa+ 2A 702 : NanoTEST 2006-2008
Partners : MINEFI/DGE/STSI, France; STMicroelectronics SA, France, TEMENTO Systems, France; CEA/LETI-DCIS, France; CNRS DR 13/LIRMM, France; TIMA/INPG, France; NXP, France & The Netherlands; INFINEON, Austria; INESC, Tecmic, Portugal; AMIS, Q-Star Test, Belgium.

NanoTEST will create breakthroughs in manufacturing test, in the area of costs as well as achieved quality and time-to-market. This project brings together four European microelectronics companies, four well-known institutes, and three SMEs. This strong consortium will deliver new test methodologies as we enter the nano-technology era. Both future SoC technology nodes and future SiP packages are addressed. Accompanied by flows, tools and standards, the project results will be ready for exploitation on time to support emerging technologies. This will contribute significantly to the commercial success of the European microelectronics industry.

Médéa+ 2A 703 : NEVA (Networks on Chips Design Driven by Video and Distributed Applications) 2006-2008
Partners : MINEFI/DGE/STSI, France; BULL, France; CERTESS, France; , CEA-LETI, France; SILICOMP, France; STMicroelectronics, France; UJF/VERIMAG, France; TIMA/INPG, France; ACE, The Netherlands; LIADS, Univ. of Leiden, The Netherlands; Philips Electronics, The Netherlands.

With circuit size potentially reaching one billion transistors by end 2008, traditional bus-based single-clock architectures become unusable for commercial circuits. Starting from successful design approaches (e.g. Multi-Processors, Asynchronous Design) proven during MEDEA+ phase-1, NEVA intends to raise 3 main innovations up to industrial level: communication-centric design for fast simulation and execution, infrastructures for real-time applications, and a complete design flow to implement asynchronous techniques. Datastream applications, mainly from the Video field, will be used as drivers, with a target computing power of 1 GOPS per chip.

Médéa+ 2A 708 : LOMOSA (Low-power expertise for Mobile & multi-media System Applications) 2006-2008
Partners : MINEFI/DGE/STSI, France; STMicroelectronics, France; THOMSON R&D, France; PHILIPS, France; THALES Communications, France; CEA/LETI, France; CEA/LIST, France; TIMA/UJF, France; Univ. of Cantabria, Spain; ALARI, Switzerland; Diseno de Sistemas en Silicio, SA, Spain; Royal Philips Electronics, The Netherlands.

The LoMoSA+ project aims at the creation of a low-power expertise for mobile and multimedia applications by initiating the development of a European low-power System-on-Chip (SoC) platform, consisting of an interacting combination of (architectural) models, design flows and methodologies, hardware design components, embedded software and test-benches. A special work package investigates the impact on power, scalability and performance of future multiprocessor SoC infrastructures based on on-chip communication solutions. The concept of hardware-dependent software (HdS) allows building efficient hardware-software interfaces and thus enables keeping power consumption under control for these novel architectures. The LoMoSA+ consortium consists of world-class experts from the industry (Philips, STM, Infineon, Thales, Thomson), a number of university research labs and institutes (CEA, TIMA, Universities of Braunschweig, Kaiserslautern, Paderborn, Munich, Berlin, Cantabria) and 2 SME’s (DS2, and Target). The contribution of TIMA in this project is the definition of a hardware dependent software API and a set of tools to support the optimized implementation of hardware/software interfaces based on a user defined library of heterogeneous components.

Médéa+ 2A717 : Beyond DREAMS 01/06/2008-31/05/2011
Partners : STMicroelectronics (Grenoble) SAS, MAGILLEM Design Services, CEA/LETI, Université PARIS VI PIERRE et MARIE-CURIE.

Design Refinement of Embedded Analogue and Mixed-Signal Systems (DREAMS) is a joined effort of the European semiconductor companies, together with leading European Universities and research institutes, to address the design issues for these novel architectures. The LoMoSA+ consortium consists of world-class experts from the industry (Philips, STM, Infineon, Thales, Thomson), a number of university research labs and institutes (CEA, TIMA, Universities of Braunschweig, Kaiserslautern, Paderborn, Munich, Berlin, Cantabria) and 2 SME’s (DS2, and Target). The contribution of TIMA in this project is the definition of a hardware dependent software API and a set of tools to support the optimized implementation of hardware/software interfaces based on a user defined library of heterogeneous components.
Objective is to develop modelling techniques which will be by the standardization bodies, and the proof-of-concept implementation developed in the project must be freely available as open-source software. In addition to this, a design environment facilitating IP integration, modeling and simulation is required. This unified design framework, which should be based on standardized meta-data model descriptions, should bring the different design disciplines together, enabling design/IP reuse and interfacing with third-party design and simulation tools.

- **Medea+ 2A714 : SOFTSOC** 01/01/2008-31/03/2011
  Partners: THALES Communications SA, THOMSON R&D France, CEA/LETI.
  SoftSoC aims at solving the main SoC productivity bottleneck by providing Hardware Dependant Software (HDS) solutions to enable SoC designers to aggregate multiple HW IP with their associated HDS into efficient design.
  SoftSoC solutions will enable Europe to maintain its leadership in key strategic markets by increasing the capacity of SoC designers to build larger and better quality systems in less time. The consortium involves European leaders in system and SoC design interested in the exploitation of the results.

- **Medea+ iGLANCE (interactive Genius Look At Numerous Contemporary Events)** 01/07/2008-30/06/2011
  Partners: STMicroélectronics(Grenoble) SAS, 4D VIEW Solution, LOGICA IT SERVICES France, INRIA.
  High-Definition Television (HDTV) is close to mass-market development in Europe, as the most important key component, i.e. the flat screen display, has become affordable for consumers, and besides this, media and standards for HDTV content distribution are available (BD, HD-DVD, H.264 video coding). In fact, experiments with HD displays have revealed that three-dimensional TV (3DTV) for consumers may be implemented at low cost by extending the display with a lenticular lens coating and a feasible 3D rendering engine. A next-generation processing chip for HDTV receivers should therefore not only upgrade the existing generation of chips in terms of performance of high-definition AV quality, but also prepare for the development of a new innovative application. Simultaneously, the breathtaking growth of the Internet and the increasing use of cameras is pushing innovations in AV content distribution, user content creation such as a YouTube channel, and remote information sharing. Therefore, the broadcasting market is experimenting with new forms of video distribution, like IPTV. These developments call for a TV chip design which innovates in the direction of 3DTV, featuring so-called multi-view decoding. This allows interactive selection of viewpoints within a scene between the available camera viewpoints (Free-Viewpoint TV). This viewing mode also appears in medical analysis applications. Furthermore, the healthcare market provides interesting cases 3DTV, since 3D data is common for many medical imaging modalities (e.g. CT, MR, 3D/4D ultrasound, 3D X-ray), and the visualization of such data could inherently benefit from 3D display devices and advances in the underlying techniques.

The iGLANCE project brings a strong partner in advanced imaging with the European market leader of TV chips together in their ambition to realize new innovations in digital TV platforms. This embedded system will be implemented by developing an innovative chipset and the corresponding software and architecture, where

1. the system can offer the ultimate HDTV AV quality to serve the European mass-market application of HDTV, and by
2. establishing a flexible architecture extension providing the additionally required computation power for 3D multi-view decoding, requiring the processing of several HDTV channels.

**LATIN AMERICA HIGHER EDUCATION PROJECTS (Amérique Latine Formation Académique : ALFA)**

**ALFA/NICRON** : Fault-Tolerant System Design and Verification for Safety Critical Applications
Built from Advanced Integrated Circuits. SCIENTIFIC and TECHNICAL TRAINING Europe/Amérique Latine 11/02/2006-10/02/2009
Partners: Universidade Federal do Rio Grande do Sul (UFRGS), Brazil; Instituto Nacional de Tecnologia Industrial (INTI), Argentina; Universidad del Valle (UV), Colombia; Pontificia Universidad Catolica de Peru (PUCP), Peru; Universidad de la Republica (UR), Uruguay; Instituto Nacional de Astrofisica, Optica y Electronica (INAOE), Mexico; Politecnico di Torino (POLITO), Italy; Instituto Superior Tecnico (IST), Portugal; Ecole Nationale Superieure d’Electronique, Informatique et Radiocommunications (ENSEIRB), Bordeaux, France; IMSE-CNM (Instituto de...
The constant progress accomplished in microelectronic circuits manufacturing technologies entails a significant increase of their sensitivity to different parasitic phenomena induced by the environment, making mandatory the use of fault tolerant techniques to guarantee the final system reliability/safety. The proposal goals are to support students and researchers mobility among a net of Latin American and European Universities having well-recognized skills in this area. Thanks to both the complementary experience of the network members, and the novelty of problems and proposed solutions, the offered training activities represent a precious vehicle in the diffusion of fault-tolerant design techniques in the participating countries.

**MARIE-CURIE Outgoing International Fellowships (OIF)
Support for Training and Career development of researchers**

- **Contrat “RESPONS”**: Multiple-Valued application of negative differential resistance devices in asynchronous circuits design. 31/01/2007-30/01/2010
  Partners: CEE/TIMA-INPG/ASU Fulton School of engineering (Arizona State University)
  The project targets the post-CMOS era technologies. It focuses on the digital logic applications of negative-differential resistance (NDR) semiconductor nanodevices. NDR property appears in nanometer scale devices due to quantum resonant tunnelling or Coulomb blockade effects and inherently introduces strong binary and multiple-valued processing capacities of the devices like resonant-tunelling diodes (RTD), single-electron transistors (SET), carbon nanotubes (CNT).

  This project aims to develop test strategies for mixed-signal/radio-frequency (RF) integrated devices using machine learning. The proposed efforts will be directed to two main areas, namely (a) the on-line test of mixed-signal/RF circuits when they are embedded in a System-on-Chip (SoC) or a System-in Package (SiP) that demands high reliability and (b) the testing of RF micro-electro-mechanical systems (MEMS). The key novelty of this interdisciplinary project lies in very large-scale integration (VLSI) design and test, in order to address emerging and open-ended test challenges.

**NATIONAL PROJECTS**

In addition, TIMA is a partner in a variety of national cooperative research actions which are listed below:

- **ANR projects**:
  - **SAFE**: (Fpga sécurité asynchrone pour les systèmes embarqués) 22/12/2005-21/12/2008
    Partners: CNRS Délégation Régionale Paris A/Laboratoire Traitement et Communication de l'Information (LTCI) INPG/TIMA
  - **ARESA**: (Système Enfoui et Réseaux de Capteur) 13/12/2005-12/12/2008
    Partners: France Telecom R&D/TECH/IDEA - LSR IMAG VERIMAG - CITI EA - CORONIS SYSTEMS
  - **SoCLib**: (Plate-forme de Prototypage pour Applications Logicielles Embarquées sur Puce) 01/12/2006-30/11/2009
    Partners: Université Paris VI (Pierre et Marie Curie) coordonnateur, THOMSON R&D France SNC, STMicroelectronics S.A, THALES Communications SA, CEA/Centre d'études Nucléaires SACLAY, INSA Lyon, Groupe des Ecoles des Télécommunications, INRIA, Univ de Bretagne Sud, MAGILLEM DESIGN Services, TURBOCONCEPT, CEA Grenoble, SILICOMP-AQL
  - **FME³** (programme SESUR): Enhancing the Evaluation of Error consequence using Formal Methods – 01/01/2008-31/12/2010
    Partners: LIP6 (Laboratoire Paris 6)
    The aim of the FME³ project (Enhancing the Evaluation of Error consequences using Formal Methods) is to develop and evaluate a new methodology for analyzing the robustness of circuits described at the RT level, with respect to errors caused by transient faults. We propose to improve efficiency and accuracy by combining fault injection techniques and formal methods. The keystone of our approach will be a functional modeling of both the device and the fault models. Such a
formalization will fit the capabilities of model checking tools as well as of theorem provers, thus giving the possibility to consider various kinds of circuit descriptions, including parameterized ones.

- **SFINCS (programme ARFU)**: **Semi-Formal INstrumentation for Circuits and Systems**
  01/01/2008-31/12/2010
  Partners: DOLPHIN, THALES
  The SFINCS project (Semi-Formal INstrumentation for Circuits and Systems) investigates and develops new technologies for SoC validation. SFINCS addresses **Assertion-Based Verification (ABV)**. The aim of this project is to develop and integrate methodologies to apply ABV to a variety of hardware systems, using a uniform approach founded on a technology conceived in the TIMA Laboratory. We target the following designs:
  - synchronous IPs described at the RT level
  - pseudo-synchronous, mixed functions and GALS systems (Globally Asynchronous Locally Synchronous)
  - HW/SW system aspects described at the SystemC TLM (transactional) level
  - application to complex, mixed SoC and to safety critical systems.

- **HOSPI (Programme ARFU)**: **HOmogeneous SPecification for Platform Integration**
  01/01/2008-31/12/2010
  Partners: CEA/LETI-DCIS, MAGILLEM Design Services (MDS).
  The objective of the HOSPI project is to define innovative methods, and implement the associated tools, to ease the mapping of data-streaming applications on heterogeneous platforms. From a practical point of view, it implies to reduce the gap that exists between the application description, i.e. high level specification that does not make any assumption on the implementation, and the platform description, that includes pieces of hardware and pieces of software to support the actual implementation. We propose a 3 steps process: /a/) use a general-purpose environment to describe and parallelize the application. This environment will be based on Process Networks (PN) to express the coarse grain parallelism of the application, /b/) provide an abstract view of the platform, both on communications and computations sides, based on an XML view. The target formalism will be inspired from the existing IP-XACT schema, but will require many still to be identified add-ons to express the platform capabilities and parameters, and /c/) define relationships between these two views in order to automate the way the application can be mapped from its PN representation onto the HW platform. These relationships will be used to express the mapping choices, and be supported by tools to automate the generation (or parameterization) of the HW and SW.

- **DGE projects, competitiveness cluster MINALOGIC:**
  - **SCEPTRE**: Optimisation Partitionnement, Modélisation et Compilation des SOC Multiprocesseurs
    01/10/2006-30/09/2009
    STMicroelectronics Divisions STS et HEG, INRIA Equipes MOAIS, Mescal, Arenaire et Compys,
    IRISA Equipe CAPS, TIMA Equipe SLS, UJF (Verimag), CAPs Entreprise
  - **OPEN-TLM**: Open Transaction Level Modeling
    01/10/2006-30/09/2010
    CEA/LETI, INRIAlpes, Keesda, Silicomp, STMicroelectronics, TIMA, Thomson, UJF (Verimag)
  - **ASTER**: Architectures pour mémoires STatiques haute pERformance
    01/04/2007-31/03/2010
    STMicroélectronics SA coordonnateur, Defacto Technologies, TIMA/INPG
  - **VIS-IMALOGIC**: E2V SEMICONDUCTORS SAS coordonnateur, CEA/LETI; TIMA/UJF
    01/07/2007-30/06/2010
  - **ARAVIS**: Architecture avancée Reconfigurable et Asynchrone pour Vidéo et radio logicielle Intégrée
    01/10/2007-30/09/2010
    STMicroélectronics SA coordonnateur, INRIA, CEA/LETI, France Telecom
  - **SOCKET**: SoC toolKIT for Critical Embedded systems
    02/06/2008-01/06/2011
    Partners: ASTRIUM SAS, STMicroelectronics (Grenoble) SAS, THALES Research & Technology France, AIRBUS, France, MAGILLEM Design Services, SCHNEIDER, ELECTRIC INDUSTRIE SAS, CEA/LETI, Université de Bretagne Sud, Centre National d'Etudes Spatiales
    The SoCKET project (SoC toolKit for critical Embedded sysTemS) gathers industrial and academic partners from the **Aerospace Valley** (http://www.aerospace-valley.com/en/) and **Minalogic** (http://www.minalogic.com/en/) pôles to address the issue of design methodologies for critical
embedded systems. The main goals are the following:

- to define a "seamless" design flow which integrates qualification and certification, from the system level to integrated circuits and to software
- to apply the SoC's design methodologies to critical embedded systems
- to reduce design time (by enabling concurrent hardware and software development) and to optimize SoC-based design
- to disseminate these methodologies through the Aerospace Valley and Minalogic pôles.

Other DGE projects:

- **ASTEC**: Asynchronous TECnology and components for ultra low power embedded and secured systems. 03/09/2008-02/12/2010
  Partners: CEA Centre de Grenoble, TIEMPO, UJF/TIMA.
  The aim of the Minalogic ASTEC project is to design a new family of Low power Asynchronous components (IP of 16 and 32bits micro controller core). These components will be dedicated to Low Power embedded systems and security applications. In order to demonstrate the performances of these asynchronous IPs, two microcontrollers will be designed and tested (With Tiempo SAS and TIMA Labs): A 16bits version for Low Power applications and a 32bits for security applications. The 16bits microcontroller will be used in several prototypes of low power embedded systems for medical and sport applications (with Cyberfab SARL and Tracedge SARL). The 32bits microcontroller will be validated in a security application (with CESTI LETI)

- **CROLLES III « NANO-2012 »**: 01/09/2008-31/12/2010
  Partners: Alcatel Vacuum Technology France, CCI de PARIS, CEA centre de Saclay, CEA centre de Grenoble, CNRS, (CEMES, CRHEA, IEMN, IM2NP,LAAS,LCC), Ecole Centrale de LYON, ENSEA, ENSIERT/IMS, IBM, INPG/IMEP,INPG/SIMAP, INPG/TIMA, INRIA (Grenoble), Rennes, Sophia Antipolis, Institut Supérieur d'Electronique du Nord (ISEN), MASA GROUP, STM (Crolles), (Grenoble & Wireless), Univ.MontpellierII (GES), Univ. d'Oreléans (GREMI), Univ.PARIS SUD ORSAY (IEF), Univ.PIERRE & Marie CURIE (LIP 6), Univ.de TOURS Français RABELAIS(LMP), Univ.de SAVOIE.
  Subproject "Test sequence generation for assertion acceleration" (VDS team)
  The global goal of this subproject is to develop an assertion-based methodology for testing embedded systems. In our approach, starting from PSL assertions, we generate synthesizable VHDl or Verilog descriptions of hardware checkers. These components can be connected to the device under test and used during simulation or hardware emulation to check whether the temporal properties expressed by the PSL assertions are satisfied. In that context, test sequence generation is a crucial issue. Using constrained random test generation can lead to a low coverage rate regarding the checkers's activation conditions, and checking can thus be irrelevant. The goal of this project is to propose new methods for generating test sequences constrained by temporal properties.

Rhône-Alpes (Regional projects)

- **SCADRI** : Evaluation de la sensibilité de Circuits Avancés Digitaux face aux radiations Ionisantes 20/07/2006-20/07/2009
  Partners: iRoc Technologies, E2V Grenoble, CNES, INPG/TIMA coordonnateur

- **CLUSTER II "ISLE" projet EMSGC-RECHERCHE**: 06/11/2005-05/11/2008
  Partners: Le LIG, VERIMAG, INSA Lyon, INL, LAMA, Univ. St Etienne, CEA/LETI, LAG, LCIS, INRIA.

- **NANO 2008**: (01/01/2006-31/12/2008
  Partners: FREESCALES Semiconducteurs, PHILIPS et STMICROELEC - TRONICS, CEA/LETI, INPG/TIMA

- **CILOE**: Calcul Intensif pour les LOgiciels de CAO Electronique et les applications embarquées. Pôle de compétitivité MINALOGIC. 13/06/2008-12/07/2011
  Partners: BULL, INRIA (équipe Mescal et Moais), CEA/LETI, 3 PME (EDXACT, INFINISCALE, PROBAYES)
  CILOE is a project involving Grenoble Universities (UJF-TIMA), other academic partners (INRIA, CEA-LETI), Small industries (SC, EDXact) end big industries (BULL, CS). It received the label MINALOGIC. The main goal is to study and experiment High-Performance Computing in the field
of Computer Aided Design of Electronics and in embedded applications. The contribution of TIMA (one man-year) is about the processor CELL.

  Methods, tools and models for the development, the test and the qualification of fault tolerant multiprocessor platforms
  The main goal of this project is the development of new models, methods and tools for the prediction of the reliability and the dependability of fault tolerant multi-processor systems (FTMPS), particularly with respect to faults induced by ionizing radiation. This researches are focused in FTMPS implemented by means of FPGA (Field Programmable Gate Arrays) and devoted to real-time signal processing, the final goal being the analysis of the possibility to use commercially available FPGAs for the control of intelligent antennas devoted to operate on-board satellites.
11. International activities

This section gives an overview of national and international activities in which the members of the Laboratory participated.

International cooperation agreements

The Laboratory is engaged or has been recently engaged in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations took various forms, e.g. extended visits of researchers at the cooperative location, organization of joint research, organization of workshops, etc.

- Politecnico di Torino, Italy (2006-2009)
  This cooperation takes place in the framework of ALFA NICRON project; between France and Italy. The project deals with validation of an automated technique for the realization of robust software devoted to high-safety applications with the Dipartemento di Automatica e Informatica, M. Sonza Reorda.

- The Hong Kong University of Science and Technology (HKUST), Clear Water Bay, Kowloon (2007-2008)
  Title: High-frequency MEMS sensor for aeroacoustics measurements
  This cooperation takes place in the framework of the Hong Kong Joint Research Scheme PROCORE, supported by the French Ministry of Foreign Affairs and by the French Ministry of Education and Research. The project deals with the design of the high-frequency MEMS sensor for aeroacoustics measurements. The cooperation is directed by M. Wong at the Department of Electrical and Electronic Engineering, HKUST, and by L. Rufer at TIMA.

- University “Polytechnica” of Bucarest, Romania (2006-2008)
  This collaboration focuses on architectures based on quantum devices with Prof. R. Chisleag and a TEMPUS project, “European Education in Quality for Romania”, with Prof. I. Bacivarov. The cooperation is directed by B. Courtois and L. Anghel from TIMA.

- McGill University, Montréal, Canada (2007-2008)
  This cooperation takes place in the framework of a “Centre Jacques Cartier” project. It focuses on the assertion-based verification, debug and on-line monitoring techniques. It is directed by Z. Zilic at the Electrical Engineering and Computer Science Department, and by D. Borrione and K. Morin-Allory at TIMA.

- Universidad de Cantabria, Santander, Spain (2007-2008)
  This cooperation takes place in the framework of a Franco-spanich integrated action of the PICASSO program, 2007-2008. This cooperation is directed by S. Bracho in the University of Cantabria and S. Mir at TIMA.

- Sharif University, Tehran, Iran (2008-2009)
  This cooperation, under the framework of a Gundishapur PHC program (Egide), focuses on the signal processing systems based on a non-uniform sampling scheme. The cooperation is directed by Prof. Farokh Marvasti from the Sharif University and L. Fesquet at TIMA.

- The Hong Kong University of Science and Technology (HKUST), Department of Electronic and Computer Engineering, Clear Water Bay, Kowloon, (2009-2010)
  Title: Integrated Wireless Capacitive Micromachined Ultrasonic Transducer for Bio-medical Applications
  Abstract: This project aims at developing an integrated wireless capacitive micromachined ultrasonic transducer (CMUT) for bio-medical applications. Such a device will be useful for medical diagnosis and imaging in areas that are difficult to reach using traditional ultrasound devices. Intravascular ultrasound (IVUS) imaging and minimal access surgery (MAS) imaging will be considered as possible applications. In order to be useful for these applications, the transducer must be sufficiently small (mm scale) and must be able to generate and to sense ultrasonic waves in the frequency range from 1 MHz to 30 MHz. Different research groups developed CMUTs that can work in the mentioned frequency range and can be potentially used for imaging applications. To our knowledge, there is no wireless system integrating the ultrasonic transducer with the...
interface electronics and transmitter and receiver circuitry in the same device. Moreover, the fact that only few CMUTs are actually commercially available opens space for the research in this field. The CMUT will be designed for a CMOS compatible technology with post-CMOS back-end MEMS (Micro-Electro-Mechanical Systems) device process. The CMOS compatible technology allows building the necessary electronics on the same chip and thus substantially improving the device performance. In order to obtain an optimal solution for the overall functionality, accuracy and reliability, the project will focus on the precise modeling of the MEMS, microelectronic design, simulation, and layout, fabrication process, and final test of the device.

- University of Montreal, Canada
  This cooperation with the group of Pr. El Mostapha Aboulamid, includes the exchange of staff and students. It is directed by F. Rousseau and F. Pétrot at TIMA.

- Tallin University, Estonia
  This cooperation includes the exchange of students. The cooperation contact is Pr. Raimund Ubar.

- University of Ancona, Italy
  This cooperation takes place in the framework of an ERASMUS project; between France and Italy. The cooperation contact is Pr. Massimo Conti.

Participation to Committees for Conferences and Workshops

<table>
<thead>
<tr>
<th>Conferences and Workshops in 2008</th>
<th>Location</th>
<th>Role</th>
<th>Name</th>
</tr>
</thead>
</table>
| Design of Circuits and Integrated Systems Conference (DCIS): | Grenoble, France | Techn. Prog. Chair | L. Anghel  
Special Session | R. Leveugle  
Special Session | G. Sicard  
Special Session | L. Fesquet  
Special Session | S. Mir  
Special Session | N. Zergainoh  
Plenary Sessions | M. Nicolaidis  
Plenary Sessions | R. Velazco |
| Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP): | Nice, France | General Chair | B. Courtois  
Program Committee | S. Basrour |
| European Conference on Radiation and its Effects on Components ans Systems (RADECS): | Playa del Carmen, Mexico | Co-President | R. Velazco |
| Forum on specification & Design Languages (FDL): | Stuttgart, Germany | Track Chair | D. Borrione  
Program Committee | L. Pierre |
| IEEE Annual Symposium on VLSI (ISVLSI): | Montpellier, France | Program Committee | D. Borrione  
Program Committee | L. Pierre |
| IEEE Design and Technology of Integrated Systems (DTIS): | Tozeur, Tunisia | Program Committee | R. Leveugle  
Europe Liaison Committee | S. Mir |
| IEEE European Test Symposium (ETS): | Verbania, Italy | Topic Chair | R. Leveugle  
Program Committee | S. Mir |
| IEEE International Conference on Signals, Circuits & Systems (SCS): | Hammamet, Tunisia | Program Committee | R. Leveugle |
| IEEE International On-Line Testing Symposium (IOLT): | Rhodes, Greece | Publicity Chair | L. Anghel  
Program Committee | R. Leveugle  
Audio-Visual Chair | E. Simeu  
Vice-General Chair | R. Velazco  
Publications | N. Zergainoh  
Program Committee | H. Stratigopoulos |
<p>| IEEE International Design &amp; Test Workshop (IDT): | Monastir, Tunisia | Program Committee | L. Pierre |
| IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC): | Newcastle, | Program Committee | L. Fesquet |
| IEEE International Symposium Defect and Fault Tolerance in VLSI Systems (DFT): | Cambridge, Ma., USA | Program Committee | R. Leveugle |</p>
<table>
<thead>
<tr>
<th>Event</th>
<th>Location</th>
<th>Roles</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEEE International Test Conference (ITC):</td>
<td>Santa Clara, USA</td>
<td>Topic Chair: S. Mir</td>
</tr>
<tr>
<td>IEEE Latin American Test Workshop (LATW):</td>
<td>Puebla, Mexico</td>
<td>Program Committee: L. Anghel; Steering Committee: R. Velazco; Co-Chair: R. Velazco</td>
</tr>
<tr>
<td>IEEE VLSI Test Symposium (VTS):</td>
<td>San Diego, Ca., USA</td>
<td>New Topics Panels: B. Courtois; Hot Topics and Embedded Tutorials: L. Anghel; Steering Committee: M. Nicolaidis</td>
</tr>
<tr>
<td>IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS):</td>
<td>Bratislava</td>
<td>Program Committee: D. Borrione; Program Committee: R. Velazco</td>
</tr>
<tr>
<td>International Conference on Design Automation and Test in Europe (DATE):</td>
<td>Munich, Germany</td>
<td>Chair of sponsors committee: B. Courtois; Program Committee: D. Borrione; Topic Chair: S. Mir; Moderator of Security building blocks: L. Anghel; Moderator of Fault tolerant techniques: R. Velazco; Program Committee: L. Fesquet; F. Pétrot</td>
</tr>
<tr>
<td>International Conference on Formal Methods in Computer Aided Design (FMCAD):</td>
<td>Portland, USA</td>
<td>Program Committee: D. Borrione</td>
</tr>
<tr>
<td>Symposium on Integrated Circuits and Systems Design (SBCCI):</td>
<td>Gramado, RS Brazil</td>
<td>Program Committee: D. Borrione</td>
</tr>
<tr>
<td>IEEE Ph.D. Research In Microelectronics and Electronics (PRIME):</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IEEE Workshop on Design for Reliability and Variability (DRVW):</td>
<td>Santa Clara, Ca., USA</td>
<td>General Chair: M. Nicolaidis; Program Committee: L. Anghel</td>
</tr>
<tr>
<td>International Conference on Very Large Scale Integration (VLSI-SoC):</td>
<td>Rhodes, Greece</td>
<td>Steering Committee: S. Mir</td>
</tr>
<tr>
<td>International School on the Effects of Radiation on embedded Systems for Space Applications (SERESSA):</td>
<td>Mexico</td>
<td>General Chair: R. Velazco; Finance Chair: L. Anghel; Co-President: R. Velazco</td>
</tr>
<tr>
<td>International Workshop on Dependable Circuit Design (DECIDE):</td>
<td>Florida, USA</td>
<td>General Chair: R. Velazco; Finance Chair: L. Anghel</td>
</tr>
<tr>
<td>Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC):</td>
<td>Washington DC, USA</td>
<td>Program Committee: R. Leveugle</td>
</tr>
<tr>
<td>The Fourth International Symposium on Electronic Design, Test &amp; Applications (DELTA):</td>
<td>Hong Kong</td>
<td>Program Committee: R. Leveugle</td>
</tr>
<tr>
<td>Workshop on Dependable &amp; Secure Nanocomputing (WDSN):</td>
<td>Edimburg</td>
<td>Program Committee: R. Leveugle</td>
</tr>
<tr>
<td>IEEE Rapid Prototyping Workshop (RSP)</td>
<td>Porto Alegre, Brazil</td>
<td>Program Committee: F. Pétrot</td>
</tr>
<tr>
<td>IEEE International NoC Symposium</td>
<td>Newcastle, UK</td>
<td>Program Committee: F. Pétrot</td>
</tr>
<tr>
<td>IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP):</td>
<td>Montréal, Quebec, Canada</td>
<td>Program Committee: F. Rousseau</td>
</tr>
<tr>
<td>Journées Francophones en Systèmes Hétérogènes</td>
<td>Montebello, Quebec, Canada</td>
<td>Committee: F. Pétrot</td>
</tr>
</tbody>
</table>
Organisation of Conferences

<table>
<thead>
<tr>
<th>Conferences and Workshops in 2008</th>
<th>Location</th>
<th>Role</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design of Circuits and Integrated Systems Conference (DCIS):</td>
<td>Grenoble, France</td>
<td>General Chair</td>
<td>R. Velazco</td>
</tr>
<tr>
<td>IEEE International On-Line Testing Symposium (IOLT):</td>
<td>Rhodes, Greece</td>
<td>General Chair</td>
<td>M. Nicolaidis</td>
</tr>
<tr>
<td>International School on the Effects of Radiation on embedded Systems for Space Applications (SERESSA):</td>
<td>Mexico</td>
<td>General Chair</td>
<td>R. Velazco</td>
</tr>
<tr>
<td>International Workshop on Dependable Circuit Design (DECIDE):</td>
<td>Florida, USA</td>
<td>General Chair</td>
<td>R. Velazco</td>
</tr>
<tr>
<td>IEEE Workshop on Design for Reliability and Variability (DRVW):</td>
<td>Santa Clara, Ca., USA</td>
<td>General Chair</td>
<td>M. Nicolaidis</td>
</tr>
<tr>
<td>IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW):</td>
<td>Vancouver, Canada</td>
<td>Program Co-chair</td>
<td>S. Mir</td>
</tr>
</tbody>
</table>

Participation to Societies and Working Groups

- Member of IEEE/CS, IEEE/TTTC, IEEE/CPMT, ACM, IMAPS
- Member of IEEE European Test Technology Technical Committee
- Vice-Chair of the IEEE Computer Society Test Technology Technical Council
- Vice-Chair of Technical Activities of the IEEE Computer Society Test Technology Technical Council
- Chair of Thermal Testing Activities of the IEEE Test Technology Technical Council
- Member of IFIP 10.5 Working Group (D. Borrione)
- Member of the Scientific Community Council of the European Nanoelectronics Initiative Advisory Council
- Chapter Chair of the IEEE Solid-State Circuit society (Laurent Fesquet)
- Member of the Scientific Committee Council of the ENIAC (F. Pétrot)

Awards and distinctions

- Best Paper Award (Silver Leaf) at the PRIME’08 Conference (E. Yahya)
- Distinction « Chevalier dans l’Ordre des Palmes Académiques » (R. Leveugle)
12. Educational tasks

Dealing with problems risen by advanced technologies and proposing advanced design and test methodologies, TIMA staff members are, as a matter of course, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into three categories: courses and tutorials, seminars, direction of Ph.D. students employed by French industrial companies (CIFRE program).

Courses and tutorials

The following table lists courses and tutorials that have been organized and given by members of the Laboratory, at different institutions request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA staff or externally.

<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Speakers</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIDEP</td>
<td>Inp Grenoble France</td>
<td>Janv/08</td>
<td>8h</td>
<td>L. Anghel</td>
<td>Introduction to VLSI</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>Inp Grenoble France</td>
<td>Janv/08</td>
<td>15h</td>
<td>K. Morin-Allory</td>
<td>VHDL and synthesis</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>Inp Grenoble France</td>
<td>Feb/08 &amp; March/08</td>
<td>17h30</td>
<td>D. Borrione, K. Morin-Allory</td>
<td>VHDL and synthesis</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>Inp Grenoble France</td>
<td>Feb/08</td>
<td>18h</td>
<td>L. Anghel</td>
<td>Test of Digital Circuits</td>
</tr>
<tr>
<td>Formation Physique et caractérisation des composants MOS</td>
<td>Inp Grenoble France</td>
<td>June/08</td>
<td>3 h</td>
<td>G. Sicard</td>
<td>Notions de conception de Circuits intégrés</td>
</tr>
<tr>
<td>Formation Physique du transistor</td>
<td>Inp Grenoble France</td>
<td>Sept/08</td>
<td>5 h</td>
<td>G. Sicard</td>
<td>Conception de Circuits Analogiques</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>Inp Grenoble France</td>
<td>Sep/08</td>
<td>20h</td>
<td>P. Amblard</td>
<td>Digital circuit design</td>
</tr>
<tr>
<td>ENSAT</td>
<td>Tunis, Tunisia</td>
<td>Oct/08</td>
<td>16h</td>
<td>A. ElMrabti</td>
<td>System Level Design</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>INPG Grenoble France</td>
<td>Nov/08</td>
<td>20h</td>
<td>G. Sicard</td>
<td>Conception de Circuits Analogiques</td>
</tr>
<tr>
<td>SERESSA 2008 (Summer School)</td>
<td>Palm Beach, USA</td>
<td>Dec/08</td>
<td>2h</td>
<td>L. Anghel</td>
<td>Digital Circuits Evaluation by Multiple Fault injection Simulations</td>
</tr>
<tr>
<td>SERESSA 2008 (Summer School)</td>
<td>Palm Beach, USA</td>
<td>Dec/08</td>
<td>2h</td>
<td>R. Velazco</td>
<td>Error rate prediction</td>
</tr>
<tr>
<td>Continuous education training &quot;MATRI&quot;</td>
<td>Inp Grenoble France</td>
<td>Dec/08</td>
<td>7h</td>
<td>D. Borrione</td>
<td>Systems on chip Verification Methods</td>
</tr>
</tbody>
</table>
Seminars

The following table lists seminars given by members of the Laboratory on their specific research work (internal seminars).

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Chureau (SLS team)</td>
<td>15/05/2008</td>
<td>SPIRIT IP-XACT: format d'échange de blocs IP... et un peu plus</td>
</tr>
<tr>
<td>A. Helmy (VDS team)</td>
<td>22/05/2008</td>
<td>Vérification d'infrastructures de communication</td>
</tr>
<tr>
<td>Livier Lizarraga (RMS/SLS teams)</td>
<td>19/06/2008</td>
<td>DFT pour les imageurs CMOS</td>
</tr>
<tr>
<td>P. Ferin (SLS team)</td>
<td>26/06/2008</td>
<td>Accélération vidéo</td>
</tr>
<tr>
<td>P. Maistri (ARIS team)</td>
<td>03/07/2008</td>
<td>Erreurs et fiabilité dans systèmes embarqués de chiffrement</td>
</tr>
<tr>
<td>A. Bounceur (RMS team)</td>
<td>24/07/2008</td>
<td>Plateforme CAO pour l'évaluation de test des circuits mixtes et RF</td>
</tr>
</tbody>
</table>

In addition to internal seminars, the Laboratory regularly invites people from Grenoble academic and industrial environment to attend the talks given by our visiting researchers. These people have recently had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dr. L. Gonnord</td>
<td>CITI, Lyon, France</td>
<td>27/03/08</td>
<td>Analyses de propriétés quantitatives de programmes</td>
</tr>
<tr>
<td>Dr. M. Belarbi</td>
<td>Université Ibn Khaldoun de Tiaret- Algérie</td>
<td>06/02/08</td>
<td>Thématique de recherche de l’équipe Méthodes Formelles et Systèmes Embarqués et Temps-Réal</td>
</tr>
<tr>
<td>Dr. Boulé</td>
<td>Université McGill, Montréal, Québec, Canada</td>
<td>18/02/08</td>
<td>L’outil MBAC et la synthèse de circuits vérificateurs d’assertions</td>
</tr>
<tr>
<td>Prof. S. Almukhaizim</td>
<td>Computer Engineering, Kuwait University</td>
<td>03/04/08</td>
<td>Coping with Soft Errors in Asynchronous Burst-Mode Machines</td>
</tr>
<tr>
<td>Prof. R. Reis</td>
<td>Federal University of Rio Grande do Sul, Brasil</td>
<td>10/04/08</td>
<td>Physical Design Automation at Transistor Level</td>
</tr>
<tr>
<td>Prof. G. Wilke</td>
<td>UFRGS, Porto Alegre, Brazil</td>
<td>10/04/08</td>
<td>Improving mesh-based clock distribution architectures</td>
</tr>
<tr>
<td>Prof. S. OZEV</td>
<td>Electrical Engineering Dept. at Duke University, USA</td>
<td>04/07/08</td>
<td>Effective Test and Design Approaches for Radiofrequency Transceivers</td>
</tr>
<tr>
<td>Prof. D. De Venuto</td>
<td>Politecnico di Bari, Italy</td>
<td>28/11/08</td>
<td>Design and Test of DNA Sensor Arrays</td>
</tr>
<tr>
<td>Prof. Marvasti</td>
<td>Université Sharif de Téhéran</td>
<td>06/01/09</td>
<td>Sparse Signal Processing</td>
</tr>
</tbody>
</table>
Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions:

<table>
<thead>
<tr>
<th>Institution</th>
<th>Location</th>
<th>Date</th>
<th>Speaker</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated Microsystems Laboratory</td>
<td>McGill, Montreal, Canada,</td>
<td>10/01/08</td>
<td>D. Borrione</td>
<td>Horus: Provably Correct Construction for on-line Verification of Logical and Temporal Properties</td>
</tr>
<tr>
<td>INAOE</td>
<td>Puebla, Mexico</td>
<td>01/03/08</td>
<td>L. Anghel</td>
<td>Complex Digital Circuits Evaluation through Fault Injection</td>
</tr>
<tr>
<td>France Télénom R&amp;D</td>
<td>Meylan, France</td>
<td>23/04/08</td>
<td>L. Fesquet</td>
<td>Asynchronous secure FPGA, the future of configurable smart-card</td>
</tr>
<tr>
<td>IMEP-LHAC</td>
<td>Grenoble</td>
<td>15/05/08</td>
<td>S. Basrour</td>
<td>MEMS approach for microsources of energy</td>
</tr>
<tr>
<td>McGill University</td>
<td>Montréal, Canada</td>
<td>00/03/08</td>
<td>K. Morin-Allory</td>
<td>A proof of correctness for the construction of property monitors</td>
</tr>
<tr>
<td>Cambridge University</td>
<td>Cambridge, UK</td>
<td>00/06/08</td>
<td>L. Pierre</td>
<td>ACL2-based verification of NoC communication infrastructures</td>
</tr>
<tr>
<td>Facultad de Ingenieria, Univ. de la Republica</td>
<td>Montevideo, Uruguay</td>
<td>22/09/08</td>
<td>R. Velazco</td>
<td>Predicting transient error rates due to radiation for processor-based digital architectures</td>
</tr>
<tr>
<td>Cluster MNS</td>
<td>Grenoble</td>
<td>9/10/08</td>
<td>S. Basrour</td>
<td>Micropower generators and sources</td>
</tr>
<tr>
<td>Pontificia Univ. Catolica de Peru</td>
<td>Lima, Peru</td>
<td>00/10/08</td>
<td>R. Velazco</td>
<td>Managing transient effects of radiation on complex microelectronic systems</td>
</tr>
<tr>
<td>RECAP Workshop</td>
<td>Toulouse, France</td>
<td>13-14/11/08</td>
<td>S. Basrour</td>
<td>MicroPower Generators and ULP management electronics control</td>
</tr>
</tbody>
</table>
University/industry joint research programs

A French national program, called CIFRE, allows French companies to host Ph.D. students. The thesis director must belong to a French University or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company.

TIMA researchers have been asked by companies to direct several Ph.D. theses in the CIFRE framework. The most recent ones are listed in the table below.

<table>
<thead>
<tr>
<th>Company / Institute</th>
<th>Student</th>
<th>Ph D. Advisor</th>
<th>Dur.</th>
<th>Research Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>STMicroelectronics</td>
<td>T. Baron</td>
<td>S. Basrour</td>
<td>Feb. 2008</td>
<td>Development of inertial sensors on thin SOI</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>A. Asquini</td>
<td>S. Mir</td>
<td>Feb. 2008</td>
<td>Auto test circuit development for frequency synthesizers and RF power amplifiers based on fault modelling</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>J. Goulier</td>
<td>M. Renaudin/ L. Fesquet</td>
<td>May 2008</td>
<td>Reconfigurable Analog to Digital converters for multistandard reception systems</td>
</tr>
<tr>
<td>CEA LETI</td>
<td>S. Miermont</td>
<td>M. Renaudin</td>
<td>Oct. 2008</td>
<td>Architectures asynchrones à tension d'alimentation autorégulées pour optimisation de la consommation électrique</td>
</tr>
<tr>
<td>FT R&amp;D</td>
<td>J. Hamon</td>
<td>M. Renaudin/L. Fesquet</td>
<td>Oct. 2008</td>
<td>Low power UWB tranceivers</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>F. Abouzeid</td>
<td>M. Renaudin / G. Sicard</td>
<td>Sept. 2010</td>
<td>Subthreshold architecture and digital circuits study in 45 &amp; 32nm CMOS technology</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>N. Ben Hassine</td>
<td>S. Basrour</td>
<td>Oct. 2009</td>
<td>Reability of BAW resonators</td>
</tr>
<tr>
<td>EADS</td>
<td>A. Bougerol</td>
<td>R. Leveugle</td>
<td>Sept. 2011</td>
<td>Study of failure modes induced par natural radiative environment on memory based complex devices</td>
</tr>
</tbody>
</table>
13. Publications

PUBLICATIONS 2008

Book Chapters

ANGHEL L., NICOLAIDIS M.
Cost Reduction and Evaluation of a Temporary Faults Detecting Technique
chapter in Design, Automation, and Test in Europe - The Most Influential Papers of 10 Years DATE,
Lauwereins, Rudy; Madsen, Jan (Eds.), Springer, 2008

ANGHEL L., NICOLAIDIS M.
Defects Tolerant Logic Gates for Unreliable Future Nanotechnologies
chapter in the "Computational and Ambient Intelligence", Book Series Lecture Notes in Computer
Science, Springer Berlin / Heidelberg ISSN0302-9743, 2008

AUGÉ I.*, PÉTROT F.
User Guided High Level Synthesis
Chapter in P. Coussy & A. Moraviec (eds.) High Level Synthesis, from Algorithm to Digital Circuit

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* Université Pierre et Marie Curie, Équipe ASIM/LIP6, UPMC-LIP6/SoC, Paris, France

CHAUDHURI S., HOOGVORST PH., GUILLEY S., DANGER J.-L., BEYROUTHY T., RAZAFINDRAIBE A.,
FESQUET L., RENAUDIN M.*
Physical Design of FPGA Interconnect to Prevent Information Leakage
Chapter in "Reconfigurable Computing: Architecture, Tools, and Applications", 4th International

----------

* FT R&T; ** TIEMPO SAS, Grenoble, France

MORIN-ALLORY K., FESQUET L., BORRIONE D.
Asynchronous online monitoring of logical and temporal assertions
Chapter in “Embedded Systems Specification and Design Languages”, to be published by Springer,
Selected papers from FDL 2007, Series: Lecture Notes in Electrical Engineering , Vol. 10, Villar Eugenio

Journals

ABRIL A.*, MEHREZ H.*, PÉTROT F., GOBERT J.**, MIRO C.**
Estimation et optimisation de la consommation dans les SoC utilisant la simulation précise au cycle

----------

* LIP6 ; **Philips Digital Systems Laboratory

BEN HASSINE N. ***, MERCIER D.*, RENAU PX PH.*, CHAPPAZ C.**, BASROUR S., DEFAY E.*
Linear variation of Aluminum Nitride capacitance versus voltage induced by a piezoelectric-
electrostrictive coupling
N. Ben Hassine, D. Mercier, Ph. Renaux, C. Chappaz, S. Basrour,

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*CEA-LETI/MINATEC, DRT/DIHS, Grenoble, France ; **STMicroelectronics, Crolles, France

DHAYNI A., MIR S., RUFER L., SIMEU E., BOUNCEUR A.
Pseudorandom BiST for test and characterization of linear and nonlinear MEMS
KRIAA L., BOUCHHIMA A., GLIGOR M., FOUILLART A.-M.*, PÉTROT F., JERRAYA AA.**
Parallel Programming of Multi-Processor SoC : A HW-SW Interface perspective
February 2008

* THALES, Land & Joint Systems EDS/DHD 146, Colombes, France; **CEA-LETI, Grenoble, France

KOLODIS E., NICOLAIDIS M.
Towards a Holistic CAD Platform for Nanotechnologies

LALINKSY G. T.*, RUFER L., VANKO G.*, MIR S., HASCIK S.*, MOZOLOVA Z.*, VINCZE A.*, UHEREK F.*
AlGaN/GaN heterostructure based surface acoustic wave structures for chemical sensors

MAISTRI P., LEVEUGLE R.
Double-Data-Rate computation as a countermeasure against fault analysis

MARZENCKI M., AMMAR Y., BASROUR S.
Integrated power harvesting system including a MEMS generator and a power management circuit

METZGER M.*, ANANE A., ROUSSEAU F., VACHON J., ABOULHAMID E. M.
Introspection Mechanisms for Runtime Verification in a System-Level Design Environment

* University of Montreal, Canada

PIERRE L., FERRO L.
A Tractable and Fast Method for Monitoring SystemC TLM Specifications

POPOVICI K., GUERIN X., ROUSSEAU F., PAOLUCCI P. S., JERRAYA A. A.*
Platform based Software Design Flow for Heterogeneous MPSoC

* CEA-LETI, Grenoble, France

QAISAR S.-M., FESQUET L., RENAUDIN M.*
An Adaptive Resolution Computationally Efficient Short-Time Fourier Transform

* TIEMPO SAS, Grenoble, France

SCHMALTZ J.*, BORRIONE D.
A functional formalization of on chip communications

* Institute for Computing and Information Sciences, Radboud University, Nijmegen, The Netherlands

SHEIBANYRAD A., GREINER A.*, MIRO-PANADES I.**
Multisynchronous and Fully Asynchronous NoCs for GALS Architectures

* Laboratoire d'Informatique de Paris 6, France ; ** French Atomic Energy Commission, Grenoble

SIMEU E., NGUYEN H.N., CAUVET P.*, MIR S., RUFER L., KHEREDDINE R.
Using signal envelope detection for online and offline RF MEMS switch testing

* NXP Semiconductors, 2 Rue de la Girafe, BP 5120, 14079 Caen Cedex 5, France
STRATIGOPULOS H.-G., MAKRIS Y.*
Error moderation in low-cost machine-learning-based analog/RF testing
* Dept of Electrical Engineering and Dept of Computer Science, Yale Univ., New Haven, USA

International Conferences and Workshops

ALSAYEG K., FESQUET L., SICARD G., RIOS D., M. RENAUDIN*
Synthesis of asynchronous QDI FSM based on optimized sequencers
34th European Conference on Solid-States Circuits (ESSCIRC’08), ESS Fringe Session, Edinburgh, Scotland,
September 16, 2008
* TIEMPO SAS, Grenoble, France

ASQUINI A., BADETS F., MIR S., CARBONERO J.L., BOUZAIDA L.
PFD output monitoring for RF PLL BIST
14th IEEE International Mixed-Signals, Sensors and Systems Test Workshop, Vancouver, Canada, June 2008

ATAT Y.*, ZERGAINOH N.-E.
Automatic Code Generation for MPSoC Platform Starting From Simulink/Matlab : New Approach to
Bridge the Gap between Algorithm and Architecture Design
3rd International Conference on Information and Communication Technologies: From Theory to
Applications (ICTTA’08), Damascus, Syria, April 7-11, 2008
* LIU University CCE Dept, Beirut Lebanon

A Secure Programmable Architecture with a Dedicated Tech-mapping Algorithm: Application to a Crypto-
Processor
23rd International Conference on Design of Circuits and Integrated Systems (DCIS’08), Grenoble,
France, November 12-14, 2008
* ENST, France

BORGIONE D., HELMY A., PIERRE L., SCHMALTZ J.
Executable Formal Specification and Validation of NoC Communication Infrastructures
Proc. of 21st Symposium on Integrated Circuits and Systems Design, Gramado (Brazil), September 1-4, 2008

BOUSSETTA H., MARZENCKI M., BASROUR S.
Top-Down Behavioral Modeling Methodology of A Piezoelectric Microgenerator For Integrated Power
Harvesting Systems
Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP’08), Nice, France, April 2008

Extending the Use of Failure Maps for FPGA Based Applications: A Case Studied
23rd International Conference on Design of Circuits and Integrated Systems (DCIS’08), Grenoble,
France, November 12-14, 2008
* Universidad Nacional de Córdoba e Instituto Universitario Aeronáutico ; **InstitutoUniversitario
Aeronáutico
CANIVET G., CLÉDIERE J.*, FERRON J.B., VALETTE F.**, RENAUDIN M.***, LEVEUGLE R.
Detailed analyses of single laser shot effects in the configuration of a Virtex-II FPGA
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* CESTI/CEA-LETI, France ; ** DGA/CELAR, France ; *** Tiempo, France

CANIVET G., CLEDIERES J.*, VALETTE F.**, RENAUDIN M.***, LEVEUGLE R.
Intentional Attacks on SRAM-based FPGAs
23rd International Conference on Design of Circuits and Integrated Systems (DCIS’08), Grenoble, France, November 12-14, 2008
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* CESTI/CEA-LETI, France ; ** DGA/CELAR, France ; *** Tiempo, France

CARLIOZ L., DELAMARE J., BASROUR S.
Energy scavenging using hybrid thermo-magnetic / PZT structure
Joint European Magnetics Symposia (JEMS’08), Dublin, Ireland, September 2008

CARLIOZ L., DELAMARE J., BASROUR S., POULIN G.
Hybridization of Magnetism and Piezoelectricity for an Energy Scavenger based on Temporal Variation of Temperature
Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP’08), Nice, France, April 2008

CHAUDHURI S., HOOGVORST PH., GUILLEY S., DANGER J.-L., BEYROUTHY T., RAZAFINDRAIBE A., FESQUET L., RENAUDIN M.*
Physical Design of FPGA Interconnect to Prevent Information Leakage
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* FT R&T; ** TIEMPO SAS, Grenoble, France

COURTOIS B., CHARLOT B., DI PENDINA G., RUFER L.
Electronics manufacturing infrastructures for education and commercialization (Poster)

COURTOIS B., CHARLOT B., DI PENDINA G., RUFER L.
Infrastructures for mixed signals in biology and medicine
14th IEEE Int. Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW’08), Vancouver, Canada, June 2008

DEMONTES L.*, BONACIU M., AMBLARD P.
Software for Multi Processor System on Chip: moving from generic RISC platforms to CELL
Rapid System Prototyping Symposium (RSP’08), Monterey, Cal, USA, June 2-5, 2008
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*INRIA Rhône-Alpes

EXCOFFON C., MAISTRI P., R. LEVEUGLE
Software-based BIST capabilities of the Advanced Encryption Standard

FERRO L., PIERRE L., LEDRU Y.*, DU BOUSQUET L.*
Generation of Test Programs for the Assertion-Based Verification of TLM Models
Proc. IEEE International Design and Test Workshop (IDT’08), Monastir (Tunisia), December 20-21, 2008
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* LIG (CNRS-INPG-UJF), Grenoble, France

Methodologies and Tools for the Evaluation of the Sensitivity to Radiation of SRAM-based FPGAs
23rd International Conference on Design of Circuits and Integrated Systems (DCIS’08), Grenoble, France, November 12-14, 2008
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*IMS, UMR CNRS 5218 ; **EADS ; ***Université Catholique de Louvain (ICL), Belgium
GERIN P., GUÉRIN X., PÉTROT F.
Efficient implementation of native software simulation for MPSoC
Design Automation and Test in Europe (DATE’08), Munich, Germany, March 10-14, 2008

GUIRONNET de MASSAS P., PÉTROT F.
Comparison of memory write policies for NoC based Multicore Cache Coherent Systems
Design Automation and Test in Europe (DATE’08), Munich, Germany, March 10-14, 2008

HAMON J., FESQUET L., MISCOPEIN B.*, RENAUDIN M.**
High-Level Time-Accurate Model for the Design of Self-Timed Ring Oscillators
14th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC’08), Newcastle upon Tyne, UK, 7th - 11th April 2008
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*Orange Labs - France Telecom R&D, Grenoble, France ; **TIEMPO SAS, Grenoble, France

HAMON J., MISCOPEIN B.*, SCHWOERER J.*, FESQUET L., RENAUDIN M.**
Self-Timed Implementation of an Impulse Radio Synchronisation Acquisition Algorithm
Conference on Design and Architectures for Signal and Image Processing (DASIP’08), Bruxelles, Belgium November 24 -26, 2008
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*Orange Labs - France Telecom R&D, Grenoble, France ; **TIEMPO SAS, Grenoble, France

JEAN-MISTRAL C., BASROUR S., CHAILLOUT J J.
Dielectric polymer: scavenging energy from human motion
Electroactive Polymer Actuators and Devices (EAPAD’08), San Diego, USA, March 9-13, 2008

KHEREDDINE R., SIMEU E., MIR S.
RF transceiver parameter identification using regressive models
Design and Technology of Integrated Systems (DTIS’08), Tozeur, Tunisie, March 2008

KOUADRI A., SENOUCI B., PETROT F.
Networks-In-Package: Performances management and design methodology

KOUADRI A., SENOUCI B., PETROT F.
Large Scale On-Chip Networks : An Accurate Multi-FPGA Emulation Platform
11th EUROMICRO Conference on Digital System Design Architectures Methods and Tools, Parma, Italy, September 3-5, 2008

KUPKA L.*, SIMEU E., STRATIGOPOULOS H., RUFER L., MIR S., TUMOVA O.*
Signature analysis for MEMS pseudorandom testing using neural networks
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* University of West Bohemia in Pilsen, Czech Republic

LABONNE E., ROLLAND R., SICARD G.
A Standard 3.5T CMOS Imager including a Light Adaptive System for Integration Time Optimisation
Conference on Design and Architectures for Signal and Image Processing (DASIP’08), Bruxelles, Belgium, November 24-26, 2008

Surface Acoustic Wave Excitation on SF6 plasma treated AlGaN/GaN heterostructure
12th Joint Vacuum Conference, 10th European Vacuum Conference, 7th Annual Meeting of the German Vacuum Society, Balatonalmádi, Lake Balaton - Hungary, September 22-26, 2008
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* Institute of Electrical Engineering of the Slovak Academy of Sciences, Bratislava, Slovakia ; ** Slovak University of Technology, Faculty of Electrical Engineering and Information Technology, Department of Microelectronics, Bratislava, Slovakia; *** International Laser Center, Bratislava, Slovakia

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* Institute of Electrical Engineering of the Slovak Academy of Sciences, Bratislava, Slovakia ; ** Slovak University of Technology, Faculty of Electrical Engineering and Information Technology, Department of Microelectronics, Bratislava, Slovakia ; *** International Laser Center, Bratislava, Slovakia


*University of Cantabria, Spain


MORENO E.*, POPOVICI K., CALAZANS N.*, JERRAYA A.A.** Integrating Abstract NoC Models within MPSoC Design Rapid System Prototyping Symposium (RSP’08), Monterey, Cal, USA, June 2-5, 2008

*PUCRS, Brazil; **CEA-LETI, France

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MORIN-ALLORY K., BOULÉ M.*, BORRIONE D., ZILIC Z.**
Proving and Disproving Assertion Rewrite Rules by Automated Theorem Proving
Proc. of IEEE International High Level Design Validation and Test Workshop (HLDVT'2008), Lake Tahoe, November 19-21, 2008
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* McGill University (Canada)

NICOLAIDIS M.
Special Session 2: Benchmarking and Standardization in Software-Based SER Characterization: Towards an IEEE Task Force?
14th IEEE International Symposium On-Line Testing (IOLTS’08), Rhodes, Greece, July 7-9, 2008

NICOLAIDIS M.
On the State of Superposition and the Parallel or not Parallel Nature of Quantum Computing: a controversy raising view point
European Computing and Philosophy Conference (E-CAP’08), Montpellier, France, June 16-18, 2008

NICOLAIDIS M., PEREZ R.*, ALEXANDRESCU D.*
Low-Cost Highly-Robust Hardened Storage Cells Using Blocking Feedback Transistors
IEEE VLSI Test Symposium (VTS’08), San Diego, California, USA, April 27-May 01, 2008
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* iRoC Technologies

ODDOS Y., MORIN-ALLORY K., BORRIONE D.
Assertion-Based Design with Horus

ODDOS Y., MORIN-ALLORY K., BORRIONE D.
Assertion-Based Verification and On-line Testing in Horus
Proc. IEEE International Design and Test Workshop (IDT’08), Monastir, Tunisia, December 20-21, 2008

PERONNARD P., VELAZCO R., FOUCARD G.
Impact of the Software optimization on the Soft Error Rate: a case study
23rd International Conference on Design of Circuits and Integrated Systems (DCIS’08), Grenoble, France, November 12-14, 2008

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Predicting the SEU Error Rate through Fault Injection for a Complex Microprocessor
Dependable Design of Circuits for Critical Industrial Applications (D2CCIA), session organized within the IEEE International Symposium on Industrial Electronics (ISIE’2008), Cambridge, UK, June 30-July 2nd, 2008

Remote SEE testing capabilities with heavy-ion and laser beams at Cyclone-HIF and ATLAS facilities
IEEE Nuclear and Space Radiation Effects Conference (NSREC’08), Radiation effects Data Workshop, Tucson (Arizona), USA, July 14-18, 2008
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*IMS Laboratory, UMR CNRS 5218, Université Bordeaux 1, Talence, France; **Université catholique de Louvain, Cyclotron Research Center and Unité de Physique Nucléaire, Louvain-la-Neuve, Belgium

POPOVICI K., JERRAYA A. A.*
Multilevel communication modeling for multiprocessor System-on-Chip
International Symposium on VLSI Design Automation and Test (VLSI-DAT’08), Hsinchu, Taiwan, April 23-25, 2008
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*CEA-LETI, Minatec, Grenoble, France

POUGET V.*, DOUIN A.*, FOUCARD G., PERONNARD P., LEWIS D., FOUILLAT P., VELAZCO R.,
Dynamic Testing of an SRAM-Based FPGA by Time-Resolved Laser Fault Injection
14th IEEE International Symposium On-Line Testing (IOLTS’08), Rhodes, Greece, July 7-9, 2008
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*IMS Laboratory, UMR CNRS 5218, Université Bordeaux 1, Talence, France
QAISAR S.-M., FESQUET L., RENAUDIN M.*
Computationally efficient adaptive rate sampling and adaptive resolution analysis
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*TIEMPO SAS, Grenoble, France

QAISAR S.-M., FESQUET L., RENAUDIN M.*
An improved quality adaptive rate filtering technique based on the level crossing sampling
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*TIEMPO SAS, Grenoble, France

QAISAR S.-M., FESQUET L., RENAUDIN M.*
An improved quality filtering technique for time varying signals based on the level crossing sampling
IEEE International Conference of Signals and Electronic Systems 2008 (ICSES’08), Krakow, Poland, September 14-17, 2008
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* TIEMPO SAS, Grenoble, France

RUSU C., GRECU C.*, ANGHEL L.
Communication Aware Recovery Configurations for Networks-on-Chip
14th IEEE International Symposium On-Line Testing (IOLTS’08), Rhodes, Greece, July 7-9, 2008
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*University of British Columbia

RUSU C., GRECU C.*, ANGHEL L.
Coordinated versus Uncoordinated Checkpoint Recovery for Network-on-Chip based Systems
4th IEEE International Symposium on Electronic Design, Test and Applications (DELTA’08), Hong Kong, January 23-25, 2008
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*University of British Columbia

RUSU C., GRECU C.*, ANGHEL L.
Improving the Scalability of Checkpoint Recovery for Networks-on-Chip
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*University of British Columbia

RUSU C., GRECU C.*, ANGHEL L.
Blocking and Non-blocking Checkpointing for Networks-on-Chip
2nd IEEE Workshop on Dependable and Secure Nanocomputing (WDSN’08), Anchorage, Alaska, USA, June 27, 2008
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*University of British Columbia

RUSU C., GRECU C.*, ANGHEL L.
Efficient Coordinated Checkpointing Recovery Schemes for Network-on-Chip based Systems
2nd International Workshop on Dependable Circuit Design (DECIDE’08), Playa del Carmen, Mexico, November 27-29, 2008
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*University of British Columbia

SENOUCI B., KOUADRI A., ROUSSEAU F., PETROT F.
Multi-CPU/FPGA Platform Based Heterogeneous Multiprocessor prototyping: New Challenges for Embedded Software Designers
Rapid System Prototyping Symposium (RSP’08), Monterey, Cal, USA, June 2-5, 2008

SHEN H., PÉTROT F.
MPSoC Communication Architecture Exploration Using an Abstraction Refinement Method
21st International conference on VLSI Design, Hyderabad, India, January 4-8, 2008

SHEN H., GERIN P., PÉTROT F.
Configurable Heterogeneous MPSoC Architecture Exploration Using Abstraction Levels
Rapid System Prototyping Symposium (RSP’08), Monterey, Cal, USA, June 2-5, 2008
STRATIGOPOULOS H., TONGBONG J., MIR S.
A general method to evaluate RF BIST techniques based on non-parametric density estimation
Design, Automation and Test in Europe Conference (DATE’08), Munich, Germany, March 10-14, 2008

VANHAUWAERT P., PORTOLAN M., LEVEUGLE R., ROCHE P.*
Usefulness and effectiveness of HW and SW protection mechanisms in a processor-based system
IEEE International Conference on Electronics, Circuits and Systems (ICECS’08), Saint Julians, Malta, September 1-3, 2008
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* STMicroelectronics

YAHYA E., RENAUDIN M.*
Optimal Asynchronous Linear-Pipelines
The fourth conference on Ph.D. Research in Microelectronics and Electronics (PRIME’08), Istanbul, Turkey, June 22-25, 2008 (Award: Best Paper Award (Silver Leaf))
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*TIEMPO SAS, Grenoble, France

YAHYA E., RENAUDIN M.*
AHMOSE: Towards a Circuit Level Solution for Process Variability
Design, Automation and Test in Europe Conference (DATE’08), Munich, Germany, March 10-14, 2008
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* TIEMPO SAS, Grenoble, France

YAHYA E., RENAUDIN M.*
Asynchronous Linear Pipelines: An Efficient-Optimal Pipelining Algorithm
15th IEEE International Conference on Electronics, Circuits and Systems (ICECS’08), Malta, August 31-September 03, 2008
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* TIEMPO SAS, Grenoble, France

YAHYA E., RENAUDIN M.*, LOPIN G.
Standard-Logic Quasi Delay Insensitive Registers
16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC’08), Rhodes Island, Greece, Pages:465-468, October 13-15, 2008
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*TIEMPO SAS, Grenoble, France

YAHYA E., RENAUDIN M.*
Asynchronous Linear-Pipeline with Time Variable Delays: Performance Modeling, Analysis and Slack Optimization
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* TIEMPO SAS, Grenoble, France

ZAKARIA H., FESQUET L., DURAND S., ALBEA-SANCHEZ C., THONNART Y., CANUDAS DE WIT C., MARCHAND N.
Integrated Asynchronous Regulation for Nanometric Technologies: Application to an Embedded Parallel System
MINATEC CROSSROADS’08, June 23-27, 2008, Grenoble, France

National Conferences

ANGHEL L., FESQUET L., MORIN-ALLORY K.
Initiation à la conception de VLSI numériques
10èmes Journées Pédagogiques de la Coordination Nationale pour la Formation en Micro et nanoélectronique (JPCNFMT’08), Saint-Malo, France, November 26-28, 2008

AKKOUCHE N., MIR S., SIMEU E., STRATIGOPOULOS H.
Réduction de tests fonctionnels en utilisant des techniques d’estimation non paramétrique
11th Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’08), Bordeaux, France, May 14-16, 2008
ARTHAUD Y., RUFER L., MIR S.
Capteur MEMS faible impédance mécanique haute sensibilité pour la chirurgie de l’oreille moyenne
Journées GDR MNS, Montpellier, France, December 03-05, 2008

CANIVET G.*, CLEDIERES J.*, LEVEUGLE R., RENAUDIN M.**, VALETTE F.***
Injection de fautes sur composant Virtex-II XC2V1000
11\textsuperscript{th} Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’08), Bordeaux, France,
May 14-16, 2008
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*CESTI/CEA-LETI, France ; **TIEMPO SAS, Grenoble, France ; ***DGA/CELAR, France

CHAGOYA A., GUERIN X., ROUSSEAU F.
Outils de génération de logiciel pour les systèmes sur puce multi-processeur hétérogènes
11\textsuperscript{th} Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’08), Bordeaux, France,
May 14-16, 2008

CLAVEL R., PIERRE L., LEVEUGLE R.
Premiers résultats sur l’utilisation d’ACL2 pour l’évaluation de la conséquence des erreurs logiques
2\textsuperscript{ème} Colloque du GdR SoC-SiP, Paris, France, June 4-6, 2008

DANG T., ANGHEL L., LEVEUGLE R.
Structures robustes pour circuits logiques à base de CNTFET
11\textsuperscript{th} Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’08), Bordeaux, France,
May 14-16, 2008

DUBOIS M., MANSOURI I., CHOUBA N.*, MIR S.
Calibrage automatique d’un convertisseur Sigma-Delta utilisant un BIST
11\textsuperscript{th} Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’08), Bordeaux, France,
May 14-16, 2008
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*STMicroelectronics, Tunis, Tunisie

HAMON J., MISCOPEIN B.*, SCHWOERER J.*, FESQUET L., RENAUDIN M.
Implémentation en logique asynchrone d’un algorithme de synchronisation de signaux radio impulsionnelle
7\textsuperscript{ème} journées d'études Faible Tension Faible Consommation, (FTFC’08), Université Catholique de
Louvain, Belgique, May 26-28, 2008
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* Orange Labs - France Telecom R&D, Grenoble, France

HELMY A., PIERRE L.
Formal Verification of the Communications in Networks on Chips
2\textsuperscript{ème} Colloque du GdR SoC-SiP, Paris, France, June 4-6, 2008

KHEREDDINE R., SIMEU E., MIR S.
Utilisation des modèles de régression pour l'identification des paramètres d’un transceiver RF
11\textsuperscript{th} Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM’08), Bordeaux, France,
May 14-16, 2008

RUFER L., ARTHAUD Y., MIR S., SCHMERBER S., DAUVÉ S., NOURY N.
Outil de monitoring per-opératoire dans la chirurgie de l’oreille moyenne
Journées du Groupement de Recherche de Micro et Nano Systèmes, Toulouse, France,
November 21-23 2007

RUSU C., GRECU C.*, ANGHEL L.
Network-on-Chip Fault Tolerance through Checkpoint and Rollback Recovery
National Symposium on System-on-Chip - System-in-Package (GdR SoC-SiP’08), Paris, France,
June 4-6, 2008
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*University of British Columbia

SCHMERBER S., ARTHAUD Y., RUFER L., MIR S.
Outils de monitoring per-opératoire de la biomécanique ossiculaire par micro-capteur en chirurgie
otologique - Etude de faisabilité (Poster)
115\textsuperscript{ème} Congrès de la Société Française d’Oto-Rhino-Laryngologie, Paris, France, October 12-14, 2008
VELAZCO R., PERONNARD P., FOUCARD G., FERNANDEZ S.*, PECHIAR J.*
A generic platform for SEE high altitude experiments,
Conference RADSSOL “Electronique et rayonnements naturels au niveau du sol », CNRS, Campus
Gérard Mégie, Paris June 11-12, 2008
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*UDELAR, Facultad de Ingenieria, Universidad de la Republica, Montevideo, Uruguay

Invited Conferences

BORRIONE D.
HORIZ: proven correct support for on-line property verification
FETCH'08, Ecole d'Hiver Francophone sur les Technologies de Conception des systèmes embarqués
HétérogènesMontebello, Québec, Canada, January 7-9, 2008

BORRIONE D.
Assertion Based Test
Forum on specification & Design Languages (FDL’08), Stuttgart, Germany, September 23-25, 2008

COURTOIS B., CHARLOT B., DI PENDINA G., RUFE L.
Infrastructures for education, research and industry: CMOS and MEMS for BioMed
The 12th World Multi-Conference on Systemics, Cybernetics and Informatics (WMSCI’08) Orlando,
USA, June 2008

FESQUET L., BEYROUTHY T.
A secure asynchronous configurable cell: an embedded programmable logic for smartcards
Workshop on Cryptographic Architectures embedded in reconfigurable devices (CryptArchi’08),
Tregastel, France, June 1-4, 2008

MIR S.
Evaluation of mixed-signal/RF DFT solutions for SiP devices using statistical techniques
Workshop on Reliability & DfX engineering for System-in-Package Technologies, Invited Talk, Pallanza,
Italy, May 2008

NICOLAIDIS M.
Fault Tolerant Architectures for Mitigating Variability Issues
Workshop: Impact of Process Variability on Design and Test, Design Automation and Test in Europe
(DATE’08), Munich, Germany, March 10-14, 2008

NICOLAIDIS M.
Dealing with soft errors in nanometric CMOS
Invited talk, 2008 Reliability and Design (Zuverlässigkeit und Entwurf - ZuE 2008), Ingolstadt, Germany,
September 29 – October 1, 2008

Theses

Katalin POPOVICI
Multilevel programming environment for heterogeneous MPSOC architectures

Pierre VANHAUWAERT
Fault-injection based dependability analysis in a FPGA-based environment
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – April 4, 2008

Aurélien BUHRIG
Optimization of the energy consumption in wireless sensor network nodes

Thomas BARON
NEMS inertial sensor Development on thin SOI and its integration with industrial process
Thèse de Doctorat UJF, spécialité Micro et Nano électronique – April 30, 2008

Julien GOULIER
Contribution to the design of continuous time delta sigma converters, from specifications to silicon.
Application to a wide band wireless standard
David RIOS  
Low power asynchronous systems  

Trong Trinh DANG  
CNTFET-based logic gates - characteristic dispersions and defect tolerance  

Claire JEAN-MISTRAL  
Scavenging energy with electroactive polymer for wireless autonomous sensor  
Thèse de Doctorat UJF, spécialité Micro et Nano électronique – October 8, 2008

Alexandre CHUREAU  
Definition of a Service-Based Intermediate Representation for Virtual Prototyping of Systems-on-Chip  
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – November 12, 2008

Livier LIZARRAGA  
BIST technique for CMOS imagers  
Thèse de Doctorat INPG, spécialité Micro et Nano électronique – November 27, 2008

Benaoumeur SENOUCI  
Fast MPSoC prototyping methodology on reconfigurable hardware platforms  

Habilitations à diriger des recherches

Laurent FESQUET  
Systèmes Intégrés Asynchrones et de Traitement des Signaux Non Uniformément Échantillonnés  
Habilitation à diriger des recherches, INPG – March 31, 2008

Gilles SICARD  
Conception de systèmes intégrés concurrents : Des capteurs de vision CMOS aux circuits intégrés sans horloge  
Habilitation à diriger des recherches, UJF – June 20, 2008

Patents

LEFEBVRE A., FEUILLEBOIS C., SIMEU E., BORTOLIN-ARGENTON E.  
Procédé de détection de défaillance d’un capteur analogique et dispositif de détection pour mettre en œuvre le dit procédé  
Brevet n°08/03.420, déposé le 19 juin 2008

MOREAU-GAUDRY A., BONVILAIN A.  
Dispositif d’intervention chirurgicale comprenant un instrument susceptible de se déformer  
Brevet n° FR0855617, déposé le 19/08/2008
14. Press articles and special events in 2008

Summary

► Asynchronous design startup closes first round of funding
EE TIMES
February 6, 2008

► DATE 2008
TIMA Exhibition at DATE
March 10-15, 2008

► Silver Prize in PRIME 2008
The fourth conference on Ph.D. Research in Microelectronics and Electronics (PRIME’08)
June 22-25, 2008

► A balloon is launched at 30000 meters with an experiment resulting from the cooperation of european and latin-american scientists
AFP Nuestro Pais
September 29, 2008

► Des vibrations capables de produire de l’énergie (projet VIBES à TIMA)
Les Echos
October 22, 2008

► EmSoc 2008
Villars de Lans, France,
October 23-24, 2008

► « Fête de la Science » in Grenoble
Tima Laboratory
November 2008

► Des circuits intégrés dans la stratosphère
« à savoir, Grenoble INP »,
December 15-26, 2008

► Régis Leveugle nommé Chevalier dans l’Ordre des Palmes Académiques
Distinction remise lors d’une cérémonie par Paul Jacquet,
March 3, 2009
Asynchronous design startup closes first round of funding

Anne-Francoise Pele
(02/06/2008 3:20 AM EST)
URL: http://www.eetimes.eu/france/206104852

PARIS — French startup Tiempo, specializing in the design of asynchronous ICs, has raised €1.1 million ($1.6 million) in an initial round of financing with venture capital firms Emertec Gestion and Schneider Electric Ventures.

Tiempo said the funds would be used to strengthen the development plan of the company's IP and EDA products but also to accelerate their commercialization worldwide.

Tiempo claims its solution allows semiconductor companies to design complex chips with ultra low power consumption and ultra low electromagnetic emission. It also contributes to reduce time-to-market by suppressing major design efforts on clock distribution and timing closure issues, and to increase productivity by improving the resistance of their circuits to the physical variations of the manufacturing technologies, the startup specified.

Tiempo noted that its portfolio of IPs includes asynchronous cores of microcontrollers, microprocessors, crypto-processors and miscellaneous communication and sensor interfaces.

Tiempo was founded in July 2007 by Serge Maginot, former R&D director at Synopsys, Inc., and Marc Renaudin, former Professor at the National Polytechnical Institute of Grenoble (INPG) and former head of the CIS research group of the TIMA Laboratory (research labs from INPG, CNRS and Joseph Fourier University). The startup is located in Montbonnot Saint-Martin, near Grenoble (France).

"Tiempo technology is the result of more than 15 years of scientific researches – the latest 8 years within the TIMA Laboratory – on the design of asynchronous integrated circuits and the development of dedicated EDA tools," stated Renaudin, CTO of Tiempo. "The outcome of these researches is chip prototypes that demonstrate outstanding performances for a very competitive silicon area, as well as a synthesis tool that makes our innovating asynchronous design technology now usable at industrial level."

To access Tiempo's website, click here.

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TIMA Exhibition at DATE: March 10-15, 2008

Participants to TIMA booth

A view of posters and demos on the booth
The CIS group TIMA Ph.D. Eslam Yahya's paper is awarded the Silver Prize in PRIME 2008
A balloon was launched at 30 000 meters with an experiment resulting from the cooperation of European and Latin American scientists.

"A balloon was launched up to 30 000 meters in Uruguay, in the frame of the ALFA (Amerique Latine Formation Académique) NICRON project. The payload included an experiment devoted to put in evidence the sensitivity to the transient effects of radiation (SEE) of advanced SRAMs operating in the Earth’s atmosphere. The launch was successful, obtained experimental data being presently analyzed."
Des vibrations capables de produire de l’énergie

Les vibrations capables de produire de l’énergie sont envisagées pour transformer en électricité les vibrations des machines industrielles.

L’état de la technique à Rotterdam, Londres et Boston (New York), des besoins en eau ont lieu d’inculquer de l’eau dans le sous-sol des bâtiments. Étude de la pertinence des bassins de dépollution des eaux, des besoins en eau et de la qualité des eaux. Étude de la pertinence des bassins de dépollution des eaux, des besoins en eau et de la qualité des eaux. Étude de la pertinence des bassins de dépollution des eaux, des besoins en eau et de la qualité des eaux.
TIMA members participated in the Grenoble yearly "Fête de la Science" event in November 2008. This event aims at explaining the scientific activities to the general public.

Showing the use of design tools

Explanations in the clean room
Rubrique : A explorer - Des circuits intégrés dans la stratosphère

Pouvez-vous nous décrire le contexte dans lequel sont menés ces travaux ? Raoul Velazco : L’incessante réduction de la taille des circuits intégrés augmente leur sensibilité aux neutrons présents dans l’atmosphère terrestre. Lorsqu’une de ces particules traverse un circuit intégré, l’énergie transmise est suffisante pour provoquer une réaction et engendrer un “bug”. Dans certains cas, les conséquences peuvent être critiques. Souvenez-vous de la Vel Satis de Renault, qui avait rencontré des problèmes de régulateur de vitesse. Il a été prouvé depuis que ces dysfonctionnements peuvent avoir été provoqués par l’impact d’un neutron ayant provoqué une faute transitoire dans l’un des circuits du contrôleur du régulateur de vitesse. On a également rapporté des cas de déclenchements indépendants d’avions récemment liés à l’environnement radiatif naturel.

La caractérisation sous rayonnements constitue donc une étape déterminante pour la compétitivité et la fiabilité des circuits intégrés avancés.

Comment procédez-vous pour étudier le comportement des circuits face à ces phénomènes ?

R. V. : Si l’on veut obtenir des résultats dans les conditions normales de fonctionnement d’un circuit donné, cela peut prendre beaucoup de temps car les flux de particules sont faibles. Afin d’optimiser les “chances” d’observer des erreurs, les circuits étudiés doivent être exposés à des flux de particules beaucoup plus importants que ceux rencontrés dans les conditions normales de fonctionnement.

Comment ? On sait que le flux de radiations augmente avec l’altitude. Ainsi, on estime qu’au sol (référence la ville de New York) il parvient environ 14 neutrons...
Régis Leveugle nommé Chevalier dans l'Ordre des Palmes Académiques....
Distinction remise lors d’une cérémonie par Paul Jacquet, Administrateur Général de Grenoble INP le 3 mars 2009
15. Social life and cultural life

The Laboratory had the pleasure to congratulate some of its members for births.

Born children of Laboratory's members:

- Wendelin MORIN-ALLORY, 21 January 2009
- Valentin FOURNERET -ITIE, 14 April 2008
- Ali MIAN-QAISAR, 03 March 2008
- Mélissa MARTINEAU, 23 January 2008

Besides fundamental research activities, TIMA Laboratory encourages the creativity of its members and promotes cultural activities such as temporary fine arts exhibitions or dissemination of scientific knowledge to the general public.

David Rios exhibits his photographs in TIMA. Private view on October 28th, on the occasion of the event: "welcome to new members" ([Pictures 1](#)).

On July 8, 2008, TIMA organised a picnic ([Pictures 2](#)).

A lunch and exchange of presents for Christmas 2008 ([Pictures 3](#)).
Picture 1:
David Rios' Exhibition
Getting together

Smile despite an empty plate!
They got seats

Desert time on the floor

Pictures 2:
TIMA picnic on July 2\textsuperscript{nd}
Pictures 3:
For Christmas 2008 gifts were books