Abstract

The Laboratory has a long experience on hardware design (computer architecture, microprocessor-based architectures, VLSI) and on CAD software (multi-level and mixed-mode simulation, physical design, architectural synthesis, system-level design). Today, the Laboratory is focusing on various aspects of the design, CAD and test of circuits and systems. The Laboratory is approximately 130 people large. It is organized in research groups: Micro and Nano Systems (MNS), Reliable Mixed-signal Systems (RMS), System Level Synthesis (SLS), Verification and modeling of Digital Systems (VDS), QualiFication of circuits (QLF), Concurrent Integrated Systems (CIS). The Laboratory is very international: many staff members enjoy 2 countries of citizenship, and there are many foreign researchers and visitors (usually more than 20 countries of citizenship). The Laboratory is also hosting the CMP Service, serving for chips and microsystems fabrication, down to 90 nm.

Two multidisciplinary projects are ongoing. One is concerned with the development of the WUCS, Wireless Universal Control System, in view of Ambient Intelligence, and the most recent one is dealing with Quantum Architectures, in cooperation with LEIBNIZ, a theoretical computer science Grenoble-based Lab for Quantum Computing and with Physics and Chemistry Labs working on the implementation of quantum dots.

Keys issues in 2004 have been to preserve the EUROSOCC project in view of a strong development in 2005, the development of a new paradigm on CAD for Bio-Nanodevices, the consolidation of TAST, the TIMA Asynchronous Synthesis Tools and the development of a full identification system for an integrated tactile fingerprint sensor.

In 2004, the Laboratory chaired or co-chaired IOLT in Funchal, THERMINIC in Sophia-Antipolis, DTIP in Montreux, IMSTW in Portland, DFT in Cannes, EWHRE in Grenoble, EMN in Paris. In addition, one summer school has been organized on Multiprocessor SoCs.

The Report is organized into 8 main sections including the Research and Service activities, the Resources and the Technology Transfer activities.
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1 - Overview

1-1 Organization

Since the late 60s, the members of the Laboratory have dealt with projects and tools on hardware and software:

### Hardware

- Computers:
  - the geo-physical machine
  - the PASCAL machine PASCHLL (1972/1981)

- Microprocessor-based architectures:
  - electronic exchange system CANOPUS
  - the CORAIL machine
  - the CRESUS project

- Microprocessor type circuits:
  - microsequencer MSQ
  - microprocessor 8 bits NMOS P68
  - microcomputer 4 bits SOS MOM 400
  - the MOSAIC project for the architecture of VLSI systems
  - series line control by LISA
  - microcontroller
  - microprocessor 8 bits POPY
  - microprocessor 8048 CMOS
  - microcontroller COBRA
  - mathematical coprocessor FELIN
  - compiled microprocessor 6502
  - MAPS controller
  - 1553 controller

- AI oriented machines:
  - OPALE machine
  - LAIOS lattice
  - SPAN mechanisms
  - SYMBION architecture

- VLSI
- Macro-systems and Microsystems

### Software

- Electrical simulation:
  - IMAG 2
  - IMAG 3
  - IMAG 4

- Digital simulation:
  - CASSANDRE
  - LASCAR

- System simulation:
  - LASSO

- Multilevel, mixed-mode simulation:
  - CASCADE

- Physical design:
  - LUCIE

- Architectural synthesis:
  - AMICAL

- Verification:
  - PREVAIL

- Co-design:
  - COSMOS

This experience serves as background to research in the field of the Design and Test of circuits and systems.

In 2004, the Laboratory was organized in 6 research groups, as listed below:

- MiCro and Nano Systems (MNS), S. Basrour & B. Courtois
- Concurrent Integrated Systems (CIS), M. Renaudin
- Reliable Mixed-signal Systems (RMS), S. Mir
- System Level Synthesis (SLS), A.A. Jerraya
- Verification and modeling of Digital Systems (VDS), D. Borrione
- QuaLiFication (QLF), R. Velazco
1-2 Research themes

Each topic of the research groups is briefly described below:

Micro and Nano Systems (S. Basrour & B. Courtois)
This research group addresses the following topics:
- micro systems: technologies, design and test, applications
- nano systems: architectures based on quantum effects
- CAD for nanosensors
- nanosprint: an infrastructure for nanotechnology foresight

Concurrent Integrated Systems (M. Renaudin)
This research group addresses the following topics:
- asynchronous circuits and systems (design and CAD tools)
- microprocessors smart devices
- low power, low noise circuit design
- secure chip design
- asynchronous mixed-signal and RF circuits

Reliable Mixed-signal Systems (S. Mir)
This research group addresses the following topics:
- test of analogue, mixed-signal, and RF circuits
- CAD tools for testing
- design and test of microsystems
- deep submicron analogue and mixed-signal design

System Level Synthesis (A.A. Jerraya)
This research group addresses the following topics:
- application-specific multi-processor system on chip
- software and RTOS synthesis
- on-chip communication network
- validation and prototyping of heterogeneous systems
- flexible & reconfigurable architectures

Verification and modeling of Digital Systems (D. Borrione)
This research group addresses the following topics:
- specification languages
- symbolic simulation
- formal verification
- theorem proving

QuaLiFication of circuits (R. Velazco)
This research group addresses the following topics:
- methods and tools for radiation testing
- fault injection
- hardware and software fault tolerance technics
- design and realisation of on-board satellite experiments
- hardware and software techniques for fault tolerance

In addition, 2 multidisciplinary projects are ongoing:
- Wireless Universal Control Systems for Ambient Intelligence
- Architectures based on quantum effects
1-3 Some past realizations of the Laboratory

The following pictures illustrate some past and recent realizations of the Laboratory.

(a) Cooperation with THOMSON led to the design of a self-checking, self-testing circuit (CMOS, 1.2 μ, 2 metallization layers, 650,000 transistors). The circuit is testable at the "transistors, metallizations, etc ..." level (1985).

(b) The SYCO silicon compiler took as input a behavioural ("Pascal like") description of the algorithms to be implemented in the silicon.
   b-1 is a 6502 CMOS control section compiled by the CPC specialized control section compiler.
   b-2 is a 6502 NMOS data path compiled by the APOLLON specialized datapath compiler (ca 1988).
(c) Electron-beam testing has been experimented through two equipments: a CAMECA ST-15 electron-beam tester and a JEOL 35C scanning electron microscope equipped for voltage contrast. Those equipments have been served by a SUN and an IBM workstation, respectively (1987 - 1993).

(d) The FELIN circuit was a design resulting from a cooperation with the Parallel Algorithmic Laboratory. It is aimed at the calculation of elementary functions like sine, cosine, etc. The circuit involved approximately 100,000 transistors, fully generated by a program describing the circuit (1987).

(e) CMP National Service gives the possibility to Research Centers, Universities and Commercial Firms to have their circuits manufactured. The Université Catholique de Louvain, CNET-CNS, THOMSON, MHS, ES2, TCS, AMS have manufactured bipolar, GaAs, NMOS and CMOS circuits for the CMP since 1981. One 4 inches wafer holds 73 CMOS different projects (15 wafers) and one 5 inches wafer holds 40 CMOS projects (5 wafers). Both have been processed by MHS, in 1986 and 1987, respectively.

(f) The computing room regrouped computers that were not distributed in offices. Here are several SM 90, a SPS 9, and a MicroVAX. The air conditioned room had been fully remodeled in 1987 (electric power, floor, etc...). Today, all computers are distributed in offices.
In the past, computers have been designed. g-1 shows the GEOPROCESSEUR (1970) which resulted from a cooperation with IFP, g-2 depicts the PASCHLL (1976) language-oriented computer, and g-3 shows the CANOPUS (1980) system which resulted from a cooperation with CNET-LAA. Presently the computer architecture projects are dealing with parallelism and with a logic-numeric integration.
(h) ADELAIDE was a project aimed at testing PCB populated by SMT devices. A prototype demonstrated the feasibility of an ATE, which uses extensively anisotropic elastomer conductors. Such a tool would allow a resolution of 10/1000 inches. The project has now been passed to industry.

(i) Circuit synthesized by AMICAL (1993). This circuit is a PID synthesized by AMICAL (300 behavioral VHDL lines as input, 4000 RTL VHDL lines as output) feeding a commercial logic synthesis tool generating 50,000 transistors (20 mm², .8µ CMOS). Design time: 1 week. This design results from a hierarchical use of AMICAL. One of its components is a fixed point arithmetic unit that has been designed using AMICAL.

(k) Microelectronics for Physics. BiCMOS wafer from CMP.

(l) Micromachining by CMP. Process at industrial manufacturers, post-process at Central Laboratories.
1-4 Some data on Grenoble’s environment

Grenoble offers a very good environment in terms of Education, Research, High Tech Activities, Industry.

Higher Education

Grenoble was awarded the title of "European University and Scientific Pole" in 1990, allowing the universities to stand on the international scene along with Oxford, Bologna or Tubingen.

- 60,000 students
- 6,000 foreign students
- 12.7% higher education
- 40.2% high school graduates

Research

Grenoble is the first French research center in Engineering Sciences, the second in Physics, the third in Mathematics.

1st in France and 5th in Europe for participation by its laboratories in the EU Research and Development Framework Programme.

- 17,000 researchers (the largest concentration of CNRS researchers in Engineering Sciences after Paris)
- 1,500 foreign researchers
- 250 laboratories
- 11,000 jobs in public research
- 4,000 jobs in private research
- 3,500 doctorate students and interns in local laboratories
- 30% foreigners in doctorate schools

5 European research centers:

- ESRF, European Synchrotron Radiation Facility
- ILL, Laüe Langevin Institute
- IRAM, Millimetric Radio Astronomy Institute
- SNCI, National Service for Intense Magnetic Fields
- EMBL, European Molecular Biology Laboratory

5 National research centers:

- CNRS, National Center for Scientific Research
- Grenoble CEA, Atomic Energy Commission
- CNET, National Center in Telecommunications Research
- CRSSA, Research Centre for the Army Health Services
- INRIA, National Institute for Research in Computer Science and Control

1 research center of international proportions acquired every 10 years since 1946
High tech Activities

- Microelectronics: 27% of jobs in France are located in Grenoble
- Electronics: 470 industrial companies, 13,250 jobs
- Biomedical technologies: 104 industrial companies, 2,600 jobs
- Imaging technologies: 50 industrial companies, 800 jobs

1 Technopole as part of Grenoble’s regional economic development, the “Zone for Innovation and Scientific and Technological Creation” (ZIRST) has become one of the foremost French technology parks, covering about 280 acres with over 275 companies employing 8500 people, mainly in the sectors of new technologies

Industry

3,500 companies created and 1000 buyouts per year in Isère
145 foreign-owned capital companies, employing 28,000 people
1 Business District to welcome company headquarter and professional services (EUROPOLE)

Electronics

Education:
- Engineering schools of INPG and UJF
  ENSEEG
  ENSERG
  ENSGI
  ENSIEG
  ENSIMAG
  ENSPG
  POLYTECH

Research
- Laboratories of CNRS, INPG, UJF
  IMEP
  LCIS
  LEPES
  LMGP
  TIMA

Infrastructures for research and education
- CIME
- CMP

Applied research
- LETI, a division of the French Atomic Energy Commission (CEA)
- France Telecom R&D, Grenoble Center

Industry
- STMicroelectronics, ATMEL, Thomson Electronic Tubes, Thomson Consumer Electronics, Thomson LCD, Schneider Electric, Mentor Graphics, AURIS, Dolphin Integration, SOFRADIR, RADIALL, MEMSCAP, TNI-Valyosis, iROC, SOITEC
A few key dates in local history

43 B.C.
Vienne, capital of the roman dominated region
Foundation of the town of Cularo (Grenoble).

1084
Foundation of the Monastery of the Grande Chartreuse.

1339
Creation of a University in Grenoble, including four sections: medicine, liberal arts (sciences and literature), canon law and civic law.

1709
Birth of Jacques DE VAUCANSON, biomechanist. His automata (Le Joueur de Flûte, 1738) were aimed at "reproducing means in view to obtain the experimental intelligence of a biological mechanism".

1712
Birth of Joseph FOURIER, mathematician and prefect of Isère department. In 1811 Joseph FOURIER sets up the Faculty of Sciences. In 1987, the Scientific, Technologic and Medical University of Grenoble will take the name "Université Joseph FOURIER".

1783
Birth of Henri BEYLE, so-called STENDHAL, novelist

1869
Invention of the hydro-electric power, the "White Coal", by Aristide BERGES.

1946
National Council for Scientific Research (CNRS).

1955
Grenoble Atomic Energy Commision (CEA Grenoble).

1963
First laboratory integrated circuit at LETI

1965
First industrial integrated circuit at SESCOSEM. First computer LAG/INPG-MORS.

1966
Laüe Langevin Institute (ILL).

1968
Winter Olympics in Grenoble.

1970
Louis NEEL is Nobel Prize in Physics. Louis NEEL has been President of Institut National Polytechnique de Grenoble (formerly Institut Polytechnique de Grenoble), from 1954 to 1976; he is now Honorary President of INPG.

1976
National Centre for Telecommunications Research (CNET).

1985
Nobel Prize awarded to Klaus von Klitzing.

1986
European Synchrotron Radiation Facility (ESRF).

1988
Research Centre for the Army Health Services (CRSSA).

1994
The European Synchrotron Radiation Facility is available to research scientists from virtually all countries.
2 - Research Activities

2-1 Micro and Nano Systems (MNS)

Group Leader: S. Basrour (e-mail: Skandar.Basrour@imag.fr)
Permanent Members: B. Charlot, K. Matou
Ph.D students: N. Galy, M. Marzencki, Y. Ammar, A. Zenati, F. Ciontu, C. Roman
Partners: M. Rencz1, K. Torki2, Ph. Jorrand3, V. Soumann4, J.C. Jeannot4

Research areas
- Micro power generators for autonomous microsystems
- Design and technologies of Integrated Microsystems
- Thermal characterization of MEMS and ICS
- MEMS Fingerprint sensors
- Architectures based on quantum effects

Contracts
- European: VIBES (IST)
- National ACI CNRS Energie
- Memberships: GDR CNRS 2503 micro et nanothermique

Industrial Partners
- PHILIPS
- METRAVIB 01db
- MEMSCAP
- STMicroelectronics
- MICRED
- BERTIN technologies
- Start-up company created: MEMSCAP (France).

Academic Partners
- T.U. Budapest, Hungary
- LEIBNIZ Lab., France
- FEMTO-ST, France
- LEG, France
- ESPCI, France
- Univ of Southampton, UK
- Tyndall, Ireland
- LÉOM, France
- SPIINTEC, France

Topics:

In recent years, a very large amount of scientific work has been achieved around microelectromechanical systems (MEMS). Some industrial success stories (accelerometers, gyroscopes and MOEMS) have shown their maturity. MEMS are now starting to take place around us in our everyday life as the microelectronic did 20 years ago. However, a lot of effort is still needed for the integration of ICs and MEMS. Quite every kind of sensor or actuator has been successfully developed with MEMS technologies whereas a very little work has been done on integration of MEMS devices with complex integrated circuits. An important part of the MNS group research activity is centred on integrated MEMS with the vision of “SoC including MEMS” as target. We believe that the future of MEMS is beside millions of transistors in large mixed signal Systems On Chip. These integrated MEMS devices will act not only as sensors but also as actuators or electric devices like switches and filters.

Recently, the MNS group started a new field of investigation concerning the nanosystems and in particular the CAD tools for the design of new nanosensors based mainly on Carbon Nanotubes (CNT).

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1 Technical University of Budapest, Hungary
2 CMP: Circuit Multi Projet Group, TIMA.
3 LEIBNIZ Laboratory, Grenoble, France
4 FEMTO-ST, Besançon, France
2-1.1 MEMS technologies

Members: S. Basrour, B. Charlot

Cooperation: V. Soumann, J.C. Jeannot (FEMTO-ST) and J.M. Terrot (CIME5)

2-1.1.1 DROGS process

The DROGS process (Double side Reactive ion etching On silicon and bonding of Glass on Silicon) has been developed to be a simple, reliable and low cost MEMS process to be used both for research and education purposes. It is devoted to the fabrication of high aspect ratio silicon microstructures.

This process uses a combination of side deep reactive ion etching on both side of a silicon wafer and an anodic bonding process on a glass substrate.

Suspended structures are then even attached to the glass+silicon substrate or attached to silicon pillars bonded on silicon (shown in Figure 2-1.1). The silicon pillars are electrically isolated of the substrate. Electrical connections are being made by wedge bonding on top of these pillars.

![Cross section of the DROGS MEMS process](image)

**Figure 2-1.1** Cross section of the DROGS MEMS process

**Figure 2-1.2** shows SEM pictures of structures implemented with the DROGS process, a double axis capacitive accelerometer and a close-up view of a comb electrode structure.

![SEM view of 2 axis capacitive accelerometers](image)

(a)

(b)

**Figure 2-1.2** SEM view of 2 axis capacitive accelerometers (a) and detail of comb fingers made with the DROGS process

5 Centre Interuniversitaire de Micro Electronique
2-1.2 Micro power sources for autonomous microsystems

Members: S. Basrour, Y. Ammar, B. Charlot, M. Marzencki

2-1.2.1 Introduction: wireless microsystems

Over the recent years a growing interest in the field of miniature sensor nodes could be seen. They are planned to be used in a wide range of applications, from medical implants to embedded sensors in buildings. In spite of a big research in this domain, there was one area that received little attention – energy source for the devices. Until now in the majority of such systems an electrochemical battery was used. This approach has a primary drawback – the device lifetime is directly linked with the battery size. With millimetre size devices, it is hard to extend lifetime beyond one year. There is a solution for this problem – profiting from very low power consumption of current electronics, such a device can be powered by harvesting external energy. Recent projects like SMARTDUST, WINS or SAND use photovoltaic and thermoelectric principles for harvesting energy of the environment.

Mechanical vibration energy is a promising solution when other sources like heat and light are not available. The main advantage of this solution is the abundance of mechanical vibrations in the environment and their relatively high power. Another important point is that the device needs only to be coupled mechanically through its package with the vibrating environment, the microsystem itself is then isolated.

This research field is addressed within two main parts that concerns the development of MEMS micro power generators and the development of innovative electronic circuits for managing the power produced by these devices. This research topic is funded in the frame of a European research project called VIBES

2-1.2.2 The VIBES project

VIBES stands for Vibration Energy Scavenging and is a Specific Targeted Research Project (STREP) of the 6th Framework Program of the European Union (EU). The project is leaded by PHILIPS research, the rest of consortium is composed of public research laboratories (TIMA, Tyndall, University of Southampton FEMTO-ST) and Small companies (MEMSCAP and 01db METRAVIB).

The goal of this project is to develop and demonstrate a micro power generator able to scavenge vibrations and motions from the surrounding (like building, machines, human body). This device will produce electrical power (in the range of µW) in order to feed an autonomous microsystem. The microsystem will embed an Ultra Low Power controller, a low power RF communication module, several MEMS sensors and a micro battery for energy storage. The project will focus on piezoelectric and electromagnetic transduction principles implemented with MEMS microfabrication techniques. Figure 2-1.3 shows a schematic of the architecture of the autonomous microsystem in development within the VIBES project.

Figure 2-1.3 Architecture of an autonomous microsystem including a vibration micro power generator

2-1.2.3 Micro power generators

From the two initial transduction principle, piezoelectricity and electromagnetic induction, we decide to investigate more in detail a piezoelectric transducer. The reason is that piezoelectric materials are deposited by sputtering techniques and then are compatible with CMOS microfabrication techniques.

Piezoelectricity

Piezoelectricity is the property of some materials to generate electrical charges on their surfaces when they are subject to a mechanical stress, as shown in Figure 2-1.4. These materials are widely used either for actuation (where mechanical stress is induced by applied voltage – indirect effect) or for sensing (electrical charge appears when mechanical stress is applied – direct effect). The best piezoelectric materials available are able to transfer mechanical energy to electrical energy with 80% efficiency.
Piezoelectric micro power generator

We design and fabricate a first prototype of piezoelectric micro power generator. The device, as shown in Figure 2-1.5 is composed of a seismic mass made of a Silicon cube connected to the substrate by a cantilever. When excited at its resonant frequency, the system will move according to its fundamental mode which is out of plane. During the movement, the cantilever is stressed in compression and elongation on the upper and bottom surfaces. The piezoelectric layer, placed on top of the cantilever will be stressed and by consequence some electrical charges will appear on the surface. These charges will be collected by the metallic electrodes and sent to the electrical load or to the Energy Harvesting Circuit described in the next section.

The device has been fabricated with MEMS microfabrication techniques in cooperation with MEMSCAP and FEMTO-ST. Basically, the process is composed of Deep Reactive Ion Etching (DRIE) steps on both sides of a Silicon On Insulator (SOI) wafer. The piezoelectric layer is made of Aluminium Nitride (AlN) and will be replaced by a thicker layer of PZT in a near future. Figure 2-1.5(b) shows an SEM photo of the first prototype.

Performances

Work performed within this project has proven that a power of 0.5\(\mu\)W can be obtained from a single device with an excitation of 10m.s\(^{-2}\) (~1g). Moreover, a large number of these devices can be fabricated together in the same substrate. This result confirms that a very low power microsystem can be powered with mechanical vibrations. However, long term scavenging and an energy storage device are still needed to power a RF transceiver that consumes typically 1mW for short range communication.

2-1.2.4 Energy Harvesting Circuit

The goal of the power management module is to transfer the energy produced by the micro power generator to the energy storage module, i.e., the micro battery. In order to charge the battery, a stable DC voltage is needed with a specific voltage that depends on the battery characteristics. On the other hand, the signal coming from the µPG is generally alternative (AC) and the voltage can be very low (~<100mV). By consequence, some operations such voltage rectification and elevation are required. In addition, these operations must be made with the best efficiency and the circuit must have very low power consumption.
Figure 2-1.6 shows the architecture of the power management module. The Energy Harvesting Circuit (EHC) is composed of an AC/DC circuit for the rectification, and of a DC/DC circuit for the elevation of the voltage. The DC/DC circuit is managed by a digital controller which maximises the energy transfer from the power generator to the micro battery.

**AC/DC converter**

In our case, the micro power generator produces low voltage which implies to use non-conventional rectifier circuit. A solution based on the use of comparators and transmission gates has been investigated; this active structure has estimated power consumption lower than 0.1µW.

**DC/DC converter**

Different types of DC/DC converters based on switching mode were studied. Figure 2-1.7 shows an example of a boost converter architecture. The circuit is controlled by a PWM signal applied to the switch. Depending on the duty cycle of this signal, the current which flows in the battery (mean value of I L(t)) will change. There is an optimal value of this duty cycle for which the current flowing to load is maximum, as shown by simulation in Figure 2-1.8(a). This optimal value is related to the excitation applied to the generator, which can be expressed by the value of the equivalent current coming from the generator, as shown by simulation in Figure 2-1.8(b).
We develop an algorithm that computes the best duty cycle and that drives the DC/DC circuit. We report in Figure 2-1.9 the experimental results of our algorithm and an algorithm found in the literature. We notice that our algorithm can achieve the optimal value of current faster than the other. This is very important since the generation of energy is a transient phenomenon and by consequence the value of current must be set as fast as possible.

![Figure 2-1.9 Battery current (I_{bat}) variations versus time, comparison between a reference algorithm (Ottman et al\textsuperscript{6}) and the algorithm developed at TIMA](image)

**Micro Battery**

The characteristics of micro batteries have an influence on the design of the previous blocks i.e AC/DC and DC/DC converter. For that reason, a model of micro battery has been developed. The model includes the effect of temperature and discharge current on the capacity of the battery.

### 2-1.3 Global simulation and Co-simulation of heterogeneous systems

**Members:** A. Zenati, K. Matou, S. Basrour

**Cooperation:** A. Jerraya, L. Kriaa (TIMA-SLS)

Since a few years, we can see the development of System on Chips (SoCs) that includes several technologies in the same substrate. For example, recent SoCs includes digital, analog and RF electronic circuits but also memory blocks (SRAM, MRAM, flash,..), and specially MEMS parts. This fact leads to a certain amount of heterogeneity that has an effect on the design and validation aspects.

Until now, every technology has its dedicated design and validation tools based on different levels of description (from system to device) and process of simulation (for example event or time driven). A very active research effort has been spent on the development of Co-design tools that can manage the design of both hardware and software parts of a digital system. With the addition of analog, RF, opto and MEMS parts, there is still a lot of work to build a design environment that can manage the validation of every part of an heterogeneous system within the same framework.

The goal of this work is to develop both design methods and tools for the validation of heterogeneous systems. In this specific project, we focus on the design of an autonomous microsystem developed in the frame of the VIBES project (see section 2-1.2).

This work is divided in two main tasks which are:

- Block Modelling with a hierarchical approach
- Global simulation and Co-simulation

**Modelling**

The modelling approach used is based on a top down design methodology. Models are described using analytical expressions or by equivalent electrical circuit. Our case study is the whole system reported in Figure 2-1.6. It includes:

---

- The piezoelectric micro power generator
- The Energy Harvesting Circuit (§ 2-1.2.4)
- and a microbattery.

Simulink is an environment of Matlab which supports the heterogeneous modelling (multi domains, mixed signals, multi languages) of our microsystem. Within this environment, the piezoelectric micro power generator, Energy harvesting circuit and the micro battery have been modelled at circuit level using an electrical component library available in the SimPOWER toolbox. At first, the controller is described with analytical equations and then a VHDL implementation was done in order to be simulated with SMASH \(^7\) and MODELSIM \(^8\) simulators.

**Global Simulation and co-simulation**

The global simulation has been performed with Simulink only. On the other hand, the Co-simulation has been realized using both Simulink and SMASH or Modelsim simulators.

**Figure 2-1.10** presents the comparison of the \(I_{bat}(t)\) curves (current reaching the microbattery) obtained with different simulation methods and the experimental results (already shown in **Figure 2-1.9**).

The simulation results are very close whatever the simulation methods. These results show the same qualitative behaviour compared with the experimental data. Quantitative discrepancy comes from a mismatch on several physical parameters like MOSFET transconductance or battery capacity.

**Model Refinement**

At the moment, simulations have been carried out with electrical equivalent models for both the \(\mu\)PG and the battery. These simple models will be replaced in a near future by more complex descriptions.

Concerning the \(\mu\)PG, the electrical equivalent model will be replaced by a behavioural model based on an analytical description taking into account several shape factors and material parameters. In addition, a model order reduction technique will be employed to produce a compact model from a complex finite element analysis.

---

\(^7\) Dolphin integration

\(^8\) MENTOR Graphics
2-1.4 Biometrics
Members: B. Charlot, N. Galy

2-1.4.1 MEMS tactile fingerprint sensor
An integrated fingerprint sensor has been developed to be used as an access controller in several kinds of electronic portable devices like cellular phones or laptop computer.

The device is composed of a 1.28 cm long row embedding 256 sensitive elements. The sensitive elements are tactile micro cantilevers (100µm long and 30µm width) distributed at a pitch of 50µm along the row. When the user sweeps its finger on the device the cantilevers are bent down. A piezoresistive gauge placed at the clamped end of each cantilever allows the measurement of the bending and by consequent the measurement of the finger’s roughness.

The device embeds a read out electronic circuit that manages the scan of the cantilevers row at a frequency of 100 kHz. At each clock pulse, the signal coming from a cantilever is switched to an electronic circuit that amplifies and digitizes the signal. The fingerprint sensor is then fully digital.

A test board including a programmable integrated circuit drives the fingerprint sensor and records the data. In a near future the programmable circuit will include all the software needed for the fingerprint recognition in development at the laboratory.

![Figure 2-1.11 Schematic of the tactile fingerprint sensor (a), detail of the micro cantilevers (b), Photo of the chip on board (c) showing the bonding wires protection and SEM photo of the micro cantilevers (d) ](image)

2-1.4.2 Full identification system
To test the sweeping sensor described previously, we have implemented a full fingerprint verification system. The latter takes in input one finger and provides a binary result in output. The global structure of such a system is shown on Figure 2-1.12 and follows 4 stages.
Fingerprint acquisition: a fingerprint is acquired in a digital form by means of our tactile sweeping mode sensor. It provides a 256 grey levels rectangular image (Figure 2-1.13-a).

Pre-processing: it is a very important component of the system prior to extraction stage. The image is locally enhanced by means of directional filters in order to cancel noise and various distortions as much as possible (Figure 2-1.13-b).

Feature extraction: we use the classical approach based on minutiae extraction (Figure 2-1.13-e) from a thinned representation (Figure 2-1.13-d) of the binary ridge structure (Figure 2-1.13-c). At the end of that stage we have a signature file (Figure 2-1.13-f) featuring the fingerprint image.

Matching: the final goal of our system is to confirm the identity of the person whose fingerprint has been submitted to the system. Two signatures coming from the same fingerprint will always be different due to various acquisition conditions. Thus the matching stage consists in computing the similarity degree between two signatures, and deciding if they are similar enough according to a threshold.
2-1.5 Thermal evaluation of MEMS and ICs

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2-1.5.1 Electrothermal simulation

State of the art integrated circuits are now currently using millions of transistors within a few mm² of Silicon and dissipating a very high amount of power. Traditionally the temperature rise due to the power consumption was simply evaluated while taken into assumption that the temperature would be uniformly distributed all over the surface of the chip. This hypothesis is no more true with the rising performance of chips and at low timescales. The temperature gradients induced in a chip while consuming power can easily destroy the signal integrity of an IC and increase the failure rate.

The electrothermal analysis of an IC is then the computing of the temperature map of the chips induced by a specific electrical activity of it. Due to the large amount of information to be taken into account for a precise electrothermal analysis, (e.g. FEM analysis) this way is impossible for most devices.

The envisaged solution is to reduce the simulation complexity. The proposed solution for reducing simulation complexity is to switch one level in circuit description, This is done by describing the circuit at logic cell level (gates, flip flops, …) whereas at device level (transistor, connexions, …). The electrical behaviour of the circuit (toggles) will be extracted from digital simulations and the physical informations (size and positions of cells) will be extracted form layout. These informations will then be translated into a Therman simulator compliant format. The Therman simulator is a 2D thermal simulator developed by MicReD, Hungary.

The proposed method is based on the digital model as it is widely used for functional and timing sign off. The detail procedure for performing logic cell level electrothermal simulation is as follows:

1. Logic level simulation :

   Toggle count either on line during the simulation or off line by parsing the VCD file. The output is the number of toggle (switch from 0 to 1 or 1 to 0) for each cell instances and for a given test bench. This is done using the VERILOG simulator with specific PLI routines.

2. Power calculation :

   Computes power dissipated by each cell as a function of their toggle, fanout load, and wire resistance.

3. Annotation :

   With the physical representation, information on size and position of each cell are added to the dissipating informations. A Therman compliant file is produced.

4. Thermal simulation and graph :

   The Therman software runs a DC thermal simulation and plots the temperature map.

An electrothermal simulation has been made on a test circuit. The circuit has been chosen to be representative. It is a RII filter implemented using an austriamicrosystems 0.6 µm standard process. It contains 20000 gates on 15 mm² and runs at 40 MHz under 5V, The Figure 2-1.14 (a) shows the circuit’s layout, we can easily see the pad ring and the two RAM cells on the top of the chip.
Figure 2-1.14  Layout of the chip (a) and its electrothermal simulation (b)

The Figure 2-1.14(b) shows a Therman plot of the logic cell level simulation. The temperature map shown in the graph is the temperature of the chip after having run the test bench.

We can see different informations:

- The cells that have an important toggle during the test sequence will dissipate more than the others, the results are some warm points in the chip.
- The electrothermal simulation gives informations on the temperature map of the chip during a specific sequence. These results can be taken into account for the place and route steps in order to minimize temperature gradients and thus keep the integrity of the signal.

2-1.5.2 Imaging the thermal activity of digital ICs

The goal of this project is to produce a dynamic thermography of a digital chip while running a given test bench. The thermography will produce a map of the temperature at the surface of the chip at different moment of the computing process. These results will then be compared with simulation results described in the previous chapter in order to confirm the simulation method. The thermography method is thermoreflectance. It consists in measuring the variation of the optical reflection coefficient with temperature at the surface of the chip. The measurement setup is composed of a monochromatic illumination system and a CCD camera controlled by a computer. The thermoreflectance measurements have been made in the laboratoire d'optique physique in ESPCI, Paris.

For this experiment a digital chip has been fabricated with specific features:

- The circuit is representative of a large amount of ASIC chips manufactured nowadays to be use as a benchmark for thermography techniques.
- The circuit has a repetitive, determinist and controllable working cycle.
- The circuit is easily testable, and not require the use an IC tester.

The circuit is composed of two 8bits programmable linear feedback shift registers (LFSR). The LFSR will produce pseudo random sequences of 255 bytes. Several operations will then be applied to these bytes like addition/subtraction and multiplication/division. The result of these operations is then compared with inputs. This way of computing allows the creation of a repetitive heat transfer pattern in the digital core and a controllable temperature map at the surface. Figure 2-1.15 show the layout and photographs of the fabricated chip. Figure 2-1.16 shows the results of the static thermoreflectance measurement made at different clock frequency.

The future work in that topic will be the dynamic measurement of the temperature map along the computing cycle.
2-1.6 Nanosystems

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2-1.6.1 CAD for nanosensors

The last years have brought nanotech applications closer to reality mainly due to considerable progress in fabricating nanostructures with controlled properties. Carbon nanotubes followed this path with huge advances in synthesis techniques as well as in functionalization, solubility and selection. On the other hand bio-sensing is one domain offering clear opportunities to transpose theoretical and technological advances related to nanotubes into applications. In this project we exploit the remarkable coherence between theoretical models of carbon nanotubes and measurements to develop a CAD-centered design approach based on the exploration of possible devices through reasoning on their models. At this point, we have explored two possible devices that have passed the test of validation through modelling.

The first device, depicted in Figure 2-1.17(a), is a classical set-up for carbon nanotube sensors. At the first sight, the functioning principle is quite simple: given that a carbon nanotube has all atoms on the surface, external stimuli will be transposed in a modification of its conductance. Beyond this seducing simplicity, the real mechanism is still a matter of debate: is that carbon nanotube or the contact region that determines a change in the conductance.

In our project, we are focusing on the sensitivity of carbon nanotubes to the physisorption of four amino acids: Histidine (HIS), Phenylalanine (PHE), Tryptophan (TRP) and Tyrosine (TYR). Through a new method of parameterization of empirical models developed at TIMA, we were able to perform a first validation of this concept. Aminoacids physisorbed on a graphene sheet through pi-stacking, induce states close to the Fermi level as shown in Figure 2-1.17(b) for Histidine. These results also hold for carbon nanotubes.

After this first step, we intend to proceed with modelling a system including realistic contacts. A first approach would consist of including various corrections in order to be able to model semiconductor contacts within the framework of density functional theory. A realistic modelling of this device should allow distinguishing between aminoacids based on their I/V characteristics (I-V spectroscopy.)
Figure 2-1.17 Basic set-up of a carbon nanotube transconductance sensor (a) and States created in the vicinity of the Fermi level of graphene by the absorption of Histidine (b)

The second device, sketched in Figure 2-1.18, converts the deflection of a carbon nanotube, upon the application of an external force, into an electric current difference at the ends of a second nanotube, perpendicular to the former.

Three of the four nanotube ends are clamped metal leads and one is free to move, being the end to which an external force will be applied. Mechanically, one tube is a cantilever while the other one is a linear bearing. The bearing is placed underneath the cantilever, restraining its vertical movement and preventing it from bending and sticking to the substrate. The inter-tube friction does not impede the cantilever from bending laterally under an external force, although it will modify the amplitude of thermal fluctuations in the region of the junction.

The first part of the study of this device focused on an assessment of the sensitivity of the devices with forces in the tens of pico Newtons, developed typically at the cellular scale. A second part targeted the transduction of the deflection of the cantilever into an electrical signal, employing methods borrowed from non-equilibrium Green's function. Several issues related to the importance of thermal effects in the proper operation of the sensor have been investigated in detail. Non-zero temperature was included through molecular dynamics in quantum conductance calculations. One could note however several challenges posed by the coupling of phenomena belonging to different scales like the influence of the inter-tubes distance, typically modelled though molecular dynamics, and the variation of the currents computed through a quantum transport method.

2-1.6.2 Design for Nanoimprint

Pattern transfer fidelity problems were acknowledged from the initial stages of nanoimprint research. Their causes are diverse and originated at different stages of the nanoimprint process: molding, de-molding or post-molding. In this project we focus only on pattern transfer fidelity problems for which the causes can be controlled at the design level. Most often, these problems appear due to incomplete polymer flow on molds with complex patterns.
Our goal is to develop an approach for coping with nanoimprint reliability issues while working at the design level. The “classical” approach towards mitigating these caveats relies heavily on development of new resins and optimization of process parameters. Our approach is somewhat different as it relies on the following principle:

- A correlation model is established between parameters controllable at the design level and defects on the final imprinted mold.
- The initial design is modified (automatically) such that, while maintaining its functionality, the modifications will compensate the errors introduced through the hot embossing process.

Existing works on this topic have a common limitation – they are confined to periodic structures because otherwise FEM-based models rapidly reach their limits in terms of computational tractability. Since, as previously discussed, the type of errors we are interested in appears specifically in the case of heterogeneous pattern densities, this limitation drastically restricts the applicability of FEM studies.

At the moment, we focus on implementing a workflow which brings two original contributions to the state-of-the-art:

- First, the correlation model is inferred using equation discovery techniques rather than being the result of bottom-up modeling. By consequence, the correlation model is minimal which in turn maximizes the tractability of molds with complex, aperiodic patterns. This makes our technique suitable for real-life applications.
- To the best of our knowledge, this is should be the first work on automatic mold redesign for nanoimprint. Moreover, we intend to implement a redesign strategy for classical as well as quantum models. While using general physics networks as equivalence class is relatively common in various CAD systems, to our knowledge this should also be the first work using equivalence classes for quantum transport.
2-2 Concurrent Integrated Systems (CIS)

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2-2.1 Introduction: asynchronous circuits and systems

The global synchronization strategy of synchronous circuits was introduced in the early 70s because at that time, it was a satisfactory answer to design needs and technological potentials. This initial choice of an implementation strategy, drove and is still driving the design of algorithms/architectures, languages and CAD tools. Today, integration potentials of advanced technologies are going beyond design productivity, and one can wonder whether the synchronous circuit style is still relevant. Asynchronous circuits which were introduced in the mid 50s, receive now increasing interest. What significant benefits are they likely to offer? Can they contribute to improve design productivity in the future?

Our motivation is to answer these questions, investigating what impact asynchronous circuits may have on the design of integrated systems and how to take advantage of this circuit style at different levels: circuit level, architectural/algorithmic level, specification level, and system level? Because asynchronous circuits provide more flexible, robust and reliable synchronization and communication mechanisms, they give rise to alternative and innovative solutions that have to be analyzed and evaluated.

At the circuit level, asynchronous logic enables the design of delay insensitive circuits which do not require accurate and costly delay characterization. In fact delay insensitivity guarantees a correct functional behavior independently of the propagation delays in the basic components (gates, interconnects...). Delay insensitive asynchronous circuits are for example insensitive to some emerging problems like delay fault due to crosstalk. The delay insensitivity property makes asynchronous circuits very promising to explore and exploit advanced CMOS and future technologies.

Eliminating the global clock, which synchronizes all parts of circuit in synchronous logic, provides more flexibility to design system architectures. In fact, the control is naturally distributed rather than centralized. Hence, communications as well as synchronization through «rendezvous» for example, are easily implemented by a collection of independent and local finite state machines, which do not require knowing the state of the whole system. Data to be computed by the system flow in the architecture as fast as they can according to resources' availability and hardware implementation. The processing cost (in terms of delay and power consumption) is exactly the image of what is specified by the algorithm, given the chosen hardware implementation. It means that speed and power consumption may depend on the data processed. The data-flow behavior of asynchronous circuits, at any level of granularity, is the source of significant improvements in terms of speed/power optimizations and ease of design.

Today, one of the main challenges is the design of efficient and convenient CAD tools for asynchronous circuits. This is currently one of the priorities of our research work. We have adopted a CSP based language, called CHP, as the specification language (introduced by Alain Martin - Caltech). The specification and
development of a design framework for asynchronous/synchronous circuits is in progress. This work follows two main motivations: i) to provide the asynchronous circuit designers with a powerful execution/simulation framework, mixing high-level CHP descriptions, HDL programs and gate level descriptions, 2) to give to synchronous designers familiar with existing HDL-based top-down design flows, the opportunity to include clock-less circuits in their designs. The main challenge is to efficiently synthesize behavioral descriptions written in CHP into gates. One of our goals is to provide a synthesis tool that would target different styles of circuit, QDI and Micropipeline circuits, thus enabling designers to compare the merits of different approaches.

Finally, asynchronous circuits also bring flexibility at the system level. Complex, highly concurrent image processing applications naturally take advantage of the locality and modularity of clock-less circuits. Because they don't need a global synchronization signal, modularity is a major property of asynchronous circuits which enables the design of complex integrated systems by simply assembling functional blocks. Design time is thus reduced and reusability increased. As an example, the design of locally-synchronous globally-asynchronous SoCs bring a solution to the problem of communications between distant parts using long interconnects. Without requiring drastic change in terms of tools and methodologies, synchronous parts of SoCs may be interconnected using advanced and robust asynchronous interfaces.

The potentials of asynchronous circuits are being investigated through the design of portable systems (from smart-card to multimedia terminal). There are three main properties of asynchronous circuits that can improve such systems and/or make their design easier: electromagnetic compatibility, low power and free power management, flexible interfacing capabilities. Interfacing digital asynchronous circuits with analog parts (RF front-end, sensors, actuators, etc.) is also a major field of interest. It is in fact essential if we expect to successfully design SoCs that may integrate various kinds of digital and analog parts.

2-2.2 The TAST design environment

TAST stands for TIMA Asynchronous digital circuit Synthesis Tools. This is a design environment which is gathering researches carried out in the group on asynchronous circuits design methods and associated CAD tools.

It consists of a compiler/synthesizer with the capability of targeting several outputs from a high level description language. We have adopted a high level description language derived from CHP (Communicating Hardware Processes introduced by Caltech) with specific features to cope with communication protocols, data encoding, arbitrary precision arithmetic, non-determinism, hierarchy, project management, and traceability. All these features make our CHP a very practical system description language to develop with. It also makes scalability and modularity easy to manage.

The flow (Figure 2-2.1) is organized around an intermediate form based on Petri Nets (PNs) associated to Data Flow Graphs (DFGs). Such models have been used for years to model synchronous circuits and systems and find a particularly adequate application in the field of asynchronous digital circuits and systems design.

CHP models can be simulated using our non-deterministic simulator which fully supports the semantic of the TAST CHP language. The simulator includes powerful commands to trace code execution, compute statistics along simulation runs, perform code coverage, watch process variables, etc... Petri Nets animation is also provided to enable didactic analysis of CHP model behaviors.

CHP synthesis into asynchronous digital circuits is based upon the DTL (Data Transfer Logic) specification we have defined. It provides a set of rules to guarantee that PN-DFG graphs are synthesizable into asynchronous digital circuits. DTL CHP programs are compiled into M-ary Decision Diagrams (MDDs) which are reduced, factorized and synthesized into QDI circuits. It is theoretically proven that all these steps preserve the Quasi Delay Insensitivity of the circuits.

Technology mapping is finally applied to enable the designer to freely choose its preferred target. He/she can choose between conventional synchronous standard cell libraries, dedicated libraries including C-elements for example (like TAL), or even FPGAs.

Current research is carried out in the CIS group to improve TAST in the following areas:
- get better performance of synthesized circuits in terms of area, speed and power,
- security driven synthesis to get power attack resistant and fault tolerant circuits,
- EMI (Electro Magnetic Interference) driven synthesis,
- testability and ATPG,
- formal verification of models and circuits (collaboration with the VDS group).
2-2.3 The TAL Library

TAL-130 stands for TIMA Asynchronous Library, and it has been designed using the standard CMOS 130nm process from STMicroelectronics in collaboration with the LIRMM laboratory. The library contains around 170 standard cells that we unfortunately do not find into conventional synchronous standard cell libraries. About 30 different functionalities implementing various kinds of C-element and combination of C-elements have been included in the library. All the cells of TAL are layout compatible with the standard cell library provided by STM so that the designer can mix the use of conventional and TAL cells in his/her design.

The aim of TAL is to enable the design of asynchronous circuits that are smaller, faster and which consume less power than those obtained using conventional synchronous standard cell libraries. To evaluate the performance gains brought by the library, two cryptographic circuits (DES) have been designed and fabricated using TAL-130. The first results show an average improvement of about 35% of the circuit areas when compared to the previous versions of the same circuits exclusively designed with conventional standard cells. Speed and power gains will be measured as soon as the chips come back from foundry.

2-2.4 CMOS Imagers for automotive applications
(Collaboration with ATMEL)

Novel security applications in automotive require to study a new class of CMOS imagers. One of the goals of the PICS Medea+ European project is to explore the possibility to design such CMOS sensors while being compliant with industrial constraints. The critical conditions and properties this work has to tackle are:

- Light conditions: when in a car, the vision system has to work within hard light conditions; a wide input dynamic range is expected for the sensor, together with an efficient anti-blooming system.
- A good sensitivity in the IR domain is expected because IR Leds will be used for night conditions.
- Speed constraints: when the car is in motion the image should not be distorted by the displacement.
- The pixel area cannot exceed 100µm² which limits the maximum number of transistors and requires choosing between full-PMOS or full-NMOS transistor circuits.

Therefore, the imager has to provide a high input dynamic range (up to 100dB) and an instantaneously image acquisition (Global Shutter system) whereas currently available CMOS imagers provide an input dynamic range around 65dB and implement sequential image acquisition (Rolling Shutter system).

The ultimate goal of the project is to design a single chip which should include the sensor we are designing as well as the ATMEL signal processing chain. Such a goal makes impossible the use of CCD sensors and fully justifies this research.

The work carried out so far has been focused on the specification and design of a pixel architecture enabling around 120dB of dynamic range, including a global shutter system. Its area does not exceed 100µm², and is designed using the 0.18µm CMOS process from ATMEL.
2-2.5 Secure circuit design and smart-cards

2-2.5.a Integrated system for contact less smart-cards

(Collaboration with France Telecom R&D & STMicroelectronics)

We have designed MICABI a Contactless Smart-Card Chip which integrates an on-chip coil connected to a power reception system and an emitter/receiver module compatible with the ISO 14443 standard, together with the MICA 8-bit microcontroller described above (see Figure 2-2.2). Beyond the contactless smart-card application field, this new chip demonstrates that System on Chip integrating power reception and management, radio-frequency communication and signal processing are feasible. The chip, fabricated in a CMOS 6 metal layers 0.25 µm technology from STMicroelectronics, associates analog/digital parts as well as synchronous/asynchronous logic.

Power reception and data transmission are performed using a modulated magnetic field emitted by the reader. The antenna was integrated on silicon (on-chip coil), using 5 metal layers, to suppress interconnect issues and decrease card cost. Computation power in the card-chip is provided by the MICA quasi delay insensitive microcontroller in order to limit power consumption, noise, and sensitivity to supply voltage variations. The 8-bit microcontroller core integrates a 32 Kbytes RAM and a 2 Kbytes ROM containing a BIST (Built In Self Test) and a boot program.

The power-supply reception system is designed in order to allow operation of the micro-controller while in reception or in emission. A voltage regulation system decouples the micro-controller voltage supply and the RF front end voltage supply which transmits data. This regulation ensures correct operation of the RF front-end while the micro-controller is in operation at its own speed according to its data treatment and received current. In normal mode of operation its supply-voltage is regulated to 2 volts. At this voltage level the microcontroller delivers 18.6 Mips on average and consumes about 13.3 mW. At 1 volt, the core still delivers 4.3 Mips and consumes only 800 µW.

A dedicated interface between the asynchronous processor core and the ISO 14443 compliant analog emitter/receiver module was designed. This interface implements a handshake-based protocol which ensures minimum power consumption and noise when the chip is receiving or emitting data.

Figure 2-2.2 The contact less smartcard MICABI and its reader
2-2.5.b Secure circuits design

The goal of this research is to propose new design methods and tools to improve circuit resistance against non-invasive attacks such as timing attacks, PA (Power Analysis), EMA (ElectroMagnetic Analysis) and FA (Fault Analysis). Today, cryptography and cryptanalysis are both evolving very rapidly opposing hackers and secure systems providers. The smart card market is the primary concerned, but e-commerce, e-banking and data ciphering in general are all sensitive to attacks. Searching for new counter measures against such attacks, jointly at the software and the hardware levels, is becoming a major issue.

DPA attacks consist in measuring current consumption or electromagnetic emission of a running circuit in order to extract secret or private information. Glitch attacks are methods to disrupt circuit execution by applying sharp signal changes to the clock signals or to the power supply lines.

The asynchronous technology provides a means for designing DPA resistant circuits. In fact, it can be shown that quasi delay insensitive circuits can be designed so that the execution time and power consumption do not vary with the data processed. Thus, the electric and electromagnetic signatures of a running circuit are data independent making DPA type attacks inefficient.

In this field, the challenge is to get the best of asynchronous circuits to improve security at the smallest cost possible. Today, known solutions are rather costly in terms of area. Current works carried out in the CIS group are focused on low-complexity secure asynchronous circuits.

Glitch attacks in particular and DFA (Differential Fault Analysis) in general, are also important issues that we are currently investigating theoretically.

MICA processor.

On the practical side, we have recently performed DPA on the MICA microprocessor. Results obtained when performing power analysis on the MICA 8-bit QDI asynchronous micro-controller reveal that the processor resists to standard DPA attacks. These results practically demonstrate the relevancy of using the asynchronous technology to design new secure circuits for smartcards and cryptographic applications (Figure 2-2.3).

DES and AES crypto processors

DES and AES crypto processors were designed to evaluate the benefits brought by asynchronous logic to improve circuits’ resistance against power analysis attacks. DES prototypes (Figure 2.2.4) were jointly designed by TIMA, LETI and STMicroelectronics within the Esp@ss-is Medea+ European project. The goal of this work is to study the introduction in smart-card IC design of an innovative hardware technology, namely Asynchronous Logic, and to evaluate how it can improve security.

A test board is under development to enable us to perform Differential Power Analysis and measure the ability of this technology to resist against such attacks.
**Fault tolerant QDI asynchronous circuits**

Differential Fault Analysis (DFA) is a well-known method for cryptanalysis. With DFA it is possible to retrieve secret cryptographic keys by analysing the results of correct and erroneous cryptographic computations. A successful DFA attack depends on two conditions. First: the algorithm must be known and vulnerable. Second: it must be possible to induce faults on the hardware platform. The procedure of DFA depends on the cryptographic algorithm. Successful attacks were done on the Data Encryption Standard (DES). QDI asynchronous circuits are attractive to design fault resistant systems against a large class of faults. We show that the fault resistance of a circuit can be improved by exploiting QDI asynchronous logic properties. A secure fault tolerant DES prototype was designed to evaluate the hardening techniques we apply against fault injection. The secure circuit is only 7% larger and about 20% slower than the non secure initial circuit. Both the reference and the secure circuits are to be tested under a laser fault injection system within the Duracell RNRT project.

It is worthwhile to mention that the proposed techniques to harden the QDI circuits against faults do not alter the counter measures that can be applied for PA. Therefore, this technology enables us to jointly harden circuits against fault and power attacks.

**2-2.6 Modeling and design of asynchronous priority arbiters for on-chip communication systems**

The design of complex arbitration modules, like those required in SoC communication systems is addressed. Clock-less, delay-insensitive arbiters are studied in the perspective of making easier and more practical the design of future GALS or GALA SoCs. The work focuses on high-level modeling and delay-insensitive implementations of fixed and dynamic priority arbiter. Gate-level electrical simulations show that arbiters which are able to process several hundreds mega requests per second can be designed using the 0.18 μm CMOS process of STMicroelectronics.

One of the critical components of a SoC is the communication system, commonly named on-chip bus. Such an on-chip communication system has to be very flexible to interface in-house and external virtual components, providing high bandwidth, low latency, low power, arbitration mechanisms and routing capabilities.

In a SoC the on-chip bus connects the components to each other and dynamically allocates a path from one block to another. Several blocks running concurrently may require accessing the same resource leading to
contentions. In this case, an arbiter is needed to solve the conflicts and to ensure that only one block is accessing the resource. The choice is done with the help of priorities affected to each request.

Several arbitration algorithms were proposed in the past to solve the problem of accessing a unique resource from an arbitrary number of blocks. These algorithms can be classified according to the characteristics of their corresponding hardware implementation. To mention a few, arbitration structures can be distributed or centralized, can be linear like daisy-chain arbiters, or ring-based like token-ring and round-robin arbiters.

Most on-chip communication systems and the arbitration modules they include are today designed with synchronous circuits. In this paper, delay-insensitive asynchronous arbiters are considered, to be part of future on-chip busses of GALA (globally asynchronous locally asynchronous) or GALS (globally asynchronous locally synchronous) SoCs.

In the SoC design perspectives, delay-insensitive arbiters have this main advantage of being hundred-percent reliable (enough time is given to resolve metastability). Today, reliability of on-chip communication systems is a major issue since the increasing transaction rate is drastically reducing the so-called Mean Time Before Failure characterizing clocked synchronizers.

As far as power consumption is concerned, such event driven communication/arbitration structures have a minimal electrical activity. Indeed, unlike clocked circuits, power consumption of delay-insensitive asynchronous arbiters is proportional to access rates. Furthermore, delay insensitivity enables the design of fast “long distance” communication busses. Finally yet importantly, such delay-insensitive communication systems are fully autonomous blocks, which can easily be reused in complex SoC architectures as soft, firm or hardware virtual components, hence decreasing design time and complexity.

Based on these motivations, this work contributes to two fundamental issues: arbitration algorithms are modeled using a high-level description language called CHP (Communicating Hardware Processes), and the delay-insensitive arbiter architectures are derived from these CHP specifications.

Three fixed priority arbiters were designed, daisy-chain, binary-tree and parallel-request-sampler as well as a dynamic priority arbiter based on the parallel-request-sampler algorithm. This work demonstrates that it is today possible to cleanly and formally model and design delay-insensitive arbiter modules that are reliable, modular and fast. It also defines the fundamentals of an automated synthesis process devoted to arbiters. Finally, it constitutes an enabling factor for the asynchronous technology to be increasingly adopted in the design of SoCs.

Prospective works will be focused on the automation of the synthesis process within TAST, and the improvement of arbiter architecture and circuit performances. “n initiators to p receivers” fixed or dynamic priority routers will also be investigated to address the design of complex on-chip routing systems.

### 2-2.7 Lowering electromagnetic disturbances with asynchronous circuits

#### 2-2.7.1 Asynchronization method

Asynchronization method was elaborated in order to exploit low EMI benefits of asynchronous circuits. It consists in obtaining asynchronous circuits from Register Transfer Level description of synchronous ones. This method suggests replacing identified synchronous structures (clock control) by equivalent asynchronous ones (handshake communications) inside the circuit. Cycle compatibility is respected in order to validate the circuit functionality.

This method was validated on a 4 coefficient Finite Impulse Filter reducing significantly the level of the spectrum.

![Figure 2-2.6 Current spectrum of synchronous FIR filter and asynchronized FIR filter](image-url)
2-2.7.2 A Current shaping methodology for lowering EM disturbances in asynchronous circuits

This work proposes a design methodology aiming at reducing peak-currents in asynchronous digital circuits. The method exploits the flexibility brought by handshake based communication mechanisms implemented in asynchronous circuits. It starts from a structural description of the circuit, which is then refined according to the communication protocol used, and annotated with operator latencies and current consumption. Force Directed Scheduling is then applied on the refined and annotated structural model of the circuit to determine the set of delays that have to be inserted in the handshaking protocols in order to minimize the peak-current without increasing the latency of the critical path.

It is important to mention that the method is general and can be applied to any asynchronous circuits, based on different protocols and different logic styles. Evaluated on a micropipeline asynchronous FIR filter, the method enabled a 20% reduction of the maximum peak-current.

Future work will be focused on including the method in the TAST framework and applying it to different asynchronous circuit styles in order to define which asynchronous circuit style is the best suited to low EMI circuit design.

2-2.7.3 Quasi Delay Insensitive Asynchronous Circuits for low EMI

This approach proposes a new design alternative for controlling/reducing electromagnetic emissions of integrated circuits. Our design approach is based on the exploitation of Quasi Delay Insensitive Asynchronous logic properties. In fact, by using a four-phase protocol combined with 1 to N encoded data, we demonstrate how QDI circuits can be used for tuning and lowering electromagnetic emissions. The investigation is based on the characterisation of two DES crypto-processors: an asynchronous and a synchronous version. The spectra of the measured currents show a significant reduction of the EMI of the asynchronous DES when compared to the synchronous one.

Figure 2-2.7 Current Spectrum of DES circuits

2.2.8 Analog-to-Digital Converters Based on Non-Uniform Sampling

This work is a contribution to a drastic change in standard signal processing chains: Analog-to-Digital Converters (ADCs), digital processing circuits, Digital-to-Analog Converters (DACs)… Integrated Smart Devices and Communicating Objects are the important applications targeted by this study. The main objective is to reduce their power consumption by one or two orders of magnitude, by completely rethinking their architectures and the associated signal processing theory.

Most of integrated systems bring signals with interesting statistical properties into operation, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, electro-cardiograms, speech signals…) are almost always constant and may vary significantly only during brief moments. Thus, classical regular sampling systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. The new idea of this work consists in realising an adaptive sampling scheme of the analog input signal based on its amplitude variations, and implementing an architecture only driven by the samples occurrences. The sampling scheme is based on “level-crossing” that provides a non equi-repartition of the samples in time. Quantization levels are regularly disposed along the amplitude range of the signal. A sample is taken only when the analog input signal crosses one of them (cf. Figure 2-2.8). Samples are not regularly spaced out in time, because it depends on the signal variations. This kind of sampling is the dual case of Nyquist sampling: the amplitude of samples is perfectly known but their time instants are quantized.
In this context, we propose a new class of ADCs, based on this non-uniform sampling and on an asynchronous hardware implementation (without any global clock). The term A-ADC for “Asynchronous ADC” is now used. Contrary to previous works carried out in other laboratories, not only does the term “asynchronous” define the design mode but also the sampling scheme. The architecture of the A-ADC is a tracking loop enslaved on the analog signal (cf. Figure 2-2.9). It is composed of a difference quantifier, an up/down counter, a Digital-to-Analog Converter (DAC), and a timer delivering the time intervals. No external signal as a clock is used to trigger the conversion. To preserve the same state of mind, an asynchronous structure is chosen for the circuit. The information transfer is locally managed with a bi-directional control signaling between senders and receivers (requests and acknowledgements).

The theory associated with the A-ADC is completely different from classical Nyquist ADCs. The Signal-to-Noise Ratio (SNR) only depends on the resolution of the local timer and not on the number of quantization levels. A very low hardware resolution can also be implemented insuring a high SNR i.e. a high Effective Number Of Bits (ENOB). The silicon area and the power consumption can thus greatly be reduced. We have elaborated a methodology to enable the designers to precisely calculate the design parameters of an A-ADC, given a target application. The input parameters are the analog signal characteristics and the desired ENOB, from which the four parameters characterizing an A-ADC are computed: the number of quantization levels, the loop delay, the timer period, and the number of bits for the timer. The following input signal characteristics must be perfectly known: Power Spectral Density, bandwidth, dynamic, and probability density. This method also determines the design constraints on the analog blocks of the loop.

We designed an A-ADC according to this theory, using the standard CMOS 0.12µm process from STMicroelectronics, for a speech application and an effective resolution of 10-bit. The converter has been implemented with a three stage micro-pipelined architecture, and a 4-phase handshake protocol. The photography of the die is given in Figure 2-2.10.

The maximum input frequency of the converter is: \( f_{\text{max}} = 160\text{kHz} \). This is much higher than the bandwidth of a speech signal, but this fact will not cause extra useless activity, nor extra power consumption for the converter. When the chip is running at its maximum speed, a power consumption lower than \( 180\mu\text{W} \) is measured. Lastly, the targeted resolution of 10-bit is reached for a frequency of the timer lower than \( 1\text{MHz} \). The comparison of the A-ADC with standard Nyquist ADCs is done using the following Figure of Merit:

\[
\text{FoM} = \frac{2^{\text{ENOB}} \cdot f_{\text{max}}}{P_m \cdot S},
\]

where \( P_m \) is the average dissipated power in Watts, \( f_{\text{max}} \) is the maximum frequency of the input signal in Hertz, and \( S \) the area of the core of the circuit in m\(^2\). The FoMs of ADCs coming from recent publications have been computed or estimated. The best converters verify: \( \text{FoM} < 10^{19} \), and most of them: \( 10^{17} < \text{FoM} < 10^{18} \). Considering the characteristics of the A-ADC, the FoM of the A-ADC is:

\[
\text{FoM} = 2.10^{19},
\]

that is twice higher than the best ADC.

These interesting performances have been achieved by reducing the activity of the converter thanks to the non-uniform sampling scheme and its asynchronous hardware implementation. These two aspects constitute very promising ways of investigation in order to significantly reduce the power consumption of complex systems such as Communicating Objects or Smart Devices for Sensor Networks and/or ad-hoc networks applications.
2.2.9 Non uniformly sampled digital signal processing

According to the asynchronous digital signal processing chain defined in Section 2.2.8 and to the expected gain on power consumption, this work focuses on the signal theory of non-uniform sampling schemes and on possible implementations/architectures of such a non uniformly sampled signal processing.

It is well known that asynchronous designs exhibit interesting properties like low-power, low-voltage, low-EMI, etc. This kind of design has been used in a few publications to improve the performances of Nyquist ADCs such as: immunity to meta-stable behavior, reduction of the electromagnetic interference, speed, and power consumption savings. Moreover, most of the systems using ADCs imply signals with interesting statistical properties, but Nyquist signal processing architectures do not take advantage of them. Actually, these signals (such as temperature sensors, pressure sensors, electro-cardiograms, speech signals...) are almost always constant and may vary significantly only during short moments. Thus, classical regular sampling and converting systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. It has been proved that ADCs using a non equi-repartition of the samples in time leads to interesting power savings compared to Nyquist ADCs. The new class of ADCs presented in Section 2.2.8 uses both the “level-crossing” sampling scheme and an asynchronous implementation of the circuit (no global clock).

This work follows this previous contribution, joining up the A-ADC to an asynchronous implementation of a circuit processing the non uniform samples (Figure 2-2.11).

![Figure 2-2.11 Dual Approaches of Signal Processing Chains](image)

Our new approach of signal processing is to combine asynchronous designs with signal event triggered processes in order to reduce dynamic activity. This work is dedicated to low-power applications especially in the area of Smart Devices and Communicating Objects.

Many studies deal with non uniform signal theory but are limited to mathematical aspects like recovery of additive-random or jittered sampling process. We decided to study the sampling scheme of the level-crossing sampling technique. Indeed, a sampled signal is obtained in the time domain by the multiplication between the analog signal and a function called "sampling function". This implies in the frequency domain that the spectrum of the analog signal is convolved by the Fourier Transform of the sampling function: the sampling scheme. Usually in the uniform case, as the sampling function is a Dirac comb, the sampling scheme is also a Dirac comb. So the band base spectrum is duplicated around each multiple of the sampling frequency (the Shannon theorem is a consequence of the duplications). In the level-crossing non uniform case, as the sampling function depends on the signal, the sampling scheme has the same shape as the band base spectrum. Then the spectrum of the sampled signal is aliased. Thus the General Discrete Fourier Transform (GDFT) or Non-Uniform Discrete Fourier Transform (NUDFT) commonly employed for the spectral analysis of non uniformly sampled signals is useless. However, hold or linear interpolated Digital-to-Analog conversion can reconstruct a signal from its non uniform samples according to the time-interval values.
because they contain signal information. This allows a spectral analysis by computing the Continuous Fourier Transform on the interpolated functions.

Moreover, among all the digital processes, the Finite Impulse Response (FIR) filters have been chosen for their stability and convergence properties to illustrate this work. The convolution operator is formalized in the non uniform sampling context in order to define an algorithm for the FIR filtering computation of non uniformly sampled signals. An asynchronous iterative architecture is also proposed to implement the algorithm. It is formally proven that the computational complexity of the asynchronous FIR filter can be far lower than the computational complexity of the synchronous FIR filter, provided that the signal statistics are well exploited. A speech application has been considered to illustrate this new approach. It has demonstrated that the computational requirements, and hence the energy, can be reduced by more than one order of magnitude when compared to the standard uniform sampling scheme. This gain is due to the reduction of the number of samples processed. It should be noted that the gain could even be higher for other applications (medical, monitoring…).

To conclude, the digital signal processing chain using a level crossing sampling scheme behaves like the classical regularly sampled chain: an analog signal measured by a sensor can be sampled, processed and reconstructed in order to provide to an actuator a new analog signal. The difference between the standard technique and ours lies in the reduced number of samples taken for low-active signals. The level crossing scheme and the proposed signal processing theory implemented using asynchronous hardware lead to a significant reduction of power consumption making this technology very attractive for the low power SoC era. Other signal processing tools treating irregularly sampled signals such as Infinite Impulse Response (IIR) filters are currently being studied.

2-2.10 Real-time dynamic voltage scheduling: embedded asynchronous systems outperform embedded synchronous systems

Power consumption is becoming a major issue for embedded system design such as cellular phones, personal digital assistants (PDA’s) and “Internet appliances”. In these systems, there is a trend towards high performance computation and service integration which increases power demand. Reducing power consumption is required to keep autonomy and weight reasonable in these battery powered devices, to ensure reliability, and to reduce heat dissipation and system cost. A number of research efforts have recently investigated aspects of energy-efficient dynamic voltage scaling. This technique allows processors to dynamically change their voltage and speed at run-time under the control of voltage scheduling algorithms. However, there is no study that deals with asynchronous processors. This work introduces a new power reduction technique that combines an asynchronous processor and voltage scheduling algorithms. The asynchronous processor that we have designed is a CMOS standard-cell Quasi-Delay-Insensitive processor. It is ideal for embedded applications: it is low power and functional within a wide supply voltage range from 2.5 VDC down to 0.65 VDC. In cooperation with voltage scheduling algorithms that we developed, the operating system adjusts the performance level of the processor to the task requirements at run-time by controlling the processor operating voltage. This scheme exploits the ability of the asynchronous processor to self-regulate its processing speed with respect to the supply voltage.

Real-time embedded systems have often to manage periodic and sporadic tasks. While periodic tasks are commonly used to process sensor data and update the current state of the system, sporadic tasks are required to process asynchronous events. However, most of the voltage scheduling schemes presented in the literature considers systems with periodic tasks only. No attention has been dedicated to a system with sporadic tasks. We consequently consider in this work both periodic and sporadic tasks and propose 3 voltage scheduling algorithms. The first algorithm, Sporadic Tasks Voltage Scheduling, considers a case where only sporadic tasks arrive to the system. The second algorithm, Periodic Tasks Voltage Scheduling, assumes that all tasks are periodic. The last algorithm, Periodic and Sporadic Tasks Voltage Scheduling, deals with both periodic and sporadic tasks. This voltage scheduling is based on the two previous algorithms. These algorithms determine the required processor speed to regulate the processor operating voltage and so the computational power at run-time. The processor speed is computed considering workload and task deadlines and updated whenever a task is added to or removed from the system. This ensures minimum energy consumption.

Simulation results, based on real measurements performed with an asynchronous processor mother board supplied with different voltages show that low power voltage scheduling – asynchronous processor combination reduces drastically power consumption in a real-time embedded system. Further, the inefficiency of dynamic voltage scaling in synchronous systems is pointed out. Since asynchronous processor can instantly be stopped and woken up without any time overhead and the computation can continue during the voltage switching, all tasks meet their deadlines. In synchronous systems this technique is less efficient. Because sporadic tasks have random arrival times, it is difficult to predict the future idle times. Furthermore shutting down, waking up and switching voltage and frequency of synchronous
processors cause a time and energy overhead. Thus, tasks can miss their deadlines and voltage scheduling overhead is much higher.

2-2.11 Asynchronous Processors

2-2.11.a ASPRO Microprocessor

(Collaboration with France Telecom R&D & STMicroelectronics)

![Figure 2-2.12 The ASPRO microprocessor](image)

We have designed a CMOS standard-cell Quasi-Delay-Insensitive (QDI) 16-bit asynchronous microprocessor using a 0.25 µm technology (see Figure 2-2.12). ASPRO-216 has been developed for embedded applications. It can be customized both at the hardware and software levels to fit specific application requirements. It is a scalar processor which issues instructions in-order and completes their execution out-of-order. Its architecture extensively uses an overlapping pipelined execution scheme involving de-synchronized units. ASPRO owns four bi-directional serial links with 50 Mb/s throughput, two 16-bit parallel ports, 16 Kwords program memories on chip, and 64 Kbytes data memories on chip. ASPRO operates with a power supply between 0.8V and 2.5V. The performance of ASPRO-216 is 140 Mips, 0.5 Watt, at 2.5 Volts and 24 Mips, 27 mW, at 1V (see Table 2-2.1 for a comparison with other asynchronous processors).

<table>
<thead>
<tr>
<th>Processor</th>
<th>mW</th>
<th>Mips</th>
<th>Supply (V)</th>
<th>mw/Mips</th>
<th>Techno.</th>
<th>Circuit style</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASPRO (2.5v)</td>
<td>500</td>
<td>140</td>
<td>2.5</td>
<td>3.6</td>
<td>0.25</td>
<td>QDI, std-cell</td>
</tr>
<tr>
<td>ASPRO (1v)</td>
<td>27</td>
<td>24</td>
<td>1</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Caltech 1st</td>
<td>225</td>
<td>18</td>
<td>5</td>
<td>12.5</td>
<td>1.6</td>
<td>QDI, full custom</td>
</tr>
<tr>
<td>MiniMips (3.3v)</td>
<td>4000</td>
<td>170</td>
<td>3.3</td>
<td>23.5</td>
<td>0.6</td>
<td>QDI, full custom</td>
</tr>
<tr>
<td>MiniMips (1.6v)</td>
<td>220</td>
<td>60</td>
<td>1.6</td>
<td>3.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phillips 80c51</td>
<td>9</td>
<td>4</td>
<td>3.3</td>
<td>2.3</td>
<td>0.5</td>
<td>µ−pipeline, std-cell</td>
</tr>
<tr>
<td>Amulet2e</td>
<td>150</td>
<td>42</td>
<td>3.3</td>
<td>3.6</td>
<td>0.5</td>
<td>µ−pipeline, full custom</td>
</tr>
<tr>
<td>Ticac2</td>
<td>2100</td>
<td>54</td>
<td>3.3</td>
<td>38.9</td>
<td>0.5</td>
<td>SDI, full custom</td>
</tr>
</tbody>
</table>

Table 2-2.1 ASPRO compared to other asynchronous processors

The design flow we set-up to design ASPRO is described in Figure 2-2.13. The specification language used is a CSP like language called CHP (from Caltech). The processor is first described by a high level sequential CHP program which is automatically translated into VHDL and validated by simulation. This program is then refined by process decomposition and transformed to get a parallel structural version.
The synthesis phase is constrained by cycle time and latency specifications. When every part of the processor is available at the gate level, an optimization of the whole architecture is performed to get maximum performance (pipeline balancing, slack matching) according to the pipeline depths and latencies of each block (see 2.2.1.d. for details on the design flows and associated tools).

Software development tools, C compiler, assembler, linker and simulator are available for the development of applications using the ASPRO processor. We have also developed a motherboard to demonstrate the capabilities of the microprocessor. The board includes an ASPRO, flash memories for the boot, reset / interrupt logic, four communication links and a parallel interface to connect peripheral boards. Three peripheral boards have been designed, one is based on LED and Switches (see Figure 2-2.14), another one includes an RF interface and the last one is a digital camera. Experiments performed with the motherboard shows that the processor is running correctly down-to 0.65 volt (nominal supply voltage is 2.5 Volts).

An example of a system built using the boards we have designed is presented in Figure 2-2.14. This is a multiprocessor system based on two ASPRO processors, a camera and an RF interface. The application consists in capturing an image, processing it and transmitting the result through the radiofrequency. This prototype enables us to carry on experimentation on multiprocessor systems, low power Operating System implementing a dynamic voltage scheduling strategy.
2-2.11.b MICA micro-controller
(Collaboration with France Telecom R&D & STMicroelectronics)

MICA is a QDI asynchronous 8-bit micro-controller CISC machine, based on a dedicated "luxurious" micro-architecture (see Figure 2-2.16). In order to facilitate the design of a "C" compiler and also to limit memory accesses, we decided to integrate two different register-files: eight 8-bit registers are devoted to data, and eight 16-bit registers are devoted to pointers (including the program counter and the stack pointer). Specific arithmetic units are associated with each register files enabling concurrent computations of data and addresses. A dedicated unit is managing the standard status bits Z, N, V and C. A peripheral unit is also included, supporting six 8-bit parallel ports (1 input, 4 outputs and 1 bi-directional used to control external flash memories and the synchronous/ asynchronous interface) and four serial links (using a two-phase delay insensitive protocol compatible with our high performance RISC asynchronous ASPRO processor – described above -). Moreover, the micro-controller integrates 16 Kbytes RAM and 2 Kbytes ROM. The latter includes a Built-In-Self-Test which is executed at reset according to the boot mode selected (eight modes are available). It is a 350 assembly instruction routine which performs a complete stuck-at-fault test, thanks to the QDI asynchronous logic. The BIST routine computes a signature written on the fly, on one of the parallel port to report on self-test progress.

- Instruction set

The eight 8-bit data registers are named r0 to r7, and the eight 16-bit index registers i0 to i7, where i6 and i7 are the stack-pointer and the program-counter respectively. The controller implements the common arithmetic and logic instructions. All instructions are encoded within one word (16 bits). Four basic addressing modes are available (immediate, register, indexed with displacement, indexed post-incremented or pre-decremented) which can be used in conjunction with data or index register operands. Lastly, the controller implements a maskable interrupt mechanism and a "wait for interrupt" instruction (Wfi). Table 2.2.2 summarizes the instruction set, note the "copy" (Cp) and the "Puch&Load" (Pl) instructions. A complete software development suite of tools is currently under development including a "C" compiler, an assembler, a linker and a simulator.
logic/arithmetic processing units. The register files are also designed with 4-rail encoded data. Instead of bit-
	the number of transitions per communication action, and hence minimizes the dynamic power consumption.
	Finally, at the signal level, communication channels are using a low power data encoding. Instead of using
	A four-phase protocol is used in conjunction with an n-rail encoding. This chip has been a vector for developing new skills

time to memory is available)  
P1 (push & load)  
Psh, Pshsr (push, push status register), Pop  
Index  
Pshx, Popx  

Control flow  
Rti, Rts, Jmp, Jsr  
Bcc, Bsrcc (cc = a, eq, ne, cc, cs, l, le, lt, le, ge, gt, gte, vc, vs)  

Misc  
Nop, Wfi, Eint, Dint (enable and disable interrupt)  

Table 2-2.2 The MICA microprocessor Instruction set

- Architecture design

The micro-controller core is designed using the so-called Quasi Delay Insensitive (QDI) logic. A four-phase
protocol is used in conjunction with an n-rail encoding. This chip has been a vector for developing new skills
in the design of standard-cell based QDI asynchronous circuits. The design of MICA was focused on two
related concerns: designing distributed asynchronous finite state machine and designing for low power.
In order to reduce the power consumption of the micro-controller we have worked on minimizing the number
and the energy-cost of communication actions occurring during the execution of each instruction, and
minimizing the number of sequential steps to perform each instruction. In other words, instead of designing
the architecture around a big central sequencer, we have tried to distribute the sequencing implementation
all over the architecture as much as possible. The asynchronous logic is particularly well suited to satisfy
such a design approach since by nature the sequencing of an asynchronous circuit is performed by multiple
local sequencers implementing handshaking communications and local treatments.
Thus, the architecture of MICA has been designed as a distributed system, each part providing specific
services. For example, the two register-files, the status register and the memory integrate local units which
manage the memory resources. These modules implement functions such as "read", "write", "read then write
back" or even more complex function like : read a byte, increment/decrement the pointer/address and read
the corresponding byte (Cp and Pl instructions for examples use these features). Adopting such an approach
significantly simplifies the design of the main sequencer of a CISC microprocessor like MICA. It then
minimizes the power consumed by the main sequencer, the consumption associated with each instruction
being the direct image of its complexity. In fact, complex instruction implementation does not penalize simple
instruction implementation at the main sequencer level. Moreover, such a distributed approach minimizes the
power consumed by communications since the minimum number of transactions occurs through busses
(memory accesses for example).
Because of the low-power constraint and because computational power was not a priority for the targeted
applications, a minimum number of pipeline stage was introduced. This does not prevent parallel execution
of instruction sub-parts, but simply means that parallel execution of instructions is not supported. In some
cases however, subsequent instructions may partially overlap.
Finally, at the signal level, communication channels are using a low power data encoding. Instead of using
dual-rail coding, we have implemented N-rail coding (also called "One Hot"), i.e. one out of the N wires is
active during a transaction (instead of one out of two with dual-rail). The different parts of the architecture are
all controlled by the main sequencer through channels using 5-rail to 12-rail data encoding which minimizes
the number of transitions per communication action, and hence minimizes the dynamic power consumption.

The data paths (8-bit and 16-bit) are entirely designed with 4-rail encoded data, requiring radix-4
logic/arithmetic processing units. The register files are also designed with 4-rail encoded data. Instead of bit-
registers they are built of digit-registers, each digit representing 4 values.
• Micro-controller performance

A test chip has been designed, fabricated and tested. The micro-controller has been easily tested thanks to the BIST, and was fully functional at first silicon between 3 Volts down to 0.8 Volt (2.5 Volts is the nominal voltage of the.25\mu m CMOS technology used). Table 2.2.3 gives the Mips (mean number of instructions executed per second when running the BIST program), Power and Mips/watt figures at different voltages (based on the total current consumed by the core, the memory and the pads). It is noticeable that the chip only consumes 800 µW at 1 volt, still delivering a computational power of 4.3 MIPS. At 0.8 volt, the chip consumes less than 400 µW.

<table>
<thead>
<tr>
<th>Supply(V)</th>
<th>Mips</th>
<th>Current (mA)</th>
<th>Power(mW)</th>
<th>Mips/Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,0</td>
<td>4,3</td>
<td>0,8</td>
<td>0,8</td>
<td>5503,6</td>
</tr>
<tr>
<td>1,5</td>
<td>11,9</td>
<td>3,1</td>
<td>4,7</td>
<td>2560,2</td>
</tr>
<tr>
<td>2,0</td>
<td>18,6</td>
<td>6,7</td>
<td>13,3</td>
<td>1398,0</td>
</tr>
<tr>
<td>2,5</td>
<td>23,8</td>
<td>11,2</td>
<td>28,0</td>
<td>850,3</td>
</tr>
</tbody>
</table>

Table 2.2.3  MICA measured performances

We have developed a motherboard to demonstrate the capabilities of the MICA microprocessor. The board includes a MICA processor, a flash memory for the boot (and also programmable), reset / interrupt logic, four communication links and a peripheral interface. The same peripheral board developed for the ASPRO processor can be used. This system enabled us to show that the processor is running correctly down-to 0.65 volt (see Figure 2-2.17).

2-2.12 Arithmetic operators

2-2.12.a Automatic generation of arithmetic operators

The CIS group participates in the development of web-based support for VLSI design training. In this framework, it is currently developing exercises on arithmetic operator synthesis and characterisation. They are aimed to be a self-training lecture completement.

Table 2-2.4 lists available exercises, implemented in JavaScript and Java. The exercises fall in 4 categories: synthesis, simulation, diagram (plot) and operation part synthesis.
Activity in carry propagate adders: Simulation
Carry propagation free addition (Carry Save): Simulation
Brent-Kung carry look-ahead tree generation: Synthesis
Serial multiplication (add/sub and shift): Simulation
Generation of multipliers partial products: Synthesis
Generation of multiplier reduction tree: Synthesis
Generation of modulo reduction (for self-checking operators): Synthesis
Layout of "Robertson's diagram" for division: Diagram
Datapath of a sequential divider: Operation part
Sequential division (add/sub and shift): Simulation
Datapath of a square root extractor: Operation part
Sequential square root extraction (add/sub and shift): Simulation
Floating point add/subtract/multiply/divide: Simulation
Datapath of a sequential logarithm (Cordic): Operation part
Sequential logarithm and exponential (add/sub and shift): Simulation
Layout of the convergence domain for Sine/Cosine (Cordic): Diagram
Sequential sine and cosine (add/sub and shift): Simulation

<table>
<thead>
<tr>
<th>Table 2-2.4 List of available exercises</th>
</tr>
</thead>
</table>

**Figure 2-2.18** shows a typical synthesis. The result in the right window can be edited, verified and simulated.

**2-2.12.b Asynchronous arithmetic operators**

Skills developed in automatic generation and design of synchronous arithmetic operators are naturally exploited to conduct research in the domain of asynchronous arithmetic operators. The goal of this work is to provide the TAST synthesis tool with powerful adder and multiplier generators. Therefore, based on our knowledge on asynchronous circuit, arithmetic operators are revisited for the design of compact, fast and low-power asynchronous structures.
Generalized 1-of-M QDI Asynchronous Adders.
In this area, we first focused on QDI asynchronous adders’ generation. Ripple-carry and parallel-prefix adders using 1-of-M data encodings are studied and generalized. Automatic generation of these adders’ structures is integrated into the TAST environment as illustrated in Figure 2.2.19. It is also available as a stand-alone tool with a graphical user interface. This tool allows the designer to explore and compare several implementations for a desired adder.

Many adders were generated using distinct digit numbers and digit data encoding. The results were compared in terms of area, power consumption and latency. A first analysis shows that increasing M in ripple-carry adders leads to increase the area. However, increasing M lead to lower the digit number and therefore implies reducing power consumption and critical path length. Parallel-prefix adders exhibit different behaviour. In these adders, carry computation redundancy is used to allow parallel carry resolution. The carry tree computation is only dependent of the number of digits. So, increasing M and hence reducing the digit number reduces the redundancy in these adders. In this way, increasing M conducts to smaller, faster and lower power consumption adders. Table 2.2.5 shows a comparison between a 128-digits dual-rail encoded adder and a 64-digits 1-of-4 rails encoded adder (standard-cells based designs).

<table>
<thead>
<tr>
<th>Domain</th>
<th>encoding</th>
<th>digits</th>
<th>#wires</th>
<th>Area #transistors</th>
<th>Power #transitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2^{128}$</td>
<td>dual-rail</td>
<td>128</td>
<td>256</td>
<td>23332</td>
<td>1169,25</td>
</tr>
<tr>
<td></td>
<td>1-of-4</td>
<td>64</td>
<td></td>
<td>22042</td>
<td>573,63</td>
</tr>
<tr>
<td>% Reduction</td>
<td></td>
<td></td>
<td></td>
<td>5.53</td>
<td>50.94</td>
</tr>
</tbody>
</table>

Table 2.2.5 – Comparaison between dual-rail and 1-of-4 rails implementation for Sklansky parallel-prefix adder

The obtained results show the limitation of the commonly used dual-rail representation when fast adders have to be designed. This tool enables the designer to choose the data encoding in order to optimize his/her adder designs. Future work will be focused on applying this approach to other arithmetic functions such as multipliers, as well as logical functions.
2-3 Reliable Mixed-signal Systems (RMS)

**Group Leader:** S. Mir  
(e-mail: Salvador.Mir@imag.fr)


(*ST Microelectronics & TIMA, *RMS and CIS Groups, #Hong-Kong University of Science and Technology)

<table>
<thead>
<tr>
<th>Research areas</th>
<th>Contracts</th>
<th>Industrial Partners</th>
</tr>
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<td>Test techniques for mixed-signal integrated circuits and systems</td>
<td>TECHNODAT (MEDEA+ T-101, 2001-2004)</td>
<td>ST Microelectronics</td>
</tr>
<tr>
<td>Computer-Aided-Test (CAT) tools for mixed-signal testing</td>
<td>CIFRE-ST 2002-2005</td>
<td>Atmel</td>
</tr>
<tr>
<td>Design of mixed-signal circuits and microsystem electronic interfaces</td>
<td>CIFRE-ST 2003-2006</td>
<td>Philips</td>
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<tr>
<td>Design and test of microsystems</td>
<td>IPCI (LEONARDO, 2003-2004)</td>
<td></td>
</tr>
</tbody>
</table>

2-3.1 Design and test of mixed-signal circuits

2-3.1.1 Analogue BIST based on harmonic testing

**Members:** G. Prenat, L. Rolíndez, S. Mir, D. Vázquez*  
(´Instituto de Microelectrónica de Sevilla IMSE-CNM, Sevilla, Spain)

This work is aimed at providing a low-cost fully digital and programmable approach for testing mixed-signal cores. Since most of a complex circuit is digital, it is very interesting to use a test technique which is compatible with low-cost digital testers instead of using very expensive mixed-signal testers. We have then studied a full BIST technique based on harmonic testing. A BIST silicon demonstrator has been fabricated using a 0.18µm CMOS ST Microelectronics technology to validate the technique. **Figure 2-3.1** shows the overall architecture of the BIST and the fabricated demonstrator.

![Figure 2-3.1](image)

**Figure 2-3.1** Mixed-signal BIST based on harmonic testing: (a) overall architecture of the BIST technique and (b) silicon demonstrator

The analogue test signal generation follows a known approach of loading a Circular Shift-Register (CSR) with a binary stream encoding the required analogue signal. This binary stream is generated by a CAT tool using a model of an oversampling second order ΣΔ converter. Once the binary stream is loaded, the CSR is...
clocked at the sampling frequency producing at its output a periodic binary stream. This stream is filtered by a programmable third order switched-capacitor low-pass filter to recover the analogue signal. By programming the length of the CSR and the sampling frequency, it is possible to have a frequency resolution better than 0.1 percent, in the range from 10 Hz to 1 MHz. In this demonstrator, we have chosen a length for the CSR between 100 and 200 bits, so that the amplitude of the test signal has less than 8 bits of resolution. Figure 2-3.2 shows simulation and test results for the generation part. In this case, the signal generated is a sine wave signal at 833 Hz that shows an SFDR around 60dB.

Figure 2-3.2 Demonstrator signal generation results: (a) spectrum of an 833 Hz sine-wave signal generated by simulation and (b) spectrum of the same signal generated by the chip

The analogue response analysis consists in generating digital signatures that represent the harmonics of a test signal response. This is done by using a known technique of modulating the test signal by two square wave signals with phases 0 and $\pi/2$, respectively, at the frequency of the required harmonic. This technique is especially easy to implement here, since the square waves can be directly obtained from the signal generation part of the BIST. The result of each square wave modulation is encoded into a binary stream and next integrated by a 16-bit counter, providing one of the two components of the harmonic signature.

The suitability of this technique for detecting circuits out of specifications has so far been evaluated by Monte Carlo simulations. Figure 2-3.3 shows the results of simulations of the BIST technique in Figure 2-3.1, using the third order low-pass filter as the circuit under test. For this linear circuit, the signature $I_1$ corresponding to the fundamental component $H_{1\text{nom}}$ provides the best results in terms of false acceptance (FA) and false rejection (FR). Currently, experimental tests are under way to evaluate the BIST quality of the silicon demonstrator. Obviously, test quality must improve by using a test signal with a precision much higher than 8 bits. This just requires using more bits in the CSR. For a first demonstrator, we have chosen a lower resolution in order to see experimentally the quality of the test results with such a low-cost implementation.

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<th>Signature space</th>
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<tr>
<td>Test parameters</td>
<td>$I_0$</td>
</tr>
<tr>
<td>Yield</td>
<td>98.30</td>
</tr>
<tr>
<td>Escapes</td>
<td>32.35</td>
</tr>
<tr>
<td>FA</td>
<td>31.80</td>
</tr>
<tr>
<td>FR</td>
<td>01.10</td>
</tr>
</tbody>
</table>

$n = 1000$
Fault-free circuits = 676
Faulty circuits = 324
$I_{0\text{min}}=0.190, I_{0\text{max}}=0.2130, H_{0\text{nom}}=0.2000$
$I_{1\text{min}}=0.3441, I_{1\text{max}}=0.3650, H_{1\text{nom}}=0.3538$
$I_{2\text{min}}=0.370e^{-3}, I_{2\text{max}}=0.370e^{-3}, H_{2\text{nom}}=1.1443e^{-4}$

Figure 2-3.3 Results for the signature analysis with 1000 instances generated by Monte Carlo simulation: (a) test quality parameters for different harmonic signatures and (b) distribution of the signatures corresponding to the fundamental harmonic
2-3.1.2 Structural testing of radio-frequency integrated circuits

Members: R. Kheriji+, V. Danelon*, S. Mir, J.L. Carbonero*
(*ST Microelectronics, Crolles, France, +TIMA and ST Microelectronics)

The integration on the same System-on-Chip (SoC) of digital, mixed-signal and Radio-Frequency (RF) cores is a main challenge in the development of wireless devices. Apart from the design challenge, the cost of testing these devices is a major concern given the costs of RF testers and the length of test times. Production testing of RF components generally targets the validation of the functional specifications. Often, market pressures and reduced testing time limits the number of functional specifications that are actually verified during production.

This work has studied defect-oriented test techniques for RF front-end components with the intention of optimizing production test sets. A fault simulation campaign for a 0.25 µm BiCMOS ST Microelectronics Low-Noise Amplifier (LNA) configured as shown in Figure 2-3.4(a) has been used to verify the suitability of applying just simple current consumption tests rather than more sophisticated tests directed to measure functional specifications such as S parameters and Noise Figure (NF). Fault simulation results for catastrophic faults in the LNA are shown in Figure 2-3.4(b). S parameters have the highest fault coverage. Results of this study indicate that fault coverage of 89.6 % is obtained using only parameter S11. The most important information is that we need essentially the measure of one S parameter and of the current consumption in order to achieve the highest fault coverage (96 %). The measurement of the NF, IP1 and IP3 parameters are not so relevant for the detection of catastrophic faults. The analysis of parametric faults is currently under way.

![Figure 2-3.4 Optimisation of test sets for RF circuits: (a) ST Microelectronics Low Noise Amplifier in its testing configuration, and (b) fault coverage results for LNA catastrophic faults allowing for an optimal selection of test measurements](image)

2-3.1.3 On-line testing of digital circuits for mixed-signal BIST

Members: E. Simeu, S. Mir

Classical BIST techniques correspond to an off-line testing philosophy, suitable for end-of-production testing or for periodic life-time testing. Strong reliability constraints have contributed to the evolution of highly reliable digital components. For applications requiring high system reliability, some kind of on-line testing techniques for identifying faults occurring during normal operation of the product has to be introduced. Such solutions generally exploit characteristics of the application to achieve the required performance while limiting the redundancy needed. Different on-line self-test techniques are studied in our activity related to this topic including non-concurrent, semi-concurrent and concurrent approaches.

In our non-concurrent self-checking techniques, a test sequence is applied to the system functional units (FUs) at predetermined idle times in the operation of the system. This approach is especially useful in systems that run for extended periods during which FUs are not requested in the nominal operation.
On the other hand, concurrent test techniques continuously check for errors in the system. Our solution is built on the model-based parity space fault detection and isolation (FDI) which, compared to other known FDI architectures, allows not only efficient fault coverage but also efficient implementation facilities inducing small area overhead. The basic principle of the approach is based on the generation of detection signals (also called residuals) using only actual and previous available signal values (see Figure 2-3.5(a)). These residuals are sensitive to the occurrence of faults as shown in Figure 2-3.5(b). The detection signal must be able to detect the occurrence of a fault as well as to isolate its effects from all other undesirable inputs (as disturbances) affecting the system behaviour.

Our semi-concurrent self-checking approach is introduced during high-level synthesis. The proposed approach relates to arbitrary application-specific systems, described by data flow graphs (DFG). The aim of the approach can be summarized as follows: for a given periodicity of checking and a given optimum nominal scheduling and allocation of a DFG, we synthesize a new data path that will allow semi-concurrent self-checking with minimum redundancy of functional units and minimum risk of aliasing. These techniques are being applied to the digital components of analogue BIST architectures.

As a case-study, on-line test techniques have been studied for the decimation filter of an ΣΔ Analogue-to-Digital converter that is in turn used in a BIST circuitry for mixed-signal core testing. Thus, the filter itself must be self-testable for an implementation in a 0.18 μm CMOS technology. A basic stage of the decimation filter is composed of a Cascaded-Integrator-Comb filter (CIC). The structure of a 3rd order filter of this type is shown in Figure 2-3.6(a). It contains two basic building blocks: an integrator and a comb. The filter has a typical audio Nyquist rate of 44.1 kHz with a sampling frequency of 5.6448 MHz, thus an OSR of 128. Semi-concurrent and non-concurrent on-line test approaches have been studied for this filter for an implementation in a 0.18 μm CMOS technology. In all cases, the on-line test circuitry is automatically synthesized and exploits the idle time of the FUs to apply either a structural or a functional test. The impact of these methods on the circuitry is analyzed in terms of area and timing overhead. In terms of area, the semi-concurrent on-line testing methods are more suitable for small area digital systems than the non-concurrent technique. A practically negligible area overhead is obtained when an on-line test DFG is inserted in the idle times of the nominal scheduling. In terms of timing overhead, since the highest sampling frequency of the filter (5.6 MHz) is much smaller than the possible operation frequency of the FUs (above 100 MHz), the insertion of the on-line testing approaches do not degrade at all the timing specifications in all cases. Figure 2-3.6(b) shows the architecture of the filter with the semi-concurrent on-line test technique.
2-3.1.4 CAT tools for mixed-signal testing

Members: A. Bounceur, S. Mir, E. Simeu

2-3.1.4.1 Analogue fault simulation tool

We are developing a new fault modelling, fault injection and fault simulation environment that must be independent of the type of cell considered (digital, analog or even microsystem) and of the level of representation (schematics, layout, behaviour). The graphical interface of the tool, which is being integrated in the CADENCE design framework environment, is shown in Figure 2-3.7.

As an example of fault injection, Figure 2-3.7(a) shows the injection of short between the drain and the source of the CMOS pixel. A graphical interface allows the definition and selection of the fault models used (see Figure 2-3.7(b)). Each simulation represents a faulty pixel generated by injecting one fault in the fault list. Figure 2-3.7(c) shows an example of fault coverage graph. Finally, Figure 2-3.7(d) shows the different test parameters calculated for a campaign of 20 fault simulations. These parameters include yield, false acceptance, false rejection and percentage of test escapes.
Figure 2-3.7 Analogue fault simulation tool: (a) example of injection of a short fault between the drain and source of a CMOS imager pixel, (b) graphical interface for the definition and selection of fault models, (c) example of fault coverage graph, and (d) the test evaluation parameters window

2-3.1.4.2 Analogue test pattern generation tool

Members: A. Bounceur, S. Mir, E. Simeu

A tool has been developed for determining the digital test vector that must be loaded in the BIST unit described in Section 2-3.1.1. The tool takes as input a description of the required analogue signal (typically a single or multi-tone test signal) and produces as output the digital test vector that must be loaded in the test circuitry, optimising the shift-register length and the sampling frequency that allow obtaining the best analogue signal in terms of parameters such as Total Harmonic Distortion, Spurious Free Dynamic Range or Peak-to-RMS values. Different algorithms for multi-objective optimisation have been implemented. Figure 2-3.8(a) illustrates the graphical interface of the tool that is fully integrated in the CADENCE environment. Figure 2-3.8(b) shows an example of a multi-objective optimisation, S/THD and amplitude deviation (ADev), of a multi-tone test signal using two different algorithms: Monte-Carlo and WARGA (Weighed Average Ranked Genetic Algorithm). For single tone signals the use of the WARGA algorithm is recommended. For multi-tone signals, the use of Monte-Carlo algorithm is best. Finally, Figure 2-3.8(c) shows an example of a digital test vector generated by the tool in a format directly acceptable by a digital tester.

Figure 2-3.8 Analogue test pattern generation: (a) graphical interface of the tool, (b) optimisation of S/THD and ADev by using Monte-Carlo and NSGA methods and (c) test vector generated by the tool in a format compatible with a digital tester
2-3.1.5 BIST of CMOS imager pixels

Members: L. Lizarraga, E. Labonne*, G. Sicard*, S. Mir
(*CIS Group)

Current test techniques for CMOS imagers use a special tester that includes light sources, making the test of these devices more complicated and expensive. In general, BIST techniques for CMOS imagers have not yet been considered, basically because of the light stimuli needed for testing the photosensitive elements that cannot be generated on-chip. Thus, there are no CMOS imagers with self-test capabilities. In this work, we are investigating a BIST technique for the pixels of a CMOS imager using electrical signals for the stimuli of all components. In particular, we are studying the possibility of electrically testing photosensitive elements within the chip. This technique can allow the detection of malfunctioning pixels, enabling the system to evaluate the quality of the images and to introduce techniques of error correction. We use the CAT tools developed in the RMS group for the validation of the structural BIST technique. The main objective of the structural BIST is to make the production test of CMOS imagers compatible with digital testers and thus reducing costs. This project is carried out in collaboration with ATMEL.

2-3.1.6 Bulk-driven CMFB circuit for a fully differential amplifier

Members: L. Rolíndez*, S. Mir.
(*TIMA and STMicroelectronics)

With the downscaling of the CMOS processes, integrated circuits include low-voltage and complex analogue and digital circuits in the same die. In this context, the use of fully-differential signal paths presents several advantages over the utilisation of single-ended circuits. Common noise existing in both signal paths does not affect the differential signal, and the power supply rejection ratio is notably improved. This is very important in mixed-signal circuits, where the substrate receives much noise from the digital blocks. Moreover, the use of differential signals doubles the voltage range, increasing the dynamic range by 6 dB. In fully-differential amplifiers, a common-mode feedback (CMFB) circuit is required in order to establish the output common voltage. The design of this circuit is a difficult task because the common-mode loop (necessary for the control of the output common voltage) should have a gain as high as possible and a bandwidth similar to that of the differential loop (which performs the differential amplification). Furthermore, in contrast to the input stage, the output stage works with large differential signals, and the CMFB circuit ought to correctly work through the whole output swing. That is why the performances of fully-differential amplifiers are limited by the CMFB circuit.

In this activity, we have designed a new CMFB circuit (Figure 2-3.9) which allows for an improvement of the performance of fully-differential amplifiers. It is based on the detection of the common-mode (CM) voltage by means of a bulk-driven differential pair, which in contrast to the gate-driven differential pair, does not reduce the output swing by a threshold voltage ($V_{th}$). This circuit detects the output common voltage ($V_{out}$) and generates $V_{CM}$ to counteract any deviation of the CM voltage from $V_{ana}$. The separation of the bulk-driven transistor substrates is made by using different N-Well regions. This technique has been applied to a folded-cascode fully-differential amplifier and implemented in a 0.18 µm CMOS ST Microelectronics technology. Table 2-3.1 shows the performances obtained. High gain, high slew-rate, low distortion and very large output swing are obtained with a very small die area (3180 µm²).

![Figure 2-3.9 Bulk-driven CMFB circuit](image)

<table>
<thead>
<tr>
<th>Parameter</th>
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</tr>
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<td>$GBW_D$</td>
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<td>$A_{CM}$</td>
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<td>Phase Margin $\phi_{CM}$</td>
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<td>Output Swing</td>
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<td>SR+, SR− ($C_{C}=1$ pF)</td>
<td>6.15 V/µs</td>
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<tr>
<td>THD</td>
<td>-77.07 dB (2.4 Vp-p @ 1kHz)</td>
</tr>
<tr>
<td>ID</td>
<td>-79.17 dB (1.2 Vp-p @ 9.11kHz)</td>
</tr>
<tr>
<td>Equivalent Input Noise</td>
<td>42 nV/√Hz @ 100kHz</td>
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<tr>
<td>CMRR</td>
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</tr>
<tr>
<td>PSRR</td>
<td>78.6 dB @ 1kHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2.50 mW</td>
</tr>
</tbody>
</table>

Table 2-3.1 Bulk-driven CMFB amplifier performances
2-3.2 Design and Test of Microsystems

2-3.2.1 BIST of linear MEMS using MLS

Members: L. Rufer, A. Dhayni, S. Mir, E. Simeu

It is well known that the input-output Cross-Correlation Function (CCF) of a LTI system provides an estimation of the system impulse response when the input signal has the frequency spectrum of a white noise. It is also known that the auto-correlation of a pseudo-random signal approaches the one of a white noise for small values of the rectangular pulse width and high values of sequence length N. These facts have been exploited in the past for pseudorandom testing of mixed-signal circuits. We have developed a cost-effective implementation of this technique and its application to different AMS components, including Micro-Electro-Mechanical-Systems (MEMS). The technique is based on Impulse Response (IR) evaluation using pseudo-random Maximum–Length Sequences (MLS). This technique provides a vastly superior dynamic range in comparison to the straightforward technique using an impulse excitation. It is then suitable for measurements in noisy environments and for low-power test signals. It also leads to a practical on-chip implementation that is efficient in terms of the extra hardware required.

As shown in the block diagram of this implementation in Figure 2-3.10(a), the MLS signal $x(k)$, generated by means of a Linear Feedback Shift-Register, is directly applied to a sampled input LTI Circuit Under Test (CUT). An ADC at the CUT output provides the digital output signal $y(k)$ that is correlated with the MLS signal $x(k)$ in the correlation block. The output signal of the correlator $h(k)$ corresponds to the impulse response of the CUT that is used to construct a signature for testing. The structure of the correlator block is shown in Figure 2-3.10(b), with a Simplified Cross-Correlation (SCC) block being described in Figure 2-3.10(c).

As an example, we have applied this BIST technique to the case of basic MEMS components such as cantilevers and bridges for which we consider electrothermal stimuli generation and piezoresistive detection. Figure 2-3.10(d) shows an example of a self-testable MEMS device containing several cantilevers that have been fabricated using a 0.8 µm CMOS bulk micromachining technology. The surface of each cantilever is covered with heating resistors made with polysilicon. The heating of the cantilever will cause it to bend, and the actual deflexion is measured by means of piezoresistors placed at the anchor point of the cantilevers. For each cantilever, a Wheatstone bridge is used for measurement. Temperature compensation is achieved by using two piezoresistors at the anchor of each cantilever, one transversal and one longitudinal. One of the problems that can be encountered for the test of these microstructures is the broad frequency range covered by the mechanical and thermal behaviour. Indeed, thermal time constants are generally much larger than mechanical time constants. We have demonstrated that the MLS-based BIST technique allows for an on-chip fast and accurate broadband determination of MEMS behaviour.
The MLS method has been used for finding the IR of the MEMS, without any consideration of nonlinear and noise distortions that can exist in the measurement circuitry. Different IR measurement techniques are now considered and compared according to their immunity to nonlinear and noise distortions. The most important disadvantage of the MLS Impulse Response based BIST technique is its low immunity to distortion due to weak nonlinearities. To measure the distortion immunity and compare between different BIST test signals, the measurement system in Figure 2-3.10(e) has been designed. For each of the measurement techniques, the test signal is generated in Labview and then applied through the data acquisition card NI PCI-6115 to the linear DUT. The output signal is then digitized in the 12-bit ADC found at the input of the NI PCI-6115 and entered to Labview where signal processing is done to evaluate the corrupted impulse response of the DUT and calculate the corresponding distortion immunity and signal to noise ratio.

The test signals considered are the IE (Impulse excitation), MLS and IRS (Inverse Repeated sequence). The IRS has proved a total immunity advantage over both MLS and IE, and MLS has a total immunity advantage over IE. We noticed that for even-order nonlinearities IRS has a very high immunity advantage over MLS (235.642 dB at the second-order nonlinearity and 79.35 dB at the third-order one). However only approximately 3 dB of immunity advantage can be offered by the IRS for the case of odd-order nonlinearity. As a result, in spite of the extra hardware and complexity that is needed in the BIST and the fact that using IRS will increase the test time, IRS is much more interesting when testing a DUT in the presence of even-order nonlinearity. However, in the present of just odd-order nonlinearity in the DUT, choosing the MLS is better because it is simpler and the 3 dB of immunity advantage offered by the IRS can be compensated by a single averaging of the output sequence. Other IR measurement techniques than these listed above were considered. Among these techniques are the linear and logarithmic sweep techniques that require a fast Fourier transform calculator. The complexity of this calculator needs a Digital Signal Processing unit on-chip with the BIST.

2-3.2.2 Towards BIST techniques for non-linear MEMS behaviour

Members: A. Dhayni, S. Mir, L. Rufer

Generally the binary MLS method can be employed only to test and model linear devices. In our work, to test nonlinear MEMS, some modifications are added to the test sequence in order to be used to stimulate nonlinear DUTs as well. These modifications depend on the existing nonlinearity. According to the nonlinear system modeling theory, we demonstrate our technique by comparing the results with the Volterra kernels coefficients usually used in nonlinear system modeling (see Section 2-3.2.3). The sophisticated methods used to calculate the Volterra kernels are replaced by the simple MLS method, allowing for a BIST implementation.

In the case of purely nonlinear systems, as the case of the microbeam shown in Figure 2-3.10(d), modification of the MLS_{(-1,1)} may be needed according to the kind of nonlinearity. In general, purely nonlinear systems can be modeled by the Hammerstein model shown in Figure 2-3.11. Here the 1st Volterra kernel (Linear IR) is zero and hence we are obliged to evaluate higher order kernels. For the microbeam, the dynamic linear part corresponds to the linear IR of the suspended microbeam, and the static nonlinear part is the squaring function due to the electrothermal excitation.

Once x(k) is chosen such that x(k) = w(k), the crosscorrelation of x(k) and y(k) can be derived as function of h(k). In this way, coefficients of higher order Volterra kernels can be evaluated. For the case of a nonlinear system other than the Hammerstein model, the BIST can be applied only to test the linear behavior. We consider this as a sufficient test since any fault will harm in general both the linear and nonlinear behaviors.
Experimental results have been obtained for this microbeam where the BIST has been modeled in Labview using the test setup of Figure 2-3.10(e). Work is on the way to fabricate the BIST circuit and add it on-chip. For the nonlinear case, only the test signal will be modified and hence the BIST architecture remains as shown in Figure 2-3.10(a).

2-3.2.3 Test pattern generation tool for non linear MEMS

Members: A. Bounceur, A. Dhayni, S. Mir, L. Rufer

We have developed a tool for the generation of multi-level test patterns suitable for non linear MEMS testing. A polynomial model of a non linear system is described as

\[ y(k) = h_0 + \sum_{r=0}^{N-1} \sum_{m_1=0}^{M-1} \sum_{m_2=0}^{M-1} h_r (m_1, m_2) \times \prod_{j=1}^{r} u(k - m_j) \]

where \( u \) and \( y \) are, respectively, the input and the output of the system, \( N \) is the order of nonlinearity, \( M \) is the memory of the system and \( h_i \) is the \( i \)-th order Volterra Kernel that carries information only about the \( i \)-th order nonlinear behaviour of the system.

In this work, we have used the well known Wiener model of non linear systems and we have developed a tool that allows the generation of a multi-level test pattern to stimulate the MEMS. Figure 2-3.11(a) shows the graphical interface of this tool that has been developed using the language Builder C++ language. An special feature of the tool is the ease to manipulate the matrices required in the computations. Figure 2-3.11(b) shows an example of a MEMS second order Volterra Kernel calculated by the tool and Figure 2-3.11(c) the required multi-level test stimuli for measuring this order of non-linearity in the MEMS under test.

![Figure 2-3.11 Analogue test pattern generation for non linear MEMS: (a) graphical interface of the tool, (b) example of the 2nd order Volterra Kernel calculated by the tool and (c) multi-level test stimuli for measuring this order of non-linearity](image)

2-3.2.4 Test techniques for RF MEMS

Members: N. Nguyen, L.Rufer, S. Mir, P. Cauvet*  
(*Philips Caen, France)

Technologies of the type SiP (System-In-Package) and SoC (System-on-Chip) allow integrating MEMS (Micro Electro-Mechanical Systems) components and micro-electronics parts on separated chips in the same package, or directly on the same substrate. The design of such systems makes use of many advantages which are compactness and uniformity of the medium enclosing these systems, shorter data paths, smaller parasitics, and increase the speed and bandwidth of communication. But increasing levels of integration and high speeds of operation have made the problem of testing very difficult. This new integrated level asks for new methods of test in order to obtain a good coverage of defects and faults. There are no solutions of test and diagnosis available for MEMS RF. Recently, some solutions of structural test for low-frequency MEMS components (e.g. accelerometers) have been proposed. But techniques of integrated test for MEMS RF (e.g. SAW and BAW filters, RF switches, or variable capacitors) do not yet exist.

Testing of complex SiPs may proceed in two phases: “verification testing and design debugging” and “manufacturing test”. The design verification procedure consists of application of a set of “verification tests” followed by design diagnosis. If necessary, the design is altered, new prototypes are built and a new set of
tests are applied until eventually a “perfect” design is obtained. Hence, the goal is to identify SiPs that are defective through application of tests during volume production. A typical SiP encapsulates many of its internal functions but production test is performed by application of test signals to the SiP under control of external automatic test equipment (ATE). The key problem is that the external ATE does not have direct access to all the internal embedded functions of the SiP. However, these internal signals operate at frequencies that cannot be observed directly by an external ATE due to the frequency limitations of the encapsulating package and lower speed of external I/O. This problem can be estimated by the fact that test cost is approaching almost 40% of the total manufacturing cost of these packages. To alleviate test costs, various solutions relying on Built-In-Self-Test (BIST) of embedded high-speed components of SiPs need to be developed.

This project carried out in cooperation with Philips (Caen, France) aims at the development of new approaches for the test of RF components, in particular those based on acoustic wave propagation. Typical functional RF tests, as the measurement of the S parameters or of the noise figure, can be applied in a rather standardized way to these components but do not allow a simple screen test between good and bad devices. Functional RF tests are also not matched with the study of the various failure mechanisms. Our research goal is to develop methods that will solve the problem of testing RF MEMS devices embedded in SiP components.

2-3.2.5 A MUT-based pulse-echo system

Members: C. Domingues, L. Rufer, S. Mir, J. Jaros

In this project we develop a Micromachined Ultrasound Transducer (MUT) for pulse-echo applications as distance measurement or presence detection. Different principles of electroacoustic transducers can be used to produce or detect the ultrasonic signal. We have chosen the electrothermal conversion for signal generation and piezoresistive effect for sensing. This solution was adopted mainly for its relative design simplicity, CMOS compatibility and easy micromachining post process. The device consists of the MEMS part and the associated electronics. The employment of only one element in the MEMS dynamic structure simplifies the design considerations in terms of mechanical stability and membrane damping as well as the fabrication process. The device was fabricated in a 0.8 µm CMOS technology. This process is combined with a back-side bulk micromachining of the silicon wafer with SiO₂ etch-stop to free up the membrane. This design is fully integrated and CMOS compatible. There are two phases of the device operation - emission and reception. Figure 2-3.12(a) shows the overall architecture of the microsystem, including the mixed-signal interfacing electronics, the MEMS part and the medium acoustic propagation. Figure 2-3.12(b) shows a simulated complete cycle of emission/reception for an object placed at 10 cm from the device.

During emission, the electro-thermo-mechanically excited membrane generates an acoustic pulse at 40 kHz. The echo of this pulse is measured during the reception phase by piezoresistive gauges. During emission, the MEMS device is placed in an oscillator loop. A voltage \( V_i \) at the MEMS electrical input results in a current through the heating resistors that heats up the membrane by Joule effect. The displacement of the membrane results in the generation of mechanical stresses providing an electrical variation resistance of the piezoresistors. A Wheatstone bridge converts it in a voltage proportional to these stresses that is amplified by two differentiators and a differential amplifier, ensuring high gain and zero phase-shift. The differentiators placed at the MEMS output allow decoupling the DC offset of the MEMS caused by residual membrane stresses. The output of the differential amplifier, gained by drivers ensuring high current, is fed back to the heating resistors. The temperature on the membrane is measured by means of thermopiles. The average temperature increase is stored by the temperature control module. This temperature module ensures the same resonance frequency in both modes thus optimising the system sensibility.

Figure 2-3.12 (a) Overall microsystem architecture, and (b) simulation results of two pulse-echo cycles

During reception the reflected ultrasonic signal is measured. The membrane temperature is monitored to ensure the same temperature as during emission by forcing a DC current into the heating resistors. This
allows having the same values for the mechanical parameters in both phases, in particular for the membrane frequency that is slightly dependent on temperature (Young's modulus coefficient and thermal expansion coefficient temperature behaviour). The resonance frequency must be the same in both phases in order to maximise sensitivity. The differentiators are compensated during reception to avoid instability in the measuring chain.

Figure 2-3.13(a) illustrates the MEMS device composed by a square membrane made of silicon dioxide (SiO2) and silicon nitride (Si3N4) layers. Different thermal expansion coefficients of these layers result in the membrane deflection induced by a current passing through the heating resistors placed in the central part of the membrane. Four piezoresistors of polysilicon are integrated on the membrane sides, close to the edges where the mechanical stress caused by the membrane displacement is maximal. Two of them are oriented in parallel to the edge and the other two are perpendicular to edges. Finally, four thermopiles are placed diagonally from the corners of the membrane towards its centre. They serve the purpose of measuring the membrane temperature. Figure 2-3.13(b) shows the fabricated 0.8 µm CMOS chip. At the centre there is a membrane etched by a Deep Reactive Ion Etching (DRIE Bosch process) and the electronic part is around it. Some interferometer measurements results are presented in Figure 2-3.13(c) showing the 3D screen shot of the membrane surface. An important residual stress is seen after fabrication. A dynamic measurement showing the membrane deflection near resonance is shown in Figure 2-3.13(d).

![Figure 2-3.13](image)

Figure 2-3.13 MUT-based pulse-echo system: structure of the MEMS device (a), fabricated chip in a 0.8 µm CMOS technology combined with DRIE micromachining (b), result of the interferometer measurement of the membrane surface (c), membrane deflection at resonance (d)

2-3.2.6 Micromachined capacitive devices

Members: L. Rufer, M. Wong*, W. Ma*, F. Koukoui

(*Hong-Kong University of Science and Technology)

The activity in the field of the design and validation of capacitive micromachined electroacoustic and electromechanical transducers is developed in collaboration with the Hong Kong University of Science and Technology (HKUST). Two topics are studied in this project. Firstly, the capacitive microphone is developed as a device with specific features allowing its test. The second topic is devoted to the design and implementation of an integrated floating-gate electrostatic power generator.

2-3.2.6.1 Capacitive micromachined microphone

Capacitive (electrostatic) transducers consist basically of two plate electrodes separated by a dielectric. One of these electrodes (backplate) is fixed and the other one (membrane) is used for acoustic signal sensing. This transducer arrangement requires a source of polarization voltage that can be replaced by deposition of
electret material on one of the transducer plates. The use of silicon micromachining in the transducer fabrication process gives a number of advantages, including the transducer small size, high precision and low cost. Another advantage consists in the possibility of integrating such a transducer altogether with electronic circuits on the same chip.

A microphone is one of the applications of a capacitive micromachined transducer aiming at the low frequency domain. Microphones as acoustic sensors are widely used in the consumer electronics such as telephones, portable computers and hearing aids. The electrostatic transduction principle is the most convenient for realization with micromachining techniques due to high sensitivity and the compatibility with the CMOS process. A version of a capacitive micromachined microphone with free-floating diaphragm with no residual stress, currently under the development in collaboration with the HKUST, is shown in Figure 2-3.14.

![Figure 2-3.14 Layout of a microphone structure](image)

A theoretical study of this type of microphone based on the detailed behavioral model has been undertaken, showing the potential of this device to provide good characteristics in the audio frequency range. Moreover, the device is designed with testing concerns. One part of the split backplate electrode will serve as the membrane actuator used for testing.

2-3.2.6.2 Capacitive micromachined power micro-generator

Vibration-to-electricity conversion offers the potential for autonomous systems to be self-sustaining in many environments. Recent advances in MEMS technology enable the creation of a self-powered system with a MEMS device acting as an electromechanical transducer. An electrostatic effect was shown as a promising solution. The most significant advantage is its potential for integration with microelectronics. The solution of an integrated floating gate electrostatic power micro-generator that was developed at HKUST is shown in Figure 2-3.15(a) and (b).

![Figure 2-3.15 Layout of a power micro-generator](image)

The complete model of the system based on the state equations describing its dynamic behavior is shown in Figure 2-3.15(c). This model describes a nonlinear behavior of both electrical and mechanical parts of the system.

A linear equivalent circuit network based on an electro-mechanical analogy was also built. Both models show the consistency in the small-signal regime. Power generation up to 1 µW is predicted, at a driving frequency around 4 kHz and assuming an input displacement of 5 µm.
Figure 2-3.15 Capacitive micromachined power micro-generator: (a) schematic diagrams of a 2x2 array with a magnified view of the resonator over the fixed floating-gate of the generator, (b) secondary-electron micrograph of a 5x4 array generator, and (c) dynamic model of the power generator built with SIMULINK
2-4 System Level Synthesis (SLS)

Group Leader: A. A. Jerraya
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2-4.1 Long Term Trends for Embedded System Design: Multiprocessor SoC

An embedded computing system is an application specific electronic subsystem used in a larger entity such as an appliance, an instrument or a vehicle. The embedded system may embody the complete system functionality in several different ways—using software running on CPUs or in specialized hardware accelerators. The evolution of technologies is enabling the integration of complex platforms in a single chip; called System-on-Chip, SoC. Modern SoC may include one or several CPU subsystems to execute software and sophisticated interconnect in addition to specific hardware subsystems. Additionally non digital hardware, e.g. analog, RF and micromechanical parts, may be included in the same chip or package.

Mastering the design of these embedded systems is a challenge for both system and semiconductor houses that used to apply only software strategy or only hardware strategy. In order to meet performances requirements, these two parts need to be jointly designed. This requires a new kind of modeling strategies to allow for concurrent hardware and software design.

2-4.1.1 The trends: Programmable design

90% of new ASICs already include a CPU in 130nm technology. Multimedia platforms (e.g. Nomadik and Nexperia) are already multi-processor system on chip (SoC) using different kinds of programmable processors (e.g. DSPs and microcontrollers). Heterogeneous cores are exploited to meet the tight performance and cost constraints. This trend of building heterogeneous multi-processor SoC will be even accelerated. SoCs will be composed of multiple, possibly highly parallel processors for applications such as mobile terminals, set top boxes, game processors, video processors, and network processors. Moreover, these chips will contain very sophisticated communication networks called networks-on-chips (NoC). So the

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\(^2\) Visitor
design of a SoC will consist of an assembly of processors executing tasks concurrently. As a result, design methodologies must change their focus to selecting and using processors—either programmable or dedicated—as basic components rather than the logic modules, such as gates and ALUs, used by the current methods. It is easy to imagine that the design of a SoC with more than a hundred processors will become a current practice in few years, e.g., with 65nm technology in 2007. Compared with conventional ASIC design, such a multi-processor SoC is a fundamental change in chip design.

2-4.1.2 High-end design remains application-specific

With a particular application space, after a few generations of application design, it is possible to build a platform that can be effectively used as the basis for many products within that space. This is the case of TI-OMAP and Nomadik for mobile terminals and Nexperia for digital TV. New high-end applications push towards new architectures and application-specific solutions.

High-definition video recording illustrates the need for application-specific design. High definition video compression requires 32 TIPS (Tera Instruction Per Second) in computation power. Assume that a pure software approach is used with a SoC platform consisting of programmable processors. In this case, to meet the computation requirement, 32,000 RISC processors running at 1GHz are needed on the SoC platform. Currently and in the near future, such a SoC platform may not be realisable in terms of chip area and, especially, power consumption. In terms of power consumption, such a platform has a significant limitation since it requires a large number of transistors and the leakage current that will be dominating more and more is proportional to the number of devices. When designed as an application-specific solution the same video encoder can be implemented using only a four-processor solution in the case of the digital cinema application. This is made possible thanks to the adaptation of the architecture to encoding algorithms.

2-4.1.3 Higher level design approaches require HW-SW interfaces abstraction

Current ASIC design approaches are hard to scale to such a highly parallel multi-processor SoC. Designing these new systems by means of classical methods gives unacceptable realization costs and delays. This is mainly because different teams contributing to SoC design used to work separately. Traditional ASIC designers have a hardware-centric view of the system design problem. Similarly, software designers have a software-centric view. System-on-chip designs require the creation and use of radical new design methodologies because some of the key problems in SoC design lie at the boundary between hardware and software.

As shown in Figure 2-4.1.a, an SoC may include specific HW subsystems and one or several CPU subsystems to execute software. Some sort of hardware adaptor—a bridge or a communication co-processor—is generally required to connect CPU subsystems to the other subsystems. The CPU subsystem itself includes an RTL or a gate model of the CPU and a set of peripherals connected using the bus of the CPU. In the final design, the software is compiled and represented as a binary code that can be loaded in the memory of the CPU subsystem. Current SoC design process uses 2 separate teams working in a serial methodology to achieve HW and SW designs.

In order to allow for concurrent HW/SW design, we need abstract models of both software and hardware components (Figure 2-4.1.b). The HW/SW interface needs to handle two different interfaces: one on the...
software side using API and one on the hardware side using wires. This heterogeneity makes HW/SW interface abstraction very difficult because any abstraction of HW/SW interfaces requires the hiding of the CPU.

In general-purpose computer design, system designers must also consider both hardware and software, but the two are generally more loosely coupled than in SoC design. As a result, general-purpose computer systems generally model HW/SW interfaces twice. HW designers use a HW/SW interface model to test their hardware design, and software designers use a HW/SW interface model to validate the functionality of their software. Using two separate models induces a discontinuity between hardware and software. The result is not only a waste of design time but less efficient, lower-quality hardware and software. This overhead in cost and loss in efficiency are not acceptable for SoC design. A single HW/SW interface needs to be shared between both hardware and software designers. We believe that an additional type of designer, i.e. HW/SW system designer, is required to connect hardware and software design teams in an efficient way.

2-4.2 Breakthroughs: Concurrent Hardware/Software design flow based on a unified HW/SW interface model

2-4.2.1 Unified Hardware/Software Interface Model

HW/SW interfaces can be abstracted using different abstraction levels. Of course, the complexity of the codesign process will depend on the level at which the design starts. Existing literature and ongoing research work have identified clearly five abstraction levels that will constitute the key milestones for future research towards HW/SW codesign automation.

a) All explicit HW/SW interfaces: This is the currently used model for SoC design. Within this model, HW is described as RTL modules. The CPU acts as the HW/SW interface and the software is detailed down to assembly code or low level C programs using an explicit memory and I/O architectures.

b) Abstract data transfer HW/SW interfaces model: At this level, the CPU is abstracted. HW and SW modules interact through exchanging transaction transported by explicit interconnect structure. This model is generally called Transaction Level Modeling (TLM). Several TLM languages exist, the most popular are those developed using SystemC. Refining a TLM model down to RTL requires the refinement of the interfaces for different HW modules and the design of a CPU subsystem for each SW subsystem.

c) Abstract synchronization HW/SW interfaces model: At this level, the interconnect and synchronization are abstracted. The HW and SW modules interact by exchanging data following well defined communication protocols. MPI is an example model that is to abstract synchronization and interconnect when specifying HW/SW interfaces. Refining an abstract synchronization HW/SW interfaces model requires first to design the interconnect (bus or network-on-chip) and fix the synchronization schemes. This will also need to refine the data transfer down to RTL.

d) Abstract HW/SW communication: At this level, the communication protocol is abstracted. The HW and SW modules interact by exchanging abstract data without assumption on the protocol used, the synchronization and the interconnect that will be implemented. SDL is a typical model to abstract communication. Refining an SDL model requires first to select a communication protocol, e.g. message passing or a shared memory and then go through all the refinement steps listed above.

e) Abstract HW/SW partitioning: The ultimate abstraction level is the functional model where HW and SW partitioning is not decided. Wide variety of models may be used to abstract HW/SW partitioning. This may range from sequential programming languages such as C/C++, concurrent languages, and higher level models such as algebraic notation, e.g. the B. language. Refining such a model requires first to fix which function needs to be software and which function needs to be hardware and perform all the refinements listed above.
Figure 2-4.2  HW/SW interfaces abstraction levels and codesign steps

So far SW design focused mainly on levels (b) to (e) and HW design tried to move the design to a higher level than (a). Of course, the ultimate goal would be to handle both HW and SW at all abstraction levels. A full HW/SW codesign scheme is detailed in Figure 2-4.2. Traditional HW/SW codesign research concentrated on HW/SW partitioning, but without solving the problem of abstracting the hardware platform. Rather than using ad-hoc models of hardware as has been done with traditional co-design, system-on-chip designs demand a well-thought-out approach to the hardware/software interface. The next step in automation is the synthesis of data transfer, then synchronization and interconnect, then synthesis of communication and finally HW/SW partitioning.

2-4.2.2 Concurrent Hardware/Software Design Approaches to SoC

Figure 2-4.3 shows a simplified flow of mixed hardware/software design, where both software and hardware are designed concurrently. This scheme opens the design process to several new optimizations that were not possible when using the classical separate HW and SW design scheme. The most obvious optimization is a better adaptation of the CPU to both HW and SW interfaces. For example, new flexible processor technologies such as Tensilica can be used to optimize performances of the HW/SW interfaces by introducing application-specific I/O operation. Another example may be the use of the capabilities of reconfigurable hardware, such as the Xilinx Virtex II Pro, to optimize hardware interfaces to an embedded CPU.
2-4.3 Key Results: ROSES a Component-based approach for Hardware/Software Integration

ROSES is a system-level methodology for multiprocessor SoC design starting from a virtual architecture and using a communication refinement approach. The system is described as a virtual architecture made of a set of virtual components interconnected via communication channels. A virtual component consists of a wrapper and a component (or module). The component corresponds to software tasks or a hardware function. The wrapper adapts accesses from the component to the channels connected to the virtual component. The component and the channel(s) can be different in terms of: (1) communication protocol, (2) abstraction level, and (3) specification language. Depending on the difference, the functionality/structure of the wrapper is determined and automatically generated.

The design flow starts with a virtual architecture model that captures the global organization of the system into modules and architecture configuration parameters (as indicated in Figure 2-4.4.a) with abstract HW/SW interfaces. This input model may be manually coded or may be generated automatically by specification analysis tools.

The goal is to produce a synthesizable RTL model of the MPSoC that is composed of processor cores, IP cores, the communication network IP, and HW/SW wrappers. The wrappers are automatically generated from the interfaces of virtual components (as indicated by the arrows and dark grayed boxes in Figure 2-4.4.a. Software written for the virtual architecture specification runs without modification on the implementation because the same APIs are provided by the generated custom OSs.
ROSES is composed of a set of tools and a unified representation called COLIF:

- COLIF is a design representation based on XML. It acts as a metamodel for describing system hierarchy and abstract HW/SW interface at different design levels. All tools in ROSES operate on COLIF models.
- ASOG is a software targeting tool allowing to adapt high level software model to an execution platform. ASOG has been used for the generation of application specific OS and for the refinement of high level test vector programs.
- ASAG is a hardware interface generator tool allowing to adapt two hardware modules using different interface structures and communication protocols. ASAG is used for generating CPU subsystems and HW adaptation layers for SoC.
- COSIMIX is a functional interface generator tool allowing to produce an executable model for heterogeneous systems. COSIMIX is used to produce cosimulation model at different abstraction levels.

2-4.4 Exploratory research: PhD topics

1. Paviot Yannick, “Communication services partitioning for automatic generation of hardware software interfaces”
2. Sasongko Arif, “Prototyping based on reconfigurable platform for verification of system-on-chip”
3. Dziri Anouar, “Design tools and hardware/software components integration models for heterogeneous embedded systems design”
4. Blampey Alexandre, “Rapid prototyping methods using multiple emulation platforms”
5. Grasset Arnaud, “Automatic hardware interfaces generation using a services based specification”
6. Fiandino Maxime, “Definition of a new approach for the integration of a 1000+ heterogeneous processor network on a chip”
7. Senouci Benaoumeur, “Automating the targeting of complex HW/SW model on reconfigurable prototyping platform”
8. Bouchhima Aimen, “Multilevel modeling of HW/SW interfaces for MPSoC architecture exploration”
9. Hunsinger Frédéric, Automatic high level test program generation for SoC including CPUs”
10. Oyamada Marcio, “Simulation-Based Software Performance Estimation in MPSoC design”
11. Petkov Ivan, “Physical Design of MPSoC: Link between simulation and realization”
13. Kriaa Lobna, “Execution model for heterogeneous systems”
14. Youssef Wassim, “HW/SW interface design and exploration for highly parallel SoC based on high level parallel programming model and high level performance estimation”
15. Atat Youssef, “MPSoC design methodology from Simulink”
16. Cho Youngchul, “Scheduling tasks and communications for MPSoC with NoC”
17. Lemaire Romain, “Network-on-Chip (NoC) architecture for telecommunication applications”
18. Han Sang Il, “Automated design of flexible memory server for highly parallel MPSoC”
19. Pieralisi Lorenzo, “SoC challenges ahead: Networks on Silicon”
2-5  Verification and modeling of Digital Systems (VDS)

Group Leader: D. BORRIONE  
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Topics:
Specification Languages, Symbolic Simulation, Formal Verification, Proof of Correctness, Theorem Proving, Model Checking, Verification Flow

2-5.1  Multi-paradigm formal verification from standard simulation languages

Members: G. Al Sammane, D. Borronoe, P. Ostier, D. Toma

In the context of the design of systems on a chip, the need for rigorous design and verification methods that guarantee freedom from design errors is now well recognized. Too often, "formal verification" is understood as Boolean level equivalence and property verification, where efficient commercial software is now available. The VDS group focuses on verification techniques that can be plugged in the design flow from the very early specification and first design description levels, before bit accurate design is reached. More precisely, the objective is to develop mathematical models and verification techniques that can establish the essential properties of a system specification, prove the correctness of a design, and provide automatic diagnosis when design errors have been exhibited. Many aspects of a chip behavior have to be considered, and no single verification paradigm can apply to all of them. So we consider value simulation and symbolic simulation as the first method to gain initial confidence in the design, at all levels of abstraction; equivalence checkers at logic level, as well as general purpose theorem proving for the proof of correctness; symbolic model checking as well as theorem proving for the proof of properties.

Figure 2-5.1 gives our vision of a multi-HDL, multi-tool formal verification environment. Depending on the task, the type of circuit, and the initial specification level, the first formalized specification of the design is expressed in one among many possible languages: algorithmic programming languages for mixed hardware/software systems (e.g. C++ or SystemC), mathematical or data-flow languages for hardware DSP operators, concurrent processes for asynchronous designs (e.g. CCS, CHP), specialized property and temporal logic specifications (e.g. PSL), or standard HDL's for clock-synchronized RTL hardware (e.g. Verilog, VHDL). Complementary to the usual simulation of test cases, formal methods can be called to validate initial specifications, or prove the correctness of a design step.

The research of the VDS group aims at providing effective specification methods, description guidelines, semantic definitions, and proof strategies, to ease the use of new verification techniques. In particular, we define and implement the necessary automatic translators from conventional design languages to the input format of formal and semi-formal verification tools. Moreover, we stress the fact that no single verification paradigm will be sufficient to solve the problems posed by big designs, and a recent aspect of our work is the cooperation of several tools and techniques to perform a particular verification or validation task.
The following paragraphs focus on particular combinations of description formalisms, verification objectives and tools, applied to particular classes of digital designs.

2-5.2 Validation of high level specifications by theorem proving: application to on-chip communications

Members: J. Schmaltz, D. Borrione

The design of a system on a chip involves several processor-like modules, and several memories and peripherals. The initial phase when concepts are first written down, and which involves critical decisions on the number of units, their communication, the main pipelines, memory size and global system performances, is only supported by simulation tools taking as input relatively ad hoc formalisms. It is far from obvious that the RTL implementation is ever checked compliant with the description model produced at the concept phase. Yet, as systems reuse preexisting processor and memory cores, which have been verified intensively in isolation, an essential aspect of an overall system functional correctness relies on the correctness of their communications. In this context, our work focuses on the specification of the communications on a chip at a high-level of abstraction, and involving generic network components where the number of interconnected modules is finite, but possibly not fixed. Our goal is to prove that a token travels correctly, and arrives to its destination on a parameterized communication structure. At this level, automatic equivalence checkers and model checkers, suitable for fixed structures, are no longer applicable. The reasoning capabilities of theorem provers are needed.

We use the ACL2 theorem proving system to establish the correctness of formal functional specifications, particularly for parameterized communication systems. The ACL2 model, being written in LISP, is both executable and provable in logic. Our approach starts with specification documents written with the traditional mixture of English sentences, drawings and timing diagrams. We first manually construct a formal model for each generic component and prove each one correct. Then we model their interconnections and prove the communications function correct. Finally, we obtain a correct formal model of a complex structure. We have built a specification and functional verification methodology for the very first design steps of
parameterized communication virtual modules. Our formalism is pictured on Figure 2-5.2. We consider master/slave communications. Masters initiate communications by sending orders to slaves. As computations and communications are orthogonal, they are separated in two different components: applications (in yellow) and interfaces (in green). The interfaces encapsulate orders and results in requests and responses which are compatible with the communication architecture protocol. These encapsulations are performed by the four functions of the interfaces. Each interface is represented by two functions which are independent from one another. But, the functions of the master interface may differ from the functions of the slave interface. The model is complemented by the function CommArch which represents the communication medium and the function Slave which represents a generic slave application.

Transfers are represented by compositions of functions. A complete transfer from a master to a slave and the reception of the corresponding result is modeled by the following composition:

\[
Transfer(ord) = MI_{res} \circ SI_{resp} \circ Slave \circ SI_{ord} \circ CommArch \circ MI_{req}(ord)
\]  

(Equation 1)

The communications are correct if the result received by the master is equal to the application of the function Slave to the initial order. Formally, this is expressed by the following theorem:

\[
\forall ord, \ Transfer(ord) = Slave \ (ord) \quad (Theorem \ 2)
\]

We have applied this methodology to the Octagon, a state-of-the-art network on chip developed by STMicroelectronics. As shown on Figure 2-5.3, an Octagon interconnects eight nodes with twelve bidirectional links. In fact, Octagon is a special case of a generic structure containing an arbitrary number of nodes, provided it is a multiple of 4. A node of the network is a small system around a local bus, inspired by the AHB AMBA bus, containing: an address decoder, a memory unit, a slave and a master interface (see Figure 2-5.4). The Octagon specification is built around three main functions: Route models a parameterized routing algorithm, Schedule models the scheduling of messages over the network and Trip (i.e. CommArch) represents the physical interconnection structure.

To prove Theorem 2 above for every pending order in the Octagon, we prove that (a) function Trip does not modify messages; (b) function Route produces routes consistent with the network topology between the correct source and destination nodes; (c) function Schedule satisfies the scheduling policy of the protocol. These properties allow every transfer on the Octagon to be reduced to the application of the function Transfer (1) above after removing the function calls. Then, to prove Theorem 2, we prove that the composition of the interfaces yields the identity function.
2-5.3 Verification of high-level descriptions by combining theorem proving and symbolic simulation

Members: G. Al Sammane, D. Toma, P. Ostier, J. Schmaltz, D. Borrione

2-5.3.1 The Combined verification tool: TheoSim

TheoSim is a prototype assertion based verification system that bridges the gap between informal and formal validation techniques, by combining simulation and theorem proving in the same framework, and providing automatic translators from conventional design languages (currently VHDL). Thus, TheoSim can easily be inserted in the design and validation flow.

TheoSim is implemented on top of two robust and powerful systems: Mathematica, well established in technical computing, has also been used for the symbolic specification of discrete systems; ACL2, a general purpose theorem prover, has successfully been used for digital systems verification. Both Mathematica and ACL2 rely on functional programming.

TheoSim is based on Constrained Symbolic Simulation developed in our group. It provides a VHDL compiler, an event driven symbolic simulator written in Mathematica and the automatic generation of functional formalizations and theorems submitted to the ACL2 theorem prover. The architecture of TheoSim is given in Figure 2-5.5.

One of the advantages of TheoSim is the fact that it uses the same concept for test cases as classical simulation. In effect, the symbolic computation engine incorporated in TheoSim is more general. Two modes for the execution of the design over test cases are distinguished: the tracking mode and the reasoning mode. Any combination of these is supported.

TheoSim offers a partial solution at an abstraction level where the current automatic property checkers are not applicable. Here, verification experts may accept technologies that are not fully automatic in order to overcome automatic tools limitations. In that case TheoSim can assist experts in the navigation of the design and in quickly locating interesting proof regions.

2-5.3.2 Verification of a network on chip design using TheoSim

We have written a VHDL implementation model for the Octagon network on chip. A request is generated at a source Octagon node to be sent to a destination Octagon node. It contains a symbolic packet, the data that must be transferred, and its destination address. The amount of details provided in the VHDL implementation is much greater than in the LISP specification: data types, timing, and synchronization were left abstract in the initial model, and are now fully described. It is thus not possible to show a direct functional equivalence between the two models. Rather, we must show that the VHDL design correctly implements the specification, i.e. provides a result that can be interpreted as the result of the specification function after the computation time has elapsed (counted in clock cycles).

A tool capable of accumulating the computation over several clock cycles is thus needed. To this aim, we have used TheoSim.

Using the tracking mode: In the tracking mode, we make use of already defined numerical simulation test cases provided by designers. One assigns numerical values to the source and destination nodes identifiers, but the data carried over the network is a symbol. The TheoSim simulation tracks this symbolic packet and the designer can check the correctness of each traveling step.
Example. Assume one assigns value 0 to the source node and 2 to the destination node. At the end of the one simulation cycle the packet reaches node 1. Then, the packet reaches node 2, which ends the test case. It is easy to check manually that every step is correct.

In the tracking mode, a designer detects if a message does not reach its final destination. So, this mode is similar to a network debugging system. This mode is more sensitive to CPU resources than memory; no state explosion is possible since only the data part is symbolic.

Using the reasoning mode: In the reasoning mode, we can be more abstract: the source and the destination nodes can both be symbols that may stand for any address between 0 and 7. By symmetry of Octagon, all combinations of source and destination node pairs are equivalent to those taking 0 as source number, modulo an index rotation. Moreover, there is no need to simulate all possible communications in the Octagon structure: for any source node number, two connections remain unused. Figure 2-5.6 shows all the longest paths starting at node 0. Thus, only three routers are observed during simulation in this mode. After the necessary number of simulation cycles, the response of a request is a normalized conditional expression depending on different addresses in the network.

We prove that the packet is delivered to its destination by case analysis in ACL2. The proof is performed on (i = 0), and generalized to all nodes by symmetry.

2-5.4 Symbolic Simulation of RTL designs

Members: G. Al Sammane, D. Toma, D. Borrione

2-5.4.1 Extending the cycle-based symbolic simulator implemented in a Computer Algebra System

Between formal methods and cycle-based simulation, symbolic simulation is a semi-formal technique that is gaining popularity for the verification of digital electronic circuits. Instead of simulating a design with numerical values, symbolic inputs are given to the simulator, which produces an algebraic expression for the memory and output variables, as a function of the initial state and of the inputs.

We have used the computer algebra system "Mathematica" to implement a cycle-based symbolic simulator for a subset of the VHDL language. It uses the Mathematica symbolic computation engine, and algebraic terms are simplified on the fly; the manipulation of huge terms can thus be avoided.

In order to support the 2004 synthesis VHDL standard, the functional Mathematica model of VHDL (the M-code defined in 2002-2003) has been radically changed. The model contains transition functions that compute the next value of each signal and variable in the design using normalized if-then-else expressions. A translator from our existing intermediate format LIF to our new model has been implemented.

With this new model, the approach is suitable for the multi-paradigms verification of behavioral descriptions: theorem proving, SAT-solving and Pattern-Matching.

2-5.4.2 Application to the Verification of generic RAM using Pattern-Matching

The simulation results of the Mathematica symbolic simulator are often complex nested if-then-else expressions: it computes all possible values of the design object for all possible execution paths. Naturally, visual examination of these long expressions is impossible, and reasoning tools must be invoked to exploit such results.
A pattern is a written formula that can stand for any expression. When we write $f[x_\_]$, $x_\_$ stands for any symbolic expression. For example, $x_\_^n$ may stand for $(a+b)^n$, $(a+b+c)^n$ and for $(a-b)^n$. With the use of patterns, we can define complex forms that stand for a class of symbolic expressions. An abstract form can be built using these patterns, standing for a class of symbolic expressions. In fact, Mathematica offers helpful pattern matching capabilities that we have adopted for verification purposes.

Using the above concept of forms, the designer can specify the property to be verified as a matching between the abstract form and the symbolic expressions after the simulation. Pattern matching in Mathematica is then used to reduce these properties to True or False. Until now, we have implemented the following pattern matching constructors:

$\text{SameQ}[x, y]$: this function gives True if the exact correspondence between $x$ and $y$ is matched, and gives False otherwise. Example: $\text{SameQ}[a+b, a+c]$ gives False and $\text{SameQ}[a+b, a+b]$ gives True.

$\text{MatchQ}[\text{expr}, \text{form}]$ is the main pattern matching function: it gives True if the expression $\text{expr}$ matches $\text{form}$, False otherwise. Example: $\text{MatchQ}[(a+b)^n, x_\_^n]$ gives True and $\text{MatchQ}[\text{if}e[a, b, x^\_], x_\_^n]$ gives False.

$\text{PathQ}[\text{obj}, \text{form}]$: gives True if an element in the execution tree of an output $\text{obj}$ matches $\text{form}$, gives False otherwise. Example: assume the execution tree of an output $\text{sig}$ is the if-then-else expression $\text{ife}[\text{Event}[\text{clock}], x', 0]$. In this case $\text{PathQ}[\text{sig}, x_\_^n]$ gives True.

$\text{FreeQ}[\text{obj}, \text{form}]$: gives True if no element of the execution tree of $\text{obj}$ matches $\text{form}$, gives False otherwise.

The verification of a generic description of an industrial circuit SPSMALL has been performed using the pattern-matching algorithm.

**Property Verification**

Behavior VHDL Model

High Level

Equivalence Checking

Refinement

VHDL Model

Abstraction Tools

RTL

Low Level

Net-list Model

**Figure 2-5.7 Verification of SPSMALL**

**Figure 2-5.7** gives the overall verification approach. The design of the memory is written as a transistor net-list. It is a legacy design that was initiated on a previous technology, and then transferred to a newer one. A RTL level design is produced from this transistor net list, through a transistor abstraction; in this case, the TLL tool by Transeda was used to compute the logical gates and the memory points (latches and flip-flops) directly from the transistor net list.

The behavioral model of SPSMALL is a synthesizable VHDL description that is written by hand. It is intended for use as an IP by SoC architects, and is provided as a generic model of parameterized size.
Our approach is a two-step verification process:

- First we verify the correctness of the behavioral level, by checking essential properties using Pattern-Matching. With the use of symbolic techniques, the coverage is 100%.

- Then, the behavioral description is checked against the abstracted net-list, for a fixed size, by equivalence checking. This ensures formally that two description levels for the same design are equivalent. This step guarantees that the properties that hold on the high level are preserved in the abstracted RTL.

2-5.5 Formal proof of correctness of safety-critical IP's using theorem proving

Members: D. Toma, D. Borrione

Ensuring the correctness of circuits for safety-critical applications requires a rigorous design flow. Further to the numeric simulation of test cases, that provides initial confidence in the design, formal methods are subsequently invoked, to validate initial specifications, or prove the correctness of a design step. Here again, the Boolean level techniques (BDDs, SAT) are not applicable at the initial phases of a project, where the specification is expressed with arithmetic operations and high-level algorithms. Yet, it is essential to establish:

- the functional validity of the specification and of the initial implementation choices, before investing extensively at more detailed levels;
- that the manually derived synthesizable RTL correctly implements the specification.

Both needs are successfully addressed with mechanized theorem provers, whose reasoning capabilities, in particular induction, free the proof argument from the data size complexity. The ACL2 system reuses libraries of pre-verified function definitions and theorems, is highly automatic and efficient.

The traditional mixture of English sentences, drawings, timing diagrams, etc. forms the source for the functional specification. The credibility of the formal model we build for the specification relies on its efficient execution on numerical values, and that a reasoning engine can prove mathematical and safety properties on it. This validation step provides, as far as possible, a "correct" functional specification.

Figure 2-5.8 Using symbolic simulation to construct the state machine model of the circuit

The synthesizable RTL is assumed to be written in VHDL (the following applies to Verilog as well). To prove that the RTL correctly implements the specification, no simple equivalence exists, as encoding details and timing information have enriched the model. We translate the RTL design into a functional format (Figure 2-5.8), simulate the model symbolically for one clock cycle, actually corresponding to several VHDL simulation cycles, and extract the Moore machine, i.e. the transition function for each output and state variable of the design. The functions are automatically translated into Lisp. This cycle accurate model is proved compliant to the Lisp specification, which has no timing information, using ACL2.

We applied this method to the design of a cryptographic component implementing SHA-1. This study was part of a secure smart card reader project, developed in cooperation with several industrial partners. The SHA-1 is a standardized hash function, which processes a message of size up to $2^{64}$ bits, and produces a 160 bit message digest, with the following property: any alteration to the initial input message will result, with a very high probability, in a different message digest. The applications of this algorithm include fast encryption, password storage and verification, computer virus detection, etc.
Figure 2-5.9 SHA-1 algorithm steps

The principle of the SHA-1 is shown on Figure 2-5.9. The input message \( M \), a bit sequence of arbitrary length \( L \), undergoes two preprocessing steps:

- **Padding**: \( M \) is concatenated by bit 1, followed by \( k \) bits 0, followed by the 64-bit binary representation of number \( L \). \( k \) is the least non-negative solution to the equation: \((L+1+k) \mod 512 = 448\). As a result, the padded message holds on a multiple of 512 bits.
- **Parsing**: The padded message is read in blocks of 512 bits. After reading each block, it must be decided if this is the last block or not.

The computation of the message digest is performed on the message blocks in order, considered a sequence of 32 bit words, as an eighty-iteration algorithm over five 32-bit words initialized with predefined constants, and the succession of message words.

From the standard, we wrote a general model (referred later as \( \text{sha}_\text{norm} \)) to capture the common principles of the four versions of the SHA algorithm: SHA-1, SHA-256, SHA-384 and SHA-512, which differ essentially in the sizes of the message blocks, word, and digest. We proved safety and mathematical properties on this model, using ACL2. This resulted in executable and reusable specifications for this previously informally written standard.

The SHA core was designed as a cycle accurate control machine and a data path, at the RTL level. Let \( \text{sha}_\text{vhdl} \) be the automatic translation of the VHDL description.

To prove that the VHDL is compliant to the functional specification, we show that for any arbitrary input message the execution of \( \text{sha}_\text{vhdl} \) for the appropriate control inputs and number of clock cycles (until the computation is done) returns the same message digest as the one returned by \( \text{sha}_\text{norm} \).

\( \text{sha}_\text{vhdl} \) needs 3 clock cycles to initialize the system; then it needs 342 clock cycles to compute the digest for one block. The 342 cycles are decomposed as: 16 for reading the first 16 words and computing 16 steps of digest, 320 to compute an intermediate digest, 3 to combine the results with the initial hash values of the block, 2 to store the message digest obtained so far. The last cycle returns to the digest computation for the next block, or to the idle state. So, in order to process \( nb \) blocks, the design needs \( 3 + (342 \times nb) \) clock cycles.

In contrast to simulation, we proceed with a stepwise approach, which proves by induction intermediate theorems for each main computation step of the overall \( \text{sha}_\text{vhdl} \). This approach can be reused for other control - data path combined designs. The reasoning engine considers the initial value of all memories and registers as arbitrary, and \( nb \) (the number of blocks) to be an unbounded (but finite) natural integer. The proof of correctness for an arbitrary message could be performed using theorem-proving techniques only.

A couple of errors were uncovered in the initial VHDL, the most serious being an excessive number of cycles in the digest computation. The use of an executable logic was key to the successful validation of both the specification and the RTL, as it provides an easy model debugging facility.

The generality of this method, and reusability of the specially developed library of functions and proved theorems in the ACL2 logic, are currently tested on other cryptographic components.
2-5.6 Verification of asynchronous circuits

Members: M. Boubekeur, D. Borrione

This work, in cooperation between our team and the CIS team of TIMA, is the finalization of a research that was started three years ago. It consists in the analysis and the automatic validation of asynchronous specifications written in CHP, prior to their synthesis. The goal of our work is to introduce formal methods into the asynchronous synthesis flow.

Two approaches were implemented and compared. In both cases, we verify safety properties such as freedom from deadlock or livelock, and temporal behavior.

- Translate the Petri Net interpretation of the CHP as a pseudo synchronous VHDL description, and use an industrial symbolic model checker to perform property checking on this RTL finite state machine. A pseudo clock is introduced to make the result of each computation cycle a visible state. The translation performs a static pre-order reduction, by replacing all independent event interleavings by data-flow concurrency. Due to the semantics of process communication by signals in VHDL, channels have to be synthesized prior to property verification. This approach gives good results on models where decisions on data encoding and communication protocols are taken.

- In order to introduce formal verification sooner, adapt formalisms and tools coming from the field of software validation. The CADP toolset from INRIA, whose execution model is similar to the asynchronous circuits one, was selected. CHP specifications are analyzed and translated in terms of LTS (labeled transitions systems) with guarded commands. These LTS descriptions explicitly integrate channels and simple “read” and “write” actions. They appear to be more appropriate for the formal validation of initial CHP specifications.

We performed performance comparisons on the two methods applied on identical asynchronous circuit examples. In both cases, safety properties can be proven on the specification, provided aggressive simplification strategies are applied.

2-5.6.1 A new environment for the validation of the asynchronous circuit specifications

Figure 2-5.10 shows the validation environment based on the enumerative approach, taking as input a CHP specification, to achieve the formal verification of logical and temporal properties. It includes several automatic techniques for model reduction and abstraction. These improvements allowed the verification of realistic case studies (an asynchronous four stage Filter and an asynchronous DES “Data Encryption Standard” chip).
2-5.6.2 Verification of mutual exclusion between the guards of deterministic choice structures

The CHP compiler does not check that the guards of deterministic choices (one of the control structures of CHP) are mutually exclusive. Yet such verification is of a great interest for the asynchronous circuits designer: when ascertained before the construction of the execution model, in a pre-verification phase, it eases the successive formal verification task.

As an early decision is critical to the efficiency, we propose a treatment in two phases:

- The first one is at a static level (Figure 2-5.11(a)). The idea is to extract all the guards from a deterministic choice operator, and locally check their mutual exclusion using a symbolic decision tool.

- The second phase happens during the formal verification step (Figure 2-5.11(b)). If the static analysis response is negative (the guards do not inherently satisfy mutual exclusion), then dynamic verification confirms that no bad case is provided by the overall model, or gives a counter-example. The idea is to test the non-determinism during the construction of the global execution model.

The results of this work constitute a solid base for an effective and powerful integration of formal methods in the asynchronous design flow “TAST”. Details are fully reported in the PhD dissertation of Menouer Boubekeur, defended in October 2004.

2-5.7 Generation of proven correct monitors for PSL properties

Members: D. Borrione, E. Gascard, M. Liu, K. Morin-Allory, P. Ostier

The aim of our current study is to define an algorithm to synthesize RTL monitors for PSL formulas. The final goal is to implement hardware monitors on the same chip as the circuit being developed. This will allow crucial and complex properties of the circuit to be checked during the normal circuit functioning. The proposed flow is described in Figure 2-5.12.

For the first prototype, we have identified a subset of the PSL language, the Foundation Language (FL), which is the so called "simple subset" of PSL excluding Sequential Extended Regular Expressions (SEREs). We recognize properties such that time advances forward when we evaluate the formula from left to right; and we limit all operators to Boolean expressions (rather than sequences of Boolean expressions). For that subset:

- We have written a library of basic synthesizable VHDL components that evaluate each temporal operator in its weak or strong version.
- We have defined an algorithm to translate PSL properties as interconnections of those basic components.

A prototype automatic translator for this PSL subset (restricted to the VHDL flavour of expressions) produces a structural VHDL description that observes the design signals named in the PSL property, and raises an output signal when the property is violated.

We compared the monitors generated with our tool with monitors generated by FoCs. FoCs is a tool of IBM that generates monitors from Sugar properties (Sugar was donated by IBM and it is the basis for PSL). In
the Foundation Language of PSL that we consider, most operators are common with Sugar. Contrary to our approach, which is structural, FoCs produces a behavioral description (VHDL process) that invokes an "assert" statement when the property is violated.

We formally verified with the RuleBase model checker of IBM that, for all common operators, our monitors and corresponding FoCs monitors behave identically.

On going work intends at providing the synthesis of properties written with SERE's, and at proving correct the library and the general synthesis algorithm.

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**Figure 2-5.12 Monitored verification flow**

- **PSL formula**
  - `psl2 vhdl`
- **RTL VHDL monitor**
- **RTL VHDL monitored circuit**
  - `synthesis flow`
  - `gate netlist`
2-6 Qualification of circuits (QLF)

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<tr>
<th>Research areas</th>
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| - Methodology and tools for the test under radiation of ICs;  
- Study of the effects of atmospheric neutrons on commercial integrated circuits;  
- Design of experiments on board satellites;  
- Methods and tools for fault injection;  
- HW and SW techniques for hardening digital architectures and embedded systems;  
- Secure digital implementations;  
- Robust logic implementations based on single electron transistors;  
- Defect Tolerant Architectures targeting very high defect densities. | ALCATEL, ATMEL, BOSCH, CNES, ST Microelectronics, ACI-SI-Mars Project, ACI-SI-Venus Project | ARTISAN (USA), CEA/LETI, INTA (Spanish Space Agency), IROC (France), TRAD (France), GEMPLUS (France), NASA GFSC (Washington, USA), |

2-6.1 Summary
The QLF group has joined TIMA in 1996. Research activities of the group deal with the study of the behaviour in harsh environment for digital circuit and systems. The main stress considered is radiation of nuclear and space environments, but it is interesting to mention that particles reaching the Earth’s surface from the Sun, up to now innocuous for microelectronics circuits, have sufficient energy to flip bits in memories and corrupt logic inside processors for parts manufactured with less than 0.25 µm and supply voltages drop to less than 2.2 Volts. This can constitute a threat to avionics control systems (at 30,000 feet, the neutron activity is 4 to 8 times higher than the ground), and even to systems operating at sea level. Another related area is the new threat of secure systems, related to fault-based attacks. The activities of the QLF group concern both natural and intentional faults in integrated systems.

One of the important issues of these researches, is the prediction of error rates of a studied system (circuit, architecture, software,...). The refinement of forecasting error rate strategies needs both to perform ground test by means of simulated radiation environment (particle accelerators) and to compare ground test results to data obtained from experiments aboard of spacecrafts. Two different satellite experiments were developed in collaboration with CNES with the goal of studying the behaviour in space of various commercial circuits (COTS) including memories, general purpose microprocessors and dedicated processors. One of them deals with satellite image texture analysis by means of an Artificial Neural Network designed by CEA/DAM. This experiment is presently on board of a scientific satellite launched November 1997 by Naval Research Laboratories (NRL-Washington). The second one, designed in collaboration with CNES (French Space Agency) and NASA GFSC (Goddard Flight Space Center), aims at studying the sensitivity to transient errors provoked by SEUs of advanced FPGAs (Field Programmable Gate Arrays). The satellite carrying this experiment, presently at the end of development phase, will be launched in 2006 in the frame of NASA LWS/SET project (Living With a Star/Space Environment Testbed).
One of the critical effects of radiations can be drastically attenuated by a proper design of memory cells. A patent developed at QLF, the so-called HIT (Heavy Ion Tolerant) memory cell, has been transferred to Matra MHS, presently ATMEL, to manufacture a Digital Signal Processor, the TSC 21020, suitable for space applications. Ground tests performed on this circuit have proved its immunity to Single Event Upsets. A new industrial transfer under discussion concerns the THESIC (Testbed for Harsh Environment Studies on Integrated Circuits) test platform, which is a tool allowing to perform both radiation ground testing and fault injection on a large scope of integrated circuits, including memories, advanced processors and MEMs.

2-6.2 Study of the effects of atmospheric neutrons on the operation of submicronic integrated circuits

Members: F. Faure, P. Peronnard, R. Velazco

Ionization resulting from charged particles issued from the atomic reaction between neutrons reaching the earth’s atmosphere and atoms present in the substrate of CMOS circuits, may flip a memory cell content or provoke a transient pulse within a combinational circuit. This phenomenon constitutes a potential obstacle to the reliable operation of circuits manufactured from future deep submicronic processes.

A first step towards a thorough study of this problematic consists in putting in evidence the phenomenon through experimentation with suitable test vehicles and an appropriate neutron beam. In February 2000 was carried out one of the first experiments performed in France in this area. The THESIC tester was used to expose two circuits (1 Mega byte static memory manufactured with a 0.25 \( \mu \)m process and a digital signal processor with a huge internal memory) to high fluxes of neutrons using beams available at Institut Laué-Langevin (ILL, Grenoble). These experiments put in evidence the need for the use of hardening techniques (design hardened memory cells, error detecting and correcting codes,…) in future deep submicronic circuits. Indeed, the number of detected bit flips suggest that next generation of SoCs (Systems on a Chip) or high-capacity static memories may be the source of frequent errors even for systems operating at sea level. In Figure 2-6.1 is shown a photo of the experimental set-up used to perform neutron tests.

Current researches in this area are dealing with the design and exploitation of an experiment including a very large capacity SRAM memory, which will be exposed to the effects of natural atmospheric radiation at different sites, this to derive realistic error rates in real life environment of future submicronic components. Candidate SRAMs for this real life testing were evaluated using a fault simulation technique and dedicated tools (Giant 4). Obtaining real life versus accelerated test figures will help in giving trends for future technologies.
2-6.3 Development of a test bed suitable for the qualification of integrated circuits devoted to operate in harsh environment

Members: F. Faure, P. Peronnard, R. Velazco

With the miniaturization, integrated circuits become more and more sensitive to perturbations resulting from the effects of the environment (temperature, radiation, EMC,...). This activity concerns the design of a test system which facilitates the realization and exploitation of qualification tests for all kind of circuits, from a simple register bench to complex components such as processors.

Screening tests are mandatory to predict error rates. They consist in exposing the studied parts, eventually operating in vacuum, to simulated stress conditions. The hardware and software developments related with such tests must take into account the random nature of event occurrence, both in time and space. On one hand this entails on-line error detection, on the other hand this makes mandatory the need for development of ad hoc hardware mechanisms related with critical errors detection (sequencing loss, system crashes, latchups) and recovering. Most of commercially available functional testers have these capabilities, potentially offering a powerful solution to qualification test implementation for all circuit types. Nevertheless, two main drawbacks must be mentioned:

- functional testers cannot fit inside most of vacuum chambers available at generally used radiation facilities. The alternative consisting in using them outside the chamber connected to the device under test (DUT) inside the enclosure, may lead to serious signal propagation problems,

- test stimuli are defined by a set of binary patterns corresponding to circuit pins values at each clock period. For complex circuits (processors for instance) the development and debugging at this low-level of such test programs can be a difficult task. Note that these constraints may also apply for testing under other type of conditions such as temperature, magnetic perturbation, vibrations, or other type of harsh environments.

Since 1988 we have been collaborating with different European and American space agencies in projects aiming at the study of the behavior under radiation of circuits devoted to space applications. Our role was the development of the hardware and software aspects of the test under radiation of candidate circuits. Experiments were performed by means of a family of dedicated testers we designed and realized to cope with radiation testing requirements. The use of these testers for a wide range of circuits, including memories, general-purpose processors and dedicated processors, pointed out their capabilities for the qualification of complex digital ICs, but their adaptation to test a new device needs some hardware development, limited to the architecture of the Device Under Test (DUT) daughter-board. Even if such architectures are not too complex and follow quite close the basic principles of block diagrams exposed in the DUT’s datasheet, the experience proved us that their development needed specialized skills constituting thus the main obstacle to easily “export” our tester concept to other teams.

In the past we have prototyped different versions of a dedicated test system having the following characteristics:

- The DUT operates in its “natural” digital environment, i.e. it is interfaced to a typical architecture. When the DUT is a processor, such architecture includes memories to store the boot and test programs, glue logic and needed power and clock circuitry. Instead of test vectors that mimic the activity of input pins at each clock cycle, during the test stimuli is applied to the processor under study as the result of the execution of a program stored in a suitable memory. Test results are stored in the memory as a byte sequence.

- An external board provides the interface with the user and controls the operation of the architecture built around the DUT.

- The whole system (DUT board and control board) communicates through a serial link with a computer for user’s control of the experiment.

For the architecture of THESIC+ (Testbed for Harsh Environment Studies on Integrated Circuits), the last version of these functional testers, we have adopted the same principle, taking a particular care to meet the following requirements:

- The whole system must have a size allowing to entirely fit it in enclosures commonly used for environmental qualification tests.

- The DUT must be tested on-line, operating in nominal conditions.
The system should allow to exercise as many circuits (among candidates to a given project for instance) as possible, to avoid waste of time/money consequence of delays provoked by operating the facilities used to simulate the studied environment.

The THESIC+ system we developed allow coping with these requirements. It comprises mainly (Figure 2-6.2):

![Diagram of THESIC+ architecture](image)

**Figure 2-6.2** THESIC+ architecture

The efficiency of this tester’s architecture was proved by various cooperations with space agencies aiming at performing the test under radiation of processors candidate to their applications. As a significant example, it can be mentionned the use of THESIC by JPL/NASA ofr the study of the behaviour under heavy ions of the PPC750, a complex processor candidate to be included in the electronic equipments of a satellite. A collaboration with JAXA (Japanese Space Agency) based on the use of THESIC+ platform is in progress and aims at the evaluation of the sensitivity to radiation of a design hardened processor (based on the MIPS architecture) which is included in a space mission presently operational.

The last version of the THESIC test platform constitutes a powerful tool with generic capabilities for the qualification of digital circuits. The idea is to implement the whole DUT board architecture by means of an FPGA whose configuration is obtained from compiling the description of key features of the DUT in a hardware description language such as VHDL. In this way, there is only a minor hardware development, limited to wiring the DUT pins to the ones of the tester connector.

- **The control board**: this block is basically based on the previous THESIC motherboard with minor additions. It includes a micro-controller (Atmel 89C52) having in charge the following tasks: it controls the circuit to qualify, runs on and the test sequences and checks the current consumption to avoid latchups. It is also able to transfer test programs and to gather test results from the component being studied to/from the PC user interface (via serial link RS 232).

- **The interface board** represents the new feature we developed to improve the test-platform. It comprises an FPGA (Field Programmable Gate Array) and several memory banks: common memory (MMI) to share data between control board and the device under test (DUT), and EEPROM banks to enable fast and efficient processor tests. To cope with a wide range of DUTs, they are all managed by the FPGA. We have chosen for this device a FLEX10KE from Altera, which is multi-volt Input/Outputs compliant, that means it can drive signals in 5 or 3.3 or 2.5 Volts, reducing the number of components needed to interface the DUT. The FPGA must be properly configured in order to assign the interface board resources to the device under test. The high-level program code (in VHDL for instance) that interface Control Board with memories and DUTs, is downloaded from the PC into the FLEX (via the parallel port). As an example, this board is able to interface a processor with up to 64 bits data lines and 32 bits address lines.

- **The DUT board** (called “daughter-board” in the previous version of THESIC) comprises exclusively the component to test and, in some cases, clocks, latches and current regulators. The THESIC modes mentioned in [4] (the slave mode which consists in managing all the tests from the control board, and master mode in which the DUT is driven by a processor that is present on the daughter board) are still available in THESIC+. However in slave mode the 89C52 present on the control board will manage the DUT while the FPGA will just ensure the
correct assignment and the bi-directional exchanges of signals between them. Therefore, the master mode is slightly different in THESIC+: a suitable VHDL description (such as a simplified micro-controller) implemented in the FPGA, will enable it to drive the DUT. In both cases, the memory-mapped interface present in the interface board, still allows data sharing between control board and DUT.

- Obviously, a computer is also needed in THESIC+ as a user interface. It allows the on-line control of test operations, the display of results and their storage in a mass memory in convenient formats for future analysis.

When the circuit under test is a processor, errors perturbing test control operation may have consequences difficult to be predicted and/or understood through the analysis of test results. As an example, malfunctions leading to sequence loss may result in “black out” situations at the motherboard level (which keeps waiting for daughter-board interruption indicating either power consumption problems or “test results available”). To cope with such critical errors, a programmable software watchdog was implemented in the control-board.

A particular effort was invested on the development of a friendly and powerful user interface capable to provide the operator with on-line test result data.

Photo depicted in Fig. 2-6.3, shows the THESIC+ hardware installed in the experimental cave of radiation facility. The board shown in the background is fixed to a moving stage support allowing performing the alignment DUT-beam. It communicates to an external PC through a serial link connection. During a radiation test, targets DUTs are aligned with the beam.

THESIC+ has been successfully used to test a wide range of devices such as microcontrollers, DSPs, a SPARC processor as well as SRAM memories, FPGAs and Analog to Digital converters. It is presently used in the frame of a cooperation with CNES as the hardware platform for the definition of a methodology for the evaluation of the sensitivity to ionizing radiation of applications implemented by means of FPGAs.
2-6.4 A methodology based on fault injection for the prediction of architectures’ error rates

Members: F. Faure, P. Peronnard, R. Velazco

To predict the error rate provoked by radiation for an application executed by a given processor, we have investigated an approach allowing to characterize and to quantify the effects of Single Event Upsets (SEU) also called *bit flips* or *upsets*, on the operation of microprocessor-based digital architectures. The principle is to determine, from the results of fault injection experiments, the rate of “effective” bit flips for the tested programs, and thus to derive realistic figures for the expected error rate in the final application environment. Such experiments have lead to a well sound methodology for error-rate estimation, based on both a limited radiation testing (to evaluate the individual sensitivity to radiation of registers or memory words) and hardware/software fault injection to statistically evaluate the fraction of errors having consequences for the program execution.

The approach relies on the injection of errors affecting information stored in registers and memory locations, whose occurrence instant and location follow a suitable distribution. For a processor fault injection must be performed concurrently with the execution of a program and can be achieved at different levels (simulation, software level, hardware level). As an example, hardware level fault injection can be achieved with minimal “intrusiveness” using the interruption mechanism. The key idea is the generation and storage at an appropriate memory area, of a piece of code, called *CEU (Code Emulating an Upset)*, whose execution will provoke the content inversion of selected bits, called *CEU targets*. If the processor is properly configured, the CEU code execution can be triggered by the assertion of an interrupt-like signal. The interruption activation instant and the CEU target can be pseudo-randomly chosen by an ad-hoc external mechanism. In this way, errors can be injected in all accessible processor's CEU targets (internal registers and SRAM memory area) as well as in the external SRAM where program data and code is stored. A particular effort was done to extend the approach to critical registers (program counter, stack pointer, status registers…). Main advantages of such a hardware fault injection strategy are the reduced intrusiveness in the system, the low-cost, the possibilities of automation and the flexibility of the model in terms that several modules can be migrated on tests developed for other processors.

The architecture of THESIC+ tester, offered a suitable platform for CEU injection. The THESIC+ motherboard was enhanced with pseudo-random interruption generation capabilities and a new operation mode providing different options for CEU injection. With these options the selection of the two parameters of simulated upsets, the bits locations to be corrupted and the instant of fault occurrence, can be chosen according to the considered strategy (pseudo-randomly or deterministically). This flexibility appears to be very useful for the investigation of the effects of upsets on complex applications. For instance, repeated experiments with an appropriate statistical choice for both the CEU target and the occurrence instant, allow to get objective figures about the fraction of upsets which have no effects for a given program. Moreover, it may also put in evidence the configuration (occurrence instant / location) of critical upsets.

The capabilities of the CEU injection approach and the efficiency of error rate predictions were put in evidence through fault injection sessions performed using THESIC+, on architectures built on different processors including microcontrollers (the Intel 8051, the Motorola 68332, the PPC 750) and digital signal processors (the TI 320C50, the AD 21060). Faults were injected concurrently with the execution of modules extracted from final application programs. The same architectures and programs were used during radiation ground testing performed with different facilities, in which the processors were exposed to the effect of particles beams to get measures of error rates. The good agreement between predicted and measured error rates proved the validity of the approach.

However, this method has serious limitations when the targeted processor has significant hidden sensitive parts (cache memories for example), since it exploits processor instructions to inject faults and observe their effects.

The major flaw of the CEU method is that the obtained results are not relevant if the cache memory is not accessible through the instruction set. This problem can be solved by turning off cache memories during the program execution. However modern processor architectures rely on cache availability for their improved performance. For example, turning off cache memory leads to the loss of pipeline contributions to performance. Moreover cache memory sizes in the latest microprocessors have significantly grown:

- 532 KB for the latest Intel P4,
- 608 KB for the latest IBM PPC970.
Therefore, a modern processor running in a harsh environment is likely to have a high concentration of SEUs corrupting its cache memory bits.

Advanced work performed in the area of error rate prediction includes:

- Comparing the CEU approach to other fault injections methods using circuits simulated at different levels, such as: VHDL descriptions and ISS (Instruction Set Simulators).
- Enhancing it to allow fault injections in cache memories.
- Performing a complete error rate prediction and comparing it against a radiation measured one. The targeted chips for this study is a SPARC v.8 core and a MIPS64 one.

The PhD dissertation of Fabien Faure (scheduled in April 2004) will provide a comprehensive methodology to predict error rates for advanced integrated circuits.

2-6.5 Fault injections for predictive analysis of the erroneous behaviours of complex VLSI circuits

Members: A. Ammari, K. Hadjiat, R. Leveugle

Complex integrated circuits are today used in almost all application areas, including critical ones. Furthermore, the probability of faults (and especially transient faults) is rapidly increasing with the advances of the manufacturing processes; these faults are more and more critical even in consumer applications (e.g. SEUs resulting in bit-flips and disturbing the circuit operation even at the sea level). Designers must thus take care of the fault consequences in an increasing number of cases. Traditional fault injection techniques, allowing the study of the consequences of faults once a circuit prototype has been manufactured, are not an answer because they cannot cope with the decreasing time-to-market constraints. Analysing the behaviour of a circuit when faults occur is therefore becoming a major concern at the different steps in a design flow, and not only after the circuit is manufactured. Such an analysis is required to:

- identify unacceptable error propagation paths and unacceptable failure modes, and then guide design modifications at an early design stage,
- validate the efficiency of fault detection and/or fault tolerance integrated mechanisms,
- quantify the probability of the remaining failure modes for a given workload,
- prepare documentation for the circuit and/or reusable blocks (IPs).

To provide efficient support to the designers, the analysis must be possible very early in the design cycle. It should therefore be performed on high-level descriptions of the circuit. Then, the analysis must be refined along with the refinement of the circuit description during the different design steps, down to the gate-level implementation.

The goals of the project are:

- to develop a CAD environment, compatible with up-to-date design flows, helping the designer to analyse the behaviour of a digital circuit when faults occur. The environment can cope with different levels of descriptions of the circuit and different fault models. The consequences of the faults are assessed qualitatively and quantitatively by generating a graph similar to a Markov chain and showing the error propagation paths, the erroneous configurations reached for a given workload and the probability of each propagation. Fault classification is also possible.

- to propose and automate fault injection techniques for circuits described in high-level description languages. The first approach studied consists in modifying an initial VHDL description so that faults can be injected on a set of target nodes. This includes the insertion of saboteurs and the generation of mutants. Mutants are currently the main focus because saboteurs cannot help in injecting faults such as SEUs in behavioural descriptions. The generation of mutants is performed taking into account synthesis constraints, so that the injection mechanisms are compatible with both simulation-based and emulation-based experiments. Emulation has two advantages over simulation: the reduced time for running the injection campaign and the possibility to analyse the faulty behaviours taking into account real-time system interactions (in-system emulation). In the case of emulation-based experiments, an alternative approach has also been studied. It consists in injecting the faults directly in the hardware prototype by local reconfiguration of the FPGA. In that
case, the initial circuit description is not modified but the faults are injected by manipulations in the bit-stream used to implement the circuit onto the emulator (run-time reconfiguration).

Tools have been developed to automate the behaviour analysis (result analysis, generation of the graph, ...). A tool has also been developed to generate mutants allowing a designer to inject erroneous transitions in finite state machines or RT-level control flowcharts. Such erroneous transitions can model the consequences of SEUs in the state registers, and can be injected before the state assignment is performed by the synthesis tool, thus very early in the design cycle. Several types of VHDL modifications had been implemented and compared, demonstrating that some approaches are noticeably more efficient than others when emulation is to be considered. This generation is applied to high-level descriptions, before any synthesis is done, by identifying the locations in which flip-flops or latches will be required. The generation of mutants allowing the injection of SEUs in all memory points in the circuit is also available and the extension to other fault models (especially transient stuck-ats) and multiple faults is on-going.

Considering multiple faults becomes essential for several reasons. One is the increasing probability of transients in the combinatorial logic (Single Event Transients, or SETs), that can result in latching several erroneous bits on the combinatorial block outputs. Such SETs can be due to particle hits, but also to the signal integrity problems that are increasing in the most recent technologies. Another reason for considering multiple faults is the case of voluntarily induced faults aiming at perturbing the circuit to access to some unauthorized information. Such fault-based attacks are a real threat for security-oriented devices such as smart cards. Studies on security-oriented early analyses are on-going in the framework of the RNRT DURACELL project, run in collaboration with Gemplus, Thalès Communications and iRoC Technologies, and supported by the French Ministry of Research. They will be continued in the project VENUS of the program "ACI Sécurité & Informatique", also supported by the French Ministry of Research and started in 2004.

Injection campaigns have been run on various circuit examples, including microprocessor cores and industrial examples. Experiments have been done in particular on an example from STMicroelectronics, in the framework of the ERC project. In 2004, several studies have been launched in order to improve the outcomes of early dependability analyses. The accurate modelling of the circuit environment was shown to be an important point (study published at the Defect and Fault Tolerance Symposium). Preliminary experiments based on formal property checking were run. The interest of combining fault classification and error propagation analysis has been asserted (study published at the On-Line Testing Symposium). Finally, an extension towards analog blocks described using a high level language (VHDL-AMS) has been studied; results have been published at DATE in 2004. All these studies will continue in 2005.

2-6.6 Multi-level hardening of integrated embedded system for safety/availability and security

Members: R. Leveugle, M. Portolan

The goal of this project is to develop methods, libraries and tools to design robust integrated embedded systems. These systems must be able to cope with both natural faults and security-related attacks. In a first step, only fault-based attacks are considered. In a second phase, it is planned to include also robustness against side-channels attacks. The protection mechanisms are studied at several levels: logic, architecture, operating system and software.

A tool is currently developed, allowing a designer to easily insert, in a digital circuit, specific devices for on-line detection or tolerance of errors. The automated approaches must be flexible enough to provide answers for various application constraints (in terms of area, speed, power consumption and error coverage). Several approaches, previously proposed to be applied at the gate level or during the synthesis process, have been revisited to evaluate the feasibility of their implementation earlier in the design flow. The tool provided to automate this implementation must be compatible with industrial design flows based on commercial synthesis and simulation tools; we therefore focus on a stand-alone tool able to modify synthesizable VHDL descriptions. The modified description must of course be optimised for an efficient synthesis.

A prototype tool had been developed and proved the feasibility of the concept. Two types of modifications were automated. The first one aims at tolerating SEUs in the state registers and in the combinatorial logic computing the next state in finite state machines. The second approach is based on control flow checking and performs the on-line monitoring of the internal operation sequencing. The tool developed allows a designer to automatically
modify the VHDL description of either a finite state machine or a circuit described as a RT-Level control flowchart. The efficiency of the approach was demonstrated by comparison with previous results obtained when implementing the same techniques at a lower level, i.e. during the synthesis process using a specific synthesis tool. Furthermore, modifying directly the high-level description allows an earlier validation of the system response in presence of faults and provides extra benefits in terms of re-usability. Several other approaches are currently considered to extend the capability of the tool to address various types of block architectures and various application constraints. The hardening approaches that are considered target either safety/availability in presence of natural faults, or security against attacks. Part of this work is applied in the framework of the RNRT DURACELL project, in collaboration with Gemplus, Thalès Communications and iRoC Technologies, and supported by the French Ministry of Research.

In parallel, robust versions of processor cores are studied. In particular, a robust version of the Leon processor is being developed. Also, modifications of the eCoS real-time operating system have been defined to provide low-cost fault tolerance and secured cryptographic IPs are designed (AES, RSA, ...). The global project has lead in 2004 to the development of a first embedded system demonstrator, implemented on a Xilinx Virtex II Pro development board. This work will continue in 2005, in particular with fault injections performed on the demonstrator.

In addition to the development of hardening techniques and tools, a study has started on the impact of fault-oriented protections on leakage information. As a matter of fact, it is useless to protect a circuit against only one type of attack, since a hacker could use several approaches to obtain a secret information. Fault-based attacks are one type of threats. Another one is the use of so-called "side channels", and in particular the power consumption or the electromagnetic emissions, to infer some confidential data used during a computation. It is therefore very important to ensure that protections against fault-based attacks do not facilitate an attack using the side channels (and vice-versa). This is the main goal of the MARS project, part of the program "ACI Sécurité & Informatique" supported by the French Ministry of Research. This project has started in 2004 in collaboration with ENST.

2-6.7 Towards robust nanoelectronics design

Member: R. Leveugle

Some work started in 2000 on the implementation of logic circuits using nanoelectronic devices. This project had been defined in collaboration with CEA/LETI and aimed at taking advantage of the silicon-based single-electron transistors (SETs) developed in Grenoble. A preliminary study of the state-of-the-art had been performed, including the study of simple logic and arithmetic components and some expertise of the simulation approaches available for such devices. The use of carbon nanotubes transistors (CNTFETs) is also considered.

The work aims at proposing, at medium term, solutions to implement robust logic elements based on these components. This implies defect tolerance due to the expected high density of manufacturing defects, as well as fault tolerance to cope with other problems such as process parameter variability, background charges and transient faults. This is our proposed contribution in the NANOSYS project, part of the program "ACI Nanosciences" supported by the French Ministry of Research and started in 2004 in collaboration with many French research teams.

2-6.8 Built-in self-repair architectures for nanotechnologies

Members: L. Anghel, N. Achouri

Built-in self-test (BIST) is becoming today the dominant memory test approach, especially for embedded memories. In fact, memory devices represent by far the largest part of electronic systems (e.g. even 70% of the total area in Pentium processor). Because memory cells are designed at the physical limits of the technology, they are more prone to failures than standard logic. Therefore they collect the larger number of defects and become the main cause of quality reduction and yield loss. In nanometric technologies this situation will be even worsen. In fact, reliability issues will block the introduction of new technologies if not addressed properly. Therefore, fault tolerance is mandatory. The fault tolerance techniques proposed are based on memory repair
(Built In Self Repair). They use redundant resources to ensure correct operation when the regular resources are affected by the fault.

This work has been done under IST -FET Project named FRACTURE. In this project, several BISR solutions considering memories affected high defect densities have been proposed. With respect to traditional BISR approaches, they represent a serious innovation in this domain because:

- they consider high defect densities
- they consider faults affecting both the regular and spare elements.
- they perform multiple faults repair per test and repair pass
- they propose BISR circuitry for performing the memory reconfiguration.

Some of the BISR techniques developed are summarized below:
1. One of the approaches consider a dynamic repair approach that increases the multiplicity of repaired faults by using a single spare unit for repairing faults affecting several regular units.
2. A diversified approach is also proposed that combine dynamic data repair scheme with block repair scheme.
3. Another approach combines faulty units to provide a repaired unit, instead of replacing a faulty unit by a fault free one. This approach should work better for very high densities, since for these densities it becomes difficult to dispose fault-free units. The combination it is based on the fact that in the majority of situations the faulty cells will not affect the same positions in two different units. Thanks to these principles, these techniques can handle large fault multiplicities and are suitable for memories affected by high defect densities
4. Another diversified approach mixes ECC codes that repair the majority of the faulty memory words with a word repair scheme that repair the words left un-repaired because they include a large number of faults.

Thanks to these principles, these techniques can handle large fault multiplicities and are suitable for memories affected by high defect densities. However, evaluation were performed to determine the comparative merit of these techniques with respect to memories affected by high defect densities. Evaluations have been performed by means of statistical fault injections, to determine the best approach for various memory sizes and defect densities.

2.6.9 Study of the efficiency of hardware and software hardening techniques

Members: R. Velazco, F. Faure

The increasing popularity of low-cost safety-critical computer-based applications in new areas (such as automotive, biomedicall, telecontrol) requires the availability of new methods for designing dependable systems. In particular, in the areas where computer-based dependable systems are currently being introduced, the cost (and hence the design and development time) is often a major concern, and the adoption of commercial hardware is a common practice. As a result software implemented fault tolerance is an attractive solution for this class of applications, since it allows the implementation of dependable systems without incurring the high costs coming from designing custom hardware or using hardware redundancy.

This project aims at evaluating the efficiency of two different approaches studied to enhance system dependability: one of them, consists in a software modification strategy allowing the on-line detection of bit flips affecting memory elements of digital architectures, while the other aims at the automated rapid prototyping of processors including error detection and correction capabilities achieved by means of Hamming codes.

This project is done in collaboration with the Politecnico di Torino.

Fault tolerance capabilities can be obtained in hardware designs using traditional error detection and correction strategies such as Hamming codes. For a complex circuit such a processor, protecting by suitable codes every
memory element potentially sensitive to bit flips resulting from radiation, may lead to a robust low-cost device version. To investigate the potentialities of such a hardware hardening strategy, a simplified version of the 8051 microcontroller, for which Hamming codes were added to registers and internal memory, was fully implemented in an FPGA. The digital board including the FPGA implementing the 8051 hardened micro-controller was exposed to heavy ion beams using a cyclotron (the Cyclone facility available at Louvain-la-Neuve, Belgium). Performed tests revealed the 100% immunity to upsets for the robust circuit, while for the standard version, implemented in the same board by proper configuration of the FPGA, hundreds of errors were detected for the same particle beams. This robustness with respect to bit flips is obtained with acceptable hardware and time overhead.

The design of a software tool for the automatic generation, from a circuit high level description (in VHDL for instance) of the hardened description circuit is now in progress. The flexibility offered by modern FPGAs will allow the validation of this tool by performing ground testing and fault injection experiments on a wide range of processors.

This project was done in collaboration with Politécnico di Torino and UFRGS (Université Fédérale de Rio Grande do Sud, Porto Alegre, Brésil).

2.6.10 A methodology to generate hardened cells based on automatic layout generation

Members: L. Anghel, C Lazzari

Soft error rates induced by cosmic radiation become unacceptable in future very deep sub-micron technologies. Many hardening techniques at different abstraction levels have been proposed to cope with increased soft error rates. Depending on the abstraction level some techniques need to modify the design at architecture, circuit or transistor level, others required the modification of the circuit layout or to use new hardened cells within the circuit. In most of the situations, these kinds of structures are not implemented in standard cell libraries. Thus the classic ASIC standard cell based design cannot be completed. Automatic layout generators may be used to create those structures to finalize the design, thus reducing the system design time. An automatic layout generator develops each element (transistors and connections) according to a layout pattern that is intrinsically programmed within its algorithms. Furthermore, automatic generation can be flexible to create optimized layouts to each situation where they are inserted. A fist version of such a tool named Parrot Punch has been developed in University Federale Rio Grande do Sul, Bresil and new optimized versions are currently under study in TIMA. The tool is able to generate any kind of static CMOS circuit on-the-fly. Generated layouts have transistors and nets optimized according logic characteristics of the circuit. This tool is used to implement some hardened solution on complex structures such as processors. Further improvements will address analog circuits, and dynamic logic.

This project is done in collaboration with UFRGS (Université Fédérale de Rio Grande do Sud, Porto Alegre, Brésil).

2-6.11 A methodology for test replacement solutions of obsolete processors

Members: R. Velazco, L. Anghel, P. Peronnard, S. Saleh

Processor obsolescence is becoming an increasingly complex problem for industrial embedded computer users. Since 1970’s when computers become popular for public use, computer hardware and software technology has grown at an exponential rate. As computer technology improved and became more efficient and functional, the computer user has been too often pushed to take decisions about how to upgrade the hardware, operating system and the software. Obsolescence of electronic components affects basically electronic equipments design engineers involved in safety critical applications (automotive, avionics, airframe, nuclear plants, military applications...). These applications are active years longer than it was originally anticipated. They often include microelectronic parts that now become obsolete. In this context, these applications are expensive to maintain, because they continuously require additional processing elements and software but also memory parts to face changing requirements.
Computer obsolescence is manifesting in different ways: either we assist at a dramatic decrease of the spare parts availability for processor replacements or we observe the inability of the processor to be adapted to new software requirements. Regardless how the problem manifests itself, the solution which is often proposed is to replace some of the obsolete parts with more modern ones. In this case, the basic idea is to completely redesign the replaceable unit in order to update the system. The main drawback of such a solution is the huge engineering design efforts and costs, including qualification testing and certification in case of critical applications, to meet reliability/safety requirements. Revision of the software is also costly, sometimes exceeding the original time required for hardware design.

At the heart of the microelectronic applications of interest to this work, out-of-date processors (microcontrollers, microprocessor, DSP, etc.) constitute the biggest bottleneck. In this project, we only address processors, having considered an 8 bits microprocessor: the Motorola 6800 as a first test vehicle. This component is included today in the equipments of some French nuclear plants. These equipments are supposed to run 40 more years. Unfortunately, even if companies have stocked obsolete parts, these stocked parts will be rapidly exhausted. Thus, the only viable solution is to replace obsolete parts.

A very flexible and less costly replacement solution consists in emulating the obsolete processors by means of programmable logic devices such as FPGAs. Indeed, high level descriptions in an appropriate language can be developed from the description of the circuit datasheet, and used further to replace targeted obsolete processors. The problem is how to prove that the emulated version is equivalent to the original hardware one, and these in term of functionality, performances and signal integrity. To prove such equivalence we have used a specific test platform allowing both to exercise the emulated version and the original one by running appropriate test programs, and to compare the input/output values of both versions at suitable temporal granularity.

**Obsolete parts replacement methodology**

The strategy proposed in this work to deal with processor obsolescence aims at replacing only legacy hardware in a given architecture. The action is done by creating a HDL (Hardware Description Language) model from the old hardware version and emulating it on a FPGA device without any architecture modification around. This replacement solution is a very low cost approach in case we have small parts replacements, even if the replacement requires some modifications at the board level, and comprises the following steps:

\[ a) \] Create a high-level description design of the circuit under study. In our work, we have chosen VHDL for modelling the 6800 Motorola processor. In this phase, we need to consider the functionality and performances of the original processor from the original datasheet.

\[ b) \] Validate the VHDL description by means of simulation of original input vectors created in the specification phase. If the original input vectors are unusable, create an appropriate test program to completely test the microprocessor. The test program will respect the state of the art of microprocessor testing. The main issue of this step is the list of DUT response output vectors.

\[ c) \] Compare the obtained output vectors with the golden ones issued from running the same program on the processor obsolete hardware version.

\[ d) \] Modify the VHDL code according to identified divergences between versions and re-simulate if required.

\[ e) \] Synthesize the VHDL description on an appropriate FPGA device. The main constraint in this phase is to emulate the HDL model on a single device.

\[ f) \] Run test vectors used in steps b) and c) on both an architecture built around an FPGA and the architecture including the obsolete part. The comparison of vector output files provides information about the identity of two tested versions.

\[ g) \] The final step is to validate the original architecture including now the emulated part instead of the obsolete ones at the customer requirements.

Hardware and software requirements are the key points of simulation and validation methods. Indeed, running both the original processor and the emulated version needs dedicated test equipment allowing to be easily adapted to the DUT interfaces. On the other hand, the test program being the key point to guarantee the significance of the identity between the two versions, it is mandatory to generate it by means of suitable automated tools.
Hardware and software tools to cope with processor obsolescence

The main problem entailed by the proposed strategy is the wide scope of targeted circuits, requiring the availability of a hardware platform having enough flexibility to lower timing and cost efforts to implement any suitable architecture.

The THESIC+ tester developed for radiation testing purposes and described in §2.6.3 of this section, appeared as meeting the requirements of the proposed methodology for validation of “cloned” version of obsolete processors. Photos given in Figure 2.6.4 illustrate the hardware simplicity of the DUT board built around the 6800 microprocessor due to the features of THESIC+ tester. Indeed, practically all the hardware interface is implemented in the FPGA of the THESIC+ after a suitable description in an HDL language. As shown in the photo at the right, the hardware comprises only the target microprocessor, its cloned version being implemented in the FPGA of the THESIC+ board. Both implementation can run the same test programs, differences in results being automatically identified for the identification of potential errors in the HDL description.

Figure 2-6.4  Adapting the THESIC+ tester to validate the emulated version of the 6800 microprocessor

Pseudo-exhaustive functional test program generator

In the 80’s many approaches were investigated to cope with the test and diagnosis of processors without taking into consideration the structural information (electrical schemes, topology, etc.). Among relevant strategies can be mentioned the ones starting from a functional error model to derive test programs, for which it was estimated a fault coverage. Most significant approaches have all the same weakness: the difficulty of stating a priori a significant functional error model. As real defects have often very complex manifestations at functional level, difficult to be modelized without structural information, the solution we adopted was to develop a tool allowing to generate pseudo-exhaustive test program which exercises all the valid combinations of instruction opcodes and addressing modes. Each of these combinations is preceded by an initialization sequence in which pseudo-random data was loaded in all registers of the tested microprocessor, being followed by an observation sequence whose execution store the register’s contents in a specific memory area for further analysis.

Such a module, called elementary module, allows performing diagnosis in case of obtention of data different from the expected one. As the fault will not propagate out of the elementary module borders, several elementary modules corresponding to each possible combination of opcodes and addressing modes must be exercised to reach significant defect coverage.

Obtaining pseudo-exhaustive test program for a particular processor is not an easy task and requires dedicated tools. It can even become not affordable for complex (32 bits and more) processors. In the past, an automated tool, so called GAPT, was proposed to get experimental results and validate the proposed approach. Defects like stuck at, open, shorts have been produced on a wafer of 68000 processors by means of a laser. A relevant set of experimental results, issued from the application of the test programs generated by GAPT to a set faulty 68000 processors were obtained. Moreover it was shown how such an approach could lead to useful diagnosis allowing to locate defects if required structural information is provided.

A case study: the 6800 processor

We have selected the Motorola 6800 processor, which is today a major concern for French nuclear plants. Indeed, this component, selected 25 years ago to be part of high safety equipments, is no more available in the market, and the company is quickly running out of stocks. One of the solutions studied is to replace it by implementing the 6800 processor by a suitable emulation implemented by means of a programmable device (e.g. FPGA).
After a detailed analysis, it was evident that this error was produced by an erroneous synthesis model of the HDL 6800 description. This transition fault has never been observed by any other application or testbench program. This fault will never manifest itself as an error. It concerns the 6th bit of the CCR register which is not used in applications (X bit interrupt). In fact, the instruction set does not provide any “set” or “clear” instruction. In addition this bit is never update by any other instruction from the instruction set.

After a thorough analysis of results produced by the cloned version, other errors in the VHDL were identified and corrected:

- Wrong execution of transfer with increment / decrement instructions “TSX” and “TXS” between two particular registers (the stack pointer SP and the index register IX): the increment/decrement was not performed.
- Wrong execution of decimal adjust (DAA) instruction: no operation was performed and bad affection of flags C and V of conditional code register (CCR).
- Wrong positioning of flags when executing instruction of comparison between and index and a byte addressed by any of the addressing modes (instruction CPX).
- Wrong storage of the value of the program counter (PC) in the stack when two particular instructions SWI (software interrupt) and WAI (Wait) were executed AFTER a one of the instructions of a particular set. It is important to note that the involved instructions, when executed not in sequence, operate correctly.

After this validation the corrected microprocessor description was placed and routed and the cloned 6800 was then prototyped using an Altera FPGA component.

Future work

The studied method to cope with the validation of HDL processor’s descriptions aiming at replacing obsolete processors provided an efficient way to identify and correct errors in the HDL description of the target processor. The proposed methodology final goal is to prove at both the functional and timing points of view, that an emulated version using an FPGA and the original version are strictly identical. This methodology and the selected tools are both automated and flexible enough to be adapted to any target processor with limited time, cost and development efforts.
2-7 Multidisciplinary projects

2-7.1 Wireless Universal Control System for Ambient Intelligence

Members: all groups
Editor: M. Renaudin, CIS group

The WUCS project emerged from a consensual idea of conducting at TIMA a collaborative research work on an advanced high technological system, involving the top level research activities carried out at TIMA. The project's goal is to create the conditions of a fruitful interaction between researches having a high level of knowledge in different but related scientific domains. Every group leader adheres to this idea and is convinced that such a project is stimulating knowledge and innovation. Besides, such a project gives to the research groups the opportunity to contribute to a wide scientific spectrum collective work, valorizing the sharp and deep skills they develop.

The WUCS concept is definitely in the straight line of the emerging "ambient intelligence" paradigm. It is a wireless, communicating, multi-sensor system, embedding powerful computing capabilities. It is a smart device, part of a distributed network, interacting with its environment and providing services in a general sense to users or other devices.

Therefore, WUCS is a system able to capture information, to recognize and identify its environment, and securely exchange information through wireless communication links. It should be autonomous, embedding its own source of energy. It is then characterized by three essential functionalities:
- automatic recognition of its environment,
- wireless communication with other WUCS devices,
- secure storage and exchange of data,
- autonomy.

Hence, WUCS is a heterogeneous system, that includes hardware/software, analog/digital, electrical/mechanical parts, all adapted and tuned to the targeted services/applications.

The design of such a smart device requires a tremendous amount of knowledge in different scientific fields, ranging from computer science and networking to physic and nano-electronic. The following competences developed at TIMA will contribute to the WUCS project:
- formal modeling and verification,
- hardware/software, continuous/discrete and electrical/mechanical co-simulation,
- test and qualification of integrated systems,
- high level synthesis, hardware/software co-design,
- radio-frequency system design,
- low-power digital and mixed circuit design,
- sensors, actuators and micro-systems design (mems).

As the first step and proof of concept, an instance of a WUCS is being designed. It integrates some of the key functionalities previously described. Pushing this work until the fabrication of a prototype is considered as essential. There is here a difficult tradeoff which consists in designing a real object to master the technologies and prove the concept without ambiguity, while focusing on research activities and not spending too many resources in pure development efforts.

Figure 2-7.2.1 WUCS architecture
Figure 2-7.2.1 shows the WUCS architecture and the following paragraph highlights some of the key technologies involved in this smart device. The system can be seen as a generic platform. Each component can be chosen to better fit the field of applications targeted. This modularity is possible thanks to the clockless architecture.

WUCS can be either self powered or integrate batteries. When self powered, the environmental energy surrounding it is converted into electrical energy. Many solutions can be focused on, but the most suitable and investigated at TIMA is based on piezoelectric elements (Figure 2-7.2.2). Indeed, piezoelectric micro-power-generators can deliver a sufficient amount of energy to supply the whole system by converting mechanical vibrations into electrical energy. A power control optimizes the yield of the micro-electromechanical device. If the energy produced exceeds the circuit’s need, it can be stored in a buffer storage battery.

Combining such a micro-generator with the asynchronous technology is particularly interesting because asynchronous circuits do accommodate of a low supply voltage as well a low quality voltage regulation. This enables significant complexity savings and therefore energy savings.

WUCS is to be part of an ambient intelligence overall system which thus requires software running on a microprocessor. An asynchronous 32 bit MIPS-like processor is chosen for software intensive applications whereas an 8 bit asynchronous microcontroller is preferred when software load is low. Several power reduction techniques are used to optimize both the dynamic and static power consumptions of the different components of the system. Apart from low-power design techniques applied at architectural, logical and transistor levels, our system includes dynamic voltage scaling (DVS). Voltage scaling/scheduling is performed by a dedicated co-processor and a very light and cheap software layer. According to the application requirements (computational loads and real-time constraints), the co-processor controls a DC-DC converter following a law which minimizes the energy consumed by the processing parts. Note that because the microprocessor is clock-less, controlling its speed and energy consumption only requires adjusting the voltages, and does not require a costly frequency generator. Figure 2-7.2.3 describes the principle of the system. Hence, in our system, the total energy burned is directly dependent on the application or the environment demands and is dynamically minimized by jointly controlling Vdd and Vbb.

In order to integrate sensors in the WUCS and interface them with the digital processing parts, new asynchronous analog to digital converters were developed. Asynchronous ADCs take advantage of the analog signal properties to perform non-uniform sampling thus saving activity and power. Non uniformly sampled signals are processed by the asynchronous processor following a dedicated theory we are developing. Again, non uniform signal processing is another source of power saving.
To satisfy security considerations that an embedded system can suffer from, low-power, low-voltage DES and AES crypto-modules are available and can be integrated in the WUCS architecture. Software applications can therefore exploit these hardware resources to perform cryptographic tasks. This not only increases the speed but also reduces the energy consumption. Security is also addressed at the hardware level by using asynchronous logic which protects the system from hacking techniques based on common side channel attacks such as SPA (Single Power Analysis) and DPA (Differential Power Analysis). Asynchronous logic is also exploited to protect the hardware from fault injection and DFA (Differential Fault Analysis) based attacks.

Apart from the wide spectrum of competencies and technologies involved in the design of such a complex device, it is worthy to mention that another wide spectrum of competencies is necessary in terms of design methodologies to successfully prototype such a WUCS.

**2-7.2 Architectures based on quantum effects**

Members: F. Ciontu, B. Courtois
Partner: PH. Jorrand

The advent of nanotechnologies will make quantum effects play a primordial role in the functioning of the next generations of computation devices. Considered today a problem from the perspective of deep submicron CMOS miniaturization, quantum effects will gradually become technological concepts on which the “alternative” devices will rely and eventually will provide the physical support for a new algorithmic concepts in quantum computation. A prospective study performed at TIMA analyzed the state of the art technologies based on quantum effects, the proposed architectures based in these devices and the changes in terms of computation model (Figure 2-7.2.1a).

![Image](https://via.placeholder.com/150)

**Figure 2-7.2.1**

One of the topics approached in TIMA’s research on nanosystems are quantum architectures. This research takes place in the framework of a multidisciplinary project between TIMA, LEIBNIZ Laboratory (theoretical computer science) and several physics laboratories including the Louis Néel Laboratory (Figure 2-7.2.1b).

![Image](https://via.placeholder.com/150)

**b) The partnership in the framework of the interdisciplinary project Quantum Computing on Cellular Architectures**

Research on quantum computing at TIMA focused on architecture-related issues while strongly interfacing with both computation and physics. The goal of this work is to study the impact of physical constraints on different quantum computational paradigms and to define a framework for assessing qubit and quantum gate implementation proposals from an architectural point of view.

This goal meets some important challenges as the field of proposals for physical implementation of qubits and quantum gates is anything but homogenous. Indeed, different technologies range from NMR and

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1 LEIBNIZ Laboratory, Grenoble, France
2 Louis Néel Laboratory, Grenoble, France
trapped ions to solid state proposals and make the finding of common denominators rather difficult. Thus, the QIQT Roadmap partially covers the existing proposals through no less then eight classes of technologies with radically different characteristics.

Solid-state technologies share a certain number of essential constraints. This allowed us to envision a work where fundamentally, we are interested in the relationship between elementary, qualitative physical constraints and decoherence. This should in turn give us a common basis for evaluating different paradigms. Our recent activity consisted of creating an abstract architecture model. This model has associated a metric related to decoherence that provides a common basis for comparing different architecture primitives or qubits implementation technologies.

Although the general framework for these kinds of considerations remains vague, we could focus on two fundamental results. The first one refers to the constant limit of decoherence per operation, usually taken as $10^{-4}$, that is necessary in order to implement quantum correction codes. The second one refers to the fact that, without quantum error corrections, the probability of decoherence increases exponentially with the number of quantum gates. Introducing quantum error correction costs might solve this problem but often at a very high cost in terms of resources.

The core issue of this task was the definition of the constraints mentioned above and finding how they can be parameterized. The constraints apply to a lattice-based model where qubits and operators are subject to restrictions in their positioning. A first class consists of fundamental constraints like the impossibility of copying quantum information. Other conditions, while still qualitative can be more technology specific: e.g. the availability of the “flying qubits” introduced by DiVincenzo as a desiderata in addition to his famous five criteria. Sometimes, physical qubits are mobile like in the case of electrons or photons. In some others, they are static, which is the case in Kane’s proposal. Moreover, coupling a technology with static but more reliable qubits used for computation and mobile qubits used for communication cannot be excluded. Other geometric constraints can be introduced by various physical classical-quantum interfaces. At the nanometer scale and especially in the low temperature ranges needed to prevent decoherence, “classical” wires and devices exhibit strong quantum behavior. This can be an important issue when classical control is needed and quantum behavior would negatively influence it. By consequence, minimal size constraints could be imposed on the classical components in order to prevent quantization effects. This could pose important architectural constraints if the length of some communication channels would have to increase and the probability of decoherence would increase exponentially with the length. Finally, some existing proposals for qubit implementation come with numerical details.

Ultimately, the abstract model should automatically map these constraints to decoherence and allow the comparison of different paradigms or architectural primitives in terms of their suitability for implementation. In some cases the mapping should be expressed in terms of decoherence times (static decoherence). In other cases decoherence can be introduced through different error-models: e.g. depolarizing errors, phase shift errors or measurement errors.

Future work will focus on the use of this abstract model for the study of micro-architecture primitives. Similar questions have been explored in the litterature in a study of the scalability of a switch chain vs teleportation as a communication mechanism for the Kane’s qubit proposal. Our approach should be more more general since the fundamental constraints defining the abstract architecture model are not related to a particular technology. An immediate example from the plethora of new problems to be investigated is the extent to which the mix between ‘flying’ and ‘static’ qubits is the source of a permanent interplay between communication and computation.
3 - Service Activity

The Laboratory is hosting the CMP Service Activity\(^1\)

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<tr>
<th>CMP Members</th>
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<th>N. Brechet</th>
<th>S. Colin</th>
<th>P. Chassat</th>
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<td>A. Khalid</td>
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Introduction

The CMP project (Circuits Multi Projets®) is a project undertaken since 1981 by the Laboratory. In 1984, the service became a "Unité de Service et de Recherche", depending on CNRS and INPG. This project allows the Universities, Research Laboratories and Companies to fabricate the Integrated Circuits and Microsystems they have designed. Fabrication is for prototypes or low volume production. The originality of the project consisted initially in the regrouping, on the same slice of silicon, of a large number of circuits. Thus accessible costs of fabrication are obtained.

Since 1981, more than 700 Institutions from 60 countries have been served, about 4500 projects for Research, Education and Industry have been prototyped through more than 500 manufacturing runs, and 50 different technologies have been interfaced.

For each project the operations to be achieved are the following:
- collection of circuits described in a common language
- checking of the circuits (syntax checking and design rules checking)
- assembly in macro-blocks (sets of chips)
- generation of the entry connections for the manufacturer
- subcontracting the fabrication of the circuits
- subcontracting the post processing (if any, for Microsystems)
- subcontracting sawing and packaging of the chips
- delivery of chips to the end users.

In parallel CMP distributes the design rules for each technology and the standard cell libraries for each specific software tool (design kits). CMP handles about 30 different design kits corresponding to the different technologies and CAD tools. They are sent to customers upon signature of a Confidentiality and Licence Agreement. More than 700 customers have already signed the agreements and received the kits.

Development since 1981

Since 1981, 526 fabrication runs have been undertaken. The complexity of the circuits has passed from several thousands transistors in 1981 to hundreds of thousands transistors in 1985 and next millions of transistors. The history of CMP development is presented below. Each time the new technologies proposed were among the most advanced ones in the considered period.

| 1981–1982       | launching CMP with NMOS |
| 1983–1984       | development of NMOS, launching CMOS |
| 1984–1986       | development of CMOS |
| 1987–1989       | abandon NMOS, increase the frequency of CMOS runs |
| 1990–1994       | launching Bipolar, BiCMOS, MESFET GaAs, HEMT GaAs, advanced CMOS (.5 µ TLM) and MCMs |
| 1995–1997       | launching CMOS, BiCMOS and GaAs compatible MEMS, DOE, deep-submicron CMOS (.25 µ 6LM) |
| 1998            | launching surfacemicromachined MEMS, abandon MESFET GaAs |
| 1999            | launching SiGe, 18 µ CMOS |
| 2001            | .35µ HBT SiGe BiCMOS, .12µ CMOS, SOS/CMOS |
| 2003            | .25 µ HBT SiGe BiCMOS, InP HBT, MEMS: PolyMUMPS, SOIMUMPS, MetalMUMPS |
| 2004            | launching 90nm CMOS |

Table 3-1 presents the Institutions which submitted circuits from 1981 to 2004.

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\(^{1}\) A specific report is available upon request.
Table 3-2 gives an overview of the different manufacturing runs. Nearly 4500 circuits were manufactured since 1981.

**CMP projects in 2004**

In 2004 a total of 260 circuits were fabricated for 86 organizations (Universities, Research Laboratories and Industrial Companies) all over the world (24 countries). This is comparable to 2003 figures (283 circuits for 85 organizations). Hereafter are the technologies used in 2004:

For Integrated Circuits:
- 0.8 µ CMOS DLP/DLM from austriamicrosystems
- 0.6 µ CMOS DLP/TLM from austriamicrosystems
- 0.35 µ CMOS DLP/4LM from austriamicrosystems
- 0.35 µ CMOS-Opto DLP/4LM from austriamicrosystems
- 0.35 µ CMOS RF DLP/4LM from austriamicrosystems
- 0.8 µ BiCMOS DLP/DLM from austriamicrosystems
- 0.35 µ SiGe BiCMOS from austriamicrosystems
- 0.18 µ CMOS 6LM from STMicroelectronics
- 0.12 µ CMOS 6LM from STMicroelectronics
- 0.35 µ SiGe BiCMOS 5LM from STMicroelectronics
- 0.2 µ GaAs P-HEMT E/D from OMMIC

For Micro Electro Mechanical Systems:
- 0.8 µ CMOS DLP/DLM from austriamicrosystems, compatible front-side bulk micromachining
- Multi-User MEMS Processes (MUMPs) PolyMUMPS from MEMSCAP, surface micromachining

**Type of circuits and evolution during the last years**

*Figure 3-1* shows the evolution in total number of circuits manufactured per year. From 1994, around 300 circuits are manufactured every year.

*Figure 3-2* shows the distribution of circuits per technology during the four last years. CMOS and BiCMOS together represent 87% of the manufactured circuits. The relative part of CMOS is always growing. GaAs accounts for 8% and is stable along the 4 last years. MEMS represent 5%.

*Figure 3-3* shows the distribution of circuits depending on the purpose: research, education or industry. As in 2001, 2002 and 2003 the percentage of industrial circuits represents nearly ¼ of the circuits (21%). The percentage of circuits for research is 65%.

*Figure 3-4* shows the year of arrival on the market of the different CMOS technologies (source: Semiconductor Industry Association), given by the good size in microns, and the technologies used by CMP. Both curves have converged. This means that CMP continues to use the most advanced CMOS technologies as soon as they are introduced.

**Participation of Industry**

In 2004, 55 industrial circuits, 43 from France and 12 from foreign countries, were fabricated for 25 industrial companies or national research laboratories. This level of industrial participation is nearly the same along the last four years (about 25% of the total number of circuits). They were manufactured for prototyping or low volume production (21 low volume circuits from fifty pieces to hundred of thousands pieces).

**Micromachining Program**

CMP has been the first non-US multi-project-wafer service to introduce Microsystems manufacturing, as early as 1995. Two types of technologies are proposed. One is fully compatible with microelectronics processes, and allows the monolithic integration of microstructures and electronics circuitry (front side bulk micromachining). The technologies used are CMOS and BiCMOS from austriamicrosystems and P-HEMT E/D GaAs from OMMIC. Applications are thermal sensors, mechanical sensors (acceleration, force, pressure), etc. The other is specific to MEMS structures (surface micromachining). It is used in particular for micro motors, micro mirrors, etc. It is provided by MEMSCAP through 3 processes MetalMumps, SOIMumps and PolyMumps. 18 circuits were manufactured in 2004 (5 bulk micromachining and 13 surface micromachining) for 6 organizations.
Collaborations with other Services and Organizations

Cooperative agreements: CMP has signed cooperative agreements with the following Institutions:

- CIC, Taiwan
- FAPESP, Brazil
- Royal Institute of Technology, Sweden

CMP Distributors:

- Southeast University, Nanjing – China
- K&H, Beijing – China (North)
- DesignFuture, Pondicherry – India
- Integrated Microsystems (IMS), Gurgaon - India
- WizTrade, Ranana – Israel
- Also distributors in Singapore, Russia, Australia and New Zealand

Collaboration CMP – CMC – MOSIS

From 2001 the three main ICs manufacturing services from USA (MOSIS), Canada (CMC) and France (CMP) started a partnership in order to exchange some of their services and to enlarge the portfolio of technologies proposed by each partner. In this way technologies from austriamicrosystems and OMMIC were offered to MOSIS customers and technologies from Peregrine, IBM and Vitesse were offered to CMP customers. This program will still be developed in 2005. Such program is necessary to support escalating costs of very deep sub-micron processes or the low demand of very specialized processes.

CAD tool offers

CMP distributes and supports several CAD softwares for Universities or companies. More precisely CMP has agreements with:

- Tanner Research, Inc. to distribute the L-edit layout editor and the T-Spice simulator, for University and Industry
- ARM Ltd. to provide academic institutions with software and hardware materials developed by ARM for designing and manufacturing Systems on Chips based on RISC processor architecture. The goal is to give engineering students the up to date tools to gain skill and experience in systems development. More than 180 CAD licenses have been distributed among 87 Universities and Research Laboratories including 31 in France.
- CADinformatique company to offer the package HDL-designer/ModelSim/Leonardo to academic Institutions.
- SoftMEMS tools: CMP distribute the SoftMEMS software tools (MEMS Xplorer for UNIX workstations and MEMS Pro for PC operating systems) to Universities, Research Laboratories and Industrial Companies.
- CMP also widespreads information on free software tools available from other services or Universities and distribute design kits for these tools.

IP exploitation

- RAMs and DP-RAMs are available for the processes offered at austriamicrosystems and STMicroelectronics
- Risc processor: In 2003 CMP signed an agreement with STMicroelectronics and ARM to make available the integration of ARM cores in 0.12 CMOS, for circuit prototypes of Universities and Research Laboratories. Three projects were going on in 2004.
- Access to other IPs blocks will be developed in 2005.

Other activities

In addition to the manufacturing of circuits, various other tasks are carried out in order to develop specific tools, to answer specific needs or to gain new competences. That has been for example:

- the determination of the rules of multitechnological design,
- the development of translators for various IC descriptive formats,
- the development of tools to check or correct syntax descriptions,
- the development of design kits. In the past CMP developed design kits for TANNER/L-Edit, EXEMPLAR/GALILEO, COMPASS, CADENCE, etc. In 2004 CMP developed a full custom and standard cell design kit for 0.35 µ CMOS austriamicrosystems and Tanner L-Edit, for digital and mixed signal circuits.
Quality Assurance System

By the end of 1997, in order to increase and to promote the quality of the service, CMP began to implement the ISO9002 Quality Assurance standards. The quality assurance manual was written as well as the various quality assurance procedures. The system was completely set up by mid 1998. During the two following years the various requirements of the Quality Assurance System were applied, and in June 2000 the service was assessed and got the certification “ISO 9002” (see the certificate at the end of the chapter). In June 2001 and September 2002 the certification was renewed. CMP continued to apply these ISO 9002 standards in 2003 and 2004. Now the “ISO 9001/2000” standards have to be implemented.

Conclusion

France has been a pioneer country in this type of infrastructure since chip fabrication for Universities has been started in 1981 by CMP; the elementary CAD software LUCIE issued from the Laboratory was provided to 36 Academic Institutions in France and foreign countries. In the 80s industrial CAD software was distributed to Universities in 1987 by CNFM and testing equipment was centrally purchased in 1988. As early as 1990 CMP opened chip fabrication services to Industry.

The most recent advanced industrial processes were offered as early as possible such as .5µ CMOS in 1994, .25µ CMOS in 1998, .12µ CMOS in 2001. Multi-Chip-Modules were launched in 1992 and MEMS in 1995.

In 2004 CMP continued to offer a large portfolio of technologies (23 different processes : 17 for ICs and 6 for MEMS) and a wide variety of associated services to a lot of institutions for academic and industrial purposes. The total number of circuits remains at a high level (260 circuits), with a significant part of industrial circuits (22%) and low volume production (8% of the total).

In 2005 fabrications in the very advanced technologies recently open (.25µ SiGe:C BiCMOS and 90nm CMOS from STMicroelectronics) will take place. New processes for MEMS will be available. IPs access will be developed and cooperation with other similar services extended to support a large number of various advanced technologies.
Figure 3-2 – Distribution of circuits per technology (4 last years)

Figure 3-3 – Distribution of circuits depending on the purpose (2 last years)
Figure 3-4  SIA Roadmap and CMP technologies

Size in microns

Feature size, 1983 - 2010

Industry (SIA where available)

CMP
## Institutions

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Total in 2004: 14 technologies 37 runs 170 35 55 260 circuits

Table 3-2 (b) – CMP runs in 2004

**CMP runs total since 1981: 526 runs / 50 Technologies**

4,466 circuits: 2,363 Research circuits / 1,378 Educational circuits / 725 Industrial circuits
CERTIFICATION

N° QUAL/2000/14731

La Système Qualité adopté par :
The Quality System developed by :

CMP

pour les activités suivantes :
for the following activities :

FABRICATION DE CIRCUITS INTEGRES ET DE MICRO-SYSTEMES
EN PROTOTYPES ET PETITS VOLUMES POUR LES UNIVERSITES,
LABORATOIRES DE RECHERCHE ET SOCIETES INDUSTRIELLES
FRANCAISES ET ETRANGERES.

MANUFACTURING OF INTEGRATED CIRCUITS AND MICROSYSTEMS
IN PROTOTYPES AND SMALL VOLUMES FOR UNIVERSITIES, RESEARCH
LABORATORIES AND FRENCH AND FOREIGN INDUSTRIAL COMPANIES.

exercées sur le(s) site(s) suivant(s) :
carried out in the following location(s) :

45, avenue Felix Viallet F-38031 GRENOBLE CEDEX

a été évalué et jugé conforme aux exigences de la norme :
has been assessed and found to conform to the requirements of the standard :

ISO 9002 (1994)

Le certificat correspondant a été délivré dans les conditions d’application fixées par AFAQ le :
The corresponding certificate has been delivered under AFAQ application rules on :

2000-07-06

2003-07-05

(année-mois-jour) (year-month-day)

Le Président du Comité de Certification
The President of the Certification Committee

Le Directeur Général d’AFAQ
The Managing Director of AFAQ

Le Représentant de l’Entreprise
On Behalf of the Firm

A. PIGEONNIER

O. PEYRAT

B. COURTOIS
### 4 - Resources

#### 4-1 Human resources

#### 4-1.1 Members of the Laboratory

Table 4-1 lists researchers, engineers and clerical staff involved in the TIMA Laboratory throughout 2004 and Table 4-1 points out researchers currently on secondment to French companies. The researchers working in companies or abroad, but enrolled for a thesis in the TIMA Laboratory are respectively listed in Table 4-1 and last but not least Table 4-1 4 and Table 4-1 5 list researchers (visitors and trainees) who stayed in the Laboratory for a while.

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<td>Libor - Contracted Researcher</td>
<td></td>
</tr>
<tr>
<td>SALEH</td>
<td>Susi - Ph.D. student</td>
<td></td>
</tr>
<tr>
<td>SALIZZONI</td>
<td>Marie-Christine - Contracted Accountant</td>
<td></td>
</tr>
<tr>
<td>SARMENTO</td>
<td>Adriano - Ph.D. student</td>
<td></td>
</tr>
<tr>
<td>SASONGKO</td>
<td>Arif - Ph.D. student</td>
<td></td>
</tr>
<tr>
<td>SCHAUNER</td>
<td>Isabelle - Contracted Secretary</td>
<td></td>
</tr>
<tr>
<td>SCHMALTZ</td>
<td>Julien - Ph.D. student</td>
<td></td>
</tr>
<tr>
<td>SENOUCI</td>
<td>Benaoumer - Ph.D. student</td>
<td></td>
</tr>
<tr>
<td>SICARD</td>
<td>Gilles - Associate Professor - UJF/UFR Physique</td>
<td></td>
</tr>
<tr>
<td>SIMEU</td>
<td>Emmanuel - Associate Professor - UJF/ISTG</td>
<td></td>
</tr>
<tr>
<td>SIRIANNI</td>
<td>Antoine - Ph.D. student</td>
<td></td>
</tr>
<tr>
<td>SLIMANI</td>
<td>Kamel - Ph.D. student</td>
<td></td>
</tr>
</tbody>
</table>
### Members of the Laboratory (for 2004)

<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Country</th>
</tr>
</thead>
<tbody>
<tr>
<td>AST = «Agent des Services Techniques»</td>
<td>Lucie</td>
<td>AST - UJF/ISTG</td>
</tr>
<tr>
<td>IR = «Ingénieur de Recherche»</td>
<td>Kholdoun</td>
<td>IE – CNRS</td>
</tr>
<tr>
<td>DR = «Directeur de Recherche»</td>
<td>Pierre</td>
<td>Ph.D. student</td>
</tr>
<tr>
<td>CR = «Chargé de Recherche»</td>
<td>Raoul</td>
<td>CR – CNRS</td>
</tr>
<tr>
<td>IE = «Ingénieur d’Etudes»</td>
<td>Gerard</td>
<td>IE – CNRS</td>
</tr>
<tr>
<td>CIFRE = Support from ANRT for Industry-University cooperation</td>
<td>Sung Joo</td>
<td>Contracted Researcher</td>
</tr>
<tr>
<td>EN = «Attaché Temporaire d’Enseignement et de Recherche»</td>
<td>Mohamed Wassim</td>
<td>Ph.D. student</td>
</tr>
<tr>
<td>NICOLAIDIS</td>
<td>Mihail</td>
<td>DR - CNRS</td>
</tr>
<tr>
<td>IROC Technologies, Grenoble, France</td>
<td>Amel</td>
<td>Ph.D. student</td>
</tr>
</tbody>
</table>

### Member on secondment (for 2004)

<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Country</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAUCHETEUX</td>
<td>Damien</td>
<td>CEA-LETI, Grenoble, France</td>
</tr>
<tr>
<td>GOULIER</td>
<td>Julien</td>
<td>STMicroelectronics, Meylan, France</td>
</tr>
</tbody>
</table>

### Thesis prepared in companies or labs with TIMA advisor (for 2004)

<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Country</th>
<th>Duration</th>
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</thead>
<tbody>
<tr>
<td>BACIVAROV</td>
<td>Ioan</td>
<td>Romania</td>
<td>2 weeks</td>
</tr>
<tr>
<td>JEMAI</td>
<td>Abderrazak</td>
<td>Tunisia</td>
<td>3 weeks</td>
</tr>
<tr>
<td>KADLEC</td>
<td>Frantisek</td>
<td>Czech Republic</td>
<td>1 week</td>
</tr>
<tr>
<td>MA</td>
<td>Wei</td>
<td>China</td>
<td>6 months</td>
</tr>
<tr>
<td>MOREIRA</td>
<td>Luiz Carlos</td>
<td>Brazil</td>
<td>1 week</td>
</tr>
<tr>
<td>OLIVER</td>
<td>Juan Pablo</td>
<td>Uruguay</td>
<td>3 months</td>
</tr>
<tr>
<td>RENCZ</td>
<td>Marta</td>
<td>Hungary</td>
<td>2 months</td>
</tr>
<tr>
<td>SZEKELY</td>
<td>Vladimir</td>
<td>Hungary</td>
<td>1 week</td>
</tr>
<tr>
<td>TENHUNEN</td>
<td>Hannu</td>
<td>Finland</td>
<td>4 months</td>
</tr>
<tr>
<td>WONG</td>
<td>Man</td>
<td>Hong Kong</td>
<td>3 weeks</td>
</tr>
<tr>
<td>ZIADE</td>
<td>Haissam</td>
<td>Lebanon</td>
<td>1 week</td>
</tr>
</tbody>
</table>

### Visitors (for 2004)

<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Country</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABOULFADL</td>
<td>Driss</td>
<td>Morocco</td>
<td>2 months</td>
</tr>
<tr>
<td>AKKARI</td>
<td>Samir</td>
<td>Tunisia</td>
<td>1 month</td>
</tr>
<tr>
<td>ANNETTE</td>
<td>Michel</td>
<td>France</td>
<td>3 months</td>
</tr>
<tr>
<td>BEN ALAYA</td>
<td>Skander</td>
<td>Tunisia</td>
<td>4 months</td>
</tr>
<tr>
<td>BIONDI</td>
<td>Laetitia</td>
<td>France</td>
<td>1 month</td>
</tr>
<tr>
<td>BOUAZIZ</td>
<td>Ayman</td>
<td>Tunisia</td>
<td>2 months</td>
</tr>
<tr>
<td>CAPPELLETTI</td>
<td>Marcelo</td>
<td>Italy</td>
<td>6 months</td>
</tr>
<tr>
<td>Name</td>
<td>Country</td>
<td>Duration</td>
<td></td>
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<tr>
<td>-----------------------</td>
<td>---------</td>
<td>----------</td>
<td></td>
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<tr>
<td>CARTIER</td>
<td>France</td>
<td>4 months</td>
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<tr>
<td>CHO</td>
<td>Korea</td>
<td>6 months</td>
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<tr>
<td>CIMONNET</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>COLLE</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>COSTA</td>
<td>Brazil</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>DONG</td>
<td>China</td>
<td>3 months</td>
<td></td>
</tr>
<tr>
<td>DUBREUIL</td>
<td>France</td>
<td>3 months</td>
<td></td>
</tr>
<tr>
<td>DUMITRASCU</td>
<td>Romania</td>
<td>3 months</td>
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<tr>
<td>GAFSI</td>
<td>Tunisia</td>
<td>2 months</td>
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<tr>
<td>GIRIN</td>
<td>France</td>
<td>4.5 months</td>
<td></td>
</tr>
<tr>
<td>HADHRI</td>
<td>Tunisia</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>HUOT</td>
<td>France</td>
<td>3 months</td>
<td></td>
</tr>
<tr>
<td>KASPAR</td>
<td>Czech Republic</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>KHROUF</td>
<td>Tunisia</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>LATRECHE</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>LEJEUNE</td>
<td>France</td>
<td>5 months</td>
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<tr>
<td>LOPIN</td>
<td>France</td>
<td>7.5 months</td>
<td></td>
</tr>
<tr>
<td>M'RAD</td>
<td>Tunisia</td>
<td>2 months</td>
<td></td>
</tr>
<tr>
<td>MACHACEK</td>
<td>Czech Republic</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>MAINGOT</td>
<td>France</td>
<td>2.5 months</td>
<td></td>
</tr>
<tr>
<td>MARCHI</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>MEHADJI</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>MELIANE</td>
<td>Tunisia</td>
<td>2 months</td>
<td></td>
</tr>
<tr>
<td>NOTIN</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>OGIER</td>
<td>France</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>OULD MOHAMED YAHIA</td>
<td>Mauritania</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>OULLION</td>
<td>France</td>
<td>12 months</td>
<td></td>
</tr>
<tr>
<td>PESINA SIFUENTES</td>
<td>Mexico</td>
<td>4.5 months</td>
<td></td>
</tr>
<tr>
<td>POPOVICI</td>
<td>Romania</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>REDROVAN</td>
<td>United States</td>
<td>5 months</td>
<td></td>
</tr>
<tr>
<td>STEFANI</td>
<td>France</td>
<td>4.5 months</td>
<td></td>
</tr>
<tr>
<td>TELLIER</td>
<td>France</td>
<td>6 months</td>
<td></td>
</tr>
<tr>
<td>THIEMONGE</td>
<td>France</td>
<td>1 month</td>
<td></td>
</tr>
<tr>
<td>TIMOUYAS</td>
<td>Morocco</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>VINTU</td>
<td>Romania</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>WANG</td>
<td>China</td>
<td>6 months</td>
<td></td>
</tr>
<tr>
<td>ZEKERIYA</td>
<td>Turkey</td>
<td>4.5 months</td>
<td></td>
</tr>
</tbody>
</table>

Table 4-1-5 – Trainees (for 2004)
### 4-1.2 Biographies of staff members

<table>
<thead>
<tr>
<th>AMBLARD Paul</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Born on February 25th 1951, Married, 3 children, French</strong></td>
</tr>
<tr>
<td><strong>Position</strong>: Associate Professor (Maître de Conférences) at University Joseph Fourier, Grenoble, UFR Informatique et Mathématiques Appliquées</td>
</tr>
<tr>
<td><strong>Education</strong></td>
</tr>
<tr>
<td>1984</td>
</tr>
<tr>
<td>1972</td>
</tr>
<tr>
<td><strong>Past activities</strong></td>
</tr>
<tr>
<td>October 1997</td>
</tr>
<tr>
<td>From 1984</td>
</tr>
<tr>
<td>From 1973 to 1982</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>ANGHEL Lorena</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Born on December 9th 1972, Single, Romanian</strong></td>
</tr>
<tr>
<td><strong>Position</strong>: Associate Professor (Maître de Conférences) at ENSERG (Ecole Nationale Supérieure d'Electronique et Radioélectricité de Grenoble) since 2001</td>
</tr>
<tr>
<td><strong>Education</strong></td>
</tr>
<tr>
<td>1996</td>
</tr>
<tr>
<td>1997</td>
</tr>
<tr>
<td>2000</td>
</tr>
<tr>
<td><strong>Past activities</strong></td>
</tr>
<tr>
<td>Assistant Professor (ATER) at UJF (Université Joseph Fourier Grenoble) in 2000</td>
</tr>
<tr>
<td><strong>Research interests</strong></td>
</tr>
<tr>
<td>Test and On Line testing, Defect-tolerant techniques, computer architecture</td>
</tr>
<tr>
<td><strong>Current responsibilities</strong></td>
</tr>
<tr>
<td>Researcher in the « Qualification Group » group (QLF), ACI Venus Project Coordinator</td>
</tr>
<tr>
<td>General Chair of 11th International On Line Testing Symposium 2005 to be held July 6 to 8 in Saint Raphael, France</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BAIXAS Arnaud</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Born on March 22th 1978, single</strong></td>
</tr>
<tr>
<td><strong>Position</strong>: Microelectronic and Informatic R&amp;D Engineer in Concurrent Integrated Systems group of the TIMA laboratory (INPG).</td>
</tr>
<tr>
<td><strong>Education</strong></td>
</tr>
<tr>
<td>2002</td>
</tr>
<tr>
<td>2001</td>
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</tbody>
</table>
BASROUR Skandar

Born on August 24th 1964, Married, two children, Italian and Tunisian

Position: Professor in Electronics and Microsystems at Ecole Polytechnique de l'Université de Grenoble (Polytech’G). Electrical Engineering Department (3I)

Education
1987-1990: PhD in Microelectronics – Université Joseph Fourier de Grenoble
1986-1987: DEA in Microelectronics – Université Joseph Fourier de Grenoble
1982-1986: Graduated from Ecole Normale Supérieure of Tunisia (Physics and Chemistry)

Past activities
2001: Assistant Professor in Electronics and Microsystems at the Université de Franche-Comté. (Topics Contribution to the development of the X ray LIGA technique in France. Development and improvement of the UV LIGA Techniques for the realization of original Microsystems)
1991-992: Postdoctoral situation at the Laboratoire de Microstructures et Microélectronique CNRS – Bagneux (Topics: Fabrication and characterization of submicron gated TEGFET’s)

BORRIONE Dominique

Born on February 20th 1950, 2 children, French

Position: Professor at Université Joseph Fourier, Grenoble

Education
1981: Doctorat d’Etat in Computer Science, University of Grenoble
1976: PhD in Computer Science, University of Grenoble
1971: DEA in Computer Science, University of Grenoble
1970: B. S. in Applied Mathematics, Aix-Marseille University

Past activities
Director of the ARTEMIS Laboratory (1991-1995)

Current responsibilities
Leader of the Verification and Modeling of Digital Systems Group

Miscellaneous
* Has served in many Conference and Workshop Committees
* IFIP Silver Core

BRECHET Nicolas

Born on February 26th 1983, single, French

Position: database administrator at CMP

Education
2001-2003: DUT (University Degree in Technology) in Computer Science, IUT 2, Grenoble
Since 2003: DEST in Network and Communications, CNAM, Grenoble
<table>
<thead>
<tr>
<th><strong>CESARIO OLIVEIRA Wander</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Born on August 17th 1968, Married, 2 children, Brazilian</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Position</strong> : Researcher with TIMA</td>
<td></td>
</tr>
<tr>
<td><strong>Education</strong></td>
<td></td>
</tr>
<tr>
<td>1999  Ph. D. Degree - &quot;Microeletronics&quot; – INPG</td>
<td></td>
</tr>
<tr>
<td>1994  Master Degree - &quot;Microeletronics Engineer&quot; – Escola Politécnica da Universidade de São Paulo</td>
<td></td>
</tr>
<tr>
<td><strong>Current responsibilities</strong></td>
<td></td>
</tr>
<tr>
<td>Member of the System Level Synthesis Group</td>
<td></td>
</tr>
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</table>

<table>
<thead>
<tr>
<th><strong>CHARLOT Benoît</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Born on June 6th 1972, Married, 2 children, French</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Position</strong> : Chargé de Recherche CNRS</td>
<td></td>
</tr>
<tr>
<td><strong>Education</strong></td>
<td></td>
</tr>
<tr>
<td>2001  Ph.D. in microelectronics, Institut National Polytechnique de Grenoble</td>
<td></td>
</tr>
<tr>
<td>1996  DEA, Optics, Optoelectronics and Microwaves, Institut National Polytechnique de Grenoble</td>
<td></td>
</tr>
<tr>
<td>1995  Maîtrise degree in Semiconductor Science, University of Montpellier</td>
<td></td>
</tr>
<tr>
<td>1990  Baccalauréat degree in mathematics and mechanical engineering</td>
<td></td>
</tr>
<tr>
<td><strong>Current responsibilities</strong></td>
<td></td>
</tr>
<tr>
<td>- Member of the Micro and Nano Systems (MNS) group</td>
<td></td>
</tr>
<tr>
<td>- Technical responsible since 1999 for the MEMS prototyping service at CMP</td>
<td></td>
</tr>
<tr>
<td>- Responsible for several European research project</td>
<td></td>
</tr>
<tr>
<td>- In charge of different research projects such as the MEMS Fingerprint sensor, active biochip and energy scavenging for autonomous microsystems projects</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>CHEVROT Frederic</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Born on August 17th 1976, Single, French</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Position</strong> : Contracted technician with TIMA Laboratory since March 2003</td>
<td></td>
</tr>
<tr>
<td><strong>Education</strong></td>
<td></td>
</tr>
<tr>
<td>2001  IUP MIAGE (Méthodes Informatiques Appliquées à la Gestion d'Entreprise), UFR IMA : (Grenoble)</td>
<td></td>
</tr>
<tr>
<td>1998  DEUG Technologie Industrielle, Université Joseph Fourrier.</td>
<td></td>
</tr>
<tr>
<td>1995  BAC S Tec</td>
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</tr>
<tr>
<td><strong>Current responsibilities</strong></td>
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</tr>
<tr>
<td>Informatic technician</td>
<td></td>
</tr>
</tbody>
</table>
COLIN Sébastien
Born July 4th 1973, Single, French

Position: Contractual technician with CMP since August 1996

Education
1995: DUT in Electrical Engineering and Industrial Computer Science, Electronics option, at I.U.T. 1, Grenoble
1992: Baccalaureat degree in Mathematics and Technics

Current responsibilities
Data preparation ICs at CMP

COURTOIS Bernard
Born April 17th 1948, Married, 2 children, French

Position: Directeur de Recherches CNRS

Education
1981 - Docteur d'Etat degree
1976 - Doctor-Engineer degree
1973 - Engineer degree
1970 - 1973 National School for Informatics and Applied Mathematics in Grenoble
1967 - 1970 Mathematics in Paris
1968 - Baccalaureat degree – Philosophy
1967 - Baccalaureat degree – Mathematics

Current responsibilities
Director of TIMA Laboratory
Director of CMP Service

Miscellaneous
Has authored or co-authored many scientific papers
Has served in many Committees of Conferences & Workshops
Has served as a reviewer of research proposals to CEC, NATO, NSF, SERC
Doctor Honoris Causa of the Technical University of BUDAPEST
IEEE Golden Core

DELORI Hubert
Born on December 26th 1946, Married, 5 children, French

Position: "Ingénieur de Recherche 1ère classe" at CNRS (Centre National de la Recherche Scientifique)

Education
1970 Engineer degree from Ecole Centrale de Lyon.
1967-1970 Engineer studies at Ecole Centrale de Lyon, Ecully
1964-1967 Mathematiques Supérieures & Mathématiques Spéciales, Lycée Janson de Sailly, Paris
1964 Baccalaureat degree - Mathematics, Lycée Claude Bernard, Paris

Past activities
- 79 - 80 : Complementary studying in System Programming at "Institut de Programmation de Grenoble" (1 year).
- 78 - 79 : Engineer at ICARE (Informatique Communale Alpes Rhône) at the town hall of Saint Etienne: operating responsible of all the informatic applications.
- 75 - 78 : Education of physically handicapped young people for social re-insertion at Association IMC Rhone Alpes, Lyon.
- 73 - 75 : Engineer statistician at "Cabinet Roland Olivier", Paris and Algiers: setting up statistical method, based on aerial pictures, to realize a national inquiry of ground occupation for the Agriculture Ministry of Algeria. Experimenting this method by real enquiries in selected regions.
- 72 - 73 : Teaching in Mathematics and Statistics in Algiers, Algeria, as for the cooperation in place of the military service.
- 70 - 71 : Analysis and programming at IBM, Corbeil-Essonnes

**Current responsibilities**
Quality management, coordination, and general information of the CMP Service (Circuits Multi Projets: National Service for manufacturing integrated circuits for Universities, Research Laboratories and Industrial Companies).

---

**DI PENDINA Grégory**

Born on August 11th 1979, Single, French

**Position:** Contractual technician with CMP since November 1999

**Education**
2003: Maitrise in Electronics (DEST électronique)
2001: Licence Ingénierie Electrique, UJF of Grenoble
1999: UT degree (Electrical Engineering and Digital Technology) option: Electrotechnics, UJF of Grenoble, IUT 1
1997: TI Baccalauréat diploma, in Electrotechnics

---

**DUMONT Sophie**

Born on March 7th 1978, Single, French

**Position:** Engineer in Microelectronic, working on asynchronous circuits Back End

**Education**
2003: Master degree in Analog and Digital Integrated System Design (DESS CSINA) at the University of Grenoble

---

**EYRAUD Sylvaine**

Born on March 23rd 1970, Married, 2 children, French

**Position:** Contractual technician with CMP since February 1993

**Education**
1994: "Diplôme d'Études Supérieures Techniques d'informatique d'entreprises" (informatics for companies)
1991: DUT in Computer Sciences
1989: Baccalauréat degree in Mathematics and Natural Sciences

**Current responsibilities**
Manufacturing run's data management
### FESQUET Laurent

Born on May 10th 1969, Married, 2 children, French

**Position**: Associate Professor (Maître de conférence) at ENSERG (Ecole Nationale Supérieure d’Électronique et Radioélectricité de Grenoble)

**Education**
- 1997: PhD in Electronics - UPS Toulouse
- 1994: Agrégation (teaching degree) in applied physics, Ecole Normale Supérieure de Cachan
- 1993: Engineering degree in Physics, Ecole Nationale Supérieure de Physique de Strasbourg
- 1993: DEA degree in Photonics - ULP Strasbourg

**Past activities**
- 1998-1999: Researcher at LAAS-CNRS (Laboratoire d'Analyse et d'Architecture des Systèmes) in Toulouse
- 1998-1999: Teacher in charge of physics, electrotechnics and power electronics courses in BTS (technician degree) Brive
- 1996-1998: Teacher at Paul Sabatier University - Toulouse
- 1995-1999: Teacher in electronics at Sup'Aéro (Ecole Nationale Supérieure de l'Aéronautique et de l'Espace)
- 1994-1995: Teacher at the French Navy instruction center in Toulon in charge of electronics and inertial navigation systems lectures

**Current responsibilities**
- Researcher in the « Concurrent Integrated Systems » group (CIS)
- Chair of the french IEEE-SSCS Chapter (Solid-State Circuit Society)

**Miscellaneous**
- Has organized in 1997 a workshop on New Technologies, Interconnects and Communications in Distributed and Parallel Systems in Toulouse (France)
- Has organized in 2000 the AciD-workshop in Grenoble (France)
- Has organized in 2002 the Summer School on Asynchronous Circuit Design in Grenoble (France)

### FILLION Sébastien

Born on October 14th 1974, Married, French

**Position**: Contractual engineer with TIMA Laboratory since August 2000

**Education**
- 2000: MST ESI (Maîtrise des Sciences et Techniques Experts en Système Informatique) Université Joseph Fourier (Grenoble)
- 1997: DEUG Technologie Industrielle, Université Joseph Fourrier.

**Current responsibilities**
- System Engineer at TIMA Laboratory

### GASCARD Eric

Born on October 27th 1973, Single, French

**Position**: Associate Professor with TIMA Laboratory since September 1st, 2003

**Education**
- Ph.D. in Computer Science from University Provence (Aix-Marseille 1), France, 3 July 2002

**Current responsibilities**
- Associate Professor University Joseph Fourier (Grenoble 1), UFR, Polytech’Grenoble, France, since September 1, 2003
GUYOT Alain

Born on September 11\textsuperscript{th} 1945, Married, 3 children, French

**Position**: Associate Professor (Maître de Conférences) at ENSIMAG (Ecole Nationale Supérieure d’Informatique et de Mathématiques Appliquées de Grenoble) since 1986

**Education**
- 1991 - “Habilitation à diriger des Recherches”
- 1975 - Ph.D in Computer Science from Grenoble University
- 1970 - Master in Computer Science from Grenoble University

**Past activities**
Teacher in computer architecture and VLSI design mainly at ENSIMAG and Grenoble University since 1971
Visiting scholar or invited professor with the CSL group in Stanford University (M.Flynn), Microelectronic group in Telecom University, Paris (Prof. Jutand) and LEG- EPFL in Lausanne (Prof. M. Declercq)
Author or co-author of more than 50 scientific publications in Journals, Conference Proceedings, or Research Reports
Served as a reviewer for ESSCIRC, VLSI, Computer Arithmetic, EUROASIC, IEEE TC, CAVE and other conferences

JERRAYA Ahmed Amine

Born on August 1\textsuperscript{st} 1955, Married, 2 children, French and Tunisian

**Position**: Research director with CNRS, the French National Center for Scientific Research.
Section : Computer Science

**Education**
- 1989: Thèse d'Etat degree, University of Grenoble, France
- 1983: Thèse Docteur Ingenieur (PhD), University of Grenoble, France
- 1980: Dipl. Ing. Computer Science, University of Tunis, Tunisia

**Professional Experience**
European Representative in DAC Executive Committee, 2002 – 2005
Member of scientific staff, Bell-Northern Research Ltd., Ottawa, Ontario, Canada, March 1990-April 1991
General Chair, DATE 2001

**Awards and Successful CAD projects**
Co-founder of the International Seminar on Application-Specific Multi-processor SoC “MPSOC”
Best paper award ED&TC 1995, HW/SW cosimulation
Award of President de la Republique in Tunisia, 1980, highest computer science engineer degree

**Publications**
More than 200 international publications: [http://tima.imag.fr/SLS/publications_sls.html](http://tima.imag.fr/SLS/publications_sls.html)

Régis LEVEUGLE

Born on December 4\textsuperscript{th} 1964, Married, 1 child, French

**Position**: Professor at INPG (ENSERG), joined TIMA in December 1999

**Education**
- 1987: Engineer Degree from ENSERG (INP Grenoble)
- 1987: DEA Degree in Microelectronics (Grenoble)
- 1990: PhD in Microelectronics (INP Grenoble)
- 1995: Habilitation à Diriger des Recherches (French National Degree for Research Supervising)

**Past activities**
Leader of the Design group in the CSI laboratory (INPG) between 1991 and 1999. Participation to six European projects
Director of Studies at the INPG Telecommunications Department between 2001 and 2003.

**Research interests**
Computer architecture, VLSI design methods, dependability analysis, fault-tolerant architectures, concurrent checking, test, logic implementations in nanotechnology.

**On-going research activities**
Project on the hardening of digital circuits and embedded systems by modification of high level hardware descriptions and/or operating system functions. Collaboration with Xilinx. Laboratory leader of the ACI-SI project MARS in collaboration with ENST (Paris, France), 2004-2007.
Scientific leader for TIMA of the DURACELL project on chip security (RNRT program), in collaboration with Gemplus, iRoC Technologies, Thalès and the CIS Group in TIMA, 2002-2005.
Project on circuit design based on nanoelectronic devices (SETs). Laboratory leader of the ACI project NANOSYS in collaboration with many French laboratories, 2004-2007.

**Miscellaneous**
Member of the scientific committee of the French national action on "Computer and security" (ACI Sécurité & Informatique).
Authored or co-authored more than 100 scientific papers in journals, books, conferences and workshops.
Served in more than 40 conference committees (in particular in 2004: Program Chair for the IEEE International On-Line Testing Symposium, Madeira, Portugal, 12-14 July).

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**MIR Salvador**

Born on September 21st, 1963, Married, 2 Children, Spanish

**Position**: Chargé de Recherche CNRS (French National Center for Scientific Research) since 2000

**Education**
1993: Ph.D. degree - Computer Science, University of Manchester, United Kingdom
1989: Master degree - Computer Science, University of Manchester, United Kingdom.
1987: Industrial Engineering degree - Electrical, Polytechnic University of Catalonia, Barcelona, Spain

**Past activities**
1998 - 2000 Contractual researcher at TIMA
1996 - 1997 Contractual researcher at Centro Nacional de Microelectrónica, Seville, Spain
1993 - 1995 Postdoctoral and contractual researcher at TIMA
1988 - 1993 M.Sc. and Ph.D. in the University of Manchester, UK,
1988 Teaching Assistant at Polytechnic University of Catalonia, Spain

**Current responsibilities**
Leader of the RMS Group at TIMA (Reliable Mixed-signal Systems) created in 2002

**Miscellaneous**
Has published over 100 scientific papers in international journals, conferences and workshops
Editor of two books on silicon microsystems
General chair of IMSTW’05, VLSI-SoC’06
Program co-chair of IMSTW’04
Local chair of WTW’05
Serves in the Program Committee of ETW, IMSTW, VLSI-SoC, EMT, IWASI
Regular reviewer for International Journals and Conferences
Member of IEEE, IEEE Computer Society and IEEE Circuits and Systems Society
Participation in the European projects SMART, JESSI-COMMON-FRAME, ARCHIMEDES, AMATIST, PROFIT, TECHNOBAT, PICS, NANOTEST
Award from Association of Industrial Engineers of Catalonia, Spain, to the best Work Graduation Dissertation in Industrial Engineering, Barcelona, 1988
OSTIER Pierre

Born on February 5th 1968, Single, 3 children, French

Position: Contractual Research Engineer with VDS

Education
1997 PhD in Computer Science, University of Grenoble, France.
1992 DEA in Computer Science, INPG, Grenoble, France.

Current responsibilities
Design and development of compilers for the vhdl language for formal verification.
Integration of formal tools for hardware verification and diagnosis in the Prevail environment.
System administration of VDS machines

PAILLOTIN Jean-François

Born on October 6th 1955, Single, French

Position: "Ingénieur de Recherche" National Education

Education
1981: DEA Computer Sciences - INP Grenoble
1980: Master Degree Computer Sciences - UJF Grenoble
1979: Licence Computer Sciences - UJF Grenoble
1978: Licence Telecommunications - Reims University

Past activities
LCS researcher, INP Grenoble
Assistant Teacher at IUT of Computer Sciences, Grenoble
Assistant Teacher at UJF.

Current responsibilities
Technical responsible since 1985 for the CMP (Circuits Multi Projets): national Service for Universities, Research Laboratories and Industry
AMS CUP runs, ST HCMOS8 runs and OMNIC runs responsible
ACMO (Agent Chargé de la Mise en Œuvre de l’hygiène et de la sécurité)

PERONNARD Paul

Born on May 12th 1980, single, french

Position: Technician

Education
2001-2004 DEST Electronique - CNAM Grenoble
2000-2001 Licence EEA - Université Joseph Fourier
1998-2000 DUT Genie Electrique et Informatique Industrielle - IUT Joseph Fourier
PETROT Frédéric
Born on September 14th 1966, Married, two children, French

Position: Professor in Computer Architecture at the École National Supérieure d'Informatique et de Mathématiques Appliquées of the Institut National Polytechnique de Grenoble (ENSIMAG/ INPG)

Education
1989-1994: PhD in Computer Science - Université Pierre et Marie Curie, Paris, France

REMOND Yann
Born on September 14th 1974, French

Position: Software engineer in TIMA Laboratory

Education
1998-2001: PhD in Computer Science - Université Joseph Fourier (Grenoble I).

RENANE Salim
Born on August 10th, 1974, Algerian

Position: Research Engineer in CIS group

Education
2001-2002 : DESS in microelectronics
2000 -2001 : DEA in signal processing

RENAUDIN Marc
Born on March 29th 1963, Married, 3 children, French

Position: Professor at INPG/Telecom, Grenoble, France

Education
1998 : HDR (Authorization to advise doctorate students) – INPG, France
1990 : PhD in Microelectronics and Signal Processing – INPG, France
1987 : Graduated Engineer and MSc in Signal Processing – INPG, France

Past activities
1990-1998: Assistant Professor, ENST (Graduate School of Telecommunications Engineering), Brest, France
1998: Visiting Professor, Computing Science Dept, Californian Inst. of Technology, Pasadena, USA

Current responsibilities
"Concurrent Integrated Systems" Research Group Leader
**Research interests & activities**

* **Publications:**
  Author and Co-author of 33 publications in Journals, 101 publications in Conferences, 10 Book's Chapters and 21 Invited Talks.

* **Project Management:**
  - Mica and Micabi projects on the design of a CISC 8 bit asynchronous microprocessor and its integration in a Contactless Smart Card IC using an on-chip antenna.
  - ASPRO project, "A Standard-Cell Q.D.I. 16-Bit RISC Asynchronous Microprocessor".
  - TAST project focused on the specification and development of a framework devoted to the design of asynchronous systems.
  - RNRT and MEDEA+ projects focused on the design of secure chips. Goals of this research is to evaluate the use of asynchronous technology to improve circuits' resistance against Timing, Power and Fault Attacks, especially crypto processors and coprocessors such as DES and AES.

* **Reviewer Role:**
  He serves as a reviewer for IEEE JSSC, Trans. on VLSI, Trans. on Computers, Micro, ASYNC, ESSCIRC, VLSI.

* **Conference Committee Membership:**
  He takes part as a member in the Program Committees of ASYNC, ESSCIRC and DATE.

* **Current Research Interests:**
  Include the design of secure chips, resistant against timing, power and fault attacks (especially crypto processors and coprocessors such as DES and AES). He is concurrently developing the TAST tool suite, a CAD framework devoted to the specification, verification and synthesis of asynchronous circuits.

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**RENZETTI Françoise**

Born on July 11th 1943, Married, 2 children, French

**Position:** Electronic publishing officer

**Education**

1979 Doctor degree in History of Science
1980 Certificat d'Aptitude aux fonctions de bibliothécaire
1994 Doctor degree in Communication

**Past activities**

Director of Médiathèque de l’Institut d’Informatique et de Mathématiques Appliquées de Grenoble (IMAG)

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**ROUSSEAU Frédéric**

Born on March 2nd 1967, Single, French

**Position:** Assistant Professor (Maître de conférences) at UJF (Joseph Fourier University), Grenoble

**Education**

1997 : Ph.D. in computer science from the University of Evry, France
1992 : DEA degree in Computer Science, INPG, Grenoble, France
1991 : DEA degree in Microelectronics, University Joseph Fourier,
1991 : Engineer degree, computer science and electrical engineering (3i), University Joseph Fourier, Grenoble, France,

**Past activities**

1996 – 1999 Teacher – Researcher at the engineer school of Marseille (ESIM), France in the computer science and electrical engineering department.

**Current responsibilities**

Researcher in « System Level Synthesis » group (SLS)
RUFER Libor

Born on July 4th 1951, Married, 1 Child, Czech

Position: Researcher / Expert in Microsystems and Test at the National Polytechnic Institute of Grenoble (INPG).

Education
1993: Diplôme d'Études Approfondies en Acoustique - Ecole Centrale de Lyon
1984: Ph.D. in Acoustics - Czech Technical University, Prague
1974: Engineer degree - Faculty of Electrical Engineering, Prague

Past activities
1994 - 2004: Associated Professor, Joseph Fourier University, Grenoble
1997 - 1999: Invited Researcher, Acoustics Laboratory of School for Building, Concordia University, Montreal, Canada
1992 - 1993: Invited Researcher, Centre Acoustique, Ecole Centrale de Lyon
1980: Research fellow, Acoustics Laboratory, Danish Technical University, Lyngby
1976 - 1993: Associated Professor, Czech Technical University, Prague

Current responsibilities
ECO-NET project leader (partners: Joseph Fourier University, Grenoble; Czech Technical University, Faculty of Electrical Engineering, Czech Republic; Academy of Science, Institute of Electrical Engineering, Slovak Republic), submitted.
PROCORE project leader (partners: Joseph Fourier University, Grenoble; City University, Hong Kong), 2005-2006. Local chair of the IEEE 'International Mixed-Signals Testing Workshop' (IMSTW), Cannes, France, 2005.
DUO – France project leader (partners: Joseph Fourier University, Grenoble; Hong Kong University of Science and Technology), 2003-2005.

Research interests:
MEMS-based sensors and actuators, electro-acoustic and electro-mechanical transducers and their application in acoustics and ultrasonics, associated measurement techniques, analogue and mixed-signal systems test.

SICARD Gilles

Born on July 7th 1970, Married, 1 child, French

Position: Associate Professor (Maître de conférence) at UJF (Joseph Fourier University), Grenoble

Education
1999 : PhD in Microelectronics, INPG.
1994 : DEA degree in Microelectronics, INPG.

Past activities
Contractual teacher (ATER) at ENSERG (Ecole Nationale Supérieure d'Electronique et Radioélectricité de Grenoble) and researcher at LIS Laboratory (Laboratoire des Images et des Signaux), Grenoble, 1999.

Current responsibilities
Researcher in « Concurrent Integrated Systems » group (CIS). His research interests analog circuits design, asynchronous circuits design, and imaging systems on a chip.

Miscellaneous
Has developed a smart image sensor in 1998. This analog retina contains an array of 64x64 pixels which performs three analog image processings in real time: Edge extraction, motion detection and a light adaptive system.
SIMEU Emmanuel

Born on December 25th 1959, Married, 3 children, French and Cameroonian

Position: Associate Professor at Ecole Polytechnique de l’Université de Grenoble (Polytech’G)

Education
1992 Ph.D in Automatic Control and System Theory, Institut National Polytechnique de Grenoble
1988 DEA degree in Automatic Control and Signal Processing, Institut National Polytechnique de Grenoble
1987 Engineer degree -Electrical- University of Casablanca (Morroco)

Current responsibilities
Member of the Reliable Mixed -signal Systems (RMS) Group

Past Activities
1992-1995: Associate Professor at ISAR (Institut Supérieur d'Automatique et de Robotique de Valence)
1988-1995: Researcher in LAG (Laboratoire d'Automatique de Grenoble)
1989-1992: Researcher in CNET-CNS Grenoble (SITAR Project)

Miscellaneous
Pedagogic responsibility in the department of industrial risk management of ISTG.
Courses and lectures on reliability, automatic control and applied mathematics in the Department of Polytech’Grenoble
Courses and lectures of automatic control Maîtrise  EEA  of Joseph Fourier University
Courses and lectures of automatic control, IUP of Joseph Fourier University
Program Committee member of IEEE International On-line Testing Symposium

TORKI Kholdoun

Born on February 21th 1961, Married, 2 children, Tunisian

Position: Engineer at CNRS since 1994

Education
1990 : Ph.D. degree, INPG, Grenoble
1986 : DEA microelectronics, INPG, Grenoble
1985 : "Maîtrise" degree in physics and electronics, University of Constantine

Past activities
Contractual engineer with CMP-TIMA Laboratory since June 1990
Contractual researcher with TIMA Laboratory (1986-1990)

Current responsibilities
Engineering Manager of CMP
Project Coordinator for PhD students exchange between TIMA Laboratory and the University of Monastir (Tunisia)
Supervising PhD students at TIMA Laboratory
VELAZCO Raoul

Born on December 14th 1952, Married, 1 child, French

Position: “Director of Researches” at CNRS (French Research Agency); Researcher with TIMA laboratory (Techniques of the Informatics and Microelectronics for computer architecture) since 1996

Education
1990 Dr. ès Sciences from INPG
1982 Ph D degree from Polytechnique Institut of Grenoble (INPG)
1979 Engineer degree
1976-1979 National School for Informatics and Applied Mathematics (ENSiMAG) Grenoble

Current Responsibilities
Leader of the “Qualification of Circuits” research group of TIMA laboratory
Member of the Scientific Committee of TIMA since 1998
Responsible of the design of a flight experiment included on board a scientific satellite: NASA Project LWS/SET (Living With a Star / Space Environment Testbed)
Expert Radiation au CNRS

Miscellaneous
General Chair of RADECS 2001 (Grenoble, France).
General Chairman of LATW 2002 (Montevideo, Uruguay).
Program Chair of DFT 2003 (Boston, U.S.A.).
General Chair of EWRHE 2004 (Villard-de-Lans, France)
General Chair of DFT 2004 (Cannes, France)

VITRY Gérard

Born on August 5th 1947, Married, 2 children, French

Position: "Ingénieur d'Etudes" at CNRS

Education
1973: "Programmeur Expert en Systèmes Informatiques" - Grenoble

Current responsibilities
System Engineer
Web administrator

YOO Sungjoo

Born on March 10th 1969, Married, 2 children, Korean

Position: Researcher at TIMA

Education

Current responsibilities
Modeling, implementation and simulation of hardware/software interface for system-on-chip
ZERGAINOH Nacer-Eddine

Born on May 18th 1969, Single, French and Algerian

**Position**: Associate Professor (Maître de Conférences) in Computer Engineering and architecture, Ecole Polytechnique (Polytech’G), Joseph Fourier University, Grenoble

**Education**
- 1984 Baccalaureat degree, Mathematics
- 1989 Engineer degree, Telecommunication, National School of telecommunication
- 1990 DEA degree, Signal Processing & Control, Signals and Systems Laboratory, Supélec.
- 1996 PhD degree, Computer Engineering, INRIA & Paris XI University, France

Methods and tools-aided design of reactive systems. Distributed Real-time Operating System for an embedded obstacle detection system.

**Past activities**
- Participated to the European Esprit-Polyglot Project.
- Participated to the European Prometheus Project.
- Teacher in telecom and computer (ESIGITEL, EPITA, Paris XIII University).
- Contractual engineer of research with LIMSI-CNRS Laboratory Gif/Yvette.

**Current responsibilities**
- Researcher in System Level Synthesis Group of TIMA Laboratory.
- His research interests include system-level design and CAD issues, multiprocessor architectures modeling, and real-time operating system. Currently, his research focuses on multiprocessor architectures exploration, RTOS, and interface Synthesis.

**Miscellaneous**
- Has authored or co-authored several scientific papers.
- Has served in many program committees of conferences and workshops.
- Has served as a reviewer of many journals and conferences.
4-1.3 Research interests of Ph. D. candidates

- **ACHOURI, Mohamed Nadir**
  - Fault tolerance techniques for memories
  - Completed in 2004
  - Previous degrees: DEA in microelectronics (2000), INPG, Grenoble, France

- **AESCHLIMANN, Fabien**
  - Irregular sampling and asynchronous circuits
  - 2005 (expected date of defense)
  - Previous degrees: Master degree in signal, image, speech processing and telecom at INPG, Grenoble, France (June 2002); Agregation (teaching degree) in electrical engineering at “Ecole Normale Supérieure de Cachan”, France (June 2001)

- **ALEXANDRESCU, Marian Dan**
  - SEU, Transient Fault Simulation, Accelerated Fault Simulation Algorithms
  - 2005 (expected date of defense)
  - Previous degrees: DEA Microélectronique, UJF Grenoble

- **AL SAMMANE, Ghiath**
  - Formal verification of a mixed HW/SW systems
  - 2005 (expected date of defense)
  - Previous degrees: Master in Microelectronics (2001)

- **AMMAR, Yasser**
  - Integration of micro generator of energy for autonomous systems
  - 2006 (expected date of defense)
  - Previous degrees: DEA Microelectronics (UJF-Grenoble)

- **AMMARI, Abdelaziz**
  - Safety analysis and hardening of mixed integrated circuits in high-level language
  - 2006 (expected date of defense)
  - Previous degrees: DEA degree, INSA Lyon, France (2002)

- **ATAT, Youssef**
  - Component-based design of DSP specific SOC
  - 2006 (expected date of defense)
  - Previous degrees: Master Electronic, INSA, Rennes, France (2003)

- **BACIVAROV, Iuliana**
  - Performance evaluation and optimisation of HW/SW interfaces in MP SoC design
  - 2006 (expected date of defense)
  - Previous degrees: Electronics Eng. degree from Polytechnic University of Bucharest, Romania (2002); MS degree in Microelectronics from University Joseph Fourier, Grenoble, France (2003)

- **BLAMPEY, Alexandre**
  - Fast prototyping method using a hardware reconfigurable emulator
  - 2006 (expected date of defense)
  - Previous degrees: Supelec engineering degree (2003); Microelectronic DEA (2003)

- **BONACIU, Marius**
  - Flexible and scalable algorithm/architecture platform for MP-SoC design of the MPEG4-DivX video encoding technology
  - 2006 (expected date of defense)
  - Previous degrees: Dispense of Master, INPG Grenoble, France (2003); Engineer in Computer Sciences and Architectures, Faculty of Electrotechnics and Informatics, University of Oradea, Romania (1996-2001); Analyst assistant programmer in informatic, “Aurel Lazăr” High School, Oradea, Romania (1992-1996)

- **BOUBEKEUR, Menouer**
  - Formal verification of asynchronous circuits
  - Completed in 2004
  - Previous degrees: DEA informatics, systems and communication (2000), UJF, Grenoble, France

- **BOUCHHIMA, Aimen**
  - Software modeling at different abstraction levels for HW/SW SoC validation
  - 2005 (expected date of defense)
  - Previous degrees: DEA Microelectronic (2002)
• BOUESSE, Fraidy
  o Integrated cryptography
  o 2005 (expected date of defense)
  o Previous degrees: Master degree in Microelectronics from the University of Grenoble

• BOUNCEUR, Ahcene
  o Generation and optimization of test vectors for analogue, mixed-signal and RF components
  o 2006 (expected date of defense)
  o Previous degrees: DEA degree in Operational Research, Combinatorial and Optimization (2003);
    Ingineer degree in Operational Research (2002)

• BREGIER, Vivian
  o Logical optimisation of quasi-delay insensitive circuits
  o 2006 (expected date of defense)
  o Previous degrees: Dea d'Informatique Fondamentale, ENS Lyon

• BUHRIG, Aurélien
  o Optimization of the power consumption of wireless ad-hoc sensor network nodes
  o 2007 expected date of defense)
  o Previous degrees: engineer degree in telecommunication at the telecom department (INPG), Grenoble,
    in 2004; master in micro-nano electronic at the Joseph Fourier University (UJF), Grenoble, in 2004

• CAUCHETEUX, Damien
  o Architecture study and design of asynchronous mixed circuits: application to low consumption and
    contactless systems
  o 2005 (expected date of defense)
  o Previous degrees: Engineering degree in Electronics from the "Ecole Nationale Superieure d'Electronique et
    Radioelectricite de Grenoble" (2002); Master degree in Microelectronics from the University of Grenoble
    (2002)

• CIONTU, Florin
  o Modeling of molecular nano-bio interfaces
  o 2006 (expected date of defense)
  o Previous degrees: Engineer Diploma - Computer Science, Politehnica University of Bucharest (2003)

• DHAYNI, Achraf
  o BIST techniques for microsystems
  o 2006 (expected date of defense)
  o Previous degrees: DEA Signal-Image-Parole-Telecom (ENSERG); Engineering in Communications and
    electronics (BAU)

• DOMINGUES, Christian
  o Design of micromachines ultrasonics transducers
  o 2005 (expected date of defense)
  o Previous degrees: DEA in microelectronics (2001); Master's degree in electronic, engeneering & control
    (2000); Bachelor's degree in electronic, engeneering & control (1999)

• DZIRI, Mohamed
  o Modèles de représentations pour la composition d'objets logiciels/matériels dans le cadre d'un flot de
    conception flexible
  o Completed in 2004
  o Previous degrees: DEA (2000)

• FAURE, Fabien
  o Study of radiation effects on complex VLSI devices
  o 2005 (expected date of defense)
  o Previous degrees: DEA (2002)

• FIANDINO, Maxime
  o Definition of a new way to integrate a network of thousand heterogenous processors on one single chip
  o 2006 (expected date of defense)
  o Previous degrees: Research Master in "Components and Systems for Data Processing" (DEA CSTI);
    Engeneer in computer science (ISIMA - France)

• FOLCO, Bertrand
  o Methodology of automated hardening using asynchronous logic
  o 2006 (expected date of defense)
  o Previous degrees: Master degree (DEA) in microelectronics, Grenoble (2002-2003)
- **FOUCARD, Gilles**
  - Radiation hardening of applications designed for complex SRAM based FPGA
  - 2008 (expected date of defense)
  - Previous degrees: Master Pro Conception des systèmes intégrés numériques et analogiques, INPG (2003-04); Maîtrise Electronique, Electrotechnique et Automatique UFR de Physique, UJF, Grenoble (2002-03); Licence Ingénierie Electrique, UFR de Physique, UJF, Grenoble (2001-02); DUT Génie Electrique et Informatique Industrielle IUT1, UJF, Grenoble (1999-01)

- **FRAGOSO, Leonardo-Joao**
  - Asynchronous circuits design
  - 2005 (expected date of defense)
  - Previous degrees: Master in Computer Science (2001)

- **GALY, Nicolas**
  - System on a chip for signal processing of a fingerprint sensor
  - 2005 (expected date of defense)
  - Previous degrees: Engineering degree (2001) in the computerized systems architecture field; Postgraduate certificate (“Diplome d'Etudes Approfondies”) in signal and image processing (2001)

- **GRASSET, Arnaud**
  - Automatic generation of architectures for multiprocessor system-on-chip
  - 2005 (expected date of defense)

- **HADJIAT, Karim**
  - Predictive evaluation of the reliability for a digital integrated circuit
  - 2005 (expected date of defense)
  - Previous degrees: Engineer (1999)

- **HAN, San II**
  - New message passing architecture for 100+ MPSoC
  - 2005 (expected date of defense)
  - Previous degrees: Master Science in electrical engineering from seoul national university

- **HUNSINGER, Frédéric**
  - Global validation method for system on chip
  - 2005 (expected date of defense)
  - Previous degrees: Master degree in Microelectronics (DEA) at UJF Grenoble

- **KHERIJI, Rabeb**
  - Structural testing of radio-frequency integrated circuits
  - 2005 (expected date of defense)
  - Previous degrees: master degree & engineer degree

- **KOCH-HOFER, Cedric**
  - Automatic synthesis of asynchronous circuits for GALS architectures (Globally Asynchronous Locally Synchronous) with TLM (Transaction Level Modeling) specifications in systemc
  - 2007 (expected date of defense)
  - Previous degrees: engineer degree in computer science at ENSIMAG (INPG) Grenoble (2004)

- **KOLONIS, Eleftherios**
  - CAD technics for nano-technologies
  - 2004 (expected date of defense)
  - Previous degrees: DEA in Microelectronics (2001); Engineer in Informatics (2000)

- **KRIAA, Lobna**
  - Modellisation and Validation of Heterogeneous systems
  - 2005 (expected date of defense)
  - Previous degrees: Master degree of Computer Sciences (Systems and Communications) at the University Joseph Fourier (UFR-IIMA), Grenoble, France. Diploma of engineer in Computer Sciences at the University of the Sciences of Tunis (FST), Tunisia

- **LABONNE, Estelle**
  - Design of a high dynamic range CMOS image sensor
  - 2006 (expected date of defense)
  - Previous degrees: DESS and DEA in Microelectronic
LAZZARI, Cristiano
- Development of techniques for automatic layout generation of hardening circuits
- 2007 (expected date of defense)
- Previous degrees: Master in Computer Science – Microelectronics, UFRGS - Universidade Federal do Rio Grande do Sul Porto Alegre/RS – Brazil (2003); Computer Science Graduation, URICER - Universidade Regional Integrada do Alto Uruguai e das Missões, Campus de Erechim/RS – Brazil (2001)

LIU, Miao
- Generation of verification environments for standard property specification languages
- 2006 (expected date of defense)
- Previous degrees: M.S. degree in Electrical Engineering, July 2000, Tsinghua University, Beijing, China; B.S. degree in Electrical Engineering, July 1998, Tsinghua University, Beijing, China

LIZARRAGUA, Livier
- Study and development of self-test techniques for CMOS imager pixels
- 2007 (expected date of defense)
- Previous degrees: Electronic engineer (Mexico), Master Research (DEA) Micro – Nano Electronic at UJF (Université Joseph Fourier), Grenoble

MARZENCKI, Marcin
- Design of integrated microgenerators for autonomous System on Chip applications
- 2006 (expected date of defense)
- Previous degrees: Master of Science of University of Science and Technology in Cracow, Poland

MONNET, Yannick
- Study and modelisation of secure circuits against non invasive attacks
- 2005 (expected date of defense)
- Previous degrees: Master degree in computer science, UJF Grenoble (2002)

NGUYEN, Hoang Nam
- Design for test of RF MEMS components and microwave acoustic devices
- 2007 (expected date of defense)
- Previous degrees: Master Instrumentation and Microelectronics at Henri Poincare University (Nancy 1) (2004)

OYAMADA, Marcio
- Performance Estimation of Embedded Software based on OS
- 2006 (expected date of defense)
- Previous degrees: MSc. Computer Science - UFRGS - Brazil ; BSc. Computer Science - UEM - Brazil

PANYASAK, Dhanistha
- Asynchronous design for low EMI
- Completed in 2004
- Previous degrees: Master in Microelectronics (DEA in microelectronics /INPG) 2000

PAVIOT, Yannick
- Hardware/Software trade off in implementation of multiprocessor system on chip communication
- Completed in 2004
- Previous degrees: Master (2002)

PETKOV, Ivan
- Physical Design of Multithreaded Systems on Chip & HDL Design Prototyping
- 2006 (expected date of defense)
- Previous degrees: MSc in Electronic engineering in Technical University - Sofia, Bulgaria (1996 – 200); PhD Student - Double doctor's degree between ECAD Laboratory - Sofia, Bulgaria and TIMA Laboratory Grenoble, France (2002)

PIERALISI, Lorenzo
- Modeling flexible Networks On-Chip
- 2006 (expected date of defense)
- Previous degrees: Electronics and Telecommunications High School obtained by ITIS “V.Volterra” in Ancona; Graduate at the University of Studies of Ancona in Electronic Engineering with a specialization in microelectronics, which is the equivalent of a Masters degree in microelectronics (2002)
- **PORTOLAN, Michele**
  - Dependable and secure design of an embedded system
  - 2006 (expected date of defense)
  - Previous degrees: "DEA en Microélectronique" with UJF Grenoble (September 2003); "Laurea in Ingegneria Elettronica, 110L/110" with Politecnico di Torino (September 2003) (Master Degree in Electronics and Computer Science); "Diplôme d'ingenieur" with the Département Télécommunications of the INPG (June 2003)

- **PRENAT, Guillaume**
  - Self-testable mixed-signal design in deep submicron technologies
  - 2005 (expected date of defense)
  - Previous degrees: Master of science, INPG, Grenoble, France (sept 2002); Engineer degree, enserg, INPG, Grenoble, France (July 2002)

- **QUARTANA, Jérôme**
  - Asynchronous IC, on-chip bus architectures & protocols, HW/SW interfaces
  - Completed in 2004
  - Previous degrees: Electronics Engineering Degree (2000) in Microelectronics, CPE Lyon, France; DEA degree in Microelectronics (2000), INSA Lyon, France

- **REZZAG, Amine**
  - Logic synthesis and testability of asynchronous circuits
  - Completed in 2004
  - Previous degrees: electronics engineer (1997), USTHB, Alger; computer engineer (1999), ENSIMAG, Grenoble; DEA degree in microelectronics, (2000), UJF-INPG, Grenoble

- **RIOS, David**
  - Low Power Microprocessor System
  - 2007 (expected date of defense)
  - Previous degrees: Master 2 micro and nano electronics (2004); Engineering degree in electronics (2003)

- **ROLINDEZ, Luis**
  - Study and development of analogue BIST techniques
  - 2006 (expected date of defense)
  - Previous degrees: Ingeniero Superior Industrial, Zaragoza, Spain (2003)

- **ROMAN, Cosmin**
  - Modeling and design of molecular nanosensors
  - 2005 (expected date of defense)
  - Previous degrees: Ms.C. Computer Science, Polytechnical University of Bucharest, Romania

- **SALEH, Susi**
  - Modélisation de phénomènes transitoires dans les technologies intégrées CMOS
  - 2005 (expected date of defense)
  - Previous degrees: Ingineer degree (1995)

- **SARMENTO, Adriano**
  - Design and validation of systems-on-chip
  - 2005 (expected date of defense)
  - Previous degrees: Bsc in Computer Science, Center of Informatics - Federal University of Pernambuco/Brazil (1997); Msc in Computer Science, Center of Informatics - Federal University of Pernambuco/Brazil (2000)

- **SASONGKO, Arif**
  - Conception d'architectures multiprocesseurs pour les systèmes monopuces
  - Completed in 2004
  - Previous degrees: Magister Teknik (2000)

- **SCHMALTZ, Julien**
  - Formal verification of SoCs using theorem proving techniques
  - 2005 (expected date of defense)
  - Previous degrees: DEA in Microelectronics, UJF Grenoble (2002); Engineering Degree, Polytech'Grenoble (2002)
- **SENOUCI, Benaoumeur**
  - Title: Automatisation of prototyping flot, based on reconfigurable plateform for the hardware/software interface validation
  - 2007 (expected date of defense)
  - **Previous degrees**: Master 2 Research micro and nano electronics

- **SIRIANNI, Antoine**
  - Analyse et amélioration des performances de circuits logiques asynchrones, une approche automatisée
  - Completed in 2004
  - **Previous degrees**: Ingineer (1995)

- **SLIMANI, Kamel**
  - Asynchronous microprocessors
  - Completed in 2004
  - **Previous degrees**: DEA in microelectronics UJF/INPG, Grenoble, France (2000)

- **TOMA, Diana**
  - Spécification et vérification formelle de systèmes sur une puce
  - 2005 (expected date of defense)
  - **Previous degrees**: DEA (2001)

- **VANHAUWAERT, Pierre**
  - Fault-injection based dependability analysis in FPGA-based Prototyping environment
  - 2007 (expected date of defense)
  - **Previous degrees**: DEA Microelectronics (2003); ENSERG engineer diploma (2003)

- **YOUSSEF, Mohamed**
  - Architectural exploration within the framework of Fonction/Architecture Co-design of Multiprocessor SOC
  - 2005 (expected date of defense)
  - **Previous degrees**: Master In computer Science (DEA), UFRIMA, Université Joseph Fourier (2002)

- **ZENATI, Amel**
  - Modeling and multiangle simulation of a SoC/ SoP including MEMS
  - 2005 (expected date of defense)
  - **Previous degrees**: DEA(Master degrees) in Microelectronique
4-2 TIMA network and computer equipment

4-2.1 Computer equipment

In order to continuously provide its users with services of an improved quality, TIMA computers department continuously renews its computer equipment. Today the computerised system of TIMA Laboratory consists of the following units:

| Servers: | 1 SunUltra5 (FTP). |
|          | 1 SunFire V60x (e-mail, file, backup). |
|          | 1 SunUltra1 (Development). |
|          | 1 Sun Ultra 1 (DNS cache, DHCP). |
|          | 1 Sparc20 (Printers). |
|          | 1 SunBlade 1000 (Development, Proxy HTTP). |
|          | 1 DELL Poweredge 2400 (WWW). |
|          | 1 Athlon 850 Mhz (SGBD, WWW-Intranet) |
| Devices: | 1 CD Recorder |
|          | 1 DLT 7000 Tape Drive |
|          | 1 DDS 3 Tape Drive |
|          | 2 HP LaserJet 4000N Printers |
|          | 1 HP LaserJet 4050N Printer |
|          | 1 HP LaserJet 4050N (Duplex) Printer |
|          | 1 HP LaserJet 4100 DTN Printer |
|          | 1 HP LaserJet 4200 DTN Printer |
|          | 4 Epson DeskJet Printers |
| Personal Computers: | TIMA provides a workstation for each user incoming in the laboratory, which corresponds to a continuous of 140 PCs. The PCs fleet is composed both of Pentium 166 Mhz and PIV 2.6 Ghz and notebooks for laboratory external jobs. All those computers have the same standard configuration with Windows 2000 or XP (few windows 98) office software and a permanent internet connection. Moreover, a computer can bee freely accessed to use the scanner and a colour jet-printer. There are about 140 PCs in use. |
| Micro computers MAC: | 1 mac G5 |
|            | 7 macs G4 |
|            | 1 mac G3 |
|            | 1 powerbook G4 |
4-2.2 Network equipment

In 2001 the TIMA Laboratory network has been entirely restructured. A router and a firewall appears at the head of the network to allow to segment the network. This router is an OMNICORE 5010 sold by ALCATEL. The firewall offered functionalities made the network more secure with filters of levels 3 and 4. To help the router, two switches OMNICORE 5010 sold by ALCATEL are installed at the head of each annex of the laboratory. This OMNICORE, like the router has functionalities allowing remote management and measurement on the network. That equipment alone is not enough to connect all the users to the network, that is why under that equipment there are some switches that allowing to provide enough ports for all the computers of TIMA Laboratory.

<table>
<thead>
<tr>
<th>Router:</th>
<th>1 Omnicore 5010 (Alcatel)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switches:</td>
<td>7 Omniswitch 6024 (Alcatel)</td>
</tr>
<tr>
<td></td>
<td>2 Omnicore 5010 (Alcatel)</td>
</tr>
</tbody>
</table>

4-2.3 Interconnection schemes

4-2.3.1 Logical scheme

The scheme below introduces the logical network of TIMA defined with VLANs (This scheme does not mention physical location).
4.2.3.2 Physical scheme

See the following detailed scheme about TIMA Network Wiring:

- **CISCO 5000** connected to **Internet (Renater)**
- **Link 1000 FX** connected to **CISCO 5000**
- **Link 2*100 TX**
- **Link 100 BSX**
- **1 Omnicore 5010**
- **2 switch 6024**
- **68 ports ethernet 10/100**
- **2 ports 1000 BSX**
- **1 Omnicore 5010** connected to **Switch 6024**
- **92 ports ethernet 10/100**
- **2 ports 1000 BSX**
- **Link 1000 FX**
- **802.1q**
- **Link 1000 FX**
4-3 Financial resources

Some data are given below on financial aspects. They are provided for 1989-2004 budget years, to allow comparisons (Table 4-3 1). The budget of the Laboratory does not include salaries of government employees, like CNRS researchers and Professors.

This budget comes from research funds provided by CNRS or Universities (INPG and UJF), from contracts signed with industrial firms or CEC, and from "exceptional" funds or "exceptional" invoices (emitted for example against services). Those funds are accounted by either CNRS, or INPG or UJF. It is to be noted that the input for contracts represent the total amount of the contracts when they are signed, even if the contract will last for several years.

<table>
<thead>
<tr>
<th></th>
<th>Research Funds</th>
<th>Exceptional Funds</th>
<th>Exceptional Invoices</th>
<th>Contracts</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1989</td>
<td>44</td>
<td>129</td>
<td>123</td>
<td>1094</td>
<td>1390</td>
</tr>
<tr>
<td>1990</td>
<td>40</td>
<td>551</td>
<td>149</td>
<td>568</td>
<td>1308</td>
</tr>
<tr>
<td>1991</td>
<td>40</td>
<td>450</td>
<td>300</td>
<td>631</td>
<td>1421</td>
</tr>
<tr>
<td>1992</td>
<td>54</td>
<td>386</td>
<td>400</td>
<td>1007</td>
<td>1847</td>
</tr>
<tr>
<td>1993</td>
<td>112</td>
<td>380</td>
<td>474</td>
<td>1688</td>
<td>2653</td>
</tr>
<tr>
<td>1994</td>
<td>107</td>
<td>284</td>
<td>364</td>
<td>2179</td>
<td>2935</td>
</tr>
<tr>
<td>1995</td>
<td>137</td>
<td>309</td>
<td>986</td>
<td>857</td>
<td>2289</td>
</tr>
<tr>
<td>1996</td>
<td>99</td>
<td>272</td>
<td>1219</td>
<td>1339</td>
<td>2929</td>
</tr>
<tr>
<td>1997</td>
<td>108</td>
<td>89</td>
<td>1485</td>
<td>977</td>
<td>2660</td>
</tr>
<tr>
<td>1998</td>
<td>115</td>
<td>37</td>
<td>1128</td>
<td>915</td>
<td>2195</td>
</tr>
<tr>
<td>1999</td>
<td>123</td>
<td>64</td>
<td>1377</td>
<td>2178</td>
<td>3742</td>
</tr>
<tr>
<td>2000</td>
<td>132</td>
<td>27</td>
<td>1511</td>
<td>3430</td>
<td>5100</td>
</tr>
<tr>
<td>2001</td>
<td>139</td>
<td>31</td>
<td>2752</td>
<td>1269</td>
<td>4191</td>
</tr>
<tr>
<td>2002</td>
<td>169</td>
<td>53</td>
<td>2541</td>
<td>1223</td>
<td>3986</td>
</tr>
<tr>
<td>2003</td>
<td>87</td>
<td>53</td>
<td>2677</td>
<td>1376</td>
<td>4193</td>
</tr>
<tr>
<td>2004</td>
<td>99</td>
<td>90</td>
<td>2276</td>
<td>1900</td>
<td>4365</td>
</tr>
</tbody>
</table>

Table 4-3 1 Budget from 1989 to 2004 (k€, excluding VAT)
If we consider 1989, 1990, 1991, 1992, 1993, 1994, 1995, 1996, 1997, 1998, 1999, 2000, 2001, 2002, 2003, 2004 together, then we get the global data given in Table 4-3 2 and represented by Figure 4-3 1. Such data are more representative of the reality. Now, we get a part of the contracts which is 47,40 % of the budget. From 1991, the average percentages of EC and JESSI/MEDEA shares are respectively 24,77 % and 40,98 %.

<table>
<thead>
<tr>
<th>Research funds</th>
<th>1 605</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exceptional funds</td>
<td>3 745</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>19 762</td>
</tr>
<tr>
<td>Contracts</td>
<td>22 631</td>
</tr>
<tr>
<td></td>
<td>47 743</td>
</tr>
</tbody>
</table>

Table 4-3 2  Budget 1989-2004 (k€, excluding VAT)

Figure 4-3 1  Budget 1989 - 2004
In 2000, the budget has been 5100 k€ (excluding VAT). The Table 4-3 3 gives the distribution, and the Figure 4-3 2 represents it. In 2000, the contractual part represents approximately 67.25 %. The MEDEA part represents 31.75 %.

The Table 4-3 4 gives the list of contracts signed in 2000.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>30</td>
<td>84</td>
<td>18</td>
<td>-</td>
<td>-</td>
<td>132</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>9</td>
<td>18</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>27</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>369</td>
<td>464</td>
<td>7</td>
<td>3</td>
<td>668</td>
<td>1511</td>
</tr>
<tr>
<td>Contracts signed in 2000</td>
<td>271</td>
<td>2015</td>
<td>1027</td>
<td>-</td>
<td>117</td>
<td>3430</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>679</td>
<td>2581</td>
<td>1052</td>
<td>3</td>
<td>785</td>
<td>5100</td>
</tr>
</tbody>
</table>

Table 4-3 3  Budget 2000  (k€ excluding VAT)

![Figure 4-3 2 Budget 2000](image)

<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNES</td>
<td>60</td>
</tr>
<tr>
<td>FRANCE TELECOM</td>
<td>80</td>
</tr>
<tr>
<td>INTA</td>
<td>38</td>
</tr>
<tr>
<td>CEC/CODAC</td>
<td>54</td>
</tr>
<tr>
<td>CEC/HIPERLOGIC</td>
<td>9</td>
</tr>
<tr>
<td>CEC/IST ACID-WG</td>
<td>20</td>
</tr>
<tr>
<td>CEC/IST MATISSE</td>
<td>271</td>
</tr>
<tr>
<td>CEC/IST/PROFIT</td>
<td>169</td>
</tr>
<tr>
<td>CEC/OMI-LIBRES</td>
<td>9</td>
</tr>
<tr>
<td>ESPRIT/TALENT</td>
<td>88</td>
</tr>
<tr>
<td>SERICS/MEDEA SMT AT 403</td>
<td>956</td>
</tr>
<tr>
<td>SERICS/MEDEA A 401</td>
<td>133</td>
</tr>
<tr>
<td>ST MICROELECTRONICS</td>
<td>1536</td>
</tr>
<tr>
<td>XILINX</td>
<td>7</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>3430</td>
</tr>
</tbody>
</table>

Table 4-3 4  Contracts signed in 2000 (k€, excludingVAT)
In 2001, the budget has been 4191 k€ (excluding VAT). The Table 4-3 5 gives the distribution, and the Figure 4-3 3 represents it. In 2001, the contractual part represents approximately 30,30 %.

The Table 4-3 6 gives the list of contracts signed in 2001.

<table>
<thead>
<tr>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>47</td>
<td>77</td>
<td>15</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>10</td>
<td>19</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>752</td>
<td>661</td>
<td>17</td>
<td>76</td>
<td>1246</td>
</tr>
<tr>
<td>Contracts signed in 2001</td>
<td>-</td>
<td>430</td>
<td>600</td>
<td>174</td>
<td>65</td>
</tr>
<tr>
<td>TOTAL</td>
<td>809</td>
<td>1187</td>
<td>634</td>
<td>250</td>
<td>1311</td>
</tr>
</tbody>
</table>

Table 4-3 5  Budget 2001  (k€, excluding VAT)

Figure 4-3 3  Budget 2001

<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEA</td>
<td>15</td>
</tr>
<tr>
<td>CEE/IST FRACTURE</td>
<td>34</td>
</tr>
<tr>
<td>IROC TECHNOLOGIES / JPL</td>
<td>212</td>
</tr>
<tr>
<td>MEFI/MEDEA+ T101</td>
<td>71</td>
</tr>
<tr>
<td>MEFI/MEDEA+ A302</td>
<td>213</td>
</tr>
<tr>
<td>MEFI/MEDEA+ A502</td>
<td>146</td>
</tr>
<tr>
<td>PREDIT/MIRFAS</td>
<td>9</td>
</tr>
<tr>
<td>RNTL/VERHAUNIC</td>
<td>420</td>
</tr>
<tr>
<td>ST MICROELECTRONICS</td>
<td>149</td>
</tr>
</tbody>
</table>

1269

Table 4-3 6  Contracts signed in 2001  (k€, excluding VAT)
In 2002, the budget has been 3 984 k€ (excluding VAT). The Table 4-3 7 gives the distribution, and the Figure 4-3 4 represents it. In 2002, the contractual part represents approximately 30,70 %. The MEDEA part represents 41,78%.

The Table 4-3 8 gives the list of contracts signed in 2002.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>49</td>
<td>105</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>169</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>22</td>
<td>31</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>53</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>350</td>
<td>955</td>
<td>9</td>
<td>8</td>
<td>1219</td>
<td>2541</td>
</tr>
<tr>
<td>Contracts signed in 2002</td>
<td>-</td>
<td>561</td>
<td>522</td>
<td>49</td>
<td>91</td>
<td>1223</td>
</tr>
<tr>
<td>TOTAL</td>
<td>421</td>
<td>1652</td>
<td>546</td>
<td>55</td>
<td>1310</td>
<td>3984</td>
</tr>
</tbody>
</table>

Table 4-3 7 Budget 2002 (k€, excluding VAT)

<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEE/IST “G3CARD”</td>
<td>65</td>
</tr>
<tr>
<td>CEE/IST “REASON”</td>
<td>125</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ T101 “TECHNODAT”</td>
<td>61</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A302 “Esp@ssIS”</td>
<td>155</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A502 “MESA”</td>
<td>130</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A106 “INCA”</td>
<td>165</td>
</tr>
<tr>
<td>MINEFI/ARCHIFLEX</td>
<td>143</td>
</tr>
<tr>
<td>MINEFI/OPPIDUM-ISIA2</td>
<td>72</td>
</tr>
<tr>
<td>MINDEF/SGDN</td>
<td>54</td>
</tr>
<tr>
<td>CEA/LETI</td>
<td>83</td>
</tr>
<tr>
<td>ATMEL</td>
<td>30</td>
</tr>
<tr>
<td>CNES</td>
<td>91</td>
</tr>
<tr>
<td>NASA/JET PROPULSION LAB.</td>
<td>49</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>1 223</strong></td>
</tr>
</tbody>
</table>

Table 4-3 8 Contracts signed in 2002 (k€, excluding VAT)
In 2003, the budget has been 4 159 k€ (excluding VAT). The Table 4-3 9 gives the distribution, and the Figure 4-3 5 represents it. In 2003, the contractual part represents approximately 33.10 %. The MEDEA part represents 51.38 %.

The Table 4-3 10 gives the list of contracts signed in 2003.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>20</td>
<td>50</td>
<td>17</td>
<td>-</td>
<td>-</td>
<td>87</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>31</td>
<td>17</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>53</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>146</td>
<td>1 112</td>
<td>24</td>
<td>13</td>
<td>1 382</td>
<td>2 677</td>
</tr>
<tr>
<td>Contracts signed in 2003</td>
<td>-</td>
<td>799</td>
<td>466</td>
<td>111</td>
<td>0</td>
<td>1 376</td>
</tr>
<tr>
<td>TOTAL</td>
<td>197</td>
<td>1 978</td>
<td>512</td>
<td>124</td>
<td>1 382</td>
<td>4 193</td>
</tr>
</tbody>
</table>

Table 4-3 9 Budget 2003 (k€, excluding VAT)

<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>NASA/JET PROPULSION LAB</td>
<td>51</td>
</tr>
<tr>
<td>ST MICROELECTRONICS</td>
<td>15</td>
</tr>
<tr>
<td>BOSCH</td>
<td>25</td>
</tr>
<tr>
<td>EDF</td>
<td>20</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ T101 “TECHNODAT”</td>
<td>84</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A302 “Esp@ssIS”</td>
<td>157</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A502 “MESA”</td>
<td>140</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A511 “TOOLIP”</td>
<td>326</td>
</tr>
<tr>
<td>MJENR/DURACELL</td>
<td>344</td>
</tr>
<tr>
<td>ST MICROELECTRONICS (CIFRE)</td>
<td>174</td>
</tr>
<tr>
<td>LEONARDO/IPCI</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>1 376</td>
</tr>
</tbody>
</table>

Table 4-3 10 Contracts signed in 2003 (k€, excluding VAT)
In 2004, the budget has been 4210 k€ (excluding VAT). The **Table 4-3 11** gives the distribution, and the **Figure 4-3 6** represents it. In 2004, the contractual part represents approximately 43.53%. The MEDEA part represents 32.79%.

The **Table 4-3 12** gives the list of contracts signed in 2004.

<table>
<thead>
<tr>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>32</td>
<td>50</td>
<td>17</td>
<td>-</td>
<td>99</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>38</td>
<td>35</td>
<td>17</td>
<td>-</td>
<td>90</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>106</td>
<td>809</td>
<td>-</td>
<td>3</td>
<td>1358</td>
</tr>
<tr>
<td>Contracts signed in 2003</td>
<td>45</td>
<td>998</td>
<td>376</td>
<td>456</td>
<td>25</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>221</strong></td>
<td><strong>1892</strong></td>
<td><strong>410</strong></td>
<td><strong>459</strong></td>
<td><strong>1383</strong></td>
</tr>
</tbody>
</table>

**Table 4-3 11  Budget 2004 (k€, excluding VAT)**

**Figure 4-3 6  Budget 2004**

<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATMEL</td>
<td>50</td>
</tr>
<tr>
<td>CNES</td>
<td>110</td>
</tr>
<tr>
<td>CEA</td>
<td>45</td>
</tr>
<tr>
<td>COMPS/EDITH EDITH COWAN UNIVERSITY</td>
<td>119</td>
</tr>
<tr>
<td>ST MICROELECTRONICS (CIFRE)</td>
<td>35</td>
</tr>
<tr>
<td>CEE/VIBES</td>
<td>214</td>
</tr>
<tr>
<td>CEE/MINAEST</td>
<td>8</td>
</tr>
<tr>
<td>MENESR/ACI “NANOSYS”</td>
<td>14</td>
</tr>
<tr>
<td>MENESR/ACI “VENUS”</td>
<td>140</td>
</tr>
<tr>
<td>MENESR/ACI “MARS”</td>
<td>132</td>
</tr>
<tr>
<td>MENESR/ACI “EUROSOC ”</td>
<td>12</td>
</tr>
<tr>
<td>MENESR/&quot;SYSTEM C'MANTIC&quot;</td>
<td>243</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ T101 “TECHNODAT”</td>
<td>63</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A302 “Esp@ssIS”</td>
<td>174</td>
</tr>
<tr>
<td>MINEFI/MEDEA+ A502 “MESA”</td>
<td>120</td>
</tr>
<tr>
<td>MINEFI “MERCED”</td>
<td>266</td>
</tr>
<tr>
<td>MD/SGDN2</td>
<td>155</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>1900</strong></td>
</tr>
</tbody>
</table>

**Table 4-3 12  Contracts signed in 2004 (k€, excluding VAT)**
5 - Cooperative activities

5-1 Contracts

**Public Institutions:**
MINEFI (Ministère de l’Économie, des Finances et de l’Industrie) ; Ministère de la Défense – Secrétariat Générale de la Défense Nationale ; Ministère de la Jeunesse, de l’Education Nationale et de la Recherche.

**Industrial contracts:**
STMICROELECTRONICS, CEA, CNES, NASA, AEROSPATIALE.

5-2 European Projects and MEDEA Projects

5-2.1 Summary

Long ago, members of the Laboratory participated to EC Projects like CASCADE and CVT. Presently, or recently, the Laboratory participates or has been participating to the following projects:

**ESPRIT PROJECTS**
- ESPRIT I: ADVICE, AIDA, SPAN
- ESPRIT II BASIC RESEARCH: ASCIS, EUROCHIP
- ESPRIT III BASIC RESEARCH: ARCHIMEDES, FASED, BARMINT, AMATIST, GRASS
- ESPRIT III RESEARCH AND DEVELOPMENT: CHIPSHOP
- ESPRIT III KIT: ARCOS, ATAME
- ESPRIT IV KIT: DETERMIN, LICDST, LIMITE
- ESPRIT IV LTR: HIPERLOGIC
- ESPRIT IV RESEARCH AND DEVELOPMENT: COMITY, TALENT
- ESPRIT IV OMI: IUN2, EUROMIC, OMILIBRES, CODAC, ASSISTEC
- ESPRIT IV BEST PRACTICE: SYSLINK

**IST**
- MATISSE
- PROFIT
- ACID-W
- FRACTURE
- REASON
- G3CARD
- VIBES

**CEC/NSF Cooperation**
- NDIMST
- CSLS

**JESSI PROJECTS**
- AC6
- AE11
- AC8
- AC3
- AE102
- AE1

**MEDEA PROJECTS**
- AT 403
- AT 401-408

**MEDEA+ PROJECTS**
- T 101
- A 302
- A 502
- A 106
- A 511

**COMETT PROJECTS**
- COMET
EUROSYSTEMS, EPIQCS

EUREKA PROJECT
- MITHRA

TEMPUS PROJECTS
- Advanced JEP for Microelectronics Design Methodology
- MECC
- Initiation of Formal Training in CAEE in Romanian Universities
- Computer-aided Methods and Technical Management in Electrical Engineering Education
- Digital System Design Based on PLD-Technology
- Education for Quality Control in Electrical Industry Equator
- Postgraduate Education in ASIC Design
- EUROQUALROM: European Education in Quality for Romania

COPERNICUS (PECO) PROJECTS
- EDAC-EAST: Attendance of Central and Eastern European Engineers and Researchers to the EDAC Conference
- Design of VLSI self-checking digital circuits
- Developing design automation technique in ASIC and VLSI Design
- CAD/CAT tools integration for sensor-based microsystems
- Dependability Analysis of Complex Electronic Components and Systems
- East European Microelectronics Cooperation Network of support and competence centres of Central and Eastern Europe
- Functional Test Generation and diagnosis (FUTEG)
- EUROEAST: Extension of EUROCHIP services to Central and Eastern European Countries
- THERMINIC: New Methods for Thermal Investigation of Integrated Circuits
- MINAEAST: Project Micro & Nanotechnologies going to Eastern Europe through networking

HUMAN CAPITAL MOBILITY PROJECT
- GARDEN

LATIN AMERICA HIGHER EDUCATION
- HUERTA, ELACIAC, ALFA/TOSCA

5-2.2 Details

Below are described the European Projects the Laboratory has been involved in since 1984.

They are divided in two categories:
- the finished ones
- those which are ongoing.

For the finished ones, only few data are given (more information is available in previous reports). For the ongoing projects, an abstract describing the project is given.

5-2.2.1 European Projects that came to the end in 2003 or before

ESPRIT PROJECTS

ESPRIT-I
- ADVICE
- AIDA
  (SIEMENS, ICL, SGS THOMSON, TIMA, University of Manchester), 1986-1990, Advanced Integrated-circuit Design Aids
- SPAN
  (THORM-EMI, CIMSA-SINTRA, CTI, INESC, PCS, TIMA, University College London), 1987-1990, Parallel Computer Systems for Integrated Numeric and Symbolic Processing
ESPRIT-II Basic Research

- EUROCHIP (GMD, CMP, IMEC, University of Lyngby, RAL), 1989-1994, Service organisation of the VLSI Design Action, CMP was a member of the Service Organisation.

ESPRIT-III Basic Research

- AMATIST (CNM Sevilla, MESA Institute - Univ. of Twente, TIMA, Univ. of Cantabria, Univ. of Lancaster, Univ. of Pavia), 1994-1997, Analogue & Mixed-signal Advanced Test for Improving System-level Testability
- GRASS (Working Group) (Univ. de Las Palmas de Gran Canarias, TIMA, Middlesex University, Techn. Univ. of Denmark, EPFL, Fraunhofer-Gesellschaft Erlangen), 1994-1997, Gallium arsenide Research action on ASIC Synthesis

ESPRIT-III Research and Development


ESPRIT-III KIT ("Keep-In-Touch")

- ARCOS (IMEC, TIMA, University of Sao Paulo), 1995-1997, ARChitectural synthesis of COmplex Systems on silicon
- ATAME (IMEC, TIMA, Polytechnical Univ. of Madrid, Institute of Microelectronics – Singapore, National University), 1995-1997, Advanced Telecom And Multimedia design technology Environment

ESPRIT-IV KIT ("Keep-In-Touch")

- DETERMIN (Technical University of Budapest, TIMA), 1998-2001
- LIMITE (LIRMM, TIMA, ATMEL ES2, UAB, PUC-RS), 1998-2001

ESPRIT-IV Long Term Research

- HIPERLOGIC (IMS, TIMA, IMC, IPVR, TUB), 1996-1999, Thousand MOPS per MilliWatt CMOS High PERformance LOGIC
ESPRIT-IV Research and Development

- COMITY
  (VERILOG, AEROSPATIALE, BMW, INTRACOM, C-LAB, DIT/UPM, ISI, TIMA), 1997-1999
  Codesign Method and Integrated Tools for Advanced Embedded Systems

- TALENT
  (ANACAD, AMS, BOSCH, TIMA, MEMSCAP, NMRC, SENSENOR, TUB/DED), 1998-2000
  Tools Adaptation and Library development towards microsystems design environment

ESPRIT-IV OMI

- IUN2
  (CMP, UNED, Archimedes, IMEC, OMIMO, Sussex University, TODiTEC and UPM), 1995-1996, Inter University Network

- EUROMIC
  (CMP, FhG, IMEC, OMIMO, Sussex University and UPM), 1996-1997, EUropean OMI Centres

- OMILIBRES
  (CMP, Alcatel Mietec, Compass, Mentor, Nokia, SIDSA, Telefonica I+D, Thomson-CSF and Viewlogic), 1996-1997, OMI LIBrary REpresentation Standards

- CODAC
  (IMEC, CoWARE, ARM, Alcatel-Mietec, SGS-Thomson, Alcatel-Bell, INTRACOM,TIMA), 1997-1998

- ASSISTEC
  (IPRIAS Ltd., DOLPHIN INTEGRATION, SEND, SYNDESIS Ltd, TIMA), 1997-1999, Assistance to SMES in the pre-licence phase of the exploitation of their intellectual property

ESPRIT-IV Best Practice

- SYSLINK
  (GMD, Politecnico di Torino, TIMA), 1995-1997, Linking System Designers and CAD Developers in Europe

IST PROJECTS

- MATISSE
  (DERA, Univ. of Southampton, TIMA/CNRS, Aabo Akademi Univ., MATRA Transport International, STERIA), 2000-2002

- PROFIT
  (Philips Electronics Nederland B.V. (Philips), ST Microélectronis s.r.l.(ST Italy), Infineon Technologies AG (Infineon), Philips Semiconductors B.V.(philips sc), Flomerics Ltd.(Flomerics), Technical University of Budapest(TUB), Mic red Microelectronics Research and Development Ltd.(Micred), INPG/TIMA, Centre for Quantitative Methods B.V.(CQM), Nokia Corporation (Nokia)), 01/01/2000-31/03/2003

- FRACTURE
  Nanoelectronic Devices & Fault-Tolerant Architectures
  (National Centre for Scientific Research "DEMOKRITOS", University of Durham, Iroc Technologies, UJF/TIMA), 01/01/2001-31/12/2003

- G3CARD
  Generation 3 Smartcard
  ARM LIMITED (ARM)*, THE CHANCELLOR MASTERS AND SCHOLARS OF THE UNIVERSITY OF CAMBRIDGE (UCAM-CLAB), CRYPTOMATHIC A/S (CRM), GEMPLUS S.A., UNIVERSITE CATHOLIQUE DE LOUVAIN (UCL), THE VICTORIAT UNIVERSITY OF MANCHESTER (UoM), NDS TECHNOLOGIES ISRAEL (NDSTI), TIMA/INP 01/01/2000-31/01/2003
CEC/NSF Cooperation

- **NDIMST**
  (University of Texas at Austin, TIMA), 1993-1995, New Directions In Mixed Signal Test

- **CSLS**
  (University of California at Irvine, TIMA), 1994, Circuit and System-Level Synthesis

- **AC6**

- **AE11**

- **AC8**
  Integrating AMICAL within industrial CAD environment, 1993-1996; *Industrial partners*: AHL, Bosch, Bull, Philips, Siemens, Siemens-Nixdorf, SGS-Thomson, Synthesia, Thomson-TCS; *Associated partners*: TIMA

- **AC3**

- **AE102/AE103**
  Conception de circuits ATM, 1996-1998; *Industrial partners*: SGS-Thomson, Italtel, Telefonica I+D; *Associated partners*: TIMA

MEDEA PROJECTS

- **AT 403**
  System level Methods and Tools, 1997-1998-1999-2000; (STMICROELECTRONICS, BULL SA, METASYMBIOSE, LIP6, TIMA)

- **AT 401-408**

- **A106 : INCA (Integrated Network Copper Access)**
  (ST microelectronics, THOMSON Multimedia R&D France, France-Telecom, ENS Cachan, UJFTIMA)

- **A511 : TOOLIP (Tool IP “Intellectuel Properties”)**

COMETT PROJECTS

COMETT I

- **COMET**
  (IMEC, TIMA, Universities of Darmstadt, Limerick, Lyngby, Madrid), 1988-1990; Consortium for microelectronic training

COMETT II

- **EUROSYSTEMS**
  (University of Darmstadt, IMEC, University of Lyngby, TIMA)

- **EPIQCS : Masters Degree Specialized in Quality of Complex Integrated Systems**
  (INPG, Imperial College of London, Universities of Darmstadt and Eindhoven)
EUREKA PROJECTS

- MITHRA
  (BROSSARD, BERTIN, ITMI, SEIV, LAMM, ELKRON, OLMAT, SEPA, EPFL, CERBERUS, TIMA), 1988-1990

TEMPUS PROJECTS

- Advanced Joint European Programme for Microelectronics Design Methodology
  (University of Darmstadt, Technical University of Budapest, IMEC, University of Lyngby, TIMA, Institute of Electron Technology of Warsaw)

- MECC (Management, Electronics, Computer science)
  (Ecole Polytechnique Fémiline, TIMA, Institut Universitaire de Technologie de Cachan, Ecole Supérieure d'Optique d'Orsay, Technische Universität Munchen, Technische Universität Karlsruhe, Universität Gesamthochschule Duisburg, Friedrich Alexander Universität Erlangen-Nürnberg, Fraunhofer Gesellschaft Erlangen, Fachhochschule München, Universidad Pontificia Comillas, Czech Technical University Prague, Technische Universität Dresden, Ingenieurshochscule Mittweida, Technische Hochschule ILMENAU, Slovak Technical University Bratislava, EMPRESARIOS AGRUPADOS, SIEMENS AG Erlangen, DORNIER GmbH, CORSE COMPOSITES, PIROSPACE, ONERA, EUROPEAN SILICON STRUCTURES)

- Initiation of Formal Training in Computer Aided Electrical Engineering in Romanian Universities
  (TIMA, ENSIEG/INPG, Univ. of Bucharesti, Bath, Genova, Cassino, Paris 6 & 11, Graz, EDF, Politecnico di Torino)

- Computer-aided Methods and Technical Management Inelectrical Engineering Education
  (Technical Univ. Budapest, Univ. Karlsruhe, Univ. Erlangen-Nürnberg, University College London, TIMA, Univ. of Pisa, Techn. Univ. of Delft, MOTOROLA GmbH, TEXAS INSTRUMENTS DEUTSCHLAND, HEWLETT PACKARD, DIGITAL EQUIPMENT, IBM)

- Digital System Design Based on PLD-Technology
  (Technische Hochschule Darmstadt, TIMA, Tallinn Technical Univ.)

- Education for Quality Control in Electrical Industry (Equator)
  (Technical Univ. of Brno, Czech Technical University of Prague, Technical Univ. of Ostrava, Leeds Metropolitan Univ., Bournemouth Univ., TIMA, Univ. of Hull)

- Postgraduate Education in Asic Design
  (Warsaw Univ. of Technology, Technical Univ. of Lodz, Univ. of Mining and Metallurgy of Cracow, TIMA, Technische Hochschule Darmstadt, Eindhoven Univ. of Technology, Helsinki Univ. of Technology)

- Euroqualrom: European Education in Quality for Romania
  (Univ. "POLITEHNICA" of Bucharest, Academy for Economic Studies of Bucharest, Univ. of Oradea, Univ. of Pitesti, TIMA, "Ecole Nationale Supérieure des Arts et Métiers" of Paris, Univ. Aberta of Lisbon, Univ. Politecnica de Catalunya of Barcelona, Univ. of Piraeus, Politecnico di Torino, Univ. of Angers, Univ. of Paisley, Romanian Foundation for Quality Promotion of Bucharest, Romanian Society for Quality Assurance of Bucharest, Erasmus Univ. of Rotterdam)

COPERNICUS PROJECTS

COPERNICUS : Cooperation in science and technology with Central and Eastern Europeancountries.

European Conferences, workshops and training seminars:

- EDAC-EAST
  Attendance of Central and Eastern European Engineers and Researchers to the EDAC Conference

Mobility scheme for scientists :

- Design of VLSI Self-Checking Digital Circuits
  (Stanislaw PIESTRAK, Technical University Wroclaw, Poland)

- Developing Design Automation Technique in ASIC and VLSI Design
  (Tania VASSILEVA, Technical University Sofia, Bulgaria)

- CAD/CAT Tools Integration for Sensor-Based Microsystems
  (Teodor CALIN, Polytechnical Institute of Bucharest, Romania)
Dependability Analysis of Complex Electronic Components and Systems
(Ioan BACIVAROV, Polytechnical Institute of Bucharest, Romania)

Pan European Scientific Networks:

East European Microelectronics Cooperation Network of support and Competence Centres of Central and Eastern European Countries

Joint Research Proposals:

Functional Test Generation and Diagnosis (FUTEG)
(Technical University of Tallinn - Estonia, Kaunas University of Technology - Lithuania, Institute of Computer Systems Bratislava, Technical University of Budapest, TIMA, Fraunhofer Institute for Integrated Circuits EAS Dresden) 1994-1997

Extent of Eurochip Services to Central and Eastern European Countries (EUROEAST)
(GMD, CMP, DTH, IMEC, RAL, Polytechnic Institute of Bucharest, ITME Warsaw, Warsaw University, Silesian Technical University)

New Methods for Thermal Investigation of Integrated Circuits (THERMINIC)
(Technical University of Budapest, Hungary, Technical University of Lodz, Poland, Technical University of Lviv, Ukraine, SEMILAB Budapest, Hungary, TIMA) 1995-1997

Projet Micro & Nanotechnologies going to Eastern Europe through networking (MINAEAST)

HUMAN CAPITAL AND MOBILITY PROJECT

GARDEN: Gallium Arsenide Reliable Design Environment, 1994-1997
(Universidad de Las Palmas de Gran Canarias, TIMA, Philips Electr. Laboratories, Middlesex University, Techn. Univ. of Denmark, EIDG. Technische Hochschule Zürich, Fraunhofer Inst. for Applied Solid State Physics at Freiburg, Fraunhofer Inst. for Integrated Circuits at Erlangen, GIGA at Brondby, Thomson CSF)

LATIN AMERICA HIGHER EDUCATION PROJECTS (Amérique Latine Formation Académique : ALFA)

HUERTA: Higher University Education and Research Training Action, 1998
(Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil; Universidad Federal do Rio de Janeiro/COPEPE, Rio de Janeiro, Brazil; Universidad de los Andes, Bogota, Colombia; Universidad Autonoma Metropolitana, Mexico, Mexico; Univ. Catholique de Louvain; Louvain La Neuve, Belgium; TIMA; Technische Hochschule Darmstadt, Germany; Universidad de Aveiro, Portugal)

ELACIAC: European-Latin American Cooperation for Intelligent Automation and Control, 1998
(Universidad Nacional de Rosario, Instituto de Fisica de Rosario, Rosario, Argentine; Universidad de Chile, Facultad de Ciencias Físicas y Matemáticas, Departamento de Ingeniería Eléctrica, Santiago, Chile; Escuela de Ingeniería "Mcal. Antonio José Sucre", La Paz, Bolivia; Universidad de Guadalajara, Centro Universitario de Ciencias Exactas de Ingeniería, Mexico; TIMA; School of Engineering, University of Wales Cardiff, UK; Technische Universität Clausthal, Institut für Elektrische Informationstechnik, Germany; Universidad Politécnica de Madrid, Departamento de Señales Sistemas y Radiocomunicaciones, Madrid, Spain)
5-2.2.2 New European Projects or European Projects still ongoing in 2004

IST PROJECTS

- ACiD-WG
  (South Bank University, UK), 28/08/2000-27/08/2004
  Working group on Asynchronous circuit Design
  ACiD-WG aims at improving the systematic exchange of information and the forging of links between teams with carry out RTD or take-up activities around the theme of asynchronous circuit design. Its objectives in FPS are as follows:
  1. To encourage excellence in science and technology research pertaining to asynchronous circuits and systems.
  2. To facilitate the development of methods and tools that are usable by engineers for the design of asynchronous VLSI systems.
  3. To promote the adoption of asynchronous circuit design in industry.

- REASON
  Research and Training Action for System on Chip Design
  (POLITECNIKA WARSZAWSKA (WUT) "the coordinator", Poland, Instytut Technologii Elektronowej (ITE) Poland, TALLINNA, TEHNIKUT UëRA, POLITEHNICA DIN BUCURESTI ( PUB), Romania, TECHNISCHE UNIVERSITÄT ILMENAU (TUI) Germany, POLITECNIKA LODZKA (TUL) Poland, INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZXW (IMEC) Belgium, TECHNISCHE UNIVERSITEIT EINDHOVEN (TUE) The Netherlands, SLOVAK ACADEMY OF SCIENCES –INSTITUTE OF INFORMATICS (II SAS) Slovak Republic, TEHNICE UNIVERSITET SOFIA (TUS) Bulgaria, LVIV POLYTECHNIC NATIONAL UNIVERSITY (LPU) Ukrainian SSR, BELARUSSKI GOSUDARSTVENNIY (LPU) Ukrainian SSR, BELARUSSKI GOSUDARSTVENNIY UNIVERSITET INFORMATIKA I RADIOELEKTRONIKI (BSUIR) Byelorussian SSR, TECHNICAL UNIVERSITY OF LIBEREC (TULC) Czech Republic, KAUNAS UNIVERSITY OF TECHNOLOGY (KTU) Republic of Lithuania, BELARUSIAN STATE UNIVERSITY (BSU) Byelorussian SSR, UNIVERZA V LJUBLJANI, FAKULTETA ZA ELEKTROTEHNIKO (UOL) Republic of Slovenia, RIGA TECHNICAL UNIVERSITY (RTU) Republic of Latvia, COUNCIL (CCLRC) United Kingdom, et UJF/TIMA. 01/01/2002-31/12/2004.
  The goal is to facilitate integration of the academic and research institutions of Central and Eastern Europe working in the field of microelectronics into the mainstream R&D activities going on in the EU countries. The main objectives of the project are as follows:
  (1) Raising the level of awareness of industrial problems and the level of competencies among researchers in CEE in methodologies of system-on-chip design and test and analogue and mixed signal IC design for wireless communication, networking, and multimedia.
  (2) Strengthening of links between academic and industrial partners, in order to facilitate formulation of new RTD projects and formation of project consortia.
  (3) Maintaining and expanding the research infrastructure in the academic and research institutions of Central and Eastern Europe.
  (4) Knowledge transfer to the SMEs and raising the level of awareness of the IST programme, in order to facilitate participation of SMEs in FP5 and the next Framework Programme projects.
  The workplan includes the following activities:
    - Introductory actions:
      - Analysis of needs of local industries in CEE countries,
      - Access to EUROPRACTICE by partners from Russia, Ukraine and Belarus.
    - Training actions in the field of system-on-chip design and ASICs for wireless communication, networking, and multimedia.
    - Practical training in usage and maintenance of advanced CAD tools.
    - Development of EDUCHIP - special VLSI chip for microelectronic education.
    - Topical workshops devoted to tutorial-based discussions of narrow but vital areas of research in microelectronic design.
    - Development and deployment of Web-based training materials.
    - Special conference sessions and/or tutorials on industrial and educational problems.
  The partners from EU member states will play three important roles:
  They will provide information, help and guidance for project partners which aim at joining EUROPRACTICE and start their training and research in close co-operation with the microelectronic community of the unified Europe,
  They will bring to the project their expertise in state-of-the-art methodologies and tools of system-on-chip design, and
  They will provide links to the European microelectronic manufacturers.
VIBES
VIBration Energy Scavenging
(Philips Electronics Nederland BV, Netherlands- Philips Inovative Technology Solutions NV, Belgium - ADR, France - University of Southampton, United Kingdom - University of Cork, Ireland – CNRS, France – MEMSCAP, France – METRAVIB, France - Philips GmbH, Germany)
01/01/2004-31/12/2006

VIBES is a Specific Targeted Research Project (STREP) of the 6th Framework Program of the European Union (EU). The goal of this project is to develop and demonstrate a micro power generator able to scavenge vibrations and motions from the surrounding (like building, machines, human body). This device will produce electrical power (in the range of µW) in order to feed an autonomous microsystem. The microsystem will embed an Ultra Low Power controller, a low power RF communication module, several MEMS sensors and a micro battery for energy storage. The project will focus on piezoelectric and electromagnetic transduction principles implemented with MEMS microfabrication techniques.

MEDEA+ PROJECTS

T 101 : TECHNODAT

Project n° 2 : Low-cost test solutions for systems on silicon

The evolution of technology towards a higher density and new materials is resulting in a flow of new constraints that should be taken into account at design level. The right technology-dependent environments are necessary not only to accelerate or secure today's designs, but also to make future designs simply feasible.

The goal of this Project is to allow designers to get the best benefits of the new technologies (down to 0.07 µ), without additional overload. This strong consortium will guarantee efficient know-how transfer from academic research down to production level. The Project consists in combining 3 challenges:

1. A know-how acquisition challenge concerning local and interdependent physical modeling down to 0.07 µ: e.g. new materials (e.g. SOI), stringent needs for new parasitics extraction to reach timing closure, upgrade of 2-D modeling to 3-D
2. An industrial challenge to cope with exploding product complexities and performance figures for an ever faster going market place (bigger cells, more views, more types of cells, higher speeds) and with new kinds of team-working (SOC, reuse, distributed teams)
3. A clear market

A 302 : Esp@ssIS (Enhanced SmartCard Platform for Accessing Securely Services of the Information Society)
(STMICROELECTRONICS, SCHLUMBERGER, BULL CP8, CELA-LETI, THOMSON MULTIMEDIA, TRUSTED LOGIC, PHILIPS CONSUMER ELECTRONICS, INTERPAY, TELECOM ITALIA MOBILE, SMART TRUST, TIMA), 2001-2002-2003-2004

The EsP@ss-IS project's primary goal is to provide open smart-card platforms (both hardware and software) to support the development of value added electronic and mobile commerce services. On a secondary level the development of the open smart-card platforms will provide a set of reusable innovative technological bricks from which future generations of high security smart-card products may be created.

A 502 : MESA (Multi-processor Embedded Systems Architectures)
(ALCATEL, BULL, COWARE, EDSN, EONIC, EPUN/MCSE, FRONTIER-DESIGN, IMEC, INRIA, KU-Leuven, METASYMBOIOSE, PHILIPS, POLYSPACE, STMicroelectronics, UJF/TIMA, UPMC/LIP), 2001-2004

To meet the huge computational capabilities of the 100 nm IC generation, together with exploding market needs, efficient design methods for reconfigurable multi-processor architectures are urgently needed: today, when a multi-processor architecture is targeted, no satisfactory solution is available for analysing the application domain, providing reconfigurable IP blocks, defining communication protocols, and validating the resulting solution. This Project aims at providing flexible design platforms for multi-processor architecture design, in order to fill this gap. Each new environment delivered by the project will be driven by an industrial test-case in these application fields: Telecom terminals, Digital Radio Communication Networks, Consumer and Computer.

TIMA will investigate the formal validation of the initial specifications and early design steps, when the system behavior is given in terms of abstract functions, prior to making bit accurate decisions on the data path, or cycle accurate instruction set architectures. We propose to combine simulation of test cases, symbolic simulation and theorem proving, as complementary techniques applied to a variety of system level specification formalisms.
**COPERNICUS PROJECTS**

COPERNICUS: Cooperation in science and technology with Central and Eastern European countries.

- **MINAEAST-NET (Micro & Nanotechnologies going to EASTern Europe through NETworking)**

  The aim of the project MINAEAST-NET is to support a concerted effort for preparing the participation of ACC’s to projects in FP6 on Micro and Nano technologies (MNT). The main objective is networking on micro and nanotechnologies, according to priority thematic areas 2 (IST) and 3 (NMP) from FP 6. The MINAEAST-NET project will develop a network of networks, called also MINAEAST-NET, which will be composed of networks of micro and nanotech-nologies from ACC as before 1st of May (2004) when the enlargement will take place). Core members of this MINAEAST-NET network of networks originating during the duration of the project will be the project partners (from both ACC and MS), as well as the coordinators or contact points of the above existing or emerging networks in micro and/or nanotechnologies.

**LATIN AMERICA HIGHER EDUCATION PROJECTS**

(Amérique Latine Formation Académique : ALFA)

- **ALFA/TOSCA : Co-operation for Scientific and Technical Training**

  The rapidly increasing adoption of electronic systems for safety-critical applications even in low-cost and high-volume products demands for a new class of researchers and highly-skilled designers. The proposal aims at supporting the researcher mobility among a net of European and Latin American Universities with well-recognized skills in this sector, and to increase the mobility of young researchers among the participating institutions. Thanks to the complementary experience of the network members, and to the novelty of problems and proposed solutions, the training activities they will offer will represent a precious help in the diffusion of fault-tolerant design techniques in the interested countries.
5-3 International cooperation agreements

The Laboratory is engaged or has been recently engaged in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations allow to remote researchers at the cooperative location for in-deep fruitful exchanges of results to organize joint research and Workshops.

- **Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil**
  - This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with R. REIS, on the automatic design of integrated circuits.

- **Universidade Federal do Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil**
  - This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with A. MESQUITA, on high level synthesis and test of integrated circuits.

- **Ecole Nationale d'Ingénieurs de Monastir (ENIM), Monastir, Tunisia**
  - This cooperation takes place in the framework of a project sponsored by the French ministry for education and research and the Tunisian ministry for research and technology; cooperation program which name is "Réseaux Formation-Recherche franco-tunisiens", with S. NASRI, on computer-aided design of communication-dedicated circuits.

- **Universidad Polytecnica de Catalunya (UPC/ETSI), Spain**
  - This cooperation (PICASSO) is carried out with J. CABESTANY on the study of Robustness of Digital Implementation of artificial neural networks, with exchanges of students and researchers between TIMA and UPC.

- **Faculté des Sciences de Monastir, Tunisia**
  - This cooperation takes place in the framework of TEMPRA, between France and Tunisia. The project deals with FPGA to ASIC retargetting, with Electronic and Microelectronic Laboratory, Prof. R. TOURKI and M. ABID. 8 PhD students and 1 post-doctoral from FSM have been involved and defended their PhD thesis. This cooperation is renewed with a new name : MIRA.

- **Ngee Ann Polytechnic, Singapore**
  - This cooperation includes the exchange of staff members and students.

- **University of Tripoli, Lebanon**
  - This cooperation is about a test system for the validation of computers based on microprocessors in space, Professor Z. HAISSAM.

- **University “Polytechnica” of Bucarest, Romania**
  - This collaboration consists of a project focused on architectures based on quantum devices with Prof. R. CHISLEAG and a TEMPUS project, "EUROPEAN EDUCATION IN QUALITY FOR ROMANIA", with Prof. I. BACIVAROV.

- **Budapest University of Technology and Economics (BUTE), Hungary**
  - This cooperation takes place in the framework of the PhD work of L. ANTONI, co-directed by R. LEVEUGLE at TIMA and B. FEHER at BUTE (Department of Measurement and Information Systems). The project deals with run-time reconfiguration of FPGAs for fault injection applications.

- **Politecnico di Torino, Italy**
  - This cooperation takes place in the framework of GALILEO; between France and Italy. The project deals with validation of an automated technique for the realization of robust software devoted to high-safety applications with the Dipartamento di Automatica e Informatica, M. SONZA REORDA.

- **National University of Singapore, Institute of High Performance Computing (IHPC), Singapore**
  - This collaboration started with a preliminary project; carried out in 2002 on the implementation in a single chip of a dependable multiprocessor embedded system. R. Leveugle made a one-week visit in IHPC in June 2002; as Invited Scientist. This first collaboration led to a 3-year project proposal; submitted in Singapore to A*STAR (Agency for Science; Technology & Research ) and NSTB (National Science and Technology Board). This project aims at developing a wireless router; as a demonstrator of a hardened single chip multiprocessor embedded system. The partners are TIMA, IHPC, the Center for Wireless Communication in Singapore and an industry (Smartbridges). A second project has also been prepared and submitted for funding by A*STAR. It aims at developing a CAD environment for nanoelectronics (SET-based circuits), with a special focus on simulation tools and defect/fault tolerance. The collaboration includes several partners in Singapore and India.
The Czech Technical University, Faculty of Electrical Engineering, Prague
- This cooperation takes place in the framework of a bilateral project Barrande, sponsored on the French side by the French Ministry of Foreign Affairs and by the French Ministry of Education. The collaboration is established with the department of Microelectronics and with the department of Radioelectronics in the field of MEMS testing.

Universidade Federal do Rio Grande do Norte (UFRN), Natal, Brazil
- This cooperation has been settled in the context of the CAPES-COFECUB project titled “Design of Mixed Hardware-software Multiprocessor Architectures” that also involves the Universidade Federal do Rio Grande do Sul (Porto Alegre). The two groups involved are directed by David Déharbe at UFRN, and Dominique Borrione at TIMA, on the topic: improvement of techniques and tools for the formal validation of systems designs.

Japan Aerospace Exploration Agency (JAXA), Ibaraki, Japan
- JAXA has launched the research and development of the 64-bit microprocessor in order to realize radiation hardened high-speed onboard processors dedicated for JAXA’s future satellite missions. JAXA intends to establish the estimation method of single event upset (SEU) rate applying to the 64-bit microprocessor for the purpose of developing reliable onboard processor with optimized architecture for JAXA’s future satellites missions. TIMA has studied and specialized in SEU rate estimation by injection of code emulated upset (CEU), and desires to provide and apply its expertise for the 64-bit microprocessor developed by JAXA to be demonstrated in JAXA’s future satellite missions.

The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon
- This cooperation takes place in the framework of the project DUO-France, sponsored by the French Ministry of Foreign Affairs. The collaboration is established mainly with the department of Electrical and Electronic Engineering in the field of MEMS.

City University of Hong Kong
- This cooperation takes place in the framework of the Hong Kong Joint Research Scheme PROCORE, supported by the French Ministry of Foreign Affairs and by the French Ministry of Education and Research. The project deals with the reliable packaging of integrated micro-electro-mechanical sensors. The cooperation is directed by Y.C. Chan at the Department of Electronic Engineering, CityU, and by L. Rufer at TIMA.

Zhejiang University, Hangzhou City, China
- This cooperation takes place in the framework of the Asia Link Programme, supported by the European Commission. The project deals with SECER - Sino Euro Centre of Education & Research on SoC. The cooperation is directed by Prof Yan Xiaolang, and by A.A. Jerraya at TIMA.

Royal Institute of Technology, Stockholm, Sweden
- This cooperation takes place in the framework of the Asia Link Programme, supported by the European Commission. The project deals with Educating Multi cultural multi - national future leaders in electronic engineering. The cooperation is directed by Prof Hannu Tenhumen, and by A.A. Jerraya at TIMA.

5-4 National cooperation

Project on Quantum Computing Technology

A new project has been started end of 2000 / beginning of 2001 on quantum computing technology in cooperation with a Computer Science Laboratory LEIBNIZ (http://www.imag.fr/leibniz) located in Grenoble. The long term goal is to study how quantum electronics can be used to build quantum computing structures. One paradigm to explore is the tradeoffs between the complexity of algorithms when moving to quantum computing compared to the complexity of hardware when moving to quantum electronics to execute quantum algorithms. Informal contacts are also taken with CRTBT (http://www-crtbt.polycnrs-gre.fr/) a fundamental physics Laboratory in Grenoble, where superconducting nano-circuits are studied in order to realize quantum bits.
5-5 International activities

This section gives an overview of national and international activities to which participated recently the members of the Laboratory.

Participation to Committees for Conferences and Workshops

- **Asian Test Symposium (ATS):**
  1992 (Hiroshima); 1993 (Beijing); 1994 (Osaka); 1995 (Bangalore); 1996 (Taipei); 1997 (Akita); 1998 (Singapore); 2002 (Guam Island)

- **Asia Pacific Conference on Hardware Description Languages (APCHDL):**
  1993 (Brisbane); 1994 (Toyohashi); 1996 (Bangalore); 1997 (Taiwan); 1998 (Seoul)

- **Asia Pacific Symposium on Microelectronics and MEMS (MICRO/MEMS):**
  2001 (Adelaide)

- **Built-in Self-Test Workshop (BIST):**
  1984-1993 (Charleston); 1994-1996 with DFT

- **CEC CAVE (CAD for VLSI in Europe) workshops (CAVE):**
  1983-1988

- **COMPEURO:**
  1991 (Bologna); 1992 (The Hague)

- **Conference on Advanced Research in VLSI (ARVLSI):**
  1999 (Atlanta)

- **Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS):**
  1997 (Bratislava); 1998 (Szczyrk); 1999 (Bratislava); 2001 (Győr)

- **Design Automation and Test in Europe Conference (DATE):**
  1998 (Paris); 1999 (Munich); 2000 (Paris); 2001 (Munich); 2002 (Paris); 2003 (Munich); 2004 (Paris)

- **Design for Testability Workshop (DFT):**
  1991-1992 (Vail); 1994-1996 with BIST

- **Design of Circuits and Integrated Systems (DCIS):**
  1996 (Barcelona); 1997 (Sevilla); 2000 (Montpellier)

- **East-West Design & Test Workshop (EWDTW):**
  2004 (Crimea)

- **Electron and Optical Beam Testing of Integrated Circuits (EOBT):**
  1987 (Grenoble); 1989 (Duisburg); 1991 (Como); 1993 (Zurich); 1995 (Wuppertal)

- **Electronics Packaging Technology Conference (EPTC):**
  2003 (Singapore)

- **EuroDAC-EuroVHDL:**
  1994 (Grenoble); 1995 (Brighton); 1996 (Geneva)

- **EUROMICRO:**
  1991 (Vienna); 1992 (Paris)

- **European Conference on Design Automation (EDAC):**
  1990 (Glasgow); 1991 (Amsterdam); 1992 (Brussels)

- **European Conference on Design Automation/EUROASIC (EDAC-EUROASIC):**
  1993 (Paris); 1994 (Paris)

- **European Design and Test Conference (ED&TC):**
  1995-1997 (Paris)
- European Design for Testability Workshop (E-DFT):
  1990 (Segovia); 1992 (Brugge); 1996 (Montpellier); 1998 (Sitges)

- European Safety and Reliability Conference (ESREL):
  1996 (Greece); 1997 (Lisbon); 1998 (Trondheim); 1999 (Munich)

- European Solid-State Circuits Conference (ESSCIRC):
  1986 (Delft); 1990 (Grenoble); 1995 (Lille); 1997 (Southampton); 2002 (Florence); 2003 (Lisboa)

- European Test Conference (ETC):
  1989 (Paris); 1991 (Muenchen); 1993 (Rotterdam)

- European Workshop on Dependable Computing (EWDC):
  1989 (Toulouse)

- Fault-Tolerant Computing Symposium (FTCS):
  1983 (Milano); 1988 (Tokyo); 1989 (Chicago); 1990 (Newcastle upon Tyne); 1991 (Montreal);
  1992 (Boston); 1993 (Toulouse); 1994 (Austin); 1995 (Los Angeles); 1999 (Madison)

- Health and Mass Transfer Conference (HMTC):
  2006 (Guwahati)

- High Level Design Validation and Test Workshop (HLDVT):
  1996-2000 (Oakland); 2001 (San Diego); 2002 (Cannes); 2003 (San Francisco)

- High Level Synthesis Workshop:
  1994 (Niagara Falls); 1995 (Cannes); 1996 (La Jolla)

- IC/Package Design Integration (IPDI):
  1998-1999 (Santa Cruz)

- IEEE Conference on Nanotechnology (NANO):
  2001 (Maui); 2002 (Washington); 2004 (Munich)

- IEEE Great Lakes Symposium on VLSI (GLSVLSI):
  1999 (Ann Arbor); 2000 (Chicago)

- IEEE International Conference on Electronics; Circuits and Systems (ICECS):
  1998 (Lisbon); 2000 (Kaslik); 2001 (Malta); 2003 (Bratislava)

- IEEE International Northeast Workshop on Circuits & Systems (NEWCAS):
  2005 (Quebec City)

  1999 (Barcelona)

- IEEE International Workshop on Design; Test and Applications:
  1998-1999 (Dubrovnik)

- IEEE International Workshop on IDDQ Testing:
  1995-1997 (Washington)

- IEEE International Workshop on Testing Embedded Core-based Systems (TECS):
  1997 (Washington); 1999 (Dana Point)

- IEEE Latin-America Test Workshop (LATW):
  2001 (Cancun)

- IEEE Symposium on Quality of Electronic Design:
  2000-2001 (San Jose)

- IEEE Multi-Chip Module Conference (MCMC):
  1995-1997 (Santa Cruz)
IEEE Mixed-Signal Testing Workshop (IMST):
1996 (Quebec); 1997 (Seattle); 1998 (Twente); 2000 (Montpellier); 2001 (Atlanta)

IEEE VLSI Test Symposium (VTS):
1991-1993 (Atlantic City); 1994 (Cherry Hill); 1995-1996 (Atlantic City); 1997-1998 (Monterey);
1999 (Dana Point); 2000 (Montreal); 2001 (Los Angeles); 2002 (Monterey); 2003 (Napa Valley);
2004 (Napa Valley); 2005 (Palm Springs)

IFIP TC10 Conference "Design Methodologies for VLSI and Computer Architecture":
1988 (Pisa)

IFIP WG10.2 Advanced Research Workshop on Correct Hardware Design Methodologies:
1992 (Torino); 1993 (Arles)

IFIP WG10.5 Advanced Research Working Conference on Correct Hardware Design and
Verification Methods (CHARME):
1995 (Frankfurt); 1997 (Montreal); 1999 (Bad Herrenalb)

IFIP WG10.2 bi-annual International Conference on "Computer Hardware Description Languages
and their Applications" (CHDL):

IFIP WG10.2 International Working Conference "Applied Formal Methods for Correct VLSI Design":
1989 (Leuven)

IFIP WG10.2 International Working Conference "C.A.D. Systems Using AI Techniques":
1989 (Tokyo)

IFIP WG10.2 International Working Conference "The fusion of hardware design and verification":
1988 (Glasgow)

International Conference on ASIC (ASICON):
1996 (Shanghai); 1998 (Beijing); 2001 (Shanghai)

International Conference on Computer-Aided Design (ICCAD):
1991-1993 (Santa Clara); 1994 (San Jose); 1995 (Santa Clara); 1996-1998 (San Jose); 2002 (San Jose);
2003 (San Jose); 2004 (San Jose)

International Conference on Computers and Information Technology (ICCIT):
1998; 2001 (Dhaka)

International Conference on Computer Design (ICCD):
1987 (New-York)

International Conference on Mathematical Methods in Reliability (MMR):
1997 (Bucharest)

International Conference on Microelectronics (ICM):
1991 (Cairo); 1992 (Monastir); 1993 (Dahran)

International Conference on Microelectronic Systems Education (MSE):
1997 (Arlington); 1999 (Arlington); 2001 (Las Vegas); 2005 (Anaheim)

International Conference on Modeling and Simulation of Microsystems; Semiconductors; Sensors
and Actuators (MSM):
1998 (Santa Clara); 1999 (Puerto Rico); 2000 (San Diego); 2001 (Savannah)

International Conference on Probabilistic Safety Assessment and Management:
1991 (Beverly Hills); 1996 (Greece)

International Conference on Quality and Safety:
1999 (Paris)

International Conference on Quality; Reliability and Maintainability-CCF:
2000 (Sinaia)
• International Festival on Scientific TV Programmes:
  2003 (Paris)

• International Workshop on Field Programmable Logic and Applications (FPL):
  1997 (London); 1998 (Tallinn); 1999 (Glasgow); 2000 (Villach)

• International Workshop on Nanotechnologies Engineering & Modelling Outreach (NEMO):
  2004 (Genoa)

• International Workshop on FPGAs and Applications:
  1992 (Vienna); 1994 (Prague); 1996 (Darmstadt)

• INTERPACK Conference:
  1997 (Mauna Lani); 1999 (Maui); 2001 (Kauai); 2003 (Maui), 2005 (San Francisco)

• Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM):
  2000 (Las Vegas); 2002 (San Diego); 2004 (Las Vegas); 2006 (San Diego)

• Low Dimensional Structures and Devices (LDSD):
  1995 (Singapore); 1997 (Lisbon)

• MCM Test:
  1995-2000 (Napa Valley)

• Memory Technology, Design, and Testing (MTDT):
  1993-1995 (San Jose); 1996 (Singapore); 1997-2001 (San Jose); 2002 (Bandol)

• Microelectronics: Design, Technology & Packaging:
  2003 (Perth)

• MICRO SYSTEM Technologies:
  1998 (Postdam); 2003 (München)

• Modeling and Simulation of Electron Devices Workshop (MSED):
  2005 (Pisa)

• Nuclear and Space Radiation Effects Conference (NSREC):
  1997 (Snowmass)

• Optical Microsystems Conference (OUS):
  2005 (Capri)

• Power and Timing Modeling; Optimisation and Simulation:
  1995 (Oldenburg); 1996 (Bologna); 1997 (Louvain-La-Neuve); 1998 (Copenhagen)

• Radiation Effects on Circuits and Systems (RADECS):
  1997 (Cannes)

• Rapid System Prototyping Workshop (RSP):
  1990 - 1993 (Raleigh); 1994 (Grenoble); 1995 (Raleigh); 1996 (Thessaloniki); 1997 (Chapel Hill); 1998 (Leuven)

• Reconfigurable Architectures Workshop (RAW):
  1997 (Geneva); 1998 (Orlando); 1999 (Puerto Rico)

• Sciences of Electronic, Technologies of Information and Telecommunications (SETIT):
  2005 (Susa)

• Signal Propagation on Interconnects (SPI):
  1997-1998 (Travemünde)

• Smart Electronics & MEMS Conference:
  2000 (Melbourne)
Simulation in Electronics:
1994 (Santander)

SPIE Conference on Micromachining and Microfabrication:
1996-1997 (Austin)

SPIE Conference on Smart Structures, Devices, and Systems:
2002 (Melbourne); 2004 (Sydney)

Southwest Symposium on Mixed-Signal Design (SSMSD):
1999 (Tucson); 2000 (San Diego); 2003 (Las Vegas)

Symposium on Integrated Circuits and Systems Design (SBCCI):
2001 (Brasilia); 2002 (Porto Alegre, Brazil); 2004 (Porto de Galinhas, Brazil); 2005 (Florianopolis)

"VHDL Forum for CAD in Europe":
1989 to 1998 (annual)

VLSI Design (VLSI):
1991 (New Dehli); 1992 (Bangalore); 1993 (Bombay); 1994 (Calcutta); 1995 (New Delhi);
1996 (Bangalore); 1997 (Hyderabad); 1998 (Madras); 1999 (Goa); 2000 (Calcutta); 2001 (Bangalore);
2003 (New Delhi); 2004 (Mumbai); 2005 (Kolkata)

Workshop on Design and Test of Defect and Fault Tolerant Nanoscal Architectures:
2005 (Palm Springs, CA)

Workshop France-Brazil:
1992 (Paris); 1996 (Rio de Janeiro)

Workshop on Fault Diagnosis and Tolerance in Cryptography:
2004 (Florence)

Workshop on Hardware-Software Codesign:
1994 (Grenoble)

European representation (or liaison) to Conferences and Workshops

- Built-In-Self-Test Workshop (several issues)
- Asian Test Symposium (several issues)
- High-Level Design Validation and Test Workshop (several issues)
- VLSI Design (several issues)
- MCM Conference (several issues)
- IC/Design Package Integration (1998)
- Memory Technology, Design and Testing (several issues)
- International Workshop on System Test and Diagnosis (1998)
- ICCAD (1996-1997)
- Steering Committee Member of the SASIMI Workshops (Japan)

Participation to Editorial Boards of Journals and Book Series

- CDTA
- IEEE Design and Test of Computers Magazine
- Journal of The Brazilian Microelectronics Society
- Computational Mechanics Publications
- Microelectronics Journal (Editor-in-Chief)
- IEEE Press Book Series
- Formal Methods in System Design
- ASME Journal of Electronic Packaging
- IEEE Transactions on Components and Packaging Technologies
- STUDIA INFORMATICA Journal
Organisation of Conferences

- **ACM Transactions in Embedded Computing Systems (TECS)**
- **IEEE Transactions on VLSI**

** ACM Transactions in Embedded Computing Systems (TECS)**

- **Advances Research Working Conference on Correct Hardware Design and Verification Methods (CHARME):**
  - 2005 (Saarbrücken, Germany, Co-General Chair)

**Asia Pacific Symposium on Microelectronics and MEMS (MICRO/MEMS):**

- 1999 (Gold Coast, Characterisation and Test Conference co-Chair)

**Colloque CAO de circuits intégrés et systèmes:**

- 1996 (Grenoble – Villard de Lans, Organizer); 1999 (Aix en Provence, Organizer)

**Copernicus Summer School: EDA standards:**

- 1997 (Prague, Organizer)

**Design Automation and Test in Europe (DATE):**

- 1998 (Paris; Vice-Program Chair); 1999 (Munich, Program Chair); 2000 (Paris, Vice-General Chair); 2001 (Munich, General Chair)

**Design, Test and Microfabrication of MEMS/MOEMS (DTM):**

- 1999 (Paris, General Chair)

**Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP):**

- 2000 (Paris, General Chair); 2001 (Cannes, General Chair); 2002 (Cannes, General Chair); 2003 (Cannes, General Chair); 2004 (Montreux, General Chair); 2005 (Montreux, General Chair)

**Electron and Optical Beam Testing of Integrated Circuits (EOBT):**

- 1987 (Grenoble, General Chair); 1989 (Duisburg, Program Chair); 1991 (Como, Program Chair); 1993 (Zurich, Program Chair); 1995 (Wuppertaal, Program Chair)

**EUROCHIP Workshop on VLSI Design Training (General Chair) (EUROCHIP):**

- 1991-1992 (Grenoble); 1993 (Toledo); 1994 (Dresden)

**European Conference on Design Automation / EUROASIC (EDAC-EUROASIC):**

- 1993 (Paris, General Chair)

**European Conference on Design Automation / European Test Conference / EUROASIC (ED&TC):**

- 1994 (Paris, Program Co-Chair)

**European Latin American Workshop on Europe – Latin America Cooperation on Circuits and Automation and Test (EURO-LAT):**

- 2005 (Grenoble, Organizer)

**European Micro and Nano System (EMN):**

- 2004 (Paris, Scientific Committee Chair)

**European Solid-State Circuits Conference - European Solid-State Device Research (ESSCIRC-ESSDERC):**

- 2005 (Grenoble, Co General Chair)

**European Workshop on Microelectronics Education (EWME):**

- 1996 (Grenoble, Co-Program Chair); 2000 (Aix en Provence, Co-Organizer)

**European Workshop on Radiation Hardened Electronics (EWRHE):**

- 2004 (Grenoble, Chair)

**Euro-VHDL:**

- 1996 (Geneva, Program Chair)
- **Forum on Design Languages (FDL):**
  1999 (Lyon, General Chair)

- **IEEE Latin-America Test Workshop (LATW):**
  2002 (Montevideo, General Chair)

- **IEEE Mixed-Signal Test Workshop (IMSTW):**
  1995 (Grenoble, General Chair); 2004 (Portland, Programme Chair); 2005 (Cannes, General Chair)

- **IEEE Workshop on On-Line Testing (IOLT):**
  1995 (Nice, General Chair); 1996 (Biarritz, General Chair); 1997 (Crete, General Chair); 1998 (Capri, General Chair); 1999 (Rhodes, General Chair); 2001 (Taormina, General Chair); 2002 (Isle of Bendor, General Chair); 2003 (Kos Island, Greece, Co-General Chair); 2004 (Funchal, Portugal, Program Chair); 2005 (St. Raphael, General Chair)

- **High-Level Design Validation and Test (HLDVT):**
  2002 (Cannes, General Chair)

- **IFIP ICAD:**
  2000 (Beijing, Co-Program Chair)

- **International Conference on Compilers Asian Green Electronics – Design for Manufacturability and Reliability (AGEC):**
  2005 (Pudong, China, General Chair)

- **International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES):**
  2002 (Grenoble, Co-Program Chair)

- **International Conference on Polymers and Adhesives in Microelectronics and Photonics (POLYTRONIC):**
  2003 (Montreux, General Chair)

- **International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT):**
  2001 (San Francisco; Co-Program Chair), 2002 (Vancouver; Co-General Chair); 2003 (Boston, Program Chair); 2004 (Cannes, General Chair)

- **International Symposium on Microelectronics and Assembly (ISMA):**
  2000 (Singapore, Program Chair)

- **International Symposium on System Synthesis (ISSS):**
  1995 (Cannes, Program Chair); 1996 (La Jolla, General Chair)

- **International Workshop on Hardware/Software Codesign (CODES):**
  1998 (Seattle, Co-Chair); 1999 (Rome, Co-General Chair)

- **MEDEA+ Design Automation Conference:**
  2004 (Stuttgart, Steering Committee); 2005 (Les Mesnuls, Steering Committee)

- **MEDEA-ESPRIT Workshop on Hardware-Software Codesign:**
  1998 (Grenoble, Chair)

- **Memory Technology; Design and Testing (MTDT):**
  2001 (San José, Co-General Chair); 2002 (Isle of Bendor, General Chair)

- **Modeling and Simulation of Microsystems; Semiconductors; Sensors and Actuators (MSM):**
  1999 (Puerto Rico, Co-Chair)

- **NATO ASI Course on Low Power Design in Deep Submicron Electronics:**
  1996 (Lucca, Organizer)

- **NATO ASI Course on System Level Design:**
  1998 (Organizers)
- **Radiation Effects on Circuits and Systems (RADECS):**
  2001 (Grenoble; General Chair)

- **Rapid System Prototyping Workshop (RSP):**
  1994 (Grenoble, General Chair); 1996 (Thessaloniki, Program Chair)

- **Thermal Challenges in Next Generation Electronic Systems (THERMES):**
  2002 (Santa Fe, Program Co-Chair)

- **Thermo-mechanical issues in Packaging and Assembly of MEMS and MOEMS; part of Photonics Fabrication Europe:**
  2002 (Brugges, Conference Chair)

- **VLSI Test Symposium (VTS):**
  1995-1996 (Princeton, Vice-Program Chair); 1997 (Monterey, Program co-Chair); 1998 (Monterey, Program Chair); 1999 (Dana Point, General Chair)

- **Workshop on Thermal Investigations in ICs and Systems (THERMINIC):**
  1995 (Grenoble, General Chair); 1996 (Budapest, General Chair); 1997-1998 (Cannes, General Chair); 1999 (Rome, General Chair); 2000 (Budapest, General Chair); 2001 (Paris, General Chair); 2002 (Madrid, General Chair); 2003 (Aix-en-Provence, General Chair); 2004 (Sofia-Antipolis, Côte d'Azur, France, General Chair); 2005 (Montreux, General Chair)

### Participation to Societies and Working Groups
- Member of IEEE/CS, IEEE/CPMT, ACM, IMAPS
- Member of IEEE European Test Technology Technical Committee
- Vice-Chair of Technical Activities of the IEEE Test Technology Technical Committee
- Chairman of the European Design and Automation Association (1994-1995)
- Chair of Thermal Testing Activities of the IEEE Test Technology Technical Committee
- Member of IEEE WG 1076.6: VHDL subset for Synthesis

### Others activities
- Review of papers for numerous Journals and Conferences
- Review of research proposals for EC, NSF, NATO, SERC

### 5-6 Awards and distinctions
- IEEE Meritorious service awards (1993)
- Doctor Honoris Causa of the Technical University of Budapest (1994)
- IEEE Computer Society's Golden Core member (1996)
- Best Paper Award ED&TC, 1995
- Best Poster Award IMAPS (1998)
- Best Poster Award FDL (1999)
- Best Paper Award DATE (1999)
- Award by Schlumberger Stiching Fund (1999)
- Best Paper Award DATE (2000)
- Best Paper Award HDLCON (2000)
- Best Paper Award VTS (2004)
- Best Dissertation Prize in Microelectronics (2005)
Bernard COURTOIS is conducting the sake barrel break (Picture 5-5 1) of Kagamiwari; a sake ceremony after an address (Picture 5-5 2) at the SASIMI Workshop (Tohoku: 1998)

Pictures 5-6 1 : Bernard COURTOIS is being awarded Doctor Honoris Causa of the Technical University of Budapest

Later, the President of INPG, Maurice RENAUD, congratulates him by remitting a sash, made to the colours of the city of Budapest

R. BIANCHI congratulated at the end of his thesis defence by Mr. Eric DONZIER from Schlumberger
R. BIANCHI has been awarded by Schlumberger for his results on the design of high temperature circuits systems
6 – Technology Transfer Activities

Besides their research and service activities, TIMA staff members are also concerned with technology transfer activities. For that purpose, they are regularly solicited to serve as consultant for technical and educational tasks, mainly by industrial companies, but also by foreign universities. Some results of these tasks have already been evoked throughout this report for the sake of consistency of the different sections, others only appear in this section. Up to now, the transfer technology activities have taken the forms detailed in the following :

6-1 Technical tasks

6-1.1 Industrial Transfers

- Transfer of a set of codesign tools to a TIMA spin-off. These include :
  1. COSMOS : a SDL based codesign environment.
  3. MCI : a multilanguage cosimulation tool supporting C, VHDL, MATLAB, SDL and COSSAP.
- VCI, an early C-VHDL cosimulation tool was transferred to STMicroelectronics since 1995. It was productized and used in several divisions in Grenoble and Bristol.
- Hits cells : Heavy ion tolerant memory cells, to Matra MHS/TEMIC. Hit memory cells were used to design a radiation hardened version of a digital signal processor : the TSC 21020 commercialised by TEMIC since November 1998.

6-1.2 Patents

TIMA Laboratory staff members have filed the following patents:

- Allier E., Fesquet L., Renaudin M., Sicard P.
  Procédé et dispositif de conversion analogique-numérique : publ. date 01/08/03; FR2835365
- Rezgui S., Velazco R.
  Method for error injection by interruptions : publ. date 19/07/02; FR2819603; eq. WO02056177
- Abrial A., Bouvier J., Senn P., Renaudin M., Vivet P.
  Composant micro-électronique intégrant des moyens de traitement numérique asynchrone et une interface de couplage électromagnétique sans contact : publ. date 05/01/01 ; FR2795891
- Hazard Ph., Karam J.M., Veychard D.
  Capteur thermoélectrique notamment pour appareils électriques : publ. date 19/11/99; FR2778742
- Moore D.F., Daniel J., Karam J.M.
  Micromechanical ring oscillator sensor : publ. date 15/04/98; GB2316231
- Bessot D., Velazco R.
  Memory cell insensitive to collisions of heavy ions : publ. date 07/06/97; US5640341; eq. EP0689713 (WO9422143), DE69414100D; DE69414100T; FR2702873; JP8512422T; WO9422143
- Vargas F.L., Nicolaidis M.
  Correction d'erreurs dans une mémoire : publ. date 15/12/95; FR2721135; eq. EP0765497, WO95334858, DE6950239T
- Nicolaidis M.
  Transparent techniques of integrated circuits : publ. date 21/11/95; US5469445; eq. EPO585435, GR92100088, WO9318457
- Armand M., Balme L., Silvy C.
  Supply component of the credit card type : publ. date 12/09/95; US5449994; eq. DE69207101D, DE69207101T, EP0524304
- Nicolaidis M.
  Fail safe interface for appts control - has inputs for receiving two binary control signals and concurrent checker which provides error detection signal if error exists in input signals : publ. date 09/03/95; WO9506908; eq. GR93100359
6-1.3 Industrial Circuit Fabrication

In addition to its service activity for university and research laboratory circuit fabrication, CMP is offering circuit fabrication services for industrial circuit prototyping and low volume production. Since its inception in 1990, CMP has fabricated over 720 industrial circuits, including 42 from France and 19 from foreign countries, for 100 companies and 20 universities/research laboratories.

The following consulting tasks have recently been achieved:

<table>
<thead>
<tr>
<th>Company</th>
<th>TIMA member</th>
<th>Duration</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPCS/IN2P5, France</td>
<td>K. Torki</td>
<td>1 week</td>
<td>2005</td>
</tr>
<tr>
<td>IXL/CNRS, Bordeaux</td>
<td>K. Torki</td>
<td>1 week</td>
<td>2004</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>2 weeks</td>
<td>2003</td>
</tr>
<tr>
<td>iRoC Technologies</td>
<td>R. Velazco</td>
<td>1 month</td>
<td>2001</td>
</tr>
<tr>
<td>Univ. of Tohoku - Japan</td>
<td>K. Torki</td>
<td>1 day</td>
<td>2000</td>
</tr>
<tr>
<td>VDEC – Tokyo -Japan</td>
<td>K. Torki</td>
<td>2 days</td>
<td>2000</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>M. Nicolaidis</td>
<td>8 days</td>
<td>1999</td>
</tr>
<tr>
<td>CORNING SA</td>
<td>K. Torki</td>
<td>1 week</td>
<td>1999</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>1 week</td>
<td>1999</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>3 weeks</td>
<td>1999</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>8 weeks</td>
<td>1999</td>
</tr>
<tr>
<td>CEA/LETI</td>
<td>K. Torki</td>
<td>2 weeks</td>
<td>1999</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>2 months</td>
<td>1998</td>
</tr>
<tr>
<td>Univ. of Rome</td>
<td>K. Torki</td>
<td>6 days</td>
<td>1998</td>
</tr>
<tr>
<td>Mentor Graphics Corp.</td>
<td>M. Nicolaidis</td>
<td>10 days</td>
<td>1996-97</td>
</tr>
<tr>
<td>Alcatel/Alsthom (France)</td>
<td>M. Nicolaidis</td>
<td>2 days</td>
<td>1994</td>
</tr>
<tr>
<td>AMS (Austria)</td>
<td>K. Torki</td>
<td>8 months</td>
<td>1991-93</td>
</tr>
<tr>
<td>IN2P3/LAL (France)</td>
<td>K. Torki</td>
<td>5 days</td>
<td>1992</td>
</tr>
</tbody>
</table>
6-1.5 Creation of spin-off companies

These start-up companies have been recently created by members of the Laboratory. The Press Releases issued at the time of the launching are reproduced below.

6-1.5.1 MEMSCAP

MEMSCAP® : a TIMA spin-off specialized in MEMS

Grenoble, France - December 1997. The challenges in Telecommunication, Automotive, Aerospace and Biomedical system design using Micro Electro Mechanical Systems (MEMS) have been clearly identified. To address this increasing demand, MEMSCAP®, a commercial spin-off from TIMA Laboratory research, provides Intellectual Properties (IP) enabling system designers to get access to the MEMS technology without excessive complexity and design time and cost. Very wide range temperature sensors, IR detectors, inertial sensors and other MEMS devices can be directly purchased in both software or hardware forms.

The company is starting with 7 engineers, mainly composed from researchers getting out from the Microsystems Group of TIMA Laboratory. This group will keep a staff of 15 researchers addressing joint long and medium term research activities on CAD of MEMS, fault modeling, MEMS testing methodologies, microelectronics compatible manufacturing techniques and new MEMS device generations (e.g. Active Pixel Sensors, etc.). In addition, the CMP service will be the preferred source for prototyping and low-volume production of Integrated Circuits, MEMS and Multi-Chip-Modules for MEMSCAP®.

MEMSCAP® design solution enables system designers to fully leverage MEMS component behavioral models in HDL-A\(^1\) (soon into VHDL-AMS and Verilog-A standards) for system-level verification and manufacturability analysis, by providing technology specific MEMS Engineering Kits, Model Generation Tools and Services and MEMS Intellectual Properties.

MEMSCAP® is predicting 10 million dollars of turn-over in 2001. The company has already received the support of the Centre National d'Etudes Spatiales (CNES) in France, for the qualification of space technologies for MEMS and has established a partnership with Mentor Graphics Corporation in the area of CAD of MEMS.

6-1.5.2 AREXSYS

Start-up forms in Grenoble, France to deliver system design software for embedded systems

San-Fransisco, CA (Design Automation Conference) - June 15, 1998 - The founders of the Syntyx Technology project in Grenoble, France, today announced the formation of Arexsys, Inc. to deliver an innovative hardware/software co-design solution for embedded system and system-on-chip (SOC) designs. François Constant, formerly regional manager of Southern Europe for Synopsys Inc., was named president and chief executive officer. In addition to Constant, Arexsys founders include Ahmed Jerraya, research director at the TIMA laboratory, and Jean-Pierre Moreau, director of research partnerships at STMicroelectronics.

Arexsys' solutions are used as a high level front-end to industry standards EDA tools such as register-transfer level (RTL) synthesis and digital signal processing (DSP) design tools. The technology supports a full top-down system design methodology, reading and writing multi-languages description and performing co-simulation at any level.

In contrast to other system-level design products that use proprietary languages, the Arexsys tools use SDL, the industry standard design language used by more than 25,000 system designers worldwide.

Currently, system-level designers write SDL description to map out the major functional blocks in the system and then have to painstakingly hand-code a behavioral or RTL description, deciding piece by piece what gets implemented in hardware vs. software. Arexsys automates this process: the tools read in an SDL description, designers interactively partition the design into hardware and software, and the tools then compile the design into RTL hardware and low-level C software. Designers then send the RTL hardware portion to a hardware description language (HDL) synthesis tool to create gates.

Arexsys automatically generates the interfaces required for communication between the hardware and the software at the RT level. Designers can explore different combinations of hardware and software along the way until the optimum solution is reached.

The company expects to have its products into beta sites this summer, and to have production software ready by end of 1998.

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\(^1\) HDL-A is a registered trademark of Mentor Graphics Corporation.
A new start-up takes on soft errors challenge

Grenoble, France – March 13, 2000 - iRoC Technologies is providing unique and global design solutions for integrating Robustness on Chip, and is taking on one of the biggest challenges in the semiconductor industry: the "transient errors" issue.

Soft Errors, coming from cosmic rays or alpha particles, and timing faults, coming from crosstalk, may stop the very deep submicron scaling progress.

A commercial spin-off from TIMA laboratory research in Grenoble, France, iRoC Technologies offers a new design methodology to provide a breakthrough, by using fault tolerance concepts.

Michael NICOLAIDIS, leader of the Reliable Integrated Systems group at TIMA Laboratory warns that technological progress in the semiconductor industry will be stunted abruptly if no specific actions are taken to cope with increasingly high soft-error rates and undetected timing faults, at reasonable costs.

iRoC's products will consist in design tools for automatic fault tolerance insertion. iRoC combines a group of optimized circuits in a global technology named " Transient Fault Tolerant Architecture" (TFTArchitecture™).

"This TFTArchitecture™ is the result of a 5 years technology development by Michael NICOLAIDIS and his group" said Bernard COURTOIS, TIMA Director. "We trust TFTArchitecture™ technology, which is based on a portfolio of international patents, to be the most effective technology to protect ICs against soft-errors" he added.

Reduced power supply levels and the size of device, as well as increased operating speeds are known to dramatically affect the sensitivity of very deep submicron scaling technologies, to noise and in particular to alpha particles and cosmic rays.

In the VLSI era, drastic reliability improvements reserved the costly technology “fault tolerance” in a narrow domain of high-end products. In the near future, increased sensitivity to perturbations will block the very deep submicron scaling. It is making fault tolerance mandatory, even for commodity products.

"Timing defects are a currently key problem in the semiconductor industry and soft errors are a major challenge for next generation of ICs. I strongly believe that ICs – at least 10% for the 180nm and 50% for the 130nm- will have to be fault tolerant. iRoC Technologies is providing the unique low-cost full solution for ICs and IPs, facing these challenges" said Eric DUPONT, President and CEO of iRoC Technologies.

In addition, iRoC Technologies provides professional services to characterize and simulate TFTArchitecture™ performance and cost on commercial deep submicron ICs.

The founders of iRoC Technologies include Dr Michael NICOLAIDIS, leader of the Reliable Integrated Systems group at TIMA, Dr Jean-Michel KARAM, President and CEO of MEMScAP, Dr Bernard COURTOIS, Director of TIMA, Joel RODRIGUEZ-ALANIS, CEO of Mentor/Anacad and Eric DUPONT, President and CEO.

6-1.6 Technical Advisory Board membership

Members of the Laboratory are presently on the Technical Advisory Boards of the following companies :

- STMicroelectronics,
- MEMSCAP,
- VALIOSYS.

In the past, a member of the Laboratory has been on the Technical Advisory Board of SUNRISE.

6-2 Educational tasks

Dealing with problems arisen by advanced technologies and proposing advanced design and test methodologies, TIMA staff members are, as a matter of course, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into five categories : courses and tutorials, seminars, support of - or participation in - foreign university teaching programs, participation in EU educational and technology transfer programs, direction of Ph.D. students employed by French industrial companies (CIFRE program), and finally, an interactive course is described.
### 6.2.1 Courses and tutorials

The following table lists courses and tutorials that have been organized and given by members of the Laboratory, at different institutions request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA staff or externally.

<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Organizer</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPG</td>
<td>Grenoble, France</td>
<td>2/05</td>
<td>4 hours</td>
<td>L. Anghel</td>
<td>Crossing 100nm and beyond</td>
</tr>
<tr>
<td>FORMATECH</td>
<td>INPG, Grenoble, France</td>
<td>2/05</td>
<td>8 hours</td>
<td>S. Mir</td>
<td>Introduction aux microsystèmes sur silicium</td>
</tr>
<tr>
<td>Slovak Academy of sciences</td>
<td>Smolenic Castle, Slovakia</td>
<td>9/04</td>
<td>5 days</td>
<td>A.A. Jerraya</td>
<td>SoC’04</td>
</tr>
<tr>
<td>Zenasis Technologies</td>
<td>Campell, CA USA</td>
<td>8/04</td>
<td>4 hours</td>
<td>L. Anghel</td>
<td>Low Power: Optimization and Estimation Techniques</td>
</tr>
<tr>
<td>Universitat de Girona</td>
<td>Girona, Spain</td>
<td>7/04</td>
<td>4 hours</td>
<td>S. Mir</td>
<td>Mixed-signals integrated circuit testing - an overview</td>
</tr>
<tr>
<td>IEEE Circuits &amp; Systems Society and in-cooperation with EDAA</td>
<td>St Maximin, France</td>
<td>7/04</td>
<td>4 days</td>
<td>A.A. Jerraya</td>
<td>4th International Seminar on Application-Specific Multi-Processor SoC</td>
</tr>
<tr>
<td>La Revue d’ASPROM</td>
<td>Bresson, Grenoble, France</td>
<td>5/04</td>
<td>2 days</td>
<td>A.A. Jerraya</td>
<td>Les Systèmes monopuces</td>
</tr>
<tr>
<td>INPG</td>
<td>Grenoble, France</td>
<td>5-6/04</td>
<td>8 hours</td>
<td>L. Anghel</td>
<td>Conception VLSI Formation Continue MIDEP</td>
</tr>
<tr>
<td>Canal Industries</td>
<td>Paris, France</td>
<td>3/04</td>
<td>3 hours</td>
<td>R. Velazco</td>
<td>Contraintes radiatives &amp; parades</td>
</tr>
<tr>
<td>TIMA Lab.</td>
<td>Autrans, France</td>
<td>3/04</td>
<td>3 days</td>
<td>R. Velazco</td>
<td>Synchronisation des circuits électroniques</td>
</tr>
<tr>
<td>INPG</td>
<td>Grenoble, France</td>
<td>2/04</td>
<td>4 hours</td>
<td>L. Anghel</td>
<td>Design for Testability Formation continue en microélectronique</td>
</tr>
<tr>
<td>INPG</td>
<td>Grenoble, France</td>
<td>2/04</td>
<td>8 hours</td>
<td>L. Anghel</td>
<td>Design for Testability Formation continue en microélectronique</td>
</tr>
<tr>
<td>Libanese University</td>
<td>Tripoli, Lebanon</td>
<td>1/04</td>
<td>3 jours</td>
<td>L. Anghel</td>
<td>ASIC versus FPGA</td>
</tr>
<tr>
<td>Ecole Polytechnique de l'Université Grenoble</td>
<td>Grenoble, France</td>
<td>12/03</td>
<td>1,5 hours</td>
<td>S. Mir</td>
<td>Mixed-signals testing - A tutorial on testing of integrated analogue, mixed-signal and MEMS devices</td>
</tr>
<tr>
<td>SOREP/INPG</td>
<td>Grenoble, France</td>
<td>8/03</td>
<td>2 weeks</td>
<td>K. Torki</td>
<td>Training courses on digital DSM design flow (front-end and back-end)</td>
</tr>
<tr>
<td>ESRF</td>
<td>Grenoble, France</td>
<td>8/03</td>
<td>2 weeks</td>
<td>K. Torki</td>
<td>Automatic place &amp; route support and expertise for a mixed A/D design</td>
</tr>
<tr>
<td>European Design and Automation Association</td>
<td>Hotel Alpina Chamonix, France</td>
<td>7/03</td>
<td>4 days</td>
<td>A.A. Jerraya</td>
<td>International Seminar on Multi-Processor SoC</td>
</tr>
<tr>
<td>ISIM, Inst. des Sciences de l’Ingénieur</td>
<td>Montpellier, France</td>
<td>1/03</td>
<td>3 hours</td>
<td>M. Renaudin</td>
<td>Asynchronous Circuits and Systems</td>
</tr>
<tr>
<td>EDAA European Design &amp; Automation Association</td>
<td>Chamonix, France</td>
<td>7/03</td>
<td>5 days</td>
<td>A. Jerraya &amp; W.H. Wolf</td>
<td>Summer School on Multi-Processor SoC</td>
</tr>
<tr>
<td>EDAA European Design &amp; Automation Association</td>
<td>Chateau de Pizay, France</td>
<td>7/02</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>2nd Summer School on Application-Specific Multi-Processor SoC</td>
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<tr>
<td>ACID-WG</td>
<td>Grenoble</td>
<td>7/02</td>
<td>5 days</td>
<td>M. Renaudin</td>
<td>Summer School on Asynchronous Circuit Design</td>
</tr>
<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>7/02</td>
<td>5 days</td>
<td>M. Renaudin &amp; R. Leveugle</td>
<td>Conception de circuit</td>
</tr>
<tr>
<td>(I)ISIM inst. des Sciences de l’Ingénieur</td>
<td>Montpellier</td>
<td>1/02</td>
<td>3 h</td>
<td>M. Renaudin</td>
<td>Asynchronous Circuits and Systems</td>
</tr>
<tr>
<td>IEEE Circuits &amp; Syst Society EDAA</td>
<td>Aix-les-Bains</td>
<td>7/01</td>
<td>4 days</td>
<td>A. Jerraya</td>
<td>Application-Specific Multi-Processor SoC: Summer School</td>
</tr>
<tr>
<td>TEMPRA</td>
<td>Monastir</td>
<td>6/01</td>
<td>6 days</td>
<td>K. Torki</td>
<td>Deep Sub-Micron front to back design methodology</td>
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<tr>
<td>Eurotraining</td>
<td>Grenoble</td>
<td>5/01</td>
<td>3 days</td>
<td>K. Torki</td>
<td>System-On-Chip Advanced Course</td>
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<tr>
<td>MIGAS</td>
<td>Autrans</td>
<td>6/00</td>
<td>6 days</td>
<td>M. Renaudin</td>
<td>International Summer School on Advanced Microelectronics</td>
</tr>
</tbody>
</table>
### Technology Transfer Activities

<table>
<thead>
<tr>
<th>Event</th>
<th>Location</th>
<th>Duration</th>
<th>Speaker(s)</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>AciD-WG Workshop</td>
<td>Grenoble</td>
<td>1/00</td>
<td>M. Renaudin</td>
<td>Asynchronous Circuit Design Workshop</td>
</tr>
<tr>
<td>SSDM 2000 Short Course</td>
<td>Japan</td>
<td>8/00</td>
<td>K. Torki</td>
<td>RF Analog Circuits and Layout Techniques</td>
</tr>
<tr>
<td>INTELECT Sum. Course</td>
<td>Sweden</td>
<td>8/00</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
</tr>
<tr>
<td>ASP-DAC 2000</td>
<td>Japan</td>
<td>1/00</td>
<td>A. Jerraya</td>
<td>Multilanguage System Design</td>
</tr>
<tr>
<td>SDL Forum</td>
<td>Canada</td>
<td>6/99</td>
<td>A. Jerraya</td>
<td>Hardware/Software Codesign from SDL</td>
</tr>
<tr>
<td>DATE 99</td>
<td>Germany</td>
<td>3/99</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
</tr>
<tr>
<td>DATE 99</td>
<td>Germany</td>
<td>3/99</td>
<td>A. Jerraya</td>
<td>R. Ernst</td>
</tr>
<tr>
<td>NATO School</td>
<td>Italy</td>
<td>8/98</td>
<td>A. Jerraya</td>
<td>Codesign</td>
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<tr>
<td>Internat. Course</td>
<td>Taiwan</td>
<td>12/98</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
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<td>Internat. Course</td>
<td>Tokyo</td>
<td>12/97</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
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<td>Internat. Course</td>
<td>Grenoble</td>
<td>10/96</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
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<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/95</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
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<td>ST Course</td>
<td>Grenoble</td>
<td>04/95</td>
<td>A. Jerraya</td>
<td>High-Level Synthesis</td>
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<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/94</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>12/94</td>
<td>M. Lubaszewski</td>
<td>Mixed-Signal Testing</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Irvine-CA</td>
<td>11/94</td>
<td>A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/Chipshop</td>
<td>Grenoble</td>
<td>04/94</td>
<td>K. Torki</td>
<td>VLSI Design on PC platforms</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>04/94</td>
<td>A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
</tbody>
</table>

#### 6-2.2 Seminars

In addition to internal seminars, the Laboratory regularly invites people from Grenoble academic and industrial environment to attend the talks given by our visiting researchers. These people have recently had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. Archie Yan-Cheong CHAN</td>
<td>City University, Hong Kong</td>
<td>03/05</td>
<td>Réduction des substances dangereuses en électronique</td>
</tr>
<tr>
<td>Prof. J. Machado da Silva</td>
<td>Faculdade de Engenharia da Universidade do Porto, INESC-Porto, Portugal</td>
<td>02/05</td>
<td>Analogue and mixed-signal testing activity at INESC-Porto</td>
</tr>
<tr>
<td>Dr. Man WONG</td>
<td>Hong Kong University of Science and Technology</td>
<td>07/04</td>
<td>Low-Temperature Electroplating Technology for Integrated Micro-Systems</td>
</tr>
<tr>
<td>Prof. Vojin G. Oklobdzija</td>
<td>ACSE Lab, University of California Davis, USA</td>
<td>06/04</td>
<td>Energy Minimization Method for Optimal Energy-Delay</td>
</tr>
<tr>
<td>Prof. Christian Piguet</td>
<td>CSEM, Jaquet-Droz 1, CH-2000 Neuchatel, Switzerland</td>
<td>06/04</td>
<td>Leakage and Total Power Reduction at Architectural Level</td>
</tr>
<tr>
<td>Dr Nabil Sabry</td>
<td>CIDRE – Egyptian France University</td>
<td>05/04</td>
<td>Modélisation de l’écoulement et du transfert thermique dans les micro-canaux</td>
</tr>
<tr>
<td>Prof. Warren Hunt</td>
<td>Texas University Austin, USA</td>
<td>10/03</td>
<td>Linear and non-linear arithmetic in ACL2</td>
</tr>
<tr>
<td>Prof. Kazuya Masu</td>
<td>Precision and Intelligence Laboratory, Tokyo Institute of Technology</td>
<td>10/03</td>
<td>GHz Interconnect in Multilevel ULSSI Interconnection</td>
</tr>
<tr>
<td>Prof. P.R. Mukund</td>
<td>Rochester Institute of Technology, USA</td>
<td>10/03</td>
<td>Chip-Package Co-Design of RF Microsystems</td>
</tr>
<tr>
<td>Prof. Ali Shakouri</td>
<td>University of California at Santa Cruz</td>
<td>10/03</td>
<td>Nanoscale Devices for Nanoscale Devices for Opto Thermo Electronic Energy Conversion</td>
</tr>
<tr>
<td>Soc-Ik Chae</td>
<td>Center for SoC Design Technology / Seoul National University - KOREA</td>
<td>09/03</td>
<td>Energy measurement in CMOS circuits</td>
</tr>
<tr>
<td>Roy Emek</td>
<td>IBM Research Laboratory in Haifa, Israel</td>
<td>07/03</td>
<td>Model-Based Test-Case Generator for Systems on a Chip (SoCs)</td>
</tr>
<tr>
<td>Prof. Jan M. Rabaey</td>
<td>GSRC, University of California at Berkeley</td>
<td>05/03</td>
<td>The Gigascale Silicon ResearchCenter: Past, Present and Future</td>
</tr>
<tr>
<td>Prof. Stanislaw J. Pietrak</td>
<td>Université de Technologie, Wroclaw, Pologne</td>
<td>04/03</td>
<td>RNS (Residue Number System - l’arithmétique des nombres résidus) : ses applications au traitement numérique du signal pour performance, basse consommation et reconfiguration</td>
</tr>
<tr>
<td>Salil Desai</td>
<td>Dept. of Electrical Engin. &amp; Comp. Science at MIT, USA</td>
<td>01/03</td>
<td>Measuring Motions of MEMS/MST</td>
</tr>
<tr>
<td>Prof. Vincent John Mooney III</td>
<td>Georgia Institute of Technology, USA</td>
<td>12/02</td>
<td>Design of a Hardware/Software RTOS for SoC</td>
</tr>
<tr>
<td>Luca Benini</td>
<td>DEIS Università di Bologna, Italy</td>
<td>09/02</td>
<td>On-Chip Networks: designing the communication fabric for next-generation SoCs</td>
</tr>
<tr>
<td>Gary Swift</td>
<td>JPL/NASA</td>
<td>09/02</td>
<td>A Brief History of Memory Devices and Single-Event Upset in Space</td>
</tr>
<tr>
<td>Name</td>
<td>Affiliation</td>
<td>Date</td>
<td>Title</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>----------------------------------</td>
<td>-------</td>
<td>-------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Frédéric Petrot</td>
<td>Laboratoire LIP6, Université Pierre et Marie Curie (Paris VI)</td>
<td>09/02</td>
<td>Digital System Design Environment - Une méthode et des outils pour la conception de SoCs</td>
</tr>
<tr>
<td>Renate Sitte</td>
<td>Griffith University, Australia</td>
<td>06/02</td>
<td>MEMS Virtual Prototyping CAD Tool for Robust Design</td>
</tr>
<tr>
<td>David Moulinier</td>
<td>MEMSCAP, Saint-Ismier</td>
<td>06/02</td>
<td>MEMS Master: A tool for fast MEMS prototyping</td>
</tr>
<tr>
<td>Flavio Rech Wagner</td>
<td>Universidade Federal do Rio Grande do Sul, Brazil</td>
<td>05/02</td>
<td>Intégration d’outils et de composants IP dans un environnement de conception au niveau système</td>
</tr>
<tr>
<td>G. Martin*</td>
<td>*Cadence; **Infineon; ***STMicroelectronics</td>
<td>01/02</td>
<td>VCC: A Tool For HW/SW Codesign and Architectural Space Exploration</td>
</tr>
<tr>
<td>Prof. G. De Micheli</td>
<td>Stanford University, USA</td>
<td>12/01</td>
<td>Network on a chip: a new paradigm for System on Chip design</td>
</tr>
<tr>
<td>Warren A. Hunt, Jr.</td>
<td>IBM Austin Res. Lab., Univ. of Texas, USA</td>
<td>06/01</td>
<td>Verification at IBM and the FM9801 Microprocessor Verification</td>
</tr>
<tr>
<td>Luciano Lavagno</td>
<td>Univ. of Udine, Italy</td>
<td>04/01</td>
<td>Embedded system design</td>
</tr>
<tr>
<td>Vojin Oklobdzija</td>
<td>Univ. de Californie, Davis, USA</td>
<td>03/01</td>
<td>Clocked storage elements: master-slave latches and flip-flops for high performance and low power systems</td>
</tr>
<tr>
<td>Skandar Basrour</td>
<td>Univ. Franche-Comté, Besançon</td>
<td>03/01</td>
<td>Conception et réalisation de micro-résonateurs à mode de Lamé</td>
</tr>
<tr>
<td>Philippe Jorrand</td>
<td>Laboratoire LEIBNIZ, Grenoble</td>
<td>03/03</td>
<td>Informatique quantique : principes et algorithmes</td>
</tr>
<tr>
<td>Traian Muntean</td>
<td>CNRS (TIMA) &amp; Univ. de la Méditerranée</td>
<td>12/00</td>
<td>Global Communicating Systems (A distributed refinement design model)</td>
</tr>
<tr>
<td>Sergio Martinez</td>
<td>Tima Lab, Grenoble, France</td>
<td>12/00</td>
<td>Silicon Micromachined Cross-Connects in Optical Networks</td>
</tr>
<tr>
<td>Steven P. Levitan</td>
<td>Univ. of Pittsburgh</td>
<td>12/00</td>
<td>CAD Tools and Modeling Challenges for Optoelectronic System</td>
</tr>
<tr>
<td>Saeyang Yang</td>
<td>SEVITS Technology Inc., Pusan, Korea</td>
<td>10/00</td>
<td>Simulation + Emulation : A New Hope in Verification Crisis ?</td>
</tr>
<tr>
<td>Jean-Luc Lambert</td>
<td>Valiosys SA, Caen, France</td>
<td>10/00</td>
<td>LPV: a new technique, based on linear programming, to formally prove or disprove safety properties on software and hardware systems</td>
</tr>
<tr>
<td>Gary M. Swift</td>
<td>California Inst. of Tech., Passadena, Ca., USA</td>
<td>09/00</td>
<td>Measurements of the Power PC750 Upset Susceptibility to Protons and Heavy Ions</td>
</tr>
<tr>
<td>K. Chakrabarty</td>
<td>Duke Univ., USA</td>
<td>07/00</td>
<td>Optimization problems in system-on-chip test automation</td>
</tr>
<tr>
<td>F. Vargas</td>
<td>Univ. of Porto Alegre, Brazil</td>
<td>07/00</td>
<td>Les dernières avancées sur les descriptions VHDL : tolérance aux fautes transitoires et estimation de la fiabilité</td>
</tr>
<tr>
<td>D. Bouldin</td>
<td>Univ. of Tennessee, USA</td>
<td>05/00</td>
<td>Enhancing System-level education with reusable designs</td>
</tr>
<tr>
<td>F. Anceau</td>
<td>CNAM, Paris</td>
<td>12/99</td>
<td>Vers une étude objective de la conscience</td>
</tr>
<tr>
<td>A. Jantsch</td>
<td>Royal Inst. of Technol., Sweden</td>
<td>08/99</td>
<td>System-level cosimulation with SDL and Matlab</td>
</tr>
<tr>
<td>P. Franzon</td>
<td>North Carolina State University, USA</td>
<td>07/99</td>
<td>Microsystems and VLSI – Wireless and other applications</td>
</tr>
<tr>
<td>M. Renaudin</td>
<td>TIMA</td>
<td>06/99</td>
<td>ASPRO : un microprocesseur asynchrone</td>
</tr>
<tr>
<td>P. Vivet</td>
<td>CENT/DTMCET</td>
<td>06/99</td>
<td>Synthesis and optimization of algorithmic hardware descriptions</td>
</tr>
<tr>
<td>S. Kundu and S. Sengupta</td>
<td>Intel, Santa Clara, USA</td>
<td>03/99</td>
<td>Technology development directions for Microprocessor test at Intel</td>
</tr>
<tr>
<td>J. Memmet /A.A. Jerraya</td>
<td>NATO</td>
<td>98</td>
<td>System level synthesis</td>
</tr>
<tr>
<td>K. Torky</td>
<td>Cadence</td>
<td>98</td>
<td>Deep submicron design</td>
</tr>
<tr>
<td>L. Semeria</td>
<td>Univ. of Stanford, USA</td>
<td>12/98</td>
<td>Synthesis from C : issues and resolution of pointers</td>
</tr>
<tr>
<td>J. Madrenas</td>
<td>UPC Barcelona, Spain</td>
<td>07/98</td>
<td>The field-programmable system-on-chip mixed circuit</td>
</tr>
<tr>
<td>R. Douence</td>
<td>IRISA, Rennes</td>
<td>04/98</td>
<td>Architectures logicielles et wright</td>
</tr>
<tr>
<td>Dr. P. Wodey</td>
<td>ISIMA, Clermont-Ferrand</td>
<td>01/98</td>
<td>Méthodologie et outils de codesign à partir de E-LOTOS</td>
</tr>
</tbody>
</table>

**Picture 6-2.11 (a,b,c) :** AMICAL seminars (Tokyo, October 1993 and Singapore, December 1993) and International Course on Hardware-Software codesign (Tokyo, December 1997)
Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions.

<table>
<thead>
<tr>
<th>Institution</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Speaker</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISEP, Paris</td>
<td>ISEP, Paris</td>
<td>11/03</td>
<td>1 day</td>
<td>M. Renaudin, L. Fesquet</td>
<td>Asynchronous Circuits Design</td>
</tr>
<tr>
<td>UFGRS, Brazil</td>
<td>UFGRS, Brazil</td>
<td>09/03</td>
<td>2 days</td>
<td>M. Renaudin, Fragoso J., Reis R.</td>
<td>Asynchronous Circuits Design</td>
</tr>
<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>01/02</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
</tr>
<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>01/01</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
</tr>
<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>01/00</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
</tr>
<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>01/99</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
</tr>
<tr>
<td>Univ. of Chile</td>
<td>Chile</td>
<td>11/98</td>
<td>20h</td>
<td>R. Velazco</td>
<td>Artificial neural networks implementation</td>
</tr>
</tbody>
</table>

6-2.3 Support of universities teaching programs

The Laboratory has established for many years solid contacts with other research institutions and universities throughout the world. Exchange of students and post-doctoral fellows are very common, and TIMA members are often invited to participate in foreign university teaching programs. The following table lists this kind of activities during the recent academic years.

<table>
<thead>
<tr>
<th>University</th>
<th>Country</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISIM Montpellier</td>
<td>France</td>
<td>12/95</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Microelectronics</td>
</tr>
<tr>
<td>ISEP Paris</td>
<td>France</td>
<td>11/95</td>
<td>5 days</td>
<td>P. Kission</td>
<td>AMICAL</td>
</tr>
<tr>
<td>Ecole Poly.Fédérale Zürich</td>
<td>Switzerland</td>
<td>05/95</td>
<td>3h</td>
<td>I. Bacivarov</td>
<td>Dependability of distributed systems</td>
</tr>
<tr>
<td>Universität de Monastir</td>
<td>Tunisia</td>
<td>05/95</td>
<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Univ. de Las Palmas</td>
<td>Canarias</td>
<td>05/95</td>
<td>4h</td>
<td>A. Guyot</td>
<td>Garden Ws.: Operators in GaAs</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>02/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>CMOS circuitry</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>01/95</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Arithmetic</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>11/95</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>12/94</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>Universität de Monastir</td>
<td>Tunisia</td>
<td>06/94</td>
<td>3h</td>
<td>M. Marzouki</td>
<td>Partial Boundary Scan Test</td>
</tr>
<tr>
<td>Politechnica Bucharest</td>
<td>Romania</td>
<td>05/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>CMOS VLSI design course</td>
</tr>
</tbody>
</table>
6-2.4 Participation in EU educational programs

TIMA Laboratory activities have a strong European profile. In addition to numerous research projects listed in other sections of this report, the following table indicates the involvement of TIMA staff members in educational programs launched by the European Union. This involvement take the form of organizing and/or teaching courses.

<table>
<thead>
<tr>
<th>Framework</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>EUROPRACTICE COURSE</td>
<td>Germany</td>
<td>09/97</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>Test Technology for Digital and Mixed-Signal ASICs and MCMs</td>
</tr>
<tr>
<td>EUROPRACTICE COURSE</td>
<td>Germany</td>
<td>09/97</td>
<td>3h</td>
<td>R. Velazco</td>
<td>On-Line Testing for VLSI</td>
</tr>
<tr>
<td>Comett</td>
<td>Netherlands</td>
<td>09/95</td>
<td>3days</td>
<td>Kission/Rahm.</td>
<td>AMICAL</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>09/95</td>
<td>5days</td>
<td>Jerraya/Kission</td>
<td>System design</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Denmark</td>
<td>08/95</td>
<td>5days</td>
<td>A. Jerraya</td>
<td>Co-design</td>
</tr>
<tr>
<td>Comett</td>
<td>Austria</td>
<td>04/95</td>
<td>3days</td>
<td>C. Liem</td>
<td>Reconfigurable architecture</td>
</tr>
<tr>
<td>JTTC Comett II</td>
<td>Greece</td>
<td>12/94</td>
<td>15h</td>
<td>M. Nicolaidis</td>
<td>Advanced Course on VLSI Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>08/94</td>
<td>6h</td>
<td>A. Jerraya</td>
<td>System Design</td>
</tr>
<tr>
<td>JTTC Comett II</td>
<td>Italy</td>
<td>02/94</td>
<td>1h</td>
<td>M. Nicolaidis</td>
<td>European School on High Reliability Integrated Systems</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Germany</td>
<td>02/94</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>France</td>
<td>12/92</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>JTTC Comett II</td>
<td>Greece</td>
<td>02/92</td>
<td>15h</td>
<td>A. Guyot</td>
<td>VLSI Design Course teaching</td>
</tr>
</tbody>
</table>

6-2.5 University/industry joint research programs

A French national program, called CIFRE, allows French companies to receive French Ph.D. students. The thesis director must belong to a French University or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company.

TIMA staff members have been asked by companies to direct several Ph.D. theses in the CIFRE framework. The most recent ones are listed in the table below.

<table>
<thead>
<tr>
<th>Company</th>
<th>Student</th>
<th>Director</th>
<th>Dur.</th>
<th>Research Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST Microelectronics</td>
<td>J. Goulier</td>
<td>M. Renaudin</td>
<td>05-08</td>
<td>Reconfigurable Analog to Digital converters for multistandard reception systems</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>P. Vanhauwaert</td>
<td>R. Leveugle</td>
<td>04-07</td>
<td>Fault-injection based dependability analysis in FPGA-based Prototyping environment</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>L. Rolindez</td>
<td>S. Mir</td>
<td>03-06</td>
<td>BIST of analogue and mixed-signal integrated circuits with emphasis on Sigma-Delta</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td>R. Kheriji</td>
<td>S. Mir</td>
<td>03-06</td>
<td>Structural testing of RF circuits for optimising production test sets</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>A. Blampey</td>
<td>A. Jerraya</td>
<td>03-06</td>
<td>Platform-based rapid prototyping method</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>M. Fiandino</td>
<td>A. Jerraya</td>
<td>03-06</td>
<td>Definition of a new approach for the integration of a network-on-chip with 1000+ heterogeneous processors</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>L. Perialisi</td>
<td>A. Jerraya</td>
<td>03-06</td>
<td>Modeling of a flexible communication network for SoC</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>F. Hunsinger</td>
<td>A. Jerraya</td>
<td>03-06</td>
<td>Global validation method for SoC</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>L. Tambour</td>
<td>A. Jerraya</td>
<td>00-03</td>
<td>A Methodology and Semi-Automated Flow for Design and Validation of Digital Signal Processing ASIC</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>J. Quartana</td>
<td>M. Renaudin</td>
<td>00-03</td>
<td>Asynchronous IC, On-Chip Bus Architectures &amp; Protocols, HW/SW Interfaces/</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>D. Panyasak</td>
<td>M. Renaudin</td>
<td>00-03</td>
<td>Low Noise Asynchronous Circuit Design</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>Ph. Guillaume</td>
<td>A. Jerraya</td>
<td>96-98</td>
<td>Low-power</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>F. Naçabal</td>
<td>A. Jerraya</td>
<td>95-96</td>
<td>Heterogeneous System Design</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>E. Berrebi</td>
<td>A. Jerraya</td>
<td>93-96</td>
<td>Heterogeneous System Design</td>
</tr>
<tr>
<td>IMD</td>
<td>A. Benali</td>
<td>L. Balme</td>
<td>92-95</td>
<td>Electro-optic ATE</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>F. Lemery</td>
<td>M. Marzouki</td>
<td>92-95</td>
<td>Analog and Mixed Macromodeling</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>M. Kodjma</td>
<td>A. Guyot</td>
<td>92-95</td>
<td>Analog Voltage Controlled Oscillators and Phase-Locked Loops</td>
</tr>
<tr>
<td>Hewlett Packard</td>
<td>P. Dulleux-Verguin</td>
<td>B. Courtois</td>
<td>91-94</td>
<td>Failure Analysis of ICs by Liquid Crystals</td>
</tr>
<tr>
<td>IMD</td>
<td>Ch. Vaucher</td>
<td>L. Balme</td>
<td>90-93</td>
<td>PCB Testing</td>
</tr>
</tbody>
</table>
6.2.6 Interactive course

An interactive course has been developed by A. GUYOT. The interactive course explains the design of integrated combinatorial arithmetic operators. It is available on internet: http://tima-cmp.imag.fr/~guyot/Cours/Oparithm/english/Op_Ar2.htm. An user's manual (80 pages) in PDF as well as course slides (only in French) are joined.

Operations like addition, subtraction, multiplication, division, square root extraction, evaluation of logarithm, exponential, sine, cosine, tangent, arc sine, arc cosine, arc tangent are currently present in microprocessors. Although they are sometimes implemented by a mix of software and hardware, the present course focuses only on hardware.

All the operators introduced in the course are combinatorial. In digital circuits operators are often sequential or pipelined. Thanks to the operators' high regularity, it is generally easy to make them sequential by register insertion. This aspect is not addressed in the present course.

The interactive course offers 125 applets windows, most of them generate and simulates arithmetic operators. They are controlled through a "dash board" at the bottom, more or less similar to the one below.

The input and output digits can be set with the mouse, as well as some internal signals. Since this signals are in radix two (but not always bit), an automatic conversion to and from decimal is provided. It is advisable to use a pocket calculator to cross-check the results. After a modification, a decimal window is validated by hitting the "enter" key. Hitting the key twice (in the same window) starts the simulation. The keys "|←" or "→|" moves to the next or previous decimal window.

Arithmetic operators are "telescopic", meaning that it is easy to unfold them to any number of bits. However to keep the figure readable on the screen the number of bits is limited, often to 16 or 32 bits (but less or not limited in the VHDL synthesis). A few operators lacking layout regularity are incompletely displayed, some other does not display all the interconnections.

Many applets generate a VHDL description of the operator. This file may be used for simulation or synthesis on FPGA or ASIC. A superficial knowledge of VHDL is sufficient to read the generated file, for it uses only bits (Std_Logic), bit vectors (Std_Logic_Vector), logic gates "not", "and", "or", "xor", "nand", "nor" and signal connection "<=". Since the operators are combinatorial, there is no register, no clock, no FSM. Signals at the periphery are declared "in" (input) or "out" (output) in the "entity". The VHDL describes as exactly as possible the circuit on display, from left to right and top down.

Three criteria: complexity, delay and activity, ascertain an operator quality. The complexity is the gate number. Delay is the period of time necessary to execute an operation. Delay is measured by the applets in cell's delay (cell's delay model). Finally activity records the number of output changes (internal activity is not recorded). The blue button starts the simulation and stays down as long as the circuit is active (not stabilised).
Arithmetic operators are made of interconnected cells instances. Each operator makes use of a small number of cells models (typically from 1 to 3). A cell encapsulates a handful of logic gates. Each cell has three views: the truth table, the VHDL model and the layout. To click in a cell in a circuit merely displays its name. Clicking in a leaf cell shows its truth table. To hide the name or the table, click outside the cell at the right.

Course content

Each of the course seven chapters starts with a naïve realisation. This is most of the times a transposition from radix ten to radix two of the "paper and pencil" algorithm. Then the algorithm is refined in stages. Most of the times improvement consists in getting rid of carry propagation thanks to the use of redundant notation. Moreover for many operators, a specific notation gives the better performance, eight different notation systems are used through the course. The tables below give a rough idea of the circuits in each chapter.

<table>
<thead>
<tr>
<th>Chapter 1 : addition</th>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carry propagate adder</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Carry look-ahead adder</td>
<td>Brent-Kung, Sklansky, Zimmerman optimization, Kogge-Stone, Ling</td>
<td>yes</td>
</tr>
<tr>
<td>Carry propagation free adder</td>
<td>Carry-save &quot;CS&quot;, Borrow-save &quot;BS&quot;, Hybrid conversion</td>
<td>yes, no</td>
</tr>
</tbody>
</table>

special purpose adders (compound adders) all based on Sklansky’s adder.

| Adder/subtractor/comparator (with overflow detection) |
| Maximum, minimum (no difference computation) |
| Carry late adder (carry increment) |
| Two-output adder : A + A, A + B + 1 |
| Three-output adder : A + B, A + B + 1, A + B + 2 |
| Framing adder: A + B – 1, A + B + 1 |
| Distance (absolute value of A – B) |
| Addition in sign/magnitude representation |
| Adder modulo $2^n – 1$ (Mersenne numbers) |
| Adder modulo $2^n + 1$ (Fermat numbers) |

<table>
<thead>
<tr>
<th>Chapter 2 : multiplication</th>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carry propagate multiplier</td>
<td>Unsigned, Signed</td>
<td>yes</td>
</tr>
<tr>
<td>Partial products generation</td>
<td>Unsigned, Signed (Pezaris), Baugh-Wooley, Modified Booth, Canonical Booth</td>
<td>yes</td>
</tr>
<tr>
<td>Partial product reduction</td>
<td>Late (Dadda), Early (Wallace), Hybrid with &quot;4:2 counter&quot;</td>
<td>yes</td>
</tr>
<tr>
<td>Partial product reduction</td>
<td>TDM (Oklobdzija)</td>
<td>yes</td>
</tr>
<tr>
<td>Final adder with uneven arrival times</td>
<td>(Zimmermann)</td>
<td>yes</td>
</tr>
<tr>
<td>Carry-save multiplier (inputs and output in &quot;CS&quot;)</td>
<td>Late (Dadda), Early (Wallace)</td>
<td>yes</td>
</tr>
<tr>
<td>Multiplication by many constants (factorization)</td>
<td></td>
<td>yes</td>
</tr>
</tbody>
</table>
### Chapter 3: division

<table>
<thead>
<tr>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carry propagate divider</td>
<td></td>
</tr>
<tr>
<td>Restoring (unsigned)</td>
<td>yes</td>
</tr>
<tr>
<td>Non-restoring (signed)</td>
<td></td>
</tr>
<tr>
<td>Carry-free radix 2 divider</td>
<td></td>
</tr>
<tr>
<td>SRT (Hamacher)</td>
<td>yes</td>
</tr>
<tr>
<td>Range reduction (Tung)</td>
<td></td>
</tr>
<tr>
<td>On-the-fly quotient conversion</td>
<td></td>
</tr>
<tr>
<td>Brent-Kung</td>
<td>yes</td>
</tr>
<tr>
<td>Synthesis of redundant division</td>
<td></td>
</tr>
<tr>
<td>(any reasonable radix)</td>
<td>no</td>
</tr>
</tbody>
</table>

### Chapter 4: square root extraction

<table>
<thead>
<tr>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carry propagate square root extraction</td>
<td>yes</td>
</tr>
<tr>
<td>Restoring</td>
<td></td>
</tr>
<tr>
<td>Non-restoring</td>
<td></td>
</tr>
<tr>
<td>Carry-free square root extraction</td>
<td></td>
</tr>
<tr>
<td>(includes on-the-fly conversion)</td>
<td>yes</td>
</tr>
<tr>
<td>SRT</td>
<td></td>
</tr>
<tr>
<td>Fused SRT division and root extraction (SRT)</td>
<td>not yet</td>
</tr>
</tbody>
</table>

### Chapter 5: floating-point addition

<table>
<thead>
<tr>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shifter (with guard, round and sticky)</td>
<td>yes</td>
</tr>
<tr>
<td>Zero leading counter</td>
<td>yes</td>
</tr>
<tr>
<td>Zero leading prediction</td>
<td>yes</td>
</tr>
<tr>
<td>Correction of the zero leading prediction</td>
<td>no</td>
</tr>
<tr>
<td>Significand sorting (smaller, larger)</td>
<td>yes</td>
</tr>
<tr>
<td>Distance (exponents difference)</td>
<td>yes</td>
</tr>
<tr>
<td>Compound adder (speculative rounding )</td>
<td>yes</td>
</tr>
<tr>
<td>Full 32-bits floating point adder normalized and denormalized (IEEE compliant)</td>
<td>yes</td>
</tr>
</tbody>
</table>

On this figure the rounding mechanism is not shown
### Chapter 6 : elementary functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exponential (CORDIC)</td>
<td>Carry free (BS)</td>
<td>yes</td>
</tr>
<tr>
<td>Logarithm (CORDIC)</td>
<td></td>
<td>no</td>
</tr>
<tr>
<td>Sine and cosine (CORDIC)</td>
<td>Non restoring</td>
<td>yes</td>
</tr>
<tr>
<td></td>
<td>Carry free (SRT)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Range reduction</td>
<td></td>
</tr>
<tr>
<td>Arctangent (CORDIC)</td>
<td></td>
<td>no</td>
</tr>
<tr>
<td>Arcsine and arccosine (Muller)</td>
<td></td>
<td>no</td>
</tr>
</tbody>
</table>

### Chapter 6 : RNS operations

<table>
<thead>
<tr>
<th>Operation</th>
<th>Variants</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modular addition (RNS)</td>
<td></td>
<td>no</td>
</tr>
<tr>
<td>Modular multiplication (RNS)</td>
<td></td>
<td>no</td>
</tr>
<tr>
<td>Residue (remainder)</td>
<td>Wallace tree</td>
<td>yes</td>
</tr>
<tr>
<td>Adder modulo $2^n - 1$</td>
<td>Kogge-Stone</td>
<td>yes</td>
</tr>
<tr>
<td>Adder modulo $2^n - 1$</td>
<td>Kogge-Stone</td>
<td>yes</td>
</tr>
<tr>
<td>Multiplier modulo $2^n + 1$</td>
<td>Wallace tree</td>
<td>yes</td>
</tr>
<tr>
<td></td>
<td>Use 4:2 counter</td>
<td></td>
</tr>
<tr>
<td>Adder modulo $2^n + 1$ (Hiasat)</td>
<td>Kogge-Stone</td>
<td>yes</td>
</tr>
<tr>
<td>Multiplier modulo $2^n - 1$</td>
<td>Wallace tree</td>
<td>yes</td>
</tr>
<tr>
<td></td>
<td>Use 4:2 counter</td>
<td></td>
</tr>
<tr>
<td>Multiplier modulo $2^n$</td>
<td>Wallace tree</td>
<td>yes</td>
</tr>
<tr>
<td></td>
<td>Use 4:2 counter</td>
<td></td>
</tr>
<tr>
<td>Conversion from RNS to mixed-radix</td>
<td></td>
<td>no</td>
</tr>
</tbody>
</table>
7 - Publishing

7-1 Electronic Publishing: http://tima.imag.fr

During the past year, TIMA Laboratory has promoted and developed a searchable Web site that provides reliable research-based information related to the Laboratory’s activities:

- Regarding scientific publishing, electronic versions of the TIMA annual report are posted on the web. The “TIMA Laboratory research report collection” and theses elaborated at TIMA Laboratory are also available (too).
- Dynamic interactive database pages publish fresh information relating to TIMA Laboratory publications, educational activities, business activities, joint activities, and participation in the organisation of conferences.
- The EDA Portal Directory can be accessed by the whole Internet community. It offers an Open Database Service, including the Web-based Job Opportunities service and the Web-based Calendar service (conferences, technical meetings, …), a valuable selection of links related to TIMA Laboratory research domains regularly updated, and finally the “Who’s Who” database more than 400 people involved professionally in various specific domains: Asynchronous systems, MEMS/OEMS, SoC and Thermal engineering.
- TIMA Laboratory web server mirrors the DAC conference web site.

In the 2003 new-look TIMA Website - http://tima.imag.fr - we have streamlined the subject headings on the home page and the page sections are now highlighted at the top of each page. We hope that these changes will make the service even more user-friendly.

Web log frequency statistics for January 2004:

- Number of visits: 231 451
- Number of visitors: 114 000
- Number of consulted pages: 1 096 649

With regards to internal communication and facilitating information sharing, the internal resource website gives access to the G@el Library Portal (5200 journals) and to the CNRS BIBLIOSCIENCE Database portal.(aWebSPIRS Connexion).
A considerable number of utilities, administrative tools and links are also available.
7-2 Books and magazines

2003

ALACOQUE L.*, RENAUDIN M., NICOLLE S.*
Irregular sampling and local quantification scheme A-D converter

* Department Electronic, CPE, Villeurbanne, France

ANTONI L., LEVEUGLE R., FEHER B.*
Using Run-Time Reconfiguration for Fault Injection Applications

* Budapest University of Technology and Economics, Hungary

CHO Y.*, LEE G., CHOI K.**, YOO S., ZERGAINOH N.
Scheduling and timing analysis of HW/SW on-chip communication in MP SoC design

* Seoul National University, Seoul, Korea; ** Samsung Electronics, Soowon, Korea

COURTOIS B.
Infrastructures for education and research: from national initiatives to worldwide development
Invited paper at Festkolloquium Zukunftstrendsin der Mikroelektronik Anlass: von 60. Geburtstag
Professor Manfred Glesner, Darmstadt, Germany, August 29, 2003

Design, Test, Integration, and Packaging of MEMS/ MOEMS (DTIP’03), May 5-7, 2003
Mandelieu – La Napoule, France, SPIE Proceedings

* JDS Uniphase/Cronos, USA ; ** Univ. of Freiburg, Germany ; *** MEMSCAP, Grenoble, France ;
**** Columbia Univ., USA ; ***** IZM, Berlin, Germany

COURTOIS B., Guest Editor
Special Issue on DTIP 2002 (The Symposium on Design, Test, Integration of MEMS/MOEMS held in
Cannes, May 6-8, 2002)
Publishers,
Vol.37, No.1, October 2003

COURTOIS B., RENCZ M.*, LASANCE C.**, SZEKELY V.***, Editors
Proceedings of 9th International Workshop on THERmal Investigations of ICs and Systems
(THERMINIC’03), Aix-en-Provence, France, 24-26 September 2003

* MicRed Microelectronics Res & Dev Ltd., Hungary; ** Philips, The Netherlands; *** Budapest University
of Technology and Economics, Hungary

FAURE F., VELAZCO R., VIOLANTE M.*, REBAUDENGO M.*, SONZA REORDA M.*
Impact of data cache memory on the single event upset-induced error rate of microprocessors
IEEE Transactions on Nuclear Science, Vol.50, No.6, December 2003

* Politecnico di Torino, Italy

JERRAYA A.A., YOO S., VERKEST D., WEHN N. (Eds.)
Embedded Software for SoC

LEVEUGLE R., CHAPMAN G.*, Guest Editors
Special Issue on International Symposium on Defect and Fault Tolerance in VLSI
Systems (DFT’01), Microelectronic Journal, Vol. 34, No. 1, January 2003

* Simon Fraser University, Burnaby, Canada
LEVEUGLE R., HADJIAT K.
Multi-level fault injections in VHDL descriptions: alternative approaches and experiments
Special Issue on the Eighth IEEE International On-Line Testing Workshop (IOLTW’02), Journal of
Electronic Testing, Vol. 19, No. 5, 559-575, October 2003

MIR S., CHARLOT B.
From Microelectronics to integrated microsystems testing
Chapter in Microsystems Technology – Fabrication, test and reliability, J. Boussey (Ed.), Hermes Penton
Science, 2003

PAVIOT Y.
Application du flot de ciblage logiciel
Chapter in "Conception des logiciels embarqués pour les systèmes monopuces", traité EGEM
Electronique - Génie Electrique - Microsystèmes, Série : Electronique et Micro-électronique, Hermes

RENAUDIN M., FRAGOSO J.
Asynchronous Circuits Design: An Architectural Approach
Chapter in "V Escola de Microeletrônica da SBC-Sul", Edited by José Guntzel & Ricardo Reis, Rio
Grande, Brazil, Sept. 17-20, 2003

ROMAN C., MIR S., CHARLOT. B.
Building an analogue fault simulation tool and its application to MEMS

SASONGKO A., BAGHDADI A., ROUSSEAU F., JERRAYA A.A.
Towards SoC validation through prototyping: a systematic approach based on reconfigurable platform

SASONGKO A., BAGHDADI A., ROUSSEAU F., JERRAYA A.A.
SoC validation through prototyping on ARM integrator platform

VELAZCO R., REZGUI S.*, ZIADE H.*
Assessing the soft error rate of digital architectures devoted to operate in radiation environment: a
case studied
No.1, 83-90, February 2003

*Lebanese University, Faculty of Engineering I, Tripoli, Lebanon

VOROS N.S.*, SANCHEZ L.*, ALONSO A.*, BIRBAS A.N.***, BIRBAS M.***, JERRAYA A.A.
Hardware/software co-design of complex embedded systems - An approach using efficient process
models, multiple formalism specication and validation via co-simulation
No.1, March 2003

*INTRACOM S.A., Greece ; **Universidad Carlos III de Madrid, Spain ; ***Dept. of Electrical
Engineering,University of Patras, Greece

YOO S., JERRAYA A.A.
Introduction to Hardware Abstraction Layers for SoC
Chapter in "Embedded Software for SoC", Ed. by A.A. JERRAYA, S. YOO, D. VERKEST, N. WEHN,

YOO S., NICOLESCU G., BACIVAROV I., YOUSSEF W., BOUCHHIMA A., JERRAYA A.A.
Multi-Level Software Validation for NoC
Chapter in "Networks on Chip", Axel Jantsch & Hannu Tenhunen (Eds), Kluwer Academic Publishers,
2003
ALEXANDRESCU D.*, ANGHEL L., NICOLAIDIS M.*
Simulating single event transients in VDSM ICs for ground level radiation
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* iRoC Technologies, Grenoble, France

ALLIER E., SICARD G., FESQUET L., RENAUDIN M.
A New Type of Asynchronous Analog to Digital Interface

BASROUR S.
Dépôts en phase liquide : application aux microtechniques
Chapter in « Techniques de fabrication des microsystèmes », Volume 1, Traité EGEM Hermès Editeur, ISBN 2-7462-0817-2, pp 91 – 120, Mai 2004

BOUBEKEUR M., BORRIONE D., MOUNIER L., SIRIANNI A., RENAUDIN M.
Modeling CHP descriptions in labeled transitions systems for an efficient formal validation of asynchronous circuit specification

BOUESSE F., RENAUDIN M., GERMAIN F.*
Asynchronous AES Crypto-Processor Including Secured and Optimized Blocks
---------
*SGDN/DCISS, 51 bd. De la Tour Maubourg, 75700 Paris, France

CESARIO W., WAGNER F., JERRAYA A.A
Hardware/Software Interfaces Design for SoC

CESARIO W., PAVIOT Y., GAUTHIER L., LYONNARD D., NICOLESCU G., YOO S., JERRAYA A.A.
Object-based hardware/software component interconnection model for interface design in system-on-a-chip circuits

CHARLOT B., PARRAIN F., GALY N., BASROUR S., COURTOIS B.
A sweeping mode integrated fingerprint sensor with 256 tactile microbeams

COURTOIS B., RENCY M.*, LASANCE C.**, SZEKELY V.***, Editors
Proceedings of 10thInternational Workshop on THERmal Investigations of ICs and Systems (THERMINIC’04), Sophia Antipolis, Côte d’Azur, France, 29 September - 1 October 2004
---------
* MicRed Microelectronics Res & Dev Ltd., Hungary; ** Philips, The Netherlands; *** Budapest University of Technology and Economics, Hungary


COURTOIS B., KORVINK J.G.*, Guest Editors
Special Issue on The Symposium on Design, Test, Integration of MEMS/MOEMS (DTIP 2003)
---------
* Albert Ludwig University in Freiburg, Germany
COURTOIS B., MICHEL B.*, Editors
Foreword to Special Issue on The Symposium on Design, Test, Integration of MEMS/MOEMS (DTIP 2003)
---------
* IZM, Berlin, Germany

FESQUET L., ES SALHIENE M., RENAUDIN M.
Asynchronous technology for energy reduction in embedded systems
Annals of telecommunications, Systems-on-chip for telecommunications, Vol. 59 n°7-8, July-August 2004

JERRAYA A.A., NICOLESCU G.
La spécification et la validation des systèmes monopuces

JERRAYA A. A., WOLF W.*, Ed.
Multiprocessor Systems-on-Chips
Morgan Kaufmann Publishers, September 2004
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* Princeton University, USA

MAJIAUSKAS G. *, LYONNARD D., CESARIO W., PAVIOT Y., GAUTHIER L. **, JERRAYA A.A., STUIKYS V.*
Communication Co-Processor Design by Composition of Parameterized Cells
Chapter in "Information Technology and Control", 2004 m. Nr. 1(30), ISSN 1392-124X, 2004
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* Kaunas University of Technology, Kaunas, Lithuania; ** Kyushu, Japan

NICOLESCU B.*, SAVARIA B.Y.*, VELAZCO R.
Software detection mechanisms providing full coverage against single bit-flip faults
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* Ecole Polytechnique de Montreal, Canada

PANYASAK D., SICARD G., RENAUDIN M.
A Current Shaping Methodology for Lowering EM Disturbances in Asynchronous Circuits

SCHMALTZ J., BORRIONE B.
A Functional Approach to the Formal Specification of Networks on Chip

SLIMANI K., FRAGOSO J., FESQUET L., RENAUDIN M.
Low Power Asynchronous Processors
Chapter 22 in "Low-Power Electronics Design" written by Christian Piguet", Published by CRC Press, ISBN 0849319412, July 2004

TOMA D., BORRIONE B., AL SAMMANE G.
Combining several paradigms for circuit validation and verification

VELAZCO R., FAURE F.
Single event effects characterization of complex digital circuits: test methodology and tools
WAGNER F.R.*, CESARIO W.O., CARRO L.*, JERRAYA A.A.

* UFRGS, Porto Alegro, Brazil

YOO S., BOUCHHIMA A., CESARIO W., JERRAYA A.A., GAUTHIER L.
Low-power SoC with power-aware operating systems generation
Chapter in “Low-Power Electronics Design”, CRC Press, n°1941, August 2004

ZERGAINOH N.-E., BAGHDADI A., JERRAYA A.A.
A generic architecture platform based-methodology for an efficient design of Hardware/Software application-specific multiprocessor System-On-Chip
Annals of telecommunications, Systems-on-chip for telecommunications, Vol. 59 n°7-8, July-August 2004

ZERGAINOH N.-E., BAGHDADI A., JERRAYA A.A.
Hardware/Software Codesign of On-chip communication architecture for application-specific multiprocessor System-On-Chip

ZIADE H.*, AYOUBI R.**, VELAZCO R.
A survey on fault injection techniques
International Arab Journal of Information Technology (IAJIT), Vol. 1, No. 2, pp.171-186, July 2004

7-3 Conferences and Workshops

2003

Radiation test methodology for SRAM-based FPGAs by using THESIC+

* Istituto di Astrofisica Spaziale e Fisica Cosmica, CNR, Milano, Italy; ** Sanitas EG S.R.L., Milano, Italy

Proposal for a radiation test of virtex-based ALUs
Radiation and Effects on Components and Systems Workshop (RADECS’03), Noordwijk, The Netherlands, 15-19 September 2003

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* iMediasoft Group, Grenoble, France and Politechnica University of Bucharest, Romania

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*LPMO, FEMTO-ST Institut, Besançon, France

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* School of EECE, Univ. of Newcastle upon Tyne, NE1 7RU, UK

RENCZ M.*, POPPE A.*, COLLARD E.**, RESS S.**, SZEKELY V.**, COURTOIS B.
A procedure to correct the error in the structure function based thermal measuring methods
20th Semiconductor Thermal Measurement and Management Symposium (SEMITHERM’04), San Jose,
California, USA, March 7-11, 2004
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* MicRed Microelectronics Res & Dev Ltd., Hungary; ** Budapest University of Technology and
Economics, Hungary

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* MicRed Microelectronics Res & Dev Ltd., Hungary; ** Budapest University of Technology and
Economics, Hungary

RENCZ M.*, SZEKELY V.**, POPPE A.*, COURTOIS B., ZHANG L.***
Testing the die attach quality of 3D Stacked dies
International Mechanical Engineering Congress and Exposition (IMECE’04), Anaheim, California, USA,
November 13-19, 2004
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* MicRed Microelectronics Res & Dev Ltd., Hungary; ** Budapest University of Technology and
Economics, Hungary; *** National Semiconductor Corporation, Santa Clara, CA, USA

RENCZ M.*, FARKAS G.*, SZEKELY V.**, POPPE A.**, COURTOIS B.
Thermal qualification of 3D stacked die packages
6th Electronics Packaging and Technology Conference (EPTC’04), Singapore, December 8-10, 2004
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* MicRed Microelectronics Res & Dev Ltd., Hungary; ** Budapest University of Technology and
Economics, Hungary

SANCHEZ E.*, SONZA REORDA M.*, SQUILLERO G.*, VELAZCO R.
Automatic verification of RT-Level microprocessor cores using behavioral specifications: a case study
XIX Conference on Design of Circuits and Integrated Systems (DCIS’04), Bordeaux, France,
November 24-26, 2004
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* Politecnico di Torino, Italy

SARMENTO A., CESARIO W., JERRAYA A.A.
Automatic building of executable models from abstract SoC architectures
15th IEEE International Workshop on Rapid System Prototyping (RSP’04), Geneva, Switzerland, June
28-30, 2004
SCHMALTZ J., BORRIONE B.
A Functional Specification and Validation Model for Networks on Chip in the ACL2 Logic
Proceedings of the 5th International Workshop on the ACL2 Theorem Prover and its Applications
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SCHMALTZ J., BORRIONE B.
A functional approach to the formal specification of networks on chip
in Proc. of Formal Methods in Computer-Aided Design (FMCAD'04), Austin, Texas, USA, November 14-

SLIMANI K., REMOND Y., SICARD G., RENAUDIN M.
TAST profiler and low energy asynchronous design methodology
14th International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS'04),
Isle of Santorini, Greece, September 15-17, 2004

SLIMANI K., SICARD G., RENAUDIN M.
A Methodology for Estimating Energy Consumption of QDI Asynchronous Circuits
14th International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS'04),
Isle of Santorini, Greece, September 15-17, 2004

SZEKELY V.*, BOGNAR G.*, RENCZ M.**, CIONTU F., CHARLOT B., COURTOIS B.
Design and verification of an electrostatic MEMS simulator
Nanotechnology Conference and TradeShow (NanoTech'04), Boston, Massachusetts, U.S.A.,
March 7-11, 2004

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* Budapest University of Technology and Economics, Hungary; ** MicRed Microelectronics Res & Dev
Ltd., Hungary

TOMA D., BORRIONE D., AL SAMMANE G.
Combining several paradigms for circuit validation and verification
CASSIS'04, Marseille, France, March 10-13 2004

TOMA D., PEREZ A.*, BORRIONE D., BERGERET E.*
Design of a proven correct SHA circuit
International Conference on Electrical, Electronic and Computer Engineering (ICEEC-04), Cairo, Egypt,
September 5-7, 2004

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* L2MP, IMT - Technopôle de Château Gombert, 13451 Marseille Cedex 20, France

TOMA D., BORRIONE D.
Verification of a cryptographic circuit: SHA-1 using ACL2
5th International Workshop on the ACL2 Theorem Prover and its Applications (ACL2'04)
Austin, Texas, USA, September 18-19, 2004

YOUSSEF W., YOO S., SASONGKO A., PAVIOT Y., JERRAYA A.A.
Debugging HW/SW interface for MPSoC: video encoder system design case study
Design Automation Conference (DAC'04), San Diego, USA, June 7-11, 2004

ZERGAINOH N., POPOVICI K., JERRAYA A.A., URARD P.∗
Matlab based environment for designing DSP systems using IP blocks
The 12th Workshop on Synthesis and System Integration of Mixed Information technologies (SASIMI'04),
Kanazawa, Japan, October 18-19, 2004

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* STMicroelectronics, Crolles, France

7-4 Theses

2003

Anh Vu DINH-DUC
Automatic synthesis of QDI asynchronous circuits
Thèse de Doctorat INPG – 14 March 2003
Damien LYONNARD  
An approach for the systematic gathering of interface items toward the generation of multiprocessor architectures  
Thèse de Doctorat INPG – 30 April 2003

Zein JUNEIDI  
CAD tools for MEMS  
Thèse de Doctorat INPG – 26 May 2003

Ferid GHARSALLI  
Hardware-software interface design for global memory intégration in system on chip  
Thèse de Doctorat INPG – 1 July 2003

Lorinc ANTONI  
Fault injection using run-time reconfiguration of FPGAs  
Thèse de Doctorat INPG – 19 September 2003

Emil DUMITRESCU  
Construction de modèles réduits et vérification symbolique de circuits industriels décrits au niveau RTL  
Thèse de Doctorat INPG – 7 October 2003

Emmanuel ALLIER  
Asynchronous analog to digital interface: a new class of converters based on time quantization  
Thèse de Doctorat INPG – 27 November 2003

Ludovic TAMBOUR  
A methodology and semi-automated flow for design and validation of digital signal processing ASIC macro-cells  
Thèse de Doctorat INPG – 3 December 2003

2004

Nadir ACHOURI  
Memory Built-In Self-Repair techniques for high defect densities  
Thèse de Doctorat INPG – 1 April 2004

Mohamed-Anouar DZIRI  
Design tools and hardware/software components integration models for heterogeneous embedded systems design  
Thèse de Doctorat INPG – 26 May 2004

Dhanista PANYASAK  
Electromagnetic emission reductin in integrated circuits : the asynchronous alternative  
Thèse de Doctorat INPG – 14 June 2004

Antoine SIRIANNI  
Modeling, simulating and verifying asynchronous digital circuits in SystemC v2.0.1 standard  
Thèse de Doctorat INPG – 18 June 2004

Yanick PAVIOT  
Communication services partitioning for automatic generation of hardware software interfaces  
Thèse de Doctorat INPG – 1 July 2004

Arif SASONGKO  
Prototyping based on reconfigurable plateforme for verification of system on chip  
Thèse de Doctorat UJF – 15 October 2004

Menouer BOUBEKEUR  
Validation of Asynchronous Circuits Specifications: Methods and Tools  
Thèse de Doctorat UJF – 22 October 2004

Amine REZZAG  
Logical synthesis of micropipeline asynchronous circuits  
Thèse de Doctorat INPG – 13 December 2004
Kamel SLIMANI  
Low power asynchronous microprocessors  
Thèse de Doctorat INPG – 16 December 2004

Jerome QUARTANA  
Design of Asynchronous Network on Chip: application to GALS systems  
Thèse de Doctorat INPG – 20 December 2004

7-5 Patents

2003

ALLIER E., FESQUET L., RENAUDIN M., SICARD P.  
Procédé et dispositif de conversion analogique-numérique  
publ. date 01/08/03; FR2835365
8 - Miscellaneous

8-1 What did they do after graduating from the Laboratory (1984-2004) ?

Below is the list of researchers which graduated from TIMA Laboratory, from 1984.

The first affiliation corresponds to their affiliation right after the thesis. Eventually, successive affiliations are provided.

From 1984 to 2004, 160 theses have been defended.

It might be noticed that (apart from foreign students who returned in their country) several members of the group have been or are working abroad.

NICOLAIDIS Michael
Conception de circuits intégrés ou testables pour des hypothèses de pannes analytiques.
Thèse de Docteur-Ingénieur, 6 January 1984
CNRS - TIMA Laboratory - Grenoble – France
Next : iROC Technologies – Grenoble – France

DERANTONIAN Henri
Génération automatique de parties contrôles de microprocesseurs sous forme de PLA spécialisés.
Thèse de Docteur-Ingénieur, 1er July 1984
BULL – Grenoble - France

CHUQUILLANQUI Samuel
Une nouvelle approche pour l'optimisation topologique et l'automatisation du dessin des masques de PLA complexes.
Thèse de Docteur-Ingénieur – 15 Octobre1984
BULL Systèmes - Les Clayes Sous Bois - France
Next : THOMSON THOM'6 - Paris - France
Next : GEC ALSTHOM - Paris la Défense - France
Next : GEC ALSTHOM Transport - Saint-Ouen - France

LAURENT Jacques
Projet ACIME : Analyse des Circuits Intégrés par Microscopie Electronique.
Thèse de Doctorat, 22 Octobre 1984
CNRS - TIMA Laboratory - Grenoble - France
Next : CNRS - IMAG - Grenoble - France

BOURCIER Emile
Conception et réalisation du simulateur de langage de description de circuits intégrés IRENE C.
Thèse Ingénieur CNAM - Octobre 1984
STMicroelectronics - Grenoble - France

HMIMID Mohamed
Assemblage et génération automatique des dispositifs périphériques de PLA complexes.
Thèse Docteur de 3ème cycle – 12 November 1984
SIEMENS - Munich - Germany

SAHBATOU Mohamed Djameeddine
Une méthode de conception de microprocesseurs CMOS : application au 8048 (INTEL)
Thèse de Docteur-Ingénieur – 12 November 1984

JANSCH Ingrid
Conception de contrôleurs autotestables pour des hypothèses de pannes analytiques.
Thèse d'Etat – 14 January 1985
Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil

SCHOELLKOPF Jean-Pierre
SILICIEL : Contributions à l'architecture des circuits intégrés et à la compilation du silicium.
Thèse d'Etat – 1er April 1985
BULL Systèmes - Les Clayes Sous Bois - France
Next : STMicroelectronics – Crolles - France
IANESELLI Jean-Christophe  
Un opérateur d'unification pour une machine base de connaissance PROLOG.  
Thèse de 3ème cycle - 3 June 1985  
MERLIN GERIN - Meylan - France  

SUWARDI Iping Supriana  
Mécanismes prédictifs d'évaluation des caractéristiques géométriques des circuits VLSI.  
Thèse de Docteur-Ingénieur - 3 June 1985  

BERGER Laurent  
Analyse de défaillances de circuits VLSI par microscopie électronique à balayage.  
Thèse de Docteur-Ingénieur – 7 June 1985  
STMicroelectronics - Grenoble - France  
Next : BULL Systèmes - Les Clayes Sous Bois - France  
Next : STMicroelectronics - Grenoble - France  
Next : Thomson TCEC - Grenoble - France  

BERTRAND François  
Conception descendante appliquée aux microprocesseurs VLSI  
Thèse de 3ème cycle - September 1985  
BULL Systèmes - Les Clayes Sous Bois - France  
Next : LETI - Grenoble - France  

PEREZ SEGOVIA Thomas  
PAOLA : un système d'optimisation topologique de PLA.  
Thèse de 3ème Cycle – 25 Octobre 1985  
CNET - Meylan - France  

GUIGUET Isabelle  
Liaison d'un microscope électronique à balayage aux outils CAO de description des circuits intégrés.  
Thèse Ingénieur CNAM – 28 November 1985  
APYSIS - Meylan - France  

MARTINEZ François  
CIRENE : Compilateur du langage IRENE  
Thèse Ingénieur CNAM – November 1985  

MARINE Souheil  
Un langage pour la description, simulation et synthèse automatique du matériel VLSI  
Thèse de Docteur Ingénieur – 3 February 1986  
STMicroelectronics - Grenoble - France  
Next : ALCATEL-Alsthom - Marcoussis - France  

BASCHIERA Daniel  
Modélisation de pannes et méthodes de test de circuits intégrés CMOS  
Thèse de Doctorat – 6 March 1986  
TRT - Paris - France  
Next : NORSKDATA - Norway  
Next : EPFL - Lausanne - Switzerland  
Next : HMT - Brügg b/Biel - Switzerland  
Next : id3 Semiconductors - Fontanil Cornillon – France  
Next : STMicroelectronics - France  

ALIOUAT Mahklouf  
Reprise de processus dans un environnement distribué après pannes matérielles transitoires ou permanentes  
Thèse de Docteur Ingénieur – 1er April 1986  
University of Constantine - Algeria  

OSSEIRAN Adam  
Définition, étude et conception d'un microprocesseur autotestable spécifique : COBRA  
Thèse de Doctorat – 12 May 1986  
EPFL - Lausanne - Switzerland  
Next: University of Geneva, Switzerland
JAMIER Robert  
Génération automatique de parties opératives de circuits VLSI de type microprocesseur  
Thèse de Docteur Ingénieur – 1er December 1986  
STMicroelectronics - Grenoble - France

HOCHET Bertrand  
Conception de VLSI : Applications au calcul numérique  
Thèse de Doctorat – 12 January 1987  
EPFL - Lausanne - Switzerland  
Next : University of Adelaide - Australia  
Next : University of Yverdon, Switzerland

ROUGEAUX François-René  
Outils de CAO et conception structurée de systèmes intégrés sur silicium  
Thèse de Doctorat – 2 February 1987  
University of Laval - Canada  
Next : IBM - Montpellier - France

VARINOT Patrice  
Compilation de silicium : application à la compilation de parties contrôles  
Thèse de Doctorat – 2 February 1987  
Professor at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil  
Next : MATRA - Paris - France

DANG Weidong  
Parallélisme dans une machine base de connaissances PROLOG  
Thèse de Doctorat – 3 July 1987  
CRIL - Colombes - France

BEKKARA Noureddine  
Optimisation et compromis surface-vitesse dans le compilateur de silicium SYCO  
Thèse de Docteur Ingénieur – 19 Octobre 1987  
STMicroelectronics - Grenoble - France

SOUAI Mohamed  
Etude d’un moniteur d’un système fonctionnellement réparti.  
Thèse de Docteur Ingénieur – 1er November 1987

CAISSO Jean-Paul  
Contribution à la vérification des circuits intégrés dans un environnement multivalué.  
Thèse de Doctorat – 16 November 1987  
Mc GILL University - Montreal - Canada  
Next : MATRA-MHS – Nantes - France  
Next : STMicroelectronics– Rousset – France

BERGER-SABBATEL Gilles  
Machines spécialisées et programmation en logique  
Thèse d’Etat – 1er June 1988  
CNRS - TIMA Laboratory - Grenoble - France  
Next : CNRS - LGI Laboratory - Grenoble - France

MHAYA Noureddine  
Compilateur de parties contrôle de microprocesseurs  
Thèse de Doctorat INPG – 24 June 1988  
IFATEC - Versailles - France  
Next: IFATEC - Montigny-Le-Bretonneux - France

DUPRAT Jean  
LAIOS : un réseau multiprocesseur orienté intelligence artificielle  
Thèse de Doctorat INPG – 22 July 1988  
E.N.S.L. - Lyon – France
FERNANDES Antonio Otavio
Test des PLAs optimisés topologiquement
Thèse de Doctorat INPG – 9 September 1988
University of Belo Horizonte - Brazil

MOISAN Frédéric
Optimisation du contraste image en microscopie optique (application à l’inspection microélectronique)
Thèse de Doctorat UJF – 28 September 1988
Direction des Constructions et des Armes Navales (DCAN) - Brest - France

MICOLLET Dominique
Etude de la contrôlabilité de circuits intégrés par faisceaux d’électrons
Thèse de Doctorat INPG – 29 September 1988
University of Dijon – France

ZYSMAN Eytan
Conception de parties contrôles de circuits VLSI - Application au coprocesseur arithmétique
FELIN
Thèse de Doctorat INPG – 27 October 1988
EPFL - Lausanne - Switzerland

HORNIK Armand
Contribution à la définition et à la mise en oeuvre de NAUTILE
Thèse de Doctorat INPG – 6 June 1989
APSIS - Meylan - France
Next : BULL - Echirolles - France

DARLAY Françoise
Contribution au test des circuits intégrés CMOS : étude du test des pannes stuck-on et stuck-open
Thèse de Doctorat INPG - 20 November 1989
EPFL - Lausanne - Switzerland
Next : Ecole Polytechnique de Montréal - Canada
Next : STMicroelectronics - Grenoble - France
Died in plane crash in July 1996

BONDONO Philippe
Contribution à NAUTILE : un environnement pour la compilation de silicium
Thèse de Doctorat INPG - 8 December 1989
IBM - Corbeil - France

JERRAYA Ahmed Amine
Participation à la compilation de silicium et au compilateur SYCO
Thèse d’Etat - 19 December 1989
CNRS - TIMA Laboratory - Grenoble - France

NORAZ Serge
Application des circuits intégrés autotestables à la sûreté de fonctionnement des systèmes
Thèse de Doctorat INPG - 20 December 1989
MERLIN GERIN - Meylan - France

PIRSON Alain
Conception et simulation d’architectures parallèles et distribuées pour le traitement d’images
Thèse de Doctorat INPG - 4 May 1990
CENG Division LETI – Grenoble - France
Next : STMicroelectronics/TCEC – Meylan – France
Next : SYNOPSYS – Mountain View – California - USA
Next : C-Cube Microsystems - Milpitas - California - USA

SAVART Denis
Analyse de défaillance de circuits intégrés VLSI par testeur à faisceau d’électrons
Thèse de Doctorat INPG - 27 June 1990
IMAGERIE INFORMATIQUE - Grenoble – France
Société Savart et Michel – Meylan – France
TORKI Kholdoun
L’autotest intégré dans un compilateur de silicium
Thèse de Doctorat INPG - 12 July 1990
CMP - Grenoble - France

BALME Louis
Habilitation à diriger des recherches. 21 May 1990
On secondment to SGS, Geneva, from 1.1.1991
Next : TIMA Laboratory

CHAUMONTET Gilles
Etude de faisabilité d'un micro-contrôleur de très haute sécurité
Thèse de Doctorat INPG - 26 Octobre 1990
Centre de Compétence en Conception de Circuits Intégrés (C4I), Archamps - France

MARZOUKI Meryem
Approches à base de connaissances pour le test de circuits VLSI : application à la validation de prototypes dans le cas d'un test sans contact
Thèse de Doctorat INPG - 6 February 1991
CNRS - TIMA Laboratory – Grenoble - France
Next: CNRS - LIP6 Laboratory - Paris - France

CONARD Didier
Traitement d'images en analyse de défaillances de circuits intégrés par faisceau d'électrons
Thèse de Doctorat INPG - 11 February 1991
INFI Company (ARM Group) - Paris, France
Next: OCE Graphics – Créteil - France

COURT Thierry
Conception d'une famille de coprocesseurs parallèles intégrés pour le traitement d'images
Thèse de Doctorat INPG - 9 December 1991
I2S - Bordeaux - France

JEMAI Abderrazak
A study of a RISC processor for a parallel symbolic system
Thèse de Doctorat INPG - 22 June 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble - France
Next : ENSI – Tunis - Tunisia

PARK Inhag
AMICAL: an assistant for the architectural synthesis and exploration of control circuits
Thèse de Doctorat INPG - 3 July 1992
DAS/ETRI - Daejon, Research Laboratory in Korea

COLLETTE Thierry
Architecture and VHDL behavioural validation of a parallel process or dedicated to computer vision
Thèse de Doctorat INPG - 14 September 1992
CEA/LETI/DEIN - Gif sur Yvette - France

CASTRO ALVES Vladimir
Fault modelling and test algorithms for multi-port RAMs
Thèse de Doctorat INPG - 10 October 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble - France
Next: Lecturer at Aveiro University - Portugal
Next: Professor at UFRJ - Rio de Janeiro - Brazil

BOURAOUI Rachid
Computation with large numbers and vlsi: application to PGCD, extended PGCD and Euclidean distance
Thèse de Doctorat INPG - 15 January 1993
Bell Northern Research (BNR) – Ottawa - Canada
Next: Plaintree Systems Inc. – Stittsville – Ontario - Canada
O’BRIEN Kevin
Silicon computation : from circuit to system
Thèse de Doctorat INPG - 31 March 1993
LEDA S.A. – Meylan - France

KUSUMAPUTRI-HORDNIK Yustina
On-line standard arithmetic operators for large precisions
Thèse de Doctorat INPG - 11 May 1993

BEN OTHMAN Mohamed Tahar
Evaluation of a memory hierarchy for a symbolic machine
Thèse de Doctorat INPG - 8 September 1993
Dean of the Faculty of Science & Engineering, Univ. of Science & Technology - Sana’a - Yemen Republic

VAUCHER Christophe
The test of high resolution bare printed circuit boards
Thèse de Doctorat INPG - 25 November 1993
IMD, Grenoble, and TIMA Laboratory - France
Next: IMD Bandol, France
Next: Consultant Engineer, True Test Techniques & Training (T4) – Bandol, France

HAMDI Belgacem
CAD tools for automatic generation of self-checking data paths
Thèse de Doctorat INPG - 18 April 1994

AICHOUCHI Mohamed
Linking architectural synthesis with register transfer level synthesis
Thèse de Doctorat INPG - 20 June 1994
Post-doctoral position at Ecole Polytechnique de Montréal - Canada
CADABRA – Ottawa - Canada
Newbridge Networks Corporation – Kanata – Ottawa - Canada

LUBASZEWSKI Marcelo
Advanced methods for the test of analogue and mixed-signal circuits
Thèse de Doctorat INPG - 20 June 1994
Professor at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil

KEBICHI Omar
Techniques and CAD tools for automatic generation of BIST and DFT for RAMS
Thèse de Doctorat INPG - 15 July 1994
Engineer/researcher at TIMA Laboratory - Grenoble - France
Next: Mentor Graphics – Portland - USA

KOLARIK Vladimir
Advanced methods for the test of analogue and mixed-signal circuits
Thèse de Doctorat INPG - 31 October 1994
University of Brno - Czech Republic

BEDERR Hakim
Contribution to the design for testability of iterative arithmetic and logic operators
Thèse de Doctorat INPG - 23 November 1994
Post-Doctoral position at AT&T Bell Laboratories – Princeton - USA
Next: Texas Instruments – Villeneuve Loubet - France

VERGUIN Pascale
Industrialization of a fault method on integrated circuits using liquid crystals
Thèse de Doctorat INPG - 20 December 1994
Primary school teacher - France

MONTALVO Luis
Number systems for high performance divider
Thèse de Doctorat INPG, 13 March 1995
University of Minnesota – Minneapolis – USA
Next: Post-doctoral position at CNET – Meylan - France
VARGAS Fabian Luis
  Improving electronics reliability for space systems based on current monitoring
  Thèse de Doctorat INPG, 5 May 1995
  Associated Researcher at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil
  Next: Prof. at Pontificia Universidade Catolica do Rio Grande do Sul - Porto Alegre - Brazil

BOUDJIT Mokhtar
  Algorithmes de testabilité basés sur la description à deux-niveaux "Groupe-E-Concurrente" des fonctions logiques
  Thèse de Doctorat INPG, 19 May 1995

SKAF Ali
  Design of redundant and on-line arithmetic processors: algorithms, architecture types and VLSI implementations
  Thèse de Doctorat INPG, 11 September 1995
  Lecturer at Aveiro University, Portugal
  Next: HIAST Institute - Damascus University - Syria

LEMERY François
  Behavioural modelling of analog and mixed circuits
  Thèse de Doctorat INPG, 20 December 1995
  STMicroelectronics - Crolles - France

BEN ISMAYL Tarek
  System-level synthesis and hardware/software codesign
  Thèse de Doctorat INPG, 9 January 1996
  Hewlett Packard - Bristol, UK
  AREXSYS - Meylan, France

STEFANI Robert
  Application of the ISO 9000 standard to service entreprises which are highly dependent on their information system
  Thèse Professionnelle INPG, Mastère Qualité des Syst. Intégrés complexes, 10 January 1996
  AFAQ Auditor, Bagneux (Paris), France

TOUATI Mohamed Hédi
  Test et diagnostic de cartes et de MCMs partiellement boundary scan
  Thèse de Doctorat INPG - 24 January 1996
  Northern Telecom – Ottawa - Canada

KISSION Polen
  High level synthesis involving hierarchy and the re-use of existing blocks
  Thèse de Doctorat INPG - 25 January 1996
  Researcher at TIMA Laboratory - Grenoble
  Next: ANACAD – Meylan - France

DING Hong
  Synthèse architecturale interactive et flexible
  Thèse de Doctorat INPG - 2 April 1996
  Post-Doctoral position at "Ecole Polytechnique de Montréal" - Canada
  Next: Nortel Semiconductors – Ottawa - Canada

KARAM Jean-Michel
  Méthodes et outils pour la conception et la fabrication des microsystèmes
  Thèse de Doctorat INPG - 20 May 1996
  Researcher at TIMA Laboratory - Grenoble - France
  Next: MEMSCAP - St Ismier (Grenoble) - France
MOUSSA Imed  
Application of GaAs integrated circuits for high speed communication systems and high performance computing  
Thèse de Doctorat INPG - 10 June 1996  
Engineer at TIMA Laboratory - Grenoble - France  
Next: AREXSYS - Meylan – France  
Next: Verisity Design - Grenoble - France

CHANGUEL Adel  
Prototypage rapide d'architectures mixtes logiciels/matériels à partir de modèles mixtes C-VHDL  
Thèse de Doctorat INPG - 22 October 1996  
Associate Professor at ENIM – Monastir - Tunisia

BENALI Aadil  
Contribution to quality assurance in bare printed wiring board testing: treatment of CAD information, using image processing techniques, for electrical test data generation  
Thèse de Doctorat INPG - 3 December 1996  
IMD Marcoussis - France

DEHARBE David  
Temporal logic model checking: study and application to VHDL  
Thèse de Doctorat UJF - 15 November 1996  
Carnegie Mellon University – Pittsburgh - USA

VIJAYARAGHAVAN Vijay  
Exploration of links between the High Level Synthesis (HLS) and the Register Transfer Level (RTL) synthesis  
Thèse de Doctorat INPG - 29 November 1996  
SYNOPSYS – Mountain View - USA

ROMDHANI Mohamed  
Embedded systems engineering using a hardware/software co-design methodology. Application on avionics  
Thèse de Doctorat INPG - 9 December 1996  
Post Doctoral Position at TIMA - Grenoble - France  
Next : Associate Professor at INSAT – Tunis - Tunisia

VACHER André  
Hard-wired computation of a Fourier transform with a large number of samples, possibly multi-dimensional  
Thèse de Doctorat INPG - 8 January 1997  
Teacher at Lycée de Meylan - France

PARET Jean-Marc  
A study and implementation of silicon microsystems design methodology and collective fabrication  
Thèse de Doctorat INPG - 13 January 1997  
ALPLOG – Grenoble - France

RAHMOUNI Maher  
Scheduling and optimizations for high-level synthesis of control designs  
Thèse de Doctorat INPG - 21 February 1997  
Hewlett Packard – Bristol - UK

WAHBA Ayman  
Design error diagnosis in digital circuits: the case of simple errors  
Thèse de Doctorat UJF - 7 May 1997  
Associate Professor at Ain Shams University – Cairo - Egypt

OLIVEIRA DUARTE Ricardo  
Techniques and CAD tools for automatic generation of BIST and DFT for RAMs  
Thèse de Doctorat INPG – 30 June 1997  
Post-doctoral position at University of Belo Horizonte - Brazil ("Univ. Federale de Minas Gerais")
MOHAMED Firas
A fuzzy logic-based approach for the test and the diagnosis of analog circuits
Thèse de Doctorat INPG – 3 July 1997
ANACAD – Meylan – France
Next: MEMSCAP – Meylan - France

Liem Clifford Benjamin
Retargetable compilers and tools for embedded processors in industrial applications
Thèse de Doctorat INPG – 18 July 1997
Improv Systems Inc. - Santa Clara – California - USA

BERREBI Elisabeth
Methodology for the industrial application of architectural synthesis
Thèse de Doctorat INPG – 11 December 1997
STMicroelectronics – Crolles - France

KODRNJA Marc
Voltage controlled oscillator study for intermediate frequency oscillator noise analysis and simulation
Thèse de Doctorat INPG – 12 December 1997
STMicroelectronics – Grenoble - France

DAVEAU Jean-Marc
System level specification and communication synthesis for hardware/software co-design
Thèse de Doctorat INPG – 19 December 1997
Post-doctoral position at IBM New York - USA

NOGUET Dominique
Parallel architectures for image processing
Thèse de Doctorat INPG – 26 January 1998
LETI - Grenoble - France

NAÇABAL François
Tools for exploration of embedded programmable architectures in industrial applications
Thèse de Doctorat INPG – 27 February 1998
STMicroelectronics – Crolles - France

COISSARD Vincent
Processor core for exact arithmetic
Thèse de Doctorat INPG – 2 September 1998
ALPLOG/ATMEL-ES2 - Le Rousset (Aix-en-Provence) - France
Next: ALPLOG/STMicroelectronics - Crolles - France

VINCI DOS SANTOS Filipe
Design techniques for radiation-hardening of ICs
MEMSCAP - St Ismier (Grenoble) - France
Next: CERN - Geneva - Switzerland

VALDERRAMA Carlos Alberto
Virtual prototyping for the generation of mixed hardware/software architecture
Universidade Federal do Rio Grande do Norte (UFRN) - Brazil

NEGOI Andy Catalin
Virtual device and its simulation processors
Philips Semiconductors AG, Zurich, Switzerland

PEREZ-RIBAS Renato
Maskless front-side bulk micromachining compatible with standard GaAs IC technology
Professor-Researcher at the Computering Institute of Pontificia Universidade Catolica (PUCCamp) - Campinas – Brazil
Next: Professor at Universidade do Rio Grande do Sul (UFRGS) – Porto Alegre - Brazil
MARCHIORO Gilberto Fernandes
Transformational partitioning for the co-design of mixed hardware/software systems
Thèse de Doctorat INPG – 26 November 1998
Professor at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil

TCHOUMATCHENKO Vassiliy
Modeling, architecture and tools for fast adders synthesis
Thèse de Doctorat INPG – 17 December 1998
Sofia University - Bulgaria

ABOU-SAMRA Sélim Joseph
Low energy integrated circuit design in 2D and 3D SOI technologies : applied to arithmetics
Thèse de Doctorat INPG – 18 December 1998
AREXSYS - Meylan – France
Next: iROC Technologies – Grenoble – France
Next : SOISIC, Grenoble – France

CHEYNET Philippe
Study of the robustness of the intelligent control facing with radiation induced faults
Thèse de Doctorat INPG – 5 May 1999
Next: Contractual Researcher at TIMA
Next : VERIMAG – Grenoble - France

GUILLAUME Philippe
Contribution to the back-end of system on a chip synthesis
Thèse de Doctorat INPG – 11 June 1999
STMicroelectronics - Crolles - France

LAURENT Bernard
Design of reuse blocks - reflections on methodology
Thèse de Doctorat INPG – 18 June 1999
AREXSYS - Meylan - France

VELASCO-MEDINA Jaime
Bist techniques for analog and mixed-signal circuits
Thèse de Doctorat INPG – 1er July 1999
Prof. at Universidad del Valle - Cali - Colombia

CHAAHOUB Faouzi
Study of design methods and CAD tools for analog integrated circuits
Thèse de Doctorat INPG – 29 September 1999
Rockwell Semiconductor Systems - Newport Beach - USA

CESARIO Wander
Flexible architectural synthesis
Thèse de Doctorat INPG – 14 Octobre 1999
Post-doctoral position at TIMA Laboratory - Grenoble - France

BIANCHI Raul Andrés
Analog integrated circuits design techniques for high temperature applications in standard silicon technologies
Thèse de Doctorat INPG – 21 Octobre 1999
STMicroelectronics - Crolles - France

BERNAL NOREÑA Alvaro
Design of a high speed digital architecture for computing the modular exponentiation
Thèse de Doctorat INPG – 22 Octobre 1999
Prof. at Universidad del Valle - Cali - Colombia

DUSINA Julia
Formal verification of high level synthesis results
Thèse de Doctorat UJF – 27 Octobre 1999
STMicroelectronics - Bristol - UK
CALIN Teodor
CMOS system design and test for reliability and fault tolerance
Thèse de Doctorat INPG – 8 November 1999
STMicroelectronics - Grenoble - France

VEYCHARD Damien
Electro-thermal converter with long time constant in microsystem technology for thermal breaker
Thèse de Doctorat INPG – 3 December 1999
STMicroelectronics - Grenoble - France

CLERMIDY Fabien
Reliability improvement of SIMD parallel computers by test and structural fault-tolerance
Thèse de Doctorat INPG – 8 December 1999
CEA - Saclay – France

SUGAR Zoltan
Behaviorial synthesis based on scheduling
AREXSYS - Meylan - France

HESSEL Fabiano
Multilanguage codesign of heterogeneous systems
Thèse de Doctorat INPG – 16 June 2000
Pontifical Catholic Univ. of Rio Grande do Sul (PUCRS) – Porto Alegre – Brazil

LE MARREC Philippe
Multilevel co-simulation in a multilanguage design flow
Thèse de Doctorat INPG – 28 June 2000
AREXSYS - Meylan – France

MORAWIEC Adam Jan
Improvement of simulation performance of models described in hardware description languages
Thèse de Doctorat UJF – 26 Octobre 2000
ESCI – Grenoble - France

ANELLI Giovanni
Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technologies for the LHC experiments
Thèse de Doctorat INPG – 11 December 2000
CERN – Geneva - Switzerland

ANGHEL Lorena
Fault tolerance versus technological limitations of silicon
Thèse de Doctorat INPG – 15 December 2000
Researcher Position at TIMA Laboratory – Grenoble – France
Next : Associate Professor at ENSERG– Grenoble – France

COSTE Pascal
Heterogeneous system design
Thèse de Doctorat UJF – 12 January 2001
BOURGET S.A. – Roussillon (Vienne) – France

REZGUI Sana
Error rate prediction for digital architectures: A method and experimental results
Thèse de Doctorat INPG – 8 March 2001
Researcher Position at TIMA Laboratory – Grenoble – France
Staff Product Applications Engineer (Radiation Effects) at Xilinx – San Jose, CA - USA

CHARLOT Benoît
Fault modeling and design-for-test of MEMS
Thèse de Doctorat INPG – 12 March 2001
Researcher Position at TIMA Laboratory – Grenoble – France
Next : Chargé de Recherches, CNRS – Grenoble – France
RITTER Gerd
Formal sequential equivalence checking of digital systems by symbolic simulation
Thèse de Doctorat UJF – 20 April 2001
Research Ingineer Position at Infineon – Allemagne
Next : SAP Labs France S.A. – Paris – France

ABDELHAY Ahmad
On-line testing of linear digital systems
Thèse de Doctorat INPG – 12 March 2001
Faculté de génie électrique et électronique, Université d’Alepp – Alepp – Syrie

ALZAHER-NOUFAL Imed
CAD tools for the generation of self-checking arithmetic operators
Thèse de Doctorat INPG – 23 May 2001
iROC Technologies – Grenoble - France

VIVET Pascal
A quasi-delay insensitive integrated circuit design methodology : application to the study and design
of a 16-bit asynchronous RISC microprocessor
Thèse de Doctorat INPG – 21 June 2001
STMicroelectronics – Grenoble – France

GEORGELIN Philippe
Formal verification of synchronous digital designs, based on symbolic simulation
Thèse de Doctorat INPG – 18 Octobre 2001
Post-doctoral position at TIMA in cooperation with STMicroelectronics – Grenoble – France
Next : Consultant Secteur Privé

GAUTHIER Lovic
Operating system generation for multitask software targeting on heterogeneous multiprocessor
architecture for embedded systems
Thèse de Doctorat INPG – 5 December 2001
ISIT (Institute of Sytems & Information Technologies) - Fukuoka – Japan

ROUX Sébastien
Algorithm and architecture for embedded multimedia system
Thèse de Doctorat INPG – 22 January 2002
FranceTélécom R&D - Meylan – France

PALAN Bohuslav
Design of low noise pH-ISFET microsensors and integrated suspended inductors with increased
quality factor Q
Thèse de Doctorat INPG – 1er March 2002
ESAT K. Stransky - Pelhrimov – Czech Republic

BAGHDADI Amer
Exploration and systematic design of application-specific heterogeneous multiprocessor SoC
Thèse de Doctorat INPG – 14 May 2002
ATER at ENSERG – Grenoble – France
Professor at ENST – Bretagne - France

MARTINEZ Sergio
Design of silicon micromachined cross-connects for all-optical networks
Thèse de Doctorat INPG – 21 May 2002
Professor ITESM – Mexico

ZAIDAN Nidal
Conception of a secure interface
Thèse de Doctorat INPG – 27 May 2002
Professor ITESM - Mexico
GOY Jérome
Study, conception and fabrication of an APS image sensor in standard CMOS technology for low light level applications such as star trackers
Thèse de Doctorat INPG – 4 June 2002
MEMSCAP - St Ismier (Grenoble) - France

MEFTALI Sami
Architectures exploration and memory allocation/assignment in multiprocessor SoC
Thèse de Doctorat INPG – 6 September 2002
LIFL – UST - Lille - France

NAAL Mouhamad Ayman
High-level synthesis for test, built-in self test
Thèse de Doctorat INPG – 24 September 2002
Post-Doctoral position at TIMA Laboratory – Grenoble – France
Next : Professor at University of Aleppo, Syria

NICOLESCU Bogdan
A software approach for the detection of transient errors occurring in processor-based digital architectures: principles and experimental results
Thèse de Doctorat INPG – 24 September 2002
University of Montreal – Quebec - Canada

GALILEE Bruno
Algorithm-architecture study for multimedia handset: image segmentation thanks to an asynchronous processors array
Thèse de Doctorat INPG – 8 October 2002
France Telecom R&D – Meylan - France

NICOLESCU Gabriela
Specification and validation for heterogeneous embedded systems
Thèse de Doctorat INPG – 27 November 2002
University of Montreal – Quebec - Canada

PARRAIN Fabien
Tactile fingerprint sensor using piezoresistive microstructures
Thèse de Doctorat INPG – 2 December 2002
ATER IEF – Orsay
Next : Maître de Conf. at IUT Cachan, France

BOUTOBZA Slimane
Tools for Memory BIST/BISR generation
Thèse de Doctorat INPG – 20 December 2002
iROC Technologies – Grenoble - France

RIGAUD Jean-Baptiste
Libraries specification for the synthesis of asynchronous circuits
Thèse de Doctorat INPG – 23 December 2002
ATER at ENSERG – Grenoble – France
Next : EMSE – CMP Georges Charpack – Gardanne - France

DINH-DUC Anh Vu
Automatic synthesis of QDI asynchronous circuits
Thèse de Doctorat INPG – 14 March 2003
Teacher/Researcher – Hô Chi Minh University - Vietnam

LYONNARD Damien
An approach for the systematic gathering of interface items toward the generation of multiprocessor Architectures
Thèse de Doctorat INPG – 30 April 2003
STMicroelectronics – Ottawa – Canada
JUNEIDI Zein
CAD tools for MEMS
Thèse de Doctorat INPG – 26 May 2003
Consulting Bureau of Marketing – Damas - Syria

GHARSALLI Ferid
Hardware-software interface design for global memory intégration in system on chip
Thèse de Doctorat INPG – 1 July 2003
ATER at ENSIMAG – Grenoble - France

ANTONI Lorinc
Fault injection using run-time reconfiguration of FPGAs
Thèse de Doctorat INPG – 19 September 2003
Budapest University of Technology and Economics – Hungary
Next : Enginieur at Duolog Technologies, Hungary

DUMITRESCU Emil
Construction de modèles réduits et vérification symbolique de circuits industriels décrits au niveau RTL
Thèse de Doctorat INPG – 7 October 2003
INRIA Rhône-Alpes – Grenoble – France

ALLIER Emmanuel
Asynchronous analog to digital interface: a new class of converters based on time quantization
Thèse de Doctorat INPG – 27 November 2003
ATER at ENSERG – Grenoble – France

TAMBOUR Ludovic
A methodology and semi-automated flow for design and validation of digital signal processing ASIC macro-cells
Thèse de Doctorat INPG – 3 December 2003

ACHOURI Nadir
Memory Built-In Self-Repair techniques for high defect densities
Thèse de Doctorat INPG – 1 April 2004
Synopsis Inc. – Montbonnot – France

DZIRI Mohamed-Anouar
Design tools and hardware/software components integration models for heterogeneous embedded systems design
Thèse de Doctorat INPG – 26 May 2004
CERIM, University of Lilles – France

PANYASAK Dhanista
Electromagnetic emission reductin in integrated circuits : the asynchronous alternative
Thèse de Doctorat INPG – 14 June 2004
Philips Semiconductors – Grenoble – France

SIRIANNI Antoine
Modeling, simulating and verifying asynchronous digital circuits in SystemC v2.0.1 standard
Thèse de Doctorat INPG – 18 June 2004

PAVIOT Yanick
Communication services partitioning for automatic generation of hardware software interfaces
Thèse de Doctorat INPG – 1 July 2004
FleXody SaS – Grenoble – France

SASONGKO Arif
Prototyping based on reconfigurable plateforme for verification of system on chip
Thèse de Doctorat UJF – 15 October 2004
Post Doctoral Position at TIMA – Grenoble – France

BOUBEKEUR Menouer
Validation of asynchronous circuits specifications: methods and tools
Thèse de Doctorat UJF – 22 October 2004
Post Doc researcher, CEOL Research Center – University College Cork – Ireland
8-1.1 Best INPG Thesis Awards

Every year, INPG awards a series of Best INPG Thesis Awards. Recently several TIMA Doctoral candidates have been awarded in Microelectronics and Computer Science specialities.

Specification and validation for heterogeneous embedded systems
Doctoral Candidate: NICOLESCU Gabriela
Advisor: JERRAYA A.A.
Type: Thèse de Doctorat INPG, Spécialité Microélectronique
Awards: Microelectronics Best INPG Dissertation Prize

A quasi-delay insensitive integrated circuit design methodology: application to the study and design of a 16-bit asynchronous RISC microprocessor
Doctoral Candidate: VIVET P.
Advisor: RENAUDIN M.
Defense: 21/06/2001
Type: Thèse de Doctorat INPG, Spécialité Microélectronique
Award: INPG Best Thesis Prize Ceremony

Fault tolerance versus technological limitations of silicon
Doctoral Candidate: ANGHEL L.
Advisor: NICOLAIDIS M.
Defense: 15/12/2000
Type : Thèse de Doctorat INPG, Spécialité Microélectronique
Award : Microelectronics Best INPG Thesis

Analog integrated circuits design techniques for high temperature applications in standard silicon technologies
Doctoral Candidate: BIANCHI R. - A.
Advisor: COURTOIS B.
Defense: 21/10/1999
Type: Thèse de Doctorat INPG, Spécialité Microélectronique
Award: Microelectronics Best INPG Thesis

Study of the robustness of the intelligent control facing with radiation induced faults
Doctoral Candidate: CHEYNET Ph.
Advisor: VELAZCO R.
Defense: 05/05/1999
Type: Thèse de Doctorat INPG, Spécialité Informatique
Award: Computer Sciences Best INPG Thesis
8-2 Press articles in 2004

In the following are collected copies of articles that appeared in Newspapers in 2004.

8-2.1 Summary

► Comment le roi des MEMS a rebondi  
LE NOUVEL OBJECTIF RHONE-ALPES N°13  
February/March 2005

► Formation sur les effets neutroniques les 23 et 24 Mars à Palaiseau  
ELECTRONIQUE INTERNATIONAL HEBDO N°589  
10 February 2005

► TIMA inspire les créateurs d’entreprise de la microélectronique  
LES NOUVELLES DE GRENOBLE  
October 2004

► La technologie CMOS 90 nm disponible pour la fabrication en petites séries  
ELECTRONIQUE INTERNATIONAL HEBDO N°568  
2 September 2004

► Une journée dédiée aux systèmes embarqués le 28 Mai à Grenoble  
ELECTRONIQUE INTERNATIONAL HEBDO N°560  
13 May 2004

► Les spectateurs du Grenier  
LIBERATION, supplément Ville  
24-25 April 2004

► Jean-Michel Karam : Memscap affiche sa réussite  
L’EXPRESS n°2750  
21 March 2004

► iROC cède son activité test intégré de mémoires à SYNOPSYS  
ELECTRONIQUE INTERNATIONAL HEBDO N°552  
18 March 2004

► La french touch s’affirme en CAO électronique  
L’USINE NOUVELLE N°2905  
25 February 2004
A 35 ans, le Grenoblois Jean-Michel Karam vient de racheter Optogone, une entreprise basée à Brest et spécialisée dans les cristaux liquides. Une nouvelle acquisition pour cet immigré libanais qui a fait de Memscap le numéro un mondial des mems. Avec 7,6 millions de chiffre d’affaires et 120 salariés. Pourtant, son entreprise a connu une grave crise il y a quelques années. Mais il a su rebondir. Portrait.

Pour moi dans la vie, il faut être premier ou, au pire, second !”
Jean-Michel Karam peut agacer par son assurance. Grand, regard sombre, costume italien bien coupé, élégant et séducteur, il attire sans complexes sa réussite avec Memscap. Il faut dire qu’après avoir été chercheur, ce Franco-Libanais a réussi à s’imposer dans la “Silicon valley” grenobloise avec une petite start-up qui est devenue leader mondial sur le créneau des mems, des systèmes microélectroniques qu’on utilise dans la mécanique, l’optique… En plus il est sportif, généreux… Alors, enfin un chef d’entreprise parfait?
Si on gratte, on trouve quand même les petits travers d’un vrai patron. D’abord, il ne répond pas aux questions qui le dérangent. Enfin, il est malin, il esquive, avec talent.


Basketteur professionnel
a rebondi

Ce jeune ingénieur fait déjà preuve d'un certain charisme

J'étais très attentif en cours, ce qui me permettait de sortir le soir !” Il mène alors une vraie vie parisiennne : restos, bars, boîtes de nuit… Et ce jeune ingénieur fait déjà preuve d'un certain charisme. Dans son école, il est élu président du club des élèves. Mais il consacre aussi beaucoup de temps à sa passion, le basket. Basket est professionnel au Liban, il devient entraineur d'équipes féminines à Paris. Et puis sa vie va basculer de côté des mers : “Un jour, un prof de l'école m'a proposé d'étudier les mers. À l'époque, personne ne connaissait ces systèmes microélectroniques qui ont la taille d'un grain de sable et qu'on insère dans des éléments mécaniques, électroniques ou optiques… comme les alliages par exemple, ou les pace-makers”.

Le jeune Karam travaille jour et nuit pour boucher son étude qui sera brillante, bien sûr. Tout en découchant, au passage un DEA de micro-informatique, évidemment avec mention. Du coup,

Ses revenus

“Ce n'est jamais été tabou pour moi de parler d'argent” affirme Jean-Michel Karim. Mais quand on lui demande d'évaluer sa fortune, il sourit. Une fortune qui s'est elle au milieu des années 90 à creuser, 13 millions d'euros, puisqu'il détient 27% de Memescap. “Quand en partie de chiffres, ça agace Jean-Michel Karim : “Les journaux feront mieux de faire rêver leurs lecteurs, plutôt que de parler de moi et disent “fortune”.” Et, toujours humble, il ajoute : “Guido Memescap n'allait pas très bien, je n'ai pas gagné un seul salaire dans l'entreprise, le mieux, que j'ai réduit de 60%. Le coup de 1999 qui a gagné en 2000 n'a pas suivi la pente des impôts de 2000.” Impossible de lui faire dévoiler son salaire. En tout cas, il avait à ses besoins Gucci, Prada, Versace ou Mugler. Et sa maison à Grenoble. Mais, la encore, il n'oublie pas de rappeler qu'il est généreux. Il n'a pas hésité à créer une association pour lutter contre les maladies ostéopores. Il aide aussi les jeunes patrons en investissant dans certaines start-up prometteuses aux États-Unis et en France.”

L'entreprise

Memescap
Forme juridique : SA
Création : 1997
Implantation : Bernin (loire)
Activités : production de mers, des systèmes microélectroniques
Capital : 36 400 153 euros
Actionnaires : 12 % Jean-Michel Karim, 10,7 % SIEP Venture, 9,8 % Evergreen partenaires, 5,7 % EIF
Investissement : 1 200 salariés
Chiffre d'affaires 2003 : 7,6 millions d'euros
Résultat net 2003 : NC

Chiffre d'affaires

en millions d'euros

Résultats nets

en millions d'euros

Nombre de salariés

en milliers d'euros
pas de surprise, il est débauché par le Tima, un centre de recherche grenoblois où il est subjugué par le directeur Bernard Courtois. "Un des hommes qui a le plus compté dans ma vie, car il a été le premier à m'avoir fait confiance" affirme-t-il. Courtois lui propose de créer une unité de recherche sur les neurones.

"Je réussis ou je meurs" A 26 ans, il a déjà sous ses ordres une trentaine de collaborateurs. Il apprend à

**Il lève la première année 2 millions d'euros**

faire du reporting, à réaliser un business plan... Et son unité de recherche commence à être reconnue en France, puis aux États-Unis. Son labo décroche même des contrats avec de grandes groupes comme Schlumberger. Karam envisage alors de quitter le Tima : "Les neurones commençaient vraiment à décoller, je me suis dit qu'il était temps de lancer ma boîte... J'ai décidé de démissionner en me disant : où je réussis ou je meurs ! Et pour réussir, j'ai misé sur le travail."

En 1997, il lance Memscap. Il débauche de nombreux ingénieurs de la région en leur proposant d'être actionnaires de l'entreprise. Ça marche ! Avec un investissement personnel de 60 000 euros, Karam réussit à lever la première année presque 2 millions d'euros. Et dès 2000, il franchit la barre des 3 millions d'euros de chiffre d'affaires.

Ses références

J’admire beaucoup Jacques Welch, l’ancien patron de General Electric. Un type exceptionnel, car il a embauché 258 000 personnes et a réussi à rendre milliardaire un nombre incroyable de gens. Mais j’admire aussi Warren Buffett, le deuxième homme le plus riche du monde qui a une carrière exceptionnelle dans la Bourse. J’ai aussi beaucoup de respect pour le parcsour d’Alan Greenspan, le patron de la réserve fédérale américaine. Bref, les patrons qui m’impressionnent sont surtout américains.

Même si je sais qu’il y a certains patrons français très talentueux, comme Thierry Breton, de France Télécom. La politique m’intéresse, mais uniquement comme spectateur. D’ailleurs, je préfère ne pas dire pour qui je vote, car ça pourrait être négatif pour mon activité. Côté sport, ma référence c’est bien sûr Michael Jordan, le meilleur joueur de basket de tous les temps. Il a une détente impressionnante, beaucoup d'adresse et d'énergie et une créativité incroyable sur le terrain."
Son style de management

"Je suis très proche de mes salariés avec qui j’ai des relations très directes. Pour moi, un patron doit être honnête et juste. C’est ce que j’ai appris de mon père. Exemple : je récompense toujours les salariés qui travaillent bien. Et je leur donne des perspectives en leur permettant de prendre des responsabilités. Mais je suis également très honnête avec mes clients. Quand on cherche à rouler ses clients, ça se fait toujours mal."

Ce qui lui permet de levier 11 millions d’euros pour financer son développement. Il faut dire qu’il collectionne déjà les clients prestigieux comme la Nasa, Kodak, Microsoft, Motorola, Samsung... Il peut alors s’introduire en Bourse dès mars 2001.

"Mon meilleur souvenir, c’était vraiment très dur mais on a réussi à réaliser la deuxième plus grosse introduction de toute l’histoire du Nouveau Marché avec une capitalisation de plus de 400 millions d’euros" n’hésite pas à afficher cet éternel premier de la classe un reprenant son petit refrain : "Pour moi dans la vie, il faut être premier ou deuxième. Je ne me lancerai jamais dans un business où je sais que je ne pourrai pas être au minimum le deuxième".

Une cantaine de salariés virens

Avec la Bourse, Memscap se fait un nom. Et on commence à beaucoup de parler de Jean-Michel Karam, qui a bien profité de cette valorisation puisqu’il contrôle 27 % de Memscap. D’ailleurs, de méchantes rumeurs accompagnent cette réussite. A Grenoble, certains le traitent de mégalomane, d’arrogant. Il faut dire que sa collection de voitures ne passe pas inaperçue. Ni la construction de son immense usine à Berain pour 60 millions d’euros.

Des rumeurs qui agacent Jean-Michel Karam. "Je trouve normal de gagner de l’argent car j’ai travaillé comme un fou tout et jour pendant des années pour en arriver là. En plus ma réussite n’a pas empêché d’affronter des terribles épreuves. Exemple, en janvier 2002, quand le marché de la communication optique s’est effondré. En quelques heures, j’ai perdu

"Quand je pense au Liban, je relativise"


Julie Draguier

FORMATION SUR LES EFFETS NEUTRONIQUES LES 23 ET 24 MARS À PALAISEAU

Canal Industrie propose une formation intitulée “Comprendre - Appréhender - Maîtriser les effets neutroniques”, qui se déroulera les 23 et 24 mars à Palaiseau. Cette formation porte sur la conception des équipements électroniques, l’intégration de systèmes, la fiabilité, la sûreté de fonctionnement, etc. Elle se déclinera selon les thèmes suivants : introduction sur les environnements radiatifs ; les effets directement ionisants de dose et de débit de dose, et les effets non directement ionisants de déplacement ; les effets singuliers (ions lourds, protons, neutrons) ; les mécanismes physiques ; la simulation des effets transitoires ; les méthodes expérimentales, les moyens de test et les normes ; les méthodes et outils de prédiction du taux d’erreurs transitoires.

Elle comprendra notamment des interventions de Thales Research & Technology, du CNRS (Tima), du CEA et d’Infoduc. Canal Industrie, une société privée de formation créée il y a une dizaine d’années, vient de s’installer au centre d’innovation technologique de Palaiseau.

E.F.
Renseignements : François Mabillot,
tél. 06 82 12 15 06 ; f.mabillot@canalindustrie.com
TIMA inspire les créateurs d’entreprise de la microélectronique


Bernard Courtois,
directeur du laboratoire Tima
EN BREF

LA TECHNOLOGIE CMOS 90 nm DISPONIBLE POUR LA FABRICATION EN PETITES SÉRIES

Le CMP (Circuits Multi-Projets) de Grenoble étoffe son catalogue de technologies de fabrication en petites séries avec le Cmos 90 nm de STMicroelectronics. Réservée pour l'heure aux laboratoires de recherche, aux universités et aux écoles, cette technologie permet d'intégrer plus de 400 000 portes logiques par mm², supporte les mémoires embarqués Sram, Rom et Dram et peut être employée pour la conception de circuits analogiques et radiofréquences, même si elle reste principalement destinée aux circuits numériques. Le premier lancement en production est prévu avant la fin de l'année, avec un coût de 5 000 euros/mm². 

F.R.
UNE JOURNÉE DÉDIÉE AUX SYSTÈMES EMBARQUÉS LE 28 MAI À GRENOBLE

Avec l'aide de TIMA et de la ville de Grenoble, l'Asprom organise une Journée sur les systèmes embarqués à Grenoble le 28 mai 2004 prochain (juste après le Forum 4i – voir notre numéro du 22 avril dernier). Le programme de cette journée devrait permettre de faire le point sur les tendances et les défis de la conception des systèmes embarqués, sur les besoins de l'industrie dans ce domaine ainsi que sur les start-up françaises spécialisées dans le développement de systèmes sur une puce (SoC). En clôture de la manifestation, une table ronde regroupera des experts en stratégie industrielle, qui discuteront des chances de réussite de la France, dans le domaine de l'électronique embarquée en général et des SoC en particulier.


deux sujets liés au secteur de l'électronique : externalisation et partenariat, le problème posé par les délocalisations pour l'industrie de la sous-traitance ; et le capital humain ou comment attirer les ingénieurs et les chercheurs de haut niveau.
Les spectateurs du Grenier

Au-dessus du café, les Boccard ont aménagé un petit cabaret, le Grenier, très rive gauche, intimiste. Ce soir, un poète dit ses poèmes, accompagné d’un balafon et d’un synthé. Il y a treize spectateurs. Anne et Kader, sur une banquette, écoulent les textes, attentifs, puis traînent après le concert. Ils sont éducateurs. Elle travaille avec des handicapés moteurs, lui avec des SDF. «Cette ville fait plein de choses très fortes dans le secteur social», raconte Anne. Elle vient de Marseille, adore se promener à vélo, mais pose un sacré bémoï à l’image accueillante. «Beaucoup d’étrangers, dit-elle, mais pas beaucoup de mélange. C’est en fait très cloisonné. Les étudiants sont avec les étudiants, les chercheurs avec les chercheurs, etc.» Juchés sur des tabourets, Nathalie et Jean-Michel sifflent une bouteille de vin blanc. Elle travaille pour l’instant en intérim, lui est «régisseur plateau» pour le Cargo, la maison de la Culture. «C’est vrai que, pour celui qui débarque, le contact ne se fait pas comme ça, reconnaît Nathalie. A Grenoble, il faut intégrer un réseau.» Se trouver une tribu. Ils ont grandi ici, fréquentent les bars, les concerts. «Ça fourmille de petits groupes élevés au grain d’ici, raconte Jean-Michel. C’est une ville très multiraciale et cela se ressent dans la musique.» 

Près d’eux, Raul Velazco, le menton en galloche et la bouche gourmande, raconte l’arrivée à Grenoble, en 1976. Il venait d’Uruguay pour achever ses études, faisait la manche dans les cafés. Devenu chercheur au CNRS, spécialiste de microélectronique, il travaille de temps en temps pour la Nasa et joue encore de la guitare, parfois à la Table ronde. Un vrai profil de néo-Grenoblois, écologiste, curieux, concerné par cette cité qu’il s’est appropriée. Il adore «cette ville qui se renouvelle tous les trois ans», au rythme des études ou des contrats de travail. Il aime «les quatre saisons bien marquées», et surtout ces montagnes au bout de chaque rue, qui font que «l’horizon n’existe pas». Il arrivait de la Pampa.
Jean-Michel Karam
Memscap affiche sa réussite

Implantée dans le parc technologique de Fontaine (commune de Bernin), Memscap affiche sa réussite dans une imposante cathédrale de verre, offrant une vue imprenable sur les sommeils enfelées. Après avoir décroché, en 2001, le trophée Fast 50, décerné par le cabinet Deloitte & Touche, de la société qui a réalisé la plus forte croissance de la région Rhône-Alpes et le trophée Stock-IT de la société au plus fort potentiel de croissance, Jean-Michel Karam, son PDG, peut savourer son succès. En sept ans d’existence seulement, Memscap est devenue le leader mondial des microsystèmes électronique et mécanique. Cotée en Bourse depuis mars 2001, Memscap affiche un taux de croissance exceptionnel : une part de la société achetée 1 dollar en 2000 en vaut actuellement 7 000... "Je le dois à mon étoile," répond modestement son fondateur, un jeune homme de 34 ans originaire du Liban. Grand travailleur, Jean-Michel Karam manifeste surtout une extrême rigueur dans son métier. Une qualité acquise à l’université de Beyrouth, où c’est « grande tête » a suivi ses études. Après avoir obtenu un diplôme en génie et un DEA, c’est à Grenoble qu’il soutient une thèse en micro-électronique à l’Institut national polytechnique, qui sera, dit-il, le « tremplin » de sa vie. Il y côtoie les chercheurs du CNRS au laboratoire Tima, où il exerce son premier emploi. Il apprend également à diriger une équipe.

Tombé amoureux de la région et de ses montagnes, l’ingénieur devient entrepreneur profitant des avantages offerts par la « capitale européenne de la micro-électronique » pour y créer sa propre société et y installée, en 1997, le siège de Memscap. Tels une pure, les services particuliers des télécoms et l’absence de structure polluante dans le domaine, garantie par les maitris de Bernin et de Crozat, offrent un bon environnement pour le site de production », souligne-t-il. Fan de l’immigré, Karam n’avait en réalité guère le choix. C’était réussir ou partir. Il aurait été contraint de quitter la France si Memscap n’avait pas été rentable, car il ne disposait que d’une carte de séjour temporaire conditionnée à l’emploi. La chance sourit toujours aux audacieux... Il est vrai aussi que le créneau est porteur et le produit, innovant. Même si les secrets de fabrication sont jalousement gardés par une poignée de chercheurs, les systèmes microélectroniques (Mems) sont en effet partout. Airbags, avions, téléphones portables, capteurs de pression sanguine sont autant d’applications de ces systèmes microcosmiques, capables de capter des variables extérieures ou d’actionner des mécanismes invisibles à l’œil nu. Son succès, Karam le doit également à son sens aigu des affaires et à sa capacité à rassembler rapidement le capital nécessaire. Après avoir obtenu d’investisseurs convaincus pour son projet, 2,2 millions de dollars lors de la première levée de fonds, en 1997, il décroche pas moins de 11 millions de dollars de capital-risque lors d’une deuxième levée de fonds, en 2000, ce qui lui permet d’agrandir sa société. Il quitte alors ses bureaux de Grenoble, devenus trop étroits, pour le site actuel de Bernin. « Le risque pris par les investisseurs nécessite un bon projet », se contente d’expliquer Karam. Mais il fait remarquer aussi un peu plus tard : "On investit dans une équipe beaucoup plus que dans une technologie." Forcé de ses succès, l’homme se tourne de plus en plus vers le domaine des Mems, et se félicite de rassembler à présent "la meilleure équipe de la branche de Memscap".

Enfin, le succès de la récente résidence dans ses choix stratégiques de diversification des produits, afin de fournir une clientèle très hétéroclite, de l’aéronautique au matériel médical, en passant par les télécommunications. Une restructuration de la société, en 2002, a même permis de redéfinir l’activité sur quatre pôles : outre le site de Bernin, trois filiales, en Californie, en Israël et en Norvège, couvrent la demande internationale. Premier producteur de systèmes microélectroniques, Memscap exporte dans le monde entier une large part de ses produits, mais son dirigeant ne souhaite pas créer aujourd’hui de nouvelles filiales à l’étranger, « pour ne pas se disperser ». Le site français, initialement voué à la production, sera à terme entièrement consacré à la recherche et au développement. « Grâce au système d’éducation généraliste, les Français sont très créatifs », affirme Jean-Michel Karam. 

Céline Beaufort
IROC CÈDE SON ACTIVITÉ TEST INTEGRÉ DE MÉMOIRES À SYNOPSYS

Après les fournisseurs de blocs d’IP MoSys et Accelerant Networks (voir notre numéro du 26 février), l’Américain Synopsys, le premier éditeur mondial d’outils de CAO électronique, vient de racheter la division de test intégré (built-in self test) pour les mémoires Sram, Rom et Sram à double port du Français iRoC Technologies pour un montant non dévoilé. Pour l’Américain, l’intégration dans son catalogue de la technologie issue du laboratoire Tima et au cœur du logiciel MBISTeR du Français est une nouvelle étape dans son positionnement sur ce secteur qu’il considère comme l’un des grands domaines d’avenir. Le Français, quant à lui, se recentre sur son activité d’outils et de services pour l’analyse des erreurs logicielles induites par les particules alpha et les neutrons atmosphériques (soft errors) et pour la protection des systèmes sur une puce vis-à-vis de ces sources d’inversions sporadiques de bit.
La French Touch s'affirme en CAO électronique

Une nouvelle vague de start-up françaises est en train de se faire une place dans les logiciels de conception de puces. En dépit de la présence de poids lourds américains installés depuis des années,

Hors de la Silicon Valley, point de salut ? Pour les concepteurs de puces électroniques, la Californie demeure un lieu saint et incontournable en matière de développement de logiciels de conception. Est-ce à dire qu'il ne se passe rien ailleurs ? Ce serait aller trop vite en besogne. Certes, la côte est des États-Unis a vu, il y a quelques années, naître un grand nombre de logiciels de CAO électronique comme Evolve, ProICOS, MentorGraphics et Cadence Design Systems. Mais l'Europe repend du poil de la bête. Ces dernières années, elle a donné naissance à une nouvelle vague de start-up spécialisées dans les logiciels de CAO électronique comme Evolve, ProICOS, MentorGraphics ou TNI-Valence. Le phénomène est important dans l'hexagone, où le marché est demandeur. « Cette année, 4000 à 5000 designs de puces complexes seront mis en chantier dans le monde, écrit Luc Burjaen, le P-DG d'Evolve. Parmi ceux-ci, environ 500 le seront en France. » Le salon Date, qui se tient du 17 au 20 février au Calt de Paris-la-Defense, est la vitrine de ce renouveau.

A quoi tient un tel essor ? Au rôle de plus en plus considérable de la CAO électronique. C'est à partir de ce savoir-faire que naissent les puces qui font tourner les PC, qui contrôlent l'injection des automobiles ou servent à transmettre des communications. Pour concevoir ces puces toujours plus complexes, il est nécessaire de disposer d'outils très performants. Car une puce, avant de se transformer en un bout de silicium, c'est d'abord un logiciel. La manière de concevoir celui-ci doit prendre en compte non seulement les fonctions attendues de la puce mais aussi la manière dont celle-ci sera gravée sur du silicium ainsi que les interactions prévisibles avec son environnement extérieur. Car il n'est pas question qu'une fois mise en boîtier, la puce ne réponde pas au cahier des charges. Il existe un véritable besoin de valider chacune des étapes de la conception. Il n'est plus permis de se tromper, car le coût des systèmes ne fait qu'augmenter avec la diminution de la finesse des traits de gravure en dessous de 90 nanomètres, assure Marcel Sauvioz, le P-DG de ProICOS,

un spécialiste en CAO électronique, créé en 2000.

Dans ce contexte, quel peut être le positionnement des industriels français ? Les techniques évoluant très rapidement, il est utopique d'espérer vendre un outil de conception à tout faire, qui part de projet initial pour aboutir à la puce finale, en passant par l'ensemble des étapes de vérification des fonctionnalités ou de simulation comportementale. Les plus grands s'y sont causé les dents.

Une remise à plat des principes de base de la conception électronique

Résultat, la chaîne de conception est organisée autour d'un logiciel « généraliste », sur lequel viennent se greffer, selon les besoins, des programmes hyperspécialisés, dévoué chacun à un aspect particulier du développement de la puce. Ces niches très pointues sont les cibles privilégiées des jeunes pousses de la CAO.

Mais cela ne s'improvise pas. Tout d'abord il est difficile d'espérer regagner l'assise prise par les acteurs américains. Il a donc fallu trouver d'autres voies. Et, puisque les outils génériques étaient déjà bien malaisés, autant se projeter dans l'avenir et anticiper les besoins futurs des fabricants de puces. Dans cette optique, les acteurs français ont accepté de remettre à plat les
Il garantit la fiabilité du design des puces électroniques

**ERIC SANTÉDÉ**
P-DG d'Emerald Technologies
Crée en 2000, la société est une spin-off de TIMA.

**N**ombre de start-up se sont tout d’abord appuyées sur les développements réalisés à l’intérieur des laboratoires de recherche publics et privés. TIMA-Vallée a élargi le champ d’action grâce aux partenariats renforcés et à la création de presses de recherche. Les laboratoires de TIMA-Vallée se sont dotés de centres de recherche dédiés à la recherche industrielle et à la formation des chercheurs.

**Il propose des "Meccanos" logiciels**

**MARCEL SAUSSAY**
P-DG de Prolog

**Trois questions à...**

**BERNARD COURTOIS**
Directeur de TIMA, unité mixte de recherche du CNRS.

**Situation à Grenoble, TIMA est l’un des plus grands laboratoires publics européens dédiés à la conception logicielle.**

D’où vient cette flambée de start-up françaises ?

"La loi Allégro sur l’innovation a sans doute servi de déclencheur à la création de ces PME. Elle a facilité la participation des personnels d’Etat à la création et au lancement de sociétés, grâce aux possibilités de mise en disponibilité, de détachement."

Quels sont leurs points forts ?

"La conception des puces au niveau du système représente l’atout principal des sociétés françaises de CAO électronique. C’est un domaine où elles ont un savoir-faire reconnu et une position très bonne par rapport aux sociétés américaines, davantage focalisées sur la conception de puces qui..." Et leurs faiblesses ?

"Pour réussir, il faut être basé ailleurs qu’en France. Et une implantation dans la Silicon Valley reste un point de passage obligé, même si cette étape dure très onéreuse. Deux sociétés issues de TIMA, Memscap et Iroc, ont fait cette démarche peu après leur création."
Inoffensives pour les puces traditionnelles, les particules émises provoquent des comportements erratiques des lors que les technologies de gravure des puces deviennent de plus en plus fines. Les « soft errors » et donc la manière de concevoir les puces pour les éviter représentent l'aboutissement d'une technologie à la pointe, que seuls quelques grands laboratoires partagent dans le monde.

Aujourd'hui, le développement d'acteurs français de la CAO électronique a l'heure de plaire aux électroniciens. Ainsi, le premier client d'Vee a été Tous Instruments, puis Canon et Fujitsu ont suivi. L'atout majeur de ces start-up est bien sûr la concentration d'un nombre très important de designs en Europe, dans les télécommunications, la Défense, l'aéronautique ou l'automobile. Des marchés qui sont demandeurs de systèmes complexes, c'est-à-dire qui prennent en compte non seulement les impératifs de la puce elle-même mais également ceux de son environnement proche.

Pour autant, la bataille n'est pas gagnée d'avance. « Pour réussir à pénétrer chez un grand client, il faut être au moins deux fois meilleurs techniquement qu'un grand nom de la CAO », estime un dirigeant de start-up. Il est indispensable d'avoir une visibilité à l'étranger. « Les ingrédients nécessaires au développement sont à la fois quelques grands succès et la capacité de travailler à l'international », juge Marc Frouin de TNI-Valicosys. Sa société a d'ores et déjà suivi le pas en rachetant le fabricant britannique de logiciels de CAO TransEda en octobre. La PME s'est ainsi offerte du même coup une couverture mondiale, avec un pied-à-terre à Los Gatos, en plein cœur de la Silicon Valley. Toujours la « Mecque » ! « Si vous n'avez pas d'implantation là-bas, la visibilité de votre entreprise est très difficile », explique Alain Labat, PDG de Terra Systèmes. Ce Français exilé en sait quelque chose. Il a, lui, préféré fonder sa société de CAO en Californie. O JEAN-PIERRE VERNAY
8-3 Social life and cultural life

8-3.1 Social life

Recently, the Laboratory had the pleasure to congratulate some of its members for marriage and births.

Have got married:

Sebastien FILLION 17 April 2004
Laurent FESQUET 23 March 2002
Salvador MIR 5 October 2002
Sonia UBAGO (JACQUET) 8 June 2002
Gilles SIGARD 26 May 2001
Sami MEFTALI 23 December 2000
Zein JUNEIDI 9 November 2000
Vijay VIJAYARAGHAVAN 7 July 2000
Sergio MARTINEZ 7 July 2000
Regis LEVEUGLE 6 May 2000

The following will be descendants of Laboratory's members:

Matteo SICARD 17 May 2005
Guilhem MIR 04 October 2004
Iris et Clara FESQUET 21 July 2004
Judith CHARLOT 13 March 2003
Mehdi TORKI 10 February 2003
Noemie MIR 12 January 2003
Abdoullah NAAL 17 December 2002
Hussein JUNEIDI 06 December 2002
Juliana VELAZCO 12 August 2002
Thibault SICARD 19 January 2002
Anh Thu DINH-DUC 11 January 2002
Nawar ALZAHER-NOUFAL 3 December 2001
Jeanne CHAUMONTET 28 September 2001
Djoser SIMEU 23 July 2001
Cecilia MEFTALI 22 June 2001
Garance CHARLOT 18 June 2001
David RUFER 11 February 2001
Maria-Laura MORAWIEC 19 November 2000
Amine-Mohamed TORKI 6 October 2000
Fioranne MARTINEZ 6 October 2000
Benjamin EYRAUD 4 October 2000

8-3.2 Social events and exceptional social events

TIMA was organising a football tournament between teams of research (Pictures 8-3.1 to 8-3.4).

TIMA and CMP were exhibiting at DATE 2002 (Pictures 8-3.6).

TIMA at JNRDM in Toulouse on May 2003 and May 2004 (Pictures 8-3.7 and 8-3.8).

QLF Group is pictured at the Lawrence Berkeley's Laboratories (Picture 8-3.9).

8-3.3 Cultural life

Besides fundamental research activities, TIMA Laboratory aims to encourage creativity in individual faculty members and to promote cultural activities such as temporary exhibitions of paintings, sculptures, and photographs.

In 1999, two artistically talented researchers were given the opportunity to exhibit their works:
In May 1999, Charles PAYAN, research scientist at CNRS, exhibited his collection of stereograms, some especially created for TIMA and its scientific collaborators. His minimal representations - shapes and volumes - explored perceptions of space (Picture 8-3 10).

In November 1999, Raoul VELAZCO, Director of the QLF group at TIMA, exhibited a series of paintings inspired by famous works of French painting schools of the last century as well as original creations (Picture 8-3 11).

In January 2001, Philippe JORRAND presented 48 recent paintings and drawings. Philippe JORRAND is a former CNRS research director whose career has included industrial as well as academic experience, both in France and in the US. He founded and was director for more than 15 years of an important computer science laboratory dedicated to artificial intelligence and discrete mathematics. He is now a member of the Leibniz Laboratory in Grenoble where he heads a new research group in quantum computation and quantum information, a promising long-term research topic at the cross roads of quantum physics and theoretical computer science. He was elected chairman of the Information and Communication Science and Technology board of the CNRS in Paris. He has always considered drawing and painting as a natural complement to scientific research, - another dimension for creativity. The themes which attract him are mainly inspired by nature. His trees, his female nudes and faces are always part of an on-going dialogue with life, while, at the same time maintaining a distance from reality: sometimes this distance is no more than a demure side-step, with transposed shapes and shifted hues, sometimes the fracture is more brutal with crude colours and distorted lines. His paintings and drawings show a preference for “one way, irrevocable techniques”, watercolour, ink, charcoal, there is no looking over the shoulder, once on the paper, no line, no colour may be erased or hidden. It is there for ever, the signifier of decisive commitment (Picture 8-3 12).

The April 2002 exhibition brought together the work of a talented researcher and two amateur sculptors related to TIMA members: Claire Di CRESCENZO, exhibited more than 50 recent photographs that magically transform utilitarian objects into whimsical works of beauty. Rejana WAGNER (the wife of Flavio WAGNER, Professor of the Instituto de Informática of the Universidade Federal do Rio Grande do Sul, who worked in 2002 at TIMA as a visiting professor) exhibited a series of sensual sculptures, abstract, delicate, bronze and clay nudes, while Bertrand CHARLOT, Benoît CHARLOT’s brother, presented two stylized figurative wood sculptures (Pictures 8-3 13).

In May 2003, a series of travel drawings by Professor Daniel DEROO (INPG), depicting the beauty of Chinese landscapes were exhibited (Pictures 8-3 14). By the same opportunity, the retirement of C. LE FAOU of the VDS group has been celebrated (Picture 8-3 15).

In January 2004, Nicole JOYE, an English teacher at IUT1 of University Joseph Fourier, exhibited some acrylics paintings on canvas (painted between the years 1999 and 2002). The work is expressive abstract and relies on the tension between composition and color. The scales can be intimate (40X40 cm) or more exaggerated (192X192 cm). Each painting is its own subject matter and tries to investigate the infinite variation of the fundamental elements of painting (Picture 8-3 16).
Picture 8-3 1:
TIMA football team (that beat CSI 5-0 June 1992)

Pictures 8-3 2:
Football tournament organized in 2000: The MCS and SLS team

Picture 8-3 3:
TIMA football team 2001
Pictures 8-3 4:
TIMA football team 2004

Pictures 8-3 5:
Annual Party 2001
Pictures 8-3 6:
DATE 2002: TIMA and CMP are exhibiting
Picture 8-3 7:
JNRDM, Toulouse, 14-16 May 2003

Picture 8-3 8:
JNRDM, Marseille, 4-6 May 2004

Picture 8-3 9:
Groupe QLF for experiments of radiation ground testing performed at the Lawrence Berkeley cyclotron – 2003
Picture 8-3 10:
Charles PAYAN exhibition

Picture 8-3 11:
Raoul VELAZCO exhibition

Picture 8-3 12:
Varnishing of the exhibition of Philippe JORRAND (right) paintings, with Yves BRUNET (middle), Chairman of INPG and Bernard COURTOIS (left), Director of TIMA

Pictures 8-3 13:
Bertrand CHARLOT, Réjane WAGNER & Claire Di CRESCENZO exhibition
Pictures 8-3 14:
Daniel DEROO exhibition

Picture 8-3 15:
Retirement of C. LE FAOU
Pictures 8-3 16:
Nicole JOYE exhibition