TIMA Laboratory
ANNUAL REPORT 2001
B. COURTOIS - May 2002

Techniques de l'Informatique et de la Microélectronique pour l'Architecture d'ordinateurs
Techniques of Informatics and Microelectronics for computer Architecture
ABSTRACT

The Laboratory has a long experience on hardware design (computer architecture, microprocessor-based architectures, VLSI) and on CAD software (multi-level and mixed-mode simulation, physical design, architectural synthesis). Today, the Laboratory is focusing on various aspects of the design, CAD and test of circuits and systems. The Laboratory is approximately 120 people large. It is organized in research groups: MiCroSystems (MCS), Reliable Integrated Systems (RIS), System Level Synthesis (SLS), Verification and modeling of Digital Systems (VDS), QuaLiFication of circuits (QLF), Concurrent Integrated Systems (CIS). The Laboratory is very international; many staff members enjoy 2 countries of citizenship, and there are many foreign researchers and visitors (usually more than 20 countries of citizenship). The Laboratory is also hosting the CMP Service, serving for chips and microsystems fabrication, down to .12μ.

Key issues in 2001 have been that the QLF group under the leadership of Raoul VELAZCO secured an important contract from the Jet Propulsion Laboratory for the procurement of hardware and software tools for testing ICs in radiative environments, the development of TAST, the TIMA Asynchronous Synthesis Tools by the CIS group under the leadership of Marc RENAUDIN, and the consolidation of the generation of the hardware and software communication architecture for multiprocessor SoCs by the SLS group under the leadership of Ahmed JERRAYA.

Three multidisciplinary projects have been developed. One is concerned with the global simulation paradigm of SoCs including MEMS and MOEMS where the co-simulation of hardware-software-mechanics-optics is necessary. The second one is concerned with the development of the WUCS, Wireless Universal Control System and the most recent one is dealing with Quantum Architectures, in cooperation with LEIBNIZ, a theoretical Grenoble-based Lab for Quantum Computing and with Physics and Chemistry Labs working on the implementation of quantum dots.

The three companies issued so far from the Laboratory are doing well. MEMSCAP has been introduced to the Euronext stock exchange, AREXSYS has merged with TNI-Valyosis, and iRoC Technologies has raised $5M venture capital.

In 2001, the Laboratory chaired or co-chaired IOLT in Taormina, THERMINIC in Paris, DTIP in Cannes, DATE in Munich, RADEC in Grenoble, MTDT in San Jose and DFT in San Francisco. In 2002, besides IOLT in Isle of Bendor, THERMINIC in Madrid, DTIP in Cannes, LATW in Montevideo, THERMES in Santa Fe, DFT in Vancouver, CASES in Grenoble and MEDEA+ Design Automation Conference in Stresa, the Laboratory will organize the High Level Design Validation and Test workshop in Cannes and the Memory Technology, Design and Test workshop in Isle of Bendor. These two workshops are moving for the first time to Europe. Two summer schools will also be organized on Multiprocessor SoCs and on Asynchronous Circuit Design.

The Report is organized into 8 main sections including the Research and Service activities, the Resources and the Technology Transfer activities.
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I - OVERVIEW - GENERAL INFORMATION

I-1 Organization

Since the late 60s, the members of the Laboratory have dealt with projects and tools on hardware and software:

Hardware:

- Computers:
  + the geo-physical machine GEOPROCESSOR (1970/1975)
  + the PASCAL machine PASCHLL (1972/1981)
- Microprocessor-based architectures:
  + electronic exchange system CANOPUS
  + the CORAIL machine
  + the CRESUS project
- Microprocessor type circuits:
  + microsequencer MSQ
  + microprocessor 8 bits NMOS P68
  + microcomputer 4 bits SOS MOM 400
  + the MOSAIC project for the architecture of VLSI systems
  + series line control by LISA microcontroller
  + microprocessor 8 bits POPY
  + microprocessor 8048 CMOS
  + microcontroller COBRA
  + mathematical coprocessor FELIN
  + compiled microprocessor 6502
  + MAPS controller
  + 1553 controller
- AI oriented machines
  + OPALE machine
  + LAIOS lattice
  + SPAN mechanisms
  + SYMBION architecture
- VLSI
- Macrosystems and Microsystems.

Software:

- Electrical simulation
  + IMAG 2
  + IMAG 3
  + IMAG 4
- Digital simulation
  + CASSANDRE
  + LASCAR
- System simulation
  + LASSO
- Multilevel, mixed-mode simulation
  + CASCADE
- Physical design
  + LUCIE
- Architectural synthesis
  + AMICAL
- Verification
  + PREVAIL
- Co-design
  + COSMOS

This experience serves as background to research in the field of the Design and Test of circuits and systems.

In 2001, the Laboratory was organized in 6 research groups, as listed below:

+ MiCroSystems (MCS), B. COURTOIS
+ Concurrent Integrated Systems (CIS), M. RENAUDIN
+ Reliable Integrated Systems (RIS), M. NICOLAIDIS / B. COURTOIS
+ System Level Synthesis (SLS), A.A. JERRAYA
+ Verification and modeling of Digital Systems (VDS), D. BORRIONE
+ QualiFication of circuits (QLF), R. VELAZCO
I-2 Research themes

Each topic of the research groups is briefly described below:

* MiCroSystems (B. COURTOIS)
  This research group addresses the following topics:
  + CAD tools for MEMS and MOEMS
  + testing
  + micromachining
  + thermal modeling

* Concurrent Integrated Systems (M. RENAUDIN)
  This research group addresses the following topics:
  + asynchronous circuits and systems (design and CAD tools)
  + microprocessors
  + low power, low noise circuit design
  + smart devices

* Reliable Integrated Systems (M. NICOLAI/DIS / B. COURTOIS)
  This research group addresses the following topics:
  + design of robust nanometric ICs
  + fault tolerant and fail-safe circuits
  + BIST and built-in self-repair
  + radiation hardened design

* System Level Synthesis (A.A. JERRAYA)
  This research group addresses the following topics:
  + application-specific multi-processor system on chip
  + software and RTOS synthesis
  + on-chip communication network
  + multi-level heterogeneous co-simulation

* Verification and modeling of Digital Systems (D. BORRIONE)
  This research group addresses the following topics:
  + specification languages
  + symbolic simulation
  + formal verification
  + theorem proving

* Qualification of circuits (R. VELAZCO)
  This research group addresses the following topics:
  + testing in harsh environment
  + radiation testing of integrated circuits and systems
  + fault injection
  + design and realisation of on-board satellite experiments
In addition, 3 multidisciplinary projects are ongoing:

* Global simulation of SOCs including MEMS and MOEMS
* WUCS: Wireless Universal Control Systems
* Architectures based on quantum effects
I-3 Some past realizations of the Laboratory

The following pictures illustrate some past and recent realizations of the Laboratory.

a) Cooperation with THOMSON led to the design of a self-checking, self-testing circuit (CMOS, 1.2 μ, 2 metallization layers, 650.000 transistors). The circuit is testable at the "transistors, metallizations, etc..." level (1985).

b) The SYCO silicon compiler took as input a behavioural ("Pascal like") description of the algorithms to be implemented in the silicon. b-1 is a 6502 CMOS control section compiled by the CPC specialized control section compiler ; b-2 is a 6502 NMOS data path compiled by the APOLLON specialized datapath compiler (ca 1988).

c) Electron-beam testing has been experimented through two equipments : a CAMECA ST-15 electron-beam tester and a JEOL 35C scanning electron microscope equipped for voltage contrast. Those equipments have been served by a SUN and an IBM workstation, respectively (1987 - 1993).

d) The FELIN circuit was a design resulting from a cooperation with the Parallel Algorithmic Laboratory. It is aimed at the calculation of elementary functions like sine, cosine, etc... The circuit involved approximately 100.000 transistors, fully generated by a program describing the circuit (1987).

e) CMP National Service gives the possibility to Research Centers, Universities and Commercial Firms to have their circuits manufactured. The Université Catholique de Louvain, CNET-CNS, THOMSON, MHS, ES2, TCS, AMS have manufactured bipolar, GaAs, NMOS and CMOS circuits for the CMP since 1981. One 4 inches wafer holds 73 CMOS different projects (15 wafers) and one 5 inches wafer holds 40 CMOS projects (5 wafers). Both have been processed by MHS, in 1986 and 1987, respectively.

f) The computing room regrouped computers that were not distributed in offices. Here are several SM 90, a SPS 9, and a MicroVAX. The air conditioned room had been fully remodeled in 1987 (electric power, floor, etc...). Today, all computers are distributed in offices.

g) In the past, computers have been designed. g-1 shows the GEOPROCESSEUR (1970) which resulted from a cooperation with IIP, g-2 depicts the PASCHLL (1976) language - oriented computer, and g-3 shows the CANOPUS (1980) system which resulted from a cooperation with CNET-LAA. Presently the computer architecture projects are dealing with parallelism and with a logic - numeric integration.

h) ADELAIDE was a project aimed at testing PCB populated by SMT devices. A prototype demonstrated the feasibility of an ATE, which uses extensively anisotropic elastomer conductors. Such a tool would allow a resolution of 10/1000 inches. The project has now been passed to industry.

i) Circuit synthesized by AMICAL (1993). This circuit is a PID synthesized by AMICAL (300 behavioral VHDL lines as input, 4000 RTL VHDL lines as output) feeding a commercial logic synthesis tool generating 50,000 transistors (20 mm², .8μ CMOS). Design time : 1 week. This design results from a hierarchical use of AMICAL. One of its components is a fixed point arithmetic unit that has been designed using AMICAL.

k) Microelectronics for Physics. BiCMOS wafer from CMP.

l) Micromachining by CMP. Process at industrial manufacturers, post-process at Central Laboratories.
a - Participation to a THOMSON project

d - FELIN project

f - computing room

h - SMT PCB tester

e - Electron beam testing

e - CMP service

Picture 1-3 1
Figure 3-b: SYCO silicon compiler
1 - GEOPROCESSEUR computer

2 - PASCHLL computer

3 - CANOPUS Distributed system

g - Past computer projects
i - Circuit synthesized by AMICAL.

j - GaAs wafer from CMP.
k - Microelectronics for Physics

1 - Micromachining by CMP
I-4  Some data on Grenoble's environment

Grenoble offers a very good environment in terms of Education, Research, High Tech Activities, Industry.

• Education

Grenoble has been awarded the "European University" title within the University 2,000 Project.
  * 55,000 students
  * 5,500 foreign students
  * 1,500 science degrees awarded each year
  * 1,000 engineers graduate each year
  * 600 "Erasmus" scholarship students
  * 1 International secondary school

• Research

Grenoble is the first French research center in Engineering Sciences, the second in Physics, the third in Mathematics.
  * 17,000 researchers (the largest concentration of CNRS researchers in Engineering Sciences after Paris)
  * 1,500 foreign researchers
  * 250 laboratories
  * 5 European research centers:
    - ESRF, European Synchrotron Radiation Facility
    - ILL, Laue Langevin Institute
    - IRAM, Millimetric Radio Astronomy Institute
    - SNCI, National Service for Intense Magnetic Fields
    - EMBL, European Molecular Biology Laboratory
  * 4 National research centers
    - CNRS, National Center for Scientific Research
    - CENG, Grenoble Nuclear Research Center
    - CNET, National Center in Telecommunications Research
    - CRSSSA, Research Centre for the Army Health Services
  * 1 research center of international proportions acquired every 10 years since 1946

• High tech Activities
  * Microelectronics  27% of jobs in France are located in Grenoble
  * Electronics  470 industrial companies, 13,250 jobs
* Biomedical technologies 104 industrial companies, 2,600 jobs
* Imaging technologies 50 industrial companies, 800 jobs
* Technopole of 65 ha housing 200 companies and 5,000 jobs (ZIRST Meylan)

** Industry **
* 3,500 companies created each year
* 133 foreign-owned capital companies, employing 25,000 people
* 1 Business District to welcome company headquarters and professional services
  (EUROPOLE)

** Electronics **
* Education: Engineering schools of INPG and UJF
  - ENSEEIHT
  - ENSERG
  - ENSGI
  - ENSIEG
  - ENSIMAG
  - ENSEPG
  - ISTG

* Research
  Laboratories of CNRS, INPG, UJF
  - CSI
  - LCIS
  - LEMO
  - LEPES
  - LMGP
  - LPCS
  - TIMA

* Infrastructures for research and education
  - CIME
  - CMP

* Applied research
  LETI, a division of the French Atomic Energy Commission (CEA)
  France Telecom R&D, Grenoble Center

* Industry
  STM Microelectronics, ATME, Thomson Electronic Tubes, Thomson Consumer Electronics, Thomson LCD, Schneider Electric, ANACAD, AURIS, Dolphin Integration, SOFRADIR, RADIALL, MEMSCAP, ARESYS, iROC, SOITEC, PITS
• History

43 b.c.: 1st mention of CULARO, a small town modestly built by the Celts to get across the Isère river, by Lucius Munatius Plancus in his correspondence to Ciceron.

III century a.c.: Construction of the first rampart.

379: Emperor Gratien promotes CULARO to the rank of chief town city and gives it its name: GRATIANOPOLIS.

VI century: Construction of a Christian funerary complex on the right bank of the Isère river.

1012: The Saint-Laurent group (right bank) is given to the benedictine monks of Saint Chaffre en Velay: founding of the Saint-Laurent priory and then, the development of a suburb.

c.1140: Rebuilding of the cathedral and its cloister.

1219: Flood; the bridge is taken away.

1228: Construction of the Collegiate Church Saint André: the "Dauphins" set up their administration at Grenoble.

1339: Creation of a University in Grenoble, including four sections: medicine, liberal arts (sciences and literature), canon law and civic law.

1391 - 1418: Construction of the Island Tower, first Town Hall.

1453: The setting up of the parliament of Grenoble: the town is officially recognised as a regional capital.

1593 - 1606: Construction of the wall of Lesdiguières.

1709: Birth of Jacques DE VAUCANSON, biomechanist. His automata (Le Joueur de Flûte, 1738) were aimed at "reproducing means in view to obtain the experimental intelligence of a biological mechanism".

1712: Birth of Joseph FOURIER, mathematician and prefect of Isère department. In 1811 Joseph FOURIER sets up the Faculty of Sciences. In 1987, the Scientific, Technologic and Medical University of Grenoble will take the name "Université Joseph FOURIER".

1783: Birth of Henri BEYLE, so-called STENDHAL, novelist.

7 June 1783: Day of the "Tuiles".
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<td>Construction of the HAXO fortifications.</td>
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<td>1869</td>
<td>Invention of the hydro-electric power, the &quot;White Coal&quot;, by Aristide BERGES.</td>
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<td>1946</td>
<td>National Council for Scientific Research (CNRS).</td>
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<td>1955</td>
<td>Grenoble Nuclear Research Center (CENG).</td>
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<td>1963</td>
<td>First laboratory integrated circuit at LETI.</td>
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<td>1965</td>
<td>First industrial integrated circuit at SESCOSEM. First computer LAG/INPG-MORS.</td>
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<tr>
<td>1966</td>
<td>Laéle Langévin Institute (ILL).</td>
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<td>1968</td>
<td>Winter Olympics in Grenoble.</td>
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<td>1970</td>
<td>Louis NEEL is Nobel Prize in Physics. Louis NEEL has been President of Institut National Polytechnique de Grenoble (formerly Institut Polytechnique de Grenoble), from 1954 to 1976; he is now Honorary President of INPG.</td>
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<td>1976</td>
<td>National Centre for Telecommunications Research (CNET).</td>
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<td>1985</td>
<td>Nobel Prize awarded to Klaus von Klitzing.</td>
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<td>1986</td>
<td>European Synchrotron Radiation Facility (ESRF).</td>
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<tr>
<td>1988</td>
<td>Research Centre for the Army Health Services (CRSSA).</td>
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<tr>
<td>1994</td>
<td>The European Synchrotron Radiation Facility is available to research scientists from virtually all countries.</td>
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II - RESEARCH ACTIVITIES

II-1 MiCroSystems (MCS)

*Group Leader:* B. COURTOIS  
(e-mail : Bernard.Courtois@imag.fr)

*Members:* S. BASROUR, B. CHARLOT, B. COURTOIS, C. DOMINGUES, N. GALY,  
J. GOY, Z. JUNEIDI, S. MARTINEZ, S. MIR, B. PALAN, F. PARRAIN,  
L. RUFER.

*Partners:* M. RENCZ, K. TORKI

Research areas:

The research activities of this group address the following:

- the development of micromachining techniques compatible with microelectronics,
- CAD tools for Microsystems,
- the design of safety critical and highly reliable Microsystems, particularly operating in harsh environment,
- micro-optics and MOEMS,
- ultra-sonic MEMS transducers,
- thermal testing,
- MEMS testing,
- MEMS for biometric applications.

Contracts:

European: PROFIT (IST), TECHNODAT(MEDEA+)
Memberships: NEXUS, NETPACK.

Industrial Partners:

AMS (Austria), SEMILAB (Hungary), SODERN (France), SCHNEIDER ELECTRIC (France),  
PML (France), BOSCH (Germany), SensoNor (Norway), STMicroelectronics, Philips, Infineon,  
Nokia, Flomerics
Start-up company created: MEMSCAP (France).

Topics:

One of the main obstacles to start with Microsystems is the fact that particular, and hence costly processes are needed. In order to get affordable prices and a high flexibility, Microsystems should whenever possible be designed in such a way that they can be realised on existing production lines for micro-electronics, with an additional post-processing for micro-system specific 2D and 3D structures, e.g. through Multi-Project-Wafer services. Furthermore, this approach allows to integrate microelectronics, needed in most Microsystems, on the same chip. This is the monolithic solution

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1: Technical University of Budapest, Hungary
which should be considered as the normal evolution of ASIC-foundries to microsystem-foundries (foundries strategy).

What is happening today with microsystems can be compared with the VLSI evolution during the early 80s, at the time of MEAD-CONWAY. Design rules easy to understand, basic CAD like MAGIC in the US and LUCIE in France, MOSIS in the US and CMP in France, have permitted non-specialists to get acquainted with VLSI. The difference between VLSI in the 80s and Microsystems today is that CAD for Microsystems must not be developed from scratch, but should be built on existing CAD systems. On fabrication, the manufacturing should be built on existing microelectronics manufacturing facilities to take advantage of the existing massive investments.

The MCS group within TIMA Laboratory is involved in the development of manufacturing techniques and CAD tools by the wish to make microsystems accessible to non-specialized institutions. In addition, the MCS group answers to the needs of the industry in the design of microsystems for safety critical and harsh environment applications targeting mainly, medical, aerospace and high temperature domains. The MCS group collaborates extensively with both industry, research laboratories and universities, and it put emphasis on the ability to work on medium term industrial projects.

II-1.1 Microelectronics compatible manufacturing techniques of microsystems

Members : B. CHARLOT, F. PARRAIN

There are two ways to manufacture microsystems : to develop processes specific to microsystems (hence these processes can address requirements specific to microsystems) or to use processes that have been developed for microelectronics. Among those later processes, some can be targeted to microsystems, again to address specific requirements, or it is possible to add special process steps to accommodate microsystems within integrated circuits. This later way will allow to collectively fabricate microsystems including the microelectronics part at a low-cost. This is the way addressed by the MCS group within TIMA.

II-1.1.1 Silicon compatible micromachining

The fabrication of silicon compatible micromechanical structures involves the deposition, doping of the necessary material and the selective etching of the underlying support. Two main methods can be used; bulk micromachining where structures are etched in the substrate, and surface micromachining where the micromechanical layers are formed from layers deposited on the surface.

Some advantages of these micromachining techniques include VLSI integration, low cost and rapid delivery.

Bulk micromachining is a process based on etching wells in the silicon substrate, leaving suspended structures. Using this micromachining technique, devices such as micro-hotplates, infrared sources, thermal flat-panel displays, CMOS thermopiles, thermal converters, gas flow sensors, channels for fibres, and piezoresistive sensors can be developed. In bulk micromachining two techniques can be used: etching from the front-side or etching from the back side.

Works at the MCS group address mostly front-side bulk micromachining. In the back-side bulk micromachining the structures are usually large and alignment is difficult. If the bulk micromachining is performed from the front-side this alignment problem is immediately removed and dimensions can be reduced. The end result after CMOS fabrication is an open in the dioxide and nitride mixture passivation that exposes the bulk silicon surface. These chips are placed into an anisotropic etchant, such as EDP (ethylenediamine-pyrocatechol-water) or TMAH
(tetramethylammonium hydroxide) or KOH (potassium hydroxide), and the exposed silicon is anisotropically etched.

Figure II-1.1 Schematic cross section of a CMOS integrated circuit with bulk micromachined parts

After the 1.0μ CMOS (SLP / DLM, from ES2), the 1.2μ and 0.8μ CMOS (DLP/DLM, from AMS) bulk micromachined technologies, the 0.6μ CMOS compatible front-side bulk micromachining has been fully validated. These technologies have been transferred to the CMP Service. The 0.6μ technology affords to work with 2 polysilicon layers and three metal layers. Each layer is planarized which is very interesting for optical applications. The low resistivity of the metal (interconnection between metal2 and metal3) and the etching of the substrate under the structure afford to realise passive component, like inductor. This technology also offers the possibility to use the Seebeck effect with termocouples. Poly/Alu couple shows a Seebeck coefficient close to 240μV.K⁻¹.

Figure II-1.2 Suspended electro thermal converter (a) and inductor (b) manufactured using .6μ CMOS (from AMS) compatible front-side bulk micromachining

II-1.1.2 Gallium arsenide micromachining

In the last two years, the feasibility of front-side bulk micromachining by using GaAs microelectronic technologies has been demonstrated. The open areas to be micromachined, when placed appropriately on the die, allow such as bridges, cantilevers and membranes via additional post-process to fabricate 3D microstructures wet etching respecting the total integrity of the other parts of the die (electronics, passivation).
The latest research works in this field targeted the characterization of several wet etchants in terms of etch rates, selective and preferential etching characteristics in order to produce three kinds of free-standing structures, specifically:

1. GaAs/AlGaAs mesa-shaped structure,
2. triangular GaAs prism-shaped structure and
3. suspended metal/oxide or nitride structure without GaAs material.

Each of these structures is suitable for a specific application and need a specific etching solution to be realized.

![Image showing MEMS devices](image-url)

**Figure II-1.3 MEMS devices manufactured on the 0.2μ HEMT GaAs compatible front-side bulk micromachining**

### II-1.2 CAD tools for MEMS

*Members: Z. JUNEIDI, K. TORKI*

Starting from the 70s, Microelectronics development has been made possible because of the use of CAD tools and because of the availability of foundries for Education/Research and for fabless companies, besides large IC manufacturer. Without such similar boosters, Microsystems might easily remain curiosities, top level prototypes manufactured by researchers, but they would not become industrial products.

Long ago, Education and Research in Microelectronics had taken advantage of CAD tools developed in USA and in France: MAGIC in Berkeley, LUCIE in Grenoble. These tools were provided free of charge. Later, most Universities have been provided with commercial CAD tools. Considering the background on CAD for Microelectronics, a few principles should govern the development of CAD for Microsystems:

* CAD for Microsystems should not be fully designed from scratch, but modules available for Microelectronics should be reused when existing;
* a CAD for Microsystems should look familiar to a user of CAD for Microelectronics;
* the "system" user should be distinguished from the "library" designer;
* but the challenge is to put together a framework where the "library" designer will find tools he has been using for years, besides the tools used by the "system" user.

Also, the ongoing Intellectual Property (IP) issue on electronic cores (business models, alliances like the Virtual Socket Interface) will soon emerge as an (maybe even more acute) microsystem cores IP issue.
II-1.2.1 Microsystem synthesis

The objective is to generate automatically an optimized MEMS component from its behavioral description. The resulting MEMS structure should match in performance, compatibility, and right interfacing with the electronic circuitry and/or other MEMS devices connected around. For achieving this, the research work is to setup rules for the behavioral description using a standard high-level description language. These rules will allow the interpretation of a model description by a parser to be targeted into an intermediate language and database which will be the input of the optimizer. This includes three tasks:

1. Definition of synthesis language:
   This language will be a subset of a high-level language. Directives will be added to the original language in order to allow the parser extracting the necessary parameters.

2. Implementation of a synthesis language parser:
   This parser will use the directives of the synthesis language in order to get the functional, the geometrical and the physical parameters. Those parameters will be injected into an intermediate language and database which will be the input of the optimizer.

3. Optimization of synthesized model parameters:
   The optimizer will determine the right parameters of the MEMS model depending on its geometric and physical constraints and in accordance to the interfaces and connected components. The optimizer will propose several optimal solutions which are back annotated to the initial MEMS model. This allows the simulation of the different solutions. The designer will be able to select the desired one.

![Figure II-1.4 Schematic principle of the layout synthesis](image)

II-1.2.2 Layout design rules checking

An approach to MEMS Computer Aided Design tools has been to make use of Integrated Circuits CAD suites with specific enhancements for MEMS designs. Extending the IC Design Rule Checkers to non-manhattan shapes is one of these needed enhancements. If anecdotically used in IC designs, non-manhattan shapes are intensively used in today state of the art MEMS products. High performance gyroscopes and yaw rate sensors made in surface micromachining processes feature spiral springs and torsional combdrives made of toroidal fingers.

Applying classical DRCs to these layouts generate thousands of false errors. The errors are false because they do not affect the manufacturability of the device. But because of their number, they prevent the designers from detecting real errors in their layout. Most false errors are generated by rounding floating point vertices' coordinates, translating different data types (some tools use primitives) and snapping points to a grid.

A new methodology to eliminate false errors generated by the DRC of non-manhattan shapes has been developed. This methodology includes adding a tolerance factor to Microsystem design rules with respect to the geometric properties of non-manhattan shapes and the manufacturing grid parameters, closely control the vertices coordinates when automatically generating the non-manhattan shapes and control the snapping on the grid.
II-1.3 MEMS testing

Members: S. MIR, B. CHARLOT, C. ROMAN, B. COURTOIS

MEMS are evolving from simple components to whole systems. Increased miniaturisation, in conjunction with an ability for mixed integration with electronic circuits, are key factors for the emergence of a new generation of chips embedding MEMS. Testing is a main concern for this new generation of chips. As in the microelectronics industry, the development of cost-effective tests for larger systems may well require test stimuli targeting actual faults, developing fault lists and fault models for realistic defects, and using fault simulation as a major approach for assessing testability and dependability.

II-1.3.1 Micromachining defects and failure mechanisms

Failure mechanisms and defects have been analysed in numerous MEMS fabricated using CMOS-compatible bulk micromachining, via the CMP service, and using surface micromachining via the MCNC MUMPS process. The inspection of failed devices has allowed the identification of defects and design errors typically occurring for this type of MEMS. We illustrate some examples for suspended thermal MEMS in Figure II-1.6.

Several mechanisms can prevent a full release of a suspended microstructure including the presence of unwanted oxide residuals, insufficient etching time, slow etching rate because of an
inadequate solution and the formation of hillocks, or re-depositions of etched material which may occur after micromachining. Figure II-1.6 (a) illustrates an electrothermal converter (ETC) for which the suspended cantilever has not been fully released. In this case, bulk micromachining was not applied for a sufficiently long time. It is possible to see through the silicon dioxide beam, semitransparent to the electronic microscope, the triangular shape of the silicon material under the beam which has not yet been removed. As a second example, Figure II-1.6 (b) shows an optical microscope photo of a thermal pixel chip reject. A silicon dioxide membrane is used to suspend a polysilicon resistor. Since the beams supporting the membrane have large thermal resistance, the heat generated by the resistor results in a temperature increase in the membrane and a visible heat radiation. It can be observed through the dioxide, semitransparent to the optical microscope, that part of the membrane in the central part was not freed (lighter region), and most of the heat generated by the resistor in that part is evacuated via thermal conduction to the bulk. The first part of the resistor is suspended, and the heat radiation is observed.

II-1.3.2 Fault modelling

MEMS are analogue devices, working at least partially in the electrical domain. The distinction between parametric and catastrophic faults typical of analogue electronics testing appears again for MEMS. By adequately modelling these fault effects for circuit simulation, integration of design and test can be envisaged, selecting adequate test patterns which optimise defect and fault coverage and facilitate diagnosis. We illustrate some examples of fault modelling in Figure II-1.7.

On one hand, thermal MEMS are typically described using equivalent electrical circuits, keeping an adequate linkage to the physical layout. The defect shown in the electrothermal converter of Figure II-1.6 (a) changes the heat flow in the cantilever leading to an incorrect temperature map. This is modelled at circuit-level in Figure II-1.7 (a): the cantilever is represented by means of a two-dimensional heat transmission line and the defect is modelled conveniently using thermal shorts between the suspended cantilever and the substrate.

Figure II-1.7 Fault modelling of micromachining defects at circuit level: (a) modelling the inadequate release of a cantilever using thermal shorts in a 2-D heat transfer, and (b) modelling of an electromechanical open in a micro-resonator due to a finger break.

On the other hand, an electrical equivalent circuit of the behaviour of an electromechanical micro-resonator does not keep the linkage to the physical layout. The electrical equivalent circuit models the behaviour of the overall device, but does not allow the injection of the most common faults such as those caused by finger breaks. What is needed is an electromechanical model of the device at circuit level as shown in Figure II-1.7 (b), where basic components are interconnected by means of mechanical and electrical lines, representing the interactions between basic components and
keeping the linkage to the physical realisation. The modelling of this fault becomes than easy by opening the connections between the beam that represents the broken finger and the beams that should support it.

II-1.3.3 Design-for-test for MEMS applications

A major problem for applying self-test techniques to MEMS is the multi-domain nature of the sensing parts that require special test equipment for stimuli generation. By implementing electrically induced stimuli for MEMS parts, we could avoid the use of specific test equipment and allow a complete built in self-test design. We have implemented self-test functions on specific MEMS applications such as a thermopile based infrared sensor and a piezoresistive micro-beam fingerprint sensor. Figure II-1.8 illustrates this second case: the electrically induced stimuli are obtained by placing a heating resistor in each micro-beam of the fingerprint sensor. When activated, the heating resistor will warm up the beam causing a bending down effect due to a difference of thermal expansion coefficient within the layers of the structure. The bending will create a compressive stress in the beam that mimics the effect produced by the movement of a finger on the surface.

![Figure II-1.8](image)

(a) SEM photo of a piezo resistive microbeam including a heating resistor, (b) schematics of the resistors on the microbeam and (c) FEM thermomechanical simulation of the bending

II-1.3.4 Microsystem CAD tool for fault simulation

We are currently working in an A-HDL-based fault simulation tool that will extend the capabilities of equivalent tools for analogue and mixed-signal electronic circuits to microsystems. Thus, the tool should be compatible with IC design environments and must allow the joint consideration of microelectronic and non-electronic parts.

Fault modelling will be facilitated by the use of a fault model description language, allowing the consideration of both behavioural and topological fault constraints. After a set of fault models has been provided by means of this tool, matching of the fault models with the design under test results in an automatic generation of a fault list. The fault model must also provide all details of how a fault must be injected. Thus the overall fault simulation process can become fully automatic once the fault models have been specified.

The tool should be integrated in the CADENCE IC design environment. Procedures written in the CADENCE language SKILL will allow acquiring knowledge about the design objects. The fault modelling language will contain both graphical and textual interfaces to specify behavioural and topological fault constraints for a fault model. This description will be interpreted by SKILL procedures and matched with the design to generate the fault list. From each fault in the list, a different device model is produced and simulated with Spectre-HDL. Fault models can contain Verilog-A descriptions, in particular those generated by model generation tools. The fault
simulation tool will have SKILL procedures to analyse output results and compute fault coverage figures for different test parameters.

II-1.4 Acoustic and ultrasonic MEMS devices

**Members : L.RUFER, S. MIR, Ch. DOMINGUES**

Acoustic devices employ elastic waves propagated in liquid or solid medium for acoustic signal reception or generation. Such devices, being the input and/or output part of a system, play an important role in many acoustic and ultrasonic applications. Acoustic device can be regarded as an electroacoustic transducer and an electronic part. The electroacoustic transducer ensures the signal conversion, and the electronic part is necessary for signal detection, amplification, and processing.

Recent advances in microfabrication technology have opened novel design possibilities for this kind of devices. Micro-Electro-Mechanical-Systems (MEMS) based on technologies used in microelectronics can work as electroacoustic or electromechanical transducers and can form a heart of an acoustic device. The use of silicon micromachining in the transducer fabrication process gives a number of advantages, including the transducer small size, high precision and low cost. Another advantage consists in the possibility of integrating such a transducer altogether with electronic circuits on a same chip.

As regards the frequency range of operation, we distinguish two forms of devices, acoustic in low frequency range and ultrasonic in higher frequency range. Both forms of these devices are often called acoustic. MEMS devices working in acoustic frequency range (from 20 Hz to 20 kHz) are more often used as sensors (microphones). The development of MEMS based acoustic sources in low frequency range is more difficult because of small dimensions of the membrane surface, but is possible for the use in small closed volumes (hearing aids). MEMS devices designed for the frequency range from tenths of kHz to low GHz range can work both as sensors and sources of ultrasonic signals.

Other classification approach may be based on the transducer working principle. There are different physical effects used for acoustic waves sensing and generation and most of them are applicable in the case of MEMS. The piezoelectric, piezoresistive, capacitive, and thermoelectric effects are among the most appropriate principles used in the case of acoustic MEMS.

Piezoelectric transducers can work in different configurations. All of them are based on elastic motions in transducer solid members that are usually designed in the form of a plate. Depending on the size of the solid plate forming the transducer and on the way the signal is generated or received, different modes can be distinguished. There are surface acoustic wave devices based on generation, propagation and reception of elastic wave on the surface of the solid body. There are also devices employing the bulk elastic waves in different modes (longitudinal, shear, or flexural).

Piezoresistive transducers use a material property where the bulk resistivity is influenced by the mechanical stresses applied to the material. Transducers of this type are formed either by a membrane or by a beam with usually four piezoresistors integrated on them. Piezoresistors are then connected in a Wheatstone-bridge which converts the resistance change directly to a voltage signal. Piezoresistive transducers can be used only as sensors.

Capacitive (electrostatic) transducers consist basically of two plate electrodes separated by a dielectric. One of these electrodes is usually fixed; the other being free can be used for acoustic signal sensing or generation. This transducer arrangement requires a source of polarisation voltage that can be replaced by a deposition of electret material on one of the transducer plates.
Electro-thermal mechanism can be used to produce vibrations of a solid body and thus generate the acoustic wave in adjacent medium. The principle of the mechanism is that the heat obtained from the electric current is applied at the top side of the membrane. The heat generated at the surface will diffuse and hence a gradient in the temperature will be created. Due to a thermal expansion of the material, a mechanical moment, resulting in bending of the membrane, will be induced. Such a mechanism, being irreversible is used for excitation of mechanical or acoustic waves.

Electro-acoustic transducers can be used as sensors (microphones) in a wide variety of applications, such as hearing-aids and other instruments in which space is constrained (mobile phones, headsets, wearable computers ...). Ultrasonic transducers find their use in medical imaging, NDE/I (non-destructive evaluation/inspection), acoustic microscopy, shape reconstruction and acoustic vision, proximity detection, distance measurement and others.

The Microsystems research group of the TIMA laboratory currently carries out several projects whose aim is the development of different types of MEMS-based electro-acoustic and ultrasonic transducers. One of the projects concerns the development of Capacitive Micromachined Ultrasonic Transducer (CMUT). Such a transducer will be used in the field of air-coupled Non-Destructive Testing (NDT) and/or in medical imaging applications. Non-destructive testing of advanced materials used in aerospace, nuclear, oil, gas, marine, or automobile industries is crucial for safety critical applications. Ultrasonic inspection is the most common technique; however it requires the use of a couplant, which is a great disadvantage for numerous applications. Air-coupled ultrasonics presents many advantages for intelligent production, such as high user-friendliness, improved quality inspection and reduction of resource consumption by the elimination of the liquid couplant, typically water. This technique, not yet available in current NDT equipment in Europe, presents important research challenges.

The project researches air-coupled capacitive transducers fabricated using Microsystems technologies. The use of arrayed micromachined transducers embedded in NDT probes can result in an enhanced frequency bandwidth (possibly from 40 kHz to 2.5 MHz in a temperature range from 20°C to 200°C), with the possibility to program resonant frequencies, which gives a flexibility of use and a customisation for a given application. Moreover, the microsystem technology guarantees high reproducibility and miniaturisation of the probes. In summary, the use of such probes for NDT testing allows for significant reduction in development and production costs with applicability for intelligent process control (IPC).

This research will lead to the design and fabrication of this type of micromachined transducers, including the necessary front-end electronics for signal conditioning. The main parts of the project are transducer modelling and simulation, transducer micro-mechanics and transducer micro-electronics.

In a similar project, the capacitive microphone is studied. A microphone with a sensitivity covering the audible frequency range is aimed at. As in the previous project, modelling and simulation of the transducer is a crucial part of the project. Modelling is based on Finite Element Analysis combined with a circuit level description suitable for simulation using Hardware Description Languages (HDLs).

Transducer micro-mechanics part of the project involves design and fabrication of transducers, etching of sacrificial layers, transducer chip encapsulation and preliminary characterization. Fabrication of the transducers will be done via the CMP service using a surface micromachining technology proposed by Multi-User MEMS Processes (MUMPs).
Transducer micro-electronics part of the project aims at the design of signal preamplifiers made in CMOS technology. Small transducer dimensions lead inevitably to low signal levels and low signal-to-noise ratios which demand a careful design of the electronic part of the device.

Another research project deals with an ultrasonic transducer for a pulse-echo ultrasonic application, using an electro-thermal excitation and piezoresistive signal detection. The proposed MEMS device is illustrated in Figure II-1.9. A squared membrane made of silicon dioxide (SiO$_2$) and silicon nitride (Si$_3$N$_4$) layers is suspended by back-side silicon bulk micromachining. Heating resistors are placed in the central part of the membrane providing a thermo-mechanical excitation. Four piezoresistors are placed on the membrane sides where mechanical stresses caused by the membrane displacement are maximal. Two of them are parallel to the edge and the other two are perpendicular. Finally, four thermopiles are placed diagonally from the corners of the membrane towards its centre. They serve for measuring the membrane temperature.

![Figure II-1.9 Components of the ultrasonic MEMS device](image)

The total thickness of the membrane is about 5.2 µm and its dimensions are 1.3 mm x 1.3 mm. This size results in a resonant frequency about 40 kHz.

During the emission, the membrane is placed in an oscillator loop and is thermally actuated at its resonance frequency (≈ 40 kHz). This frequency is slightly dependent on the membrane average temperature. The electronic interface circuit monitors this temperature. The membrane oscillations generate an ultrasonic signal (pulse) that propagates in the air and interacts with a solid body. As a result of this interaction, ultrasonic signal is reflected on the solid surface and is received by the microsystem (echo). During the reception, a piezoresistive bridge placed on the membrane is used for monitoring the membrane deflections. The resonance frequency of the membrane is tuned to the emitted frequency by keeping the membrane at the same temperature, achieving then the highest sensitivity.

A complete behavioural model of a pulse-echo system including the electrical, thermal, mechanical, and acoustic parts has been developed. The simulation results show the feasibility of a MEMS-based system using electro-thermal excitation and piezoresistive sensing at 40 kHz. Temperature effects have been considered in detail, in particular the control of the high temperature on the membrane surface, keeping the same value during emission and reception, and thus maximising the device sensitivity. This type of device can be used as a presence detector for distances up to a few tens of centimetres.
II-1.5 **MOEMS and CMOS image sensors**

*Members : J. GOY, S. MARTINEZ, B. CHARLOT, F. PARRAIN, S. MIR*

II-1.5.1 **CMOS infrared thermopile based sensor**

The thermopile-based infrared imager is a sensor composed by a matrix of pixels (8x8 for this first prototype) made by means of CMOS-compatible front-side-bulk micromachining via the CMP service using an Austria Mikro Systeme (AMS) 0.6 µm CUP process. The pixel is composed by a membrane (90x90 µm²) suspended by four narrow arms containing thermopiles.

![Layout of the first prototype. Details of the suspended membrane on the right.](image)

Many applications of CMOS-compatible bulk micromachining are based on the use of thermopiles on suspended structures as bridges or membranes (for example thermal breaker, vacuum sensor, gas flow sensor ...). A thermocouple is a temperature sensor using the Seebeck effect that generates a voltage at the ends of a junction (the hot and the cold point of the thermocouple) of two different materials (in our case Polysilicon/Aluminum) placed on a thermal gradient. In order to increase the sensitivity of the sensor several thermocouples can be connected in series to form a thermopile. Thermopiles present several advantages as non-offset and very low noise.

Suspended structures (as our pixels) are thermally isolated from the bulk that can be considered at ambient temperature. Thermal isolation can be improved by high vacuum packaging. In our device, the low thermal conductance of the structure is exploited to measure the incoming infrared radiation absorbed by the passivation Si₃N₄ layer that will heat up the membrane. The temperature rise is detected by means of thermopiles with the cold points placed on the bulk and the hot points on the structure. The seebeck coefficient for a Polysiliconium/Aluminum couple is very closed to 230 µV/K in the technology we have used which allows us to obtain a responsivity of 130 V/W for the pixel.
Each thermopile delivers a voltage with an amplitude below 1 mV which will be amplified using a switch capacitor circuit with autozeroing and modulation in order to reduce DC offset and Flicker (1/f) noise. The input signal is first modulated before being amplified by two consecutive stages (total gain of about 64 dB) with offset cancellation. The output of the second stage is buffered and fed into a demodulator.

In order to implement a self-test function a heating resistor is placed on the middle of the membrane. The heating resistor will heat up the membrane and produce an electrical signal into the thermopile as a heat generation induced by an incoming infrared radiation. It is then possible to measure the thermal time constant on each pixel and the output level for the constant power induced. This test stimuli allows the detection of faults affecting each pixel as, for example, non-released arms caused by insufficient etch, broken arms, shorts and opens circuits in polysilicon or aluminum lines or dust membrane.

This imager can be used in multiple applications such as overheating detection, night vision, thermal tracking and earth tracking for satellite positioning for example. A self-test approach can be very important for IR imagers embedded into a System-On-a-Chip (SOC) devices including in the same chip the sensor and the computing electronic.

### II-1.5.2 Optical Cross Connects

The capacity of Optical Networks is increasing exponentially due to an equal exponential increase in available number of wavelength channels. At the same time, Optical Amplifiers have allowed to enlarge transmission distance in long-haul point-to-point communication systems without the need of expensive electronic repeaters. However, even if Dense Wavelength Division Multiplexing (DWDM)
and Optical Amplifiers are key developments, these technology advances satisfy only partially the demands of new communications services; it seems difficult to take full advantage of this superior transmission bandwidth and extra transmission distance if parallel developments in network connectivity are not achieved. Transmission capacity available through DWDM is too large to be entirely exploited by single transmitter-receiver pairs in isolated point-to-point communication links. A much more cost effective communication solution is a multi-node architecture sharing a high-bandwidth optical layer among different services, and linking many transmitter/receiver locations; that is, a meshed network approach with nodes switching/routing signals dynamically, see Figure II-1.13. The optical layer shown in Figure II-1.13 is interconnected by means of devices commonly known as Optical Cross-Connects (OXC).

![Optical Cross-Connect](image)

**Figure II-1.13** A Network showing the Optical Layer and the Optical Cross-Connects

Among the different approaches for OXC's, free-space devices stand out due to their low attenuation and low cross-talk. Furthermore, the recent use of micromachining technologies for OXC fabrication promises not only to improve the performance of these components but to substantially reduce the manufacturing costs.

At TIMA, we work on micromachined Free-Space OXC's based on Micro-Mirrors; we mainly explore fabrication techniques, modeling and simulation approaches, and potential applications.

Fabrication Techniques.

There are two main approaches: Surface-Micromachining and Bulk-Micromachining. Surface-Micromachining provides for high design flexibility, it allows fabrication of real three dimensional devices by raising or turning the structures up the substrate plane. When using Surface-Micromachining, the main challenge is related to mirror concavity due to residual stress accumulated in the different layers during deposition. Most of our research activities have been around Surface-Micromachined Cross-Connects, a mirror-matrix of free-rotating mirrors actuated by electrostatic devices is shown in Figure II-1.14.

In contrast to Surface-Micromachining, Bulk-Micromachining provides for limited design flexibility; however the use of Silicon-on-Insulator (SOI) wafers combined with Deep Reactive Ion Etching (DRIE) and Wet Etching has recently attracted attention due to the good quality mirrors that can be fabricated.

Modeling and Simulation Approaches.

As many other MOEMS applications, an Optical Cross-Connect is an example of an heterogeneous system involving the Optical, Electromechanical, Optoelectronic and Electronic domains. We work on models for different components used in OXC's and propose approaches for system-level simulations.
Potential Applications.

Concerning transport network requirements, Cross-Connects showing attenuation lower than 2.5dB, cross-talk lower than -30dB and switching times lower than 10ms are already useful in some applications like bandwidth provisioning, fault protection and restoration. These specifications seem attainable by micromachined devices.

![Cross-Connect Diagram](image)

**Figure II-1.14** A 4x4 Surface-Micromachined Optical Cross-Connect. (a) General Architecture, (b) Mirror Detail

II-1.5.3 **Active Pixel Sensor (APS)**

Charge Coupled Devices (CCD) have reached a very high level of performance, since their appearance in the 70's. They are used in several applications such as multimedia or space star trackers. However, they now appear to be limited by their cost, their slow readout rate, their resolution, or their radiation softness.

The Active Pixel Sensor technology seems to be a possible successor of CCD's. It is characterized by the addition of electronic transistors within each pixel of the sensor. These transistors are used to buffer the signal coming from the pixel through a set of lines or columns crossing the array. This processing technique offers numerous advantages:

- the photoelectric signal coming from the pixel is directly transmitted to the column amplifier, eliminating the CCD problem of charge transfer
- the random access to a pixel or a window of the sensor reduces consumption and increases readout rate
- the CMOS-compatible APS fabrication reduces chip price and ameliorates pixel density.

A 256x256 APS array has been fabricated in AMS 0.6μm technology. It is designed to be used into a satellite in-flight star tracker. With a fill factor of 70% (ratio of photosensitive area regardless to the size of a pixel), it has a very high dynamic range and a very low noise level. The electronic control allows random access, windowing, shutter speed and frame rate control.

Within each pixel, the signal is first integrated into the photosensitive area (photodiode or photoMOS), then transferred to the sensor columns. The duration of the pixel reset determines the shutter speed.
The access to each pixel is made by selecting one line of the sensor and reading the response corresponding to the desired pixel on its column. Thanks to X and Y decoders, we can process any part or pixel of the sensor.
Some tests on the chip have revealed that the major problem resulting with common APS arrays are the non-uniformities of the columns amplifiers, resulting in column offsets and gain variations. A new architecture of pixel has been designed which eliminates the use of the transconductance transistor and thus the problem of column dispersions. Furthermore, this architecture integrates the photonic current into a poly1/poly2 capacitor, resulting in a low noise, a good sensitivity, and better radiation hardness for space applications.

We obtain the following performances:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>256 × 256</td>
</tr>
<tr>
<td>Pixel size</td>
<td>30μm × 30 μm</td>
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<tr>
<td>Fill factor</td>
<td>70 %</td>
</tr>
<tr>
<td>Windowing</td>
<td>yes</td>
</tr>
<tr>
<td>Shutter speed</td>
<td>1ms - ∞</td>
</tr>
<tr>
<td>Dark current</td>
<td>~ 600 pA/cm² at 25°C</td>
</tr>
<tr>
<td>Pixel response non-uniformities (PRNU)</td>
<td>σ = 1.8 %</td>
</tr>
<tr>
<td>Pixel offsets non-uniformities (DSNU)</td>
<td>σ = 2.5 %</td>
</tr>
<tr>
<td>Columns response non-uniformities</td>
<td>σ = 2.0 % expecting 0 % in the future</td>
</tr>
<tr>
<td>Columns offsets non-uniformities</td>
<td>σ = 3.1 % expecting 0 % in the future</td>
</tr>
</tbody>
</table>
II-1.6 Fingerprint sensing

Members: B. CHARLOT, F. PARRAIN, N. GALY

II-1.6.1 Fingerprint sensor using piezoresistive microbeams

Nowadays, the need of identifying users is becoming more and more necessary for several typical operations such as access controls, workstation login or electronic banking. In this way, many systems as credit cards, mobile phones or computers require keys or alphanumeric passwords. Biometrics recognition is envisaging new solutions using constant features of the user’s body with the convenience that they can’t be lost, forgotten or stolen. We can give as examples the human speech, the characteristic of the face, the pattern of the iris and so on. Most applications are based on the fingerprint pattern that is the easiest to use. A typical fingerprint covers an area of about 100 mm² and includes several characteristic points so called minutia (generally a number from 12 to 20). Extracting their relative positions, these minutia allow to create a specific signature for each user guaranteeing a secured identification. The criminal science has been using fingerprints for more than 150 years therefore a complete theoretical and practical knowledge has been developed on signatures extraction and comparison.

It is possible to classify fingerprint sensors according to the read mechanism it works (mechanical, optical, capacitance and thermal) and according to the sensor array arrangement (single line, full or partial matrix of pixels). Until now the most used sensing part geometry has been the full or partial array but in this case the sensor is very expensive due to the fact that it covers a large area of silicon.

We propose to realize a fingerprint sensor composed by a unique row of microbeams (in fact three in the case of the first realized prototype) so as to minimize the size of the chip and consequently its prize. In order to obtain a complete image from this single row of pixels, the user has to pass his finger following a translation movement above the active area of the sensor. In the same time, the different gauges included in the microbeams are scanned. The resistivity change induced by the microbeam deflections (i.e. the finger relief) is then amplified and numerized (8 bit i.e. 256 gray scales) using the integrated electronic interface. The Figure II-1.20 shows the process of fingerprint acquisition.
The first prototype realized includes three rows of microbeams composed by just 38 elements whereas a complete sensor has to integrate 256 pixels per line so as to obtain a full image of the user’s finger (image width of about a half inch at 512 dpi that is a standard of this kind of chip). The reduced number of pixels allows to minimize the cost of the first chip just dedicated to test. The tiniest chip that is possible to saw from a wafer has a minimum size of about 2 mm. According to this fact, it is easily possible to integrate several rows of microbeams without the need to increase the actual size of the sensor. The first chip includes three rows of pixels with the same microbeams but with different cavity sizes. The chip is composed by two distinct parts: The MEMS part and the electronic part (amplifiers, converters etc ...) including pads that are placed at one tip of the chip so as to ease the bonding and the packaging. Figure II-1.21 shows the layout and an artistic three dimensional view of the sensor.

Figure II-1.21 Layout of the first prototype (a). Artistic 3D view of the sensor after TMAH release

Figure II-1.22 shows a fingerprint image obtained from the sensor without any additional signal processing except offset correction. This image has been recomposed using the analog signal directly available from the amplifier output in order to improve the measure (no saturation or quantization distortion induced by the analog/digital converter implemented). Knowing the amplifier gain, it is possible to determinate the resistivity change of the gauges that is induced by the fingerprint relief.

Figure II-1.22 (a) Comparison between the sensor output image and the original fingerprint used (inked reference fingerprint shown at left). (b) 3D isometric view of the output image
We can measure resistivity change of more than 6% (see Figure II-1.22) without breaking any microstructure. This value is in accordance with the resistivity change range given by FEM simulations performed using ANSYS. According to these simulations, a resistivity change of 6% corresponds to a deflection of about 3 μm at the tip of the microbeam.

We expect to go further in the integration into complex SoC device including the MEMS parts, analog signal processing unit and large digital cores. This highly integrated fingerprint recognition system will make possible to perform, using a single chip, the scanning of the fingerprint, the image processing, the signature extraction and matching.

II-1.6.2 Fingerprint recognition algorithms

A fingerprint matching algorithm has been implemented to create an application for the sensor developed by MCS. Numerous algorithms exist but most of them follow the same principle: singular points are extracted from the acquired image and then compared with a database.

On a fingerprint singular points are ridge endings or ridge bifurcations and they are called minutiae (Figure II-1.23). To compare two fingerprint images one compare the two sets of extracted minutiae.

![Fingerprint characteristics](image)

The algorithm that we used, as shown in Figure II-1.24, is divided down into four parts:

- The acquisition phase: we use the fingerprint sensor described in § II-1.6.3. The sensor provides 256 gray scale images whose width is fixed at 256 pixels and height is variable between 128 and 384 pixels.

- The pre-processing phase: in the course of the fingerprint acquisition process the acquired image can be damaged and we may obtain a low quality image. Thus an enhancement process is necessary to extract the singular points with precision. We directionally filter the image by block: the image is divided into blocks such that block’s ridges are locally parallel, the local direction is calculated and the block is filtered in that direction. Indeed this type of filtering enables a better enhancement than classical filtering by using the direction information. If ridges are locally parallel, the Fourier transform shows two local maxima (see Figure II-1.25).
Directional filters like Gabor filters (Figure II-1.26) use the directional information to improve the image in the given orientation.

The minutiae extraction: minutiae are ridge endings or ridge bifurcations, their positions is a unique signature for each person. Minutiae are easily extracted from the skeleton obtained in the previous phase. Indeed we can assume that if a pixel is on a thinned ridge then it has a value 1, and 0 otherwise. Let \((x, y)\) denote a pixel on a thinned ridge, and \(\{N_i \mid i \in \{1, \ldots, 8\}\}\) denote its 8 neighbours. Then \((x,y)\) is a ridge ending if \(\sum N_i = 1\) and a ridge bifurcation if...
For each detected minutia we record the coordinate, the type of minutia and the local ridge orientation.

- The enrollment/matching phase: that phase consists in matching two minutiae sets. It must take into account possible deformations between the two samples. The point sets are compared by using a string matching algorithm.

![Figure II-1.27](image)

**Different steps of the algorithm. (a) Input image. (b) Filtered image. (c) Binarized image. (d) Skeletonized image. (e) Minutiae detection**

In long term the objective is the obtaining of a system on chip which would regroup the sensor, the fingerprint recognition algorithm and the analog/numeric processing electronic.

### II-1.7 SOCs embedding MEMS/MOEMS devices

*Members: S. Martinez, G. Nicolescu, S. Mir, B. Charlot, F. Parraín, A. Jerraya, B. Courtois*

This research activity involves the Microsystems (MCS) and System Level Synthesis (SLS) Groups. It concerns the design and global validation of heterogeneous systems embedding MEMS/MOEMS parts in either a single mixed-technology (CMOS + micromachining) SOC device, or alternatively as a hybrid system with the MEMS/MOEMS part in a separate chip.

These systems are extremely heterogeneous, including not just electronic hardware and software but mechanical and optical hardware devices. Being competitive in developing these complex systems requires procedures for rapid generation of models describing different system parts and procedures for the global validation by simulation. This allows detecting and correcting design errors in the early stages of the projects and consequently reducing the time to the market.

Unfortunately, global validation by simulation is still a bottleneck in the design process. This is because designing such complex heterogeneous systems requires cooperation of several design groups.
with quite different backgrounds. Furthermore, these groups use frequently different specification languages and simulation tools.

A traditional approach used for design and validation of systems containing MEMS/MOEMS devices makes use of Hardware Description Languages. In this case, various teams working each one in a different domain create their models in a common HDL. Models are assembled and the global behaviour of the system is obtained by using a single simulation engine. This approach allows validation of relatively complex multi-domain systems but does not take full advantage of the experience of each team in using languages and simulation tools specifically designed for each particular domain.

A more efficient approach for global validation of a complex heterogeneous system is based on the joint simulation of the various subsystems by using simulators and abstraction levels appropriate to each component at its current level of refinement. This approach is called co-simulation and benefits of the expertise of each team in the use of specialized tools. Figure II-1.28 illustrates the concept of cosimulation where electronic, electromechanical and optical devices are simulated using different engines which are interconnected via a cosimulation backplane.

![Cosimulation Backplane](image)

**Figure II-1.28** Cosimulation of heterogeneous systems embedding MEMS/MOEMS devices

Our recent activities have been focalized on the cosimulation of a free-space optical cross-connect using electrostatic actuators, see Figure II-1.29. We have used SystemC as our simulation framework.

![Free-space optical cross-connect architecture](image)

**Figure II-1.29** Free-space optical cross-connect architecture

We have represented the OXC as a hierarchical network of modules, each one containing a description of its behaviour and a set of ports. Modules were interconnected through their ports via communication channels. The driving subsystem was specified in SystemC, the electromechanical actuators in Matlab, and the optical devices (mirrors, lens, sources and detectors) as C++ models. In order to simulate the heterogeneous specification of the OXC, the interfaces adapting the different
simulators have been generated. We have successfully applied the cosimulation approach to simulate a switch transition of this device.

II-1.8 Thermal test dies for package qualification

Members: Zs. BENEDEK\textsuperscript{1}, B. COURTOIS, G. FARKAS\textsuperscript{2}, S. MIR, B. CHARLOT, A. POPPE\textsuperscript{2}, M. RENČZ, V. SZEKELY, K. TORKI

Package thermal qualification is a key task in thermal engineering. Thermal test dies are typically used to perform this task. A test die is a chip that contains heating elements and temperature sensors. The heating elements serve to heat up the package under test. The sensors measure the temperature on different points of the chip surface, either for steady-state or transient qualification. From this data, the heat transfer properties of the package can be calculated (e.g., most typically, the thermal resistance of the package).

In the frame of the European project PROFIT, TIMA has partnered with the Technical University of Budapest and its spin-off company MicRed to develop new types of thermal test dies with increased on-chip functionality and easy control. Figure II-1.30 shows example thermal test dies fabricated. Most of the chip area is occupied by a central matrix of sensor and heating elements, respecting the JEDEC standard for thermal test dies. Around each CMOS frequency-output temperature sensor there is a heating element made of polysilicon resistors (Figure II-1.30 (a)). This chip design is of scalable size, showing in Figure II-1.30 (c) a 6x6 mm\textsuperscript{2} chip with a matrix of 91 sensors/heaters, and Figure II-1.30 (b) a 2x2 mm\textsuperscript{2} chip with a matrix of 9 sensors/heaters. As a great advantage, the chips are easily controlled digitally through a standard boundary scan path, for programming dissipation patterns and reading the sensor outputs. High precision static measurements and high resolution transient measurements can then be achieved without external tester equipment. High precision analog sensors are also included to keep compatibility with traditional thermal measurements.

![Figure II-1.30 Manufactured chips: (a) Temperature sensor surrounded by polysilicon dissipators, (b) thermal test die of 2x2 mm\textsuperscript{2} and 9 sensors/heaters, and (c) thermal test die of 6x6 mm\textsuperscript{2} and 81 sensors/heaters](image)

Figure II-1.31 shows results of steady state measurements made with the 9x9mm/81 sensors chip mounted on a PGA144 package. Figure II-1.31 (a) shows the dissipation pattern and images (b) and

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\textsuperscript{2} Micred, Hungary
(c) shows temperature map in 2D and 3D. The highest temperature is 35.32°C and the lowest is 30.03°C for a 20°C ambient temperature.

![2D and 3D Temperature map at the surface of the chip given by the 6x6mm/81 sensors chip, (a) shows the dissipation pattern](image)

**Figure II-1.31** 2D and 3D Temperature map at the surface of the chip given by the 6x6mm/81 sensors chip, (a) shows the dissipation pattern

### II-1.10 Self-testable microsystem electronic interfaces

*Members: S. MIR, C. DOMINGUES, R. EBRAHIM, I. RUFER*

This work developed in the frame of the MEDEA+ project TECHNODAT looks at on-chip test strategies for analogue and mixed-signal circuits and its application to electronic interfaces for acoustic sensors. We are designing a self-testable analogue and mixed-signal core used as a general electronic interface for acoustic sensors, in the frequency range from 10 Hz to 10 MHz, covering voice and ultrasound applications. Deep sub-micron technologies (0.18 μm CMOS and below) must be used. Testing deep sub-micron chips containing audio circuits is recognised as a major challenge if they also contain a large number of noisy digital circuits. Currently we have concentrated on on-chip test signal generation.

The test circuitry is based on loading a shift-register of a programmable length with a pre-defined digital signature (called seed). After loading a seed, the shift-register is looped (the output fed back to the input) and clocked at a given frequency (sampling frequency). The output of the register is then a bit-stream that after analogue filtering allows recovering a digitally encoded analogue test signal. The signal obtained depends on the seed, the length of the shift-register (that can vary between 100 and 200 bits) and the sampling frequency. The sampling frequency is obtained by dividing the on-chip clock. A test vector for on-chip generation of an analogue signal is 256 bits long, including the seed and other parameters required by the test circuitry to control the sampling frequency (division factor), the shift-register length and the analogue filters.

A CAD tool is under development for determining the test vector that is necessary to generate on-chip an analogue test signal. The tool takes as input a description of the wanted analogue signal and produces as output the digital test vector that must be loaded in the test circuitry, optimising the shift-register length and sampling frequency that allow obtaining a high quality analogue signal. The tool is fully integrated in the CADENCE environment and is user-friendly. The simulation process inherent to the tool operation is transparent to the user.
II-2 Concurrent Integrated Systems (CIS)

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L. FESQUET, J. FRAGOSO, B. GALILÉE, A. GUYOT, Y. MONNET  
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G. SICARD, A. SIRIANNI, K. SLIMANI

Research areas:

The CIS group research activities are focused on the development of new and effective solutions for designing complex integrated systems (SoCs). Using forthcoming technologies, the successful design of complete VLSI systems requires solving many different, but related, issues ranging from electrical behavior of devices, interconnects, analog/RF blocks, circuit and systems architecture. The CIS group research activities are particularly focused on investigating and evaluating the potentials of the asynchronous logic.

II-2.1 Introduction: asynchronous circuits and systems

The global synchronization strategy of synchronous circuits was introduced in the early 70s because, at that time, it was a satisfactory answer to design needs and technological potentials. This initial choice of an implementation strategy, drove and is still driving the design of algorithms/architectures, languages and CAD tools. Today, integration potentials of advanced technologies are going beyond design productivity, and one can wonder whether the synchronous circuit style is still relevant. Asynchronous circuits which were introduced in the mid 50s, receive now increasing interest. What significant benefits are they likely to offer? Can they contribute to improve design productivity in the future?

Our motivation is to answer these questions, investigating what impact asynchronous circuits may have on the design of integrated systems and how to take advantage of this circuit style at different levels: circuit level, architectural/algorithmic level, specification level, and system level? Because asynchronous circuits provide more flexible, robust and reliable synchronization and communication mechanisms, they give rise to alternative and innovative solutions that have to be analyzed and evaluated.

At the circuit level, asynchronous logic enables the design of delay insensitive circuits which do not require accurate and costly delay characterization. In fact delay insensitivity guarantees a correct functional behavior independently of the propagation delays in the basic components (gates, interconnects...). Delay insensitive asynchronous circuits are for example insensitive to some emerging problems like delay fault due to crosstalk. The delay insensitivity property makes asynchronous circuits very promising to explore and exploit advanced CMOS and future technologies.

Eliminating the global clock, which synchronizes all parts of circuit in synchronous logic, provides more flexibility to design system architectures. In fact, the control is naturally distributed rather than centralized. Hence, communication as well as synchronization through "rendezvous" for example, are easily implemented by a collection of independent and local finite state machines, which do not require to know the state of the whole system. Data to be computed by the system flow in the architecture as fast as they can according to resources’ availability and hardware

1 Collaboration with FranceTelecom R&D
implementation. The processing cost (in terms of delay and power consumption) is exactly the image of what is specified by the algorithm, given the chosen hardware implementation. It means that speed and power consumption may depend on the data processed. The data-flow behavior of asynchronous circuits, at any level of granularity, is the source of significant improvements in terms of speed/power optimizations and ease of design.

Today, one of the main challenges is the design of efficient and convenient CAD tools for asynchronous circuits. This is currently one of the priorities of our research work. We have adopted a CSP based language, called CHIP, as the specification language (introduced by Alain Martin - Caltech). The specification and development of a design framework for asynchronous/synchronous circuits is in progress. This work follows two main motivations: i) to provide the asynchronous circuit designers with a powerful execution/simulation framework, mixing high-level CHIP descriptions, HDL programs and gate level descriptions, ii) to give to synchronous designers familiar with existing HDL-based top-down design flows, the opportunity to include clock-less circuits in their designs. The main challenge is to efficiently synthesize behavioral descriptions written in CHIP into gates. One of our goals is to provide a synthesis tool that would target different styles of circuit, QDI and Micropipeline circuits, thus enabling designers to compare the merits of different approaches.

Finally, asynchronous circuits also bring flexibility at the system level. Complex, highly concurrent image processing applications naturally take advantage of the locality and modularity of clock-less circuits. Because they don’t need a global synchronization signal, modularity is a major property of asynchronous circuits which enables the design of complex integrated systems by simply assembling functional blocks. Design time is thus reduced and reusability increased. As an example, the design of locally-synchronous globally-asynchronous SoCs brings a solution to the problem of communications between distant parts using long interconnects. Without requiring drastic change in terms of tools and methodologies, synchronous parts of SoCs may be interconnected using advanced and robust asynchronous interfaces.

The potentials of asynchronous circuits are being investigated through the design of portable systems (from smart-card to multimedia terminal). There are three main properties of asynchronous circuits that can improve such systems and/or make their design easier: electromagnetic compatibility, low power and free power management, flexible interfacing capabilities. Interfacing digital asynchronous circuits with analog parts (RF front-end, sensors, actuators, etc.) is also a major field of interest. It is in fact essential if we expect to successfully design SoCs that may integrate various kinds of digital and analog parts.

II-2.2 Asynchronous Processors

II-2.2.a ASPRO Microprocessor
(collaboration with France Telecom R&D & STMicroelectronics)

![Figure II-2.1 The ASPRO microprocessor](Image)
We have designed a CMOS standard-cell Quasi-Delay-Insensitive (QDI) 16-bit asynchronous microprocessor using a 0.25 μm technology (see Figure II-2.1). ASPRO-216 has been developed for embedded applications. It can be customized both at the hardware and software levels to fit specific application requirements. It is a scalar processor which issues instructions in-order and completes their execution out-of-order. Its architecture extensively uses an overlapping pipelined execution scheme involving de-synchronized units. ASPRO owns four bi-directional serial links with 50 Mb/s throughput, two 16-bit parallel ports, 16 Kwords program memories on chip, and 64 Kbytes data memories on chip. ASPRO operates with a power supply between 0.8V and 2.5V. The performance of ASPRO-216 is 140 Mips, 0.5 Watt, at 2.5 Volts and 24 Mips, 27 mW, at 1V (see Table II-2.1 for a comparison with other asynchronous processors).

<table>
<thead>
<tr>
<th></th>
<th>mW</th>
<th>Mips</th>
<th>Supply (V)</th>
<th>mw/Mips</th>
<th>Technology</th>
<th>Circuit style</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aspro (2.5v)</td>
<td>500</td>
<td>140</td>
<td>2.5</td>
<td>3.6</td>
<td>0.25</td>
<td>QDI, std-cell</td>
</tr>
<tr>
<td>Aspro (1v)</td>
<td>27</td>
<td>24</td>
<td>1</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Caltech 1st</td>
<td>225</td>
<td>18</td>
<td>5</td>
<td>12.5</td>
<td>1.6</td>
<td>QDI, full custom</td>
</tr>
<tr>
<td>MiniMips (3.3v)</td>
<td>4000</td>
<td>170</td>
<td>3.3</td>
<td>23.5</td>
<td>0.6</td>
<td>QDI, full custom</td>
</tr>
<tr>
<td>MiniMips (1.6v)</td>
<td>220</td>
<td>60</td>
<td>1.6</td>
<td>3.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phillips 80c51</td>
<td>9</td>
<td>4</td>
<td>3.3</td>
<td>2.3</td>
<td>0.5</td>
<td>μ-pipeline, std-cell</td>
</tr>
<tr>
<td>Amulet2e</td>
<td>150</td>
<td>42</td>
<td>3.3</td>
<td>3.6</td>
<td>0.5</td>
<td>μ-pipeline, full custom</td>
</tr>
<tr>
<td>Titac2</td>
<td>2100</td>
<td>54</td>
<td>3.3</td>
<td>38.9</td>
<td>0.5</td>
<td>SDI, full custom</td>
</tr>
</tbody>
</table>

Table II-2.1 ASPRO compared to other asynchronous processors

The design flow we set-up to design ASPRO is described in Figure II-2.2. The specification language used is a CSP like language called CHP (from Caltech). The processor is first described by a high level sequential CHP program which is automatically translated into VHDL and validated by simulation. This program is then refined by process decomposition and transformed to get a parallel structural version.

![Figure II-2.2 Synoptic of the flow used to design ASPRO](image)

The synthesis phase is constrained by cycle time and latency specifications. When every part of the processor is available at the gate level, an optimization of the whole architecture is performed to get maximum performance (pipeline balancing, slack matching) according to the pipeline depths and latencies of each block (see II.2.1.d for details on the design flows and associated tools).

Software development tools, C compiler, assembler, linker and simulator are available for the development of applications using the ASPRO processor. We have also developed a motherboard to demonstrate the capabilities of the microprocessor. The board includes an ASPRO, flash memories for the boot, reset / interrupt logic, four communication links and a parallel interface to connect peripheral boards. Three peripheral boards have been designed, one is based on LED and Switches (see Figure II-2.3), another one includes an RF interface and the last one is a digital camera.
Experiments performed with the motherboard shows that the processor is running correctly down to 0.65 volt (nominal supply voltage is 2.5 Volts).

Figure II-2.3 The ASPRO motherboard and a peripheral daughter board

An example of a system built using the boards we have designed is presented in Figure II-2.4. This is a multiprocessor system based on two ASPRO processors, a camera and an RF interface. The application consists in capturing an image, processing it and transmitting the result through the radiofrequency. This prototype enables us to carry on experimentation on multiprocessor systems, low power Operating System implementing a dynamic voltage scheduling strategy.

Figure II-2.4 Multiprocessor system for image processing with wireless communication

II-2.2.b MICA micro-controller
(collaboration with France Telecom R&D & STMicroelectronics)

Figure II-2.5 The MICA micro-controller

MICA is a QDI asynchronous 8-bit micro-controller CISC machine, based on a dedicated "luxurious" micro-architecture (see Figure II-2.5). In order to facilitate the design of a "C"
compiler and also to limit memory accesses, we decided to integrate two different register-files: eight 8-bit registers are devoted to data, and eight 16-bit registers are devoted to pointers (including the program counter and the stack pointer). Specific arithmetic units are associated with each register file enabling concurrent computations of data and addresses. A dedicated unit is managing the standard status bits Z, N, V and C. A peripheral unit is also included, supporting six 8-bit parallel ports (1 input, 4 outputs and 1 bi-directional used to control external flash memories and the synchronous/asynchronous interface) and four serial links (using a two-phase delay insensitive protocol compatible with our high performance RISC asynchronous ASPro processor – described above –). Moreover, the micro-controller integrates 16 Kbytes RAM and 2 Kbytes ROM. The latter includes a Built-In-Self-Test which is executed at reset according to the boot mode selected (eight modes are available). It is a 350 assembly instruction routine which performs a complete stuck-at-fault test, thanks to the QDI asynchronous logic. The BIST routine computes a signature written on the fly, on one of the parallel port to report on self-test progress.

- Instruction set

The eight 8-bit data registers are named r0 to r7, and the eight 16-bit index registers i0 to i7, where i6 and i7 are the stack-pointer and the program-counter respectively. The controller implements the common arithmetic and logic instructions. All instructions are encoded within one word (16 bits). Four basic addressing modes are available (immediate, register, indexed with displacement, indexed post-incremented or pre-decremented) which can be used in conjunction with data or index register operands. Lastly, the controller implements a maskable interrupt mechanism and a “wait for interrupt” instruction (WfI). Table II.2.2 summarizes the instruction set, note the "cp" (Cp) and the "Puch&Load" (Pl) instructions. A complete software development suite of tools is currently under development including a "C" compiler, an assembler, a linker and a simulator.

<table>
<thead>
<tr>
<th>Arithmetic/logic</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add, Addc, Sub, Sabb, Inc, Dec, Neg</td>
<td></td>
</tr>
<tr>
<td>And, Or, Xor, Not, Cbn (clear bit n), Sbn (set bit n), Tbn (test bit n)</td>
<td></td>
</tr>
<tr>
<td>Ror, Ror, Rel, Rec (rotate without and with carry)</td>
<td></td>
</tr>
<tr>
<td>Shr, Shr, Shr (shift left, shift right unsigned and signed)</td>
<td></td>
</tr>
<tr>
<td>Index</td>
<td></td>
</tr>
<tr>
<td>Addx, Subx</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Load/Store</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ld, Ldp, Stp (load/store peripheral), St</td>
<td></td>
</tr>
<tr>
<td>Cp (copy from memory to memory is available)</td>
<td></td>
</tr>
<tr>
<td>Pl (push &amp; load)</td>
<td></td>
</tr>
<tr>
<td>Psh, Psar (push, push status register), Pop</td>
<td></td>
</tr>
<tr>
<td>Index</td>
<td></td>
</tr>
<tr>
<td>Psx, Popx</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Control flow</th>
<th>Rti, Rtu, Jmp, Jsr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bcc, Bcrcc (cc = a,aq,ne,cc,cs,c,le,lt,lt,ge,gt,gle,ge,vc,vs)</td>
<td></td>
</tr>
</tbody>
</table>

| Misc | Nop, WfI, Bint, Dtu (enable and disable interrupt) |

Table II.2.2 The MICA microprocessor Instruction set

- Architecture design

The micro-controller core is designed using the so-called Quasi Delay Insensitive (QDI) logic. A four-phase protocol is used in conjunction with an n-rail encoding. This chip has been a vector for developing new skills in the design of standard-cell based QDI asynchronous circuits. The design of
MICA was focused on two correlated concerns: designing distributed asynchronous finite state machine and designing for low power.

In order to reduce the power consumption of the micro-controller we have worked on minimizing the number and the energy-cost of communication actions occurring during the execution of each instruction, and minimizing the number of sequential steps to perform each instruction. In other words, instead of designing the architecture around a big central sequencer, we have tried to distribute the sequencing implementation all over the architecture as much as possible. The asynchronous logic is particularly well suited to satisfy such a design approach since by nature the sequencing of an asynchronous circuit is performed by multiple local sequencers implementing handshaking communications and local treatments.

Thus, the architecture of MICA has been designed as a distributed system, each part providing specific services. For example, the two register-files, the status register and the memory integrate local units which manage the memory resources. These modules implement functions such as "read", "write", "read then write back" or even more complex function like: read a byte, increment/decrement the pointer/address and read the corresponding byte (Cp and Pl instructions for example use these features). Adopting such an approach significantly simplifies the design of the main sequencer of a CISC microprocessor like MICA. It then minimizes the power consumed by the main sequencer, the consumption associated with each instruction being the direct image of its complexity. In fact, complex instruction implementation does not penalize simple instruction implementation at the main sequencer level. Moreover, such a distributed approach minimizes the power consumed by communications since the minimum number of transactions occurs through busses (memory accesses for example).

Because of the low-power constraint and because computational power was not a priority for the targeted applications, a minimum number of pipeline stage was introduced. This does not prevent parallel execution of instruction sub-parts, but simply means that parallel execution of instructions is not supported. In some cases however, subsequent instructions may partially overlap.

Finally, at the signal level, communication channels are using a low power data encoding. Instead of using dual-rail coding, we have implemented N-rail coding (also called "One Hot"), i.e. one out of the N wires is active during a transaction (instead of one out of two with dual-rail). The different parts of the architecture are all controlled by the main sequencer through channels using 5-rail to 12-rail data encoding which minimizes the number of transitions per communication action, and hence minimizes the dynamic power consumption. The data paths (8-bit and 16-bit) are entirely designed with 4-rail encoded data, requiring radix-4 logic/arithmetic processing units. The register files are also designed with 4-rail encoded data. Instead of bit-registers they are built of digit-registers, each digit representing 4 values.

- **Micro-controller performance**

A test chip has been designed, fabricated and tested. The micro-controller has been easily tested thanks to the BIST, and was **fully functional at first silicon** between 3 Volts down to 0.8 Volt (2.5 Volts is the nominal voltage of the .25µm CMOS technology used). **Table II.2.3** gives the Mips (mean number of instructions executed per second when running the BIST program). Power and Mips/watt figures at different voltages (based on the total current consumed by the core, the memory and the pads). It is noticeable that the chip only consumes 800 µW at 1 volt, still delivering a computational power of 4.3 MIPS. At 0.8 volt, the chip consumes less than 400 µW.

<table>
<thead>
<tr>
<th>Supply(V)</th>
<th>Mips</th>
<th>Current (mA)</th>
<th>Power(mW)</th>
<th>Mips/Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,0</td>
<td>4.3</td>
<td>0,8</td>
<td>0,8</td>
<td>5503,6</td>
</tr>
<tr>
<td>1,5</td>
<td>11,9</td>
<td>3,1</td>
<td>4,7</td>
<td>2560,2</td>
</tr>
<tr>
<td>2,0</td>
<td>18,6</td>
<td>6,7</td>
<td>13,3</td>
<td>1396,0</td>
</tr>
<tr>
<td>2,5</td>
<td>23,8</td>
<td>11,2</td>
<td>28,0</td>
<td>850,3</td>
</tr>
</tbody>
</table>

**Table II.2.3** MICA measured performances
We have developed a motherboard to demonstrate the capabilities of the MICA microprocessor. The board includes a MICA processor, a flash memory for the boot (and also programmable), reset/interrupt logic, four communication links and a peripheral interface. The same peripheral board developed for the ASPRO processor can be used. This system enabled us to show that the processor is running correctly down-to 0.65 volt (see Figure II-2.6).

![Figure II-2.6 The MICA motherboard](image)

II-2.3 Secure circuit design and smart-cards

II-2.3.a Integrated system for contact less smart-cards

(collaboration with France Telecom R&D & STMicroelectronics)

We have designed MICABI a Contactless Smart-Card Chip which integrates an on-chip coil connected to a power reception system and an emitter/receiver module compatible with the ISO 14443 standard, together with the MICA 8-bit microcontroller described above (see Figure II-2.7). Beyond the contactless smart-card application field, this new chip demonstrates that System on Chip integrating power reception and management, radio-frequency communication and signal processing are feasible. The chip, fabricated in a CMOS 6 metal layers 0.25 μm technology from STMicroelectronics, associates analog/digital parts as well as synchronous/asynchronous logic.

Power reception and data transmission are performed using a modulated magnetic field emitted by the reader. The antenna was integrated on silicon (on-chip coil), using 5 metal layers, to suppress interconnect issues and decrease card cost. Computation power in the card-chip is provided by the MICA quasi delay insensitive microcontroller in order to limit power consumption, noise, and sensitivity to supply voltage variations. The 8-bit microcontroller core integrates a 32 Kbytes RAM and a 2 Kbytes ROM containing a BIST (Built In Self Test) and a boot program.

The power-supply reception system is designed in order to allow operation of the microcontroller while in reception or in emission. A voltage regulation system decouples the microcontroller voltage supply and the RF front end voltage supply which transmits data. This regulation ensures correct operation of the RF front-end while the micro-controller is in operation at its own speed according to its data treatment and received current. In normal mode of operation its supply-voltage is regulated to 2 volts. At this voltage level the microcontroller delivers 18.6 Mips on average and consumes about 13.3 mW. At 1 volt, the core still delivers 4.3 Mips and consumes only 800 μW.
A dedicated interface between the asynchronous processor core and the ISO 14443 compliant analog emitter/receiver module was designed. This interface implements a handshake-based protocol which ensures minimum power consumption and noise when the chip is receiving or emitting data.

![Image of the contactless smartcard MICABI and its reader](image)

Figure II-2.7 The contactless smartcard MICABI and its reader

II-2.3.b Secure circuit design

The goal of this research is to propose new design methods and tools to improve circuit resistance against non-invasive attacks such as timing attacks, DPA (Differential Power Analysis), DEMA (Differential Electromagnetic Analysis) and DFA (Differential Fault Analysis). Today, cryptography and cryptanalysis are both evolving very rapidly opposing hackers and secure systems providers. The smart card market is the primary concerned, but e-commerce, e-banking and data ciphering in general are all sensitive to attacks. Searching for new counter measures against such attacks, jointly at the software and the hardware levels, is becoming a major issue.

DPA attacks consist in measuring current consumption or electromagnetic emission of a running circuit in order to extract secret or private information. Glitch attacks are methods to disrupt circuit execution by applying sharp signal changes to the clock signals or to the power supply lines.

The asynchronous technology provides a means for designing DPA resistant circuits. In fact, it can be shown that quasi delay insensitive circuits can be designed so that the execution time and power consumption do not vary with the data processed. Thus, the electric and electromagnetic signatures of a running circuit are data independent making DPA type attacks inefficient.

In this field, the challenge is to get the best of asynchronous circuits to improve security at the smallest cost as possible. Today, known solutions are rather costly in terms of area. Current works carried out in the CIS group are focused on low-complexity secure asynchronous circuits.
Glitch attacks in particular, and DFA (Differential Fault Analysis) in general, are also important issues that we are currently investigating theoretically.

On the practical side, we have recently performed DPA on the MICA microprocessor. Results obtained when performing power analysis on the MICA 8-bit QDI asynchronous micro-controller reveal that the processor resists to standard DPA attacks. These results practically demonstrate the relevancy of using the asynchronous technology to design new secure circuits for smartcards and cryptographic applications (Figure II-2.8).

![Photography of the hardware system used to perform DPA measurements. The curves were obtained averaging the current consumed by the processor over 10000 runs of two different programs: (load FF, load 00, FF xor 00) and (load 00, load 00, 00 xor 00). The current consumption remains the same, and is then not data dependent.](image)

**Figure II-2.8**

**II-2.4 Analog to digital conversion based on irregular sampling**

This research work is focused on the design of new architectures of Analog-to-Digital Converter (ADC) for low-power applications. The basic idea relies on a tracking strategy not involving any clock. The implementation is based on an asynchronous design only using local control signals. Samples conversion is only triggered by the analog input signal amplitude variations, hence an irregular sampling of it.

Classical Analog-to-Digital Converter (ADC) architectures are synchronous i.e. driven by a global clock, and belong to one of these two families: the Nyquist rate converters, or the over-sampled one. The architecture choice and circuit design depend on the characteristics to privilege: resolution, speed, area, power consumption, ... signal-to-noise ratio (SNR). Such as any electronic circuit, ADC design follows the current trend that is to reduce power consumption, especially when it is used in embedded systems or SoC's (System on Chip) powered by batteries or remotely powered.

Most of the systems using ADC bring signals with interesting properties into operation, but common synchronous signal processing architectures do not take advantage of them. Actually, these signals are almost constant but may vary a lot during brief moments, like for temperature and pressure sensors, electro-cardiograms and speech signals... In this way, classical synchronous converting systems are highly constrained, due to the Shannon theory, which is to ensure for the sampling frequency to be at least twice the input signal frequency bandwidth. Therefore, in the time domain, this condition can be translated as a wide number of useless samples: as soon as the input signal is constant during a time superior to the sampling period. This effect implies a useless
increase of activity of the circuit compared to the supplied output digital information relevance, and so a useless increase of the power dissipation.

It is well known that asynchronous designs exhibit interesting properties such as low energy dissipation, immunity to metastable behavior, low electromagnetic interference generation. The new concept of conversion investigated in this work consists in building a completely asynchronous system, with an irregular sampling of the analog signal to process. The converter supplies a digital sample only if a perceptible variation of amplitude is detected in the analog input signal. This converter is not controlled by any global clock, but only by the analog input signal. It is a tracking system, enslaved on the signal.

A 6-bit resolution prototype was designed using a 0.18-μm, 1.8-V standard CMOS technology from ST-Microelectronics. Electrical simulations show that the Asynchronous Converter has an average power dissipation of only 1.5mW with a sample conversion time of 37.9ns, and a significant noise reduction is achieved. System level simulations show that significant power reduction can be achieved with this kind of ADC.

Clearly, benefits of such an asynchronous ADC can be exploited for the design of low-power, low-noise SoCs integrating analog and digital parts. This approach definitively opens new perspectives in the field of smart-sensors and smart-devices design. Jointly, it implies to develop new skills in the irregular sampling practical and theoretical domains.

II-2.5 The TAST design environment

TAST stands for TIMA Asynchronous digital circuit Synthesis Tools. This is a design environment which is gathering researches carried out in the group on asynchronous circuits design methods and associated CAD tools.

It consists of a compiler/synthesizer with the capability of targeting several outputs from a high level description language. We have developed a proprietary high level description language derived from CHP (Communicating Hardware Processes introduced by Caltech) with specific features to cope with communication protocols, data encoding, arbitrary precision arithmetic, non-determinist data flow, hierarchy, project management, and traceability. All this features make our CHP a very practical system description language to develop with. It also makes scalability and modularity easy to manage.

The flow (Figure II-2.9) is organized around Petri Nets (PNs) associated to Data Flow Graphs (DFGs). Such a model has been used for years to model synchronous circuits and systems and finds a particularly adequate application in the field of asynchronous digital circuits and systems design. Asynchronous digital circuit synthesis is based upon the DTL (Data Transfer Logic) specification we have defined. It provides a set of rules to guarantee that PN-DFG graphs are synthesizable into asynchronous digital circuits.

The TAST engine compiles three kinds of targets from communicating processes (CHP) : Behavioral VHDL simulation models, QDI (Quasi Delay Insensitive) style VHDL gate level asynchronous circuits, and Micropipeline style VHDL gate level asynchronous circuits.

Current research is carried out in the CIS group to improve TAST in the following areas :
- get better performance of synthesized circuits in terms of area, speed and power,
- security driven synthesis,
- EMI (Electro Magnetic Interference) driven synthesis,
- generation of a C self executable simulation model to address high speed simulation,
- prototyping on standard FPGAs,
- formal verification of models and circuits in collaboration with the VDS group.
II-2.6 Arithmetic operators

II-2.6.a Automatic generation of arithmetic operators

The CIS group participates in the development of web-based support for VLSI design training. In this framework, it is currently developing exercises on arithmetic operator synthesis and characterisation. They are aimed to be a self-training lecture complement. Table II-2.4 lists available exercises, implemented in JavaScript and Java. The exercises fall in 4 categories: synthesis, simulation, diagram (plot) and operation part synthesis.

| Activity in carry propagate adders | Simulation |
| Carry propagation free addition (Carry Save) | Simulation |
| Brent-Kung carry look-ahead tree generation | Synthesis |
| Serial multiplication (add/sub and shift) | Simulation |
| Generation of multipliers partial products | Synthesis |
| Generation of multiplier reduction tree | Synthesis |
| Generation of modulo reduction (for self-checking operators) | Synthesis |
| Layout of "Robertson's diagram" for division | Diagram |
| Datapath of a sequential divider | Operation part |
| Sequential division (add/sub and shift) | Simulation |
| Datapath of a square root extractor | Operation part |
| Sequential square root extraction (add/sub and shift) | Simulation |
| Floating point add/subtract/multiply/divide | Simulation |
| Datapath of a sequential logarithm (Cordic) | Operation part |
| Sequential logarithm and exponential (add/sub and shift) | Simulation |
| Layout of the convergence domain for Sine/Cosine (Cordic) | Diagram |
| Sequential sine and cosine (add/sub and shift) | Simulation |

Table II-2.4 List of available exercises
Figure II-2.10 shows a typical synthesis. The result in the right window can be edited, verified and simulated.

Figure II-2.10  Example: synthesis of a carry propagation tree

II-2.6.b Asynchronous arithmetic operators

Skills developed in automatic generation and design of synchronous arithmetic operators are naturally exploited to conduct research in the domain of asynchronous arithmetic operators. The goal of this work is to provide the TAST synthesis tool with powerful adder and multiplier generators. Therefore, based on our knowledge on asynchronous circuit, arithmetic operators are revisited for the design of compact, fast and low-power asynchronous structures.
II-3 Reliable Integrated Systems (RIS)

Group Leaders: M. NICOLAIDIS / B. COURTOIS
(e-mail: Michael.Nicolaidis@imag.fr, Bernard.Courtois@imag.fr)


Research areas:

This group investigates:

. Off-Line Testing techniques such as BIST, BISR, Iddq Testing, Synthesis for Testability, Analog and Mixed Signal Test.
. Synthesis for dependability and automatic modification of high-level descriptions for on-line test or fault tolerance.
. Predictive analysis of the erroneous behaviours of complex VLSI circuits; techniques and tools for fault injection in VHDL descriptions or FPGA implementations.
. Logic implementations in nanoelectronics

Contracts:

MIRFAS, FRACTURE, ERC (ST Microelectronics)
Start-up company created: iROC

II-3.1 Self-checking circuits

Members: I. ALZAHER-NOUFAL, M. NICOLAIDIS

Periodic off-line testing of VLSI circuits may be used to ensure hardware failure detection. However, errors produced by hard faults will remain undetected until the test phase. Also, off-line testing is not effective against transient faults. On the other hand, concurrent error detection techniques are able to detect errors due to both hard faults and transient faults as and when they occur. Concurrent error detection based on software encoding techniques needs special software development and will significantly decrease the system speed. Alternatively, hardware encoding based on special-designed self-checking circuits may be used. One advantage of self-checking circuits is that they may be designed to cover well known models of hardware faults.

Recent investigations in the group led to the development of low hardware cost TSC data paths. These developments include the carry checking / parity prediction scheme for adders, ALUs, and parity prediction for shifters and barrel shifters. Other developments concern the design of fault secure parity prediction multipliers and dividers. A comprehensive framework of CAD tools for self-checking data path design is developed. It includes various macroblock generators that generate self-checking adders and ALUs based on the above solutions. They support a vast variety of ripple-carry, skip-carry, carry lookahead and conditional sum adders and ALUs, various single-position and multiple-position shifters, regular array dividers, regular array multipliers, and fast multipliers using Wallace trees and fast carry propagate adders, with non-recoded or recoded operands (Booth).
II-3.2 Fail-safe systems

Members: S. SALEH, N. ZAIDAN, M. NICOLAIDIS

Fail-safe systems are implemented using a processing part checked using some kind of hardware or software redundancy and by a fail-safe interface which transforms the outputs of the processing part into fail-safe signals (i.e. signals which are either correct or safe). Conventionally, the fail-safe interface is implemented using specific fail-safe discrete components. Such implementations have high cost and are very cumbersome. This work presents VLSI implementable fail-safe interfaces for self-checking systems using duplication or other error-detecting code techniques, and for fault tolerant systems based on triplication. With respect to a scheme that we have proposed in the past, the new scheme uses concurrent checking techniques instead of periodic testing based on BIST implementation. We are presently implementing a fail-safe interface using a smart power technology. Thus, the delivered signals will be fail-safe and at the same time they will provide the power required to drive the actuators used in the French railways.

II-3.3 Perturbation detection/tolerance using time redundancy

Members: L. ANGHELI, D. ALEXANDRESCU, M. NICOLAIDIS

This project considers the design of perturbation detection/tolerance for combinational circuits in nanometer technologies. Since VLSI circuits destined to commodity applications can not afford traditional high-cost solutions, the project investigate new low-cost approaches. We have developed several low cost techniques that exploit the temporary nature of transient faults and achieve soft-error tolerance or detection by means of time redundancy, or by combining time and space redundancy.

II-3.4 Automatic modification of high-level descriptions for dependability

Members: R. LEVEUGLE, R. CERCUEIL

The goal of this project is to develop a tool allowing a designer to easily insert, in a digital circuit, specific devices for on-line detection or tolerance of errors provoked by SEUs. The automated approaches must be flexible enough to provide answers for various application constraints (in terms of area, speed, power consumption and error coverage). Several approaches are previously proposed to be applied at the gate level or during the synthesis process have been revisited to evaluate the feasibility of their implementation earlier in the design flow. The tool provided to automate this implementation had to be compatible with industrial design flows based on commercial synthesis and simulation tools; we therefore focused on a stand-alone tool able to modify synthesizable VHDL descriptions. The modified description had of course to be optimised for an efficient synthesis.

In 2001, a prototype tool has been developed and proved the feasibility of the concept. Two types of modifications were automated. The first one aims at tolerating SEUs in the state registers and in the combinatorial logic computing the next state in finite state machines. The second approach is based on control flow checking and performs the on-line monitoring of the internal operation sequencing. The tool developed allows a designer to automatically modify the VHDL description of either a finite state machine or a circuit described as a RT-Level control flowchart. The efficiency of the approach was demonstrated by comparison with previous results obtained when implementing the same techniques at a lower level, i.e. during the synthesis process using a specific synthesis tool. Furthermore, modifying directly the high-level description allows an earlier validation of the system response in presence of faults and provides extra benefits in terms of re-usability.
II-3.5 *Synthesis of on-line testable systems*

 Members: M. A. NAAL, E. SIMEU

VLSI technology has evolved to a level where large systems, previously implemented as printed circuit boards with discrete components, are integrated into a single IC. High-level synthesis consists in generating an RTL-level description of a digital system from its behavioral specification while satisfying a set of designer specified constraints. Control scheduling, functional units and register allocation and operation binding are the three major tasks executed in synthesis procedure with the objective of optimization of both area and speed constraints. Traditionally, on-line and off-line testability considerations are not in the synthesis level, the additional test dedicated circuit is defined and inserted later in RTL level. This would likely lead to a hard to test design. This cost may become quite higher if the test circuitry is inserted at the later stages of the design process. To avoid this difficulty, testability considerations have to be incorporated into earlier design stage, during the high-level synthesis process. In our approach, a high-level synthesis strategy is proposed for the design of on-line self-checking devices. At the present phase, the project is concentrated on the data path design. The nominal data path is first scheduled and allocated by using any scheduling-and-allocation algorithm (the designer can choose the preferred one, without any restriction). The reference nominal architecture is assumed identified and constructed using any scheduling and allocation algorithm. As well as the related schedule and allocation, the resulting nominal architecture is frozen and must not be changed during the checker construction procedure.

In the non-concurrent approach, the test stimuli are periodically applied during the functional unit’s idle time. This approach is very efficient when the operational time (time required to calculate the output) is small compared to the system’s sample time.

The semi-concurrent approach is based on a maximum reuse of the resources available for the nominal computation to minimize the requirement of additional functional units. A dual architecture, solution to the nominal system behavioral specification is implemented for on-line testing purpose, using the nominal functional units, without requiring additional hardware resources. This minimizes the need for introducing redundant resources to implement the checking data path. The nominal data path is extended to include on-line testing features. The principle of our approach can be incorporated in various scheduling and allocation algorithm.

II-3.6 *Model-based numerical redundancy generation for concurrent checking*

 Members: A. ABDELHAY, E. SIMEU

The basic principle of the model-based detection approach is to build a concurrent error indication signal using inherent analytical (rather than physical) redundancy, contained in the static and dynamic relationships among the system input and measured signals. In other words, residuals are generated using the available mathematical knowledge on the monitored system. The residuals express the deviation of the input and available measurements provided by the actual system with respect to the system nominal model. This deviation is close to zero in normal operation, different from zero in the faulty situation. According to the size and the system environment, two main strategies of residual generation are considered: hardware and software. In the hardware approach adding dedicated circuitry for concurrent error detection performs residual generation. This strategy allows for parallelism of detection tasks. Every critical element in a large plant may provide the requested detailed information on its current health status to the plant supervisor. For more complex systems including intelligent module, algorithm-based techniques are suggested and may be implemented without additional hardware. In accordance with the kind of quantity used for analytical model-based residual generation, the wide variety of possible methods can however brought down to few basic concepts:

Methods using non measurable state variable $x(t)$, methods using non measurable systems parameters $Q$, and the methods using non measurable characteristic quantity $n(u(t), x(t), Q)$. 

II-3.7 On-line testing of analog circuits

Members: I. RAYANE, E. SIMEU

In contrast to the previous project using algorithm-based fault tolerance, the error indication signal generator is directly hard-wired into the system using additional detection circuitry. Residuals are generated on-line by means of dedicated additional hardware into the system data flow graph. Using the nominal state model of linear analog systems, checksum codes have recently been proposed in the literature, as a mean for concurrent error detection in a particular class of linear analog systems: state variable systems. In such systems, the state variables are assumed to be accessible. This hypothesis only recovers a particular class of linear systems since, for the majority of real systems, the state variables are not accessible. We suggest a technique of redundancy equation generation based on the replacement of the unknown state variables by measured output signals. Further to the classical projection on the parity space, we perform an original elimination of unknown based on the analysis of the Kroneker invariant for available nodes and aggregation of equations. In our approach redundant hardware is inserted in the circuit data flow graph. The goal concurrent checking is extended to a larger class of linear analog systems than in previous methods while the hardware cost remains comparable. This extension requires the use of a special modeling of linear analog circuit. Contrary to the classical input/output modeling generally used for functional output simulation, the extended model needed for concurrent fault detection must also give an estimation of the signal on any circuit internal node, a model for unknown inputs or noise effects and a model for fault effects.

From the classical representation tools, we propose a symbolic calculation of an extended state variable model for any linear analog system. An algorithm providing this extended from a netlist description, is developed and implemented.

II-3.8 On line current monitoring

Members: L. ANGHEL, S. SALEH, M. NICOLAIDIS

Because current monitoring can cover faults creating undetermined levels and thus may escape detection by logic monitoring techniques, the use of Built-In Current Sensors (BICS) for static measurements is of high interest. The current sensors have to be faster, accurate and with a small impact on system performances.

II-3.9 Off line testing techniques

Members: N. ACHOURI, S. BOUTOBOZA, M. A. NAAL, M. NICOLAIDIS

Techniques destined to fabrication test are addressed here. Progress in technological scaling allows the integration into a single chip of hundreds of millions of transistors, moving quickly to the multi-billion transistor capacities. The integration of complex systems into a single chip, that may include heterogeneous parts such as logic, SRAM, DRAM, non-volatile memories, analog and even micromechanical and optical parts, is becoming a reality. Achieving acceptable reliability levels for these complex products is one of the most critical issues that need to be faced. Testability is therefore a key factor that could limit these trends if not addressed adequately. At these levels of complexity external testing is becoming unfeasible due to ATPG limitations (reduced controllability/observability due to rapidly increasing #devices/pin and sequential depth). At the same time, the scan approach is loosing interest due to the increasing length of scan chains (and thus test length), and low test application speed. At-speed test is a major limitation at a context where increasing clock frequencies (moving quickly to the multi-GHz domain), are making timing faults predominant. Automatic Test Environment (ATE) is another important limitation, since, although its very high cost, it does not offer the memory capacities/depth and test application speed, required for
testing nowadays ICs (development and production cycles are constraining ATF to use two-generation old IC technologies). In addition, several testers must be used to cope with the heterogeneous parts integrated into a single chip, increasing the test cost drastically. Under these constraints, the only realistic issue is to extend the BIST practice beyond memory testing. This requires new developments on logic BIST for increasing fault coverage while containing hardware cost, and extension of BIST approaches to the analog and eventually micromechanical domains.

II-3.10 **BIST and BISR for memories**

*Members: S. BOUTOBZA, N. ACHOURI, M. NICOLAIDIS*

Large static and dynamic RAM arrays are embedded in modern ICs. They often represent the largest part of the chip area. Since, in addition, memories are very dense they include the largest part of transistors of the chip. Because they are designed to be as tight on the technology as is permitted by the physical limits of the technology they are more susceptible to failures than standard logic. Memories therefore will represent the larger amount of defects in such chips. Thus, achieving low defect level in memory parts is essential for achieving low defect level for the whole chip. BIST solutions and tools able to uncover the real defects corresponding to the given memory design and fabrication process is of high importance. Memory BIST synthesis tools targeting this problem are considered in this project. These tools will address both standard memory BIST and transparent memory BIST. This last is of high importance, since it preserves the memory contents (thus allowing periodic testing in the field), and increases coverage of unmodelled faults.

At the same time, as large memory arrays will concentrate the majority of the defects of the chip, defective memory blocks will affect chip yield dramatically. Built-In Self-Repair hardware is necessary to obtain acceptable levels of manufacturing yield, or increased product life through self-repair in the field. One of the aspects of this project concerns the development of solutions and tools for low cost/high self-repair capabilities Built-In Self-Repair hardware.

II-3.11 **Signature analysis and diagnosis for mixed signal systems**

*Members: E. SIMEU*

Due to advances in semiconductor electronics, complex analog circuits are being designed. Analog designers are faced with difficult test problems for the following reasons. The analog and mixed-signal circuits have not been as well researched from a VLSI testing perspective as digital circuits. Contrary to the digital circuits that have a deterministic behavior, analog signals are inherently imprecise. Hence, the signature analysis problem is considerably more complex more for mixed signal circuit. Further the deterministic digital signature analysis schemes can not be directly used because of the inherent imprecision of analog signals. A deterministic digital signature analysis scheme can result in an incorrect signature for a perfectly valid analog signal. The purpose of the project is to present a scheme that reduces the above problems by the use of a signature analyzer that generates appropriate signatures. The strivings are focus to a scheme associating a delta-sigma modulator to signal cleaner. The cleaner aims to relieve the sampled signal of its imprecise part before the delta-sigma oscillator is used to generate a binary sequence signature.

II-3.12 **Predictive analysis of the erroneous behaviours of complex VLSI circuits and fault injections**

*Members: R. LEVEUGLE, K. HADJIAT, L. ANTONI*

Complex integrated circuits are today used in almost all application areas, including critical ones. Furthermore, the probability of faults (and especially transient faults) is rapidly increasing with the
advances of the manufacturing processes; these faults are more and more critical even in consumer applications (e.g. SEUs resulting in bit-flips and disturbing the circuit operation even at the sea level). Designers must thus take care of the fault consequences in an increasing number of cases. Classical fault injection techniques, allowing to study the consequences of faults once a circuit prototype has been manufactured, are not an answer because they cannot cope with the decreasing time-to-market constraints. Analysing the behaviour of a circuit when faults occur will therefore become a major concern at the different steps in a design flow, and not only after the circuit is manufactured. Such an analysis will be required to:

- identify unacceptable error propagation paths and unacceptable failure modes, and then guide design modifications,
- validate the efficiency of fault detection and/or fault tolerance integrated mechanisms,
- quantify the probability of the remaining failure modes for a given workload,
- prepare documentation for the circuit and/or reusable blocks (IPs).

To provide efficient support to the designers, the analysis must be possible very early in the design cycle. It should therefore be performed on high-level descriptions of the circuit. Then, the analysis must be refined along with the refinement of the circuit description during the different design steps, down to the gate-level implementation.

The goals of the project are:

- to develop a CAD environment, compatible with up-to-date design flows, helping the designer to analyse the behaviour of a digital circuit when faults occur. The environment can cope with different levels of descriptions of the circuit. The consequences of the faults are assessed qualitatively and quantitatively by generating a graph similar to a Markov chain and showing the error propagation paths, the erroneous configurations reached for a given workload and the probability of each propagation.

- to propose and automate fault injection techniques for circuits described in high-level description languages. The first approach studied consists in modifying an initial VHDL description so that faults can be injected on a set of target nodes. This includes the insertion of saboteurs and the generation of mutants. Mutants are currently the main focus because saboteurs cannot help in injecting faults such as SEUs in high-level descriptions. The generation of mutants is performed taking into account synthesis constraints, so that the injection mechanisms are compatible with both simulation-based and emulation-based experiments. Emulation has two advantages over simulation: a drastically reduced time for running the injection campaign and the possibility to analyse the faulty behaviours taking into account real-time system interactions (in-system emulation). In the case of emulation-based experiments, an alternative approach is also studied. It consists in injecting the faults directly in the hardware prototype by local reconfiguration of the FPGA. In that case, the initial circuit description is not modified but the faults are injected by manipulations in the bit-stream used to implement the circuit onto the emulator.

Tools had been developed in 2000 to automate the behaviour analysis (result analysis, generation of the graph, ...). A tool had also been developed to generate mutants allowing to inject erroneous transitions in finite state machines or RT-level control flowcharts. Such erroneous transitions can model the consequences of SEUs in the state registers, and can be injected before the state assignment is performed by the synthesis tool, thus very early in the design cycle. Several types of VHDL modifications had been implemented and compared, demonstrating that some approaches are noticeably more efficient than others when emulation is to be considered. The development of the CAD environment continued in 2001 and some effort was in particular devoted to the user interface. The generation of mutants allowing the injection of SEUs in all memory points in the circuit is still on-going. This generation is applied to high-level descriptions, before any synthesis is done, by identifying the locations in which flip-flops or latches will be required. Another part of the work in 2001 aimed at accelerating the simulation-based experiments, while maintaining the use of
a commercially available simulator. The idea was to store some simulation states during the reference fault-free simulation in order to shorten the simulations with injected faults. It appears that this approach is very memory consuming and does not provide, in many cases, noticeable time savings. The conclusion might be different in the case of modifications directly inserted in a simulator and having a direct access to the internal data formats. Comparisons were also made with emulation-based experiments, using a very low-cost environment built around a simple development board with a Xilinx FPGA. It has been shown that the level of performance of emulation-based fault injection, using such a simple set-up, essentially depends on the communication link bandwidth between the prototyping board and the host computer (classically, a PC computer). It was also shown that a small FPGA can effectively be used to validate blocks with a high number of I/Os.

For emulation-based experiments, the feasibility of the alternative approach based on the modification of the bit-stream had been demonstrated in 2000, for several types of faults including SEUs. The automation of the injection campaign using such a technique continued in 2001 and is now near completion. Fault injection campaigns using this approach are planned in 2002 in order to compare this approach with more classical approaches in terms of experiment time.

Injection campaigns were run in 2001 on a circuit described at different levels, and injecting faults also modelled at different levels (e.g., SEUs modelled as erroneous transitions at high level, and bit-flips at low level). These experiments proved that useful dependability information can be obtained very early in the design cycle. Limitations were also identified.

**II-3.13 SEU's circuit characterisation**

*Memebers: L. ANGHEL, S. SALEH*

The decision to protect a system from errors coming from SEU's can be make after the designer has analysed and evaluated the sensitivity of an IC and calculated the SEU error rate. If this evaluation shows an unacceptable error rate, the designer should develop SEU fault tolerant techniques. A tool to evaluate the efficiency of these techniques is necessary in order to make a good choice with respect to the efficiency and cost. Our previous work addresses the characterisation of transient pulses induced by cosmic particles (duration, amplitude, probability of occurrence). However, before an evaluation, cells used in a system could be characterised in terms of sensitivity. The objective is to develop a methodology, characterisation tools (pulse characteristics and sensitivity) and library cells for different types of cosmic particles. In addition, a special effort will be done to accelerate 3D physical simulations.

**II-3.14 CAD Techniques for nanotechnologies**

*Memebers: E. KOLONIS, M. NICOLAIMIS, L. ANGHEL*

The continuation of the miniaturization in the micro-electronic technologies, principal factor of the data-processing revolution, will have reached its ultimate limits near the year 2010. The reasons are not only technical (current leaks, signal integrity, power consumption, storage capacities...), but also economic. Electron transistors, quantum cellular automata, molecular logical components, nanocrystals, are some possibilities for future technologies. Manufacture alternatives of very complex circuits, with low energy consumption and low cost, point at the horizon with the fast sophistication of the chemical synthesis processes, making it possible to synthesize electronic components and their inter-connections chemically, to create very complex systems and at low cost. These circuits would integrate hundreds of billion devices in regular networks. These very low cost processes have very poor manufacture yield, and by consequence a much higher density of defects than in current technologies. This project relates to the study of techniques making possible to
configure a support containing very simple elements, possibly including defects, and interconnected in a very complex network, in order to create a system of traditional calculation or to simulate a complex system, natural or imagined by the man.

II-3.15 *Towards nanoelectronics design*

*Members: R. LEVEUGLE*

Some work started in 2000 on the implementation of logic circuits using nanoelectronic devices. This project had been defined in collaboration with CEA/LETI and aims at taking advantage of the single-electron transistors (SETs) developed in Grenoble. In 2000, a preliminary study of the state-of-the-art had been performed. The effort has been focused in 2001 on the study of simple logic and arithmetic components, and on the simulation approaches available for such devices. At medium term, the analysis of the expected behaviour of such devices is planned, with respect to process and characteristics variability. The work will aim at proposing solutions to tolerate this variability as well as process defects and transient faults.
II-4  System Level Synthesis (SLS)

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**Research areas:**

This group investigates Application-Specific Multiprocessor Systems on Chip. Research topics include:

- Multiple and mixed-level specification of heterogeneous systems
- Multi-core architecture for networks and systems on chip
- HW/SW on-chip communication design for application-specific multiprocessor Systems-on-Chip
- Memory design for multiprocessor Systems-on-Chip
- Software code for Hardware debug.

This group has a long standing experience in the area of system-level synthesis and hardware/software codesign. Previous research has generated more than 150 international publications.

**Contracts:**

FRANCE TELECOM, STMicroelectronics, MEDEA+ SPEAC  
Start-up company created: AREXSYS

II-4.1 Networks and systems on chip

ITRS roadmap predicts that in 2004, 70% of ASICs will include at least one embedded instruction set processor. In this case, most ASICs will be SoCs (Systems-on-Chip). This prediction is not only confirmed but strengthened: SoCs will include several instruction-set processors in the case of applications such as mobile terminals (e.g. GSM), set-top boxes (e.g. pnx 8500 from Philips), game processors (e.g. PlayStation2 from Sony) and network processors. These designs correspond to mass-market products that are (or will be) integrated on a single chip for production cost reasons. It is even expected that these applications act as the main drivers for the semiconductor industry. Most system and semiconductor houses are working on platforms allowing the integration of several cores (CPU, DSP, MCU, co-processors,...) and sophisticated communication networks (hierarchical bus, TDMA-based bus, point-to-point connection and packet routing switch) on a single chip. The trend is then to build large designs using an on-chip network. The game is now to interconnect standard components as we used to do for boards a few years ago.

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1 Industrial Ph.D.
This evolution is creating several breaking points in the design process and new challenges that need to be solved:

1- Systems are complex: communication cannot any more be specified manually at a low level such as the register-transfer level (RTL), where physical wires and clock cycles need to be detailed. Higher-level abstraction models of interconnect are required to master the complexity.

2- SoCs will include more than one instruction set processor executing dedicated functions implemented in software for flexibility reasons. It is expected that the complexity of this code will be higher than the hardware part and will require several hundreds or thousands man-years in the near future. This software cannot be any more designed at the assembly level.

3- Complex on-chip hardware/software communications are required to implement these SoCs: multiprocessor architectures may require application-specific communication network. When systems are integrated on a single chip, the hardware and software sides of the communication protocols need to be adapted to each other. Complex memory interfaces need also to be tackled.

To our knowledge, none of the existing tools and methods have addressed all the three above mentioned problems. Hopefully several previous works addressed them individually.

1- Several existing works deal with higher level specification. Three approaches were studied: Using an existing software system specification language (SDL, StateChart, Esterel, ...), Extending an existing language with additional syntax or runtime libraries (SystemC, SpecC, RTC, ...) and finally creating a new language (e.g. Rosetta). Additionally, some system-level synthesis tools (also called codesign) were built around these tools. However, most of these environments are restricted to single processor architectures and handle hardly multi-level specification and sophisticated real-time software.

Lots of works have also tackled heterogeneous systems dealing with several languages or models of computation. Co-simulation tools have been developed for the validation of these models. These approaches come from academia (Ptolemy, SPI, VCI, MCI, ...) and industry (CoWare, Arexsys, Seamless, VCC, ...). Unfortunately these approaches were mostly restricted to validation and few efforts are devoted to synthesis from heterogeneous models.

2- Multiprocessor architecture on chip is an emerging issue. Several computer houses (Sun, IBM, Intel) are announcing general purpose complex architecture on chip including several in-house processors and on chip buses. On the other side, telecom and multimedia applications have generated several multiprocessor designs including a DSP and a controller on the same chip. However, the design of this kind of architecture still requires some automation and the design of hardware/software interfaces in the case of multiprocessor architecture is still a bottleneck that needs to be automated.

3- Hardware/software communication is a key technology for future component-based SoC design. Component interfaces require hardware wrappers and software wrappers to isolate functions from architecture. The hardware wrappers are quite well handled in literature and several solutions exist. These include VSIA, Sonics and CoWare. Software wrappers is an OS-like layer aimed to abstract the architecture from the software application. For end-user applications, this may be a standard OS. But in the case of high-performance processors dedicated to specific functions this needs to be a custom application specific OS. This is a new research area generated by SoC design.
II-4.2 Design flow for multiprocessor system synthesis

Figure II-4.1. shows a generic design flow for multiprocessor SoCs. Hardware and software synthesis is taken into account in this flow using three abstraction levels: system or transaction level, macro-architecture or message level and micro-architecture or register transfer level. The system is initially specified at the system level: a set of hierarchical modules and processes communicating through high-level protocols via abstract channels. A channel may hide high-level protocols and communication primitives handling abstract data types. Transaction schemes are used for communication. At this level, the modules may be described using different languages and/or using different abstraction levels. Co-simulation is required to validate the functionality of the system.

System level

- Architecture definition
- Hardware/software partition
- Communication protocol selection

Macro-architecture level

- Interface synthesis
- OS synthesis
- Software targeting
- Task scheduling
- Memory architecture definition

Micro-architecture level

- Software compilation
- RTL synthesis for the HW part

Figure II-4.1 Design flow example

The second abstraction level represents an abstract architecture that we call macro-architecture. This architecture is composed of a set of modules interconnected through logical wires. Each module represents a processor in the final architecture. This may be a software processor (e.g. DSP or a microcontroller executing software), a hardware processor (specific hardware) or an existing IP (global memory, peripheral, bus controller, ...). The logical wires are abstract channels that transfer fixed data types (e.g. integer, real) and may hide low-level protocols (e.g. handshake or memory mapped I/O). The different modules may be described using a single or several languages. Co-simulation is required to validate the partitioning and the abstract communication.

The final abstraction level gives the detailed architecture that we call micro-architecture. Software modules are mapped onto specific processors. This requires the synthesis of a hardware interface to link the processor to the rest of the architecture. When the software includes parallel task a specific
operating system (OS) is synthesized. Hardware blocks are refined to the clock-cycle level. Finally, existing blocks (IPs) are encapsulated within an interface in order to accommodate the final protocols. The communication between the different blocks is made through physical wires that implement the final protocols. The interface block may include controllers and buffering when needed.

The goal of this project is to develop a methodology and a set of tools able to solve all the three above-mentioned problems. The key issues are:
1. To develop a target architecture and a design representation model that allows for flexible, modular and scalable design in order to support the synthesis of multiprocessor systems on chip.
2. To define a design flow that allows bridging the gap between heterogeneous system specification and system-on-chip implementations.
3. To define a set of methods and tools that implements the system design methodology.

II-4.3 Efficient architecture models for multiprocessor systems-on-chip

A simplified view of a Multiprocessor SoC architecture is shown Figure II-4.2. It is decomposed in several layers in order to master the complexity. The hardware is decomposed in two layers:
- The lowest layer is composed of the main hardware components such as processors, ASICs and memories.
- The architecture of the SoC is described by the hardware on-chip communication layer. This is the glue required to make the components communicating together.

The software part is also decomposed in several layers (They have been simplified for clarity). By increasing level of abstraction, we have:
- The lowest layer include the drivers and the low level architecture controllers
- The communication managers and resource management layers are made of a set of services. They constitute an OS. It provides higher level primitives such as task and memory management. This is accessed through an API.
- The highest layer is the application.

The first two layers constitute the software communication layer and may hide an Operating System (OS). In reality, the software interfaces may be much more sophisticated; they may include ASIC management.

![Figure II-4.2 Simplified view of HW/SW organization](image-url)
The key issues when designing such a SoC are:
- Abstraction of inter-module communication
- Architecture model to support hardware/software communication refinement.

In this work we develop a high-level system design methodology aimed at component-based design. This is a multiprocessor SoC design approach using a communication refinement methodology based on virtual components. In this methodology, the system is described as a set of virtual components interconnected via channels. A virtual component consists of a wrapper and an internal component. The internal component corresponds to a heterogeneous component (a software function or a hardware function) and the wrapper adapts accesses from the internal component to the external world, i.e. channels connected to the virtual component. The internal component and external channel(s) can be different in terms of (1) communication protocol, (2) abstraction level, and (3) specification language. Depending on the difference, the functionality of the wrapper is determined and automatically generated.

II-4.3.1 Virtual Architecture Model

Our component-based design methodology uses an abstract model of the architecture that we call virtual architecture. The virtual architecture, also called macro architecture, represents a system as a hierarchical network of modules (see Figure II-4.3). Each module consists of an internal behavior and ports. Modules communicate with each other through channels connected to their ports. In the case of a heterogeneous specification, channel and module may use different abstraction levels or different communication protocols. In this case, we use wrappers in order to represent the connection. The wrapper is composed of an interface made of virtual ports. It isolates the behavior of the module from the rest of the system.

A virtual port has internal and external ports (see Figure II-4.3). There could be an n to m (n and m are natural numbers) correspondence between the internal and the external ports. The virtual port can contain multiple levels of hierarchy to represent this correspondence, like the virtual port of M1 with configuration parameters in Figure II-4.3. Internal and external ports may not be directly connected because they can use different communication protocols and/or transmit signals at different abstraction levels. For this reason, in some cases the wrapper will do a conversion between different internal/external communication protocols and/or abstraction levels.

Virtual channels hide details of communication protocols, for instance, FIFO communication is realized using high-level communication primitives. In our design flow, the virtual architecture is described using an extension of SystemC. Three new concepts are used:

- the virtual module: consists of the module and its wrapper;
- the virtual port: groups the corresponding internal and external ports having a conversion relationship. Thus, a wrapper may be composed of several virtual ports;
- the virtual channel: grouping several channels having a logical relationship (e.g. wires belonging to the same communication protocol).
The virtual architecture model can be used to abstract the full system including hardware modules, software modules and interconnect. In order to allow for system refinement, this model needs to be annotated with architecture configuration parameters.

All architecture parameters, as the kind of protocol used and the physical addresses of ports, are captured as attributes. This model is not synthesizable/executable because the behavior of wrappers is not described. The main goal of this design methodology is to generate automatically these wrappers, in order to produce a detailed architecture that can be both synthesized and simulated.

II-4.3.2 The generic architecture model

When defining this model our goal was to have a generic model that can be customized to fit the specific needs of the application. Both computation and communication may be customized. For computation we may change the number and kind of components and for communication we can select a specific communication scheme. The architecture model is suitable to a wide domain of applications.
We use a generic multiprocessor SoC architecture as shown in Figure II-4.4. Processors are connected with communication networks via wrappers. In fact, the processors are separated from the physical communication network by the wrappers that act as communication coprocessors or bridges. Such a separation is necessary to free the processors from communication management and it enables parallel execution of computation tasks and communication protocols.

As shown in Figure II-4.5, the wrapper is made of a software part and a hardware part. On the hardware side, the internal architecture of the wrapper consists of a processor adapter, a channel adapter, and an internal bus. To generate the wrapper, we use the communication library where we have templates for the processor adapter, the internal bus and channel adapter. The number of channel controllers depends on the number of channels that are connected to the corresponding virtual module.

On the software side, wrappers provide the implementation of high-level communication primitives (API) used in the software module and the drivers to control the hardware. If required, the wrapper may also provide more sophisticated services such as task scheduling and interrupt management.

II-4.3.3 Design environment - conceptual view

Figure II-4.6 presents the conceptual view of our design environment; four internal models are manipulated in this environment: the virtual architecture model, the macro-architecture co-simulation model, the RTL target architecture, and the RTL co-simulation model.

The design flow starts with a virtual architecture model that captures the global organization of the system into modules and the architecture configuration parameters. This input model may be manually coded (as indicated in Figure II-4.6) or may be generated automatically by specification analysis tools.
The first executable model, the macro-architecture co-simulation model, may be used to validate the virtual architecture. In the RTL target architecture model, computation and communication are customized to fit the needs of the application. For detailed functional validation at the RT-level, the RTL co-simulation model can be used. The last three models are generated automatically from the virtual architecture model. The main technique used here is automatic generation of wrappers.

II-4.4 Component-based approach for multi-core SoC

The overall view of our design environment is shown in Figure II-4.7. The environment uses an internal representation. An initial internal model is obtained from a translation of the extended SystemC specification, which is a virtual architecture annotated with configuration parameters. There are three tools for automatic wrapper generation: co-simulation wrapper generator, hardware wrapper generator, and the software wrapper generator.

The co-simulation wrapper generator produces an executable model that is used to validate the internal model. This executable model is composed of a SystemC simulator that acts as a master for other simulators. A variety of simulators can participate in this co-simulation: SystemC, VHDL, Verilog, and Instruction-set simulators. In the co-simulation library, there are simulation adapters for the different simulators that are supported in our co-simulation environment. There are also channel adapters that implement the different communication protocols in the different supported languages.
The software wrapper generator produces operating systems streamlined and pre-configured for the corresponding software module(s) that runs on each target processor. It uses an operating system library that is organized in three parts: APIs, communication/system services, and device drivers. Each part contains elements that will be used in a given software layer in the generated OS. Furthermore, the library contains a dependency graph between the elements that is used to determine the minimal set of elements necessary to implement a given OS service. This mechanism is used to keep the size of the generated OS at a minimum, by avoiding the inclusion of unnecessary elements from the library.

The library used by the hardware wrapper generator has two parts: the processor library and the protocol library. All models stored in the hardware wrapper library are synthesizable. They are instantiated by the wrapper generator and configured using the architecture configuration parameters. The processor library contains processor adapters, template architectures for processors, processor cores, local memories and peripherals. For instance, the following configuration parameters are used for processor adapter instantiation: ports’ allocated addresses, number of interrupts and their priorities. The protocol library contains channel adapters and communication network models. Channel adapter configuration uses the following configuration parameters: input/output type, master/slave operation, type of data transmitted, buffer size, and interrupt parameters.
The output of this flow is a synthesizable RTL model that can be simulated or used to produce an implementation prototype or final SoC.

The experiment of this approach with a VDSL example shows a drastic reduction of design time without any significant loss of efficiency in the final circuit.

II-4.5 Distributed shared memory for multiprocessor architectures

The design of multiprocessor systems implies a special attention to the design of the embedded memory and usage because these are important factors that fix the performances and the cost of the resulting design. Although lots of research works have been made around memory management, this problem is still far from being solved in the case of the design of specific multiprocessor architectures. Existing work comes from two different communities:

1- distributed computing literature includes lost of works on local/global memory trade-off in the case of general purpose multiprocessor architectures. These assume the existence of parallelizing compilers able to map applications onto architectures. Unfortunately these parallelizing compilers do not produce acceptable performances.

2- Memory management literature for VLSI includes also lots of works on memory structure allocation and data management. Unfortunately, they give very few links to low-level implementation of multiprocessor architectures. Additionally most of these works restrict their input to a simple data-flow graph and also assume the existence of a parallelizing compiler. In some cases these approaches allow to improve the performances of the final compilers.

Our approach consists in designing a multiprocessor system-on-a-chip with heterogeneous application-specific memories in order to guarantee (1) good system-level specification and simulation, and (2) good memory design exploration and optimization (memory size, bandwidth ...). The key issue is the separation between the memory IPs and the communication network. Therefore, the specification and implementation of interfaces become major design problems with regard to the integration of several memory IPs into a system-on-a-chip.

Our first contribution is a flexible memory wrapper architecture that can solve the problems related to memory integration for different applications. The second contribution is the automatic generation of the memory wrapper by assembling library components.
II-5 Verification and modeling of Digital Systems (VDS)

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Research areas:

The research activities of this group address:
- the formal definition of conventional CAD specification and simulation languages
- the formal verification and diagnosis of design errors in digital systems and SOC designs
- the application of formal methods in relation with mechanized high-level synthesis

Contracts:

MEDEA-MESA, CAPES/COFECUB, RNTL-VERHAUNIC

Industrial Partners:

ST-MICROELECTRONICS, PHILIPS, VALIOSYS

Topics:

Specification Languages, Hardware Description Languages, VHDL, Symbolic Simulation, Formal Verification, Proof of Correctness, Theorem Proving, Model Checking

II-5.1 Formal verification from standard hardware descriptions

Members:  G. AL SAMMANE, D. BORRIONE, E. DUMITRESCU, P. GEORGELIN,  
C. LE FAOU, P. OSTIER

The inclusion of integrated circuits in safety-critical applications requires that the correctness of hardware (and hardware/software) designs be ensured by rigorous methods. Moreover, the cost of design iterations, and the loss of market shares in case of late detection of errors, makes it mandatory to achieve error-free designs. Simulation is still the most commonly used validation technique. Yet the application of formal methods can provide a valuable alternative, by ensuring complete correctness (and not correctness of test cases considered representative of all the possible ones), and by freeing the designer from the time-consuming development of stimuli and interpretation of simulation results.

The objective is to develop mathematical models and verification techniques that can prove the correctness of a design, and provide automatic diagnosis when design errors have been exhibited. Many aspects of hardware behavior have to be considered, and no single verification paradigm can apply to all of them. So we consider value simulation and symbolic simulation as the first method to gain initial confidence in the design, at all levels of abstraction; binary equivalence checkers at logic level, as well as general purpose theorem proving at more abstract levels for the proof of

\(^1\) Thesis on co-tutorship with Hans Eveling, Darmstadt University of Technology, Germany
correctness; symbolic model checking as well as theorem proving for the proof of properties. To include formal verification in the design flow, as a complementary technique to the other usual CAD tools, standard HDL inputs must be accepted. Our group has been a precursor in promoting the formal verification of VHDL descriptions, and is very much involved in the VHDL standardization activities.

Enhancements to the PREVAIL-V2 environment

PREVAIL-V2 is a multi-HDL, multi-tool formal verification environment, which aims at improving the ease of use of new verification techniques, by providing automatic translators from conventional design languages to the input format of formal verification tools. PREVAIL-V2 implements the formal models defined in our group for the symbolic verification and formal correctness proof of designs described in standard languages, with an emphasis on VHDL. It is based on the results of a cooperative effort between Université de Provence - Marseille, Université Joseph Fourier - Grenoble and Technische Hochschule Darmstadt (Germany).

![Diagram of the PREVAIL-V2 environment](image)

**Figure II-5.1 The PREVAIL-V2 environment for formal verification**

PREVAIL-V2 has the following features:

- A new compiler front-end for VHDL, built over LVS\(^2\), and taking advantage of the flexibility and extensibility of the LVS data model. LVS has extension capabilities for its internal data structure representing compiled VHDL design units. Using this feature, we are able to elaborate in a first phase the pertinent information needed to generate the target code, and we can attach them directly on the tree built by LVS. The second phase of the compilation exploits these informations to generate the code, in our case the semantic model for the VHDL design in the appropriate input format for the verification tool being considered. This new compiler design allows better performances, facilitates maintenance and will ease future extensions of the translator.

- The sub-language recognized has been enhanced. It is the clock synchronised part of the Level 1 "Standard for VHDL RTL Synthesis" which has been voted as IEEE P1076.6 standard, when

\(^2\)LVS is distributed by Synopsis
considering the use of model checking tools. So it fits more closely the needs of the designers. A report describes the sub-VHDL used in the Prevail verification environment. A distinction is done between "not supported" parts of the VHDL standard, "ignored" parts and "not implemented" parts.

- A translator from VHDL to Blif-mv, and an environment to help the user execute the VIS system on VHDL descriptions, for equivalence checking and model checking. Until now, the circuit descriptions we were able to handle were required to have only one global clock. This was known as the "unique clock synchronization assumption". The PREVAIL-V2 VHDL to Blif-MV translator is now able to handle circuit descriptions with multiple clocks. We refined the notion of clock abstraction by the introduction of a universal clock. All clocks are required to change their state synchronously with a state change of the universal clock. This model does not restrict, from the verification point of view, the generality of the multiple clocked circuit behaviours. The class of circuits that can be handled is much larger and fits more closely the industrial needs. Using this translator, the designer can verify the equivalence between either two VHDL descriptions, or a VHDL and a Verilog description, using the VIS system. It is also the entry point to experimenting with new algorithms for equivalence checking, prototyped in G-Check (in cooperation with Ain Shams University, Cairo, Egypt).

- A prototype translator from VHDL with integer arithmetic to a Lisp-based intermediate format, towards the use of the ACL2 theorem prover (see next section).

The first three points above were started in 1998 and the development was continued in 1999 and 2000. The last point was started in 1999, and is continuously evolving.

II-5.2 Verification of behavioral VHDL descriptions by theorem proving

Members: P. GEORGELIN, P. OSTIER, D. BORRIONE

While performing the functional validation of the initial specifications and early design decisions, documented at an abstract description level, one should be able to avoid "over specification", and concentrate on the correctness of algorithms and the essential mathematical properties of the blocks being designed. This is where state of the art equivalence checkers and model checkers cannot be applied any more, and must be complemented with symbolic simulation and theorem proving.

![Diagram showing the process from design specifications to their formal model in the ACL2 logic](image)

Figure II.5.2 From design specifications to their formal model in the ACL2 logic

However, going directly into theorem proving represents a formidable semantic abstraction, and is not likely to be accepted by the designer (Figure II.5.2); a more reasonable approach appears to
start from the currently accepted design methods, which involves test execution and simulation, and progressively introduce more formal methods. To this aim, we provide formal semantics for the design languages, and translate the designer’s specifications into their formal counterpart in logic. More precisely, the designer’s specification is assumed to be written in a "behavioral synthesis subset" of VHDL, and the formal model is written in the subset of Common Lisp that is accepted as input to the ACL2 theorem prover.

ACL2 is an automated theorem prover that uses a large applicative subset of Common Lisp as its input language. It is the descendant of the highly successful NQTHM prover of Boyer and Moore, which it has replaced. Technically, ACL2 reasons on a quantifier-free first order logic. In practice, it is a tool to state and check properties of Lisp programs that usually model some computational system. ACL2 includes powerful and automated proof techniques (e.g., induction) which are not fully automated in other tools, relieving the ACL2 user from providing the proof engine with the detailed inference steps in order to obtain a proof. Furthermore, since Lisp is a compiled programming language, all ACL2 specifications are executable in an efficient way, and the ACL2 models of computational systems are reasonably easy to build and understand. Finally, a user community has emerged, whose policy is to share all libraries being developed over the system. The research on the verification of designs using ACL2 was started two years ago, and is a long term project of the group. We are interested in high-level, behavioral descriptions, which are not quite amenable to other verification techniques such as finite model-checking.

As a first step, we limit ourselves to a behavioral style of description, and to a VHDL synthesis subset that excludes physical time and non-discrete types. We further require that processes be synchronized on a single clock edge, and that they be put in a normal form with a single \texttt{wait} statement at the beginning. Under these conditions, we may identify the simulation step with the clock cycle. Presently, a design is represented by an entity followed by its associated architecture composed of one or several processes. The semantics of the VHDL subset have been defined in the logic of ACL2.

![Figure II-5.3 Translating VHDL to ACL2 logic](image_url)

We built a translator that takes a VHDL design and generates the corresponding ACL2 model. The translator proceeds in two steps (see Figure II-5.3):

1. First we translate standard VHDL source code into a prefix, fully-parenthesized, Lisp-like intermediate format, which represents the essential characteristics of the design extracted from the source VHDL, and allows for an easier and fully automatic generation of the provable model. The intermediate format was deeply revised in 2001. It is now called NIF (New Intermediate Format). It is composed of a list of Common Lisp statement of properties, each
starting with a keyword, which correspond to the characteristics of the descriptions. This representation closely mirrors the original design, yet it is more amenable to processing by ACL2.

2. We wrote a set of macros and functions that translate the NIF representation of a VHDL design into its formalization in the Ac12 logic. All basic theorems and functions to create and manipulate the elements of the model state are now automatically generated without risk of human errors.

This model comprises a set of functions and theorems describing the simulation behavior of the VHDL design. The same model can be used for three tasks.

Value simulation

The logic model is executable: since ACL2 functions are ordinary Lisp code, the model can be executed on test cases, reproducing the effect of a standard VHDL simulator. Thus we can simulate the formal model extracted from the VHDL description on the designer’s test data, and check that the results obtained with our model are the same as the ones obtained with a conventional VHDL simulator. This is essential to gain initial confidence in the formal model.

Symbolic simulation

After this first simulation step on concrete data, symbolic simulation on indefinite data can be applied: the expected result is the general form of the expressions computed by the operator being designed. Typically, symbolic simulation will be performed starting from a well defined initial control state, and following a definite number of control steps. So data values are kept symbolic, but control values will be at least partially fixed. Thus, a single simulation run may also deal with a very large or infinite number of cases. This method is more restricted than theorem proving, but it is easier and fully automated. It is implemented by a set of theorems (also generated by the translator from VHDL to ACL2) that “direct” the theorem prover engine to symbolically simulate the design. At this stage, the theorem prover can be used to perform symbolic manipulations on the result expressions, and prove that they are equivalent to a specified function.

Correctness proof

The last and most abstract verification step consists in proving properties about the model itself, rather than properties of the symbolic execution results. The desired properties are stated as theorems on the design representation, and proved using the theorem prover engine with the aid of lemmas generated with the ACL2 model. This involves expert formal reasoning with the use of the theorem prover, and we have not yet been able to provide much automatic help to the non expert VHDL user.

By combining symbolic simulation and theorem proving, we aim at providing the verification engineer with a methodology to efficiently insert formal verification in the very early specification stages of a design. By automating the generation of the formal model from VHDL, we relieve the expert from some tedious tasks (translation, basic theorems, etc). We also make it possible to the new user of our proposed method to rapidly get started on simple models.

Currently, our prototype tool is limited to Moore machines synchronized by a single clock and we are working to extend the model to Mealy machines and hierarchically decomposed designs. We wrote a user interface that interacts with the top-level Ac12 read-eval-print loop and the user. This interface allows the user to:

- call the generation of the Ac12 functions and theorems from the NIF intermediate format;
- define numeric and symbolic values of variables and input signals for simulation;
- define constraints on variables and input signals;
- select basic theorem prover options.
This interface includes a basic "pretty printer" for the output results.

II-5.3  **Formal sequential equivalence checking by symbolic simulation**

*Members:* G. RITTER

A new approach to automatic symbolic simulation of sequential circuits has been investigated, to deal with circuits holding large memories described at the RTL and logic network levels. In the presence of memories, techniques relying on state space exploration suffer from an exponential size explosion. Moreover, these techniques are not well suited to the comparison of two sequential circuits that compute their result in differing numbers of steps.

To show sequential equivalence, all possible paths are symbolically simulated. At each step, functions are interpreted, and equivalent terms are accumulated in equivalence classes. The originality of this method relies on the application of a variety of equivalence detection techniques, including BDD's, and the avoidance of the manipulation of large symbolic terms. Using the equivalence of terms, symbolic simulation is guided along logically consistent paths in the two descriptions being compared, which avoids false negative comparisons.

This work co-tutored with Darmstadt University of Technology, is the topic of Gerd Ritter's PhD thesis defended in March 2001. It is considered ended with the departure of Gerd Ritter.

II-5.4  **Circuit verification using model checking**

*Members:* E. DUMITRESCU, M. BOUBEKEUR, D. TOMA, D. BORRIONE

II-5.4.1. **Verification methodology for industrial designs**

**Efficiency issues**

The application of Model Checking to circuit verification raises several important issues concerning speed and memory efficiency. Most candidates to this kind of verification are industrial sized circuits, whose representation is often too big to be handled by the classical push-button model checking technique: the fully automated approach of symbolic model checking is limited by combinational explosion of the BDD model representation.

Classical efficiency guidelines concerning model checking include design decomposition according to assume-guarantee techniques, data-path abstraction, case splitting, and data type reduction. A practical assessment of several of the above techniques has been performed, in the context of the collaboration with ST-Microelectronics. The study example used was an instruction cache controller designed by ST. Given the features of this design (about 1500 lines long, the VHDL elaboration gives a total number of 1000 flip-flops, address buses are 30 bits wide, and data buses are 32 bits wide, the width of the fetch port is 128 bits), it is practically impossible to perform a verification task by using the push-button approach of model checking.

A very important issue in the verification of the cache controller concerns the design decomposition. The VHDL code inspection reveals that no explicit hierarchy indications exist: the different functional blocks of the cache controller (internal fetch, external fetch, DMA, etc.) are not clearly separated. They are implemented as collections of interconnected clock synchronized and combinational processes. Hence, isolating functional blocks is the key point in the verification of
this design, allowing independent reasoning about its different parts. Thus, properties concern one functional block instead of the whole design.

A further step in verifying a property consists in deciding whether it is possible to reason about one functional block regardless of its environment. This allows the functional block to be cut away from its environment, which significantly reduces the complexity of the verification task. However, it is not always possible to completely abstract away the environment of a block. The intermediate solution consists in reproducing some of its key behaviors as a simple description which is abstract and non-deterministic and which replaces the initial definition of the environment.

Temporal case splitting is another method that has been successfully applied. It is often the case that several execution scenarios can be identified (e.g., read or write transactions). Most properties that are true for a given functional block must also be true for any execution scenario that may occur. For instance, a verification goal asserts that transactions on a port of the cache controller are correct. This goal can be split into two sub-goals, according to the following scenarios: (1) only read transactions are allowed and (2) only write transactions are allowed. If both read and write transactions are proved correct, we may conclude that all transaction on this port are correct. The two sub-goals constrain the signal indicating the direction (read or write) to constant values. Thus, the size of their underlying model becomes considerably lower due to BDD simplifications.

The set of model simplification guidelines presented here allowed a reasonable functional coverage for the verification of the cache controller design. All the functional blocks have been addressed, despite the lack of hierarchy in the RTL description of the design.

Using Model Checking for line coverage assessment

Line coverage information is a part of the design simulation results. The existence of lines that have not been executed at all, or even those which have a poor coverage, may be a precious indicator, often allowing engineers to find design errors. However, exploiting this information is not obvious, as it is also possible that an adequate test pattern could eliminate all doubts. Such situations are often delicate, as it may be very hard to decide between these two possibilities if the only available tool is simulation.

Model checking tools can be used as “test pattern generators”. It is enough to assert that a particular line is never reachable. If the proof answers “no”, a counter-example is generated, which consists of the sequence of steps leading to the execution of the line concerned. However, the result of this method strongly depends on whether the proof is applied to a single module, a few interconnected modules or the entire system: the more modules, the more accurate the counterexample, but unfortunately the less efficient the proof. Cutting down the number of modules may influence the accuracy of the counterexample: if the incoming ports of a module become free, all possible input behaviors are considered legal when generating a counterexample, while only a few of them are legal with respect to the whole initial system. Hence, this method is not well adapted for large circuits. We propose an alternative solution, which consists in using decomposition in order to validate the module (and especially the behaviors implemented by the uncovered lines) for any input behavior. Even though this workaround does not solve the coverage problem at the system level, it gives more confidence in using the suspected module.

This work shows that in the current context, given the available tools, it is essential that verification engineers are aware of the implementation details of the design they verify. The ignorant application of automatic model-checking fails in most cases.
II-5.4.2 Verification of asynchronous circuits

The VDS and CIS groups of TIMA have started to cooperate on the formal verification of asynchronous circuits. Up to now, simulation was the only verification means, and it came late in the design process. Trying to model check the synthesis result is difficult because each gate, each flip-flop is a process, each wire is a state element; an event is the arrival of a valid value on a wire, and all inter-leafings of events may a priori occur. Applying brute force model checking quickly leads to combinational explosion.

As an initial feasibility study, we use existing verification tools, even if they were initially not intended for asynchronous designs. More precisely, commercial model checkers used in hardware verification, starting from a standard Verilog or VHDL description, usually assume the existence of a single synchronization master clock for the circuit. In order to provide an early validation of the initial model properties, we extract a state machine from the kernel Petri Net and give a VHDL representation for it. In the first prototype, we introduce a fictitious clock that allows us to examine the model after each transition firing in a sequential path, and to use existing model checking software. In addition, the translation takes advantage of the known restrictions on the Petri Net, being the semantic representation of a CHP program.

Figure II-5.4 shows the introduction of a formal verification step in the TAST design flow of the CIS group. TAST mainly consists in three parts: a compiler, a synthesizer and a simulation-model generator. The compiler translates CHP programs into Petri Nets (PNs) associated to Data Flow Graphs (DFGs). The synthesizer is in charge of generating asynchronous circuits from the Petri Net representation of the CHP programs. Behavioral VHDL models of the CHP specification are generated to perform CHP programs verification using simulations (simulation model generator). More details on TAST are given in the CIS group chapter.

Figure II-5.4 Introduction of formal verification in the TAST design flow

The introduction of a formal verification flow in TAST starts from the Petri Net - DFG format. (Figure II-5.5). A first step consists in choosing an appropriate communication protocol, as well as expanding all communication primitives according to this protocol. A state encoding is associated to the resulting Petri Net, based on its global place marking. From this state encoding, a Finite State Machine interpretation of the Petri Net is constructed and implemented as a VHDL behavioral model. The model obtained can be directly fed to an industrial model-checking tool, accepting a
standard HDL entry. The formal verification task consists in modeling the environment of the description we wish to verify, and writing a set of temporal properties that need to be satisfied. On the other hand, the asynchronous synthesis tool produces a VHDL gate level netlist, which can also be fed to a model-checker. Thus, the compliance of the synthesized model with respect to its specification can be checked, by trying to prove the same set of temporal properties on the specification and the synthesis result.

![Diagram](image)

**Figure II-5.5 Formal verification flow for CHP programs and QDI asynchronous circuits**

In order to benefit from existing industrial tools, and fit in the design flow, we built a prototype which translates the Petri net representation into a register transfer level, behavioral VHDL model suited for formal verification (i.e. compliant to the 1076.6 standard). The simulation-oriented behavioral VHDL model generated in the TAST flow contains timing and attribute directives which are essential to follow the propagation of the signals, but make this model improper as an input to model checking tools. Ignoring or removing all delays alters the behavior of the model. The trick consists in replacing each unit delay by a tick of a fictitious clock, thus making visible the “delta” delay of a purely behavioral, non-timed, state transition model.

To obtain a correct behavior, a set of environment assumptions must be associated to each communication channel, ensuring that each input wire behavior is compliant to the protocol implemented by the channel, e.g. a four-phase communication protocol. The environment behavior can be modeled as a non-deterministic description, which is plugged to each channel. A fairness condition must be associated to each dual instance, in order to express the fact that it always reacts within a finite delay.

The verified properties correspond generally to the Petri net branches, i.e. the reachability of certain places or transitions by following a given path. Or they are used to express input-output relationships.

The verification of large descriptions will eventually face combinational explosion. Two main directions are explored in order to handle this problem. On the one hand, we try to reduce the number of states of the underlying model associated to a CHP program. On the other hand, a verification strategy is required, which exploits the characteristics (symmetry, control and data path, etc.) of particular classes of designs, such as the asynchronous arbiters.
II-6 Qualification of circuits (QLF)

Group Leader: R. Velazco
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Research areas:

This research group addresses the following topics:
+ methodology and tools for test under radiation
+ study of the effects of atmospheric neutrons on commercial integrated circuits
+ HW and SW techniques for hardening digital architectures devoted to space applications
+ fault injection and error rate prediction for digital architectures operating under radiation
+ design of experiments on board satellites
+ digital implementation of intelligent control (fuzzy logic, neural nets)

Contracts and projects:

CNES, JPL (Jet Propulsion Laboratories, Pasadena, USA), INTA (National Institute of Aeronautics and Space, Madrid, Spain), MPTB (Microelectronics and Photonics Test Bed).

Topics:

Testing and qualification of integrated circuits, test in harsh environments, radiation tests, SEU-like fault injection for error rate prediction, design hardening with respect to Single Event Upsets, digital implementation of intelligent control strategies, study of the robustness of fuzzy logic and artificial neural network approaches, design and exploitation of on-board satellite experiments.

II-6.1 Summary

The QLF group has joined TIMA in 1996. Research activities of the group deal with the study of the behaviour in harsh environment for digital circuit and systems. The main stress considered is radiation of nuclear and space environments, but it is interesting to mention that particles reaching the Earth’s surface from the Sun, up to now innocuous for microelectronics circuits, have sufficient energy to flip bits in memories and corrupt logic inside processors for parts manufactured with 0.3 µm and supply voltages drop to less than 2.2 Volts. This can constitute a threat to avionics control systems (at 30,000 feet, the neutron activity is 4 to 8 times higher than the ground), and in the future to systems operating in ground.

One of the important issues of these researches, is the prediction of failures in flight. The refinement of forecasting error rate strategies needs both to perform ground test by means of simulated radiation environment (particle accelerators) and to compare ground test results to data obtained from experiments aboard of spacecrafts. Two different satellite experiments were developed in collaboration with CNES with the goal of studying the behaviour in space of various commercial circuits (COTS) including memories, general purpose microprocessors and dedicated processors. One
of them deals with satellite image texture analysis by means of an Artificial Neural Network designed by CEA/DAM. This experiment is present on board of a scientific satellite launched November 1997 by Naval Research Laboratories (NRL-Washington). The second one, designed in collaboration with NASA, aims at studying the robustness of a dedicated fuzzy controller (the WARP processor from STMicroelectronics). The satellite carrying STRV will be launched April 2000.

One of the critical effects of radiations can be drastically attenuated by a proper design of memory cells. A patent developed at QLF has been transferred to Matra MHS to manufacture a Digital Signal Processor, the TSC 21020, suitable for space applications. Ground tests performed on this circuit have proved its immunity to Single Event Upsets. The TSC 21020, commercially available since end 1998, is one of the processors candidates to be included in the equipments of SKYBRIDGE european telecommunication satellite constellation.

II-6.2 Study of the effects of atmospheric neutrons on the operation of submicronic integrated circuits

Members: R. VEIAZCO, F. FAURE, P. PERRONARD

Ionization resulting from charged particles issued from the atomic reaction between neutrons reaching the earth's atmosphere and atoms of Boron present in the substrate of CMOS circuits, may flip a memory cell content or provoke a transient pulse within a combinational circuit. This phenomenon constitutes a potential obstacle to the reliable operation of circuits manufactured from future deep submicronic processes.

A first step towards a thorough study of this problematic consists in putting in evidence the phenomenon through experimentation with suitable test vehicles and an appropriate neutron beam. In February 2000 we carried out one of the first experiments performed in France in this area. The THESIC tester was used to expose two circuits (1 Mega byte static memory manufactured with a 0.25 \( \mu \)m process and a digital signal processor with a huge internal memory) to high fluxes of neutrons using beams available at Institut Laue-Langevin (ILL, Grenoble). These experiments put in evidence the need for the use of hardening techniques (design hardened memory cells, codes,...) in future deep submicronic circuits. Indeed, the number of detected bit flips suggest that next generation of SoCs (Systems on a Chip) or high-capacity static memories may be the source of frequent errors even for systems operating at sea level. In Figure II-6.1 is shown a photo of the experimental set-up used to perform neutron tests.

Future researches in this area will deal with the design and exploitation of a digital board including a very large capacity SRAM memory space architecture, which will be exposed to the effects natural atmospheric radiation to derive realistic error rates in real life environment of future submicronic components.
II-6.3 Development of a test bed suitable for the qualification of integrated circuits devoted to operate in harsh environment

Members: R. Velazco, F. Faure, F. Kaddour, P. Perronard, S. Rezgui

With the miniaturization, integrated circuits become more and more sensitive to perturbations resulting from the effects of the environment (temperature, radiation, EMC,...). This activity concerns the design of a test system which facilitates the realization and exploitation of qualification tests for all kinds of circuits, from a simple register bench to complex components such as processors.

Screening tests are mandatory to predict error rates. They consist in exposing the studied parts, eventually operating in vacuum, to simulated stress conditions. The hardware and software developments related with such tests must take into account the random nature of event occurrence, both in time and space. On one hand this entails on-line error detection, on the other hand this makes mandatory the need for development of ad hoc hardware mechanisms related with critical errors detection (sequencing loss, system crashes, latchups) and recovering. Most of commercially available functional testers have these capabilities, potentially offering a powerful solution to qualification test implementation for all circuit types. Nevertheless, two main drawbacks must be mentioned:

- functional testers cannot fit inside most of vacuum chambers available at generally used radiation facilities. The alternative consisting in using them outside the chamber connected to the device under test (DUT) inside the enclosure, may lead to serious signal propagation problems,

- test stimuli are defined by a set of binary patterns corresponding to circuit pins values at each clock period. For complex circuits (processors for instance) the development and debugging at this low-level of such test programs can be a difficult task. Note that these constraints may also apply for testing under other type of conditions such as temperature, magnetic perturbation, vibrations, or other type of harsh environments.

We have designed and prototyped a system, called THESIC (Testbed for Harsh Environments Studies on Integrated Circuits) devoted to harsh environment test implementations and particularly to Single Event Effect (upset and latchup) tests. A simplified version of this system is currently used to perform radiation tests qualification for complex parts candidates to space applications of European and
American space agencies.

The THESIC system comprises mainly (Figure II-6.2):

- a motherboard, performing the following tasks: control all operation related with the DUT test (power on/off, current consumption control, test stimuli download, starting /stopping test cycles; receiving, pre-processing and transmitting data to/from user interface computer,
- a daughterboard, implementing a suitable architecture where the DUTs will be exposed to environment effects while exercised by the chosen test stimuli,
- a computer, for user interface (on-line monitoring of test execution, result displaying on "understandable" format), and memory mass purposes (storing experiment historic for ulterior analysis).

The motherboard is built around a microcontroller (the 80C51 from Intel). It comprises an EEPROM where the micro-controller system software is stored, an SRAM for DUTs programs/stimuli and digital-analog analog-digital converters for DUT's current consumption or other measurements monitoring. Note that current consumption limit can be modified during a test experiment (this condition is mandatory for Single Event Latchup testing, where the latchup threshold is looked for). Communication with user interface computer is done trough a serial link.

The daughterboard, testbed for the DUTs, has a totally free architecture, but must adapt to motherboard protocol interface. To cope with a wide range of different types, two modes were provided: (a) slave DUT mode, in which all test operations are performed by the motherboard, and (b) asynchronous master DUT mode, in which the daughterboard has its own processor (under test or not) programmed to implement the test strategy including test result transmission to the motherboard (by interruption activation). In both modes communication is achieved through a memory area resident in daughterboard (Memory Mapped Interface, MMI) and accessible to the motherboard.

![Figure II-6.2 Building blocks of THESIC, the proposed system for qualification tests](image)

The first mode is well suited, for instance, to memory testing. The MMI being in the memory space of the 8051, the execution of an appropriate program allows to easily implement all currently used memory testing strategies. Note that a register buffering allows to extend the 8051 address bus to 16 bits, with the obvious consequences at operating test frequency.

The second mode can be used for all circuits, including memories. The principle is to design a daughterboard comprising a processor which will ensure DUT test control and communications with
the motherboard by means of asynchronous interruptions. When the circuit under test is a processor, this strategy has some limitation considering that errors perturbing test control operation can have consequences difficult to be predicted and/or understandable through the analysis of corrupted data. As an example, malfunctions leading to sequence loss will result in "black out" situations at the motherboard level (which during the test is waiting for daughterboard interruption indicating power consumption problems or "test results available"). To cope with such critical errors, a programmable software watchdog was implemented in the motherboard.

An example of a THESIC daughterboard designed and developed to test a digital signal processor and a commercial SRAM memory candidates to a Nanosat developed by INTA (Spanish Space Agency) is given Figure II-6.3.

![Block diagram of the DSP daughter board](image)

**Figure II-6.3** Block diagram of the DSP daughter board

A particular effort was invested on the development of friendly and powerful user interface capable to provide the operator with on-line test result data. Indeed, getting comprehensive information about detected errors is essential to efficiently reorient the given experiment depending on collected pre-processed information. For instance, in radiation tests, changed in beam energy or fluencies may be required depending the abundance of errors, thus avoiding expensive needless beam time.

A snapshot of a significant Thesic screen is given Figure II-6.4. The main window is devoted to motherboard configuration (threshold current consumption, watchdog time-out period) and to dispatch DUTs information about errors to appropriate sub-windows. Statistics about detected errors are permanently displayed (upper right corner). Two significant and original features of the developed user interface are: (a) the on-line visualization for representative indicators of DUT sensitivity to the studied environment, and (b) the possibility of replaying a given test session. Sensitivity to radiation is generally given as a "event cross section" curve, representing the number of error (normalized by the particle fluency) vs. particle energy. Such curves can be displayed and updated in real-time offering powerful insight on the behavior of the tested component (lower left window).

The replay function (upper-left window) makes possible to analyze off-beam the occurrence and location of errors occurring during a particular test experiment.

A relevant capability of THESIC tester is the possibility of transient bitflip injection on microprocessor-based digital architectures. This is accomplished by means of a suitable piece of software whose execution is triggered as the response to the assertion of an interrupt signal. The automation of this procedure, with pseudo random choice for both the occurrence instant and the target bit allow the simulation of SEU faults (Single Event Upsets) perturbing microelectronics circuits operating in radiative environments. Such fault injection experiments may be used to estimate the error rate of complex applications. Preliminary ground test performed at cyclone facility (cyclotron of Louvain-La-Neuve University) proved the validity of the approach.

We have chosen to illustrate in an eloquent manner this project by means of a picture taken during its
use on the field. Photo depicted in Figure II-6.5, shows the THESIC hardware within the vacuum chamber available at the LBL cyclotron facility. The motherboard shown in the background is fixed to a moving stage support allowing to perform the alignment DUT-beam. It communicates to an external PC through a serial link connection. The daughterboard, in the foreground, was designed to evaluate the behavior under radiation of an architecture built around a Transputer, a neural co-processor and different SRAMS. During a radiation test, target DUTs are successively aligned with the beam.

Figure II-6.4 A typical user’s window display

Figure II-6.5 THESIC System within the vacuum chamber available at LBL (Berkeley-CF, USA) facility

The main drawback of THESIC tester is the need for development of a dedicated interface board around the device to be tested. The experience acquired by QLF research group shown that the design and realization phases of such boards, could take many months in case of complex processors such as the Power PC studied in cooperation with Jet Propulsion Labs. An important effort is thus presently devoted to define and prototype a new version of THESIC tester, so-called THESIC+. The resulting system described in Figure II-6.6, is composed of:

- The control board: this block is basically based on the previous THESIC motherboard with minor additions. It includes a micro-controller (Atmel 89C52) having in charge the following tasks: it controls the circuit to qualify, runs on and off the test sequences and checks the current consumption to avoid
latchups. It is also able to transfer test programs and to gather test results from the component being studied to/from the PC user interface (via serial link RS 232).

- The interface board represents the new feature we developed to improve the testbed. It comprises an FPGA (Field Programmable Gate Array) and several memory banks: common memory (MMI) to share data between control board and the device under test (DUT), EEPROM and SRAM banks to enable fast and efficient processor tests. To cope with a wide range of DUT they are all managed by the FPGA. We chosen for this device a FLEX10KE from Altera, which is multi-volt Input/Outputs compliant, that means it can drive signals in 5 or 3.3 or 2.5 Volts, reducing the number of components needed to interface the DUT. The FPGA must be properly configured in order to assign the interface board resources to the device under test. The high-level program codes (in VHDL for instance) that interface Control Board with memories and DUTs, are downloaded from the PC into the FLEX (via the parallel port). As an example, this board is able to interface a processor with up to 64 bits data lines and 32 bits address lines.

- The DUT board (called "daughter-board" in the previous version of THESIS) comprises exclusively the component to test and, in some cases, clocks, latches and current regulators. The main THESIS modes (the slave mode which consists in managing all the tests from the control board, and master mode in which the DUT is driven by a processor that is present on the daughter board) are still available in THESIS+. Now in slave mode the microcontroller present on the control board will manage the DUT while the FPGA will just ensure the correct assignment and the bi-directional exchanges of signals between them. Therefore, the master mode is slightly different in THESIS+: indeed a suitable VHDL description (such as a simplified micro-controller) implemented in the FPGA, will enable it to drive the DUT. In both cases, the memory-mapped interface present in the interface board, still allows data sharing between control board and DUT.

Obviously, a computer is also needed in THESIS+ as a user interface. It allows the on-line control of test operations, the display of results and their storage in a mass memory in convenient formats for future analysis.

![Figure II-6.6 Principle of THESIS+ tester](image)
II-6.4 A methodology based on fault injection for the prediction of architectures’ error rates

Members: R. VELAZCO, S. REZGUI, F. KADDOUR

To predict the error rate provoked by radiation for a given application, we have investigated a new approach allowing to characterize and to quantify the effects of bit flips (also called upsets) on the operation of microprocessor-based digital architectures. The principle is to derive, from the results of fault injection experiments, the rate of “effective” bit flips for the tested programs, and thus to derive realistic figures for the expected error rate in the final application environment. Such experiments could lead to a well sound methodology for error-rate estimation, based on both a limited radiation testing (to evaluate the individual sensitivity to radiation of registers or memory words) and hardware/software fault injection to statistically evaluate the fraction of errors having consequences for the program execution.

The approach relies on the injection of errors, randomly in time and location and concurrently with the execution of a program, affecting information stored in registers and memory locations. This can be achieved with minimal “intrusiveness” using the interruption mechanism. The key idea is the generation and storage in an appropriate memory area, of a piece of code, called CEU (Code Emulating an Upset), whose execution will provoke the content inversion of selected bits, called CEU targets. If the processor is properly configured, the CEU code execution can be triggered by the assertion of an interrupt-like signal. The interruption activation instant and the CEU target can be pseudo-randomly chosen by an ad-hoc external mechanism. In this way, errors can be injected in all accessible processor’s CEU targets (internal registers and SRAM memory area) as well as in the external SRAM where program data and code is stored. A particular effort was done to extend the approach to critical registers (program counter, stack pointer, status registers...).

Main advantages of the proposed fault injection strategy are the reduced intrusiveness in the system, the low-cost, the possibilities of automation and the flexibility of the model in terms that several modules can be migrated on tests developed for other processors.

The architecture of THESIS tester, offered a suitable platform for CEU injection. The THESIS motherboard was recently enhanced with pseudo-random interruption generation capabilities and a new operation mode providing different options for CEU injection. With these options the selection of the two parameters of simulated upsets, the bits locations to be corrupted and the instant of fault occurrence, can be chosen either pseudo-randomly or deterministically. This flexibility appears to be very useful for the investigation of the effects of upsets on complex applications. For instance, repeated experiments with pseudo-random choice for both the CEU target and the occurrence instant, allow to get objective figures about the fraction of upsets which have no effects for a given program. Moreover, it may also put in evidence the configuration (occurrence instant/location) of critical upsets.

The capabilities of the CEU injection approach and the efficiency of error rate predictions were put in evidence through fault injection sessions performed by means of THESIS, on architectures built on different processors including microcontrollers (the Intel 8051, the Motorola 68332) and digital signal processors (the TI 32C50, the AD 21060). Faults were injected concurrently with the execution of modules extracted of final application programs. The same architectures and programs were used during radiation ground testing performed with different facilities, in which the processors were exposed to the effect of particles beams to get measures of error rates. The good agreement between predicted and measured error rates proved the validity of the approach.
Present work is related with the application of the CEU injection approach to a complex architecture built on a commercially available processor, the Power PC 750, intended to be included in a satellite project (the Space Environment Testbed project from NASA).

II-6.5 Study of the efficiency of hardware and software hardening techniques

Members: R. VELAZCO, B. NICOLESCU, S. REZGUI, F. GUSMAO da LIMA

The increasing popularity of low-cost safety-critical computer-based applications in new areas (such as automotive, biomedical, telecontrol) requires the availability of new methods for designing dependable systems. In particular, in the areas where computer-based dependable systems are currently being introduced, the cost (and hence the design and development time) is often a major concern, and the adoption of commercial hardware is a common practice. As a result software implemented fault tolerance is an attractive solution for this class of applications, since it allows the implementation of dependable systems without incurring the high costs coming from designing custom hardware or using hardware redundancy.

This project aims at evaluating the efficiency of two different approaches studied to enhance system dependability: one of them, consists in a software modification strategy allowing the on-line detection of bit flips affecting memory elements of digital architectures, while the other aims at the automated rapid prototyping of processors including error detection and correction capabilities achieved by means of Hamming codes.

The basic idea behind the software hardening method is to determine a set of transformation rules to be applied to a high-level code (in C language for instance) in order to get a functionally equivalent code with error detection capabilities. These transformations introduce data and code redundancies, which allow the resulting program to detect possible errors affecting storage elements containing data or code. Experimentation was carried out with the THESIC tester for a set of benchmark programs for which modified versions according to the studied rules were obtained. Two different kind of experiments were performed: radiation testing and fault injection. Obtained results revealed an acceptable percent of fault detection, putting nevertheless in evidence the main limitations of this approach: the overhead in memory area and execution time entailed by the transformation rule application.

This project is done in collaboration with the Politecnico di Torino.

Fault tolerance capabilities can be obtained in hardware designs using traditional error detection and correction strategies such as Hamming codes. For a complex circuit such a processor, protecting by suitable codes every memory element potentially sensitive to bit flips resulting from radiation, may lead to a robust low-cost device version. To investigate the potentialities of such a hardware hardening strategy, a simplified version of the 8051 microcontroller, for which Hamming codes were added to registers and internal memory, was fully implemented in an FPGA. The digital board including the FPGA implementing the 8051 hardened micro-controller was exposed to heavy ion beams using a cyclotron (the Cyclone facility available at Louvain-la-Neuve, Belgium). Performed tests revealed the 100% immunity to upsets for the robust circuit, while for the standard version, implemented in the same board by proper configuration of the FPGA, hundreds of errors were detected for the same particle beams. This robustness with respect to bit flips is obtained with acceptable hardware and time overhead.

The design of a software tool for the automatic generation, from a circuit high level description (in VHDL for instance) of the hardened description circuit is now in progress. The flexibility offered by
modern FPGAs will allow the validation of this tool by performing ground testing and fault injection experiments on a wide range of processors.

This project is done in collaboration with in cooperation with the UFRGS (Université Fédérale de Rio Grande do Sud, Porto Alegre, Brésil).

II-6.6 Study of the behaviour of digital implementations of intelligent control in space

II-6.6.1 Artificial Neural Networks

Members: R. VEILAZCO, B. NICOLÉSCU

Artificial neural networks (ANN) are adaptive and redundant information processing systems that offer attractive solutions to problems sometimes difficult to be tackled by classical approaches. The main goal of this project is to provide data showing that, due to the intrinsic robustness of neural network approaches to the space radiation environment, image texture analysis can be achieved directly on-board the satellite by means of ad hoc neural digital implementations. On-board image processing could be the preferred solution to some communication issues, such as limited bandwidth. We have considered an actual problem: on-board satellite classification of SPOT image textures in four classes (industrial area, residential area, scrubland, sea).

Calculations needed to evaluate the response of a given neural network can be performed either using general purpose computers or by dedicated hardware either digital, analog or hybrid. The advantages of digital neural implementations over analog ones are the flexibility (the network parameters and/or structure can be modified without modifications to the hardware), the accuracy (practically unlimited in digital and 4 bits equivalent in analog) and the noise immunity (analog implementations are sensitive to voltage drops). Presently, many commercially available circuits are capable of dealing with real-time constraints required by on-board satellite processing for problems, such as image analysis, for which the neural approach provides an efficient solution.

The natural redundancy of neural networks and the form of the activation function of neuron responses, make them somewhat fault tolerant, particularly with respect to perturbations in synaptic weights or input patterns. Most of the published work on this topic demonstrated this robustness by injecting limited (gaussian) noise on software models. Our work has shown that this robustness can be extended to single-event upsets (SEU) induced on the network parameters and/or input data. Ground tests performed on digital architectures comprising general purpose micro-processors as well as dedicated neural processors, have confirmed this SEU tolerance.

The neural network for SPOT image texture analysis, designed at CEA/DAM and trained with a standard algorithm (Back-Propagation) on a training set of 10,000 input images, was implemented on a digital architecture consisting of a Transputer (RISC microprocessor from INMOS / SGS-Thomson with parallelism capabilities) and a dedicated neural coprocessor (the L-Neuro 1.0™ chip from Philips). Figure II-6.7 gives the main features of the board architecture. The Transputer executes a program which mimics the network structure, preparing data needed to compute the state of each neuron. The weighted sum calculations are performed by the L-Neuro 1.0 coprocessor, having previously loaded its internal RAM with the necessary data (weights, thresholds) and the internal registers with the state of the input neurons.

To obtain ground test data on the network robustness, we have irradiated those circuits of the board where information related to the network operation is stored. The main SEU-sensitive area was the
memory portions where network program, parameters or inputs are stored. Performed heavy ion tests have shown that: (i) the particular neural network used is robust (90% of upsets are tolerated) with respect to upsets which makes it suitable for on board satellite image processing, (ii) some upsets (4% in the studied case) improve the performance in a significant way. Retraining the neural network with a Metropolis algorithm taking into account the addresses of those particular bits leads to more robust networks, (iii) the quasi-immunity with respect to accumulated upsets on input patterns, makes possible the use of SRAMS, (even if very large areas should contain significant data), and (iv) upsets on the program code itself are tolerated to some extent (20%), but this property could be a result not related to the neural networks, but probably to the processor used to implement it.

Two «neural experiments» designed at TIMA, in collaboration with the CNES (French Space Agency) and the CEA (French agency for Atomic Energy) were included in a project of Naval Research Laboratories (Washington D-C): the «Microelectronics and Photonics Test Bed (MPTB)». An American scientific satellite holding 24 experiments devoted to evaluate the behavior of modern electronic and photonic devices, 2 of them being the neural boards of TIMA, was successfully launched in November 26, 1997. The goal of the TIMA experiments (called neural boards A & B) are to obtain data about the behavior in real radiative environment of the neural boards implemented by means of commercial circuits. The results of the MPTB project could allow a more wide use of neural network approaches in space. During the 3 years flight mission of MPTB, the neural boards of the TIMA/CNES experiment have processed the contents of images taken by SPOT satellite, looking for the 4 predetermined textures above mentioned. All deviation between the expected and the actually identified textures were transmitted to the Earth for remote analysis. As SPOT image comprises typically 300 million pixels, its partial processing on-board satellite will drastically improve its utilization, particularly for applications such as measuring the extent of natural catastrophes (earthquake, flood) or tracking a cyclone, for which real-time cartography can be effectively provided by neural networks.
The MPTB project was successfully launched November 1997. Analysed telemetries after more than 3 years operation in orbit, proved that the executed ANN has successfully recovered from hundreds of Single Event Effects (Upsets and Latchups) which occurred on different circuits of the implemented architecture.

The effects of bitflips (SEUs) on neural boards were studied from flight data. During the whole mission time analysed, only a few times the output were faulty as the result of radiation effects: 7 times for board A, 15 times for board B. It is important to note that the ANN performances of boards A and B were affected in different ways by bitflips: the recognition rate never dropped under 60% (resp. 35%), the maximum drop (35%) occurred when a bitflip affected the T225 processor. Also it should be noticed that some bitflips resulted in the improvement of recognition rate (up to 80%).

The robustness of the on board ANN are respectively of 92% (7 times for 79 upsets) for board A and 90% for board B. But 2 facts contribute to the ponderation of these results, in one hand not all of the ANN parameters are effectively used for the network emulation, in other hand bitflips in the T225 during the neural network emulation are not take into account.

II-6.6.2 Study of the robustness of digital fuzzy control

Members: R. VELAZCO, S. REZGUI

In this project is investigated the intrinsic robustness with respect to Single Event Upset, of fuzzy control digital implementations. A commercial circuit dedicated to fuzzy control was used to implement the control part of a future ESA Mars instrument deployment vehicle. Upset fault injection experiments show the fault tolerance properties of the studied application.

Fuzzy control offers powerful solutions to a wide range of control problems. Some of them are difficult to be tackled by classical approaches because they resist appropriate mathematical modelling or require a highly non-linear reaction. Another typical difficulty arises when unexpected inputs push the controller far off the operating point where the underlying mathematical model becomes invalid. Fuzzy control shows good performances even in those cases, and it therefore has also been applied in space before.

We have investigated the effects of upsets on a fuzzy application built around a commercially available fuzzy processor, the WARP-2.0 (Weight Associative Rule Processor) from SGS-Thomson. Upsets were injected into a fuzzy model, designed for driving the motors of a Mars Instrument Deployment Device (IDD), to estimate its reliability in the destination environment.

Upsets simulations were performed on a bread-board including the WARP 2.0 which was developed as a prototype for an experiment in collaboration with CNES and NASA to be boarded on a scientific satellite: the Space Technology Research Vehicle (STRV-2) sponsored by the Defense Evaluation and Research Agency, (DERA, U.K.). The satellite carrying STRV experiments was launched end November 2000.

Studied fuzzy processor

The architecture of the chosen processor, the WARP 2.0, consists of 3 parts: an input stage, a processing stage, and an output stage. The input stage maps sensors or other inputs, such as switches, thumbwheels, etc. (8 bits digital input port) to the appropriate membership functions and truth values (Alpha Calculator, using the Antecedent Memory). The processing stage invokes each appropriate rule and generates a result for each one, then combines the results of all rules (Inference Unit, using the program and consequent memories). Finally, the output stage converts the combined result back into a specific control output value (Defuzzifier) and exports it by a digital way (8 bits Output port).
The WARP 2.0 processor has two operation modes:
- 8 inputs, each with 8 Membership Functions (MFs), and 4 outputs; or:
- 4 inputs, each with 16 MFs and 4 outputs.

Running WARP 2.0 involves a downloading phase and an on-line phase. The downloading phase allows the configuration of the processor in terms of I/O number, universe of discourse, MFs, and rules. During this phase, WARP 2.0 loads the micro-code in its internal memory. This micro-code which drives the on-line phase is generated by a compiler provided by STMicroelectronics. After that, WARP 2.0 is ready to run (on-line phase), processing inputs and producing the related outputs according to the configuration set in the downloading phase.

**Application under test**

The exploration of planet Mars is a challenging task. The IDD robots (rovers) sent to MARS have to fulfill special requirements. They must be very light, as they are transported by a lander on the surface of the planet. The equipment on the rover is used only for the collection of probes or experiments, therefore there is no sensor available for autonomous navigation. Due to the harsh climate conditions the rovers drive only during the day. The communication between the rover via the lander and the control tower on earth is done once a day in a very narrow time gap. Thus have to be short and effective. The Institute for Space Simulation (DLR, Cologne) has developed a 7 kg rover for such experiments. Based on a 3D image received from the lander, the operator on earth sends a number of commands defining the path of the vehicle. The proper execution of the given actions can only be verified a day later when the next 3D image is available. As the whole exploration on Mars takes only a week or two, it is very important that the trajectories sent are followed by the vehicle and thus only a reduced number of corrections is needed.

The application loaded on the WARP processor is the control process of steering the wheels of the Mars rover. The operator sends a trajectory to be followed by the rover. The geometric co-ordinates have to be converted into varying speeds and distances for each wheel of the rover. But wheels will slip on sand or slopes, and the motors may not exactly turn at the calculated speeds. Rather than to model these differences between geometric theory and sandy reality, we chose to implement the corrections on simple fuzzy controllers. Therefore the command is the same to all fuzzy controllers - 2 for each wheel- but the output a number of pulses for the motor is different for each wheel. The rules were determined by test runs of a prototype vehicle under typical conditions.

Two different fuzzy controllers, named FLC1 and FLC2 hereafter, were studied for the above presented application. Each fuzzy controller has 2 inputs and 1 output. The first fuzzy controller uses a reduced number of both membership functions and rules. It comprises 3 MFs for each input and output, and 9 rules. The second one has 8 MFs for each input and output and 64 rules. The linguistic labels for the input were chosen the same, thus we have symmetrical inputs (see also discussion). Figure II-6.8 shows the distribution and the shape of the MFs associated to the linguistic labels in the universe of discourse of the inputs and output.
Experimental set-up and obtained results

The hardware we developed to perform the upset injection experiments and the ground tests is based on THESIC system principles. It is composed of a "daughter board" built around the WARP fuzzy controller, a "mother board" based on a 8051 micro-controller for the control of daughterboard operation during the test under radiation and a PC for user interface. The daughterboard comprises mainly the WARP 2.0, logic glue, and clock system. Logic glue adapts the signals of the fuzzy controller to the bus of the mother board. The clock system uses a 12 MHz quartz (the maximum frequency allowed for WARP is 40 Mhz).

Evidence of the approach robustness with respect to upsets in the memories storing the fuzzy model, can be obtained by injecting errors using the experimental setup above described. For each of the bits of the WARP microcode associated with a fuzzy model, the completion of the following steps allows to identify the upset sensitive area within the WARP memories:
1 - inverting one bit of the WARP microcode,
2 - downloading the corrupted microcode within WARP,
3 - processing the outputs for the chosen pattern set,
4 - comparing the outputs with the expected values.

The injected errors provoked three types of behaviours:
A: correct value for all the tested inputs,
B: wrong values for at least one of the tested inputs,
C: no response (within a fixed time-out).

The main robustness features of the two studied fuzzy controllers (FLC1 and FLC2) extracted from obtained results, can be synthetised as:
- 257 bits (resp. 1113 bits) may be flipped without consequences at the controller behaviour. SEUs on 41% (resp. 33%) of the memory containing relevant data (FLC microcode) are totally effectless.
- 356 bits (resp. 2235 bits) should result in erroneous rover wheel's commands. However, upsets on part of these bits could be considered as tolerated because they result in a deviation considered
neglectable with respect to the reference command value. For the studied fuzzy controllers, 18% (resp. 29%) of the 5889 (resp. 32095) provoked errors when processing 108 (resp. 256) inputs coming from sensors. But the error deviation is less than 10%. For the rover control, commands is output can be considered tolerable. Detailed analysis of the obtained output set leading to determine the "wrongness" or the "quality" of the error will be presented in the final paper.

- SEUs on only 5 of the 30 bits of a register bank used to define the WARP configuration, result in system crashes (loose of WARP control). This unexpected robustness of a potentially critical area, probably due to an architectural reason, is presently under study.

**Robustness mechanisms**

We have attempt to identify the mechanisms inherent to fuzzy control strategy which leads to its robustness with respect to upsets errors. They depend on both the memory corrupted and the format used to store the fuzzy model. For the WARP architecture upsets on the membership function memory provoke: (a) changes in the slope of or (b) shifts of the abcisse of the MFs top. This leads to a "mutant" fuzzy model. From our experiments, the more serious consequences arise when such "mutant" model presents "holes" in the univers of discours (c). Figure II-6.9 illustrates these cases.

![Figure II-6.9 Fuzzy model modifications due to upsets](image)

The satellite STRV intended to carry the TIMA/NASA fuzzy logic experiment was successfully launched in 2000. Owing to a non identified problem, the 10 experiments on board STRV could not be powered. The high interest manifested by space agencies for the implementation of robust and performant control using fuzzy logic technics led to consider the inclusion of the fuzzy experiment in a futur space project: the Space Environment Technology (SET) project intended to be launched in satellites of NASA Living With a Star (LWS) project. First launch of SET/LWS project is forecasted in 2003.
II-7 Multidisciplinary projects

Beyond several research topics addressed jointly by members of 2 or more groups of the Laboratory, there are 3 large multidisciplinary projects ongoing. There are addressed in the following.

II-7.1 Global simulation of SOCs including MEMS and MOEMS

Members: MCS ans SLS groups
Editor: G. NICOLESCU, SLS group

This multidisciplinary project involves the Microsystems (MCS) and System Level Synthesis (SLS) Groups. It addresses the validation by simulation of heterogeneous SoCs including MEMS and MOEMS.

II-7.1.1 SOCs design including MEMS and MOEMS

Today’s embedded systems are getting more and more heterogeneous including multi-domains (electronic, mechanical, and optical) components. Systems such as MEMS (micro-electro-mechanical systems) are moving from abstract ideas to marketable products e.g. switching, scanning, projection, printing, etc. Illustrative examples are the optical switches that are becoming increasingly popular due to the many advantages that they propose over typical fiber optic switches. A generic 4x4 Optical Switch is shown in Figure II-7.1.1. The switching is achieved through the mechanical movement of mirrors steering the data path to the desired output. With the advancement of micro-electro-mechanical systems (MEMS) technology, these switches have become a reality, as the switches are small, fast, reliable, and eventually, very cheap to produce.

![4x4 Optical cross connect switch](image)

**Figure II-7.1.1 4x4 Optical cross connect switch**

To cope with their complexity, the MEMS/MOEMS design cycle starts with a high level specification, moving through several refinement stages to the final implementation. At any point in the design cycle, different parts of the design could be modelled at different abstraction levels. For example, mechanical actuators could be well characterized, while the electronic control might only be defined at a high-level.

In such a design flow there is a need for early validation of each of the design choices. Therefore, an efficient approach for heterogeneous system validation is based on the joint simulation of the different parts of the system utilizing simulators and abstraction levels appropriate to each component at its current level of refinement. This kind of simulation is called cosimulation.

The cosimulation of MOEMS/MEMS requires complex simulation models for the global validation. Building such simulation models is a very fastidious work that represents a source of errors and loss of design time. For these reasons, currently validation is a bottleneck in the design cycle, most of efforts (50%-80%) being devoted to it.
In this context, most of the simulation literature addresses the automatic generation of simulation models for global validation of heterogeneous systems. To our knowledge none of the existing environment or methodology takes into account all the problems implied by the systems heterogeneity: the adaptation of different abstraction levels, different communication protocols and different simulators.

II-7.1.2 Automatic generation of simulation models for global validation of SOCs including MEMS and MOEMS

Our methodology for the automatic simulation models generation is based on a generic simulation model, where the different components of the system are connected by a cosimulation bus via cosimulation interfaces. Figure II-7.1.2 illustrates a heterogeneous specification and its corresponding simulation model. The 2 modules in Figure II-7.1.2a may be described in different languages or at different abstraction levels. In the simulation model illustrated in Figure II-7.1.2b the cosimulation interfaces adapt the different specification languages, the different abstraction levels and/or the different communication protocols.

To enable automatic generation we defined a generic internal structure for the cosimulation interfaces represented in Figure II-7..b. As shown in this figure, a cosimulation interface is composed of two main modules:

1. The adapter of the simulation environment that enable the connection of a simulator to the cosimulation back-plane, but an eventual adaptation of abstraction levels or communication protocols is not yet addressed in this module.
2. The communication adapter that adapt different abstraction levels or communication protocols. This module is a hierarchical module composed of to types of components
   a. module adapter that is specific to the module that we have to adapt.
   b. channel adapter specific to a communication channel. For each channel connected to the module we assign a channel adapter.

This structure of cosimulation interface allows us to combine easily different simulators, modules and communication channels. For instance when one module is replaced by another and the communication is still the same, only the module adapter have to be replaced. If the new module is specified using an other specification language, the simulator adapter will be changed also.

![Figure II-7.1.2 Generic simulation model for heterogeneous SoCs](image)

Cosimulation interfaces are designed automatically by assembling elements from a cosimulation library. The cosimulation library contains simulator adapters, module adapters and channel adapters.
Figure II-7.1.3 illustrates a general view of our flow for automatic generation of simulation models. The input of this flow is the system specification. In a first stage, the specification is analyzed and all necessary adaptations for the simulation of the input specification are detected. Once the necessary adaptations are detected, the right elements are selected from the library and the cosimulation interfaces are built. Then the different modules of the input specification are connected through cosimulation interfaces in order to obtain the simulation model of the system.

![Diagram of the flow for the automatic generation of simulation models]

**Figure II-7.1.3 Flow for the automatic generation of simulation models**

### II-7.1.3 Global simulation of an Optical MEM Switch

We used our methodology to the validation of an optical MEM switch illustrated in Figure II-7.1.4. The system is composed of three main parts:

- The control sub-system that will be finally mapped on a processor. It calculates electronic orders (voltage) commanding motion of the mechanical mirrors of the optical sub-system.
- The optical sub-system is composed of a 2x2 mirror array, two sources and two photodetectors. Four lenses are used to collimate or focus the light.
- The electro-mechanical actuators transform the voltage from the output of the control sub-system into mechanical orders, in terms of positions, for each of the mirrors.
Each module of the system was designed by a different team. These teams cooperated only to fix the global functionality and any team took into account the communication abstraction levels or the simulation environments used for the modules designed by other teams. The electro-mechanical actuators were specified using Matlab/Simulink, the control part in SystemC and the optical sub-system in C++. The optical sub-system and the electro-mechanical actuators used different communication protocols.

**II-7.1.4 Conclusions and further developments**

This work is a result of the cooperation between the Microsystems (MCS) and System Level Synthesis (SLS) Groups. The unification of the competences of these groups allowed the application of a methodology for heterogeneous SoCs validation for MEMS/MOEMS. We believe that cosimulation can be used for even more sophisticated applications.

Further developments will focus on:

- Evaluating our methodology by applying it for more complex application including several IPs, digital components and MEMS/MOEMS.
- Adding new library elements in order to include existing CAD for optics for a better exploration of optical devices performances (e.g. ASAP).
- Enabling the joint fault simulation of MEM/MOEM sub-systems with the rest of the system. This implies providing adequate fault models for these types of sub-systems that can be simulated using a standard Hardware Description Language. In addition, the possibility of automatically generating MEM/MOEM models must be exploited here to produce realistic faulty behavioural models that can be readily simulated within the overall system. This is essential to deal with the extremely time expensive task of fault simulation.
- Coupling heterogeneous simulation tools with different resolutions (e.g. mesoscopic electric transport & intra-molecular transport) for molecular electronics simulation.
These developments will help to move towards the design of System on Chips including various components as they are depicted in Figure II-7.1.5.
II-7.2 WUCS: Wireless Universal Control Systems

Members: all groups  
Editor: M. RENAUDIN, CIS group

The WUCS project emerged from a consensual idea of conducting at TIMA a collaborative research work on an advanced high technological system, involving the top level research activities carried out at TIMA. The project's goal is to create the conditions of a fruitful interaction between researches having a high level of knowledge in different but related scientific domains. Every group leader adheres to this idea and is convinced that such a project is stimulating knowledge and innovation. Besides, such a project gives to the research groups the opportunity to contribute to a wide scientific spectrum collective work, valorizing the sharp and deep skills they develop.

The WUCS concept is definitely in the straight line of the emerging "ambient intelligence" paradigm. It is a wireless, communicating, multi-sensor system, embedding powerful computing capabilities. It is a smart device, part of a distributed network, interacting with its environment and providing services in a general sense to users or other devices. Therefore, WUCS is a system able to capture information, to recognize and identify its environment, and securely exchange information through wireless communication links. It should be autonomous, embedding its own source of energy. It is then characterize by three essential functionalities:

- automatic recognition of its environment,
- wireless communication with other WUCS devices,
- secure storage and exchange of data,
- autonomy.

Hence, WUCS is an heterogeneous system, that may include hardware/software, analog/digital, electrical/mechanical parts, all adapted and tuned to the targeted services/applications.

The design of such a smart device requires a tremendous amount of knowledge in different scientific fields, ranging from computer science and networking to physic and nano-electronic. The following competences developed at TIMA will contribute to the WUCS project:

- formal modeling and verification,
- hardware/software, continuous/discrete and electrical/mechanical co-simulation,
- test and qualification of integrated systems,
- high level synthesis, hardware/software co-design,
- radio-frequency system design,
- low-power digital and mixed circuit design,
- sensors, actuators and micro-systems design (mems).

As the first step and proof of concept, an instance of a WUCS is being designed. It integrates some of the key functionalities previously described. Pushing this work until the fabrication of a prototype is considered as essential. There is here a difficult tradeoff which consists in designing a real object to master the technologies and prove the concept without ambiguity, while focusing on research activities and not spending too much resources in pure development efforts.
II-7.3 Architectures based on quantum effects

Members: F. Ciontu, C. Cucu, B. Courtois, PH. Jorrand, B. Barbara

Editor: F. Ciontu, MCS group

The advent of nanotechnologies will make quantum effects play a primordial role in the functioning of the next generations of computation devices. Considered today a problem from the perspective of deep submicron CMOS miniaturization, quantum effects will gradually become technological concepts on which the "alternative" devices will rely and eventually will provide the physical support for a new algorithmic concepts in quantum computation. A prospective study performed at TIMA analyzed the state of the art technologies based on quantum effects, the proposed architectures based in these devices and the changes in terms of computation model (Figure II-7.3.1a). A convergence toward molecular electronics resulted from the cumulated effect of scientific, technologic and economic factors.

The research on nanosystems developed at TIMA is currently focused on the architectures based on quantum dot cells. This research takes place in the framework of a multidisciplinary project between TIMA, LEIBNIZ Laboratory (theoretical computer science) and Louis Néel Laboratory (physics) (Figure II-7.3.1b). The work on architectures at TIMA is coupled with the investigation of the decomposition of quantum algorithms performed at LEIBNIZ and the molecular implementation of the quantum cells (Louis Néel Laboratory).

II-7.3.1 Quantum Cellular Automata

The quantum cellular automata have been proposed since the middle of the 90's as an alternative technology to CMOS. Of an appealing simplicity, the model takes as basic brick a four dots quantum dots cell with two excess electrons. The two configurations corresponding to the minimal energy states are presented in Figure II-7.3.2a.

Both classical and quantum computing can be implemented on this model. For quantum computing a register consist of an N-cells row. The initial state of the qubits is prepared by forcing their polarizations by an external polarization. The evolution of the state of each cell is controlled by the

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1 LEIBNIZ Laboratory, Grenoble, France
2 Louis Néel Laboratory, Grenoble, France
same polarization and by the potential barriers between dots. Thus, rotations of the state vector of each cell are possible and the state of a qubit will evolve as a coherent superposition of two states depicted in Figure II-7.3.2a.

![Quantum gates](image)

**Figure II-7.3.2**

For classical computing the same cells can be deposited on a regular lattice. The polarization of a cell is strongly coupled with that of its neighbor cells. The topology of the cells will determine the logical function implemented. The NOT and MAJORITY gates illustrated in Figure II-7.3.2b,c constitute a universal logic gate set. Classical computing on a quantum cells array is governed by two principles: ground-state computation and edge-based computation. The polarization of the cells of one edge of a cell array is forced to an input value. The signals propagate towards the opposite edge through polarization switching while the array is relaxing into the ground state.

**Application-specific regular architecture for Quantum Cellular Automata**

An architectural assessment led to the conclusion that a direct transposition of a generic IC architecture on a QCA technology is rendered inadequate by several issues which are either characteristic to the model itself or specific to molecular implementation. Thus, the field-based interaction mechanism specific to the QCA model constitutes a serious architectural drawback because it implies localization in the device-device coupling and sets a planarity constraint for the interconnection of the logic devices. Further, direct simulation, apparently the only method to predict the behavior of an arbitrary array, is prohibitive for large arrays making infeasible cell level optimizations. Another drawback is constituted by the extremely high redundancies introduced when applying fault-tolerance techniques on arbitrary Boolean logic networks in the context of the statistical yields with a 1-10% defect rate induced by the use of the self-assembly in molecular implementations. Estimations of the cumulative effects (Figure II-7.3.3a) presented above show densities below those envisioned for the CMOS parameters in reach of the ITRS roadmap for generic architectures.

On the contrary, the QCA model is very well suited to the mapping of problems with intrinsic regularity. This has constituted the motivation for an application-specific architectural approach based on regular blocks. The proposed architecture consists of a lattice with two types of cell blocks: functional blocks and connection blocks (Figure II-7.3.3b). The functional blocks are placed in a rectangular array and are connected to each other through connection blocks. A functional block consists of memory cells, at the interior of the block, and interface cells, at the exterior of the block. The set of polarizations of the memory cells gives the internal state of the block. The connection blocks allow reciprocal interaction between neighboring functional blocks. The signal propagation is controlled through a clocking mechanism.
A methodology for automatic rule extraction was developed in order to allow mapping of regular problems on this architecture:

- Generation of the initial set of configurations and computation of the intermediary transition functions
- Partitioning of the space of internal states in order to control the redundancy in state representation and allow for fault-tolerance.
- Basic logic rules extraction
- Rules taxonomy from a geometrical and functional point of view in order to implement successive transformations of the array state.

This methodology has been applied to the mapping of image treatment algorithms on the proposed architecture. A systematic study of the regularity in various application classes and the conception of a composition mechanism of blocks of basic rules will be performed in the next development stage.

II-7.3.2 Architectures for mixed classical/quantum computing

Implementing mixed classical/quantum computation on a homogenous support may offer solutions of two of the core problems of quantum computing: inherently bounded coherence times limiting the data size and the number of operations performable in a quantum algorithm and the cooperation between classical and quantum algorithms required by the probabilistic nature of the quantum algorithms.

The concept of mixed classical/quantum architecture relies on the possibility of implementing Boolean logic as well as quantum logic by using the quantum cells. This property allows one to use a large number of quantum registers of limited size coupled to a network of classical cells whose topology implements Boolean logic functions (Figure II-7.3.4e). The coherence constraint is posed on each of the quantum registers independently of the other registers.
The definition of the architectural model consists of several intermediate level problems:

1. Optimized application of unitary transformations on the quantum registers - a study of the expression of abstract quantum algorithms in terms of a set of quantum gates optimized for a specific architecture. The optimal logic sets explored here are based on a molecular implementation based on homometallic binucleated complexes (Figure II-7.3.4 a,b).

![Diagram of molecular implementation of a quantum cell and a qubit.](image)

**Figure II-7.3.4**

2. Coupling of the quantum registers with the classical network - the quantum/classical coupling being equivalent to a measurement it must be controlled such as the presence of the classical network be non-invasive while the quantum operations are being performed and efficient enough after their completion.

3. The automated synthesis of the classical logic network

**II-7.3.3 Further developments**

Further developments will be focused on global optimizations of the mapping of quantum algorithms on cellular architectures and will be correlated with the research at LEBNIZ on the development of a language adapted to the mixed classical/quantum semantic. Studies on decoherence during the application of quantum gates on nanospins qubits will be performed in cooperation with Louis Néel Laboratory. A new project will be started in the second quarter of 2002 on CAD for molecular electronics in collaboration with LPMMC, a theoretical physics Laboratory located in Grenoble. This project targets the application of advanced engineering and CAD methodology techniques in modeling the electronic structure and characterizing the conductance of complex molecules and automatic exploration of molecular spaces for intramolecular integration of logic functions.
III - SERVICE ACTIVITY

The Laboratory is hosting the CMP Service Activity.

**CMP**


**Introduction**

The CMP project (Circuits Multi Projets) is a project undertaken since 1981 by the Laboratory. In 1984, the service became a “Unité de Service et de Recherche”, depending on CNRS and INPG. This project allows the Universities, Research Laboratories and Companies to fabricate the Integrated Circuits, Microsystems and Multi Chips Modules they have designed. Fabrication is for prototypes or low volume production. The originality of the project consisted initially in the regrouping, on the same slice of silicon, of a large number of circuits. Thus accessible costs of fabrication are obtained.

Since 1981, 520 Institutions from 60 countries have been served, about 3600 projects for Research, Education and Industry have been prototyped through 390 runs, and 40 different technologies have been interfaced.

For each project the operations to be achieved are the following:
- collection of circuits described in a common language
- checking of the circuits (syntax checking and design rules checking)
- assembly in macro-blocks (sets of chips)
- generation of the entry connections for the manufacturer
- subcontracting the fabrication of the circuits
- subcontracting the post processing (if any, for Microsystems)
- subcontracting sawing and packaging of the chips
- delivery of chips to the end users.

In parallel CMP distributes the design rules for each technology and the standard cell libraries for each specific software tool (design kits). CMP handles about 40 different design kits corresponding to the different technologies and CAD tools. They are sent to customers upon signature of a Confidentiality and Licence Agreement. About 520 customers have already signed the agreements and received the kits.

**Development since 1981**

Since 1981 390 fabrication runs have been undertaken. The complexity of the circuits has passed from several thousands transistors in 1981 to hundreds of thousands transistors in 1985 to now reach millions of transistors. NMOS technologies were used from 1981 to 1986 and CMOS from 1984. Advanced technologies have been proposed as early as 1994 for 0.5 CMOS TLM and 1999 for 0.18 CMOS 6LM and 0.8 SiGe BiCMOS. In 2000 SiGe 0.35 BiCMOS and SOI/SONS 0.5 CMOS were launched. And finally in 2001 0.12 CMOS 6LM was started. Access to Multi Chips Modules was open.

\(^1\) A specific report is available upon request.

\(^2\) On leave from November 2000 to August 2001.
in 1992. GaAs technology was introduced in 1993 and manufacturing of Microsystems was offered since 1995.

Table III-1 presents the Institution from France (III-1-a) and foreign countries (III-1-b) which submitted circuits from 1981 to 2001.

About 3600 circuits were manufactured since 1981. Table III-2 gives an overview of the different manufacturing runs.

In 2001 first fabrications were launched in 0.18 CMOS and 0.5µ SOI/SOS CMOS. The technology 0.12µ was introduced. CMP is the only service in the world offering such advanced technologies for prototyping and low volume.

**CMP projects in 2001**

In 2001 about one hundred Institutions (Universities, Research Laboratories and Industrial Companies) from France and 23 foreign countries submitted 277 circuits for education, research and industrial purposes. Hereafter are the technologies used in 2001:

For Integrated Circuits:
- 0.8 µ, 0.6 µ CMOS DLP/DLM from Austriamicrosystems
- 0.35 µ CMOS DLP/4LM from Austriamicrosystems
- 1.2 µ, 0.8 µ BiCMOS DLP/DLM from Austriamicrosystems
- 0.8 µ HBT CMCS (SiGe) from Austriamicrosystems
- 0.25 µ CMOS 6LM from STMicroelectronics
- 0.18 µ CMOS 6LM from STMicroelectronics
- 0.5 µ SOI/SOS CMOS from Peregrine Semiconductor
- 0.2 µ GaAs HEMT from OMMIC

For Micro Electro Mechanical Systems:
- 0.8 µ, 0.6 µ CMOS DLP/DLM from Austriamicrosystems, compatible front-side bulk micromachining
- 0.8 µ BiCMOS DLP/DLM from Austriamicrosystems, compatible front-side bulk micromachining
- 0.2 µ GaAs HEMT from OMMIC, compatible front-side bulk micromachining
- Multi-User MEMS Processes (MUMPs) from CRONOS, three-layer polysilicon, surface micromachining

**Type of circuits and evolution 1997-2001**

Figure III-1 shows the evolution in total number of circuits manufactured per year. From 1994, about 300 circuits are manufactured every year.

Figure III-2 shows the distribution of circuits per technology during the four last years. CMOS technology remains the most used technology (64% of the circuits in 2001, same as in 2000), the part of BiCMOS is growing (23% instead of 17%). These two types of technologies cover 87% of the total circuits manufactured.

Figure III-3 shows the distribution of circuits depending on the purpose: research, education or industry. In 2001 the percentage of industrial circuits passed from 16% to 27%. The percentage of circuits for education is stable at 18%.
Figure III-4 shows the year of arrival on the market of the different CMOS technologies (source: Semiconductor Industry Association), given by the good size in microns, and the technologies used by CMP. Both curves have now converged. This means that CMP continues to use the most advanced CMOS technologies as soon as they are introduced.

**Participation of Industry**

In 2001, 74 industrial circuits, 40 from France and 34 from foreign countries, were fabricated for 29 industrial companies or national research laboratories. This is an important increase compared to 2000 and industrial circuits now represent more than 25% of the total number of circuits. They were manufactured for prototyping (44 circuits) or low volume production. (32 circuits from 30 to 70,000 pieces).

Figure III-5 shows the development of low volume production since 1994. In 2001 twenty Institutions submitted circuits for low volume production.

**Micromachining Program**

CMP has been the first non-US multi-project-wafer service to introduce Microsystems manufacturing, as early as 1995. Two types of technologies are proposed. One is fully compatible with microelectronics processes, and allows the monolithic integration of microstructures and electronics circuitry (front side bulk micromachining). The technologies used are CMOS and BiCMOS from Austrianmicrosystems and HEMT GaAs from OMMIC. Applications are thermal sensors, mechanical sensors (acceleration, force, pressure), etc. The other is specific to MEMS structures and is provided by CRONOS (surface micromachining). It is used in particular for micro motors, micro mirrors, etc.

CMP distributes MEMS design kits for the main EDA vendors (CADENCE, Mentor Graphics, etc.). They are used to fabricate microstructures such as accelerometers, gas flow sensor, electrothermal converters, infrared detectors, etc.

**Agreements with other services in the world**

CMP has signed cooperative agreements with the following Institutions:

- CIC, Taiwan
- FAPESP, Brazil
- Royal Institute of Technology, Sweden
- Southeast University, Nanjing, China

CMP has signed distribution agreements with the following Institutions:

- ISD, Australia, New Zealand
- ALT-S, The Middle East
- Lumbini Technologies, India
- SPS-DA, Singapore, Malaisia, Thailand
- C.T.A Engineering Pte Ltd, Singapore

In addition in 2001 the three main ICs manufacturing services from USA (MOSIS), Canada (CMC) and France (CMP) started a partnership in order to exchange some of their services and to enlarge the portfolio of technologies proposed by each partner.
Multi Chip Modules

CMP introduced MCM services in 1992. Agreements were signed with different manufacturers of MCMs, depending on the type of MCM (L, C, D, V). As an example an industrial MCM project designed to work in a harsh environment was manufactured in technology MCM-L of BULL, using TAB-Bumpless for assembly, followed by a production of about 100 pieces per year.

CAD tool offers

CMP distributes and supports several CAD softwares for Universities or companies. More precisely CMP has agreements with:

- Tanner Research, Inc. to distribute the L-edit layout editor and the T-Spice simulator, for University and Industry

- Cadence Design Systems, Inc. to distribute Cadence products (ASIC Front-end and Back-End) to educational institutions and authorized research laboratories. Products are delivered for non-commercial educational and research purpose only.

- Answer Systems company to offer the package HDL-designer/ModelSim/Leonardo to academic Institutions.

- ARM Ltd. to provide academic institutions with software and hardware materials developed by ARM for designing and manufacturing Systems on Chips based on RISC processor architecture. The goal is to give engineering students the up to date tools to gain skill and experience in systems development.

CMP also widespreads information on free software tools available from other services or Universities and distributes design kits for these tools.

Other activities

In addition to the manufacturing of circuits, various other tasks are carried out in order to develop specific tools, to answer specific needs or to gain new competences. That has been for example:

- the determination of the rules of multitechnological design,
- the development of translators for various IC descriptive formats,
- the development of tools to check or correct syntax descriptions,
- the development of design kits (CMP developed design kits for TANNER/L-Edit, EXEMPLAR/GALILEO, COMPASS, CADENCE, etc.).

In 2001 CMP cooperated with:
- The University of Budapest, Micred company and TIMA for the design of thermal test chips for package qualification. One of those designs has been awarded as the best "Operational Design" of the DATE'01 Design Contest in March 2001.
- ISL (Institut franco-allemand de Recherche de Saint Louis) for a IIR filter for noise cancellation. The circuit was designed by a collaboration between ISL and CMP with the participation of "Laboratoire EpF, Faculté des Sciences de Monastir", Tunisia. All the tests were successful and the circuit was fully operational.

Quality Assurance System

By the end of 1997, in order to increase and to promote the quality of the service, CMP began to implement the ISO9002 Quality Assurance standards. The quality assurance manual was written as
well as the various quality assurance procedures. The system was completely set up by mid 1998. During the two following years the various requirements of the Quality Assurance System were applied, and in June 2000 the service was assessed and got the certification «ISO 9002» (see the certificate at the end of the chapter). In June 2001 the certification was renewed.

Conclusion

France has been a pioneer country in this type of infrastructure since chip fabrication for Universities has been started in 1981 by CMP; the elementary CAD software LUCIE issued from the Laboratory was provided to 36 Academic Institutions in France and foreign countries in the 80s industrial CAD software was distributed to Universities in 1987 by CNFM and testing equipment was centrally purchased in 1988. As early as 1990 CMP opened chip fabrication services to Industry.

Finally in 2001 CMP continues to offer a wide variety of services to a lot of Institutions for academic and industrial purposes. The number of industrial circuits increased, both for prototyping and low volume production. New very advanced processes were introduced: 0.12μ CMOS and 0.35 SiGe BiCMOS which are among the most advanced industrial processes around the world. Important efforts were still going on to control and to improve the quality of the service.

These different achievements will be pursued in 2002, always with the objective to better satisfy the needs of the customers.

Figure III-1 – Total number of circuits per year, 1992 - 2001
Figure III-2 – Distribution of circuits per technology (4 last years)
Figure III-3 – Distribution of circuits depending on the purpose (2 last years)

Figure III-4 – SIA Roadmap and CMP technologies
Figure III-5 – Number of Institutions which submitted circuits for low volume production
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**Table III-1 (a) – French Institutions having submitted circuits to CMP**
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**Total in 2001:** 11 technologies 46 runs 277 circuits 4,060 mm²

**Table III-2 (b) – CMP runs in 2001**

**CMP runs total since 1981:** 403 runs

3,641 circuits: 1,866 Research circuits / 1,247 Educational circuits / 528 Industrial circuits
CERTIFICATION

N° QUAL/2000/14731
Le Système Qualité adopté par:
The Quality System adopted by:

CMP

pour les activités suivantes:
for the following activities:

FABRICATION DE CIRCUITS INTÉGRÉS ET DE MICRO-SYSTEMES EN PROTO TYPES ET PETITS VOLUMES POUR LES UNIVERSITÉS, LABORATOIRES DE RECHERCHE ET SOCIÉTÉS INDUSTRIELLES FRANÇAISES ET ÉTRANGÈRES.

MANUFACTURING OF INTEGRATED CIRCUITS AND MICROSYSTE M S IN PROTOTYPES AND SMALL VOLUMES FOR UNIVERSITIES, RESEARCH LABORATORIES AND FRENCH AND FOREIGN INDUSTRIAL COMPANIES.

exercées sur le(s) site(s) suivant(s):

46, avenue Félix Viallet F-38031 GRENOBLE CEDEX

Le(s) site(s) est(ont) conforme(s) aux exigences de la norme:

ISO 9002 (1994)

Le certificat correspondant a été édité dans les conditions d'application fixées par AFAQ le:

2000-07-06

2003-07-05

LE PRÉSIDENT DU COMITÉ DE CERTIFICATION

O. PEYRAT

Le Directeur Général d'AFAQ

Le Directeur Général de l'AFAQ

Le Président du Conseil du Certificat

A. PIGEONNIER

O. PEYRAT

B. COURTOIS

On behalf of the Firm
IV - RESOURCES

IV-1 Human resources

IV-1.1 Members of the Laboratory

Table IV-1 I lists researchers, engineers and clerical staff involved in the TIMA Laboratory throughout 2001 and Table IV-1 II points out researchers currently on secondment to French companies. The researchers working on a thesis in cosupervision figure in Table IV-1 III while those working in companies or abroad, but enrolled for a thesis in the TIMA Laboratory are respectively listed in Table IV-1 IV and Table IV-1 V. And last but not least Table IV-1 VI and Table IV-1 VII list researchers (visitors and trainees) who stayed in the Laboratory for a while.

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<td>5.5 months</td>
</tr>
</tbody>
</table>

Table IV-1 VII: Trainees (for 2001)
IV-1.2 Biographies of staff members
Paul AMBLARD

Born on February 25th, 1951
Married, 3 children
French

Education

1972    Master of Science in Mathematic
1984    PhD Computer Science

Position

Assistant Professor (Maître de Conférences) at University Joseph Fourier, Grenoble, UFR Informatique et Mathématiques Appliquées

Previous Positions

From 1973 to 1982    Teacher of Mathematics in secondary schools
From 1984    Assistant Professor at University Joseph Fourier
In October 1997    Joined TIMA Laboratory
Lorena ANGHEL

Born December, 9th, 1972
Single
Romanian

Education

1996 : Microelectronic Engineering degree - at Polytechnic University of Bucharest, Romania
1997 : MS degree in Microelectronics – UPB, Romania
2000 : PhD in Microelectronics (INP Grenoble)

Position

Assistant Professor (Maître de Conférence) at ENSERG (Ecole Nationale Supérieure d'Électronique et Radioélectricité de Grenoble) since 2001.

Research interests

Test, fault-tolerant techniques, computer architecture

Past activities

Contractual teacher (ATER) at UJF (Université Joseph Fourier Grenoble) in 2000.

Current responsibilities

Researcher in the « Reliable Integrated Systems » group (RIS)
Skandar BASROUR

Born: August, 24th, 1964
Married, two children
Italian and Tunisian

Education

1982 - 1986: Graduated from Ecole Normale Supérieure of Tunisia (Physics and Chemistry)
1986 - 1987: DEA in Microelectronics – Université Joseph Fourier de Grenoble
1987 - 1990: PhD in Microelectronics – Université Joseph Fourier de Grenoble

Position

2001: Professor in Electronics and Microsystems at the Institut des Sciences et Techniques (ISTG) de Grenoble. Electrical Engineering Department (3I).

Research interests

Design, realization and characterization of new Microdevices and Microsystems.
RF Microsystems, adaptive optics.
New microfabrication technologies for Microsystems, compatible with CMOS flow.

Past activities

1991 – 1992: Postdoctoral situation at the Laboratoire de Microstructures et Microélectronique CNRS – Bagneux (Topics: Fabrication and characterization of submicron gated TEGFET’s)

1992 – 2001: Assistant Professor in Electronics and Microsystems at the Université de Franche-Comté. (Topics: Contribution to the development of the X ray LIGA technique in France. Development and improvement of the UV LIGA Techniques for the realization of original Microsystems)

Current responsibilities

Researcher at the MiCroSystem group (MCS) on these topics:

RF Microsystems,
Adaptive optics,
Development of new microfabrication technologies for Microsystems compatible with CMOS foundries.

Management of the Sensor and Actuator characterization facilities at the EE department of the ISTG.
Dominique BORRIONE

Born February 20th, 1950
2 children
French

Education

1970:  B. S. in Applied Mathematics, Aix-Marseille University
1971:  DEA in Computer Science, University of Grenoble
1976:  PhD in Computer Science, University of Grenoble
1981:  Doctorat d’Etat in Computer Science, University of Grenoble

Position

Professor at Université Joseph Fourier, Grenoble

Past Responsibilities

Director of the ARTEMIS Laboratory (1991-1995)

Current Responsibilities

Leader of the Verification and Modeling of Digital Systems Group

Miscellaneous

* Has served in many Conference and Workshop Committees
* IFIP Silver Core
Wander OLIVEIRA CESARIO

Born August 17, 1968
Married
Brazilian

Education

1994 Master Degree - "Microeletronics Engineer" – Escola Politécnica da Universidade de São Paulo
1999 Ph. D. Degree - "Microeletronics" – INPG

Position

Researcher with TIMA.

Current responsabilities

Member of the System Level Synthesis Group
Benoît CHARLOT

Born June 6th 1972
Married, 1 child
French

Education

1990 Baccalauréat degree in mathematics and mechanical engineering
1995 Maîtrise degree in Semiconductor Science, University of Montpellier.

Position

Contractual researcher at TIMA

Current responsibilities

Member of the Microsystem group
Technical responsible since 1999 for the MEMS prototyping service at CMP.
Responsible for the European research project PROFIT.
Responsible for the MEMS Fingerprint sensor and active biochip projects.
Sébastien COLIN

Born July 4th, 1973
Single
French

Education

1992 : Baccalaureat degree in Mathematics and Technics
1995 : DUT in Electrical Engineering and Industrial Computer Science, Electronics option, at I.U.T. 1, Grenoble

Position

Contractual technician with CMP since August 1996

Current responsibilities

Data preparation ICs at CMP.
Bernard COURTOIS

Born April 17th, 1948
Married, 2 children
French

Education

1967 - Baccalaureat degree - Mathematics
1968 - Baccalaureat degree - Philosophy
1967 - 1970 Mathematics in Paris
1970 - 1973 National School for Informatics and Applied Mathematics in Grenoble
1973 - Engineer degree
1976 - Doctor-Engineer degree
1981 - Docteur d'Etat degree

Position

"Directeur de Recherches" CNRS

Current responsibilities

* Director of TIMA Laboratory
* Director of CMP Service

Miscellaneous

* Has authored or co-authored many scientific papers
* Has served in many Committees of Conferences & Workshops
* Has served as a reviewer of research proposals to CEC, NATO, NSF, SERC
* Doctor Honoris Causa of the Technical University of BUDAPEST
* IEEE Golden Core.
Hubert DELORI

Born December 26th, 1946
Married, 5 children
French

Education

1964 Baccalaureat degree - Mathematics, Lycée Claude Bernard, Paris
1964-1967 Mathematiques Supérieures & Mathematiques Spéciales, Lycée Janson de Sailly, Paris
1967-1970 Engineer studies at Ecole Centrale de Lyon, Ecullly
1970 Engineer degree from Ecole Centrale de Lyon.

Position

"Ingénieur de Recherche 1ère classe" at CNRS (Centre National de la Recherche Scientifique).

Past activities

70 - 71 : Analysis and programming at IBM, Corbeil-Essonnes
72 - 73 : Teaching in Mathematics and Statistics in Algiers, Algeria, as for the cooperation in place of the military service,
73 - 75 : Engineer statistician at "Cabinet Roland Olivier", Paris and Algiers: setting up a statistical method, based on aerial pictures, to realize a national inquiry of ground occupation for the Agriculture Ministry of Algeria. Experimenting this method by real enquiries in selected regions..
75 - 78 : Education of physically handicapped young people for social re-insertion at Association IMC Rhone Alpes, Lyon.
78 - 79 : Engineer at ICARE (Informatique Communale Alpes Rhône) at the town hall of Saint Etienne : operating responsible of all the informatic applications.
79 - 80 : Complementary studying in System Programming at "Institut de Programmation de Grenoble" (1 year).
80 - 83 : Analysing and programming of software tools for Computer Aided Education, in the group of Prof. P. C. Scholl, University Joseph Fourier, Grenoble.

From 1983 : Engineer at CMP (Circuits Multi Projets).

Current responsibilities

Quality management, coordination, and general information of the CMP Service (Circuits Multi Projets : National Service for manufacturing integrated circuits for Universities, Research Laboratories and Industrial Companies).
Grégory DI PENDINA

Born August, 11th 1979
Single
French

Education

1997: TI Baccalauréat diploma, in electrotechnics
1999: UT degree (Electrical Engineering and Digital Technology)
      Option: Electrotechnics, University Joseph Fourier of Grenoble, I.U.T.1
1999/2000: Préparation d'une "Licence Ingénierie Electrique"

Position

Contractual technician with CMP since November 1999
Sylvaine EYRAUD

Born March 23rd, 1970
Married, 2 child
French

Education

1989 : Baccalaureat degree in Mathematics and Natural Sciences
1991 : DUT in Computer Sciences
1994 : "Diplôme d'Études Supérieures Techniques d'informatique d'entreprises" (informatics for companies)

Position

Contractual technician with CMP since February 1993.

Current responsibilities

* Manufacturing run’s data management
Laurent FESQUET

Born May 10th, 1969
Single
French

Education

1993 : Engineering degree in Physics
Ecole Nationale Supérieure de Physique de Strasbourg
1993 : DEA degree in Photonics - ULP Strasbourg
1994 : Agrégation (teaching degree) in applied physics
Ecole Normale Supérieure de Cachan
1997 : PhD in Electronics - UPS Toulouse

Position

Assistant professor (Maître de conférence) at ENSERG (Ecole Nationale Supérieure d'Électronique et Radioélectricité de Grenoble).

Past activities

- Teacher at the French Navy instruction center in Toulon in charge of electronics and inertial navigation systems lectures (1994-1995)
- Contractual teacher in electronics at Sup'Aéro (Ecole Nationale Supérieure de l'Aéronautique et de l'Espace) (1995-1999)
- Teacher in charge of physics, electrotechnics and power electronics courses in BTS (technician degree) - Brive (1998-1999)

Current responsibilities

Researcher in the « Concurrent Integrated Systems » group (CIS)
Chair of the french IEEE-SSCS Chapter (Solid-State Circuit Society)

Miscellaneous

Has organized in 1997 a workshop on New Technologies, Interconnects and Communications in Distributed and Parallel Systems in Toulouse (France)
Has organized in 2000 the AcI-D-workshop in Grenoble (France)
Sébastien FILLION

Born October 14st, 1974
Single
French

Education

2000 : MST ESI (Maîtrise des Sciences et Techniques experts en système informatique) Université Joseph Fourier (Grenoble).
1997 : DEUG Technologie Industrielle Université Joseph Fourier.

Position

Contractual engineer with TIMA Laboratory since August 2000

Current responsibilities

System Engineer at TIMA Laboratory
Alain GUYOT

Born September 11th, 1945
Married, 3 children
French

Education

1970 - Master in Computer Science from Grenoble University
1975 - Ph.D in Computer Science from Grenoble University
1991 - "Habilitation à diriger des Recherches"

Position

Assistant Professor (Maître de Conférences) at ENSIMAG (Ecole Nationale Supérieure d'Informatique et de Mathématiques Appliquées de Grenoble) since 1986

Past activities

* Teacher in computer architecture and VLSI design mainly at ENSIMAG and Grenoble University since 1971
* Visiting scholar or invited professor with the CSL group in Stanford University (Prof. M. Flynn), Microelectronic group in Telecom University, Paris (Prof. Jutard) and LEPFL in Lausanne (Prof. M. Declercq)
* Author or co-author of more than 50 scientific publications in Journals, Conference Proceedings, or Research Reports
* Served as a reviewer for ESSCIRC, VLSI, Computer Arithmetic, EUROASIC, IEEE TC, CAVE and other conferences.
Ahmed Amine JERRAYA

Born August 1st, 1955
Married, 2 children
French and Tunisian

Education

1980 Engineer degree, Faculté des Sciences de Tunis, Tunisie
1981 DEA, Computer Science, Institut Polytechnique de Grenoble, (INPG), France
1983 Doctor-Engineer degree, Computer Science, INPG
1989 Doctorat d'Etat degree, INPG

Position

Research director with CNRS, the French National Center for Scientific Research. Section : Computer Science

Past Activities

- Participated to the LUCIE system, highly successful layout tools, distributed in the early 80s to 20 Laboratories in France and 17 abroad
- Led the AMICAL project, a highly successful architectural synthesis tool transferred to industry
- Led the COSMOS project, a powerful SDL-based Co-design tool transferred to industry
- Co-Founder of AREXSYS S.A., an EDA start-up
- More than 100 international publications

Current Responsibilities

- Leader of the System Level Synthesis Group of TIMA Laboratory

Miscellaneous

- General Chair of HLDVT'02, Cannes, France, October 2002.
- Co-Program Chair, CASES 2002, Grenoble, France, October 2002.
- Co-Director of the Application-Specific Multi-processor SoC Summer School, Château de Pizay, France, July 2002.
- European Representative at Executive Committee DAC 2002/2003.
- Secretary of EDAA, 2002/2003.
- Co-Director of the Application-Specific Multi-processor SoC Summer School, Aix-les-Bains, France, July 2001.
- General Chair of DATE 2001, Munich, Germany
- Co-General Chair of CODES'99, Rome, Italy
- Co-Director of NATO ASI School on System Level Synthesis, Il CIOCCO, Italy
- Program co-chair of CODES/CASHE'98, Seattle, USA
- General Chair of ISSS'96 Conference, La Jolla, CA, USA
- Program Chair of RSP'96 Workshop
- Technical Program and Organization Chairperson of ISSS'95 Conference, Cannes, France
- Spent one year at Bell Northern Research in Ottawa, Canada
- Several tutorials in international conferences (EuroVHDL, EuroVHDL-EURODAC, APCHDL, DATE, SDL Forum, ASP-DAC)
- Served in the Program Committee of ICCAD, DATE, ISSS, EDAC, High-Level Synthesis Workshop, EuroDac, EuroVHDL, VHDL International, APCHDL, CODES Workshop and ICCD.
- Award of "President de la République" in Tunisia, 1980, Best Computer Science Engineer Degree
Claude LE FAOU

Born May 20th 1938  
Married, two children  
French

Education

1956  
Baccalaureat degree - Mathematics

1956 - 1959  
Mathématiques Supérieures & Mathématiques Spéciales, Lycée Saint-Louis, Paris

1959 - 1962  
Engineer studies at "Institut National Polytechnique de Grenoble"

1962  
Engineer degree from INPG. Speciality: "Radioélectricité"

Position

"Ingénieur de Recherche" at CNRS (Centre National de la Recherche Scientifique)

Past activities

1964-1966  
Engineer in a private research Laboratory (LEAD) : Electronical design of a very high rapidity plotter

1966-1971  
Engineer at “Institut National Polytechnique de Grenoble”, Computer Science Department : Design and development of simulation programs at circuit level : IMAG1, IMAG2

1971  
Research Engineer at CNRS

1971-1981  
Research and development in the field of Electrical Simulation. Design and development of IMAG3, IMAG4

1974-1983  
Co-management of research team (15-20 persons) at IMAG laboratory

1981-1987  
Technical management of CASCADE project : CAD system for VLSI circuits and systems (20-25 persons)

1983-1987  
Staff member of ARTEMIS Laboratory

1987-1989  
Visiting Researcher at UFRGS, Porto Alegre, Brazil

1989-1994  
Research and development on man machine interface for integration of verification tools

1990-1994  
Joint Director of ARTEMIS Laboratory

Current responsibilities

Administrator of the research group VDS at TIMA Laboratory.
Régis LEVEUGLE
Born December 4th, 1964
Married
French

Education
1987 - Engineer Degree from ENSERG (INP Grenoble)
1987 - DEA Degree in Microelectronics (Grenoble)
1990 - PhD in Microelectronics (INP Grenoble)
1995 - Habilitation à Diriger des Recherches (French National Degree for Research Supervising)

Position
- Professor at INPG (ENSGER), Director of Studies at the INPG Department in Telecommunications.
- Joined Timas in December 1999 (Group "Reliable Integrated Systems").

Research interests
Computer architecture, VLSI design methods, fault-tolerant architectures, concurrent checking, test, logic implementations in nanotechnology.

On-going Research Activities
- Leader of a project on the predictive analysis of the erroneous behaviours of complex VLSI circuits, using multi-level fault injections. Participation to the ERC contract with STMicroelectronics.
- Preliminary studies on circuit design based on nano-electronic devices (SETs).
- General co-Chair for the IEEE Symposium on Defect and Fault Tolerance in VLSI Systems, Vancouver, Canada, 6-8 November 2002.
- Vice General Chair for the IEEE International On-Line Testing Workshop, Bendor, France, 8-10 July 2002.

Past Activities
- Participation to several European projects: ESPRIT 824 "WSI" (design of a defect-tolerant microprocessor), JESSI AC8 "Synthesis, Optimization and Analysis" (development of methods and CAD tools for synthesis of dependable circuits, including on-line test and fault-tolerance capabilities), JESSI T9 "Silicon Hybrids" (design of defect-tolerant programmable interconnection networks for MCMs with active substrates), ESPRIT MODEM (development of a multimedia demonstrator for microelectronics teaching), MEDEA T505 and T553 (definition and evaluation of approaches for optimised hard IP migration towards 0.18 and 0.15 micron CMOS technologies).

Miscellaneous
- Authored or co-authored more than 80 scientific papers in journals, books, conferences and workshops.
- Served in the Executive Committee of ED&TC and in the Programme Committee of EuroASIC, VLSI, ED&TC, DATE, FTCS, IOLTW, and DFT.
- Served as a reviewer for many international journals, conferences and workshops.
- Served as a consultant for LEAS, SEMA GROUP and XILINX.
Jean MERMET

Born: February 24th, 1942
Married, 2 children
French

Education

1958 Baccalauréat C, La Réunion
1958 Baccalauréat A, Grenoble
1959 Baccalauréat in Mathematics, Lyon
1959 Baccalauréat in Philosophy, Bordeaux
1966 Engineer degree, ENSIMAG, Grenoble University
1967 Master degree in Mathematics, Grenoble University
1970 "Docteur-Ingénieur, Grenoble University
1973 "Docteur d'Etat", Grenoble University
1977 DESS degree in Economy, Grenoble University

Position

"Directeur de Recherches" CNRS

Previous positions

- July 1966 to August 1968 Research Engineer
- May 1974 to May 1978 "Délégué aux Relations Industrielles en Rhône-Alpes"
- June 1980 to June 1983 Head Department ENSIMAG of IMAG
- February 1983 to October 1985 European CERES Project Manager
- January 1984 to December 1987 Director of ARTEMIS Laboratory
- January 1988 to December 1989 "Directeur Scientifique et des Applications de la Recherche" of the Mediterranean Institute of Technology
- October 1988 Director of "UMS 815" CNRS
- Since July 1991 "European Chips and Systems design Initiative"

Responsibilities

- Founder and General Secretary of Association MICADO (1974 to 1986)
- Expert to the CEC (2 years)
- Member of the Board of INPG (1 mandate)
- Member of the Scientific Council of INPG (2 mandates)
- Member of IFIP WG 5.2 et WG 10.2 (since 1976)
- Co-Chair of the IEEE VHDL Analysis and Standardization Group (since 1990)
- Chairman of the European (ESSI) HDL Standardization Group (since 1990)
- General Chair of EuroVHDL Conference (1992, 1993)
- General Chair of the EuroDAC Conference (1994)
- General Chair of the APCHDL Conference (1995)
- General Chair of the EDA Standards Summer School (1996)

Miscellaneous

- COMPUTER Society Golden Core Member (1996)
- Meritorious Service Award IEEE (1995)
Salvador MIR

Born September 21st, 1963
Single
Spanish

Education

1987 - Industrial Engineering degree - Electrical, Polytechnic University of Catalunya, Barcelona, Spain
1989 - Master degree - Computer Science, University of Manchester, United Kingdom.
1993 - Ph.D. degree - Computer Science, University of Manchester, United Kingdom

Position

Chargé de Recherches CNRS

Past activities

1993 - 1994 Postdoctoral researcher with TIMA
1995 Contractual researcher with TIMA
1996 - 1997 Contractual researcher with Centro Nacional de Microelectrónica, Seville, Spain

Miscellaneous

* Has published 80 scientific papers in international journals, conferences and workshops
* Award from Association of Industrial Engineers of Catalonia, Spain, to the best Work Graduation Dissertation in Industrial Engineering, Barcelona, 1988
* Member of IEEE and IEEE Computer Society
* Participation in the European projects SMART, JESSI-COMMON-FRAME, ARCHIMEDES, AMATIST, PROFIT, TECHNODAT
* Regular reviewer for International Journals and Conferences
Mihail NICOLAIDIS

Born April 22nd, 1954
Single
French and Greek

Education

1978  Engineer degree- Mechanical-Electrical, Ecole Polytechnique de l'Université de Thessaloniki.
1981  DEA Electronical, Institut Polytechnique de Grenoble (ENSERG).
1984  Doctor-Engineer degree - Data processing
       Design of self-testing integrated circuits for analytical failures hypotheses.

Position

"Directeur de Recherche" at CNRS

Current responsibilities

- Responsible of the Reliable Integrated Systems Group of TIMA Laboratory
- General Co-Chair of 1997 IEEE International On-Line Testing Workshop
- Program Co-Chair of 1997 IEEE VLSI Test Symposium
- Program Chair of 1998 IEEE VLSI Test Symposium
- General Chair of 1999 IEEE VLSI Test Symposium
- 2nd Vice-Chair of IEEE Computer Society Test Technology Technical Committee (TTTC)
- Chair of Technical Activities TTTC.

Miscellaneous

Co-founder of iROC
Pierre OSTIER

Born February 5th, 1968  
Single, three children  
French

Education

1992  DEA in Computer Science, INPG, Grenoble, France.  
1997  PhD in Computer Science, University of Grenoble, France.

Position

Contractual Research Engineer with VDS.

Current responsibilities

- Design and development of compilers for the vhdl language for formal verification.

- Integration of formal tools for hardware verification and diagnosis in the Prevail environment.

- System administration of VDS machines
Jean-François PAILLOTIN

Born October 6th, 1955
Single
French

Education

1978 - Licence Telecommunications - Reims University
1979 - Licence Computer Sciences - UJF Grenoble
1980 - Master Degree Computer Sciences - UJF Grenoble
1981 - DEA Computer Sciences - INP Grenoble
1984 - Doctorate Computer Sciences - INP Grenoble.

Position

Present position: "Ingénieur de Recherche" National Education

Before:
* LCS researcher, INP Grenoble
* Assistant Teacher at IUT of Computer Sciences, Grenoble
* Assistant Teacher at UJF.

Current responsibilities

* Technical responsible since 1985 for the CMP (Circuits Multi Projets) : national Service for Universities, Research Laboratories and Industry
* AMS CUP runs, ST HCMOS8 runs and PML runs responsible
* ACMO (Agent Chargé de la Mise en Œuvre de l'hygiène et de la sécurité)
Marc RENAUDIN

Born March 29th 1963
Married, 3 children
French

Education

1987 : Engineer and DEA Degrees in Signal Processing INPG.
1990 : PhD in Microelectronics and Signal Processing – INPG.
1998 : Habilitation à Diriger des Recherches (French National Authorisation to Supervise Research) – INPG.

Position

Professor at ENSERG (Ecole Nationale Supérieure d'Electricité et Radioélectricité de Grenoble).

Current Responsibilities

Leader of the "Concurrent Integrated Systems" group (CIS).

Past Responsibilities

Assistant professor at Telecom Bretagne (1990 – 1998)
In charge of the Grenoble Entity

Scientific Activities

Has visited Caltech in 1995, Computer Science Department, Professor Alain Martin's group.
Has managed Mica and Micabi projects on the design of a CISC 8 bit asynchronous microprocessor and its integration in a Contactless Smart Card IC using an on-chip antenna.
Has managed the ASPRO project, "A Standard-Cell Q.D.I. 16-Bit RISC Asynchronous Microprocessor".
He is currently working on the TAST project (Tima Asynchronous Synthesis Tools). This project’s aim is to provide an open framework for the design of asynchronous circuits (clock-less circuits) as well as mixed synchronous/asynchronous circuits.
Has served as a reviewer for IEEE JSSC, TC and Micro, ASYNC, ESSCIRC, VLSI.
Has served in the Program Committee of ASYNC, ESSCIRC.
Françoise RENZETTI

Born July 11th, 1943
French

Education

1994 Doctor degree in Communication
1980 Certificat d'Aptitude aux fonctions de bibliothécaire
1979 Doctor degree in History of Science

Position

Electronic Publishing officer

Past activities

Director of Médiathèque de l’Institut d’Informatique et de Mathématiques Appliquées de Grenoble (IMAG).
Frédéric ROUSSEAU

Born March 2nd, 1967
Single
French

Education

1991 : Engineer degree, computer science and electrical engineering (3i), University Joseph Fourier, Grenoble, France,
1991 : DEA degree in Microelectronics, University Joseph Fourier,
1992 : DEA degree in Computer Science, INPG, Grenoble, France
1997 : Ph.D. in computer science from the University of Evry, France

Position

Assistant professor (Maître de conférences) at UJF (Joseph Fourier University), Grenoble.

Past activities

1996 – 1999 Teacher – Researcher at the engineer school of Marseille (ESIM), France in the computer science and electrical engineering department.

Current responsibilities

Researcher in « System Level Synthesis » group (SLS)
Gilles SICARD

Born July 7th, 1970
Married, one child
French

Education

1994 : DEA degree in Microelectronics, INPG.
1999 : PhD in Microelectronics, INPG.

Position

Assistant professor (Maître de conférence) at UJF (Joseph Fourier University), Grenoble.

Past activities

Contractual teacher (ATER) at ENSERG (Ecole Nationale Supérieure d’Electronique et Radioélectricité de Grenoble) and researcher at LIS Laboratory (Laboratoire des Images et des Signaux), Grenoble, 1999.


Current responsibilities

Researcher in « Concurrent Integrated Systems » group (CIS).

His research interests analog circuits design, asynchronous circuits design, and imaging systems on a chip.

Miscellaneous

Has developed a smart image sensor in 1998. This analog retina contains an array of 64x64 pixels which performs three analog image processings in real time: Edge extraction, motion detection and a light adaptive system.
Emmanuel SIMEU

Born December 25th, 1959
Married, 3 children
French and Cameroonian

Education

1987  Engineer degree -Electrical- University of Casablanca (Morroco)

Position

Associate Professor (Maître de Conférences) at ISTG (Institut des Sciences et Techniques de Grenoble).

Current responsibilities

Member of the Reliable Integrated Systems Group

Previous positions

Associate Professor at ISAR (Institut Supérieur d'Automatique et de Robotique de Valence) (1992-1995).

Researcher in LAG (Laboratoire d'Automatique de Grenoble) (1988 - 1995)
Researcher in CNET-CNS Grenoble (SITAR Project 1989 - 1992)

Miscellaneous

Pedagogic responsibility in the department of industrial risk management of ISTG.

Courses and lectures on reliability, automatic control and applied mathematics in the industrial risk management department of ISTG.

Courses and lectures of automatic control Maîtrise EEA of Joseph Fourier University.

Program Committee member of IEEB International On-line Testing Workshop.
Patrick SOURICE

Born in September 17, 1961
Married
French

Education:

1981 : B.E.P electronic
1994 : DPCT electronic

Position:

Technician

Current responsibilities:

System Administrator
Electronic’s teacher at IUT in electronics (UJF)
Kholdoun TORKI

Born February 21\textsuperscript{th} 1961
Married, 1 children
Tunisian

\textbf{Education}

1985 : "Maîtrise" degree in physics and electronics, University of Constantine.
1986 : DEA microelectronics, INPG, Grenoble.
1990 : Ph.D. degree, INPG, Grenoble.

\textbf{Position}

Engineer at CNRS since 1994.
Contractual engineer with CMP-TIMA Laboratory since June 1990.

\textbf{Current responsibilities:}

* Engineering Manager of CMP.
* Project Coordinator for PhD students exchange between TIMA Laboratory and the University of Monastir (Tunisia).
* Supervising PhD students at TIMA Laboratory.
Raoul VELAZCO

Born December 14th, 1952
Married
French

Education

1976-1979  National School for Informatics and Applied Mathematics (ENSIMAG) Grenoble
1979      Engineer degree
1982      Ph.D degree from Polytechnique Institut of Grenoble (INPG)
1990      Dr. ès Sciences from INPG

Position

- “Director of Researches” at CNRS (French Research Agency)
- Researcher with TIMA laboratory (Techniques of the Informatics and Microelectronics for computer architecture) since 1996

Current Responsibilities

- Leader of the "Qualification of Circuits" research group of TIMA laboratory
- Member of the Scientific Committee of TIMA since 1998
- Responsible of the design of a flight experiment to be included on board a scientific satellite: NASA Project LWS/SET (Living With a Star / Space Environment Testbed)

Miscellaneous

- General Chair of RADECS 2001 (Grenoble, France).
- General Chairman of LATW 2002 (Montevideo, Uruguay).
Gérard VITRY

Born August 5th, 1947
Married, 2 children
French

Education

1973: "Programmeur Expert en Systèmes Informatiques" - Grenoble

Position

"Ingénieur d'Etudes" at CNRS

Current responsibilities:

* System Engineer
* Web administrator
Sungjoo YOO

Born March 10th, 1969
Married, 2 children
Korean

Education


Position

Visiting researcher at TIMA

Current responsibilities

- System design methodology
- Cosimulation
Nacer-Eddine ZERGAINOH

Born May 18th, 1969
French and Algerian

Education

1984 Baccalaureat degree, Mathematics

1989 Engineer degree, Telecommunication. National School of telecommunication

1990 DEA degree, Signal Processing & Control, Signals and Systems Laboratory, Supélec.

1996 PhD degree, Computer Engineering, INRIA & Paris XI University, France Methods and tools-aided design of reactive systems. Distributed Real-time Operating System for an embedded obstacle detection system.

Position

Associate Professor (maître de conférence) in Computer Engineering and Architecture, Institute of Sciences and Technique (ISTG), Joseph Fourier University, Grenoble.

Past activities

* Participated to the European Esprit-Polyglot Project.
* Participated to the European Prometheus Project.
* Teacher in telecom and computer (ESIGITEL, EPITA, Paris XIII University).
* Contractual engineer of research with LIMSI-CNRS Laboratory Gif/Yvette.

Current responsibilities

* Researcher in System Level Synthesis Group of TIMA Laboratory. His research interests include system-level design and CAD issues, multiprocessor architectures modeling, and real-time operating system. Currently, his research focuses on multiprocessor architectures exploration, RTOS, and interface Synthesis.

Miscellaneous

* Has authored or co-authored several scientific papers.
* Has served in many program committees of conferences and workshops
* Has served as a reviewer of many journals and conferences
## IV-1.3 Curriculum vitae of Doctorate candidates

<table>
<thead>
<tr>
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IV-2 TIMA network and computer equipment

IV-2.1 Computer equipment

In order to continuously provide its users with services of an improved quality, TIMA computers department continuously renews its computer equipment. Today the computerised system of TIMA Laboratory consists of the following units:

| Servers: | 1 SunUltra5 (FTP).  
1 SunUltra1 (e-mail, file, backup).  
1 SunUltra1 (Development).  
1 SunUltra1 (DNS cache).  
1 Sparc20 (Printers).  
1 DELL Poweredge 2400 (WWW).  
1 Athlon 850 Mhz (SGBD,WWW-Intranet) |
| Devices: | 1 CD Recorder  
1 DLT 7000 Tape Drive  
1 DDS 3 Tape Drive  
2 HP LaserJet 4000N Printers  
1 HP LaserJet 4050N Printer  
1 HP 4050N (Duplex) Printer  
1 Konica 7050 Copier  
1 HP DeskJet 1600 CM/PS Printer  
4 Epson DeskJet Printers |
| Personal Computers: | TIMA provides a workstation for each user incoming in the laboratory, which corresponds to a continuous of 120 PCs. The PCs fleet is composed both of Pentium 166 Mhz and PIII 1GHz and notebooks for laboratory external jobs. All those computers have the same standard configuration with office software and a permanent internet connection. Moreover, a computer can bee freely accessed to use the scanner and a colour jet-printer. There are about 120 PCs in use. |
| Micro computers MAC: | 1 Quadra 800  
1 Performa 630  
3 Power Mac  
5 Powerbook |
IV-2.2 Network equipment

This year the TIMA Laboratory network has been entirely restructured. A router appears at the head of the network to allow to segment the network. This router is an OMNICORE 5010 sold by ALCATEL. The offered functionalities made the network more secure with filters of levels 3 and 4. To help this router, two switches OMNICORE 5010 sold by ALCATEL are installed at the head of each anex of the laboratory. This OMNICORE, like the router has functionalities allowing remote management and measurement on the network. That equipment alone is not enough to connect all the users to the network, that is why under that equipment there are some switches that allowing to provide enough ports for all the computers of TIMA Laboratory.

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IV-2.3 Interconnection schemes

IV-2.3.1 Logical scheme

The scheme introduces the logical network of TIMA defined with VLANs (This scheme does not mention physical location).
IV-2.3.2 Physical scheme

See the following detailed scheme about TIMA Network Wiring:
IV-3  Financial resources

Some data are given below on financial aspects. They are provided for 1989-2000 budget years, to allow comparisons.

In 1989, the budget of the Laboratory has been 9 118 kFF (excluding VAT). This amount does not include salaries of government employees, like CNRS researchers and Professors.

This budget comes from research funds provided by CNRS or Universities (INPG and UJF), from contracts signed with industrial firms or CEC, and from "exceptional" funds or "exceptional" invoices (emitted for example against services). Those funds are accounted by either CNRS, or INPG or UJF. The Table IV-3 I gives the distribution, and the Figure IV-3 1 represents it. It is to be noted that the input for contracts represent the total amount of the contracts which are signed in 1989, even if the contract will last for several years.

The contractual part represents approx. 80 % of the budget in 1989. The Table IV-3 II gives the list of contracts signed in 1989. The CEC part represents approx. 80 % of the contracts.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>182</td>
<td>8</td>
<td>290</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>140</td>
<td>705</td>
<td>0</td>
<td>845</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>569</td>
<td>239</td>
<td>0</td>
<td>808</td>
</tr>
<tr>
<td>Contracts signed in 1989</td>
<td>335</td>
<td>6 840</td>
<td>0</td>
<td>7 175</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>1 144</td>
<td>7 966</td>
<td>8</td>
<td>9 118</td>
</tr>
</tbody>
</table>

Table IV-3 I - Budget 1989 (kFF, excluding VAT)
Figure IV-3 I - Budget 1989

<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIIP</td>
<td>4 293</td>
</tr>
<tr>
<td>CEC / ASICS</td>
<td>1 853</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>579</td>
</tr>
<tr>
<td>CSEE</td>
<td>115</td>
</tr>
<tr>
<td>GCIS</td>
<td>335</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>7 175</strong></td>
</tr>
</tbody>
</table>

Table IV-3 II - Contracts signed in 1989 (kFF, excluding VAT)
In 1990, the budget has been 8,582 kFF (excluding VAT). The Table IV-3 III gives the distribution, and the Figure IV-3 2 represents it. Again, the input for contracts represents the total amount of contracts signed in 1990, even if those contracts last for several years.

In 1990, the contractual part represents approximately 43% of the budget. The Table IV-3 IV gives the list of contracts signed in 1990.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>162</td>
<td>3</td>
<td>265</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>210</td>
<td>3,404</td>
<td>0</td>
<td>3,614</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>766</td>
<td>210</td>
<td>0</td>
<td>976</td>
</tr>
<tr>
<td>Contracts signed in 1990</td>
<td>0</td>
<td>2,782</td>
<td>0</td>
<td>3,727</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>2,196</strong></td>
<td><strong>6,558</strong></td>
<td><strong>0</strong></td>
<td><strong>8,582</strong></td>
</tr>
</tbody>
</table>

Table IV-3 III - Budget 1990 (kFF, excluding VAT)

Figure IV-3 2 - Budget 1990
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNES</td>
<td>500</td>
</tr>
<tr>
<td>TMS</td>
<td>240</td>
</tr>
<tr>
<td>MATRA ESPACE</td>
<td>292</td>
</tr>
<tr>
<td>IBM</td>
<td>285</td>
</tr>
<tr>
<td>CNES</td>
<td>150</td>
</tr>
<tr>
<td>GCIS</td>
<td>945</td>
</tr>
<tr>
<td>MIAT / JESSI AC6</td>
<td>1315</td>
</tr>
</tbody>
</table>

| SUM             | 3727   |

Table IV-3 IV - Contracts signed in 1990 (kFF, excluding VAT)

The key issue when comparing data for 1989 and for 1990 is that the CEC EUROCHIP contract is financially important for 1989. In 1990, the part of industrial contracts has been increased. Those data are nevertheless partially sounded, because of the criterion consisting in account a contract once, the year it is signed.
In 1991, the budget has been 9,322 kFF (excluding VAT). The Table IV-3 V gives the distribution, and the Figure IV-3 3 represents it. In 1991, the contractual part represents approximately 44%. The CEC part represents 60% through ESPRIT Basic Research, and the JESSI part represents 38%. The Table IV-3 VI gives the list of contracts signed in 1991.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>165</td>
<td>0</td>
<td>265</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>712</td>
<td>2,238</td>
<td>0</td>
<td>2,950</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1,884</td>
<td>85</td>
<td>0</td>
<td>1,969</td>
</tr>
<tr>
<td>Contracts signed in 1991</td>
<td>0</td>
<td>4,138</td>
<td>0</td>
<td>4,138</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>2,696</strong></td>
<td><strong>6,626</strong></td>
<td><strong>0</strong></td>
<td><strong>9,322</strong></td>
</tr>
</tbody>
</table>

Table IV-3 V - Budget 1991 (kFF, excluding VAT)

Figure IV-3 3 - Budget 1991
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / ASICS</td>
<td>154</td>
</tr>
<tr>
<td>CEC / EUROCHIP</td>
<td>2352</td>
</tr>
<tr>
<td>MICE / JESSI AC6</td>
<td>855</td>
</tr>
<tr>
<td>MICE / JESSI AE11</td>
<td>727</td>
</tr>
<tr>
<td>HEWLETT PACKARD</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>4138</td>
</tr>
</tbody>
</table>

Table IV-3 VI - Contracts signed in 1991 (kFF, excluding VAT)
In 1992, the budget has been 12 118 kFF (excluding VAT). The Table IV-3 VII gives the distribution, and the Figure IV-3 4 represents it. In 1992, the contractual part represents approximately 54 %, the CEC part represents 68 % through ESPRIT Basic Research, and the JESSI part represents 32 %.

The Table IV-3 VIII gives the list of contracts signed in 1992.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>208</td>
<td>147</td>
<td>0</td>
<td>355</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>160</td>
<td>2 370</td>
<td>0</td>
<td>2 530</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2 511</td>
<td>116</td>
<td>0</td>
<td>2 627</td>
</tr>
<tr>
<td>Contracts signed in 1992</td>
<td>0</td>
<td>6 606</td>
<td>0</td>
<td>6 606</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2 879</td>
<td>9 239</td>
<td>0</td>
<td>12 118</td>
</tr>
</tbody>
</table>

Table IV-3 VII - Budget 1992 (kFF, excluding VAT)

Figure IV-3 4 - Budget 1992
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>4484</td>
</tr>
<tr>
<td>CEC / ARCHIMEDES</td>
<td>712</td>
</tr>
<tr>
<td>CEC / FASED</td>
<td>126</td>
</tr>
<tr>
<td>MICE / JESSI AC6</td>
<td>880</td>
</tr>
<tr>
<td>MICE / JESSI AE11</td>
<td>404</td>
</tr>
</tbody>
</table>

6606

Table IV-3 VIII - Contracts signed in 1992 (kFF, excluding VAT)
In 1993, the budget has been 17,403 kFF (excluding VAT). The Table IV-3 IX gives the distribution, and the Figure IV-3 5 represents it. In 1993, the contractual part represents approximately 64%. The CEC part represents 61%, and the JESSI part represents 36%. The Table IV-3 X gives the list of contracts signed in 1993.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>166</td>
<td>568</td>
<td>0</td>
<td>734</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>171</td>
<td>2,321</td>
<td>0</td>
<td>2,492</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2,859</td>
<td>247</td>
<td>0</td>
<td>3,106</td>
</tr>
<tr>
<td>Contracts signed in 1993</td>
<td>99</td>
<td>10,972</td>
<td>0</td>
<td>11,071</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>3,295</td>
<td>14,108</td>
<td>0</td>
<td>17,403</td>
</tr>
</tbody>
</table>

Table IV-3 IX - Budget 1993 (kFF, excluding VAT)

Figure IV-3 5 - Budget 1993
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>4 258</td>
</tr>
<tr>
<td>CEC / NSF - CLC</td>
<td>325</td>
</tr>
<tr>
<td>CEC / NSF - NDIMST</td>
<td>119</td>
</tr>
<tr>
<td>CEC / COPERNICUS 93 n°9093</td>
<td>97</td>
</tr>
<tr>
<td>CEC / ARCHIMEDES</td>
<td>915</td>
</tr>
<tr>
<td>CEC / HCM - GARDEN</td>
<td>137</td>
</tr>
<tr>
<td>CEC / CHIPSHOP</td>
<td>743</td>
</tr>
<tr>
<td>CEC / EEMCN</td>
<td>73</td>
</tr>
<tr>
<td>CEC / EDAC-EUROASIC 93-94</td>
<td>99</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC6</td>
<td>880</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC8</td>
<td>1 860</td>
</tr>
<tr>
<td>MIPTCE / JESSI AE11</td>
<td>414</td>
</tr>
<tr>
<td>SGS-THOMSON / JESSI AC8</td>
<td>801</td>
</tr>
<tr>
<td>CNET / SOLIST</td>
<td>350</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>11 071</strong></td>
</tr>
</tbody>
</table>

Table IV-3 X - Contracts signed in 1993 (kFF, excluding VAT)
In 1994, the budget has been 19 253 kFF (excluding VAT). The Table IV-3 XI gives the distribution, and the Figure IV-3 6 represents it. In 1994, the contractual part represents approximately 74 %.
The CEC part represents 52 %, and the JESSI part represents 32 %.
The Table IV-3 XII gives the list of contracts signed in 1994.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>185</td>
<td>518</td>
<td>0</td>
<td>0</td>
<td>703</td>
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<tr>
<td>Exceptional funds</td>
<td>40</td>
<td>1 824</td>
<td>0</td>
<td>0</td>
<td>1 864</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1 935</td>
<td>454</td>
<td>0</td>
<td>0</td>
<td>2 389</td>
</tr>
<tr>
<td>Contracts signed in 1994</td>
<td>0</td>
<td>13 431</td>
<td>565</td>
<td>300</td>
<td>14 296</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2 160</td>
<td>16 227</td>
<td>565</td>
<td>300</td>
<td>19 252</td>
</tr>
</tbody>
</table>

Table IV-3 XI - Budget 1994 (kFF, excluding VAT)

Figure IV-3 6 - Budget 1994
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>3866</td>
</tr>
<tr>
<td>CEC / BARMINT</td>
<td>799</td>
</tr>
<tr>
<td>CEC / COPERNICUS THERMINIC</td>
<td>565</td>
</tr>
<tr>
<td>CEC / COPERNICUS FUTEG</td>
<td>299</td>
</tr>
<tr>
<td>CEC / AMATIST</td>
<td>1092</td>
</tr>
<tr>
<td>CEC / GRASS</td>
<td>142</td>
</tr>
<tr>
<td>CEC / CHIPSHOP</td>
<td>701</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC6</td>
<td>1103</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC8</td>
<td>2887</td>
</tr>
<tr>
<td>MIPTCE / JESSI AE11</td>
<td>526</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>570</td>
</tr>
<tr>
<td>SGS-THOMSON / CIFRE</td>
<td>90</td>
</tr>
<tr>
<td>CNET / PSYCOS</td>
<td>1200</td>
</tr>
<tr>
<td>AEROSPAZIALE</td>
<td>300</td>
</tr>
<tr>
<td>DRET / ASTER INGENIERIE</td>
<td>156</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>14296</strong></td>
</tr>
</tbody>
</table>

Table IV-3 XII - Contracts signed in 1994 (kFF, excluding VAT)
In 1995, the budget has been 15,018 kFF (excluding VAT). The Table IV-3 XIII gives the distribution, and the Figure IV-3 7 represents it. In 1995, the contractual part represents approximately 37%.
The CEC part represents 18%, and the JESSI part represents 65%.
The Table IV-3 XIV gives the list of contracts signed in 1995.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>235</td>
<td>600</td>
<td>62</td>
<td>0</td>
<td>897</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>17</td>
<td>2,010</td>
<td>0</td>
<td>0</td>
<td>2,027</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>5,089</td>
<td>1,381</td>
<td>0</td>
<td>0</td>
<td>6,470</td>
</tr>
<tr>
<td>Contracts signed in 1995</td>
<td>0</td>
<td>4,994</td>
<td>630</td>
<td>630</td>
<td>5,624</td>
</tr>
<tr>
<td>TOTAL</td>
<td>5,341</td>
<td>8,985</td>
<td>62</td>
<td>630</td>
<td>15,018</td>
</tr>
</tbody>
</table>

Table IV-3 XIII - Budget 1995 (kFF, excluding VAT)

Figure IV-3 7 - Budget 1995
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / CHIPSHOP</td>
<td>350</td>
</tr>
<tr>
<td>CEC / KIT 106 ARCOS</td>
<td>124</td>
</tr>
<tr>
<td>CEC / KIT 107 ATAME</td>
<td>110</td>
</tr>
<tr>
<td>CEC / OMI</td>
<td>442</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC6</td>
<td>808</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC8</td>
<td>1788</td>
</tr>
<tr>
<td>SGS-THOMSON / JESSI AE102/103</td>
<td>1032</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>340</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>300</td>
</tr>
<tr>
<td>SODERN</td>
<td>330</td>
</tr>
<tr>
<td></td>
<td>5624</td>
</tr>
</tbody>
</table>

Table IV-3 XIV - Contracts signed in 1995 (kFF, excluding VAT)
In 1996, the budget has been 19 211 kFF (excluding VAT). The Table IV-3 XV gives the distribution, and the Figure IV-3 8 represents it. In 1996, the contractual part represents approximately 46%.

The CEC part represents 45%, and the JESSI part represents 40%.

The Table IV-3 XVI gives the list of contracts signed in 1996.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>65</td>
<td>520</td>
<td>63</td>
<td>0</td>
<td>648</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>13</td>
<td>1 774</td>
<td>0</td>
<td>0</td>
<td>1 787</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>5 603</td>
<td>2 338</td>
<td>0</td>
<td>54</td>
<td>7 995</td>
</tr>
<tr>
<td>Contracts signed in 1996</td>
<td>0</td>
<td>2 656</td>
<td>5 188</td>
<td>937</td>
<td>8 781</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>5 681</strong></td>
<td><strong>7 288</strong></td>
<td><strong>5 251</strong></td>
<td><strong>991</strong></td>
<td><strong>19 211</strong></td>
</tr>
</tbody>
</table>

Table IV-3 XV - Budget 1996 (kFF, excluding VAT)

![Figure IV-3 8 - Budget 1996](image)
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / COMITY</td>
<td>1 388</td>
</tr>
<tr>
<td>CEC / HIPERLOGIC</td>
<td>1 300</td>
</tr>
<tr>
<td>CEC / OMI-EUROMIC</td>
<td>424</td>
</tr>
<tr>
<td>CEC / OMI-LIBRES</td>
<td>358</td>
</tr>
<tr>
<td>CEC / SYSLINK</td>
<td>520</td>
</tr>
<tr>
<td>MIPT / JESSI AC3</td>
<td>1 322</td>
</tr>
<tr>
<td>MIPT / JESSI AC8</td>
<td>2 232</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>387</td>
</tr>
<tr>
<td>BEVERLY / FUSE</td>
<td>58</td>
</tr>
<tr>
<td>MG-ANACAD</td>
<td>280</td>
</tr>
<tr>
<td>SCLUMBERGER</td>
<td>212</td>
</tr>
<tr>
<td>DGA/DRET</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>8 781</td>
</tr>
</tbody>
</table>

Table IV-3 XVI - Contracts signed in 1996 (kFF, excluding VAT)
In 1997, the budget has been 17,447 kFF (excluding VAT). The Table IV-3 XVII gives the distribution, and the Figure IV-3 9 represents it. In 1997, the contractual part represents approximately 36%.

The CEC part represents 23%, and the MEDEA part represents 41%.

The Table IV-3 XVIII gives the list of contracts signed in 1997.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>128</td>
<td>519</td>
<td>63</td>
<td>0</td>
<td>710</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>200</td>
<td>374</td>
<td>13</td>
<td>0</td>
<td>587</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2,299</td>
<td>1,591</td>
<td>0</td>
<td>5,853</td>
<td>9,743</td>
</tr>
<tr>
<td>Contracts signed in 1997</td>
<td>0</td>
<td>2,696</td>
<td>2,977</td>
<td>734</td>
<td>6,407</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2,627</td>
<td>5,180</td>
<td>3,053</td>
<td>6,587</td>
<td>17,447</td>
</tr>
</tbody>
</table>

Table IV-3 XVII - Budget 1997 (kFF, excluding VAT)

![Figure IV-3 9 - Budget 1997](image-url)
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEVERLY</td>
<td>73</td>
</tr>
<tr>
<td>SCHNEIDER</td>
<td>175</td>
</tr>
<tr>
<td>SODERN</td>
<td>120</td>
</tr>
<tr>
<td>SODERN</td>
<td>94</td>
</tr>
<tr>
<td>ECSI</td>
<td>72</td>
</tr>
<tr>
<td>CNES</td>
<td>200</td>
</tr>
<tr>
<td>CNET</td>
<td>800</td>
</tr>
<tr>
<td>PEUGEOT</td>
<td>400</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>90</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>90</td>
</tr>
<tr>
<td>CEC/ASSISTEC</td>
<td>401</td>
</tr>
<tr>
<td>MEDEA/AT-401</td>
<td>663</td>
</tr>
<tr>
<td>CEA</td>
<td>252</td>
</tr>
<tr>
<td>CEC/CODAC</td>
<td>987</td>
</tr>
<tr>
<td>MEDEA/AT-403</td>
<td>1990</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>6407</strong></td>
</tr>
</tbody>
</table>

Table IV-3 XVIII - Contracts signed in 1997 (kFF, excluding VAT)
In 1998, the budget has been 14,397 kFF (excluding VAT). The Table IV-3 XIX gives the distribution, and the Figure IV-3 10 represents it. In 1998, the contractual part represents approximately 40%.

The CEC part represents 18%, and the MEDEA part represents 70%.

The Table IV-3 XX gives the list of contracts signed in 1998.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>160</td>
<td>530</td>
<td>63</td>
<td></td>
<td></td>
<td>753</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>200</td>
<td>41</td>
<td></td>
<td></td>
<td></td>
<td>241</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1,726</td>
<td>607</td>
<td>4,899</td>
<td>166</td>
<td>7,398</td>
<td></td>
</tr>
<tr>
<td>Contracts signed in 1998</td>
<td>1,066</td>
<td>4,389</td>
<td>350</td>
<td>200</td>
<td>6,005</td>
<td></td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2,086</td>
<td>2,244</td>
<td>4,452</td>
<td>5,249</td>
<td>366</td>
<td>14,397</td>
</tr>
</tbody>
</table>

Table IV-3 XIX - Budget 1998 (kFF, excluding VAT)

Figure IV-3 10 - Budget 1998
In 1999, the budget has been 24,549 kFF (excluding VAT). The Table IV-3 XXI gives the distribution, and the Figure IV-3 11 represents it. In 1999, the contractual part represents approximately 38%.

The MEDEA part represents 94%.

The Table IV-3 XXII gives the list of contracts signed in 1999.

<table>
<thead>
<tr>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>170</td>
<td>540</td>
<td>97</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>50</td>
<td>372</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1,286</td>
<td>988</td>
<td>18</td>
<td>5,932</td>
<td>807</td>
</tr>
<tr>
<td>Contracts signed in 1999</td>
<td>-</td>
<td>-</td>
<td>13,589</td>
<td>-</td>
<td>700</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>1,506</strong></td>
<td><strong>1,900</strong></td>
<td><strong>13,704</strong></td>
<td><strong>5,932</strong></td>
<td><strong>1,507</strong></td>
</tr>
</tbody>
</table>

Table IV-3 XXI - Budget 1999 (kFF, excluding VAT)

Figure IV-3 11 - Budget 1999
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEA</td>
<td>90</td>
</tr>
<tr>
<td>CNES</td>
<td>550</td>
</tr>
<tr>
<td>INRETS</td>
<td>150</td>
</tr>
<tr>
<td>ST MICROELECTRONICS</td>
<td>60</td>
</tr>
<tr>
<td>SERICS/MEDEA/AT-401</td>
<td>5,520</td>
</tr>
<tr>
<td>SERICS/MEDEA/AT-403</td>
<td>7,919</td>
</tr>
<tr>
<td></td>
<td>14,289</td>
</tr>
</tbody>
</table>

Table IV-3 XXII - Contracts signed in 1999 (kFF, excluding VAT)
In 2000, the budget has been 33,459 kFF (excluding VAT). The Table IV-3 XXIII gives the distribution, and the Figure IV-3 12 represents it. In 2000, the contractual part represents approximately 67,25%.
The MEDEA part represents 31,75%.
The Table IV-3 XXIV gives the list of contracts signed in 2000.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>200</td>
<td>550</td>
<td>115</td>
<td>-</td>
<td>-</td>
<td>865</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>60</td>
<td>115</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>175</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2 420</td>
<td>3 045</td>
<td>50</td>
<td>17</td>
<td>4 383</td>
<td>9 915</td>
</tr>
<tr>
<td>Contracts signed in 2000</td>
<td>1 776</td>
<td>13 216</td>
<td>6 740</td>
<td>-</td>
<td>772</td>
<td>22 504</td>
</tr>
<tr>
<td>TOTAL</td>
<td>4 456</td>
<td>16 926</td>
<td>6 905</td>
<td>17</td>
<td>5 155</td>
<td>33 459</td>
</tr>
</tbody>
</table>

Table IV-3 XXIII - Budget 2000 (kFF, excluding VAT)

Figure IV-3 12 - Budget 2000
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNES</td>
<td>395</td>
</tr>
<tr>
<td>FRANCE TELECOM</td>
<td>525</td>
</tr>
<tr>
<td>INTA</td>
<td>252</td>
</tr>
<tr>
<td>CEC/CODAC</td>
<td>351</td>
</tr>
<tr>
<td>CEC/HERPERLOGIC</td>
<td>60</td>
</tr>
<tr>
<td>CEC/IST ACID-WG</td>
<td>131</td>
</tr>
<tr>
<td>CEC/IST MATISSE</td>
<td>1776</td>
</tr>
<tr>
<td>CEC/IST/PROFIT</td>
<td>1108</td>
</tr>
<tr>
<td>CEC/OMI-LIBRES</td>
<td>57</td>
</tr>
<tr>
<td>ESPRIT/TALENT</td>
<td>577</td>
</tr>
<tr>
<td>SERICS/MEDEA SMT AT 403</td>
<td>6272</td>
</tr>
<tr>
<td>SERICS/MEDEA A 401</td>
<td>875</td>
</tr>
<tr>
<td>ST MICROELECTRONICS</td>
<td>10075</td>
</tr>
<tr>
<td>XILINX</td>
<td>50</td>
</tr>
</tbody>
</table>

22 504

Table IV-3 XXIV - Contracts signed in 2000 (kFF, excluding VAT)
In 2001, the budget has been 27.492 kFF (excluding VAT). The Table IV-3 XXV gives the distribution, and the Figure IV-3 13 represents it. In 2001, the contractual part represents approximately 30,30 %.

The MEDÉA part represents 33,80 %.

The Table IV-3 XXVI gives the list of contracts signed in 2001.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>UNIVAL</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>310</td>
<td>505</td>
<td>98</td>
<td>-</td>
<td>-</td>
<td>913</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>68</td>
<td>125</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>203</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>4,930</td>
<td>4,339</td>
<td>113</td>
<td>498</td>
<td>8,175</td>
<td>18,055</td>
</tr>
<tr>
<td>Contracts signed in 2001</td>
<td>-</td>
<td>2,820</td>
<td>3,936</td>
<td>1,140</td>
<td>425</td>
<td>8,321</td>
</tr>
<tr>
<td>TOTAL</td>
<td>5,308</td>
<td>7,789</td>
<td>4,157</td>
<td>1,638</td>
<td>8,600</td>
<td>27,492</td>
</tr>
</tbody>
</table>

Table IV-3 XXV - Budget 2001 (kFF, excluding VAT)

Figure IV-3 13 - Budget 2001
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEA</td>
<td>100</td>
</tr>
<tr>
<td>CEE/IST FRACTURE</td>
<td>226</td>
</tr>
<tr>
<td>IROC TECHNOLOGIES / JPL</td>
<td>1,390</td>
</tr>
<tr>
<td>MEFI/MEDEA+ T101</td>
<td>464</td>
</tr>
<tr>
<td>MEFI/MEDEA+ A302</td>
<td>1,397</td>
</tr>
<tr>
<td>MEFI/MEDEA+ A502</td>
<td>955</td>
</tr>
<tr>
<td>PREDIT/MIRFAS</td>
<td>59</td>
</tr>
<tr>
<td>RNTL/VERHAUNIC</td>
<td>2,755</td>
</tr>
<tr>
<td>ST MICROELECTRONICS</td>
<td>975</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>8,321</strong></td>
</tr>
</tbody>
</table>

Table IV-3 XXVI - Contracts signed in 2001 (kFF, excluding VAT)
If we consider 1989, 1990, 1991, 1992, 1993, 1994, 1995, 1996, 1997, 1998, 1999, 2000, 2001 together, then we get the global data given in Table IV-3 XXVII and represented by Figure IV-3 14. Such data are more representative of the reality. Now, we get a part of the contracts which is 52,32% of the budget. From 1991, the average percentages of EC and JESSI/MEDEA shares are respectively 31,29% and 45,14%.

![Graph showing percentages of different categories]

**Figure IV-3 14 - Budget 1989 - 2001**

<table>
<thead>
<tr>
<th>Category</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>8 206</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>19 737</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>80 483</td>
</tr>
<tr>
<td>Contracts</td>
<td>118 946</td>
</tr>
</tbody>
</table>

**Table IV-3 XXVII - Budget 1989-2001 (kFF, excluding VAT)**
V - COOPERATIVE ACTIVITIES

V-1 Contracts

Public Institutions: MAE (Ministère des Affaires Etrangères); MEFI (Ministère de l’Économie, des Finances et de l’Industrie); MIPT (SERICS) (Ministère de l'Industrie, de la Poste et des Télécommunications); Service des Industries de Communication et de Service; France Télécom (CNET) (France Télécom - Centre National d'Études des Télécommunications); Ministère de la Défense; Direction Générale pour l'Armement; Direction de la Recherche et de la Technologie; INRETS.

Industrial contracts: STMICROELECTRONICS, AEROSPATIALE, SODERN, ANACAD, SCHLUMBERGER, PEUGEOT, SCHNEIDER, CNES, CEA, INTA, IROC TECHNOLOGIES, XILINX, ATMEL.

V-2 European Projects

V-2.1 Summary

In the past, members of the Laboratory participated to EC Projects like CASCADE and CVT. Presently, or recently, the Laboratory participates or has been participating to the following projects:

EC PROJECTS:

ESPRIT I :

ESPRIT II BASIC RESEARCH :

ESPRIT III BASIC RESEARCH :

ESPRIT III RESEARCH AND DEVELOPMENT :

ESPRIT III KIT :

ESPRIT IV KIT :

ESPRIT IV LTR :

ESPRIT IV RESEARCH AND DEVELOPMENT :

ESPRIT IV OMI :

ESPRIT IV BEST PRACTICE :

IST :

CEC/NSF Cooperation :

JESSI PROJECTS :

ADVICE, AIDA, SPAN

ASCIS, EUROCCHIP

ARCHIMEDES, FASED, BARMINT, AMATIST, GRASS

CHIPSHOP

ARCOS, ATAME

DETERMIN, LICDST, LIMITE

HIPERLOGIC

COMITY, TALENT

IUN2, EUROMIC, OMILIBRES, CODAC, ASSISTEC

SYSLINK

PROFIT, MATISSE, ACiD-W, FRACTURE

NDIMST, CSLS

AC6, AE11, AC8, AC3, AE102, AE103
MEDEA PROJECTS: AT 403, AT 401-408
MEDEA+ PROJECTS: T 101, A 302, A502
COMETT PROJECTS:
COMETT I: COMET
COMETT II: EUROSYSTEMS, EPIQCS
EUREKA PROJECT:
EUREKA: MITHRA
TEMPUS PROJECTS:
TEMPUS
- Advanced JEP for Microelectronics Design Methodology
- MECC
- Initiation of Formal Training in CAEE in Romanian Universities
- Computer-aided Methods and Technical Management in Electrical Engineering Education
- Digital System Design Based on PLD-Technology
- Education for Quality Control in Electrical Industry Equator
- Postgraduate Education in ASIC Design
- EUROQUALROM: European Education in Quality for Romania
COPERNICUS (PECO) PROJECTS:
COPERNICUS (ex PECO)
- EDAC-EAST: Attendance of Central and Eastern European Engineers and Researchers to the EDAC Conference
- Design of VLSI self-checking digital circuits
- Developing design automation technique in ASIC and VLSI Design
- CAD/CAT tools integration for sensor-based microsystems
- Dependability Analysis of Complex Electronic Components and Systems
- East European Microelectronics Cooperation Network of support and competence centres of Central and Eastern
- Functional test generation and diagnosis (FUTEG)
- EUROEAST: Extension of EUROCHIP services to Central and Eastern European Countries
- THERMINIC: New Methods for Thermal Investigation of Integrated Circuits
HUMAN CAPITAL MOBILITY PROJECT:
HCM: GARDEN
LATIN AMERICA HIGHER EDUCATION:
ALFA: HUERTA, ELACIAC
V-2.2 Details

Below are described the European Projects the Laboratory has been involved in since 1984.

They are divided in two categories:
- the finished ones
- those which are ongoing.

For the finished ones, only few data are given (more information is available in previous reports). For the ongoing projects, an abstract describing the project is given.

V-2.2.1 European Projects that came to the end in 2000 or before

<table>
<thead>
<tr>
<th>ESPRIT PROJECTS</th>
</tr>
</thead>
</table>

### ESPRIT-I

**ADVICE**  
(CSELT, British Telecom, CNET, TIMA, Trinity College),  
1984-1989 (ADVICE I)  
Automatic Design Validation of Integrated Circuits using Electron Beam

**AIDA**  
(SIEMENS, ICL, SGS THOMSON, TIMA, University of Manchester),  
1986-1990  
Advanced Integrated-circuit Design Aids

**SPAN**  
(THORM-EMI, CIMSA-SINTRA, CTI, INESC, PCS, TIMA, Universty College London),  
1987-1990  
Parallel Computer Systems for Integrated Numeric and Symbolic Processing

### ESPRIT-II Basic Research

**ASCIS**  
(IMEC, TIMA, Universities of Darmstadt, Eindhoven, Lund, Lyngby, Patras),  
1989-1992  
Architecture Synthesis for Complex Integrated Systems

**EUROCHIP**  
(GMD, CMP, IMEC, University of Lyngby, RAL),  
1989-1994  
Service organisation of the VLSI Design Action  
CMP was a member of the Service Organisation.

### ESPRIT-III Basic Research

**ARCHIMEDES**  
(TIMA, Univ. of Karlsruhe, Montpellier, Hannover, Bologna, Barcelona, & INESC),  
1992-1995  
ARCHitectural MEthodologies for aDVanced tEsting of VLSI Systems.
FASED  
(IMS, TIMA, Politecnico di Milano),  
1992-1994
Failsafe Integrated Digital Electronics with Semicustoms

BARMINT  
(LAAS Toulouse, TIMA, TIMC, TH Darmstadt, TU Budapest, CNM Bellaterra, LCMM Barcelona, NMRC Cork, TU Lodz),  
1994-1997
Basic Research for Microsystems INTEGRation

AMATIST  
(CNM Sevilla, MESA Institute - Univ. of Twente, TIMA, Univ. of Cantabria, Univ. of Lancaster, Univ. of Pavia),  
1994-1997
Analogue & Mixed-signal Advanced Test for Improving System-level Testability

GRASS (Working Group)  
(Univ. de Las Palmas de Gran Canarias, TIMA, Middlesex University, Techn. Univ. of Denmark, EPFL, Fraunhofer-Gesellschaft Erlangen),  
1994-1997
Gallium arsenide Research action on ASIC Synthesis

ESPRIT-III Research and Development

CHIPSHOP  
(SCME, FhG-IIS, LETI, CMP, CNR-PF, IAM, GAME, INESC, INTRACOM, ElektronikCentralen, CNM, Nordic VLSI, ERA, ULVC),  
1992-1994
A low-cost IC prototyping production service for small and medium sized enterprises.

ESPRIT-III KIT ("Keep-In-Touch")

ARCOS  
(IMEC, TIMA, University of Sao Paulo),  
1995-1997
ARChitectural synthesis of COmplex Systems on silicon

ATAME  
(IMEC, TIMA, Polytechnical Univ. of Madrid, Institute of Microelectronics - Singapore National University),  
1995-1997
Advanced Telecom And Multimedia design technology Environment

ESPRIT-IV KIT ("Keep-In-Touch")

CICDST  
(LIRM, PUC-RS, Univ. Autonoma de Barcelona, ES2, TIMA),  
1997-1999
Library Free Integrated Circuit Design for Submicron Technologies
HIPERLOGIC
(IMS, TIMA, IMC, IPVR, TUB),
1996-1999
Thousand MOPS per MilliWatt CMOS HIgh PERformance LOGIC

ESPRIT-IV Research and Development

COMITY
(VERILOG, AEROSPATIALE, BMW, INTRACOM, C-LAB, DIT/UPM, ISI, TIMA),
1997-1999
Codesign Method and Integrated Tools for Advanced Embedded Systems

TALENT
(ANACAD, AMS, BOSCH, TIMA, MEMSCAP, NMRC, SENSOROR, TUB/DED),
1998-2000
Tools Adaptation and Library development towards microsystems design environment

ESPRIT-IV OMI

JUN2
(CMP, UNED, Archimedes, IMEC, OMIMO, Sussex University, TODITEC and UPM),
1995-1996
Inter University Network

EUROMIC
(CMP, FhG, IMEC, OMIMO, Sussex University and UPM),
1996-1997
EURopean OMI Centres

OMILIBRES
(CMP, Alcatel Mietec, Compass, Mentor, Nokia, SIDS, Telefonica I+D, Thomson-CSF and Viewlogic),
1996-1997
OMI LIBRARY REPRESENTATION STANDARDS

CODAC
(IMEC, CoWARE, ARM, Alcatel-Mietec, SGS-Thomson, Alcatel-Bell, INTRACOM,
TIMA),
1997-1998

ASSISTEC
(IPRIAS Ltd., DOLPHIN INTEGRATION, SEND, SYNDESIS Ltd, TIMA),
1997-1999
Assistance to SMES in the pre-licence phase of the exploitation of their intellectual property

ESPRIT-IV Best Practice

SYSLINK
(GMD, Politecnico di Torino, TIMA),
1995-1997
Linking System Designers and CAD Developers in Europe
CEC/NSF Cooperation

NDIMST
(University of Texas at Austin, TIMA),
1993-1995
New Directions In Mixed Signal Test

CSLS
(University of California at Irvine, TIMA),
1994
Circuit and System-Level Synthesis

JESSI PROJECTS

AC6 : Test generation and design for testability support, 1990-1996.
   Industrial partners:
   Philips, Eindhoven/Hamburg - Siemens, Munich - SNI, Munich - EZM, Villach
   SGS Thomson, Grenoble - Thomson-CSF/TMS - Alcatel/Bell, Antwerp
   Associated partners:
   University of Karlsruhe together with "Forschungszentrum-Informatik" in Karlsruhe,
   University of Hannover, Technical University of München, University of Erlangen-
   Nürnberg, TIMA, Twente University of Technology, Enschede, The Netherlands, Bennetts
   Associates, Southampton.

   Industrial partners:
   Bosch, Reutlingen, SGS-Thomson, Grenoble, Siemens, München, SEL-Alcatel, Stuttgart
   Porsche, Weinach
   Associated partners:
   University of Hannover, TIMA

AC8 : Integrating AMICAL within industrial CAD environment, 1993-1996
   Industrial partners:
   AHL, Bosch, Bull, Philips, Siemens, Siemens-Nixdorf, SGS-Thomson, Synthesia, Thomson-TCS
   Associated partners:
   TIMA

AC3 : HDL, Component Modeling and Libraries, 1996
   Industrial partners:
   Anacad, Bosch, Bull, CNET, IBM France, SGS-Thomson, SPEED, Thomson-SCTF, Thomson TCS
   Associated partners:
   TIMA

AE102/AE103 : Conception de circuits ATM, 1996-1998
   Industrial partners:
   SGS-Thomson, Italtel, Telefonica I+D
   Associated partners:
   TIMA
MEDEA PROJECTS

(STMICROELECTRONICS, BULL SA, METASYMBOISE, LIP6, TIMA),

(STMICROELECTRONICS, TIMA, SIEMENS, PHILIPS),

COMETT PROJECTS

COMETT I

COMET
(IMEC, TIMA, Universities of Darmstadt, Limerick, Lyngby, Madrid).
1988-1990
Consortium for microelectronic training

COMETT II

EUROSYS TEMS
(University of Darmstadt, IMEC, University of Lyngby, TIMA)

EPIQCS : MASTERS DEGREE SPECIALIZED IN QUALITY OF COMPLEX INTEGRATED SYSTEMS
(INPG, Imperial College of London, Universities of Darmstadt and Eindhoven)

EUREKA PROJECTS

MITHRA
(BROSSARD, BERTIN, ITMI, SEIV, LAMM, ELKRON, OLMAT, SEPA, EPFL,
CERBERUS, TIMA),
1988-1990

TEMPUS PROJECTS

ADVANCED JOINT EUROPEAN PROGRAMME FOR MICROELECTRONICS DESIGN METHODOLOGY
(University of Darmstadt, Technical University of Budapest, IMEC, University of Lyngby,
TIMA, Institute of Electron Technology of Warsaw)

MECC (Management, Electronics, Computer science)
(Ecole Polytechnique Feminine, TIMA, Institut Universitaire de Technologie de Cachan,
Ecole Superieure d’Optique d’Orsay, Technische Universitat Munchen, Technische
Universitat Karlsruhe, Universitat Gesamthochschule Duisburg, Friedrich Alexander
Universitat Erlangen-Nurnberg, Fraunhofer Gesellschaft Erlangen, Fachhochschule
Munchen, Universidad Pontificia Comillas, Czech Technical University Prague, Technische
Universitat Dresden, Ingenieurshochschule Mittweida, Technische Hochschule
ILMENAU, Slovak Technical University Bratislava, EMPRESARIOS AGRUPADOS,
SIEMENS AG Erlangen, DORNIER GmbH, CORSE COMPOSITES, PROSPACE,
ONERA, EUROPEAN SILICON STRUCTURES)
INITIATION OF FORMAL TRAINING IN COMPUTER-AIDED ELECTRICAL ENGINEERING IN ROMANIAN UNIVERSITIES
(TIMA, ENSIEG/INPG, Univ. of Bucuresti, Bath, Genova, Cassino, Paris 6 & 11, Graz, EDF, Politecnico di Torino)

COMPUTER-AIDED METHODS AND TECHNICAL MANAGEMENT IN ELECTRICAL ENGINEERING EDUCATION
(Technical Univ. Budapest, Univ. Karlsruhe, Univ. Erlangen-Nürnberg, University College London, TIMA, Univ. of Pisa, Techn. Univ. of Delft, MOTOROLA GmbH, TEXAS
INSTRUMENTS DEUTSCHLAND, HEWLETT PACKARD, DIGITAL EQUIPMENT, IBM)
DIGITAL SYSTEM DESIGN BASED ON PLD-TECHNOLOGY
(technische Hochschule Darmstadt, TIMA, Tallinn Technical Univ.)

EDUCATION FOR QUALITY CONTROL IN ELECTRICAL INDUSTRY (EQUATOR)
(Technical Univ. of Brno, Czech Technical University of Prague, Technical Univ. of Ostrava, Leeds Metropolitan Univ., Bournemouth Univ., TIMA, Univ. of Hull)

POSTGRADUATE EDUCATION IN ASIC DESIGN
(Warsaw Univ. of Technology, Technical Univ. of Lodz, Univ. of Mining and Metallurgy of Cracow, TIMA, Technische Hochschule Darmstadt, Eindhoven Univ. of Technology, Helsinki Univ. of Technology)

EUROQUALROM: EUROPEAN EDUCATION IN QUALITY FOR ROMANIA
(Univ. "POLITEHNICA" of Bucharest, Academy for Economic Studies of Bucharest, Univ. of Oradea, Univ. of Pitești, TIMA, "Ecole Nationale Supérieure des Arts et Métiers" of Paris, Univ. Aberta of Lisbon, Univ. Politecnica de Catalunya of Barcelona, Univ. of Piraeus, Politecnico di Torino, Univ. of Angers, Univ. of Paisley, Romanian Foundation for Quality Promotion of Bucharest, Romanian Society for Quality Assurance of Bucharest, Erasmus Univ. of Rotterdam)

COPERNICUS PROJECTS

COPERNICUS: Cooperation in science and technology with Central and Eastern European countries.

European Conferences, workshops and training seminars:

EDAC-EAST: ATTENDANCE OF CENTRAL AND EASTERN EUROPEAN ENGINEERS AND RESEARCHERS TO THE EDAC CONFERENCE

Mobility scheme for scientists:

DESIGN OF VLSI SELF-CHECKING DIGITAL CIRCUITS
(Stanislaw PLESTRAK, Technical University Wroclaw, Poland)

DEVELOPING DESIGN AUTOMATION TECHNIQUE IN ASIC AND VLSI DESIGN
(Tania VASSILEVA, Technical University Sofia, Bulgaria)

CAD/CAT TOOLS INTEGRATION FOR SENSOR-BASED MICROSYSTEMS
(Teodor CALIN, Polytechnical Institute of Bucharest, Romania)

DEPENDABILITY ANALYSIS OF COMPLEX ELECTRONIC COMPONENTS AND SYSTEMS
(Ioan BACIVAROV, Polytechnical Institute of Bucharest, Romania)
Pan European Scientific Networks:

**EAST EUROPEAN MICROELECTRONICS COOPERATION NETWORK OF SUPPORT AND COMPETENCE CENTRES OF CENTRAL AND EASTERN EUROPEAN COUNTRIES**


Joint Research Proposals:

**FUNCTIONAL TEST GENERATION AND DIAGNOSIS (FUTEG)**

(technical university of Tallinn - Estonia, Kaunas University of Technology - Lituania, Institute of Computer Systems Bratislava, Technical University of Budapest, TIMA, FhG-IIS-EAS Dresden)

1994-1997

**EUROEAST: EXTENSION OF EUROCHIP SERVICES TO CENTRAL AND EASTERN EUROPEAN COUNTRIES**

(GMD, CMP, DTH, IMEC, RAL, Polytechn. Bucharest, ITME Warsaw, Warsaw University, Silesian Tech. Univ., Slovak Tech. Univ.)

**NEW METHODS FOR THERMAL INVESTIGATION OF INTEGRATED CIRCUITS (TERMINIC)**

(technical university of Budapest, Hungary, Technical University of Lodz, Poland, Technical University of Lviv, Ukraine, SEMILAB Budapest, Hungary, TIMA)

1995-1997

**HUMAN CAPITAL AND MOBILITY PROJECTS**

GARDEN: Gallium Arsenide Reliable Design ENvironment

1994-1997

(Univ. de Las Palmas de Gran Canarias, TIMA, PHILIPS Electr. Laboratories, Middlesex University, Techn. Univ. of Denmark, EIDG. Technische Hochschule at Zurich, Fraunhofer Institut für Angewandte Festkörperphysik at Freiburg, Fraunhofer Institut für Integrierte Schaltungen at Erlangen, GIGA at Brondby, Thomson CSF)

**LATIN AMERICA HIGHER EDUCATION PROJECTS**

(Amérique Latine Formation Académique : ALFA)

HUERTA

1998

(Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil; Universidade Federal do Rio de Janeiro/COPPE, Rio de Janeiro, Brazil; Universidade del Valle/NTEDI, Cali, Colombia; Universidad Autonoma Metropolitana, Mexico, Mexico; Univ. Catholique de Louvain, Louvain La Neuve, Belgium; TIMA; Technische Hochschule Darmstadt, Darmstadt, Germany; Universidade de Aveiro, Aveiro, Portugal)

Higher University Education and Research Training Action
FLACIAC
1998
(Universidad Nacional de Rosario, Instituto de Física de Rosario, Rosario, Argentine; Universidad de Chile, Facultad de Ciencias Físicas y Matemáticas, Departamento de Ingeniería Eléctrica, Santiago, Chile; Escuela de Ingeniería "Mcal. Antonio José Sucre", La Paz, Bolivia; Universidad de Guadalajara, Centro Universitario de Ciencias Exactas de Ingeniería, Mexico; TIMA; School of Engineering, University of Wales Cardiff, UK; Technische Universität Clausthal, Institut für Elektrische Informationstechnik, Germany; Universidad Politécnica de Madrid, Departamento de Señales Sistemas y Radiocomunicaciones, Madrid, Spain)

European-Latino American Cooperation for Intelligent Automation and Control.

V-2.2.2 New European Projects or European Projects still ongoing in 2001

ESPRIT PROJECTS

ESPRIT-IV KIT ("Keep-In-Touch")

DETERMIN

(Technical University of Budapest, TIMA), 1998-2001

DEvelopment of Tools and Expertise for the therMal investigation of ICs and microsystems based on the results of the THERMINIC project

In the framework of this KIT project the Partners will continue the cooperation started in the THERMINIC CP940922 COPERNICUS project.
The scientific and technical objectives of the DETERMIN project on the basis of the THERMINIC project can be summarised as follows:
- to step forward in the development of novel measurement and simulation tools based on the results of the THERMINIC,
- to carry on with the thermal characterisation of IC packages with the help of the thermal benchmark chip developed in the THERMINIC project,
- to study further the feasibility of integrating temperature sensors into safety-critical, self-checking systems and to develop self-checking versions of the temperature sensors developed in the framework of the THERMINIC project,
- to exploit new ideas in the field of IDDQ testing,
- to continue the series of the THERMINIC workshops.

LIMITE

(LIRMM, TIMA, ATMEL ES2, UAB, PUC-RS), 1998-2001

Library Free Integrated Circuit Design for Submicron Technologies

This project will concentrate the research effort in low level synthesis, specially by improving the current state-of-the-art in this field, developing strategies for library free mapping, virtual libraries, automatic layout synthesis for submicron technologies and performance optimization.
The use of CMOS modern technologies, allowing high integrated densities, makes necessary the mastering of performance management. This mostly concerns speed and power parameters, taking into account the non-linearity induced by submicron processes. For that, designs must be controlled by these parameters.

In the same order of idea, the performance of a circuit is a function of the different number of cells available into the library used as a reference for the circuit mapping. Management of complex libraries, making available all the complex gate resources, is not possible. The main problems are the great number of logic gates in function of the number of serial transistors, and the need to have different templates for each cell in order to have different solutions for delay, area and power. Moreover, it has been shown that complex gates constitute a good solution for low power implementation.

To make this alternative possible, we propose the use of a library free design methodology, allowing complete use of the resources available at the transistor level. This library must be constituted by virtual cells, with all available sizes and well characterised performances. This feature can be used to reach the specified performances of a circuit under design.

The development of such library is only possible if it is available a macro-cell generator of regular structures, with predictable performances, allowing full sizing of the different cells for optimal control of the power and delay.

IST PROJECTS

MATISSE
(DERA, Univ. of Southampton, TIMA/CNRS, Aabo Akademi Univ., MATRA Transport International, STERIA), 2000-2002

Methodologies and technologies for industrial strength systems engineering

The core objective is the development of industrial strength methodologies and associated technologies for the engineering of software-based critical systems. These methodologies and technologies will support industry in providing essential services for the information society of the Third Millennium that are highly dependable and therefore lead to increased public confidence and trust in the services.

The project will make significant use of rigorous, mathematically-based software engineering techniques, so-called formal methods, that support validation throughout the development life-cycle by providing rigorous specification and design notations as well as proof techniques, model-checking techniques and simulation techniques.

The driver for the research and development in MATISSE will be four major industrial case studies representing a spectrum of the essential services for the information society.

PROFIT
(Phillips Electronics Nederland B.V. (Philips), ST Microélectronis s.r.l.(ST Italy), Infineon Technologies AG (Infineon), Philips Semiconductors B.V.(philips sc), Flomerics Ltd. (Flomerics), Technical University of Budapest (TUB), Mic red Microelectronics Research and Development Ltd (Micred), INPG/TIMA, Centre for Quantitative Methods B.V. (CQM), Nokia Corporation (Nokia)), 01/01/2000-31/12/2002

Prediction of temperature gradients influencing the quality of electronic Products
Many business objectives related to safety, performance and reliability of electronic products are a function of temperature. Higher accuracy in temperature predictability gives better control of design and manufacturing. Higher-quality products have a positive impact on the product's life-cycle-cost and people's quality of life. Industrial problems, and solutions offered by PROFIT:
- Cost/weight reduction with better quality: Significant improvements in temperature prediction for virtual prototyping,
- Physics-based prediction of reliability: accurate predictability of temperature gradients in time and space,
- Yield improvement of packages: better-defined rejection criteria based on in-line quality testing,
- Awareness of problems due to the absence of useful design specs: dissemination of combined thermal expertise in EU,
- Standardization of thermal characterization: continuation of international contacts through one European voice.

ACID-WG
(South Bank University, UK),

Working group on Asynchronous circuit Design

ACID-WG aims at improving the systematic exchange of information and the forging of links between teams with carry out RTD or take-up activities around the theme of asynchronous circuit design. Its objectives in FPS are as follows:
1. To encourage excellence in science and technology research pertaining to asynchronous circuits and systems.
2. To facilitate the development of methods and tools that are usable by engineers for the design of asynchronous VLSI systems.
3. To promote the adoption of asynchronous circuit design in industry.

FRACTURE : Nanoelectronic Devices & Fault-Tolerant Architectures
(National Centre for Scientific Research “DEMOKRITOS”, University of Durham, Iro Technologies, UJF/TIMA),
01/01/2001-31/12/2003

Develop a new inexpensive technology for the fabrication of non-volatile memories based on hybrid silicon and molecular nanotechnology and combine it with mainstream CMOS using wafer bonding at low temperature to make 3-D stacks.
Develop fault-tolerant architectures suitable for low yield non-volatile memory device fabrication processes.
Develop high throughput nanofabrication techniques using optical lithography and self limited etching techniques for Si nanostructure fabrication.
Investigate molecules used at room temperature as charge storage elements and integrate them on top of a Si channel to demonstrate a non-volatile nano-flash memory device.
MEDEA+ PROJECTS

T 101 : TECHNODAT
(CISC, FHG, HIRESH, INFINEON, IROC, ISD, PHILIPS, ST, TIMA),
2001

Project n° 2 : Low-cost test solutions for systems on silicon

The evolution of technology towards a higher density and new materials is resulting in a flow of new constraints that should be taken into account at design level. The right technology-dependent environments are necessary not only to accelerate or secure today’s designs, but also to make future designs simply feasible.

The goal of this Project is to allow designers to get the best benefits of the new technologies (down to 0.07 μ), without additional overload. This strong consortium will guarantee efficient know-how transfer from academic research down to production level. The Project consists in combining 3 challenges:
- A know-how acquisition challenge concerning local and interdependent physical modeling down to 0.07 μ: e.g. new materials (e.g. SOI), stringent needs for new parasites extraction to reach timing closure, upgrade of 2-D modeling to 3-D
- An industrial challenge to cope with exploding product complexities and performance figures for an ever faster going market place (bigger cells, more views, more types of cells, higher speeds) and with new kinds of team-working (SOC, reuse, distributed teams)
- A clear market

A 302 : Esp@ssIS (Enhanced SmartCard Platform for Accessing Securely Services of the Information Society)
(STMICROELECTRONICS, SCHLUMBERGER, BULL CP8, CELA-LETI, THOMSON MULTIMEDIA, TRUSTED LOGIC, PHILIPS CONSUMER ELECTRONICS, INTERPAY, TELECOM ITALIA MOBILE, SMART TRUST, TIMA),
2001

The EsP@ss-IS project’s primary goal is to provide open smart-card platforms (both hardware and software) to support the development of value added electronic and mobile commerce services. On a secondary level the development of the open smart-card platforms will provide a set of reusable innovative technological bricks from which future generations of high security smart-card products may be created.

A 502 : MESA (Multi-processor Embedded Systems Architectures)
(ALCATEL, BULL, COWARE, EDSN, EONIC, EPUN/MCSE, FRONTIER-DESIGN, IMEC, INRIA, KU-Leuven, METASYMBIOSE, PHILIPS, POLYSAPCE, STMicroelectronics, UJF/TIMA, UPMC/LIP)
2001-2004

To meet the huge computational capabilities of the 100 nm IC generation, together with exploding market needs, efficient design methods for reconfigurable multi-processor architectures are urgently needed: today, when a multi-processor architecture is targeted, no satisfactory solution is available for analysing the application domain, providing reconfigurable IP blocks, defining communication protocols, and validating the resulting solution. This Project aims at providing flexible design platforms for multi-processor architecture design, in order to fill this gap. Each new environment delivered by the project will be driven by an industrial test-case in
these application fields: Telecom terminals, Digital Radio Communication Networks, Consumer and Computer.
TIMA will investigate the formal validation of the initial specifications and early design steps, when the system behavior is given in terms of abstract functions, prior to making bit accurate decisions on the data path, or cycle accurate instruction set architectures. We propose to combine simulation of test cases, symbolic simulation and theorem proving, as complementary techniques applied to a variety of system level specification formalisms.

V-3 International cooperation agreements

The Laboratory is engaged, or has been recently engaged, in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations allow to remote researchers at the cooperative location for in-deep fruitful exchanges of results, to organize joint research and Workshops.

Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with R. REIS, on the automatic design of integrated circuits.

Universidade Federal do Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with A. MESQUITA, on high level synthesis and test of integrated circuits.

Ecole Nationale d'Ingénieurs de Monastir (ENIM), Monastir, Tunisia
This cooperation takes place in the framework of a project sponsored by the French ministry for education and research and the Tunisian ministry for research and technology, cooperation program which name is "Réseaux Formation-Recherche franco-tunisiens", with S. NASRI, on computer-aided design of communication-dedicated circuits.

University of California at Berkeley, USA
A research project entitled « Multi-standard verification environment for digital system design » is supported by the France-Berkeley Fund. This cooperation is carried out with the group of Robert BRAYTON, on the topic of model checking from Verilog and VHDL.

Universidad Politecnica de Catalunya (UPC/ETSI), Spain
This cooperation (PICASSO) is carried out with J. CABESTANY on the study of Robustness of Digital Implementation of artificial neural networks, with exchanges of students and researchers between TIMA and UPC.

Faculté des Sciences de Monastir, Tunisia
This cooperation takes place in the framework of TEMPRA, between France and Tunisia. The project deals with FPGA to ASIC retargetting, with Electronic and Microelectronic Laboratory: M. ABID.

Ngee Ann Polytechnic, Singapore
This cooperation includes the exchange of staff members and students.

University of Tripoli, Lebanon
This cooperation is about a test system for the validation of computers based on microprocessors in space, Professor Z. HAISSAM.
University "Polytechnica" of Bucharest, Romania
This collaboration consists of a project focused on architectures based on quantum devices with Prof. R. CHISLEAG and a TEMPUS project, "EUROPEAN EDUCATION IN QUALITY FOR ROMANIA", with Prof. I. BACIVAROV.

Budapest University of Technical and Economics (BUTE), Hungary
This cooperation takes place in the framework of the PhD work of L. ANTONI, co-directed by R. LEVEUGLE at TIMA and B. FEHER at BUTE (Department of Measurement and Information Systems). The project deals with run-time reconfiguration of FPGAs for fault injection applications.

Technical University of Budapest, Hungary
This cooperation takes place in the framework of BALATON, between France and Hungary. The project deals with thermal test dies, with the Department of Electron Devices: V. SZEKELY and M. RENZ.

Politecnico di Torino, Italy
This cooperation takes place in the framework of GALILEE, between France and Italy. The project deals with validation of an automated technique for the realization of robust software devoted to high-safety applications with the Dipartamento di Automatica e Informatica: M. SONZA REORDA.

V-4 National cooperation

Project on Quantum Computing Technology

A new project has been started end of 2000 / beginning of 2001 on quantum computing technology in cooperation with a Computer Science Laboratory, LEIBNITZ (http://www.imag.fr/leibniz), located in Grenoble. The long term goal is to study how quantum electronics can be used to build quantum computing structures. One paradigm to explore is the tradeoffs between the complexity of algorithms when moving to quantum computing compared to the complexity of hardware when moving to quantum electronics to execute quantum algorithms. Informal contacts are also taken with CRTBT (http://www-crtbt.polycerns-gre.fr/), a fundamental physics Laboratory in Grenoble, where superconducting nano-circuits are studied in order to realize quantum bits.

The French CAD Network

A network of French Laboratories had been set up in 1995 by the Ministry for Research and Education in the field of CAD for integrated circuits and systems. These Laboratories are CSI in Grenoble, ENST in Paris, IEMN in Lille (Villeneuve d'Ascq), LIRMM in Montpellier, MASI in Paris, and TIMA in Grenoble acting as the contractor to the Ministry. On January 1998, the initial network has been completed by more laboratories, namely ENSEA, INSA Toulouse, IRESTE, IRISA, I3S, LAMI, LASTI, LCIS, LESTEA, LIM, LIP, to constitute a group of Laboratories supported by CNRS. The group is led by TIMA. The main topics for research are the design of mixed systems (hardware-software, microelectromechanical-analog), and CAD for deep submicron.
V-5 International activities

This section gives an overview of national and international activities to which participated recently the members of the Laboratory.

Participation to Committees for Conferences and Workshops

- European Conference on Design Automation (EDAC): 1990 (Glasgow), 1991 (Amsterdam), 1992 (Brussels)
- European Design for Testability Workshop (E-DFT): 1990 (Segovia), 1992 (Brugge), 1996 (Montpellier), 1998 (Stuttgart)
- European Solid-State Circuits Conference (ESSCIRC): 1986 (Delft), 1990 (Grenoble), 1995 (Lille), 1997 (Southampton)
- International Conference on Microelectronics (ICM): 1991 (Cairo), 1992 (Monastir), 1993 (Dahran)
- International Workshop on FPGAs and Applications: 1992 (Vienna), 1994 (Prague), 1996 (Darmstadt)
- European Workshop on Dependable Computing (EWDC): 1989 (Toulouse)
- CEC CAVE (CAD for VLSI in Europe) workshops (CAVE): 1983-1988
- Memory Testing: 1993-1995 (San Jose), 1996 (Singapore), 1997-2001 (San Jose)
- High Level Synthesis Workshop: 1994 (Niagara Falls), 1995 (Cannes), 1996 (La Jolla)
- EuroDAC-EuroVHDL: 1994 (Grenoble), 1995 (Brighton), 1996 (Geneva)
- Workshop on Hardware-Software Codesign: 1994 (Grenoble)
- Simulation in Electronics: 1994 (Santander)
- Asia Pacific Conference on Hardware Description Languages (APCHDL): 1995 (Brisbane), 1994 (Toyohashi), 1996 (Bangalore), 1997 (Taiwan), 1998 (Seoul)
- International Conference on Probabilistic Safety Assessment and Management: 1991 (Beverly Hills), 1996 (Greece)
- European Safety and Reliability Conference (ESREL): 1996 (Greece), 1997 (Lisbon), 1998 (Trondheim), 1999 (Munich)
- International Conference on ASIC (ASICON): 1996 (Shanghai), 1998 (Beijing), 2001 (Shanghai)
- IEEE Multi-Chip Module Conference (MCMC): 1995-1997 (Santa Cruz)
- MCM Test: 1995-2000 (Napa Valley)
- High Level Design Validation and Test Workshop (HLDVT): 1996-2000 (Oakland)
- Signal Propagation on Interconnects (SPI): 1997-1998 (Travemünde)
- SPIE Conference on Micromachining and Microfabrication: 1996-1997 (Austin)
- Low Dimensional Structures and Devices (LDSD): 1995 (Singapore), 1997 (Lisbon)
- INTERPACK Conference: 1997 (Mauna Lani), 1999 (Maui), 2001 (Kauai)
- MICRO SYSTEM Technologies: 1998 (Postdam)
- IC/Package Design Integration (IPDI): 1998-1999 (Santa Cruz)
- IFIP WG10.2 International Working Conference "The fusion of hardware design and verification": 1988 (Glasgow)
- IFIP TC10 Conference "Design Methodologies for VLSI and Computer Architecture": 1988 (Pisa)
- "VHDL Forum for CAD in Europe": 1989 to 1998 (annual)
- IFIP WG10.2 Advanced Research Workshop on Correct Hardware Design Methodologies: 1992 (Torino), 1993 (Arles)
- IFIP WG10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME): 1995 (Frankfurt), 1997 (Montreal), 1999 (Bad Herrenalb)
- Radiation Effects on Circuits and Systems (RADECS): 1997 (Cannes)
- Nuclear and Space Radiation Effects Conference (NSREC): 1997 (Snowmass)
- Design and Diagnostics of Electronic Circuits and Systems Workshop (DDECS): 1997 (Bratislava), 1998 (Szczecin), 1999 (Bratislava), 2001 (Győr)
- Southwest Symposium on Mixed-Signal Design (SSMSD): 1999 (Tucson), 2000 (San Diego)
- Conference on Advanced Research in VLSI (ARVLSI): 1999 (Atlanta)
- International Conference on Mathematical Methods in Reliability (MMR): 1997 (Bucharest)
- International Conference on Quality and Safety: 1999 (Paris)
- IEEE Symposium on Quality of Electronic Design: 2000-2001 (San Jose)
- Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM): 2000 (Las Vegas)
- Smart Electronics & MEMS Conference: 2000 (Melbourne)
- International Conference on Quality, Reliability and Maintainability-CCF: 2000 (Sinaia)
- IEEE Latin-America Test Workshop (LATW): 2001 (Cancun)
- Asia Pacific Symposium on Microelectronics and MEMS (MICRO/MEMS): 2001 (Adelaide)
- IEEE Conference on Nanotechnology (NANO): 2001 (Maui)

European representation (or liaison) to Conferences and Workshops

- Built-In-Self-Test Workshop (several issues)
- Asian Test Symposium (several issues)
- High-Level Design Validation and Test Workshop (several issues)
- VLSI Design (several issues)
- MCM Conference (several issues)
- IC/Design Package Integration (1998)
- INTERPACK (1999, 2001)
- Memory Technology, Design and Testing (several issues)
- International Workshop on System Test and Diagnosis (1998)
- ICCAD (1996-1997)
- IITHERM (2000, 2002)
- Steering Committee Member of the SASIMI Workshops (Japan)

Participation to Editorial Boards of Journals and Book Series

- CDTA
- Journal of Microelectronic Systems Integration
- IEEE Design and Test of Computers Magazine
- Journal of The Brazilian Microelectronics Society
- Computational Mechanics Publications
- Microelectronics Journal (Editor-in-Chief)
- IEEE Press Book Series
- Formal Methods in System Design
- ASME Journal of Electronic Packaging
- GRETSI Traitement du Signal
Organisation of Conferences

- Electron and Optical Beam Testing of Integrated Circuits (EOBT): 1987 (Grenoble, General Chair), 1989 (Daiseburg, Program Chair), 1991 (Como, Program Chair), 1993 (Zurich, Program Chair), 1995 (Wuppertal, Program Chair)
- EUROCHIP Workshop on VLSI Design Training (General Chair) (EUROCHIP): 1991-1992 (Grenoble), 1993 (Toledo), 1994 (Dresden)
- European Conference on Design Automation / EUROASIC (EDAC-EUROASIC): 1993 (Paris, General Chair)
- Rapid System Prototyping Workshop (RSP): 1994 (Grenoble, General Chair), 1996 (Thessaloniki, Program Chair)
- International Symposium on System Synthesis (ISSS): 1995 (Cannes, Program Chair), 1996 (La Jolla, General Chair)
- IEEE Mixed-Signal Test Workshop (IMST): 1995 (Grenoble, General Chair)
- IEEE Workshop on On-Line Testing (IOLT): 1995 (Nice, General Chair), 1996 (Biarritz, General Chair), 1997 (Crete, General Chair), 1998 (Capri, General Chair), 1999 (Rhodes, General Chair), 2001 (Taormina, General Chair), 2002 (Isle of Bendor, General Chair)
- Workshop on Thermal Investigations in ICs and Systems (THERMINIC): 1995 (Grenoble, General Chair), 1996 (Budapest, General Chair), 1997-1998 (Cannes, General Chair), 1999 (Rome, General Chair), 2000 (Budapest, General Chair), 2001 (Paris, General Chair)
- VLSI Test Symposium (VTS): 1995-1996 (Princeton, Vice-Program Chair), 1997 (Monterey, Program co-Chair), 1998 (Monterey, Program Chair), 1999 (Dana Point, General Chair)
- Euro-VHDL: 1996 (Geneva, Program Chair)
- European Workshop on Microelectronics Education (EWME): 1996 (Grenoble, Co-Program Chair), 2000 (Aix en Provence, Co-Organizer)
- Colloque CAO de circuits intégrés et systèmes: 1996 (Grenoble – Villard de Lans, Organizer), 1999 (Aix en Provence, Organizer)
- NATO ASI Course on Low Power Design in Deep Submicron Electronics: 1996 (Lucca, Organizer)
- Copernicus Summer School: EDA standards, 1997 (Prague, Organizer)
- MEDEAS-ESPRIT Workshop on Hardware-Software Codesign: 1998 (Grenoble, Chair)
- Design Automation and Test in Europe (DATE): 1998 (Paris, Vice-Program Chair), 1999 (Munich, Program Chair), 2000 (Paris, Vice-General Chair), 2001 (Munich, General Chair)
- CODES: 1998 (Seattle, Co-Chair), 1999 (Rome, Co-General Chair)
- Modeling and Simulation of Microsystems, Semiconductors, Sensors and Actuators (MSM): 1999 (Puerto Rico, Co-Chair)
- NATO ASI Course on System Level Design: 1998 (Organizers)
- Asia Pacific Symposium on Microelectronics and MEMS (MICRO/MEMS): 1999 (Gold Coast, Characterisation and Test Conference co-Chair)
- Radiation Effects on Circuits and Systems (RADECS): 2001 (Grenoble, General Chair)
- Forum on Design Languages (FDL): 1999 (Lyon, General Chair)
- IFIP ICAD: 2000 (Beijing, Co-Program Chair)
- Design, Test and Microfabrication of MEMS/MOEMS (DTM): 1999 (Paris, General Chair)
- Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP): 2000 (Paris, General Chair), 2001 (Cannes, General Chair), 2002 (Cannes, General Chair)
- International Symposium on Microelectronics and Assembly (ISMA): 2000 (Singapore, Program Chair)
- Memory Technology, Design and Testing (MTDT): 2001 (San José, Co-General Chair), 2002 (Isle of Bendor, General Chair)
- International Symposium of Defect and Fault Tolerance in VLSI Systems (DFT): 2001 (San Francisco, Co-Program Chair), 2002 (Vancouver, Co-General Chair)
- IEEE Latin-America Test Workshop (LATW): 2002 (Montevideo, General Chair)
- Thermal Challenges in Next Generation Electronic Systems (THERMES): 2002 (Santa Fe, Program Co-Chair)
- High-Level Design Validation and Test (HLDV'T): 2002 (Cannes, General Chair)
- ACL2 Theorem Prover and its Applications (ACL2): 2002 (Grenoble, Co-General Chair)
- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES): 2002 (Grenoble, Co-Program Chair)
- Thermo-mechanical issues in Packaging and Assembly of MEMS and MOEMS, part of Photonics Fabrication Europe: 2002 (Brugge, Conference Chair)

Participation to Societies and Working Groups

- Member of IEEE/CS, IEEE/CPMT, ACM, IMAPS
- Member of IEEE European Test Technology Technical Committee
- Vice-Chair of Technical Activities of the IEEE Test Technology Technical Committee
- Chairman of the European Design and Automation Association (1994-1995)
- Chair of Thermal Testing Activities of the IEEE Test Technology Technical Committee
- Chair of IFIP 10.5 Working Group
- Member of IEEE WG 1076.6: VHDL subset for Synthesis

Others activities

- Review of papers for numerous Journals and Conferences
- Review of research proposals for CEC, NSF, NATO, SERC
- Member of the STMicroelectronics Technology Council

V-6 Awards and distinctions

- IEEE Meritorious service awards (1993)
- Doctor Honoris Causa of the Technical University of Budapest (1994)
- IEEE Computer Society's Golden Core member (1996)
- Best Paper Award ED&TC, 1995
- Best Poster Award IMAPS (1998)
- Best Poster Award FDL (1999)
- Best Paper Award DATE (1999)
- Award by Schlumberger Stiching Fund (1999)
- Best Paper Award DATE (2000)
- Best Paper Award HDLCON (2000)
Picture V-5 1

Picture V-5 2
As part of the international activities, Ahmed JERRAYA helps in preparing a New-Year’s cake at the SASIMI Workshop (OSAKA, 1997) (Picture V-5 1) and Bernard COURTOIS is conducting the sake barrel break (Picture V-5 2) of Kagamiwari, a sake ceremony, after an address (Picture V-5 3) at the SASIMI Workshop (Tohoku, 1998)
Pictures V-6 1:
Bernard COURTOIS is being awarded Doctor Honoris Causa
of the Technical University of Budapest

Picture V-6 2:
Later, the President of INPG, Maurice RENAUD, congratulates
him by remitting a sash, made to the colours of the city of Budapest
Picture V-7:

R. BIANCHI, congratulated at the end of his thesis defence by Mr. Eric DONZIER from Schlumberger.

R. BIANCHI has been awarded by Schlumberger for his results on the design of high temperature circuits systems.
VI - TECHNOLOGY TRANSFER ACTIVITIES

Besides their research and service activities, TIMA staff members are also concerned with technology transfer activities. For that purpose, they are regularly solicited to serve as consultant for technical and educational tasks, mainly by industrial companies, but also by foreign universities. Some results of these tasks have already been evoked throughout this report for the sake of consistency of the different sections, others only appear in this section.
Up to now, the transfer technology activities have taken the forms detailed in the following:

VI-1 Technical tasks

VI-1.1 Industrial Transfers

- Transfer of a set of codesign tools to Arexsys a TIMA spin-off. These include:
  1. COSMOS : a SDL based codesign environment.
  3. MCI : a multilanguage cosimulation tool supporting C, VHDL, MATLAB, SDL and COSSAP.

- VIN, an early C-VHDL cosimulation tool was transferred to STMicroelectronics since 1995. It was productized and used in several divisions in Grenoble and Bristol.

- Hits cells: Heavy ion tolerant memory cells, to Matra MHS/TEMIC. Hit memory cells were used to design a radiation hardened version of a digital signal processor: the TSC 21020 commercialised by TEMIC since November 1998.

VI-1.2 Patents

TIMA Laboratory staff members have filed the following patents:

<table>
<thead>
<tr>
<th>Title</th>
<th>Publication Date</th>
<th>Patent Number</th>
<th>Equivalent(s)</th>
<th>Author(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Printed circuit tester comprising stack of elastic sheets - has test point matrix card for each face of circuit sandwiched between compressed sheets conducting vertically</td>
<td>13/01/89</td>
<td>FR2617977</td>
<td>WO8900296</td>
<td>Vaucher Ch., Balme L., Motari J.Y., Pondaven P.</td>
</tr>
<tr>
<td>High-security operation frequency-coding system</td>
<td>05/09/90</td>
<td>EP03855885</td>
<td>FR2643762</td>
<td>Nicclaidis M., Novoz S.</td>
</tr>
<tr>
<td>Circuit testing device for printed circuits - has different density test blocks linked to detachable modules arranged in lines or columns on test bed</td>
<td>09/10/92</td>
<td>FR9212549</td>
<td>EP93420394</td>
<td>Vaucher Ch.</td>
</tr>
<tr>
<td>Memory cell insensitive to collisions of heavy ions</td>
<td>18/03/93</td>
<td>FR930003333</td>
<td>US950532726</td>
<td>Bessot D., Velazco R.</td>
</tr>
<tr>
<td>Test grid for tester of unpopulated printed circuits</td>
<td>30/07/93</td>
<td>FR930909571</td>
<td>EP94010055</td>
<td>Vaucher Ch.</td>
</tr>
<tr>
<td>Implementation techniques of self-checking arithmetic operators and data paths based on double-rail and parity codes</td>
<td>28/10/93</td>
<td>US5450340</td>
<td>WO9321576 GR920100163 EP0591490</td>
<td>Nicolaidis M.</td>
</tr>
<tr>
<td>Fail safe interface for appts control - has inputs for receiving two binary control signals and concurrent checker which provides error detection signal if error exists in input signals</td>
<td>09/03/95</td>
<td>WO9506908</td>
<td>GR93100359 GR920100163</td>
<td>Nicolaidis M.</td>
</tr>
<tr>
<td>Supply component of the credit card type</td>
<td>12/09/95</td>
<td>US5449994</td>
<td>DE69207101D</td>
<td>Amand M., Balme L., Silvy C.</td>
</tr>
<tr>
<td>Transparent techniques of integrated circuits</td>
<td>21/11/95</td>
<td>US5469445</td>
<td>EPO585435 GR92100088 WO9318457</td>
<td>Nicolaidis M.</td>
</tr>
<tr>
<td>Correction d'erreurs dans une mémoire</td>
<td>15/12/95</td>
<td>FR2721135</td>
<td>EP0765497 WO95334858 DE6950239T</td>
<td>Vargas F.L., Nicolaidis M.</td>
</tr>
<tr>
<td>Micromechanical ring oscillator sensor</td>
<td>15/04/98</td>
<td>GB2318231</td>
<td></td>
<td>Moore D.F., Daniel J., Karam J.M.</td>
</tr>
<tr>
<td>Capteur thermoélectrique notamment pour appareils électriques</td>
<td>19/11/99</td>
<td>FR2778742</td>
<td></td>
<td>Hazard Ph., Karam J.M., Veychard D.</td>
</tr>
<tr>
<td>Composant micro-électronique intégrant des moyens de traitement numérique asynchrone et une interface de couplage électromagnétique sans contact</td>
<td>01/01/2000</td>
<td>FR 99/08485</td>
<td></td>
<td>Abrial A., Beuvier J., Senn P., Renaudin M., Vivet P.</td>
</tr>
</tbody>
</table>

**VI-1.3 Industrial Circuit Fabrication**

In addition to its service activity for university and research laboratory circuit fabrication, CMP is offering circuit fabrication services for industrial circuit prototyping and low volume production. CMP opened the service to Industry in 1990. In 2001, 74 industrial circuits, 40 from France and 34 from foreign countries, were fabricated for 29 industrial companies or national research laboratories. They were manufactured for prototyping or low volume production. Starting from 1993, more than 500 industrial circuits have been fabricated, in CMOS, BICMOS, and GaAs technologies, for 82 companies and 16 universities/research laboratories. Also low volume production is strongly increasing: in 2001, 21 Institutions submitted 32 circuits for low volume production instead of 9 and 23 respectively in 2000.
VI-1.4 Consulting

The following consulting tasks have recently been achieved:

<table>
<thead>
<tr>
<th>Company</th>
<th>TIMA member</th>
<th>Duration</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMS (Austria)</td>
<td>K. Torki</td>
<td>8 months</td>
<td>91-93</td>
</tr>
<tr>
<td>IN2P3/LAL (France)</td>
<td>K. Torki</td>
<td>5 days</td>
<td>04/92</td>
</tr>
<tr>
<td>Alcatel/Alsthom (France)</td>
<td>M. Nicolaidis</td>
<td>2 days</td>
<td>07/94</td>
</tr>
<tr>
<td>Mentor Graphics Corp.</td>
<td>M. Nicolaidis</td>
<td>10 days</td>
<td>96-97</td>
</tr>
<tr>
<td>Univ. of Rome</td>
<td>K. Torki</td>
<td>6 days</td>
<td>98</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>2 months</td>
<td>98</td>
</tr>
<tr>
<td>CEA/LETI</td>
<td>K. Torki</td>
<td>2 weeks</td>
<td>99</td>
</tr>
<tr>
<td>ESRF</td>
<td>K. Torki</td>
<td>8 weeks</td>
<td>99</td>
</tr>
<tr>
<td>ESF</td>
<td>K. Torki</td>
<td>3 weeks</td>
<td>99</td>
</tr>
<tr>
<td>CORNING SA</td>
<td>K. Torki</td>
<td>1 week</td>
<td>99</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>M. Nicolaidis</td>
<td>8 days</td>
<td>99</td>
</tr>
<tr>
<td>VDEC - Tokyo -Japan</td>
<td>K. Torki</td>
<td>2 days</td>
<td>2000</td>
</tr>
<tr>
<td>Univ. of Tohoku - Japan</td>
<td>K. Torki</td>
<td>1 day</td>
<td>2000</td>
</tr>
<tr>
<td>iRoC Technologies</td>
<td>R. Velazco</td>
<td>1 month</td>
<td>03/01</td>
</tr>
</tbody>
</table>

VI-1.5 Creation of spin-off companies

These start-up companies have been recently created by members of the Laboratory. The Press Releases issued at the time of the launching are reproduced below.

VI-1.5.1 MEMSCAP

MEMSCAP™: a TIMA spin-off specialized in MEMS

Grenoble, France - December 1997. The challenges in Telecommunication, Automotive, Aerospace and Biomedical system design using Micro Electro Mechanical Systems (MEMS) have been clearly identified. To address this increasing demand, MEMSCAP™, a commercial spin-off from TIMA Laboratory research, provides Intellectual Properties (IP) enabling system designers to get access to the MEMS technology without excessive complexity and design time and cost. Very wide range temperature sensors, IR detectors, inertial sensors and other MEMS devices can be directly purchased in both software or hardware forms.

The company is starting with 7 engineers, mainly composed from researchers getting out from the Microsystems Group of TIMA Laboratory. This group will keep a staff of 15 researchers addressing joint long and medium term research activities on CAD of MEMS, fault modeling, MEMS testing methodologies, microelectronics compatible manufacturing techniques and new MEMS device generations (e.g. Active Pixel Sensors, etc.). In addition, the CMP service will be the preferred source for prototyping and low-volume production of Integrated Circuits, MEMS and Multi-Chip-Modules for MEMSCAP™.

MEMSCAP™ design solution enables system designers to fully leverage MEMS component behavioral models in HDL-A¹ (soon into VHDL-AMS and Verilog-A standards) for system-level

¹ HDL-A is a registered trademark of Mentor Graphics Corporation.
verification and manufacturability analysis, by providing technology specific MEMS Engineering Kits, Model Generation Tools and Services and MEMS Intellectual Properties.

MEMSCAP® is predicting 10 million dollars of turn-over in 2001. The company has already received the support of the Centre National d'Etudes Spatiales (CNES) in France, for the qualification of space technologies for MEMS and has established a partnership with Mentor Graphics Corporation in the area of CAD of MEMS.

VI-1.5.2 AREXSYS

Start-up forms in Grenoble, France to deliver system design software for embedded systems

San-Frainsisco, CA (Design Automation Conference) - June 15, 1998 - The founders of the Syntyx Technology project in Grenoble, France, today announced the formation of Arexsys, Inc. to deliver an innovative hardware/software co-design solution for embedded system and system-on-chip (SOC) designs.

François Constant, formerly regional manager of Southern Europe for Synopsys Inc., was named president and chief executive officer. In addition to Constant, Arexsys founders include Ahmed Jerraya, research director at the TIMA laboratory, and Jean-Pierre Moreau, director of research partnerships at STMicroelectronics.

Arexsys' solutions are used as a high level front-end to industry standards EDA tools such as register-transfer level (RTL) synthesis and digital signal processing (DSP) design tools. The technology supports a full top-down system design methodology, reading and writing multi-languages description and performing co-simulation at any level.

In contrast to other system-level design products that use proprietary languages, the Arexsys tools use SDL, the industry standard design language used by more than 25,000 system designers worldwide.

Currently, system-level designers write SDL description to map out the major functional blocks in the system and then have to painstakingly hand-code a behavioral or RTL description, deciding piece by piece what gets implemented in hardware vs. software. Arexsys automates this process: the tools read in an SDL description, designers interactively partition the design into hardware and software, and the tools then compile the design into RTL hardware and low-level C software. Designers then send the RTL hardware portion to a hardware description language (HDL) synthesis tool to create gates.

Arexsys automatically generates the interfaces required for communication between the hardware and the software at the RT level. Designers can explore different combinations of hardware and software along the way until the optimum solution is reached.

The company expects to have its products into beta sites this summer, and to have production software ready by end of 1998.

VI-1.5.3 iRoC Technologies ®

A new start-up takes on soft errors challenge

Grenoble, France - March 13, 2000 - iRoC Technologies is providing unique and global design solutions for Integrating Robustness on Chip, and is taking on one of the biggest challenges in the semiconductor industry: the “transient errors” issue.

Soft Errors, coming from cosmic rays or alpha particles, and timing faults, coming from crosstalk, may stop the very deep submicron scaling progress.

A commercial spin-off from TIMA laboratory research in Grenoble, France, iRoC Technologies offers a new design methodology to provide a breakthrough, by using fault tolerance concepts.

Michael NICOLAIDIS, leader of the Reliable Integrated Systems group at TIMA Laboratory warns that technological progress in the semiconductor industry will be stunted abruptly if no specific
actions are taken to cope with increasingly high soft-error rates and undetected timing faults, at reasonable costs.

iRoC's products will consist in design tools for automatic fault tolerance insertion. iRoC combines a group of optimized circuits in a global technology named "Transient Fault Tolerant Architecture" (TFTarchitecture™).

"This TFTArchitecture™ is the result of a 5 years technology development by Michael NICOLAIDIS and his group" said Bernard COURTOIS, TIMA Director. "We trust TFTArchitecture™ technology, which is based on a portfolio of international patents, to be the most effective technology to protect ICs against soft-errors" he added.

Reduced power supply levels and the size of device, as well as increased operating speeds are known to dramatically affect the sensitivity of very deep submicron scaling technologies, to noise and in particular to alpha particles and cosmic rays.

In the VLSI era, drastic reliability improvements reserved the costly technology "fault tolerance" in a narrow domain of high-end products. In the near future, increased sensitivity to perturbations will block the very deep submicron scaling. It is making fault tolerance mandatory, even for commodity products.

"Timing defects are a currently key problem in the semiconductor industry and soft errors are a major challenge for next generation of ICs. I strongly believe that ICs – at least 10% for the 180nm and 50% for the 130nm- will have to be fault tolerant. iRoC Technologies is providing the unique low-cost full solution for ICs and IPs, facing these challenges" said Eric DUPONT, President and CEO of iRoC Technologies.

In addition, iRoC Technologies provides professional services to characterize and simulate TFTArchitecture™ performance and cost on commercial deep submicron ICs.

The founders of iRoC Technologies include Dr Michael NICOLAIDIS, leader of the Reliable Integrated Systems group at TIMA, Dr Jean-Michel KARAM, President and CEO of MEMScap, Dr Bernard COURTOIS, Director of TIMA, Joel RODRIGUEZ-ALANIS, CEO of Mentor/Anacad and Eric DUPONT, President and CEO.

VI-1.6 Technical Advisory Board membership

Members of the Laboratory are presently on the Technical Advisory Boards of the following companies:
- STMicroelectronics,
- MEMSCAP,
- VALIOSYS.

In the past, a member of the Laboratory has been on the Technical Advisory Board of SUNRISE.
VI-2 Educational Tasks

Dealing with problems risen by advanced technologies and proposing advanced design and test methodologies, TIMA staff members are, as a matter of course, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into six categories: the EPIQCS programme, courses organization, seminars, support of or participation in foreign university teaching programs, participation in EU educational and technology transfer programs, and finally direction of Ph.D. students employed by French industrial companies (CIFRE program).

VI-2.1 Courses and Tutorials Organization

The following table lists courses and tutorials that have been organized and given by members of the Laboratory, at different institutions request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA staff or externally.

<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Organizer</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT</td>
<td>Paris</td>
<td>02/92</td>
<td>2 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>HP</td>
<td>Grenoble</td>
<td>06/92</td>
<td>1 day</td>
<td>M. Marzouki</td>
<td>Board Testing</td>
</tr>
<tr>
<td>MFQ</td>
<td>Paris</td>
<td>12/92</td>
<td>3 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Grenoble</td>
<td>12/92</td>
<td>5 days</td>
<td>A. Guyot</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Grenoble</td>
<td>06/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Tokyo</td>
<td>10/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Singapore</td>
<td>12/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>04/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/Chipshop</td>
<td>Grenoble</td>
<td>04/94</td>
<td>3 days</td>
<td>K. Torki</td>
<td>VLSI Design on PC platforms</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Irvine-CA</td>
<td>11/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>12/94</td>
<td>2 days</td>
<td>M. Lubaszewski</td>
<td>Mixed-Signal Testing</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/94</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>ST Course</td>
<td>Grenoble</td>
<td>04/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Synthesis</td>
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<tr>
<td>Internat. Course</td>
<td>Grenoble</td>
<td>10/96</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>HW-SW Codeign</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Tokyo</td>
<td>12/97</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>HW-SW Codeign</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Taiwan</td>
<td>12/98</td>
<td>2 days</td>
<td>A. Jerraya</td>
<td>HW-SW Codeign</td>
</tr>
<tr>
<td>NATO School</td>
<td>Italy</td>
<td>8/98</td>
<td>10 days</td>
<td>A. Jerraya - J. Mermet</td>
<td>Codesign</td>
</tr>
<tr>
<td>DATE 99</td>
<td>Germany</td>
<td>3/99</td>
<td>1 day</td>
<td>A. Jerraya</td>
<td>Multilanguage System Design</td>
</tr>
<tr>
<td>DATE 99</td>
<td>Germany</td>
<td>3/99</td>
<td>1 day</td>
<td>A. Jerraya</td>
<td>HW-SW Codeign</td>
</tr>
<tr>
<td>SDL Forum</td>
<td>Canada</td>
<td>6/99</td>
<td>1 day</td>
<td>A. Jerraya</td>
<td>Hardware/Software Codesign from SDL</td>
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<td>ASP-DAC 2000</td>
<td>Japan</td>
<td>1/00</td>
<td>1 day</td>
<td>A. Jerraya</td>
<td>Multilanguage System Design</td>
</tr>
<tr>
<td>-------------------</td>
<td>-------------</td>
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</tr>
<tr>
<td>INTELECT Summer Course</td>
<td>Sweden</td>
<td>8/00</td>
<td>1 day</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
</tr>
<tr>
<td>SSDM 2000 Short Course</td>
<td>Japan</td>
<td>8/00</td>
<td>1 day</td>
<td>K. Torki</td>
<td>RF Analog Circuits and Layout Techniques</td>
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<tr>
<td>ActiD-WG</td>
<td>Grenoble</td>
<td>1/00</td>
<td>2 days</td>
<td>M. Renaudin</td>
<td>Asynchronous Circuit Design Workshop</td>
</tr>
<tr>
<td>MIGAS</td>
<td>Autrans</td>
<td>6/00</td>
<td>6 days</td>
<td>M. Renaudin</td>
<td>International Summer School on Advanced Microelectronics</td>
</tr>
<tr>
<td>Eurotraining</td>
<td>Grenoble</td>
<td>5/01</td>
<td>3 days</td>
<td>K. Torki</td>
<td>System-On-Chip Advanced Course</td>
</tr>
<tr>
<td>TEMPRA</td>
<td>Monastir</td>
<td>6/01</td>
<td>6 days</td>
<td>K. Torki</td>
<td>Deep Sub-Micron Front to back design methodology</td>
</tr>
<tr>
<td>IEEE Circuits &amp; Systems Society EDAA</td>
<td>Aix-les-Bains</td>
<td>7/01</td>
<td>4 days</td>
<td>A. Jerraya</td>
<td>Application-Specific Multi-Processor SoC: Summer School</td>
</tr>
<tr>
<td>(ISIM) Inst. des Sciences de l'Ingénieur</td>
<td>Montpellier</td>
<td>1/02</td>
<td>3 h</td>
<td>M. Renaudin</td>
<td>Asynchronous Circuits and Systems</td>
</tr>
<tr>
<td>ACID-WG</td>
<td>Grenoble</td>
<td>7/02</td>
<td>5 days</td>
<td>M. Renaudin</td>
<td>Summer School on Asynchronous Circuit Design</td>
</tr>
<tr>
<td>EDAA European Design and Automation Association</td>
<td>Château de Pizay, France</td>
<td>7/02</td>
<td>4 days</td>
<td>A. Jerraya</td>
<td>2nd Summer School on Application-Specific Multi-Processor SoC</td>
</tr>
</tbody>
</table>

### VI-2.2 Courses and Seminars

Advanced courses and seminars are a practical way of sensitizing graduate students to state-of-the-art problems and research subjects. The attendance is also often composed by young and senior researchers who want to exchange ideas and views on specific problems of their own field or some related research domains.

In addition to internal seminars, the Laboratory regularly invites people from Grenoble academic and industrial environment to attend the talks given by our visiting researchers. These people have recently had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. A.J. Van de Goor</td>
<td>Delft U. of Technology</td>
<td>07/92</td>
<td>Test for SRAMs and FIFOs</td>
</tr>
<tr>
<td>Prof. A.J. Van de Goor</td>
<td>Delft U. of Technology</td>
<td>07/92</td>
<td>Tests for neighborhood pattern sensitive faults</td>
</tr>
<tr>
<td>Dr. G. Venkatesh</td>
<td>ASIC Technologies, Bangalore</td>
<td>09/92</td>
<td>HLS of Asynchronous Speed Independent Controllers</td>
</tr>
<tr>
<td>Prof. D. Kinniment</td>
<td>U. Newcastle Upon Tyne</td>
<td>11/92</td>
<td>Correct Interactive Transformational Synthesis of DSP Hardware</td>
</tr>
<tr>
<td>Prof. F. J. Kurdahi</td>
<td>U. California, Irvine</td>
<td>03/93</td>
<td>Architectural Synthesis of DSP Systems</td>
</tr>
<tr>
<td>Prof. M. Soma</td>
<td>U. Washington, Seattle</td>
<td>04/93</td>
<td>Mixed-Signal Testing and DFT</td>
</tr>
<tr>
<td>Prof. A. Ivanov</td>
<td>U. British Columbia, Vancouver</td>
<td>06/93</td>
<td>BIST Compaction Schemes based on Multiple Signature Checking</td>
</tr>
<tr>
<td>Prof. J. A. Abraham</td>
<td>U. Texas, Austin</td>
<td>06/93</td>
<td>Testing of Analog Circuits</td>
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<tr>
<td>Name</td>
<td>Institution/University</td>
<td>Date</td>
<td>Research Topic</td>
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<td>-----------------------------</td>
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<tr>
<td>Prof. R. Aas</td>
<td>The Norwegian Inst. of Technology</td>
<td>07/93</td>
<td>Probabilistic Model of Design Quality</td>
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<tr>
<td>Mr. J. O'Leary</td>
<td>Cornell U., Ithaca, NY</td>
<td>11/93</td>
<td>Retargeting a Hardware Compiler Proof</td>
</tr>
<tr>
<td>Dr. Y. A. Zorian</td>
<td>AT&amp;T Bell Labs, NJ</td>
<td>03/94</td>
<td>Multi-Chip Module Testing</td>
</tr>
<tr>
<td>Dr. A. Richardson</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>Defect Oriented Testability Analysis and Analog DFT</td>
</tr>
<tr>
<td>Mr. Th. Olbrich</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>BIST and Diagnostics in Safety Critical Microsystems</td>
</tr>
<tr>
<td>Dr. M. Slamani</td>
<td>Ecole Polytechnique de Montreal, Canada</td>
<td>07/94</td>
<td>BIST, Fault Diagnosis and Testability Analysis in Analog ICs based on Sensitivity Concept</td>
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<tr>
<td>H. Morel &amp; B. Allard</td>
<td>Centre de Génie Electr., Lyon</td>
<td>10/94</td>
<td>Utilisation des graphes de liens et des réseaux de Pétri pour la simulation des systèmes de l'électronique de puissance</td>
</tr>
<tr>
<td>Dr. Rajeev Murgai</td>
<td>FUJITSU Labs of America Inc., San José</td>
<td>03/95</td>
<td>Decomposition of Logic Functions for Minimum Transition Activity</td>
</tr>
<tr>
<td>Prof. N. Yevtushenko &amp; Prof. A. Matrosova</td>
<td>Tomsk State Univ., Russia</td>
<td>04/95</td>
<td>- Testing strategies for communicating FSMs&lt;br&gt;- Random simulation&lt;br&gt;- Design for testability</td>
</tr>
<tr>
<td>Prof. G. de Micheli</td>
<td>Stanford Univ.</td>
<td>05/95</td>
<td>An algebraic approach to system-level modeling and synthesis</td>
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<tr>
<td>Prof. G. de Micheli</td>
<td>Stanford Univ.</td>
<td>05/95</td>
<td>Optimal synthesis of gated clocks for low power finite state machines</td>
</tr>
<tr>
<td>Prof. V. Uskov</td>
<td>Moscow State Tech.U.</td>
<td>06/95</td>
<td>Multipurpose CAD System GRAPH-PA</td>
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<tr>
<td>Dr. A. Orailoglu</td>
<td>San Diego Univ.</td>
<td>07/95</td>
<td>Microarchitectural synthesis of self-testable lcs</td>
</tr>
<tr>
<td>Prof. P. Quinton</td>
<td>IRISA-Rennes</td>
<td>01/96</td>
<td>Conception de circuits réguliers avec le langage ALPHA</td>
</tr>
<tr>
<td>Prof. B. Robic</td>
<td>Jozef Stefan Institute Ljubljuna</td>
<td>01/96</td>
<td>Dataflow graphs: partitioning and embedding</td>
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<tr>
<td>Dr. R. Bergamaschi</td>
<td>IBM T.J. Watson Res. Center, Yorktown Heights</td>
<td>03/96</td>
<td>Observable time windows: verifying the results of high-level synthesis</td>
</tr>
<tr>
<td>Dr. R. Kumar</td>
<td>FZI, Karlsruhe Univ.</td>
<td>04/96</td>
<td>A formal approach to hardware synthesis</td>
</tr>
<tr>
<td>Prof. J. Staunstrup</td>
<td>Techn. Univ. Lyngby</td>
<td>06/96</td>
<td>A formal approach to hardware design</td>
</tr>
<tr>
<td>Prof. A. Ivanov</td>
<td>Vancouver Univ.</td>
<td>06/96</td>
<td>Space compactors for BIST</td>
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<td>Dr. R. Roy</td>
<td>NEC, Princeton</td>
<td>09/96</td>
<td>Low power design: estimation and synthesis techniques</td>
</tr>
<tr>
<td>Dr. S. Piestrak</td>
<td>Wroclaw Univ.</td>
<td>02/97</td>
<td>Arithmétique des résidus: applications et conception de matériels</td>
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<tr>
<td>Dr. G. Bois</td>
<td>Politechn. School of Montreal</td>
<td>07/97</td>
<td>H/S co-design of high performance DSP embedded systems based on reconfigurable architectures</td>
</tr>
<tr>
<td>Prof. P. Arato</td>
<td>Techn. Univ., Budapest</td>
<td>07/97</td>
<td>A high level synthesis conception in research and curriculum at TU Budapest</td>
</tr>
<tr>
<td>Dr. P. Wodey</td>
<td>ISIMA, Clermont-Ferrand</td>
<td>01/98</td>
<td>Méthodologie et outils de codesign à partir de E-LOTOS</td>
</tr>
<tr>
<td>R. Douence</td>
<td>IRISA, Rennes</td>
<td>04/98</td>
<td>Architectures logicielles et wright</td>
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<td>Name</td>
<td>Institution, Country</td>
<td>Year</td>
<td>Description</td>
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<td>J. Madrenas</td>
<td>UPC Barcelona, Spain</td>
<td>07/98</td>
<td>The field-programmable system-on-chip mixed circuit</td>
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<td>L. Semeria</td>
<td>Univ. of Stanford, USA</td>
<td>12/98</td>
<td>Synthesis from C: issues and resolution of pointers</td>
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<tr>
<td>K. Torki</td>
<td>Cadence</td>
<td>98</td>
<td>Deep submicron design</td>
</tr>
<tr>
<td>J. Mermet/A. Jerraya</td>
<td>NATO</td>
<td>98</td>
<td>System level synthesis</td>
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<tr>
<td>S. Kundu and S. Sengupta</td>
<td>Intel, Santa Clara, USA</td>
<td>03/99</td>
<td>Technology development directions for Microprocessor test at Intel</td>
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<tr>
<td>M. Muench</td>
<td>Univ. of Kaiserslautern, Germany</td>
<td>06/99</td>
<td>Synthesis and optimization of algorithmic hardware descriptions</td>
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<tr>
<td>M. Renaudin/P. Vivet</td>
<td>TIMA CENT/DTM/CET</td>
<td>06/99</td>
<td>ASPRO : un microprocesseur asynchrone</td>
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<tr>
<td>P. Franzon</td>
<td>North Carolina State University, USA</td>
<td>07/99</td>
<td>Microsystems and VLSI – Wireless and other applications</td>
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<tr>
<td>A. Jantsch</td>
<td>Royal Inst. of Technol., Sweden</td>
<td>08/99</td>
<td>System-level cosimulation with SDL and Matlab</td>
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<tr>
<td>F. Aneau</td>
<td>CNAM, Paris</td>
<td>12/99</td>
<td>Vers une étude objective de la conscience</td>
</tr>
<tr>
<td>D. Bouldin</td>
<td>Univ. of Tennessee, USA</td>
<td>05/00</td>
<td>Enhancing System-level education with reusable designs</td>
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<tr>
<td>F. Vargas</td>
<td>Univ. of Porto Alegre, Brazil</td>
<td>07/00</td>
<td>Les dernières avancées sur les descriptions VHDL: tolérance aux fautes transitoires et estimation de la fiabilité</td>
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<tr>
<td>K. Chakrabarty</td>
<td>Duke Univ., USA</td>
<td>07/00</td>
<td>Optimization problems in system-on-chip test automation</td>
</tr>
<tr>
<td>Gary M. Swift</td>
<td>California Inst. of Tech., Passadena, CA, USA</td>
<td>09/00</td>
<td>Measurements of the Power: PC750 Upset Susceptibility to Protons and Heavy Ions</td>
</tr>
<tr>
<td>Marek Tudruj</td>
<td>Inst. of Computer Science, Pologne, Varsovie</td>
<td>10/00</td>
<td>Architectures for Time Transparent Control of Look-Ahead Dynamic Reconfiguration of Interprocessor Connections including the Multi-Bus Connection Switches for this purposes.</td>
</tr>
<tr>
<td>Jean-Luc Lambert</td>
<td>Valiosys SA, Caen, France</td>
<td>10/00</td>
<td>LPV: a new technique, based on linear programming, to formally prove or disprove safety properties on software and hardware systems</td>
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<tr>
<td>Saeyang Yang</td>
<td>SEVITS Technology Inc., Pusan, Korea</td>
<td>10/00</td>
<td>Simulation + Emulation: A New Hope in Verification Crisis?</td>
</tr>
<tr>
<td>Steven P. Levitan</td>
<td>Univ. of Pittsburgh</td>
<td>12/00</td>
<td>CAD Tools and Modeling Challenges for Optoelectronic Systems</td>
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<tr>
<td>Sergio Martinez</td>
<td>Tima Laboratory, Grenoble, France</td>
<td>12/00</td>
<td>Silicon Micromachined Cross-Connects in Optical Networks</td>
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<tr>
<td>Traian Muntean</td>
<td>CNRS (TIMA) &amp; Univ. de la Méditerranée</td>
<td>12/00</td>
<td>Global Communicating Systems (A distributed refinement design model)</td>
</tr>
<tr>
<td>Philippe Jorrand</td>
<td>Laboratoire LEIBNIZ, Grenoble</td>
<td>03/01</td>
<td>Informatique quantique: principes et algorithmes</td>
</tr>
<tr>
<td>Skandar Basrour</td>
<td>Univ. Franche-Comté, Besançon</td>
<td>03/01</td>
<td>Conception et réalisation de micro-résonateurs à mode de Lamé</td>
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<tr>
<td>Vojin Oklobdzija</td>
<td>Univ. de Californie, Davis, USA</td>
<td>03/01</td>
<td>Clocked storage elements: master-slave latches and flip-flops for high performance and low power systems</td>
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<tr>
<td>Luciano Lavagno</td>
<td>Univ. of Udine, Italy</td>
<td>04/01</td>
<td>Embedded system design</td>
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<tr>
<td>Name</td>
<td>Institution and Location</td>
<td>Date</td>
<td>Description</td>
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<tr>
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<td>-----------------------------------------------</td>
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<tr>
<td>Warren A. Hunt, Jr.</td>
<td>IBM Austin Res. Lab., Univ. of Texas, USA</td>
<td>06/01</td>
<td>Verification at IBM and the FM9801 Microprocessor Verification</td>
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<tr>
<td>Prof. G. De Micheli</td>
<td>Stanford University, USA</td>
<td>12/01</td>
<td>Network on a chip: a new paradigm for System on Chip design</td>
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<tr>
<td>G. Martin*, F. Husmann*, R. Kress**, F. Castanier***, D. Benjelloun***</td>
<td>*Cadence; **Infineon; ***STMicroelectronics</td>
<td>01/02</td>
<td>VCC: A Tool For HW/SW Codesign and Architectural Space Exploration</td>
</tr>
</tbody>
</table>
Picture VI-2.1 1(c)

Picture VI-2.1 1 (a,b,c) : AMICAL seminars (Tokyo, October 1993 and Singapore, December 1993) and International Course on Hardware-Software codesign (Tokyo, December 1997)
Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions.

<table>
<thead>
<tr>
<th>Institution</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Speaker</th>
<th>Title or content</th>
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<tr>
<td>ENSL-LIP</td>
<td>Lyon</td>
<td>01/92</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line Operators</td>
</tr>
<tr>
<td>ENST</td>
<td>Paris</td>
<td>06/92</td>
<td>3h</td>
<td>A. Guyot</td>
<td>On-line Operators</td>
</tr>
<tr>
<td>EPFL</td>
<td>Lausanne</td>
<td>12/92</td>
<td>6h</td>
<td>M. Nicolaidis</td>
<td>Regular Structure Test and BIST - On-line Testing</td>
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<tr>
<td>ENST-ARCS</td>
<td>Paris</td>
<td>05/93</td>
<td>3h</td>
<td>A. Guyot</td>
<td>On-line Arithmetic Operators</td>
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<tr>
<td>EPFL</td>
<td>Lausanne</td>
<td>09/93</td>
<td>6h</td>
<td>M. Nicolaidis</td>
<td>Regular Structure Test and BIST - On-line Testing</td>
</tr>
<tr>
<td>CERN</td>
<td>Geneva</td>
<td>01/94</td>
<td>1h</td>
<td>M. Lubaszewski</td>
<td>On-line test extension to IEEE 1149.1</td>
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<tr>
<td>AFCET</td>
<td>Paris</td>
<td>02/94</td>
<td>1h</td>
<td>M. Marzouki</td>
<td>Boundary Scan Board and MCMs Test</td>
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<tr>
<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>IC Test - Main Methods</td>
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<tr>
<td>UFMG</td>
<td>Belo Hor.</td>
<td>09/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>BS Test</td>
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<tr>
<td>Telebras/CPqD</td>
<td>Campinas</td>
<td>12/94</td>
<td>2h</td>
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<td>BS Test</td>
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<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>A. Jerraya</td>
<td>Codesign</td>
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<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>A. Jerraya</td>
<td>Behavioral synthesis</td>
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<td>P. Alegre</td>
<td>11/94</td>
<td>2h</td>
<td>A. Jerraya</td>
<td>Behavioral synthesis</td>
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<td>Paris</td>
<td>03/95</td>
<td>1h</td>
<td>A. Jerraya</td>
<td>Codesign</td>
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<tr>
<td>CI Inc</td>
<td>Austin</td>
<td>04/96</td>
<td>1h</td>
<td>D. Borrione</td>
<td>Formal validation of VHDL packages</td>
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<tr>
<td>Fujitsu Lab.</td>
<td>Sta Clara</td>
<td>04/96</td>
<td>3h</td>
<td>D. Borrione</td>
<td>Formal verification in the PREVAIL system</td>
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<tr>
<td>SRI</td>
<td>Stanford</td>
<td>07/96</td>
<td>1h</td>
<td>D. Borrione</td>
<td>Integrating formal methods and CAD</td>
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<tr>
<td>UC Berkeley</td>
<td>Berkeley</td>
<td>08/96</td>
<td>1h</td>
<td>D. Borrione</td>
<td>Automatic diagnosis of simple design errors</td>
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<tr>
<td>Univ. of Chile</td>
<td>Chile</td>
<td>11/98</td>
<td>20h</td>
<td>R. Velazco</td>
<td>Artificial neural networks implementation</td>
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<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>01/99</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
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<tr>
<td>ENST de Bretagne</td>
<td>Grenoble (FT R&amp;D Meylan)</td>
<td>01/00</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
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<tr>
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<td>01/01</td>
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<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
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<tr>
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<td>01/02</td>
<td>5 days</td>
<td>M. Renaudin, R. Leveugle</td>
<td>Conception de Circuits</td>
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</tbody>
</table>

**VI-2.3 Support of Universities Teaching Programs**

The Laboratory has established for many years solid contacts with other research institutions and universities throughout the world. Exchange of students and post-doctoral fellows are very common, and TIMA members are often invited to participate in foreign university teaching programs. The following table lists this kind of activities during the recent academic years.
VI-2.4 Participation in EU Educational Programs

TIMA Laboratory activities have a strong European profile. In addition to numerous research projects listed in other sections of this report, the following table indicates the involvement of TIMA staff members in educational programs launched by the European Union. This involvement take the form of organizing and/or teaching courses.

<table>
<thead>
<tr>
<th>Framework</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Activity</th>
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<td>JTTT Comett II</td>
<td>Greece</td>
<td>02/92</td>
<td>15h.</td>
<td>A. Guyot</td>
<td>VLSI Design Course teaching</td>
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<tr>
<td>EUROCHIP Esprit</td>
<td>France</td>
<td>12/92</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Germany</td>
<td>02/94</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>JTTT Comett II</td>
<td>Italy</td>
<td>02/94</td>
<td>1h</td>
<td>M. Nicolaidis</td>
<td>European School on High Reliability</td>
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<td>Integrated Systems</td>
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<tr>
<td>JTTT Comett II</td>
<td>Greece</td>
<td>12/94</td>
<td>15h.</td>
<td>M. Nicolaidis</td>
<td>Advanced Course on VLSI Testing</td>
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<td>EUROCHIP Esprit</td>
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<td>08/94</td>
<td>6h</td>
<td>A. Jerraya</td>
<td>System Design</td>
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<td>Comet</td>
<td>Austria</td>
<td>04/95</td>
<td>3days</td>
<td>C. Liem</td>
<td>Reconfigurable architecture</td>
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<tr>
<td>EUROCHIP Esprit</td>
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<td>09/95</td>
<td>5days</td>
<td>Jerraya/Kission</td>
<td>System design</td>
</tr>
<tr>
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<td>Denmark</td>
<td>08/95</td>
<td>5days</td>
<td>A. Jerraya</td>
<td>Co-design</td>
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<tr>
<td>Comet</td>
<td>Netherlands</td>
<td>09/95</td>
<td>3days</td>
<td>Kission/Rahm.</td>
<td>AMICAL</td>
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<tr>
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<td>09/97</td>
<td>3h</td>
<td>R. Velazco</td>
<td>On-Line Testing for VLSI</td>
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<tr>
<td>EUROPRATICE COURSE</td>
<td>Germany</td>
<td>09/97</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>Test Technology for Digital and Mixed-Signal</td>
</tr>
</tbody>
</table>

VI-2.5 University/Industry Joint Research Programs

A French national program, called CIFRE, allows French companies to receive French Ph.D. students. The thesis director must belong to a French University or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company.

TIMA staff members have been asked by companies to direct several Ph.D. theses in the CIFRE
framework. The most recent ones are listed in the table below.

<table>
<thead>
<tr>
<th>Company</th>
<th>Student</th>
<th>Director</th>
<th>Dur.</th>
<th>Research Theme</th>
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</thead>
<tbody>
<tr>
<td>IMD</td>
<td>Ch. Vaucher</td>
<td>L. Balme</td>
<td>90-93</td>
<td>PCB Testing</td>
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<tr>
<td>Hewlett Packard</td>
<td>P. Dulieux-Verguin</td>
<td>B. Courtois</td>
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<td>Failure Analysis of ICs by Liquid Crystals</td>
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<td>SGS Thomson</td>
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<td>IMD</td>
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<td>A. Jerraya</td>
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<td>Heterogeneous System Design</td>
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<td>D. Panyasak</td>
<td>M. Renaudin</td>
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<td>J. Quartana</td>
<td>M. Renaudin</td>
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<td>L. Tambour</td>
<td>A. Jerraya</td>
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<td>systèmes intégrés monopuce SOC à dominante traitement du signal et</td>
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<td>comprenant du contrôle</td>
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VII - PUBLISHING


During the past year, TIMA Laboratory promoted and developed a searchable Web site that provides reliable research-based information related to the Laboratory's activities:

- Regarding scientific publishing, electronic versions of the TIMA annual report on a hand, and versions of research groups' activity reports on the other hand, are posted on the web. The "TIMA Laboratory research report collection" and theses elaborated at TIMA Laboratory are available too.
- Dynamic interactive database pages publish fresh information about TIMA Laboratory publications, educational activities, business activities and cooperation activities, such as participation in organization of conferences.
- An Open Database Service, such as the Web-based Job Opportunities service and the Web-based Calendar service (conferences, technical meetings, ...) is proposed to the whole Internet community.
- A valuable selection of links related to TIMA Laboratory research domains is regularly updated.
- TIMA Laboratory web server mirrors the DAC conference web site

Because of the large quantity of information to be managed by the server, a high level of interactivity is required. This is why basic choices have been made like the use of advanced techniques allowing dynamical page content modifications and the development of large databases.

The first results can be summarized as follows:

- TIMA Web offers 11 main directories allowing quick information retrieval,
- 2 free access open databases have been set up about jobs opportunities and a calendar of events (http://tima.imag.fr/job/job.asp and http://tima.imag.fr/events/events.asp).

These 2 databases are of premium interest to the microelectronics community, they are a first step towards the set up of the Laboratory Web server as a EDA Research portal.

Concerning internal communication, a resource centre has been recently created to find additional ways of sharing information and to increase efficiency.

The main development directions for the future will include:
- multimedia publishing (live demos);
- development of the internal resource centre to promote more facilities (calendar scheduling, administrative communication, etc.).
VII-2 Books and magazines

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SIFFLET S.***
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* Politecnico di Torino, Italy


* University of Michigan, USA
** Carnegie Mellon Univ., Pittsburgh, Pa, USA
*** MEMSCAP, Grenoble, France
**** Cronos Integrated Microsystems, Inc., North Carolina, USA
***** National University of Singapore, Singapore

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* CIME/INPG, Grenoble, France
** LPCS/CNRS, Grenoble, France
*** St University (ST Microelectronics), Pouve, France

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* Technical University of Budapest, Hungary
** Philips, The Netherlands
*** MicRed Microelectronics Res & Dev Ltd., Hungary

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* University of Nottingham, UK

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* LPNO/LMFC, Besançon, France
** SENSONOR/ASA, Horten, Norway
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* Ashenden Designs Pty.Ltd, Stirling, SA, Australia
** Forschungszentrum Informatik (FZI), Karlsruhe, Germany

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* NIST, USA
** Philips, The Netherlands

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** INTA, Torrejon de Ardoz, Spain

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* UFRIMA, University of Grenoble I, France

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* Budapest University of Technology and Economics, Budapest, Hungary
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* University Politehnic, Bucharest, Romania
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* Technical University Budapest, Hungary

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*Faculty of Sciences, Monastir, Tunisia

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Medicine and Biology, Lyon, France, 12-14 October 2000

* Czech Technical University in Prague, Prague, Czech Republic
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* Technical University Budapest, Hungary
**MicRed Microelectronics Res & Dev Ltd., Hungary

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* Politecnico di Torino, Italy

RENAUDIN M., RIGAUD JB.
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Asynchronous Interfaces : Tools, Techniques, and Implementations (AIN'T'00) Workshop,

RENAUDIN M., VIVET P., GEOFFREY Ph.
ASPRO : a toy demo

RENAUDIN M.
Asynchronous logic : a promising design alternative
Invited Tutorial at the XV Conference on Design of Circuits and Integrated Systems (DCIS)
Le Corum, Montpellier, 21-24 November 2000

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Asynchronous circuits and systems
Invited talk at International Summer School on Advanced Microelectronics-Grenoble
"MIGAS", Aix-les-Bains, 28 June - 4 July 2000

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San Diego, USA, 27-29 March 2000

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Ground testing of architecture including digital processor signal AD21060
European Conference on Digital Signal Processing (DSP’00), Munich, Allemagne, 11-12 October 2000

* INTA, Torrejon de Ardoz, Spain

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** INTA, Torrejon de Ardoz, Spain

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SICARD G.
Conception d'une rétine analogique/numérique en technologie avancée
Invited talk at Operation Thématique "Rétines", GDR, 10 March 2000

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Symbolic modeling for fault detection and isolation: application to linear analog systems
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6th IEEE International Mixed-Signal Testing Workshop (IMSTW'00), Montpellier, France,
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* Catholic Univ.
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JERRAYA A.A.
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IEEE Instrumentation and Measurement Technology Conference (IMTC’01), Budapest,
Hungary, 21-23 May 2001

* Budapest University of Technology and Economics, Hungary

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Rapid prototyping of an ATM traffic control algorithm
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*Faculty of Sciences, Monastir, Tunisia

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An efficient architecture model for systematic design of application-specific multiprocessor SoC
Design Automation and Testing in Europe (DATE’01), Munich, Germany, 13-16 March 2001
BENEDÉK Zs.*, FARKAS G.**, POHL L.*, POPPE A.*, RENCZ M.*, SZEKELY V.*, TORKI K., MIR S.
Design of a multi-functional intelligent thermal test die
1st Prize in the CMP DATE 2001 Design Contest, Munich, Germany, March 2001
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*Technical University of Budapest, Hungary
**MicRed Microelectronics Res & Dev Ltd., Hungary

BORRIONE D.
On the development of hardware description languages
Invited paper at the Wissenschaftliches Kolloquium of the Braunschweigische Wissenschaftliche Gesellschaft in the honor of Prof. R. Piloty, Braunschweig, Germany, 18 May 2001

CESARIO W., NICOLESCU G., GAUTHIER L., LYONNARD D., JERRAYA A.A
Colfi: a multilevel design representation for application-specific multiprocessor system-on-chip design
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6th Conference on Radiation and its Effects on Components and Systems (RADECUS'01), Grenoble, France, 10-14 September 2001

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* UFRGS, Porto Alegre, Brazil

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*Faculty of Sciences, Monastir, Tunisia

ES SALHİNE M., FESQUET L., QUOC THAI HOI, HUILLERY F., RENAUDIN M.
L'asynchronisme de la puce au système : état de l'art et exemples
Séminaire OBJECTS COMMUNICANTS, Grenoble, France, 17-18 October 2001

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Démonstration de prototypes d'objets communicants en technologie asynchrone
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FERREYRA P. A.*, MARQUES C.A. *, VELAZCO R., CALVO O.**
Injecting single event upsets in a digital signal processor by means of direct memory access requests: a new method for generating bit flips
6th IEEE Radiation and its Effects on Components and Systems, (RADECS’01), Grenoble, France, 10-14 September 2001
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* National University of Cordoba, Argentine
** Islas Baleares University, Palma de Mallorca, Spain

GALILEE B., RENAUDIN M., COULON P-Y., MAMALET F.
Algorithm-programmable architecture asynchronous for the segmentation of image by line of partition of the waters
7th Journées d'Études et d'Échanges "Compression et Représentation des Signaux Audiovisuels", (CORESA'01), Dijon, France, 12-13 November 2001

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Automatic generation and targeting of application specific operating systems and embedded systems software
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Application-specific operating systems generation and targeting for embedded SoCs
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Scalable and flexible cosimulation of SoC designs with heterogeneous multi-processor target architectures
Asia and South Pacific Design Automation Conference 2001 (ASP-DAC’01), Yokohama, Japan, 30 January - 2 February 2001

GOY J., COURTOIS B., KARAM J.M.*, PRESSECOQ F.**
Design and test of an active pixel sensor (APS) CMOS image sensor for space applications
Electronic Imaging 2001 Conference on sensors, cameras, and systems for scientific/industrial applications III (E117), San Jose, California, USA, 21-26 January 2001
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Global modeling and simulation of system-on-Chip embedding MEMS devices

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IEEE European Test Workshop (IETW’01), Stockholm, Sweden, May 2001

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High level modifications of VHDL descriptions for on-line detection or tolerance of errors provoked by SEUs
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Early prediction of SEU consequences through VHDL mutant generation
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A low-cost hardware approach to dependability validations of IPs
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Automatic generation of application-specific architectures for heterogeneous multiprocessor system-on-chip
38th Design Automation Conference (DAC’01), Las Vegas, USA, 18-22 June 2001

MARTINEZ S.O., COURTOIS B.
Study of scalability for micromachined free-space optical cross-connects
Photonics Packaging and Integration III part of SPIE Symposium on Integrated Optics, San Jose, California, USA, 20-26 January 2001

MARTINEZ S.O., COURTOIS B.
Insertion losses in micromachined free-space optical cross-connects due to fiber misalignments
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An optimal memory allocation for application-specific multiprocessor system-on-chip
13th International Symposium on System Synthesis (ISSS’01), Montreal, Canada, 30 September - 3 October 2001
MEFTALI S., GHARSALLI F., ROUSSEAU F., JERRAYA A.A.
Automatic code-transformations and architecture refinement, for application-specific multiprocessor SoCs with shared memory
IFIP International Conference on Very Large Scale Integration - The Global System on Chip Design & CAD Conference (VLSI-SOC'01), Montpellier, France, 3-5 December 2001

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CMOS front-end for capacitive micromachined ultrasonic transducers
1st International Workshop on Microfabricated Ultrasonic Transducers, Roma, Italy, 10-11 May 2001

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The Tenth Workshop on Synthesis And System Integration of Mixed Technologies (SASIMI'01), Nara, Japan, 18-19 October 2001

*UC, Irvine, USA

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Mixed-level cosimulation for fine gradual refinement of communication in SoC design
Design Automation and Testing in Europe (DATE'01), Munich, Germany, 13-16 March 2001

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Effectiveness and limitations of various software techniques for « soft error »
7th IEEE International On-Line Testing Workshop (IOLTW'01), Taormina, Italy, 9-11 July 2001

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*Faculty of Sciences, Monastir, Tunisia

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Design Automation and Test in Europe (DATE'01), Munich, Germany, 13-16 March 2001

* CSEM

Design issues of a multi-functional intelligent thermal test die
17th IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-TERM'01), San Jose, California, USA, March 20-23, 2001

*Technical University of Budapest, Hungary
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REBAUDENGIO M.*, SONZA REORDA M.*, VIOLANTE M.*, CHEYNET P., NICOLESCU B., VELAZCO R.
System safety through automatic high-level code transformations: an experimental evaluation
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Coping with SEUs/SETs in microprocessors by means of low-cost solutions: a comparative study
and experimental results
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On the use of don't cares during symbolic reachability analysis
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6-9 May 2001

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Asynchronous system design
Invited talk at MEDEA+ Conference on Application-oriented SoC Design, From Medea to
Medea+, Eindhoven, The Netherlands, 10-12 October 2001

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Thermal and mechanical evaluation of micromachined planar spiral inductors
Design, Test, Integration, and Packaging of MEMS/MOEMS (DTIP'01), Cannes, France,
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** LEMO/CNRS, France
*** LEOM/CNRS, France

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Modeling and design of asynchronous priority arbiters for on-chip communication systems
IFIP International Conference On Very Large Scale Integration (VLSI-SOC'01), Le Corum,
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Analysis of acoustic capacitive transducers
1st International Workshop on Microfabricated Ultrasonic Transducers, Roma, Italy, 10-11 May
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A robust fault detection scheme for concurrent testing of linear digital systems
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The Tenth Asian Test Symposium (ATS'01), Kyoto, Japan, 19-21 November 2001
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Two VLSI processors for 1D wavelet transform
Tunisian-German Conference Smart Systems and Devices (SSD'01), Hammamet, Tunisia,
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*Faculty of Sciences, Monastir, Tunisia

SVARSTAD K., BEN-FREDJ N., NICOLESCU G., JERRAYA A.A.
A higher level system communication model for object-oriented specification and design of
embedded systems
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A model for describing communication between aggregate objects in the specification and
design of embedded systems
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CMP: The access to advanced low cost manufacturing
2001 International Conference on Microelectronic Systems Education (MSE'01)
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Upset-like fault injection in VHDL descriptions: A method and preliminary results
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a case studied
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IBERCHIP, Montevideo, Uruguay, 23-28 March 2001
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A flight experiment for the evaluation of hardware and software fault tolerance techniques
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A flexible platform for the functional validation of programmable circuits
Proceedings of WRTLT Workshop (RTL ATPG and DFT Workshop) (WRTLT'01), Nara, Japan, 21-23 November 2001

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VHDL fault injection of SEUs in on FPGA based Fuzzy Logic Controller
16th Conference on Design of Circuits and Integrated Systems (DCIS'01), Porto, Portugal, 20-23 November 2001

* UIB, Palma de Mallorca, Spain

YOO S., NICOLESCU G., LYONNARD D., BAGHDADI A., JERRAYA A.A.
A generic wrapper architecture for multi-processor SoC cosimulation and design
International Symposium on Hardware Software Codesign (CODES’01), Copenhagen, Denmark, 25-27 April 2001

YOO S., NICOLESCU G., GAUTHIER L., JERRAYA A.A.
Fast timed cosimulation of HW/SW implementation of embedded multiprocessor SoC communication
IEEE International High Level Design Validation and Test Workshop (HLDVT ‘01), Monterey, USA, 7-9 November 2001

2002

CESARIO W., PAVIOT Y., BAGHDADI A., GAUTHIER L., LYONNARD D., NICOLESCU G., YOO S., JERRAYA A.A., DIAZ-NAVA M.
HW/SW interfaces design for a VDSL modem using automatic refinement of a virtual architecture specification into a multiprocessor SoC: a case study
Design, Automation and Test in Europe (DATE’02), Paris, France, 4-8 March 2002

CESARIO W., BAGHDADI A., GAUTHIER L., LYONNARD D., NICOLESCU G., PAVIOT Y., YOO S., JERRAYA A.A., DIAZ-NAVA M.
Component-based design approach for multicore SoCs
39th Design Automation Conference (DAC’02), New Orleans, USA, 10-14 June 2002

CHARLOT B., COURTOIS B., DELORI H., PAILLOTIN J.-F., TORKI K.
The CMP Service
4th European Workshop on Microelectronics Education (EWME’02), Parador de Baliona, Spain, 23-24 May 2002

GHARSALLI F., MEFTALI S., ROUSSEAU F., JERRAYA A.A.
Embedded memory wrapper generation for multiprocessor SoC
39th Design Automation Conference (DAC’02), New Orleans, USA, 10-14 June 2002
HADJIAT K., LEVEUGLE R.
Évaluation prédictive de la sûreté de fonctionnement d'un circuit intégré
Journées Nationales du Réseau Doctoral en Microélectronique (JNRDM), Grenoble, France,
23-25 April 2002

HADJIAT K., LEVEUGLE R.
Expériences d'injection de fautes multi-niveaux dans des descriptions VHDL
Colloque CAO de circuits et systèmes intégrés, Paris, France, 15-17 May 2002

KRIAA L., YOUSSEF W., NICOLESCU G., MARTINEZ S., LEVITAN S., MARTINEZ J.,
KURZVEG T., JERRAYA A.A., COURTOIS B.
SystemC-based cosimulation for global validation of MOEMS
Design, Test, Integration, and Packaging of MEMS/MOEMS (DTIP’02), Cannes-Mandelieu,
France, 5-8 May 2002

LEVEUGLE R., HADJIAT K.
Multi-Level Fault Injection Experiments Based on VHDL Descriptions: a Case Study
8th IEEE International On-Line Testing Workshop (IOLT’02), Bendor, France, 8-10 July 2002

MIR S., KERKHOF H.*, BLANTON R.D.*, BADER H.*, KLIM H.*
SoCs with MEMS? Can we include MEMS in the SoCs design and test flow
20th IEEE VLSI Test Symposium (VTS’02), Monterey, CA, USA, April/May 2002

NICOLESCU G., MARTINEZ S., KRIAA L., YOUSSEF W., YOO S., CHARLOT B., JERRAYA A.A
Application of multi-domain and multi-cosimulation to an optical MEM switch design
Asia South Pacific Design Automation Conference (ASP-DAC’02) & The Fifteenth
International Conference on VLSI Design, Bangalore, India, 7-11 January 2002

RUFER L., DOMINGUES C., MIR S.
Behavioural modelling and simulation of a MEMS-based ultrasonic pulse-echo system
Design, Test, Integration and Packaging of MEMS/MOEMS, Nice, France, 5-8 May 2002

SZEKELY V.*, RENCI M.*, FARKAS G.*, COURTOIS B.
Measuring interface thermal resistance values by transient testing
Eight International Conference on Thermal and Thermomechanical Phenomena in Electronic
Systems (ITHERM’02), Marina San Diego, California, USA, 29 May – 1 June 2002

* Technical University Budapest, Hungary
** MicRed Microelectronics Res & Dev Ltd., Hungary

RENCZ M.*, SZEKELY V.*, COURTOIS B.
An algorithm for the inclusion of RC compact models of packages into board level thermal
simulation tools
International Conference on Computational Nanoscience and Nanotechnology - Fifth
International Conference on Modeling and Simulation of Microsystems (ICCN-MSM’02),
San Juan, Puerto Rico, USA, 22-25 April 2002

* Technical University Budapest, Hungary

RENCZ M.*, COURTOIS B.
Co-simulation of dynamic compact models of packages with the detailed models of printed
circuit boards
SEMICON West STS’02, San Jose, USA, 17-18 July 2002

* Technical University Budapest, Hungary
YOO S., NICOLESCU G., GAUTHIER L., JERRAYA A.A.
Automatic generation including fast timed simulation models of operating systems in multiprocessor SoC communication design
Design, Automation and Test in Europe (DATE’02), Paris, France, 4-8 March 2002

VII-4 Theses

2000

Zoltan SUGAR
Behavioral synthesis based on scheduling

Fabiano HESSEL
Multilanguage co-design of heterogeneous systems
Thèse de Doctorat INPG – 16 June 2000

Philippe LE MARREC
Multilevel co-simulation in a multilanguage design flow
Thèse de Doctorat INPG – 28 June 2000

Adam MORIWIEC
Improvement of simulation performance of models described in hardware description languages
Thèse de Doctorat INPG – 26 October 2000

Giovanni Maria ANELLI
Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technologies for the LHC experiments
Thèse de Doctorat INPG – 11 December 2000

Lorena ANGHEL
Fault tolerance versus technological limitations of silicon
Thèse de Doctorat INPG – 15 December 2000

2001

Pascal COSTE
Heterogeneous system design
Thèse de Doctorat INPG – 12 January 2001

Sana RIZGUI
Error rate prediction for digital architectures: A method and experimental results
Thèse de Doctorat INPG – 08 January 2001

Benoît CHARLOT
Fault modeling and design-for-test of MEMS
Thèse de Doctorat INPG – 12 March 2001

Gerd RITTER
Formal sequential equivalence checking of digital systems by symbolic simulation
Thèse de Doctorat INPG – 26 March 2001
Ahmad ABDELHAY  
On-line testing of linear digital systems  
Thèse de Doctorat INPG – 20 April 2001

Issam ALZAHER-NOUFAL  
CAD tools for the generation of self-checking arithmetic operators  
Thèse de Doctorat INPG – 23 May 2001

Pascal VIVET  
A quasi-delay insensitive integrated circuit design methodology: application to the study and design of a 16-bit asynchronous RISC microprocessor  
Thèse de Doctorat INPG – 21 June 2001

Philippe GEORGELIN  
Formal verification of synchronous digital designs, based on symbolic simulation  
Thèse de Doctorat INPG – 18 October 2001

Lovic GAUTHIER  
Operating system generation for multitask software targeting on heterogeneous multiprocessor architecture for embedded systems  
Thèse de Doctorat INPG – 5 December 2001

2002

Sébastien ROUX  
Algorithm and architecture for embedded multimedia system  
Thèse de Doctorat INPG – 22 January 2002

Bohuslav PALAN  
Conception de microcapteurs pH-ISFET faible bruit et d’inductances intégrées suspendues à fort facteur de qualité Q  
Thèse de Doctorat INPG – 1st March 2002

Nidal ZAIDAN  
Conception of a secure interface  
Thèse de Doctorat INPG – 23 May 2002

VII – 5 Patents

2000

ABRIAL A., BOUVIER J., SENN P., RENAUDIN M., VIVET P.  
Composant micro-électronique intégrant des moyens de traitement numérique asynchrone et une interface de couplage électromagnétique sans contact  
Patent Number: FR 99/08485, 1 January 2000
VIII - MISCELLANEOUS

VIII.1 What did they do after graduating from the Laboratory (1984-2001)?

Below is the list of researchers which graduated from TIMA Laboratory, from 1984.

The first affiliation corresponds to their affiliation right after the thesis. Eventually, successive affiliations are provided.

From 1984 to 2001, 130 theses have been defended.

It might be noticed that (apart from foreign students who returned in their country) several members of the group have been or are working abroad.

NICOLAIDIS Michael
Conception de circuits intégrés ou testables pour des hypothèses de pannes analytiques.
Thèse de Docteur-Ingénieur, 6 Janvier 1984
CNRS - TIMA Laboratory - Grenoble - France

DERANTONIAN Henri
Génération automatique de parties contrôles de microprocesseurs sous forme de PLA spécialisés
Thèse de Docteur-Ingénieur, 1er Juillet 1984
BULL - Grenoble - France

CHUQUILLANQUI Samuel
Une nouvelle approche pour l'optimisation topologique et l'automatisation du dessin des masques de PLA complexes.
Thèse de Docteur-Ingénieur - 15 Octobre 1984
BULL Systèmes - Les Clayes Sous Bois - France
Next : THOMSON THOM'6 - Paris - France
Next : GEC ALSTHOM - Paris la Défense - France
Next : GEC ALSTHOM Transport - Saint-Ouen - France

LAURENT Jacques
Projet ACIME : Analyse des Circuits Intégrés par Microscopic Electronique.
Thèse de Doctorat, 22 Octobre 1984
CNRS - TIMA Laboratory - Grenoble - France
Next: CNRS - IMAG - Grenoble - France

BOURCIER Emile
Conception et réalisation du simulateur de langage de description de circuits intégrés
IRENE C.
Thèse Ingénieur CNAM - Octobre 1984
STMicroelectronics - Grenoble - France

HMIMID Mohamed
Assemblage et génération automatique des dispositifs périphériques de PLA complexes.
Thèse Docteur de 3ème cycle - 12 Novembre 1984
SIEMENS - Munich - Germany
SAHBATOU Mohamed Djameleddine
Une méthode de conception de microprocesseurs CMOS : application au 8048 (INTEL)
Thèse de Docteur-Ingénieur – 12 Novembre 1984

JANSCH Ingrid
Conception de contrôleurs autotestables pour des hypothèses de pannes analytiques.
Thèse d'État – 1er Avril 1985
Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil

SCHOELL-KOPF Jean-Pierre
SILICIEL : Contributions à l'architecture des circuits intégrés et à la compilation du silicium.
Thèse d'État – 1er Avril 1985
BULL Systèmes - Les Clayes Sous Bois - France
Next : STMicroelectronics - Crolles - France

LANESELLI Jean-Christophe
Un opérateur d'unification pour une machine base de connaissance PROLOG.
Thèse de 3ème cycle – 3 Juin 1985
MERLIN GERIN - Meylan - France

SUWARDI Iping Supriana
Mécanismes prédictifs d'évaluation des caractéristiques géométriques des circuits VLSI.
Thèse de Docteur-Ingénieur - 3 Juin 1985

BERGHER Laurent
Analyse de défaillances de circuits VLSI par microscopie électronique à balayage.
Thèse de Docteur-Ingénieur – 7 Juin 1985
STMicroelectronics - Grenoble - France
Next : BULL Systèmes - Les Clayes Sous Bois - France
Next : STMicroelectronics - Grenoble - France
Next : Thomson TCEC - Grenoble - France

BERTRAND François
Conception descendante appliquée aux microprocesseurs VLSI
Thèse de 3ème cycle – Septembre 1985
BULL Systèmes - Les Clayes Sous Bois - France
Next : LETI - Grenoble - France

PEREZ SEGOVIA Thomas
PAOLA : un système d'optimisation topologique de PLA.
Thèse de 3ème Cycle – 25 Octobre 1985
CNET - Meylan - France

GUIGUET Isabelle
Liaison d'un microscopie électronique à balayage aux outils CAO de description des circuits intégrés.
Thèse Ingénieur CNAM – 28 Novembre 1985
APSIS - Meylan - France

MARTINEZ François
CIRENE : Compilateur du langage IRENE
Thèse Ingénieur CNAM – Novembre 1985
MARINE Souheil
Un langage pour la description, simulation et synthèse automatique du matériau VLSI
Thèse de Docteur Ingénieur – 3 Février 1986
STMicroelectronics - Grenoble - France
Next : ALCATEL-ALsthom - Marcoussis - France

BASCHIERA Daniel
Modélisation de pannes et méthodes de test de circuits intégrés CMOS
Thèse de Doctorat – 6 Mars 1986
TRT - Paris - France
Next : NORSKDATA - Norway
Next : EPFL - Lausanne - Switzerland
Next : HMT - Brügg b/Biel - Switzerland
Next : id3 Semiconductors - Fontanil Cornillon - France

ALIOUAT Mahklouf
Reprise de processus dans un environnement distribué après pannes matérielles transitoires ou permanentes
Thèse de Docteur Ingénieur – 1er Avril 1986
University of Constantine - Algeria

OSSEIRAN Adam
Définition, étude et conception d'un microprocesseur autotestable spécifique : CCBRA
Thèse de Doctorat – 12 Mai 1986
EPFL - Lausanne - Switzerland
Next: University of Geneva, Switzerland

JAMIER Robert
Génération automatique de parties opératives de circuits VLSI de type microprocesseur
Thèse de Docteur Ingénieur – 1er Décembre 1986
STMicroelectronics - Grenoble - France

HOCHET Bertrand
Conception de VLSI : Applications au calcul numérique
Thèse de Doctorat – 12 Janvier 1987
EPFL - Lausanne - Switzerland
Next : University of Adelaide - Australia
Next : University of Yverdon, Switzerland

ROUGEAX François-René
Outils de CAO et conception structurée de systèmes intégrés sur silicium
Thèse de Doctorat – 2 Février 1987
University of Laval - Canada
Next : IBM - Montpellier - France

VARI.NOT Patrice
Compilation de silicium : application à la compilation de parties contrôles
Thèse de Doctorat – 2 Février 1987
Professor at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil
Next : MATRA - Paris - France
DANG Weidong
Parallélisme dans une machine base de connaissances PROLOG
Thèse de Doctorat – 3 Juillet 1987
CRIL - Colombes - France

BEKKARA Noureddine
Optimisation et compromis surface-vitesse dans le compilateur de silicium SYCO
Thèse de Docteur Ingénieur – 19 Octobre 1987
STMicroelectronics - Grenoble - France

SOUAI Mohamed
Etude d'un moniteur d'un système fonctionnellement réparti.
Thèse de Docteur Ingénieur – 1er Novembre 1987

CAISSO Jean-Paul
Contribution à la vérification des circuits intégrés dans un environnement multivalué.
Thèse de Doctorat – 16 Novembre 1987
Mc GILL University - Montreal - Canada
Next : MATRA-MHS – Nantes - France
Next : STMicroelectronics– Rousset – France

BERGER-SABBATEL Gilles
Machines spécialisées et programmation en logique
Thèse d'Etat – 1er Juin 1988
CNRS - TIMA Laboratory - Grenoble - France
Next : CNRS - LGI Laboratory - Grenoble - France

MHAYA Noureddine
Compilateur de parties contrôle de microprocesseurs
Thèse de Doctorat INPG – 24 Juin 1988
IFATEC - Versailles - France
Next: IFATEC - Montigny-Le-Bretonneux - France

DUPRAT Jean
LAIOS : un réseau multiprocesseur orienté intelligence artificielle
Thèse de Doctorat INPG – 22 Juillet 1988
E.N.S.L. - Lyon - France

FERNANDES Antonio Otavio
Test des PLAs optimisés topologiquement
Thèse de Doctorat INPG – 9 Septembre 1988
University of Belo Horizonte - Brazil

MOISAN Frédéric
Optimisation du contraste image en microscopie optique (application à l'inspection microélectronique)
Thèse de Doctorat UJF – 28 Septembre 1988
Direction des Constructions et des Armes Navales (DCAN) - Brest - France
MICOLLET Dominique
Etude de la contrôlabilité de circuits intégrés par faisceaux d'électrons
Thèse de Doctorat INPG – 29 Septembre 1988
University of Dijon – France

ZYSMAN Eytan
Conception de parties contrôles de circuits VLSI - Application au coprocesseur arithmétique FELIN
Thèse de Doctorat INPG – 27 Octobre 1988
EPFL – Lausanne – Switzerland

HORNIK Armand
Contribution à la définition et à la mise en oeuvre de NAUTILE
Thèse de Doctorat INPG – 6 Juin 1989
APSYS – Meylan – France
Next : BULL – Echirolles – France

DARLAY François
Contribution au test des circuits intégrés CMOS : étude du test des pannes stuck-on et stuck-open
Thèse de Doctorat INPG – 20 Novembre 1989
EPFL – Lausanne – Switzerland
Next : Ecole Polytechnique de Montréal – Canada
Next : STMicroelectronics – Grenoble – France
Died in plane crash in July 1996

BONDONO Philippe
Contribution à NAUTILE : un environnement pour la compilation de silicium
Thèse de Doctorat INPG – 8 Décembre 1989
IBM – Corbeil – France

JERRAYA Ahmed Amine
Participation à la compilation de silicium et au compilateur SYCO
Thèse d'Etat – 19 Décembre 1989
CNRS – TIMA Laboratory – Grenoble – France

NORAZ Serge
Application des circuits intégrés autotestables à la sûreté de fonctionnement des systèmes
Thèse de Doctorat INPG – 20 Décembre 1989
MERLIN GERIN – Meylan – France

PIRSON Alain
Conception et simulation d'architectures parallèles et distribuées pour le traitement d'images
Thèse de Doctorat INPG – 4 Mai 1990
CENG Division LETI – Grenoble – France
Next : STMicroelectronics/TCEC – Meylan – France
Next : SYNOPSY – Mountain View – Califonia – USA
Next : C-Cube Microsystems – Milpitas – California – USA
SAVART Denis
Analyse de défaillance de circuits intégrés VLSI par testeur à faisceau d'électrons
Thèse de Doctorat INPG - 27 Juin 1990
IMAGERIE INFORMATIQUE - Grenoble - France

TORKI Kholdoun
L'autotest intégré dans un compilateur de silicium
Thèse de Doctorat INPG - 12 Juillet 1990
CMP - Grenoble - France

BALME Louis
Habilitation à diriger des recherches - 21 Mai 1990
On secondment to SGS, Geneva, from 1.1.1991
Next: TIMA Laboratory

CHAUMONTET Gilles
Etude de faisabilité d'un micro-contrôleur de très haute sécurité
Thèse de Doctorat INPG - 26 Octobre 1990
Centre de Compétence en Conception de Circuits Intégrés (C4I), Archamps - France

MARZOUKI Meryem
Approches à base de connaissances pour le test de circuits VLSI : application à la validation de prototypes dans le cas d'un test sans contact
Thèse de Doctorat INPG - 6 Février 1991
CNRS - TIMA Laboratory - Grenoble - France
Next: CNRS - LIP6 Laboratory - Paris - France

CONARD Didier
Traitement d'images en analyse de défaillances de circuits intégrés par faisceau d'électrons
Thèse de Doctorat INPG - 11 Février 1991
INFI Company (ARM Group) - Paris, France
Next: OCE Graphics - Créteil - France

COURT Thierry
Conception d'une famille de coprocesseurs parallèles intégrés pour le traitement d'images
Thèse de Doctorat INPG - 9 Décembre 1991
I2S - Bordeaux - France

JEMAI Abderrazak
Etude d'un processeur RISC pour un système symbolique parallèle
Thèse de Doctorat INPG - 22 Juin 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble - France
Next: ENSI - Tunis - Tunisia

PARK Inhag
AMICAL : un assistant pour la synthèse et l'exploitation architecturale des circuits de commande
Thèse de Doctorat INPG - 3 Juillet 1992
DAS/ETRI - Daejon, Research Laboratory in Korea
COLLETTE Thierry
Architecture et validation comportementale en VHDL d'un calculateur parallèle dédié à la vision
Thèse de Doctorat INPG - 14 Septembre 1992
CEA/LETI/DEIN - Gif sur Yvette - France

CASTRO ALVES Vladimir
Modélisation de pannes et algorithmes de test pour mémoires RAMs multi-port
Thèse de Doctorat INPG - 10 Octobre 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble - France
Next: Lecturer at Aveiro University - Portugal
Next: Professor at UFRJ - Rio de Janeiro - Brazil

BOURAOUI Rachid
Calcul sur les grands nombres et VLSI : application au PGCD, au PGCD étendu et à la distance euclidienne
Thèse de Doctorat INPG - 15 Janvier 1993
Bell Northern Research (BNR) – Ottawa - Canada
Next: Plaintree Systems Inc. – Stittsville – Ontario - Canada

O'BRIEN Kevin
Compilation de silicium : du circuit au système
Thèse de Doctorat INPG - 31 Mars 1993
LEDA S.A. – Meylan - France

KUSUMAPUTRI-HORNIK Yustina
Opérateurs arithmétiques standards en-ligne à très grande précision
Thèse de Doctorat INPG - 11 Mai 1993

BEN OTHMAN Mohamed Tahar
Evaluation d'une hiérarchie mémoire pour une machine symbolique
Thèse de Doctorat INPG - 8 Septembre 1993
Dean of the Faculty of Science & Engineering, Univ. of Science & Technology - Sana’a - Yemen Republic

VAUCHER Christophe
Le test haute résolution de circuits imprimés nus
Thèse de Doctorat INPG - 25 Novembre 1993
IMD, Grenoble, and TIMA Laboratory - France
Next: IMD Bandol, France
Next: Consultant Engineer, True Test Techniques & Training (T4) – Bandol, France

HAMDI Belgacem
Outils CAO pour la génération automatique de parties opératives auto-controllables
Thèse de Doctorat INPG - 18 Avril 1994
AICHOUCHI Mohamed
Etude des liens entre la synthèse architecturale et la synthèse au niveau transfert de registres
Thèse de Doctorat INPG - 20 Juin 1994
Post-doctoral position at Ecole Polytechnique de Montréal - Canada
CADABRA – Ottawa - Canada
Newbridge Networks Corporation – Kanata – Ottawa - Canada

LUBASZEWSKI Marcelo
Le test unifié de cartes appliqué à la conception de systèmes fiables
Thèse de Doctorat INPG - 20 Juin 1994
Professor at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil

KEBICHI Omar
Techniques et outils de CAO pour la génération automatique de test intégré pour RAMS
Thèse de Doctorat INPG - 15 Juillet 1994
Engineer/researcher at TIMA Laboratory - Grenoble - France
Next: Mentor Graphics – Portland - USA

KOLARIK Vladimir
Techniques avancées de test de circuits analogiques et mixtes analogiques-numériques
Thèse de Doctorat INPG - 31 Octobre 1994
University of Brno - Czech Republic

BEDERR Hakim
Contribution à la conception en vue du test d'opérateurs à structure itérative
Thèse de Doctorat INPG - 23 Novembre 1994
Post-Doctoral position at AT&T Bell Laboratories – Princeton - USA
Next: Texas Instruments - Villeneuve Loubet - France

VERGUIN Pascale
Industrialisation d'une méthode de localisation de défauts sur circuits intégrés par cristaux liquides
Thèse de Doctorat INPG - 20 Décembre 1994
Primary school teacher - France

MONTALVO Luis
Systèmes de numération pour la conception de diviseurs rapides
Thèse de Doctorat INPG, 13 Mars 1995
University of Minnesota – Minneapolis – USA
Next : Post-doctoral position at CNET – Meylan - France

VARGAS Fabian Luis.
Amélioration de la sûreté de fonctionnement des systèmes spatiaux basée sur le contrôle de courant
Thèse de Doctorat INPG, 5 Mai 1995
Associated Researcher at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil
Next: Prof. at Pontificia Universidade Catolica do Rio Grande do Sul - Porto Alegre - Brazil
BOUDJIT Mokhtar
Algorithèmes de Testabilité basés sur la Description à Deux-Niveaux "Groupe-E Concurrente" des Fonctions Logiques
Thèse de Doctorat INPG, 19 Mai 1995

SKAF Ali
Conception de processeurs arithmétiques redondants et en-ligne : algorithmes, architectures et implantations VLSI
Thèse de Doctorat INPG, 11 Septembre 1995
Lecturer at Aveiro University, Portugal
Next : HIAST Institute - Damascus University - Syria

LEMERY François
Modélisation comportementale des circuits analogiques et mixtes
Thèse de Doctorat INPG, 20 Décembre 1995
STMicroelectronics - Crolles - France

BEN ISMAIL Tarek
Synthèse au niveau système et conception de systèmes mixtes logiciels/matériels
Thèse de Doctorat INPG, 9 Janvier 1996
Hewlett Packard - Bristol, UK
AREXSYS - Meylan, France

STEFANI Robert
Application de la Norme ISO 9000 aux entreprises de service fortement dépendantes de leur système d'information
Thèse Professionnelle INPG, Mastère Qualité des Syst. Intégrés complexes, 10 Janvier 1996
AFAQ Auditor, Bagneux (Paris), France

TOUATI Mohamed Hédi
Test et diagnostic de cartes et de MCMs partiellement boundary scan
Thèse de Doctorat INPG - 24 Janvier 1996
Northern Telecom – Ottawa - Canada

KISSION Polen
Exploitation de la hiérarchie et de la réutilisation de blocs existants par la synthèse de haut niveau
Thèse de Doctorat INPG - 25 Janvier 1996
Researcher at TIMA Laboratory - Grenoble
Next: ANACAD – Meylan - France

DING Hong
Synthèse architecturale interactive et flexible
Thèse de Doctorat INPG – 2 Avril 1996
Post-Doctoral position at "Ecole Polytechnique de Montréal" - Canada
Next: Nortel Semiconductors – Ottawa - Canada

KARAM Jean-Michel
Méthodes et outils pour la conception et la fabrication des microsystèmes
Thèse de Doctorat INPG - 20 Mai 1996
Researcher at TIMA Laboratory - Grenoble - France
Next: MEMSCAP - St Ismier (Grenoble) - France
MOUSSA Imed
Applications des circuits numériques en arséniure de gallium dans les systèmes à haut débit de communication et dans les calculateurs performants
Thèse de Doctorat INPG - 10 Juin 1996
Engineer at TIMA Laboratory - Grenoble - France
Next: AREXSYS - Meylan - France

CHANGUEL Adel
Prototypage rapide d'architectures mixtes logiciels/matériels à partir de modèles mixtes C-VHDL
Thèse de Doctorat INPG - 22 Octobre 1996
Associate Professor at ENIM - Monastir - Tunisia

BENALI Aadil
Contribution à l'amélioration de la qualité du test de circuits imprimés nus
Thèse de Doctorat INPG - 3 Décembre 1996
IMD Marcoussis - France

DEHARBE David
Vérification formelle de propriétés temporelles : étude et application au langage VHDL
Thèse de Doctorat UJF - 15 Novembre 1996
Carnegie Mellon University – Pittsburgh - USA

VIJAYARAGHAVAN Vijay
Exploration des liens entre la synthèse de haut niveau (HLS) et la synthèse au niveau transferts de registres (RTL)
Thèse de Doctorat INPG - 29 Novembre 1996
SYNOPSIS - Mountain View - USA

ROMDHANI Mohamed
Ingénierie des systèmes complexes avec la méthode de conception concurrente co-design matériel/logiciel, application aux calculateurs embarqués
Thèse de Doctorat INPG - 9 Décembre 1996
Post Doctoral Position at TIMA - Grenoble - France
Next : Associate Professor at INSAT - Tunis - Tunisia

VACHER André
Calcul câblé d'une transformée de Fourier à très grand nombre d'échantillons, éventuellement multidimensionnelle
Thèse de Doctorat INPG - 8 Janvier 1997
Teacher at Lycée de Meylan - France

PARET Jean-Marc
Etude et mise au point de la méthodologie de conception et de fabrication collective de microsystèmes sur silicium
Thèse de Doctorat INPG - 13 Janvier 1997
ALPLOG – Grenoble - France

RAHMOUNI Maher
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Hewlett Packard – Bristol - UK
WAHBA Ayman
Diagnostic des erreurs de conception dans les circuits digitaux : le cas des erreurs simples
Thèse de Doctorat UIJF - 7 Mai 1997
Associate Professor at Ain Shams University - Cairo - Egypt

OLIVEIRA DUARTE Ricardo
Techniques de conception et outils de CAO pour la génération des parties opératives auto-
contrôlables
Thèse de Doctorat INPG - 30 Juin 1997
Post-doctoral position at University of Belo Horizonte - Brazil ("Univ. Federale de
Minas Gerais")

MOHAMED Firas
Approche à base de logique floue pour le test et le diagnostic des circuits analogiques
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ANACAD - Meylan - France
Next: MEMSCAP - Meylan - France

LIEM Clifford Benjamin
Compileurs multicibles et outils pour les processeurs embarqués dans le cadre
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Thèse de Doctorat INPG - 18 Juillet 1997
Improv Systems Inc. - Santa Clara - California - USA

BERREBI Elisabeth
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Thèse de Doctorat INPG - 11 Décembre 1997
STMicroelectronics - Crolles - France

KODRNJA Marc
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Analyse et simulation du bruit des oscillateurs
Thèse de Doctorat INPG - 12 Décembre 1997
STMicroelectronics - Grenoble - France

DAVEAU Jean-Marc
Spécifications systèmes et synthèse de la communication pour le co-design logiciel/matériel
Thèse de Doctorat INPG - 19 Décembre 1997
Post-doctoral position at IBM New York - USA

NOGUET Dominique
Architectures parallèles pour la morphologie mathématique
Thèse de Doctorat INPG - 26 Janvier 1998
LETI - Grenoble - France

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COISSARD Vincent
  Etude d'un cœur de processeur pour l'arithmétique exacte
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  ALPLOG/ATMEL-ES2 - Le Roussel (Aix-en-Provence) - France
  Next: ALPLOG/STMicroelectronics - Crolles - France

VINCI DOS SANTOS Filipe
  Techniques de conception pour le durcissement des circuits intégrés face aux rayonnements
  MEMSCAP - St Ismier (Grenoble) - France
  Next: CERN - Geneva - Switzerland

VALDERRAMA Carlos Alberto
  Prototype virtuel pour la génération des architectures mixtes logicielles/matérielles
  Universidade Federal do Rio Grande do Norte (UFRN) - Brazil

NEGOI Andy Catalin
  Composant virtuel et ses processeurs de simulation
  Philips Semiconductors AG, Zurich, Switzerland

PEREZ-RIBAS Renato
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  Professor-Researcher at the Computing Institute of Pontificia Universidade Catolica (PUCCamp) - Campinas – Brazil
  Next: Professor at Universidade do Rio Grande do Sul (UFRGS) – Porto Alegre - Brazil

MARCHIORO Gilberto Fernandes
  Découpage transformationnel pour la conception de systèmes mixtes logiciel/matériel
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  Professor at Universidade Federal do Rio Grande do Sul (UFRGS) - Porto Alegre - Brazil

TCHOUUMATCHENKO Vassilly
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  Sofia University - Bulgaria

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  Conception pour la faible consommation en technologies SOI 2D et 3D : application à l'arithmétique
  Thèse de Doctorat INPG – 18 Décembre 1998
  AREXSYS - Meylan – France
  Next: iROC Technologies – Grenoble – France
  Next : SOISIC, Grenoble – France
CHEYNET Philippe
Etude de la robustesse du contrôle intelligent face aux fautes induites par les raciations
Thèse de Doctorat INPG - 5 Mai 1999
Next: Contractual Researcher at TIMA
Next: VERIMAG - Grenoble - France

GUILAUME Philippe
Contribution aux aspects dorsaux de la synthèse de systèmes monopuces - Optimisation de code pour processeurs embarqués - Analyse de la consommation dans un environnement de synthèse comportementale
Thèse de Doctorat INPG - 11 Juin 1999
STMicroelectronics - Crolles - France

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VELASCO-MEDINA Jaime
Techniques de BIST pour test analogique et mixte
Thèse de Doctorat INPG - 1er Juillet 1999
Prof. at Universidad del Valle - Cali - Colombia

CHAAHOUB Faouzi
Étude des méthodes de conception et des outils de CAO pour la synthèse des circuits intégrés analogiques
Thèse de Doctorat INPG - 29 Septembre 1999
Rockwell Semiconductor Systems - Newport Beach - USA

CESARIO Wander
Synthèse architecturale flexible
Thèse de Doctorat INPG - 14 Octobre 1999
Post-doctoral position at TIMA Laboratory - Grenoble - France

BIANCHI Raul Andrés
Techniques de conception des circuits intégrés analogiques pour des applications en haute température, en technologies sur substrat de silicium
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Thèse de Doctorat INPG - 22 Octobre 1999
Prof. at Universidad del Valle - Cali - Colombia

DUSINA Julia
Vérification formelle des résultats de la synthèse de haut niveau
Thèse de Doctorat UJF - 27 Octobre 1999
STMicroelectronics - Bristol - UK
CALIN Teodor
Conception et test de systèmes CMOS fiables et tolérants aux pannes
Thèse de Doctorat INPG – 8 Novembre 1999
STMicroelectronics - Grenoble - France

VEYCHARD Damien
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Thèse de Doctorat INPG – 8 Décembre 1999
CEA - Saclay - France

SUGAR Zoltan
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Thèse de Doctorat INPG – 15 Mai 2000
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HESSEL Fabiano
Conception de systèmes hétérogènes multilangages
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Pontifical Catholic Univ. of Rio Grande do Sul (PUCRS) – Porto Alegre – Brazil

LE MARREC Philippe
Cosimulation multiniveaux dans un flot de conception multilangage
Thèse de Doctorat INPG – 28 Juin 2000
AREXSYS - Meylan - France

MORAWIEC Adam Jan
Amélioration des performances de la simulation des modèles décrits en langages de
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ECSI – Grenoble - France

ANELLI Giovanni
Conception et caractérisation de circuits intégrés résistants aux radiations pour les détecteurs
de particules du LHC en technologies CMOS submicroniques profondes
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CERN – Geneva - Switzerland

ANGHEL Lorena
Les limites technologiques du silicium et tolérance aux fautes
Thèse de Doctorat INPG – 15 Décembre 2000
Researcher Position at TIMA Laboratory – Grenoble - France

COSTE Pascal
Conception des systèmes hétérogènes multilangages
Thèse de Doctorat UJF – 12 Janvier 2001
BOURGET S.A. – Roussillon (Vienne) – France
REZGUI Sana
Prédiction du taux d'erreurs d'architectures digitales : une méthode et des résultats expérimentaux
Thèse de Doctorat INPG – 8 Mars 2001
Researcher Position at TIMA Laboratory – Grenoble - France

CHARLOT Benoit
Modélisation de fautes et conception en vue du test structurel des microsystèmes
Thèse de Doctorat INPG – 12 Mars 2001
Researcher Position at TIMA Laboratory – Grenoble - France

RITTER Gerd
Modélisation de fautes et conception en vue du test structurel des microsystèmes
Thèse de Doctorat UJF – 20 Avril 2001
Research Ingineer Position at Infineon – Allemagne

ABDELHAY Ahmad
Test an ligne des systèmes digitaux linéaires
Thèse de Doctorat INPG – 12 Mars 2001
Faculté de génie électrique et électronique, Université d’Alep – Alep – Syrie

ALZAHER-NOUFAL Imed
Outil de CAO pour la génération d'opérateurs arithmétiques auto-contôlables
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Une méthodologie de conception de circuits intégrés quasi-insensibles aux délais :
application à l'étude et à la réalisation d'un processeur RISC 16-bit asynchrone
Thèse de Doctorat INPG – 21 Juin 2001
STMicroelectronics – Grenoble – France

GEORGELIN Philippe
Vérification formelle de systèmes digitaux synchrones, basée sur la simulation symbolique
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ISIT (Institute of Sytems & Information Technologies) - Fukuoka – Japan

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Conception de microcapteurs pH-ISFET faible bruit et d'inductances intégrées suspendues à fort facteur de qualité Q
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VIII.2 Press articles in 2001

In the following are collected copies of articles that appeared in Newspapers in 2001.
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- Jean-Michel Karam : un chef d'entreprise comblé
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- Le docteur Jean-Michel Karam met le feu aux MEMS
- Memscap sur la bonne route

Hubert CURIE, Minister for Research and Technology, in Grenoble in 1986 [Daniel BLOCH, Chairman of INPG in 1986].
Memscap tient ses promesses

Optical opportunities

TIMA Grenoble – un posibil model al cercetarii stiintifice

"TIMA est un terrain favorable à l’éclosion d’entreprises"

Jean-Michel Karam, le pionnier des MEMS

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SoC-design gar mod netvaerk i chip-form

La conception des circuits intégrés en pleine révolution

The all-optical future starts here

DATE est en passe de jouer l’égalité avec la DAC

MEMSCAP, la Bourse retrouvera-t-elle la fibre optique ?

La poussée irrésistible de la CAO Européenne

Technologie sur circuits complexes

Fabriquer 10 circuits sans se ruiner, c’est possible!

Les grandes ambitions de la Micro Valley grenobloise
Sans-fil et optique pour MEMSCAP

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25 January 2001

Iroc protège les puces des radiations

PAPYRUS N° SPÉCIAL : FEMMES DE SCIENCES
2001

Dominique Borrione : des mathématiques à l'informatique

MUTATIONS N°17
2001

From satellites to portable telephones: the battle against heavy ions to protect our memories
Mission : promouvoir l'Isère !

GRENoble. L'AEPi regroupe des étudiants prometteurs pour les convaincre des atouts du département, en espérant qu'ils s'en souviendront lors de leur parcours professionnel.

"Le développement à l'international d'une entreprise breuvée", tel était le thème choisi par l'AEPi et les universités grenobloises pour réunir les "Ambassadeurs juniors" autour d'une conférence. Alors, l'AEPi, qu'est-ce que c'est ? L'Agence d'Etude et de Promotion de l'Étude est une structure financée par le conseil général qui travaille avec toutes sortes de partenaires : collectivités locales ou territoriales, universités, chambres consulaires.

La mission principale consiste à promouvoir l'Izie et ses différents composants, au point de vue économique et industriel afin de favoriser l'implantation d'entreprises nouvelles dans le département. Elle dispose pour cela de toute une armée de agents et propose entre autres, un système des "Ambassadeurs juniors Grenoblois". Ces jeunes ambassadeurs sont tout simplement des étudiants étrangers de troisième cycle, basés à Grenoble, qui l'AEPi convie à des conférences, sur différents thèmes, les étudiants étant éduqués en fonction de ceux-ci, portant sur l'Izie ou le Grenoble.

Le but est bien évidemment de leur permettre de découvrir de nouvelles facettes de leur ville d'accueil, de leur donner une bonne image, que ces futurs cadres sont transmettre dans leur pays d'origine, une fois rentrés chez eux. C'est ainsi qu'ils deviennent "ambassadeurs", des actes simples et qui devraient être efficaces.

La dernière réunion se déroulait dans les locaux de l'IFNPI, les étudiants scientifiques, présents étaient accueillis par Yves Brunet, président de l'Institut grenoblois, et Jean-Marie Bérand, président de l'AEPI. La conférence fut marquée de façon très agréable par Jean-Michel Aoun, PDG de MEMSCAP, une jeune entreprise basée à Grenoble, qui a réalisé de résultats exceptionnels dans le domaine des micro-technologies en quelques années. Le but de cette conférence était de contester une "success story", M. Aoun expliqua au cours de sa conférence, les méthodes employées, les choix de son succès et ses convictions personnelles en matière de développement. Il revint aussi sur l'importance de la recherche et de sa volonté de parvenir à un fonctionnement avec la fin de sa formation à l'INPG, où il passa son doctorat, dans un laboratoire "Team A", qui lui permet de se faire connaître dans le milieu des MEMS (votre énorme et centre) et de lancer son entreprise une fois ses études terminées.

Avec des horaires atroces, le déjeuner était organisé afin de permettre à tous de se reposer dans une ambiance conviviale et d'écouter des relations, garanties d'une bonne intégration dans notre ville.
MEMSCAP, une réussite grenobloise

Revenons sur le fabuleux destin de la jeune entreprise qui a su cerner le marché et se hisser à la conférence. Le fondateur et actuel P-D.G. de MEMSCAP, Jean-Michel Karam, peut être fier de lui. Depuis trois ans, son société représente un cas d'école de réussite qui est rare aujourd'hui, dans le monde des "start-up". Spécialisée dans les MEMS, systèmes micro électromécaniques, utilisés dans la conception, à la mise au point et la fabrication de produits de communication sans fil et optiques, cette société est aujourd'hui leader mondial des entreprises privées dans son domaine. Les MEMS, composent des composants, des éléments de propriété intellectuelle, ainsi que des circuits logiques et des services associés. Issu d'un laboratoire de l'INPG, Jean-Michel Karam, après s'être fait connaître dans ce petit milieu, a fondé sa société à la sortie de ses études en proposant d'abord du "hardware", les logiciels compris dans ces micro composants que vous trouvez par exemple dans vos téléphones ou vos appareils. Puis, se servant de ce "chapeau de loup" selon sa propre expression, il est dévoilé et s'est entouré des meilleurs spécialistes du sujet pour se lancer dans la production des produits. Aujourd'hui implantée dans 8 pays et présente sur tous les marchés, MEMSCAP est une des seules sociétés de ce domaine à faire des bénéfices. Introduite sur bourse, l'entreprise enregistre rapidement des records de valorisation et reste malgré la crise une "start-up" rentable. Une exception due à la personnalité de son P-D.G. qui est tout près de l'humain, insistant sur les notions de compétence, de motivation et de rendement. Preuve de sa vitalité, l'entreprise dispose déjà de 73 brevets. Un record absolu et le nèf de la guerre pour son dirigeant. Une dynastie et une réussite récompensée l'année dernière par le prestigieux prix "Fost 60" accordé par le cabinet Deloitte et Touche pour la société technologique à la plus forte croissance de la région Rhône-Alpes. Une attaches régionales à la ville de Grenoble, dont est très fier le jeune P-D.G. qui, bien que sans remise que rien n'aurait été possible sans son parcours à l'INPG de Grenoble.
Témoignage

iRoC Technologies : le bénéfice de l'anticipation de la recherche

Directeur technique d'iRoC Technologies, la société qu'il a créée en janvier 2000, Michael Nicolaïdis s'est lancé dans l'aventure alors qu'il était chercheur dans l'équipe TIMA² de l'IMAG³ de Grenoble.

La microélectronique tend désormais vers les technologies nanométriques. Travail sur la conception de circuits intégrés et perçoit les problèmes de proches voies de la combinaison toujours plus poussée de la taille des composants électroniques, Michael Nicolaïdis s'est très vite interposé sur les conséquences de leur utilisation. « En minimisant les composants, on augmente leur sensibilité et leur vulnérabilité. En fin, on favorise l'accroissement d'un nombre accru d'erreurs durant le fonctionnement du système », explique le chercheur. De ce constat, il imagine un besoin en devenir et... un marché potentiel. La protection des composants. L'idée est d'abord vague. Mais les discussions avec les industriels partenaires du TIMA et les chercheurs à l'origine des deux premières start-up issues du laboratoire encouragent le chercheur dans son projet. Le marché n'existe pas encore. Et une question se pose : comment y parvenir ou attendre que les problèmes soient effectifs ? Le risque est pris et iRoC Technologies est créée. L'investissement des chercheurs associés au projet et la confiance d'un industriel permet à la société de démarrer avec un capital de 183 k€ (1,2 MF). La négociation avec la délégation aux entreprises (DAE) pour le transfert des technologies confère les licences exclusives à la société. Le CNRS en devient actionnaire. Michael Nicolaïdis est mis à disposition par le CNRS et perçoit désormais son salaire de la nouvelle entreprise. Actuellement, iRoC Technologies compte trente employés. La société propose une gamme de produits permettant la protection des composants (processeurs et mémoires) contre les perturbations. Précisément, elle développe des solutions qui font l'objet de dépôts de brevets, des outils d'insertion de ces solutions dans les circuits et également des processeurs tolérants les « soft errors ».

Avec un marché comme le réseau internet, l'ordinateur particulier ou les cartes à puce, l'anticipation de Michael Nicolaïdis paraît judicieuse.

Stéphane Billaud

1. TIMA : Technique de l'informatique et de la microélectronique pour l'architecture d'ordinateurs
2. IMAG : Institut d'informatique et de mathématiques appliquées de Grenoble

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Arexsys : l'union fait sa force

Arexsys a réuni ses 16 janvier dernier ses différents partenaires pour présenter le nouveau groupe auquel il appartient et dévoiler ses objectifs pour 2002.

La société éditrice de TIMA en 2001 en réunissant deux compagnies, TSL et Vallisseau, afin de constituer un groupe suffisamment fort pour se mieux positionner sur le marché et participer à la croissance économique et technologique des industries aéronautiques et spatiales. Ce choix est motivé par un regard stratégique sur les enjeux technologiques et économiques de l'avenir. Arexsys s'est précisément chez les études et les analyses des évolutions technologiques et économiques du secteur aéronautique et spatial. Les atouts de l'union sont la cohésion de ses équipes, la diversité de ses compétences, la capacité à proposer des solutions intégrées et complexes.


Chambre d'essence, directeur des ressources humaines de l'Arexsys, a précisé que l'objectif est de poursuivre l'expansion du groupe.

A la ville de Grenoble, bien que bel et bien logée dans un immeuble délabré, l'Arexsys a installé un nouveau siège de direction. Les locaux sont spacieux et modernes, offrant une vue panoramique sur le paysage environnant. Les équipements sont de qualité et répondent aux normes les plus récentes en matière de bureautique.
Lilliputian ambitions?

by Joshua Jaffe
Published: 00:15 PM EST, Dec-11-2001

Meet the American Dream à la française. Jean Michel Karam, the founder, chairman, president and CEO of Memscap S.A., the world’s only publicly traded company focused on micro electro-mechanical systems, or MEMS, technology, has Texas-sized ambitions for his company’s very, very small offerings.

Memscap, nestled in the St. literi suburb of Grenoble, France, develops wireless and optical networking products based on MEMS, which are microscopic systems that combine mechanical, optical, electromagnetic or thermal devices with electronics, usually on silicon substrates similar to those used in the semiconductor industry. The end products are smaller, more efficient devices that can be used where traditional mechanical structures would be too bulky.

Karam claims that his company’s 11 patents furnish Memscap with a key technological edge which, foothills of the French Alps, gives his company a critical manufacturing advantage over the umber of startups and a few high-tech giants chasing the same Lilliputian ambitions. His listed status on the France’s high-tech bourse in Paris, the Nouveau Marché, adds to Memscap’s market prowess, he argues, giving it more market visibility and a stronger cash position.

“We want to dominate the MEMS industry,” Karam says confidently. His plan: fiscal discipline, a sharp focus on a wide range of MEMS-based applications, and some well-timed acquisitions. These moves, he believes, will allow him to keep ahead of an estimated 200 privately held companies, which collectively have raised more than $500 million to expand beyond the traditional use of MEMS technology in semiconductor used for more than a decade.

“I believe consolidation will occur,” he says of his competition. And he plans to lead the effort. Ultimately, he hopes to grow Memscap’s product line to challenge publicly listed companies such as JDS Uniphase Corp. and Motorola Inc., both of which are conducting internal research on MEMS technology.

Is Karam’s vision as far-fetched as Gulliver’s Travels? Well, analysts are certainly upbeat about Memscap’s technology. “There is no question about the technology working,” said Bernard Mathé, a senior analyst at SG Cowies Securities Corp. in Paris, “That is a definitive yes. They are among the top two companies, if not the top MEMS company in the world.”

In spite of this head start, challenges remain. Memscap’s product focus on the telecommunications equipment market means it’s exposed to drastically lower capital expenditures by debt-laden telecommunications carriers. Memscap’s sales are suffering.

Furthermore, the company’s main claim to fame — three successful photonic switches with so-called “low port counts” capable of easing data bottlenecks on an all-optical metro or long-haul network — does not mean Memscap can build a scalable photonic switch with high port counts that can be manufactured affordably and transmit even more data. Indeed, experts question whether Memscap or anyone else can do that.

Yet even if that tech hurdle can be overcome and telecommunications companies start to increase their spending on all-optical networks, it’s still unclear if Karam can ward off the scores of nimble startups and established technology giants that have Memscap firmly in their sights. All of them are trying to deploy MEMS technology in biomedical applications such as pacemakers, electronics applications such as data storage or communications equipment applications such as tunable lasers.

Karam, though, is used to obstacles. After arriving in France from his native Lebanon in 1990, he obtained his Ph.D. in 1996 soon after launching the first MEMS research-and-development lab at Grenoble’s world-renowned TIMA research institute. He left the world of pure research in 1997 and launched Memscap the next year, spinning out the technology into his first startup.

Armed with $13.2 million in venture funding from Paris-based Innovacom, Paris-based SPEF Venture and Lugano, Switzerland-based ETT Group, Memscap was one of the few technology companies of any kind to achieve an initial public offering this year. The company raised $60.1 million ($69.3 million) on France’s Nouveau Marché in March, valuing the 32-year-old’s 27% stake in the company at $118 million.

While he tackled the down market conditions with Memscap’s IPO, Karam hasn’t escaped the sector’s ongoing woes. The company’s low point occurred on September 11 when it hit a nadir of $9.9 per share, furnishing the company with a market capitalization of only $52. The share price has recovered to a current level of $28, but still far below its $48-per-share offering price.

So, why did he rush his company to the public market when the fortunes of his two main customer bases, wireless and optical networking companies, were fading? “The money we raised allows us to cross any desert,” he said. Aside from cash, the IPO furnished the company with heaps of press coverage and the necessary financial transparency to reassure customers about its staying power.
Cont'd

Still, privately held MEMS-based startup companies are receiving significant financing these days. Clix Microsystems Inc., for example, a Richmond, Calif., MEMS-based designer of low optical switching engines, closed a $4 million third round in August led by Chicago-based JG&K Capital.

How important is the credibility gained from an IPO in Europe, where state corporations are less willing to buy gear from a startup than their American counterparts? Karam said it's only marginal, depending on the different levels of entrepreneurialism and downplaying his regular visits to Silicon Valley in the mid-1990s. Instead, he stressed his upbringing in Lebanon, where entrepreneurial business skills are highly valued.

Karam is busy exporting these values to France, he says. He sits on the investment committee of Emerica, a $20 million Grenoble-based early stage venture capital fund dedicated to backing microelectronics startups. He has also invested in four local startups, among them Iris Technologies SA, a Grenoble-based integrated circuit design company, which raised $5 million in first round funding earlier this year.

Karam can afford to spend some of his time contributing to what boosts in Grenoble consider to be the "Silicon Valley of Europe." because, unlike many young high-tech startups, his financial position is assured. "I don't have to waste energy thinking about financing," he said.

Karam doesn't waste much time either. During an interview at the end of an optical networking conference, he captivated in a pause in an interview, questioning a visiting researcher on sales with a handshake and a smile. In his consistently upbeat manner, he hinted at good news in the future.

Initially, funds raised from the IPO were supposed to be directed toward building a $65 million fabrication plant and for acquisitions. However, a few months later, Memscap cut a deal to finance 50% of the cost of the fab through bank lending, which now leaves the company with $64 million in cash for acquisitions. And, unlike its privately held crown jewels PhS-MEMS SA and Tronics Microsystems SA, Memscap has acquired currency in the form of publicly traded stock. "At this stage, since they are the only quoted player with cash on hand, they could certainly contribute to consolidation," said SG Cowen Securities analyst Mahfudhe.

So what are the company's needs? While annual revenue growth has topped 300% since 1998, it will still only amount to an estimated €10.5 million this year. Acquisitions could provide a much needed and immediate boost, Karam, however, downscaled the likelihood of an acquisition in the near future to bulk up any of Memscap's four main business units.

He argues that his company's manufacturing division will be complete when the fab is finished next year, while its MEMS-based software design tool unit is growing organically.

No deals are imminent, either, to bolster the company's two main revenue producing divisions: its microscopic wireless design business, which is targeted at portable device manufacturers seeking to shrink the size of their products, and its optical networking equipment unit, which manufactures switches, variable attenuators, tunable filters and assembly components based on its MEMS-technology.

"Memscap's differentiator is that we are MEMS-based," he said. "If we buy an optical company, we will be considered an optics company." Instead, with the support of Memscap's recently appointed head of USA, Vincent Tempere, Karam is scouting the globe for targets that can bolster the company's MEMS-based consulting services, which touch at four units of the company. Tempere joined Memscap from SG Cowen a few months after he led managed the company's IPO. At the Paris-based firm, he was vice president in the firm's European technology corporate finance group's equity development division.

"They have to focus on where they see revenues," said Gary Kelly, a senior analyst at Robertson Stephens International in London. "With optics weak and wireless telecom dead money for a long time, the consulting division is as good as any."

That division received one of its biggest contracts last month when Paris-based cosmetics provider La Licorne Laboratories SA hired Memscap to design and manufacture a sensor-based unit that analyzes the physical and chemical properties of skin surfaces in order to recommend a specific skin care product.

The company is also pushing into new areas of MEMS-based technology such as biomedical research and is considering acquisitions or organic growth as the means of bulking up, according to Karam. However, he repeatedly warned that any acquisitions would have to bring with them revenues and not bleed the company of its cash.

Acquisitions are nothing new for the MEMS industry. Last year, when communications equipment companies were riding high, chip companies such as Cypress Semiconductor Corp. and communications equipment companies such as JDS Uniphase spent more than $6 billion buying up MEMS startups. The activity was highlighted by Nortel Networks Corp.'s acquisition of Xros Inc. for a shocking $3.25 billion, most of which was subsequently written off.

Karam doesn't expect it to return to those accumulative deal values anytime soon. "I don't believe we will see many acquisitions in the near future," he said. "Companies are more focused on research and reorganizing their businesses."

The prospect of a quick trade sale isn't high on his agenda either. Karam insists he wants to build Memscap into a profitable company within hundreds of millions of euros in revenue a year.

As a sign of its long-term commitment, the company has taken the unusual step of establishing an office in Cairo to capitalize on the availability of well-educated but inexpensive engineers. He added that another motivation for the Egyptian office is that in 10 to 15 years, manufacturing could be shifted there if costs in France become too high.

If Karam does find a way to continue growing, his path from one-man spinout to IPO and beyond could end up transforming the communications equipment industry. Liliputian ambitions? Hardly.
MARC FROUIN

Il révolutionne la création des puces

Le P-DG de TNI-Valiosys associe des hautes technologies pour proposer des solutions inédites aux grands de l'électronique.

Marc Frouin, 42 ans, P-DG de la nouvelle société TNI-Valiosys, est un homme pressé. Même s'il s'en défend. En deux ans, il a créé une entreprise industrielle, basée sur le transfert d'une technologie de l'Université de Caen (un nouveau concept de logiciel pour la création de puces électroniques). Simple, mais en apparence seulement, car le marché visé n'existait pas. Aussi, dans le même temps qu'il mettait en ordre de bataille la société, Marc Frouin a pris son bâton de pèlerin afin de préparer la conversion des grands noms de l'industrie électronique, ses futurs clients potentiels.

"Je suis entrepreneur depuis le début de ma carrière. Je suis même un entrepreneur récurrent, comme disent les Américains", observe cet ingénieur de l'École de Lille, diplômé de l'Instein. Il a débrouillé chez Bank Xerox comme "corporate entrepreneur", à l'intérieur d'une entreprise entre le géant américain et le fabricant de PC français Normeler. Parti aux États-Unis, il y a adapté une société en dépôt de bilan, Visioneer, qui fabrique des périphériques pour Macintosh. Après son introduction au Nasdaq, elle est revenue à Hewlett-Packard. EtMarc Frouin revient en France, en Normandie, où il fonde Nomat, constructeur de disques durs mobiles. Après introduction au second marché, la PME est vendue à Iomega, son grand concurrent américain.

Quand il intervient, fin 1999, dans Valiosys, le projet est porté par le CNRS. "Marc Frouin intervient comme "business angel" afin de financer et structurer la nouvelle société. "Un vrai pari, pour lequel une belle confiance dans la technologie était nécessaire", avoue Marc Frouin. Il lui faut d'abord convaincre les grands noms de l'électronique du bien fondé de l'approche, évaluer les enjeux de marchés, laisser mûrir les réflexions. En un mot, être patient, "en se disant que cela va bien finir par arriver", souffre Marc Frouin.

Fédérer une offre hétéroclite

La phase d'industrialisation démarre, avec la fusion entre le nanocent TN (logiciels de conception et de simulation) et Valiosys. Et Marc Frouin, de "business angel" devient aujourd'hui P-DG à plein temps de la nouvelle entité.

La société compte actuellement 75 personnes, dispersées dans la France entière. Ce qui ne simplifie pas mes journées de travail", le savoir-faire de TNI-Valiosys dessine une carte technologique de la France. L'expertise en puces électroniques provient d'une équipe de conception située à Sophia-Antipolis. Les technologies logicielles de base sont issues de l'Université de Caen. Les langages ont été développés chez TNI et à Plaisir, dans la banlieue parisienne. Enfin, les algorithmes mathématiques sont nés à Grunoble, au sein du laboratoire Tima. Une famille nombreuse, qui ne fait pas peur à ce père de six enfants.

De cet ensemble, "à priori hétéroclite", sont nés les premiers logiciels commercialisés dans les industries des semi-conducteurs et des télécommunications. Mais Marc Frouin veut aller plus loin. "Nous allons unifier cette offre afin de proposer un ensemble cohérent. Car les marchés émergent, avec le risque de voir surgir des technologies concurrentes. L'unification sera effective l'an prochain. Marc Frouin veut aller vite, mais sans précipitation.

"Nous ne pouvons pas promettre aux industriels de l'électronique plus que l'on ne peut tenir.

Jean-Pierre VERNAY
L’ESSENTIEL N°61 - 28 November 2001

Memscap en beauté

Memscap à Bernin vient de signer un accord de "plusieurs millions de dollars" avec le laboratoire pharmaceutique La Licorne à Paris pour le développement et la fabrication d'un capteur d'analyse de la peau qui sera basé sur des composants Mems (combinant capteurs, électronique et logiciels). Cet outil d'expertise clinique très novateur sera proposé en libre-service dans la grande distribution et les pharmacies, afin d'orienter la clientèle vers les produits cosmétiques les mieux adaptés à sa peau. Les premières démonstrations de la skin station sont prévues début 2002.
JEAN-MICHEL KARAM
Un chef d'entreprise cambîé

Elegant jusqu'au bout des ongles, grand sourire de rigueur, costume soigné, chaussures fines... Jean-Michel Etourneu ne joue pas la rétention. Il est complètement dans sa passion : l'entreprise qu'il a créée voici deux ans et demi et qui connaît une croissance fulgurante. Du jamais vu : "Marinecap, le record européen de développement de valeurs." D'origine lyonnaise, docteur de l'Inp (Institut national polytechnique de Grenoble) et ingénieur de l'ESIEE, on a seulement l'impression qu'il a pris racine avant de revoir. "Et pourtant les décimateurs se manifestent pas. À chaque étape importante, les levées de fonds, l'introduction en bourse, la construction de la nouvelle usine, je devais échapper... et c'est l'année qui s'est posant. Mais cela me motive encore plus pour continuer." Mais que fabrique donc Marinecap dans sa nouvelle usine qui vient de sortir de terre à Bernin et dont l'investissement s'élève à environ 80 millions d'euros ? Des "micro": ces micro-ordinateurs électroniques qui sont révolutionner le marché des composants optiques et de la communication sans fil. Où les trouve dans les aéronefs de vol, les téléphones portables, les ordinateurs sans fil... et ils ont appelé à un futur développement. Il parle chiffres, croissance et ne tient pas d'âge pour "la fête qui est la plus grande et la plus performante du monde, avec la plus grande concentration d'experts d'Europe : plus de 120 ingénieurs." Mais les superlatifs sont ici employés à bon escient, car les résultats sont là. Avec un chiffre d'affaires de 6,1 millions d'euros pour le premier trimestre 2001, les analystes financiers prévoient un chiffre de 15 à 18 millions d'euros en 2001 et de 70 à 75 en 2002. Quid alors de la crise qui se profile ? "Avec notre cash de 88 millions de dollars nous pouvons tenir 4 à 5 ans sans qu'il ne se passe rien..." De nouveaux projets ? "Après le déménagement d'une production massive à partir du premier trimestre 2002, nous envisageons une nouvelle usine en Egypte!"
Double fusion pour Arexsys

Le deuxième tour de table de la jeune société Arexsys, essaiée de l'INPG créé en 1998 par François Constant, s'est réalisé à l'occasion d'une fusion avec Valiosys, autre star-up basée à Caen, dans le Calvados. "Cette fusion suggérée par nos investisseurs communs, du fait de la forte attirance entre nos technologies, s'est aussi concrétisée par un complément substantiel de fonds de 3,5 M€", précise François Constant. Les actionnaires historiques d'Arexsys, Innovacom, Sofinnova, Auriga, Sudinnova et Axa investissements, ayant participé à deux ans à sa première levée de fonds de 15 M€, ont ainsi été rejoint par la Société Générale et le Crédit Lyonnais. Les outils logiciels d'aide à la conception de circuits intégrés développés par Arexsys sont en effet tout à fait complémentaires de ceux de Valiosys dédiés à la vérification des systèmes, et s'adressent à la même clientèle d'ingénieurs en systèmes électroniques des grands groupes télécoms et semi-conducteurs.

Cette récente opération vient également d'être complétée par une autre fusion avec la société TNI implantée à Brest, spécialisée elle aussi dans l'aide à la conception de systèmes. Le nouveau groupe ainsi constitué, nommé TNI Valiosys, totalise 80 collaborateurs dirigés par Marc Prouin, ex-patron de Valiosys. François Constant assure aujourd'hui la direction commerciale du groupe qui conserve ses implantations locales, poursuit le développement des mêmes lignes de produits tout en bénéficiant des synergies entre ses équipes. Grâce à son offre très complémentaire, il souhaite conquérir une position de leader dans son domaine.
Memscap sur la bonne route

BERNIN. Les collaborateurs de la première société de “MEMS” cotée au monde suivent avec impatience les travaux de construction de leur usine. L’unité de “Fab” de Memscap, dont la salle blanche sera livrée en décembre, offrira une qualité de process rare...

Une grande première en faveur de Valdois, le FAB de Memscap sort du sol. A deux pas des salles blanches de Soitec, un peu plus de 1000 m² de salles blanches (1). Un chantier impressionnant surveillé de près par Jean-Michel Karan, le PDG d’une société à la fois menée et surprenante réussite, inversement proportionnelle à l’écart de ses micro-systèmes. Un dirigeant qui ne s’immisce, le Dr Karan, des en machins de cette entreprise qui navigue sur plusieurs continents. Large sourire, moustache, aux yeux directs et impassibles. L’audace international de basket — 1,94 m, 82 ans (1) — s’exhale en entreprise en novembre 1987, dans la continuité du laboratoire TIMA (Techniques de Micro-informatique et Microélectronique pour construction de Architectures, CNRS-ING-UFR) au sein duquel il dirigeait le groupe des MEMS.


Memscap est dit “Fab” et “Fab” est dit “MEMS”. Très attendue, l’usine de fabrication de Memscap tient parfaitement son calendrier de construction. Le bâtiment est aujourd’hui en “fin de construction”, le 25 décembre, la salle blanche “s’offre” en qualité de prototyde de classe A, l’installation des équipements débute, avant une phase de production en paire nent. Le début de la production de masse s’effectuera à la mi-2002. La “Fab Memscap” deviendra alors une des usines les plus modernes d’Europe.

Gérée en bonne heure depuis le 1er mars, Memscap, la première société de “MEMS” cotée au monde, séduit avec sa qualité de process rare et son “Fab” de haute technologie.

Olivier PERNIER

(1) Le bâtiment, qui compte plusieurs étages, permettra de manipuler les tranches de silicium (les “wafer”) tout au long du processus de fabrication, dans un environnement de propreté élevée. Notamment via un espace de packaging de classe 10, une performance jusqu’alors inédite. A noter que le résultat net du 1er semestre 2001 de Memscap est positif et inférieur à 1,1 million de dollars (5,5 % du chiffre d’affaires), contre une perte nette de 564 000 euros (47,6 % du chiffre d’affaires) pour la même période de l’an 2000.

Jean-Michel Karan est déplacé de l’ENSAT (École supérieure d’ingénieurs en électronique et informatique) de Nanterre. Memscap a investi 15 millions de francs dans la recherche-développement de l’écologie.
Les grandes étapes
• Création: fin 1997 à Saint-Étienne, par essai sur la base de laboratoire Tima (INPG, CNRS, UFR).
• Mai 1998: première nomination de chercheur.
• Mars 2001: production du premier article.
• Mars 2001: lancement du nouveau marché.
• Automne 2001: livraison de la nouvelle usine.
• Printemps 2002: démarrage prévu de la production en volume.

Memscap tient ses promesses

En pleine déroulée des valeurs technologiques, le producteur de microcomposants (Mems) reste dans la lignée de ses prédécesseurs.

"A la création de la société, on me disait que je ne tiendrai pas quatre mois. Mais lors de l'introduction du nouveau processus, qu'il ne serait impossible de le mettre en œuvre que demain. Nous souhaitons nous avancier, mais nous avons besoin de toutes les promesses", Jean-Michel Kamoun, très à l'aise dans son costume d'industriel high-tech, peut aborder un sourire joyeux face aux casseurs. C'est en effet que l'ancien chercheur d'origine tunisienne de 34 ans a suivi la boîte à outils. Avec 6,5 M€ de chiffre d'affaires sur les six derniers mois de 2001, le producteur de Mems - les micro-structures électroniques appliquées à la révolution du marché des composants optiques et de la communication sans fil - se parle même le livre de faire un peu mieux que promis. Les erreurs d'explication,

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<th>résultat net (M€)</th>
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<td>2001</td>
<td>5,1</td>
<td>0,37</td>
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Production sur la base de 1600 M€ de CA, 170 salariés prévus.

Une fabrication ultra-moderne

Un ancien champ de marais de 14 000 mètres carrés (38 000 mètres carrés avec la réserve foncière) a été choisi pour l'étude des opérations. Le chantier de STMicroelectronics, la grue, et les camions du chantier s'installent pour construire dans les détails la "fabrication" ultra-moderne de 3 000 mètres carrés, et une surface de 6 000 mètres carrés de bâtiments.
Optical opportunities

FRENCH COMPANY MEMSCAP HAS WON THIS YEAR'S EUROPEAN SEMICONDUCTOR/WACKER SILTRONIC AWARD FOR BEST EUROPEAN START-UP THE WINNING FIRM SUPPLIES THE WIRELESS AND OPTICAL COMMUNICATIONS INDUSTRIES WITH SOLUTIONS BASED ON MICRO-ELECTRO-MECHANICAL SYSTEMS (MEMS) OR MICROSYSTEMS. DR MIKE COOKE REPORTS ON THE RECENT DEVELOPMENTS AT THE COMPANY THAT clinched the award.

From being an obscure and largely R&D-oriented offshoot of silicon chip processing with just a few applications (accelerometers for airbags in cars, microphones), Microsystems or MEMS (micro-electro-mechanical-systems) are positioning themselves at the heart of optical communication-component production. The French-based company, MEMSCAP, launched by France's TIMA information and micro-electronics technology laboratory in 1997 - has been key to this development and also reflects the change. The company provides MEMS-based solutions for communications in the shape of components, intellectual property, computer aided design tools and related services.

The recent establishment of MEMSCAP, a wholly-owned subsidiary in Finland, will focus efforts on active optical components for the metropolitan and access layers of the optical network. The new company will have a licensing and development relationship with Finland's Optoelectronics Research Centre (ORC). Among MEMSCAP's aims is to source components optimised for the new low-cost plastic optical fibre (POF) market. Available products include RC-LEDs operating at 650nm and VCSELs operating at 690nm.

ORC has licensed RC-LED (resonant cavity light emitting diode) and VCSEL (vertical cavity surface emitting lasers) technology to MEMSCAP, which intends to ramp up additional internal capacity at a new fab in Béziers, near Grenoble, for high-volume production over the course of the next 18 months. "MEMSCAP's RC-LEDs in particular offer several advantages for short-haul polycarbonate melanin (PPMA) POF transmission," says Mihail Dimitrov, director, active optical components, MEMSCAP Oy. "These benefits include operation at the fibre's attenuation minimum, flexibility in alignment, a 50% coupling efficiency with no supplementary optics... These RC-LEDs have a high efficiency at 0.5% and hold the world record in scope for red wavelength range spontaneous emitters, achieving error-free transmission rates beyond 622Mbps."

Further work in the optical arena is represented by ADG, which made a co-development agreement and production agreement with MEMSCAP last year. ADG introduced an optical switch component based on MEMS at this year's SUPERCOMM 2001 exhibition at Atlanta GA in June. MEMSCAP also develops...
variable optical attenuators (VOAs) and filters for ADC.

RF components
Another MEMSCAP initiative is a partnership with Taiwanese company Walsin Lihwa. The companies have made a ten-year, multimillion-dollar agreement for producing wireless devices. The aim is to offer wireless designers a full concept-to-manufacture chain for low-cost MEMS-based RF components.

Walsin will license MEMSCAP's RF MEMS component designs, manufacturing know-how and MEMS design software, enabling Walsin to offer fabrication of RF components, including inductors, switches and variable capacitors. Walsin will be using MEMSCAP's patented Above-IC technology and membrane core technology.

Platform:
To push its capabilities into the electronic design automation (EDA) mainstream, MEMSCAP's MEMS Xplorer has been integrated with the system-on-chip (SOC) tool flow at Cadence Design Systems.

Within the Cadence design environment, users will be able to move from schematic capture to automated generation of component layout, select from MEMS primitives, view cross sections and simulate etching. The MEMSCAP Technology Manager software allows users to target designs to a number of technology processes and foundries. The aim of this move and others like it by MEMSCAP has been to enable system designers who are not necessarily MEMS experts to use the technology.

Washing start-up
"The success of MEMSCAP is indicative of the European industry," said David Reidale, editor for European Semiconductor, when the European Semiconductor/Wacker Silicones European Startup Award was announced. "These products are representative of new and existing markets in which Europe leads the world."

"As an emerging technology company, MEMSCAP has worked hard to demonstrate that MEMS are a proven and viable technology for the communications markets," said Jean-Michel Kanam, president and CEO, MEMSCAP. "Receiving the European Semiconductor/Wacker Silicones award is a gratifying validation of our work and on behalf of all our staff I would like to thank the publication for its recognition."

In February, MEMSCAP completed a successful initial public offering (IPO) - at a time when such listings were and continue to be generally shunned by investors. MEMSCAP's IPO success was a major factor in the award. Further market recognition came with MEMSCAP being included in the Next 150 Euronext Index by the Euronext European stock exchange organisation. MEMSCAP has been listed on France's Nascent Marché since March 2. The Euronext 100 and Next 150 indices include companies with the strongest market capitalisations listed on the Amsterdam, Brussels and Paris stock exchanges.

The award, now in its second year, was announced in Edinburgh at the JEMI UK Semiconductor 2001 conference and trade exhibition. Last year's winner was Si Automation (see below). Candidates for the award must have been running for less than five years. MEMSCAP was picked from a number of nominees from around Europe.

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TIMA Grenoble - un posibil model al cercetării științifice

Prof. dr. ing.
Ioan C. BACIVAROV

În contextul dezbatelor intense pentru această temă: îndelungata perioadă de tranziție - privind perspectivele cercetării științifice autohtone și modalitățile de organizare și finanțare a cercetării, credem că nu este lipită de interes prezentarea, în perioadele acestei reviste, a uneia dintre unitățile reprezentative ale cercetării științifice din Uniunea Europeană care desfășoară cercetări în domeniul calității și siguranței în funcționare.

Vom inaugura acesta unică personal cu prezentarea unei dintre unitățile de elita ale cercetării științifice din Franța: laboratorul TIMA din Grenoble, la activitățile carului care au avut prăbușul să conducă în ultimul deceniu, inclusiv în echipă unor proiecte educaționale și de cercetare științifică ale Uniunii Europene.
Și icle că Franța este una dintre țările care se află în topul cercetării științifice mondiale, atingând anual peste 2,5% din PIB în acest scop, conform unor statistici recente, o progresare șantajătă printre resursele necesare cercetării științifice franceze provenind din fonduri publice, iar restul din sectoarele private.

Laboratorul anual a avut și situate în pitorescul oraș

Grenoble, capitalea Alpină franceză, important pentru universității, 55,000 de studenți la populația de aproximativ 150,000 de locuitori, și considerat tocmai o ușă în cadrul politicii științifice în dascălul învățăturilor, în special high-tech, din Franța: 17,000 de cercetări al doilea centru ca importanță după Pariu.

Laboratorul TIMA (Tehnici ale Informației și ale Microelectronicii pentru Arhitecturi de Calculatoare) are o dublă subordonare, fiind affiliat ca și organizația națională a cercetării științifice, Centrul Național de la Recherche Scientifique (CNRS), cât și principalul universitar din Grenoble (Institut Național Polytechnique și Universitatea Joseph Fourier). Este o soluție eficientă, des utilizată în țările dezvoltate economic, binecunoscute pentru a valorifica strategiile de inteligentă creativă ale profesorilor și cercetătorilor, cât și ale doctoranților și tinerilor din ciclul de studii oportunitare (DEA), pentru soluționarea unor teme de cercetare științifică de vârstă.

Laboratorul TIMA are o tradiție de peste 25 de ani în cercetarea științifică de înalt nivel, fiind la aceeași structură în aceeași grupă de cercetări, și nume:
- Microsisteme (coordonator: prof. dr. Bernard Courtois)
- Sisteme integrate periferice (coordonator: prof. dr. Marc Renouvin)
- Sisteme integrate conceptuale (coordonator: prof. dr. Marc Renouvin)
- Sisteme integrate radiale (coordonator: dr. Michael Nicolaidis)
- Verificașia și modelarea sistemelor digitale (coordonator: prof. dr. Dominique Borrione)
- Calitățile circuitelor (coordonator: dr. Valerarco)

După cum se remarca, există și grupuri specializate în fabricarea și testarea automatizată, dar problematică creșterii calității și siguranței în funcționare este o componentă exercită din tehnice ale proiectului dezvoltat în TIMA. În cadrul TIMA, funcționază, din 1981 și un Centru Circuite-Multi-Proiect (CMP) care permite universităților, laboratoroarelor de cercetare și companiilor să producă circuitele integrate, microchipurile și microprocesorul. Din 1981, peste 100 de instituții din 60 de țări au beneficiat de serviciile CMP, fiind realizate prototipurile a numeroase circuite microelectronice în 38 de tehnologii diferite. De curând, sistemul de management al contractului CMP a fost certificat conform standardului ISO 9002.

Directorul laboratorului, pr. dr. Bernard Courtois, personalitate științifică de rang mondial, a fost presedintele Asociației pentru Proiectarea Automată la Electronica - EDAA, coordonatorul a numeroase conferințe de specialitate și editorul a unor reviste internaționale de prestigiu, inclusiv în "IEEE Golden Core" și Doctor Honoris Causa al unor universități de renomă, a reușit ca, prin proiectul managerial, să împărtășească laboratorul TIMA de cercetări științifice europene, asupra cărora a avut oportunitatea TIMA să fie în topul cercetării științifice europene, deși după cum am arbitrat și ultimul an al anului, TIMA este în topul celor mai importante cercetări științifice, deși unul dintre primele la creații. Acestea cum ar fi:

- parteneriat cu industria (ca procent din cifra totală de afaceri);
- eficiență cercetării (exprimată prin raportul între numărul de prototipurile și cifra de afaceri - local 5 în Franța);
- numărul de întreprinderi "nove" sau create în ansamblu din ideile de cercetători de cercetători în laboratorul TIMA, care au creat în ultimii ani - local 2 în Franța);

Din aceste întreprinderi de succes create de TIMA, numărul de afaceri "nove" sau create în ansamblu din ideile de cercetători de cercetători în laboratorul TIMA, care au creat în ultimii ani menționăm:
- ASM (microtehnică, creată de B. Courtois și J.M. Karons),
- Arexsys (produse software, creată de A. Jarcia),
- iROC (echipamente de treinări la echipă, creată de M. Nicolaidis).

TIMA este un cel mai important laborator din Franța: 50% din cercetări sunt de origine internațională, provenind din 25 de țări, între care și România, e parte din cercetări internaționale cu o selecție a cărei unicea TIMA ca urmare a participării la proiectul TEMFUS EUROPAULNOM.

Vom menționa că, în această țară, există o problemă de desfășurare a cererilor de "secretele" succeselor laboratorului TIMA, care am avut prin eficacitatea sale cunoscută în întreaga lume. În calitatea de Vering Professor al acestei laboratoare ale TIMA al INP Grenoble, avem un grup de cercetători Calitatea sistemelor integrate complexe (din 1992, unde am cooperat cu prof. dr. Paul Balint) și Microsisteme (din 1999), având deja 10 de cooperare cu prof. dr. Bernard Courtois).

Cont'd
Intrarea din domeniul primelelor probleme tehnice ale cercetării științifice aplicative europene și mondiale, cu sistem de calculatoare și sisteme electronice complexe, a spus nivelul principal în cadrul circulatorii VLSI, iar în ultimii ani, de microsisteme, calitatea și siguranța în funcționare, includind situația sistemelor tolerant la defecte, testarea automată și diagnosticul tehnic. Aceasta a făcut posibilă finanțarea cercetărilor laboratorului, în proporție de 60%, prin intermediul contractelor cu parteneri industrii importante: CNES, CEA, ST Microelectronics, France Telecom, Aérospatiale etc.

Compania managerială - dar mai ales științifică - a făcut de colectiv, iar rândul lor personalitate științifică binecunoscută în domeniile lor de activitate, este suficient de știte să mentionăm în acest sens că dr. Ahmed Jerjaya este coordonatorul unor proiecte de mare succes, ca AMICAL și COSMOS, prof. dr. Louis Balme este coordonatorul importantului program european în domeniul calității sistemelor complexe - EPICS, dr. M. Nicolaodis este președintele comitetului IEEE Computer Society în domeniul testării etc.

Participarea activă prin comunicare sau prin conducerea de secții sau grupuri de lucru) la toate reuniunile științifice naționale și internaționale importante în domeniul diferitelor membri ai TIMA, ca modalitate eficientă de a face cunoștințe cercetării proprii, dar și de stabili contacte benefice pentru colaborarea viitoare ale laboratorului. Proiecte, știri se de fotografia internaționale în domeniile de competență ale laboratorului, cu TIMA, între organizatorii sau co-organizatorii, exercitarea personalității TIMA, a fost deservit de mai de acestea. Conferințele internaționale de profil (cum sunt FOBT, EUROCHIP, FTC, ED&TC, MIST, IOL, Euro-VOHL, THERMINIC, ITI, CAD, DATE), pentru a nu menționa decât pe cele mai importante, au fost organizate - conform cu implicarea largă a TIMA.

Larga aderare a TIMA spre cooperarea științifică și educațională, aceasta fiind preventa necesară soluționării unor teme de anvergură. Este semnificativ faptul că această cooperare are în vedere cătâi teme tradițioare, dar și în teme care se referă la universitățile din țările centrale și est-europaene, în cadrul unor programe europene comune, ca PECS, COPERNICUS, TEMPUS și-a.

Unul dintre secretelor succeselor laboratorului TIMA: atmosfera de „mara familie” pe care situl managerial a reușit să o impună (în imagine, aspectele de la traditieana „sărbătoare anuală” a laboratorului), a înființă o atmosferă de încredere, cooperare și armonie.

Prof. dr. Bernard Courtois, directorul laboratorului TIMA, (în stânga imaginii, alături de prof. dr. Maurice Rousard, președintele INP Grenoble) și Doctor Honoris Causa al mai multor universități, este una dintre personalitățile internaționale ale cadrului în domeniul microelectronicii și testării automate.
"TIMA est un terrain favorable à l'écllosion d'entreprises"

À l'heure où l'essaimage d'entreprises constitue pour un nombre croissant de chercheurs du secteur public une ouverture naturelle, le laboratoire des Techniques de l'Informatique et de la Microélectronique pour l'Architecture d'ordinateurs (TIMA) a donné naissance à quelques start-up de premier plan.

Au départ, il y a la recherche, avec deux gros laboratoires spécialisés, le laboratoire d'électronique du CEA (Leti) et Tima, laboratoire commun CNRS-INPG-UJF, qui ont su tisser des liens très forts avec l'industrie. Le Leti travaille principalement sur la technologie, Tima travaille pour sa part sur la conception des circuits et systèmes électroniques intégrés et miniaturisés. "TIMA est un terrain favorable à l'écllosion d'entreprises", déclare Bernard Courtois, directeur de ce laboratoire d'une centaine de chercheurs, considéré comme l'un des deux premiers en Europe pour la microélectronique de type CAO. Pour preuve, l'expansion rapide des jeunes sociétés grenobloises Memscap, Arexys et IROC Technologies, toutes trois essaimées de TIMA. "J'ai fondé au sein du laboratoire le groupe Microsystèmes qui a vite acquis une grande notoriété", explique Jean-Michel Karam, ingénieur qui révait de créer son entreprise. Son rêve devient réalité en 1997 avec la naissance de Memscap, qui produit des outils de CAD et des IP (Intellectual Properties) de type microsystèmes. Les premiers bons de commande tombent dès 1998, il augmente le capital de 12 millions de francs en 1999, puis de 11 millions de dollars en 2000. Memscap frôle aujourd'hui la centaine de salariés et est la seule société en ce domaine à être cotée en Bourse. "Les recherches qui ont pluque-t-elles. Quant à IROC Technologies, société spécialisée dans le ducissement de circuits intégrés très avancés vis-à-vis des rayonnements cosmiques, elle a finalisé son premier tour d'investissement en mars dernier, levant 5 millions de dollars. "Etre à la pointe de la recherche ne nous a jamais empêché de travailler sur des problèmes concrets", conclut très justement Bernard Courtois.
JEAN-MICHEL KARAM,
LE PIONNIER DES MEMS

Ce jeune homme brun décontracté vaut de l'or. En moins de quatre ans, Jean-Michel Karam, ingénieur franco-libanais de 31 ans, doué d'un sens inné du business, a fait de Memscap un leader mondial en produits de communication utilisant la technologie des Mems (micro-electronical system qui permettent, par exemple, le déclenchement des airbags). En février dernier, en plein cataclysme boursier, il lève 101 millions d'euros lorsque sa start-up est introduite en bourse sur le nouveau marché. Jean-Michel Karam débarque à Grenoble, le pôle européen de la micro-électronique, en 1994, comme ingénieur chercheur au Tima, le laboratoire du CNRS associé à l'INPG*. Pionnier dans le domaine des Mems, il bouscule les habitudes du labo. Mais le jeune entrepreneur rêve de voler de ses propres ailes. En 1997, il crée Memscap. Aujourd'hui, la start-up compte cent vingt employés répartis en France, Allemagne, Etats-Unis et Égypte. Sa propre usine de fabrication est en construction à deux pas de Grenoble et devrait générer cent cinquante emplois. Jean-Michel Karam exulte : "Memscap, solide entreprise, est la société qui a rapporté le plus de valeur en relatif sur une période si courte." Et il ne compte pas s'arrêter en si bon chemin. V. L.

*Institut national polytechnique de Grenoble.
**Date 2001 : le «SOC» au cœur des innovations**

L'édition de mars dernier de Date s'est focalisée sur les aspects amont de la conception de systèmes sur silicium, notamment sur la synthèse de C++ et les techniques avancées de vérification, incluant la preuve formelle et les emulatores de nouvelle génération.

Répétition de la Dac manifestation américaine qui aura lieu dans un mois, l'exposition Date à Munich a mis l'accent, comme prévu, sur la conception des «systèmes sur silicium», des circuits intégrés de plusieurs millions de portes intégrant des cœurs CPU, DSP et autres blocs de propriété intellectuelle. Tandis que les conférences s'attachaient à étudier les architectures multi-CPU du futur (voir à ce sujet l'article d'Ahmed Jarjoura du Tina/ITPG, président de la conférence, Electrónica n°112, p.66), les fournisseurs de CAD ont présenté les outils d'aujourd'hui. Les sociétés positionnées dans le «front-end» de l'architecture système au code RTL se sont montrées dynamiques, surtout dans le domaine de la synthèse de code C/C++ et des techniques de vérification. Le secteur du «back-end» a rassemblé un placement-routage en pleine évolution et des outils d'analyse de la physique du semi-conducteur de plus en plus précis. Ici, l'innovation est due à des start-up comme le français Avectec qui a introduit, à Date, ses outils de vérification.

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**DATE 2001**

**Une progression constante depuis trois ans**

Avec 5 500 visiteurs cette année contre 4 900 visiteurs l'an dernier à Paris et 4 000 visiteurs en 1999 à Munich, l'exposition poursuit sa croissance.

Du 13 au 16 mars à Munich, l'exposition Date (Design automation & test in Europe) fut le rendez-vous des conceptrices de Dac, de FPGA, de systèmes sur silicium, circuits imprimés et systèmes électroniques. Fidèles au rendez-vous, ils se sont déplacés pour rencontrer les 106 exposants et assister aux conférences. Un axe majeur de ces dernières tournoit autour de la révolution de la conception des systèmes monopuces. Très remarquées furent les sessions détaillant les plates-formes de SMTMicroelectronics, de Sony, Nintendo et Sega et celle portant sur les architectures de communication pour systèmes monopuces, animée par le VSLA. Ce dernier, dans les allées, les préoccupations des visiteurs se situeraient aussi au niveau de la conjoncture économique. En effet, si l'ensemble de la CAD électronique a connu une progression annuelle stable de 18% par an, les perspectives sont désormais mises à la baisse avec des chiffres de l'ordre de 10% de croissance. Pendant européen de la Dac américaine qui se tient en juin, Date est également le rendez-vous des ingénieurs de test, et partenaire de l'exposition américaine ITC (International test conference). Le cycle de conférences est sponsorisé par EDA (European design and automation association), l'EDAC (EDA consortium), YMC SISBA et IEEE Computer Society, et l'exposition est organisée par EDA Exhibition. Rendez-vous l'an prochain : du 4 au 8 mars 2002 à Paris.
La logique reconfigurable monte en puissance

Date a montré l'intérêt croissant pour les FPGA des spécialistes de la synthèse de C/C++, une technologie qui transforme les algorithmes DSP écrits en C en fichiers de code RTL synthétisables. L'implantation des algorithmes dans des FPGA reprogrammables est intéressante pour le prototypage, et aussi pour le suivi des évolutions de protocoles et des demandes du marché. Frontier Design a doté son atelier A/RT Designer, un outil de synthèse de concepts C++, d'un module qui optimise l'utilisation des unités logiques et des LUT des FPGA. La société est ainsi entrée directement en concurrence avec Celoxica, start-up britannique spécialisée dans l'implantation d'algorithmes en FPGA (voir article d'Actualité p.14).

La suite de conception DK1 de Celoxica a la particularité de passer directement des algorithmes C (ou plutôt Handel-C, version maison du «C système») vers des FPGA, sans passer par l'intermédiaire d'un code HDL ou d'une liste d'interconnexions. C'est un outil multifonction, dont les fonctions sont implantées en FPGA grâce aux outils de Celoxica, et configurable en table ronde, en téléphone IP ou en lecteur MP3.

Ce terminal multifonction, dont les fonctions sont implémentées en FPGA grâce aux outils de Celoxica, est configurable en table ronde, en téléphone IP ou en lecteur MP3.

le de Chronology et de Cyn-Appl), dont la bibliothèque CynLib est le principal concurrent de Synopsys, serait également favorable à une convergence... Si l'on met à part les inconditionnels de Verilog, attachés par le langage Superlog de Co-Design Automation, l'intérêt pour SystemC grandit, poussant la société Doublous, spécialiste des formations HDL, à introduire un cours sur ce langage (en France, chez Amblot). A Date, notons que Mentor a introduit un outil de «saisie graphique de langage HDL» qui réalise de la fusion de Renoise, un produit maison assez simple, et du puissant outil DesignBook d'Escalade, société récemment absorbée par Mentor. HDL Designer incorpore notamment la technologie IBD (Interface based design), permettant de générer quelques centaines de lignes de code HDL par minute à partir de la feuille de tableur.

Accélérateurs et simulateurs : le retour

Les outils de vérification fonctionnelle étaient particulièrement en vedette à Date. La presse formelle a fait sa réapparition en force chez Verplex, Real Intent, Valiosy ou Avertix (voir Electronique n°133, p.56). Les simulateurs, eux aussi, ont fait peau neuve.

Ces outils désormais bien adaptés à la vérification du code RTL, sont très appréciés, mais pas tant pour leurs fonctions d'accélérateur matériel que pour la vitesse du code logiciel. C'est la raison d'une API ouverte de « conception » (voir Electronique n°106, p.26), à introduit à Date la Virtual Station-15M, qui fait passer la capacité d'une machine à 15 millions de portes Système p.10.

Avec la Virtual Station-15M, Illes démontre que les simulateurs de forte capacité n'ont plus besoin d'atteindre la taille d'une armoire.
Plusieurs start-up françaises étaient présentes à Date (doc Avertec).

> contre 4,5 millions précédemment, et cela grâce à l'utilisation des Virtex V800 de Xilinx. Mais surtout, l'accent est mis sur la productivité du concepteur, grâce à un outil de mise au point dédié de celui d'un simulateur. La société n'est plus le seul Challenger de Quickturn et de Mentor. Il faut désormais compter avec Axis Systems, une start-up avec laquelle Ikos a, d'ailleurs, déjà en des débuts juridiques comme souvent en CAO électronique. Axis utilise une technologie de processeur reprogrammable à base de FPGA, dotée d'une bibliothèque de fonctions préconfigurées correspondant à du code RTL ou des primitives de portes. Le compilateur embarque directement le concept HDL dans les FPGA à l'aide des outils de traitement voulus. Axis décline ses machines en versions accélérateur, simulateur et co-simulateur. À un des axes majeurs de la société est la co-validation matériel-logiciel. D'ailleurs, elle compte Jerry Fiddler, fondateur de WindRiver, et spécialiste des logiciels en tant que consultant. Il est en charge de la direction. Notons aussi que Axis a basé son bureau européen en France, sous la direction de José Gandiarz.

**Implantation physique : trouver le juste flot**

S'étant bien sûr présents à Date, les fournisseurs d'outils d'implantation qui, chacun à leur tour, ont repoussé le flot de conception: Synopsys, Pro/Engineer synthèse et placement interviennent parmi les solution existantes, tandis que Magma ou Mentor offrent des chaînes complètes "RTL-to-GDS II", renommés pour intégrer les optimisations au fur et à mesure du placement-routage. Certaines, comme Silicon Perspective ou Arista (récemment acquise par Monterey), se focalisent sur le "Design planning" ou planification de la structure en blocs de circuit intégré, une tâche qualifiée par Jacques Benoist, président et CEO de Monterey, de "front-end du back-end". D'autres, comme Sequent, se spécialisent dans l'optimisation physique, qui interviennent principalement après le routage. Sequentic a présenté l'outil Physical Studio, fruit de sa récente fusion avec Sapphire Design Automation. Combinaison l'optimisation du placement de cette dernière avec sa technologie de réoptimisation post-routage, ce produit qui intègre les analyses très précises de "grefte" sur le routage traditionnel. Difficile de s'y retrouver en ce moment parmi toutes ces approches; mais, avec un peu de recul, la Dac sera sans doute l'occasion d'y voir plus clair.

CATHERINE GROSS
Memscap produira des puces optiques

Jusqu'à présent centré sur les logiciels de conception, le spécialiste des microsystèmes pour réseaux optiques et téléphonie sans fil construit deux usines de production, en France et en Egypte.

"Il faut investir maintenant si nous voulons être leader sur un marché qui naît actuellement, mais qui devrait représenter près de 1,7 milliard de dollars dans le monde en 2003, grâce au boom des réseaux optiques à haut débit." Pour Jean-Michel Karam, PDG de Memscap, le marché mondial des commutateurs optiques à base de Mens va exploser dans les trois prochaines années, et les tickets d'entrée se vendent en ce moment. Jusqu'à présent, spécialisé dans les logiciels pour la conception de Mens, le start-up grenoblois utilise actuellement une grande partie de la centaine de millions d'euros mobilisés à l'occasion de sa récente introduction sur le marché pour se lancer dans la production (en grandes séries) de composants optiques et l'assemblage de composants dédiés aux télécommunications sans fil.

Pour cela, elle entame la construction de deux usines, en France et en Egypte. Tout d'abord, pour muscler son activité « optique », elle investit près de 50 millions d'euros dans la construction d'un fondateur à Bernin, près de Grenoble (Isère). Ce site, qui regroupera 2 000 mètres carrés de salle blanche d'un niveau d'empoussièrement contrôlé supérieur à la classe 10,1 500 mètres carrés de laboratoire et 4 000 mètres carrés de bureaux, produira des commutateurs « tout optique » en grands volumes.

100 postes supplémentaires

Ces microsystèmes intelligents, dont les premiers exemplaires devraient être commercialisés fin 2001, vont révolutionner la communication optique, selon Jean-Michel Karam. Ils sont nettement plus performants que les modèles électriques actuellement utilisés dans les réseaux de fibres optiques. Ils optimisent fortement les échanges entre les différents composants d'un microsystème, qu'ils soient optiques, électroniques, mécaniques ou électromagnétiques. Ce projet devrait permettre de créer une centaine de postes supplémentaires (ingénieurs, techniciens et agents de production).

En ce qui concerne les activités d'assemblage et de mise en boîtier de composants optiques pour les télécommunications sans fil, Memscap a choisi une stratégie mixte. Les tâches de conception et de fabrication de prototypes seront réalisées à Grenoble, tandis que 15 millions d'euros seront investis dans une usine implantée près du Caire (Egypte), équipée de 2 000 mètres carrés de salles blanches. L'opacité actuelle s'applique au développement, pour la téléphonie mobile, d'un nouveau concept permettant d'intégrer des composants actifs et passifs sur une même puce. Ces technologies seront vendues sous forme de licences à des fabricants de semiconducteurs et à des équipementiers.
Comment des microsystèmes ont fait la fortune d'un chercheur grenoblois

A 31 ans, le Grenoblois Jean-Michel Karam vient de créer la surprise en levant 760 millions de F alors que le nasdaq est au plus bas. À l'origine de ce succès : Memscape, une start-up créée en 97 à Saint-Jeanier et spécialisée dans la conception de Mems, c'est-à-dire de systèmes pour les télécommunications. Même si aujourd'hui Memscape ne réalise que 20 millions de F de chiffre d'affaires avec 100 salariés, cette entreprise est valorisée en Bourse à 2,8 milliards de F. Et, ce n'est qu'un début pour son Pdg, Jean Michel Karam qui affiche sans complexe son ambition : devenir le leader mondial dans son secteur.

A qui servent exactement ces Mems ?
Jean Michel Karam : C'est un système microélectronique de taille d'un grain de sel qui a été inventé à la fin des années 60 et qui s'insère dans des éléments mécaniques, électroniques ou optiques. En fait, ils ont un rôle d'actionneurs. C'est, par exemple, les Mems qui permettent le déclenchement d'un capteur dans une voiture en cas d'accident. Mais on trouve aussi des Mems dans les prothèses, dans les cartes d'encore... Vos compétences pour vous lancer sur ce créneau ?
Le déclic ?
Je viens de faire une expérience dans un laboratoire à Grenoble où j'ai travaillé sur des microsystèmes. C'est là que j'ai découvert le potentiel de ces microsystèmes pour les télécommunications.

C'est quand même bizarre un chercheur qui se lance dans le business ?
Non, je suis d'origine libanaise et quand on est libanaise on est toujours dans la réalité de la vie. Je suis né dans un quartier pauvre de Liban et j'ai toujours été souvent en situation de crise. Et je crois que c'est grâce à ça que j'ai vu cette rue de réussir. Au fond, vous n'êtes pas vraiment un passionné de recherche !
Je crois qu'on a une image un peu stéréotypée du chercheur. On voit les chercheurs comme des gens qui ne cessent de travailler. Mais c'est faux. Un chercheur c'est d'abord quelqu'un qui a envie d'inventer des trucs qui marchent, quelqu'un qui explore pour trouver. Et quelque part, derrière un chercheur, il y a toujours un entrepreneur, c'est-à-dire un homme prêt à relever ses défis pour passer au concours.

C'est l'argent qui vous fait avancer ?
Non, c'est l'envie de mener au bout une aventure, de construire une entreprise.
Votre salaire ?
Je gagne plus d'un million de F par an. C'est assez peu et ça peut sembler que je gagne plus que je suis chercheur au centre de Grenoble. D'ailleurs, je n'ai pas changé de trajectoire de vie.

Même si vous êtes aussi le premier actionnaire de l'entreprise ?
C'est vrai que j'ai 27% de Memscape qui est valorisé aujourd'hui à 2,8 milliards de F. Mais je trouve ça tout à fait normal car j'ai travaillé avec un ingénieur pendant plusieurs années pour en arriver là.

Trois ans c'est rapide !
Vos savez, j'ai tout séché pour cette boîte car j'ai trouvé du parti au lendemain mon poste de chercheur pour une banque en Israël. Si j'avais d'abord tout fait, je n'aurais jamais eu d'appel.

Mais vous avez été récupéré par votre labo !
Je n'y ai pas eu accès car moi je vivais en tant qu'entrepreneur. D'ailleurs, si j'avais eu de l'argent, je n'aurais pas échu à Grenoble.

Combien vous avez investi au départ ?
400 000 F. J'ai calculé qu'avec cette somme, je pouvais tenir 4 mois pour trouver les capitaux nécessaires au démarrage.

Combien vous avez levé ?
La première année, j'ai réussi à lever 12 millions de F auprès d'investisseurs, une filiale de France Télécom et auprès de la Spel, une filiale de la Banque Populaire. En avril 2000, j'ai encore levé 72 millions de F auprès de même investisseurs et du groupe suisse ETH.

Comment vous les avez convaincus ?
Je n'ai pas eu besoin de faire beaucoup d'effort car rapidement ils ont tous compris que cette technique allait révolutionner les télécommunications.

L'intérêt des Mems pour les télécommunications ?
En fait, ce sont les Mems qui réceptionnent les messages. Et comme ils sont microélectroniques, leur place sera primordiale dans le futur pour la transmission de données. C'est-à-dire que le téléphone portable devra être équipé de microsystèmes pour permettre le décodage des informations.
Je crois qu'on a une image un peu stéréotypée du chercheur. On voit les chercheurs comme des types un peu déconnectés de la réalité, des intellectuels, des marginaux... Mais c'est faux. Un chercheur c'est d'abord quelqu'un qui a envie d'inventer des trucs qui marchent, quelqu'un qui cherche pour trouver. Et quelque part, derrière un chercheur, il y a souvent un entrepreneur, c'est-à-dire un homme prêt à relever ses manches pour passer en concret.
L'entreprise

- Memsnap
- Forme juridique : SA
- Création : 1997
- Activités : fabrication et commercialisation de mems
- Capital : 16,1 millions de F
- Actionnaires : 27 % Jean Michel Karam, 35 % Innovocom, Spéf et Efi, 23 % public, 15 % business angels
- Implantation : Saint-Timier (38)
- Effectifs : 100 salariés
- Chiffre d'affaires : 20,3 millions de F
- Site : télécommunication
- Distribution : Agences commerciales en France, en Allemagne et Etats-Unis
- Résultat net : 17 millions de F

Le compact, plus léger, plus fiable et moins cher.

Votre stratégie au départ ?
J'ai mis avant tout sur les hommes en débauchant moi-même les meilleurs ingénieurs et les meilleurschercheurs. Car pour moi, les hommes qui font une entreprise, pas la technique. C'est ce qui nous a permis d'être très vivant et de nous démocratiser nos concurrents.

Comment vous les avez débauchés ?
En leur expliquant mon projet et en leur proposant d'être actionnaires de l'entreprise. Ce qui les a rejeté pas du tout au départ ! Mais cela s'est fait au moyen pour attirer de grands talents.

Mais l'entreprise ne valait rien au départ ?
Jusqu'à présent, c'est ce qui prouve que j'ai choisi des gents compétents qui ont tout de suite compris l'intérêt de ce projet car ils ne sont pas habitués aux risques. Aujourd'hui encore, tous les salariés de l'entreprise sont actionnaires.

Votre style de management ?
Memsnap ne s'est pas seulement Jean-Michel Karam mais c'est avant tout une équipe d'hommes et de femmes qui se bat pour leur entreprise. Moi, je donne les grandes orientations et je déléguerai effectivement.

L'entreprise s'est développée rapidement ?
On a même un développement rapide et spectaculaire depuis le premier trimestre. On a réalisé 3,2 millions de F de chiffre d'affaires, avec la fin de 1999 et l'on a dû 11 millions de F en 2000, on a fini avec 29,3 millions de F. En trois ans, on a perdu à peine 17 millions de F.

Vous produisez-vous même vos Mems ?
Oui, nous préférons rester indépendant car on travaille dans un univers ultra concurrentiel. Mais sans que je puise vous dire qu'il est délivré de plusieurs salles blanches dans le monde où on fabrique les composants. Une fabrication qui est bien entamée et entièrement automatisée.

Pouvez-vous installer à Grenoble ?
Parce que c'est là que l'on fait un travail sur le cahier des charges des technologies. Grenoble, c'est vraiment la Silicon Valley française.

L'importance de la recherche pour vous ?
C'est notre priorité. Si on veut rester à ce niveau il faut être en alerte permanente. Et c'est pour ça en effet, que nous avons créé un département de recherche. C'est-à-dire deux fois notre chiffre d'affaires.

A partir de votre implantation à Grenoble ?
En France, on a plusieurs unités de recherche à Toulouse et à Lorient. Mais nous avons aussi des agences commerciales un peu partout dans le monde : en Allemagne, aux Etats-Unis, en Suisse, au Japon, en Corée du Sud, en Inde, à Singapour.

Vos concurrents ?
C'est de grands groupes comme IDS, Unipulse, Corning.

Et vos principaux clients ?
On travaille pour la NASA, la DCI, la Microsystèmes, Honeywell, Bosch, Xerox, Samsung et Siemens microélectroniques.

Pourquoi vous êtes entré en Bourse quatre ans seulement après votre lancement ?
Parce que en France, on dit un peu plus que deux ans après avoir créé une certaine notoriété.

Au total combien vous avez levé ?
On a levé 160 millions de F, ce qui est exceptionnel car on est tombé en plein crise boursière. C'était la première fois en France que les Bourses n'ont pas investi.

Vos projets aujourd'hui ?
Grâce à l'argent qu'on a levé en Bourse, on va construire une usine de production près de Grenoble à Aix-les-Bains qui va produire plus que le double de ce que nous avons pu produire par celle de nos concurrents.

C'est-à-dire ?
Dans moins de trois ans, nous aurons deux usines de milliards de dollars.

Vous n'êtes pas en train de devenir majeur ?
Nous pas du tout. Le marché des solutions optiques est en train de très lentement exploser. Au début, on a été représenté par 100 millions de F seulement. Mais aujourd'hui, cela représente plus de 10 milliards.

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SÉMINAIRE SUR LA CONCEPTION ET LE TEST DES MICROSYSTÈMES

Après deux éditions réussies à Paris en 1999 et 2000, les organisateurs du symposium international sur la conception, le test, l'intégration et l'encapsulation des microsystèmes (Design, Test, Integration and Packaging of MEMS/MOEMS) ont choisi Cannes pour la 3e édition qui se tiendra du 25 au 26 avril prochain. Une petite exposition est associée à cette manifestation qui accueillera une journée d'études sur le développement de l'industrie des microsystèmes.

DATE 2001 CONFIRME SON AUDIENCE

Munich - La manifestation européenne dédiée à la CAO électronique Date, qui s'est tenue du 13 au 16 mars à Munich, a attiré 5 174 participants (dont 1 151 auditeurs aux conférences), soit un peu plus que l'édition de l'an dernier (4 850 visiteurs, dont 1 020 aux conférences), qui s'était déroulée à Paris. Logiquement, plus de la moitié des conférences de la manifestation Date ont été consacrées aux problèmes posés par la conception de systèmes sur une puce, problèmes qui sont au cœur des recherches en CAC. Il a ainsi été question de la conception conjointe du matériel et du logiciel, du choix d'un langage au niveau système, de timing, d'intégrité du signal, d'intégration du test, etc. Reste que l'étape de la vérification est aujourd'hui considérée par tous comme le principal "goulot d'étranglement" de la conception, avec, selon Date-ware, environ 50 % à 70 % du temps total qui lui est consacré. Les annonces sur ce sujet ont donc été nombreuses au salon, notamment dans le domaine de l'emulation et de la preuve formelle. Les éditeurs logiques améliorent ainsi sans cesse leurs possibilités et performances, tandis que les solutions de preuve formelle se diversifient. Le salon Date a également mis en évidence la poussée de la CAC française dont un secteur presque totalement dominé par des sociétés américaines. 

FORTE POUSSEE DE LA CAC FRANCAISE

Le marché de la CAC électronique est effectivement connu par plusieurs sociétés françaises, mais une petite vague européen. Les semiconducteurs, notamment, sont de plus en plus français, comme le démontrent les conférences sur le développement de la CAC électronique aux conférences de la manifestation Date. En France, lesennent des entreprises électroniques ont développé des logiciels de logiques et des circuits analogiques à très haute densité d'intégration. Les technologies de test et de vérification de circuits analogiques sont de plus en plus utilisées par les sociétés de logique électronique. 

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Le salon aura sans doute souffert indirectement de cette année de la crise qui touche actuellement l'industrie des semiconducteurs. On semble en effet que plusieurs grandes compagnies de ce domaine aient fortement réduit leurs budgets de développement. Cela crée, par contre, des opportunités pour les grands fournisseurs de circuits. de grandes sociétés du domaine, Ray, Eichmann pour Cadence, Art de Geeks pour Synopsys et Walden Rhines pour Mentor Graphics. Les fournisseurs de composants sont en effet obligés d'évoluer vers de nouvelles générations de circuits et donc d'investir dans de nouvelles générations d'outils de DAC. Les plus petits fournisseurs de DAC ne semblent pas inquiets, il se peut que la crise à laquelle nous sommes confrontés ne se traduise pas par un fléau, mais par une opportunité inespérée pour ces sociétés.
Les outils de vérification en première ligne pour réduire le "time-to-market"

L’obsession de tous les concepteurs est de réduire la durée du cycle de conception, dont l’étape de vérification reste la plus consommatrice de temps. D’où de nombreuses annonces dans le domaine de l’émulation et de la preuve formelle.

**Les outils de vérification en première ligne**

Mais l’un des principaux problèmes actuels de l’étape de la vérification, considérée par tous comme le principal goulot d’étranglement de la conception, avec environ 50 à 70 % du temps total de la conception selon Danqueux. De ce fait, le marché potentiel pour les outils de vérification est devenu extrêmement important (environ 1 milliard de dollars) et cela explique qu’une grande partie des annonces faites au cours du salon aient concerne ce sujet.

La vérification regroupe différents types d’outils, les simulateurs bien sûr, mais aussi les émulateurs logiques et le marché voit depuis quelque temps se multiplier les solutions de protocole en perÇue. Le concept de preuve formelle est connu depuis longtemps, et les premiers outils ont fait leur apparition sur le marché il y a plus d’une dizaine d’années (le François Bull notamment avait été à l’origine d’un de ces outils, puis ensuite chez Compass, racheté depuis par Avanti). Jusque-là, toutefois, leur diffusion avait été freinée en raison de la difficulté de leur mise en œuvre et de leurs possibilités limitées en termes de taille du circuit. Quelques sociétés ont été créées dans le domaine dont d’ailleurs disparu, telles Verigy ou Abstract Hardware. Ce concept regroupe maintenant deux grands types d’outils : les testeurs d’équivalence (équiva-

Le nombre d’experts était nettement plus élevé que l’an dernier.

Cependant en France, a présenté au salon les plus récentes versions de ses émulateurs Xtreme. Basés sur une technologie reconfigurable de vérification matérielle et logicielle unique en son genre, ces émulateurs font appel à une plate-forme à architecture parallèle. Cette technologie consiste à implanter directement des représentations prédéfinies au niveau RTL ou porte dans des FPGA, sans passer par une opération de synthèse. Les produits d’AxiS entrent en concurrence avec ceux d’une autre jeune société américaine, nommée Tharos, non présente à Date. Attention à ne pas confondre AxiS Systems avec Axis Design Automation, une société californienne fondée en 1997 (C’est en fait une émanation de l’université d’Aix-la-Chapelle) qui développe des outils de modélisation et de simulation supportant un grand nombre de coeurs de processeurs (notamment les familles ARM7 et ARM9).

[*] Voir lexique page 38
SoC-design

går mod netværk i chip-form

Baseret på virtuelle komponenter præsenterer TIMA-
laboratoriet i Grenoble en lovende metode til automatisk
design af komplekse kommunikationsnetværk mellem
systembus og komponenter i system-on-chip design med
flere processor.

Af Dr. Sangjoo Yoo og
Dr. Ahmed Jerraya,
TIMA Laboratory,
Grenoble, Frankrig

I embedsde systemer til
mange forskellige applikati-
oner, såsom 3G trådløse sys-
temmer, netværksprocesso-
rer, processor til computer-
sril, multimedia systemer og
lognende, kræves stadig
større kompleksitet og højere
performance. For at indfør-
ne sådanne applikations-
besvarende krav opbygges
embedede systemer af heter-
ogene komponenter (for
eksempel CPU'er, DSP'er, IP'er, custom ASICS, memo-
rymoduler og linærede), som
udforer applikationsbesvare-
nde opgaver (eksempelvis
tæledegangning med DSP),
og støttede kommunika-
tionsnetværk (for eksempel
netværk til masterprocessoren
samt på optimering af kommunikationen på den
delt bus. I Naco-design derved
bliver implementeringen af
systemkommunikationen
meget mere kompliseret, fordi
hvor digregenerer processorer
er involveret i kommunikationen,
ligesom der anvendes
komplekse kommunikations-
protokoller og netværk.

I et konventionelt design
florerer systemdesignet
mad globale partitionering
(fordeling) af systemet. Det
kan være baseret på en forel
eller uformel generativ
opførsel. Den behavoristiske del
af systemdesignen omfatter
procesorer og hardwareen
(ASICS, IP'er, periferifunctioner).

Komponentdesignen bliver
implementeret med en
target arhitektur, der består
af software (processorer) samt
chip kommunikation (typisk
modulateret med en
target arhitektur, der består
af software (processorer) samt
chip kommunikation (typisk
delt bus på chippen). Alle
enheder sættes sammen
i integrations trinnet.

Cont’d
vendes til at afpasse to forskellige komponentprotokoller og kommunikationsenhedene (for eksempel on-chip bus) med hinanden. For eksempel, for at designe en kommunikationsarkitektur til en delte bus med flere komponenter (CPU'er, DSP'er, IP'er, memorymoduler), skal arkitekturdesigneren designe interfaces for at kunne forbinde komponenterne med den delte bus, det vil kommunikationsdel i software og hardware muliggøres ved brug af API'er (Application Programming Interface), der giver et klart interface mellem kommunikation og behvioristik. Et eksempel herpå er API'erne VCI (Virtual Component Interface) og FI (Functional Interface) fra

En typisk NSoC arkitektur baseret på wrappere

Raffinering af kommunikationen i NSoC design

sige afpasse protokollen for hver komponent med protokollen på den delte bus. I et designflow for NaoC-design, hvor arkitekturdesigneren kan designe systemets VSIA (Virtual Socket Interface Alliance) [VSIA].

Busprotokol vs. komponentprotokol
Inden for den interface-base-
rede designmetode er der to retninger; brugen af standard busprotokol [IBM] og brugen af standard komponentprotokol [VISA] [Sonic]. Til standard busprotokol metoden har IBM for eksempel lanceret en busarchitektur kaldet CoreConnect. For at forbinde heterogene komponenter til busarkitekturen er der designet en wrapper til afpasning af protokollen for hver komponent med protokollen i CoreConnect. I modsætning her til har VISA lanceret VCI og F1 som standard komponentprotokoller. Her kan designeren selv vælge protokollen for on-chip bussen og derpå designe wrapperne til komponenterne.

Der er også lanceret flere kommercielle designværktøjer, som gør det muligt at benytte et interface-baseret designkoncept. For eksempel kan nævnes N2C værktøjet fra CoWare [N2C], VCC (Virtual Component Codesign) fra Cadence [VCC], og Sonics' SiliconBackplane mNetwork [Sonic]. Selvom disse værktøjer hjælper designerne med at reducere udviklingstiden, er de på grund af nedefnede begrænsninger stadig ikke gode nok til at give en signifikant reduktion af udviklingstiden for embeddeede systemer med optimerede multiprocessorer.

HW-orienteret IP-integration


Figur 4 viser et eksempel på denne hardware/software trade-off, hvor implementeringen af systemværket (det vil sige wrapper og kommunikationsnetværk) delvis mellem operativsystemet i software, et hardwareinterface og kommunikationsnetværket i hardware.

Tidskrævende proces

I den nuværende wrapper-baserede systemintegration foregår processen manuelt, det vil sige wrapper design samt forbindelse af komponenter og kommunikationsnetværk udføres manuelt. Derfor er integrationsprocessen af systemet tidskrævende, og fejl kan nemt forekomme. En manuel proces gør det heller ikke nemmere for designeren at afprøve andre løsninger af systemdesignet, ligesom det ikke er muligt at foretage en omfattende undersøgelse af designpladsen. En sådan udforskning kræver en automatisk arkitekturgenerer, der vil sige automatisk generering af wrapperne og automatisk interconnection af komponenter, wrapperne og kommunikationsnetværk.

En lovende metode

Interface-baseret design giver mulighed for et modulært design, hvor et subystem kan raffineres fra et højt abstraktionsniveau til et lavere niveau, uafhængigt af andre dele i systemet. Men da et helt system består af modeller med forskellige abstraktionsniveauer (det vil sige modeller af det raffinerede subystem på et lavt niveau og modeller af andre dele af systemet på et højt niveau), vil det være nødvendigt at kunne udføre co-simulering med et blandet abstraktionsniveau. Nuværende metoder til interface-baseret design giver imidlertid nogle begrænsninger, når det drejer sig om at understøtte co-simulering på et blandet niveau. Dette problemer skal løses i fremtidige værktøjer til systemdesign.

Som en lovende NsC-designmetode kan System Level Synthesis gruppen ved TIMA laboratoriet i Grenoble, Frankrig dog allerede nu præsentere en metode til raffinering af kommunikationen, baseret på virtuelle komponenter.

Virtual komponenter


I den generiske wrapper arkitektur, interne/eksterne porte har en eller flere kommunikationsprotokoller (Pn, P1, Pn, Pn, Pn, Pn, P1), abstraktionsniveau (A1, A1, A1, A1, A1, A1) samt specifikationspropr (t1, t1, t1, t1, t1, t1). Wrapper arkitekturen designet er designet til at understøtte mange-til-mange konverteringer af kommunikationsprotokoller/abstraktionsniveauer/sætninger af kommunikationer mellem interne og eksterne porte. For at kunne gøre dette er der en moduladapteer, som er specifik for den interne komponent, forbundet til de interne porte. Kanaaladapteren har kommunikationsprotokoller svarende til protokollene for de eksterne kommunikationsnætverk.

Hardware wrapper genereres automatisk ud fra den generiske wrapper arkitektur. Og ved automatisk, at generere operativsystemer samt anvende skabeleor for generelle multi-

Dr. Amed Jerraya, gruppled af System Level Synthesis, TIMA (Techniques of Informatics and Microelectronics for Computer Architecture)
processor target arkitekturer kan mikrokørekturken genereres. I co-simulatoringsmodeller for blandede niveauer kan wrapperen bestå af modeller med forskellige abstraktionssniveauer (for eksempel abstrakte simuleringssample og synetiserbare implementeringsmodeller).

**Ny processor på en uge**

Da designmetoden hverken forudsætter standard busprotokol eller standard komponentinterfaceprotokol, er det ikke nødvendigt for IP udviklere og systemintegratorer at anvende de standardprotokoller, der bruges i systemintegrationen. I stedet skal man for at inkludere en ny komponent, et nyt kommunikationsnetværk eller en ny kommunikationsprotokol udvikle moduladaptoere (én for hvert abstraktionsniveau), samt udvikle kanaladaptoere (én for hvert abstraktionsniveau) for et nyt kommunikationsnetværk eller en ny kommunikationsprotokol. De lagres i et kommunikationsbibliotek og anvendes af den automatiske værkstøj til genrewring af mikrokørekturken eller co-simulatoringsmodeller med blandede niveauer. Et case study viser, at en enkelt designet med denne metode kan føje en ny procesor til biblioteket på en uge. En enkelt designet kan også åben for 1-2 uger designe heterogene multiprocessor arkitekturer bestående af to forskellige processor (ARM7 og 68000) eller fire processor (to ARM7 og to 68000 enheder) til et IS-54 CDMA mobiletelefonsystem (IS95) og et switchsystem (789).
La conception des circuits intégrés en pleine révolution

La conception d’un système monopuce ressemblera à la création d’un calculateur dont l’épine dorsale est un réseau de communication embarqué sur la puce.

Selon les prévisions de STMicroelectronics, tous lesASIC seraient embarqués dans un CPU à partir de 2003. Ainsi, ce serait pour la plupart des systèmes monopuce (SoC pour «System on chip»). Cette tendance semble se renforcer même si tous les fabricants ont une ou plusieurs plates-formes dans ce domaine. La conception de ces systèmes nécessite une connaissance approfondie des circuits intégrés et des composants embarqués.

La révolution des systèmes monopuces

La société de la conférence, Data Design Automation and Test in Europe (DATE), a réuni à Munich, est dédiée à la révolution de la conception des systèmes monopuces. Deux sessions détaillant les protocoles et les processus de développement des systèmes monopuces, y compris la puce Bird, ont été organisées. Les archéologues de la conception de systèmes monopuces ont discuté de la création de systèmes embarqués et de la future SoC.

Les systèmes monopuces avec composants RF seront l'objet d'une session animée par Alain de la最大限度e de la conférence, et proposées pour les microprocesseurs embarqués. Une session animée par le professeur de l’Université de Berkeley, en parallèle de la conférence, se concentrera sur la future SoC.

La figure 2 montre l'architecture globale d'un système monopuce. Cette architecture est décomposée en couches pour maestroir la complexité. Elle est composée de deux couches de base. La base est composée des principaux composants utilisés par le système. Il s'agit de composants standard tels que...

Cont'd
des processeurs (DSP, MCU, IP mémoire).

Au dessus, la couche de communication matérielle embarquée sur la puce renferme les dispositifs nécessaires à l'interaction entre les composants. Cette couche peut contenir un réseau de communication complexe allant du simple pont (bridge) entre deux processeurs au réseau de communication par paquets (CP). II est souvent nécessaire d'ajouter des couches d'adaptation entre le réseau de communication et les composants de la première couche. II existe donc tout un type d'interface qui se propose de normaliser l'organisme V S I A (Virtual Socket Interface Alliance).

Le logiciel embarqué est développé pour sa part en trois couches. La couche basse contient les pilotes d'entrées/sorties et d'autres routines de base niveau qui contrôlent le matériel. Le code correspondant à cette couche est imbriqué au matériel. Cette couche sert aussi le matériel du reste du logiciel. La couche de contrôle de gestion de ressources permet, elle, d'adapter l'application à l'architecture. Elle fournit les fonctions utiles pour personnaliser l'architecture à des fins d'efficacité et d'isolement de l'application de l'architecture. Bien que fournie par la plupart des systèmes d'exploitation (OS), il sera souvent utile de réaliser une couche spécifique pour des raisons de taille ou de fiabilité. Les applications embarquées utilisent souvent des structures de données particulières avec des accès dédiés (manipulation de champs de bits ou partition rapide de tableaux) qui ne peuvent être fournies par les OS standard. D'autre part, les couches de gestion de ressources fournies par les OS sont généralement trop volumineuses pour être embarquées. Enfin, la dernière couche correspond au code de l'application.

Tout repose sur les communications entre blocs IP

Ce modèle d'architecture introduit plusieurs changements de fond par rapport à celui traditionnel utilisé par les concepteurs de circuits. Au niveau de l'architecture matérielle, les composants de base sont séparés de la couche de communication. Dans les schémas traditionnels, le travail de l'architecte consistait à assembler les composants sur mesure afin de prévoir interconnexions de manière efficiente et d'obtenir de meilleures performances. Or pour les systèmes monoportiques, le travail de l'architecte consiste à assembler des composants existants, en respectant les contraintes de performance et de coût au niveau du système global et non plus au niveau du seul composant. Ainsi la valeur ajoutée de la conception des systèmes monoportiques se situe plutôt au niveau de la couche de communication. Au niveau de l'architecture logicielle, la complexité des applications impose une décomposition du code en couches et les couches basées du logiciel doivent être fixées. Par exemple, l'existence de MMU, DMA et autres mécanismes pour les entrées/sorties permet de simplifier les couches de communication logicielle. Il y a même des solutions matérielles pour l'OS.

L'architecte se concentre sur les communications

La conception des systèmes monoportiques nécessite, au niveau du processus de conception, la coopération de quatre types de métiers (figure 3.6). Le concepteur système est en charge de l'architecture globale du système et établit les choix de découpage logique/matière, définit l'architecture du réseau de communication, les performances requises pour le matériel et sélectionne les algorithmes logiciels. Le concepteur logiciel est chargé...
La nouvelle répartition des tâches

Le métier d'intégrateur comportera de plus en plus de conception d'architecture.

Des outils encore incomplets

Au niveau des outils de CAO, les changements sont encore plus radicaux et ce pour les quatre métiers cités plus haut.

Pour la conception logicielle, le rôle d'outils existent à ce jour. Seuls Archimate d'Araxesys, Cerco VCC de Cadence et N2C de CoWare pourraient prétendre apporter une aide dans ce domaine.

Archimate permet de partitionner un système décrit en SDL, C, VHDL ou Verilog en blocs logiciels et matériels. Estelle fournit aussi des outils automatisés pour la génération du logiciel embarqué, du code matériel synthétique et des couches de communication. Son succès dépendra de la capacité d'Araxesys à s'adapter aux nouveaux standards émergeant du type SystemC.

N2C utilise, lui, un modèle de spécification écrit en SystemC et prétend aussi de fournir un outil de standardisation VSLA avec son modèle d'interfaces standard VCI (Virtual component interfaces).

VCC est, quant à lui, très avancé dans la génération de la couche matérielle. Par contre, il utilise aussi un modèle non standard pour la spécification système. La modélisation est en langage C mais peut aussi faire appel à une combinaison de langages C++ et C, basée sur la notation « Codesign FSM ».

Pour la conception logicielle, plusieurs solutions existantes peuvent être adaptées aux systèmes monopuces. Les plus populaires sont les outils de Logiciel et Rational basés sur la notation UML avec des extensions temps réel (SAD et ROC). Mais, encore une fois, ces langages ne sont pas très populaires chez les concepteurs de systèmes monopuces. Les solutions à base de C/C++ ne tarderont pas à gagner du terrain.

Deux types d'outils sont nécessaires pour la conception du matériel: les outils classiques de CAO pour concevoir les composants et de nouveaux outils de génération de code synthétisable à partir de modèles abstraits. Les outils de synthèse comportementale, développés depuis la fin des années 1990, ont essayé de réaliser cette fonction. Leur principal handicap était la difficulté de les integrer dans une approche logique.

Cont’d
La technologie de Sonics se fonde sur l'intégration des blocs IP de différentes origines sur un système de communication unifié.

Un fort de conception et la difficulté de simuler un bloc comportemental avec le reste du système. Avec les dernières évolutions, cette intégration devient possible et ce type d'outils risque d'être déterminant pour le succès de la nouvelle génération d'outils de CAO. Aresys semble avoir déjà réussi à intégrer un outil de synthèse comportementale dans son flot.

Pour la conception d'architecture, CoWare a été un précurseur avec sa méthode de synthèse d'interfaces pour des systèmes monopuces. Malheureusement, cette solution reste limitée pour l'heure à des architectures contenant un seul processeur. Cadence offre une méthode plus générale mais peu d'outils d'univers de conception sont encore disponibles pour la supporter. Aresys propose aussi des outils pour la génération automatique de code de communication embarquée. Par contre, la version actuelle ne permet pas l'intégration d'OS existants. De nouvelles solutions sont apparues dernièrement pour l'aide à la conception de réseaux de communication plus sophistiqués. Sonics fournit une solution autour du bus Silicon Backbone permettant d'intégrer plusieurs processeurs hétérogènes sur une puce.

Plusieurs solutions pour l'assemblage de composants mono-source existent en parallèle, comme les bus Amba d'Arm et CoreConnect d'Ibm.

Pour l'intégration, la co-simulation est opérationnelle et permet de valider des systèmes entiers. Les principaux outils viennent de CoWare, Mentor Graphics (Seamless CVE) et Cadence. Pour pallier la lenteur des outils de co-simulation, ils sont parfois combinés aux simulateurs matériels pour accélérer la simulation des parties matérielles.

Bien entendu, le monde de la recherche est en pleine ébullition pour accompagner cette révolution. En plus des universités et centres de recherche tels que Imec ou Tina, les centres de R & D de l'industrie ont beaucoup investi dans des méthodologies et outils pour la conception des nouvelles générations de systèmes monopuces. L'exemple le plus visible est celui de Philips, qui a développé toute une méthodologie et un environnement d'outils pour le développement de son TriMedia.

**Anne-Sophie Japon**

**TIMA-INPG**

**Sur le Web...**

http://www.dice-conference.com
http://timatim.imag.fr/gpaec
http://timatim.imag.fr
http://www.imec.be
http://www.vlsi.org
http://www.systems.org
MEMS components

The all-optical future starts here

The importance of technology based on microelectromechanical systems (MEMS) to optical networking is clear. Key component makers such as JDS Uniphase and Corning are rapidly buying specialist companies that can guarantee a steady supply of all-optical MEMS devices such as switches and attenuators. These specialist firms not only bring expertise in the design of MEMS components, but also the manufacturing capacity needed to produce devices in large volumes.

Among all these acquisitions and mergers, French company MEMSCAP is busy establishing its credentials as one of the leading independent suppliers of MEMS technology. "MEMSCAP aims to be the dominant provider of MEMS-based solutions to the telecoms industry," says Jean-Michel Karam, its president and CEO. "We have a broad-based expertise that will ensure we can meet all the demands of the communications sector."

MEMS are tiny mechanical devices created on a silicon wafer. For example, arrays of tilting mirrors can be used to switch light signals, while MEMSCAP is also developing MEMS-based tunable filters, variable optical attenuators and tunable lasers. The mechanical nature of the devices avoids the need to convert the light signal into electricity and back again, offering systems vendors an optical solution that is faster, cheaper and simpler than existing electronic components.

For Karam the advantage of MEMS is clear. "Compared with other all-optical technologies MEMS is a mature industry. Techniques already exist to manufacture components at high volume and low cost." Karam claims that MEMSCAP has developed a production process that achieves high throughputs and high yields, which will be crucial for the MEMS technology to penetrate the market for metro and access networks. The process exploits equipment developed for the semiconductor industry as well as more specialized machines for deep reactive ion etching, micromachining and wafer bonding.

According to Karam, the key challenge for MEMS manufacturers is assembly and packaging. "MEMS companies must provide complete solutions. Optical network providers are not interested in a piece of the puzzle." MEMSCAP has addressed this by introducing technology that allows automatic fibre alignment and active fibre alignment on the chip. The secret, believes Karam, is to think about the packaging at the start of the design process.

Scalability counts

Scalability is also crucial, Karam maintains that the technology used to produce 2 x 2 switches can easily be adapted to larger devices. But he admits that assembly will become more difficult, and he cannot yet envisage how it will be possible to align individual fibres to switches with thousands of ports.

One of the criticisms levelled at MEMS switches is that they lack the intelligence needed for next-generation optical networks. But Karam claims that components with variable optical attenuation and dispersion compensation will go some way to alleviating this problem. Further in the future, he believes that the answer lies in "systems-on-a-chip", which integrate MEMS technology with electronic circuitry that controls the switching process.

MEMSCAP is now positioning itself to become the market leader in telecoms MEMS technology. It has recently forged an alliance with ADC Communications to co-develop new optical MEMS components, and to supply the US network equipment vendor with advanced MEMS devices. It has also teamed up with Fujitsu Lab, the primary MEMS research facility in Japan, to develop and expand its product offering.

See also www.memscap.com.
MANIFESTATIONS

"Date est en passe de jouer l'égalité avec la DAC"

"Les conférences de Date approchent déjà celles de la DAC (350 papiers soumis à Date contre 400 pour la DAC)", précise Ahmed Amine Jerraya, président de cette manifestation qui se tiendra du 13 au 16 mars à Munich.

Les salons de CAO européens ont toujours eu dans le passé des succès très mitigés. Mais Date a connu une véritable réussite l'an dernier. S'agissait-il d'un phénomène ponctuel lié à un lieu ou à des conditions économiques particulières, ou bien était-ce le début d'un phénomène durable?

■ C'est vrai, Date est la première conférence européenne qui a réussi dans le domaine de la CAO. Je pense que ce succès est dû à la conjonction de deux facteurs. Premièrement, Date a su mettre en avant la communauté européenne de la conception électronique. Actuellement, la manifestation focalise toutes les énergies. Les ventes sont considérables et les produits sont tentants. Les concepteurs se sentent chez eux et se sont rassemblés autour de leur passion.

■ En plus de certains thèmes spécifiques où Date est en pointe au niveau mondial (systèmes embarqués, systèmes de hightech et des innovations telles que les utilisations de microprocesseurs multiprocesseurs), Date permet de rencontrer l'ensemble de la communauté des concepteurs, vendeurs de CAO et chercheurs. Ce sont les mêmes raisons que celles qui finissent par le thermomètre à la DAC. Actuellement sur 20% des salariés de Date vont à la DAC et une grande partie de ce recrutement est dû aux vendeurs de CAO.

Qu'est-ce que les visiteurs viennent chercher de façon générale dans une manifestation de CAO et plus particulièrement à Date?

Propos recueillis par Sabine Dumontet ■

Comment Date peut-elle se démarquer de la DAC et ne pas être une simple version réduite de la manifestation américaine?

■ La croissance de Date, 20% sur les quatre dernières années, la propulse sur l'échelle des grandes conférences. Actuellement, Date représente 30% de la manifestation américaine DAC, que ce soit en termes de budget, de nombre de visi-
MEMSCAP, la Bourse retrouvera-t-elle la fibre optique ?

La start-up grenobloise, spécialisée dans les composants pour les télécoms, frappe à la porte du Nouveau Marché, en pleine correction boursière. Hasardeux ?

Un nouveau prétendant frappe à la porte de la Bourse. L'opération qui aurait pris des allures de formalités il y a encore quelques mois (telle notre Sutororama) parait aujourd'hui risquée. Il faut en effet une certaine dose de témérité pour tenter de séduire des investisseurs en voyant la croissance exponentielle des réseaux télécoms optiques et le développement de la communication sans fil. Autant d'arguments balayés sur les marchés par de sévères déconvenues, comme en témoignent les plus récentes introductions du secteur, d'Ateliers Optonics à Orange.

Financer un outil de production. Memscap est née de l'assainissement de la recherche publique. La société a été créée en 1997 pour commercialiser des dispositifs de CAO (conception assistée par ordinateur) développés par ses fondateurs Jean-Michel Karam au laboratoire TIMA du CNRS. Pour espérer atteindre l'équilibre, elle doit désormais gérer plus vite. Ses produits et autres licences sont gourmandes en recherche et développement (20% du chiffre d'affaires). Surtout, dans le secteur des télécoms où les mutations technologiques obligent à des changements de stratégie. Ainsi, pour faire face à la demande dans les équipements optiques, Memscap a dû se renforcer avec des moyens d'affaires et des collaborateurs optiques, essentiels pour réunir les fibres. Mais il lui faut une usine. L'introduction en Bourse devrait permettre de financer l'installation d'usines de production à Grenoble (50 à 55 millions de dollars) et de renforcer le site égyptien [utile de test, d'assemblage et de packaging] à hauteur de 10 à 15 millions de dollars. L'appel au marché devrait également permettre d'intensifier le développement de licences dans l'autre segment prometteur de Memscap : les composants pour modules radio MEMS (Micro Electro Mechanical System).

MEMS, nouveaux "nerfs" des télécoms ? Fabrications à partir de silicium monocristallin, le MEMS (Micro Electro Mechanical System) est un système microscopique jusqu'alors très délicat à fabriquer. Ces composants sont à la recherche d'innovations technologiques de ce type qui permettent d'augmenter les performances des portables. "Nos composants MEMS sont plus performants et plus miniaturisés que les composants traditionnels" explique la société grenobloise, qui souligne en outre que ses solutions "augmentent la fiabilité et la performance des systèmes, réduisent la consommation électrique et le nombre de composants". SG Cowen, chef de file de l'introduction estime que "le marché des composants MEMS pour modules radio pourrait atteindre 850 millions de dollars en 2003". Et de souligner : "Memscap est la seule société à pouvoir développer des composants MEMS comportant des spécialisations avancées pour téléphones portables". Pour ce faire, de nombreux brevets ont été déposés.

Quel prix ? Reste à savoir quelle peut être la valeur boursière de ce savoir-faire ? Pour SG Cowen, les récentes opérations d'acquisitions dans le secteur justifient un tarif élevé pour Memscap : le montant de l'acquisition de Cronos serait spécialisé des MEMS acquis pour 750 millions de dollars par l'américain JDS Uniphase, NDLR est particulièrement intéressant pour Memscap car il a des compétences en termes de technologie de pointe. Avec Cronos et ses capacités, nous pouvons préparer de nouvelles réseaux de télécommunications optiques." D'autres émettent des réserves sur la capacité de la société à entrer dans un processus de production alors que son métier historique est la fourniture de logiciels. Enfin, la note de la Commission des opérations de Bourse fait état de plusieurs facteurs de risques, à commencer par le niveau des parts réalisées lors de l'offre de 1999 et 2000, et les perspectives de pertes dans un avenir proche. C'est justement pour sortir de cette situation que Memscap tente son entrée en Bourse. La jeune-pousse aura-t-elle le temps de s'y faire les dents ?

J.-F.E

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CONCEPTION

« La poussée irrésistible de la CAO européenne finira par payer »

Pour Ahmed-Amine Jerraya, directeur de recherche du Tima, la domination absolute de l'Amérique en matière de CAO électronique n'est pas inéluctable. Elle est en train de disparaître, et tous les "bobos" de la CAO européenne peuvent espérer réussir à s'imposer tout en restant indépendants.

L'Europe est-elle des spécificités en matière de besoins de logiciels de CAO ? Ces spécificités nécessitent-elles le développement d'un industrie européenne de la CAO ?

Oui, car l'Europe est en avance dans plusieurs domaines de la microélectronique. C'est le cas pour la RF, les systèmes monopuces (ou systèmes sur une puce) de manière générale, les applications multimédias et l'électronique automobile. Tous ces secteurs ont mis en place des outils de CAO spécifiques pour supporter leurs équipes de conception. L'exemple le plus visible est celui de Philips, qui a développé tout un ensemble d'outils de conception pour son processeur multimédia appelé Trimedia. Bien entendu, cette situation ne peut durer. Les investissements nécessaires au développement de ces outils sont très lourds, même pour les industriels. Il faudra bien un jour ou l'autre que les outils soient commercialisés. Ce qui donnera ainsi naissance de fait à une industrie européenne de la CAO électronique.

Par ailleurs, il faut reconnaître que la plupart des fabricants de circuits intégrés en matière de CAO demeurent très soucieux de leur nombre de correspondants avec l'Europe. Ainsi, par exemple, il y a plus d'équipes supposant le programme VCC des fabricants de circuits intégrés en Europe qu'aux États-Unis. De plus, il ne faut pas oublier le succès de l'Européen CoWare et celui des sociétés de conception européennes dans le domaine des systèmes avancés EU-électroniques.

Ce succès a d'ailleurs contribué à l'adoption de la nouvelle norme de conception en Europe. Ainsi, tous les produits de conception qui ont été développés par les fabricants de circuits intégrés en Europe ont été adoptés par les fabricants de circuits intégrés en Europe. De plus, il ne faut pas oublier le succès de l'Européen CoWare et celui des sociétés de conception européennes dans le domaine des systèmes avancés EU-électroniques.
TECHNOLOGIE SUR CIRCUITS COMPLEXES


Avec une équipe de cinq personnes, Eric Dupont, créateur de Iroc Technologies, vise 3,70 MF pour son premier exercice, puis 9 MF et 33 MF les années suivantes, avec 44 salariés.
FABRIQUER 10 CIRCUITS SANS SE RUINER, C'EST POSSIBLE !

Frédéric Rémond

Lorsqu'il s'agit de faire fabriquer des prototypes ou des petits volumes de circuits intégrés spécifiques, bien des industriels ou chercheurs sont en peine de trouver une solution abordable. Hériter entre les fondeurs classiques et les laboratoires publics, c'est, en général, naviguer entre Charybde et Scylla. D'un côté, les filières publiques (centres universitaires, laboratoires de recherche) n'ont pas les budgets qui leur permettraient de bénéficier en interne (et encore moins de proposer en externe) des équipements de fabrication de dernière génération. De l'autre, les fondeurs traditionnels refusent de fabriquer des circuits en faible volume (même à quelques milliers d'exemplaires) s'ils n'ont pas l'assurance de décrocher un marché plus juteux par la suite.

Même les technologies de pointe sont disponibles

"Il y a plusieurs années, j'avais contacté Philips pour un contrat de fabrication portant sur 25 000 circuits", se souvient Rob Van des Valk, directeur de la société néerlandaise XIC : "Le responsable m'avait signifié qu'il ne se levait pas de son fauteuil pour moins de 300 000 pièces! Et, lorsqu'ils consentent à fabriquer des circuits à quelques exemplaires, les fondeurs le font payer au prix fort. Comment pourrait-il d'ailleurs en être autrement, sachant qu'un jeu de masques pour une technologie CMOS de pointe se chiffre à 300 000 dollars au bar métal ?

UMG, par exemple, n'accepte pas de commande inférieure à un lot (soit 25 tranches de silicium de 200mm) par mois. « Affo de fabriquer des circuits dans une technologie BiCMOS classique, j'avais contacté il y a quelques années IBM France, qui était d'accord pour... 600 000 francs par prototype », se rappelle Jean Ditta, du Laboratoire d'Annecy-le-Vieux de physique des particules (Lapp). Depuis, le Lapp profite d'un accord entre le Cern et IBM afin d'avoir accès à ces technologies à moindre coût. Mais ce type d'accord reste un cas isolé et n'offre pas de solution pérenne aux PME-PMI et aux chercheurs isolés.

Il se sont donc organisées des filières spécialisées dans la fabrication de circuits intégrés en petites quantités, qui, lorsqu'il s'agit de prototypage, utilisent le principe de la fabrication multiprojet (MPW), mais qui peuvent aussi permettre d'accéder à des productions de moyens volumes (typiquement quelques milliers ou dizaines de milliers de pièces). Dans le cas du MPW, il s'agit de faire fabriquer sur une même tranche de silicium, dans une technologie donnée, les différents circuits de plusieurs commanditaires. Ces derniers s'y retrou-
Les tarifs indiqués ici sont applicables aux organismes d'enseignement publics. Pour les industriels, les prix sont les mêmes côté CMP (mais toutes les technologies ne sont pas disponibles), et de 60% à 80% plus élevés côté Europractice. A noter que les prix CMP s'entendent pour 15 prototypes, avec 5 circuits encapsulés, alors que l'encapsulation est en sus chez Europractice.

vent doublement: d'une part, ils portent les coûts de fabrication, et d'autre part, ils assurent au fondateur des débouchés suffisants pour lancer des rent réguliers à des prix attractifs. Le CMP à Grenoble et Europractice à l'échelle européenne sont les principaux représentants de cette filière en France. Ils servent en fait d'interface entre les clients et les fabricants, tels que pour le prototypage MPW que pour la fabrication en petites et moyennes quantités. Les deux organismes sont comparables sur bien des points. "D'une manière générale, CMP est plus convivial et plus souple, Europractice plus administratif", note de même - et il n'est pas le seul - Luc Hebrard, du Lepsi. Leur principal intérêt est d'offrir un accès à des technologies de pointe (voir tableau ci-dessous), qui comprennent des technologies Cmos 0,25 µm - voire même 0,18 µm, via UMC chez Europractice et STMicroelectronics pour CMP. Si les technologies Cmos et BICmos sur silicium sont de loin les plus demandées, des substrats plus spécifiques comme le GaAs, le SiGe (via AMS et ST); et le silicium sur isolant (via Peregrine) sont également disponibles, ainsi que la technologie de micro-usage de surface de Grenoble chez CMP. Le CMP et Europractice s'alignent grossièrement sur les prix, et font tous deux la différence entre leurs clients industriels (lesquels bénéficient de tarifs privilégiés, grâce notamment à des accords passés avec le Centre national de formation en microélectronique, ou CNFIM) et les autres. A noter que les premiers sont largement majoritaires au sein des utilisateurs de ce type de service ; à titre indicatif, seuls 16% des quelque 300 commandes soumises à CMP en 2000 émanaient d'industriels. Pour chaque technologie, les prix sont proportionnels à la surface occupée par les circuits sur la tranche et dépendent également du type de boîtier. Pour un laboratoire de recherche commandant à CMP 15 circuits mesurant 3 x 3 mm chacun en technologie Cmos 0,6 µm, il en coûtera par exemple 3800 euros, encapsulation en boîtier BGA comprise. Les organismes d'enseignement publics ont, de plus, accès aux technologies de pointe plusieurs mois avant les industriels, et se voient proposer des kits CAO à prix solidé.

Les détails de livraisons malmenés par les fondateurs
En revanche, le test fonctionnel des circuits est rarement compris en ce qui concerne le MPW. "Lorsque nous avons réalisé le design de notre circuit, le CMP ou Europractice mettent une dernière vérification des règles de dessin et des règles électroniques et nous répercutent les erreurs rencontrées pour correction", tempère Jean-Pierre Richer, du Laboratoire de l'accélérateur linéaire (Orsay), qui ajoute : "Nous sommes donc certains d'envoyer des masques corrects au fondateur, mais, par contre, la conception est de notre entière responsabilité. » L'ensemble du traitement, de la commande à la réception des circuits, prend en moyenne 5 mois. "Les délais sont souvent malmenés par les fondateurs", déplore David Lachartre, du Léti. Ces temps ne sont en effet pas prioritaires pour les fondateurs, qui n'ont d'ailleurs pas à les retarder, parfois de plusieurs mois, lorsque des périodes de pénurie aident l'industrie des semiconducteurs. A moins de payer le prix fort... Autre reproche émanant des utilisateurs du CMP et d'Europractice : l'impression désagréable d'être, in fine, laissés seuls face au fondateur pour régler les détails de fabrication. L'aide à la conception, elle, est plus difficile à quantifier. Jugée "satisfaisante" ou "négligeable" selon les utilisateurs, elle dépend évidemment du seuil d'avancement du projet. Même si, à l'image de Jean Pollard, pdg d'Opsi, certains regrettent que les offres d'outils CAO soient si larges, réservées aux utilisateurs et l'absence de logiciels à l'heure de l'ici de nombreux petits industriels. »

Une filière victime de la loi de Moore ?
Quel avenir pour ces organismes ? La tentation de concurrencer les sociétés de conception classiques est grande, tant chez CMP (notamment pour les microsystèmes, partiellement traités en interne) que chez Europractice, qui ne possède pas l'impression de l'ici. En plus de l'aspect fabrication, Europractice groupent des utilisateurs de CAO, qui peuvent faire des prestations de conception au sein d'un réseau accessibles à des tarifs préférentiels. Difficile, toutefois, de se transformer en un service à peine sans perdre de vue l'aspect "service public", pour lequel ces deux organismes sont partiellement financés. Les services offerts s'étendent toutefois, grâce à la souple offerie par l'usage de blocs d'IP (propriété intellectuelle) ; CMP a ainsi recentrement inclus dans son offre les circuits de silicium 32 bits d'ARM, avec les outils CAO d'Alcatel (600 euros par licence pour la suite logicielle ADS), pour les universitaires développant des systèmes sur une puce. Mais cela reste une exception, et la
plupart des "grands" des semiconducteurs rechignent à fournir leur IP pour une bouche de pain. Or la complexité grandissante des technologies pourrait, à moyen terme, limiter l'intérêt des fibres de prototypage bas coût : pour profiter pleinement d'une technologie CMOS 0,18µm, il n'est pas question de n'utiliser que des cellules standards et de réinventer la roue pour concevoir un simple bloc mémoire. Autre écueil, également lié à la loi de Moore : les fondeurs, en abandonnant la fabrication sur tranche de 100 mm pour passer à des tranches de 200 mm, en s'imprudent par exemple dans les engineerings pour servir à tester les lignes de production (en renonçant alors à garantir un niveau de qualité industriel).

LES SERVICES MPW À L'ÉTRANGER

De nombreux pays à travers le monde disposent de centres de fabrication MPW complétés avec que fait le CMP en France, le plus connu étant sans doute MOSIS lancé en 1980 par la DARPA américaine et rapidement étendu aux applications multimultiples. Autres organisations proposant des budgets d'essais des technologies : CMSI au Canada, VDES au Japon, IDES en Corée et CIC en Taiwan.

(1) Les industriels représentent transferts environ 30% des fabrications enregistrées par CMP, car ils sont dépourvus de demandeurs de petits et moyens volumes.

(2) Le CMP est un service à bas non lucrative mis en place en 1981 par un groupe industriel (la Xerox) en France (Télécoms R&D) ; le CNES et le CNES ont lancé en 1996 dans le cadre du 5e P.CRD ;
Autour de Grenoble, un pôle recherche et industrie en électronique a donné naissance à quelques start-up très spécialisées

nics (5 milliards de dollars de chiffre d'affaires en 1999), estalée à Croissières, Atrinex-Thomson-CSF à Saint-Egrève, Schneider Electric ou Hewlett-Packard. Timia, plus modeste, a aussi joué un rôle de passerelle entre recherche et industrie.

Sur ce terrain, le transfert de technologies permanent entre l'industrie permet de belles réussites. « Dans les années 80, le Léti a beaucoup transféré de technologies à STMicroelectronics. Depuis les années 90, il transmet de plus en plus sous la forme de start-up », explique Jean Thémer, président du CEA Grenoble. En effet, une bonne dizaine de start-up commencent à acquérir une notoriété internationale. Opstech et RIC, Memsac ou Inca, Soitec, Tronic's ou Alditech... Soitec est déjà entrée en Bourse ; Memsac, de son côté, est citée dans le Wall Street Journael comme l'une des sociétés les plus recherchées d'Europe dans les microsystèmes pour fibre optique.

Et entre start-up et laboratoire, la mayonnaise prend grâce à la constitution de liens forts. A la tête de ces start-up, se trouvent des chercheurs pour la plupart issus du CEA. Soitec, par exemple, a fondé son activité sur le technologies du SOI (Silicon On Insulator). Technologies et le procédé Smart Cut, qui consistent à déposer au moindre prix une fine couche d'isolant sur les disques de silicium sur lesquels seront gravés les transistors. Ces deux techniques achetées au Léti ont nécessité 15 ans de développement. Les dirigeants de ces start-up sont tous peu ou prou clients, fournisseurs ou partenaires les uns des autres. Opstech a développé des micro-commutateurs optiques destinés aux équipements de télécoms grâce à la mise en œuvre d'une technique recherchée au Léti.

Dans ces conditions, « impossible de renoncer à la compétence industrielle » ajoutait Jérôme, président du CEA Grenoble. En effet, une bonne dizaine de start-up commencent à acquérir une notoriété internationale. Opstech et RIC, Memsac ou In-cam, Soitec, Tronic's ou Alditech... Soitec est déjà entrée en Bourse ; Memsac, de son côté, est citée dans le Wall Street Journal comme l'une des sociétés les plus recherchées en Europe dans les microsystèmes pour fibre optique.

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Et entre start-up et laboratoire, la mayonnaise prend grâce à la constitution de liens forts. À la tête de ces start-up, se trouvent des chercheurs pour la plupart issus du CEA. Soitec, par exemple, a fondé son activité sur le technologies du SOI (Silicon On Insulator). Technologies et le procédé Smart Cut, qui consiste à déposer au moindre prix une fine couche d'isolant sur les disques de silicium sur lesquels seront gravés les transistors. Ces deux techniques achetées au Léti ont nécessité 15 ans de développement. Les dirigeants de ces start-up sont tous peu ou prou clients, fournisseurs ou partenaires les uns des autres. Opstech a développé des micro-commutateurs optiques destinés aux équipements de télécoms grâce à la mise en œuvre d'une technique recherchée au Léti.
Sans-fil et optique pour Memscap

JEAN-MICHEL Karam, Franco-libanais et Grenoblois d'adoption, sort du lot. Il est plus à l'aise dans un costume d'entrepreneur que ses collègues des start-up issues du CEA, PEG de la société Memscap, qui fabrique des "mems" (Micro-Electro-Mechanical Systems), systèmes microélectroniques pour l'industrie du sans-fil et de l'optique, il n'a pas passé vingt ans dans un laboratoire. Ce trentenaire ne fut pas père chercheur pour autant. Jean-Michel Karam a exploité ses trois ans au Tima (1), spécialisé dans les outils de CAO pour circuits intégrés, situé à l'Inpg (2), pour s'imposer comme un spécialiste des mems. « Je dois tout à un de mes professeurs de l'Esiee (3), que j'ai d'ailleurs débauché pour Memscap », précise-t-il.

Née fin 1997, Memscap, 3 millions d'euros de chiffre d'affaires en 2000, a levé plus de 70 millions de francs à ce jour. La jeune entreprise en est au même stade qu'un Tronic's ou un Optilech : il n'y a plus qu'à construire l'usine. Jean-Michel Karam a prévoit une de 40.000 mètres carrés, pourquoi pas au Bèrnin, à une dizaine de kilomètres de Grenoble, tout près de son ainé ST Microelectronics. Mais Memscap est bien plus structuré que ses cousins. La société compte déjà une centaine de salariés, cinq implantations en France, une à Berlin, deux aux Etats-Unis, et un centre de recherche et développement au Caire.

De plus, pour échapper au syndrome du monopole, Memscap s'est diversifié sur trois activités. Tout d'abord l'édition de logiciels de conception des mems, après avoir récupéré son principal concurrent, l'américain Tanner. Ensuite, la vente sous licence de mems pour l'industrie du sans-fil, qui devraient permettre l'intégration de tous les composants passifs d'un téléphone portable (battery...) sur une seule puce de radiofréquence.

Enfin, Memscap veut fabriquer des commutateurs optiques, qui permettront aux équipementiers de télécoms de concevoir des réseaux tout optique plus performants. Memscap a signé avec ADC, spécialiste américain de la fibre optique, 2,8 milliards de dollars de chiffre d'affaires en 2000, pour un accord de codéveloppement de trois lignes de produits, tout comme avec Fujitsu-Lab, premier laboratoire pour la recherche sur les mems au Japon.

Aujourd'hui, la start-up compte déjà Motorola ou Schlumberger comme clients, et elle augmente déjà l'appétit, des grands équipementiers de télécoms : « C'est une société similaire à la nôtre, a été rachetée environ 250 millions de dollars par l'américain JDS Uniphase en avril 2000... » précise Jean-Michel Karam.

C. Du.

(1) Tima : Technique de l'informatique et de la microélectronique pour l'architecture des ordinateurs.
(2) INPG : Institut national polytechnique de Grenoble.
(3) Esiee : Ecole supérieure d'ingénieurs en électrotechnique et électronique, à Paris.
Iroc protège les puces des radiations

La paroi que les radiations sont plus petites, les puces sont également plus fragiles. À leur seul, le soleil est souvent devenir une source de danger pour les circuits électroniques. Lorsqu'ils rencontrent une puce, les neutrons diffusés par les rayons solaires sont en effet susceptibles de provoquer des erreurs électriques. Bien sûr, en tant que tel, un neutron est inoffensif. Mais lorsqu'il interagit avec certains dopants, comme le bore, il peut créer des particules alpha, qui, elles, sont chargées électriquement.

Limites les erreurs dans les futurs procédés de gravure
Sans provoquer de dommage physique, ces particules agissent alors comme un signal électrique non désiré. « En technologie de gravure 0,25 micromètre, la fréquence d'apparition de ces erreurs est d'une fois sur les cinq jours. Elle passe donc à peu près inaperçue ou bien elle est masquée par les erreurs logicielles », explique Eric Dupont, P-DG d'Iroc Technologies.

Mais, du moins, les choses risquent d'être changer. D'après une étude d'Intel, AMD et Compaq, les prochaines technologies de gravure augmenteront cette occurrence à une ou deux erreurs par heure ! Car plus on accroît la densité de composants présents sur une petite surface, plus on augmente la probabilité pour les neutrons de toucher des éléments qui interagissent avec eux.

C'est à partir de cette analyse qu'Iroc a été créée en janvier 2000. À son origine, les travaux d'un chercheur, Michael Nicolaides, du laboratoire microélectronique Tima, une association d'industriels (Monsaap, Anacap...), et d'Eric Dupont, un ancien de la DGA, qui le compte.

Une capacité d'auto-vérification interne
« Plus les circuits deviennent complexes, plus il faut donner aux puces la capacité de réagir par elles-mêmes », analyse Éric Dupont. En effet, au moment où elles sont fabriquées, personne n'est capable de dire où un environnement elles vont être utilisées. De plus, leur complexité augmentant, il est quasi impossible de tester toutes les puces à 100% au moment de leur fabrication. La solution retenue est donc de leur fournir une capacité d'auto-vérification interne.

Un pari osé ! Certainement. Car il faut convaincre les industriels que leurs puces électroniques peuvent avoir des comportements erratiques. Mais aussi que la protection à un coût. « Il représente au plus 10 à 15% en surface de silicium supplémentaire », tempère Éric Dupont.

Le marché châtié est celui de l'industrie des semi-conducteurs au sens large. Éric Dupont se dit confiant. Iroc finalise actuellement un premier tour de table de 4 millions de dollars. « 2001 sera pour nous une année de construction », assure-t-il.
Informatique

Professeur à l’Institut des sciences et techniques de Grenoble (ISTG), l’école d’ingénieur de l’Université Joseph Fourier, Dominique Borronne transmet avec passion son métier d’informaticienne tournée vers l’industrie.

Dominique Borronne
Des mathématiques à l’informatique

"Je déteste les mathématiques, mais j'adore l'informatique!" Cette citation de Dominique Borronne, une des rares enseignantes en informatique au sein de la filière ingénieurs SI de l'Université Joseph Fourier, est une illustration de l'importance de l'informatique dans nos sociétés modernes.

Dominique Borronne a commencé sa carrière en informatique après avoir obtenu son BAC de Mathématiques à Marseille en 1966. "La découverte de la sociologie et l'apprentissage de l'anglais m'ont donné une expérience décisive pour la Reste de ma carrière", dit-elle. Elle a aussi obtenu une licence en anglais à l'Université Joseph Fourier.

Née en Italie, elle a suivi son enfance dans une ville de l'ouest de la France et a finalement étudié à l'Université Joseph Fourier. "J'ai aimé les mathématiques à l'école, mais j'ai détesté les mathématiques à l'université", raconte-t-elle. "Je m'attendais à ce que les mathématiques soient plus utiles en réalité, mais elles ont été un obstacle pour moi.

Désormais, Dominique Borronne enseigne l'informatique à la faculté des sciences de l'information et de la communication à l'Université Joseph Fourier. "J'adore enseigner l'informatique, c'est un terrain ouvert et plein de possibilités", dit-elle.

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Des satellites aux téléphones portables : le combat contre les ions lourds pour sauvegarder nos mémoires

L'environnement radion est un problème des perturbations dans le fonctionnement des équipements électroniques digitaux embarqués. Parmi ces perturbations, l'effet de l'ondulum est un SEU, qui provoque de la circulation dans toutes les zones sensibles d'un circuit intégré. On peut avoir pour conséquence la propagation de séquences anormales ou la défaillance de l'information contenue, dans un point critique. La nature électronique de l'ondulum impose que la mémoire cellule soit modifiée à l'ondulum et que la gravité des conséquences qu'il peut entraîner rende le phénomène SEU très critique. De plus, l'évolution technologique aboutit à un accroissement de la densité d'intégration créant une plus grande sensibilité des circuits électroniques vis-à-vis de ce rayonnement spatial.

Afin de pallier ce fléau, le laboratoire des Techniques de l'Informatique et de la Microélectronique pour l'Architecture d'ordinateurs TIMA CNRS a développé au cours des années 1990 un nouveau concept de cellules mémoire capable de restituer l'information modifiée par l'effet d'une particule. Cette approche permet l'utilisation de technologies standards pour la fabrication de circuits intégrés peu ou pas sensibles aux effets du rayonnement spatial et est utilisée sur plusieurs satellites (METOP, ROSETTA, ARgos...).

En 1995, le CNRS contrôla un Nouvel programme d'exploration dans ce domaine dont les applications terrestres et aérospatiales sont très importantes. En effet, la maîtrise de la technologie d'ondulum aurait un impact sur plus de 80% des circuits intégrés essentiels à la sécurité de l'information (military, aeronautics, satellites,...). Le CNRS a signé un accord de licence avec le CNRS pour l'utilisation de ces cellules HT (Heavy-Ion Tolerant) capables de tolérer les effets transitoires des radiations.

Les cellules HT (Heavy-Ion Tolerant) permettent de développer des applications digitales embarquées en utilisant des technologies standard existantes et en augmentant la densité de l'information stockée. Le CNRS a développé des cellules de mémoire capable de restituer l'information stockée malgré les effets transitoires des radiations. Ce sont des applications très importantes dans les domaines du numérique et de l'information. (source : CNRS)

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From satellites to portable telephones: the battle against heavy ions to protect our memories

The radiation environment in space causes interferences in the functioning of on-board digital electronic equipment. Among these interferences, the soft error (SEU) is a principal cause due to the collision of heavy ions on sensitive areas of an integrated circuit, can result in the propagation of incorrect signals or the loss of information contained in a memory location. The not very sensitive to external radiation and which are used on several satellites (METOP, ROSETTA, ARgos,...)

In 1995, the CNRS initiated a new program with the development of this process whose terrestrial and aeronautical applications are promising. The increasingly high degree of miniaturization of integrated circuits and the desire to extend the service life of products multiplies the probability of occurrence of errors as a direct or indirect consequence of radiation. At a time when computers accompany us of every step of our daily lives, where sub-orbital satellite projects are under development, this risk has not escaped the attention of the ATMEL company (ex-Motra M4S), which has signed a license agreement with the CNRS for the industrialisation of HT (Heavy-Ion Tolerant) cells capable of tolerating the transient effects of radiation.

The HT cells show the possibility of using highly advanced sub-micro techniques in severe environments without adding specific processes and they are an answer to the problems of the effects of atmospher...
VIII.3 Social life and cultural life

Recently, the Laboratory had the pleasure to congratulate some of its members for marriage and births.

Have got married:

- Lydie HEUSCH (SANZ) 25 May 1991
- Masaki NITO 8 June 1991
- Mokhtar BOUDJIT 13 June 1992
- Pascale VÉRUGIN (DULIEUX) 4 July 1992
- Francois MARTIN 15 August 1992
- Ahmed Amine JERRAYA 26 September 1993
- Patricia SCIOMONE (CHASSAT) 17 June 1995
- Sylvaine EYRAUD (LAYE) 24 June 1995
- Clifford LIEM 10 August 1996
- Kheloun TORKI 22 July 1997
- Pascal COSTE 23 January 1999
- Philippe LEMARREC 21 August 1999
- Raoul VELAZCO 8 December 1999
- Régis LEVEUGLE 6 May 2000
- Sergio MARTINEZ 7 July 2000
- Vijay VIJAYARAGAVAN 7 July 2000
- Zein JUNEIDI 9 November 2000
- Sami MEFTALI 23 December 2000
- Gilles SIGARD 26 May 2001

The following will be descendants of Laboratory's members:

- Eméric AMIELL 12 June 1991
- Luc BERGER SABBATEL 13 July 1991
- Aurelie GARNIER 7 September 1991
- Anna KOLARIK 20 September 1991
- Florian HEUSCH 2 November 1991
- Moussab BEN OTHMAN 21 November 1992
- Thaís CASTRO ALVES 2 October 1993
- Natasha LUBASZEWSKI 3 May 1993
- Aladin SKAF 2 August 1994
- Gabriel GARNIER 28 August 1994
- Andressa LUBASZEWSKI 11 December 1994
- Lydia JERRAYA 3 February 1996
- Ceyla SIMEU 14 March 1996
- Jeanne DING 7 April 1996
- Lucas PEREZ-RIBAS 1 August 1996
- Carolina OLIVEIRA-DUARTE 15 September 1996
- Laurine SCIOMONE 10 October 1996
- Paola VALDEIRRA 15 April 1997
- Gabriela LAPERSA RIBAS 23 September 1997
- Stephanie WANDER 10 November 1997
- Chloe EYRAUD 31 January 1998
- Manon COISSARD 13 February 1998
- Nels ESSALHIENE 5 September 1998
- Nelly JERRAYA 30 September 1998
- Héloïse OSTIER 19 January 1999
- Pedro Jungblut HESSEL 21 October 1999
- Benjamin EYRAUD 4 October 2000
- Flora Lanche MARTINEZ 6 October 2000
- Amine-Mohamed TORKI 6 October 2000
- Maria-Laura MORAWIEC 19 November 2000
- David RUFRER 11 February 2001
- Garance CHARLOT 18 June 2001
- Cecilia MEFTALI 22 June 2001
- Djoser SIMEU 23 July 2001
- Jeanne CHAUMONTET 28 September 2001
- Nawar ALZAEHER-NOUFAL 3 December 2001
- Anh Thu DINH-DUC 11 January 2002
- Thibault SICARD 19 January 2002

Some have even found their wife/husband in the Laboratory itself:


As for funds, the Laboratory has recurrent social events and exceptional social events. The meelou's party is a traditional annual party. The Laboratory has been a few times horse-riding, even those being very beginners. Visitors are often taken for walks in the mountains.

Besides fundamental research activities, TIMA Laboratory promotes cultural activities such as temporary exhibitions of paintings and sculptures.

In 1999, an amateur sculptor and two artistically talented researchers were given the opportunity to exhibit their works.

First, in January 1999, Sidney COHEN, whose artistic training was carried out at the "Ecole des Beaux-Arts" of Grenoble, exhibited sculptures in alabaster, dedicated to personal interpretations of the notion of creativity. (Picture VIII-3 10).

In May 1999, Charles PAYAN, research scientist at CNRS, exhibited his collection of stereograms, some especially created for TIMA and its scientific audience. His minimal representations - shapes and volumes - explored perceptions of space. (Picture VIII-3 11).

In November 1999, Raoul VELAZCO, director of the QLF group at TIMA, exhibited a series of paintings inspired by famous works of French painting schools of the last century as well as original creations. (Picture VIII-3 12).

In January 2000, Ali BENAYHIA, an amateur painter, who has been living in the South Grenoble area for the last 20 years exhibited a series of landscapes and country life scenes of the "South Vercors Massif". (Picture VIII-3 13).

And finally, in his exhibition at TIMA, from the 15th to the 26th of January 2001, Philippe JORRAND has shown 48 of his recent paintings and drawings. Philippe JORRAND holds a position of research director at CNRS. His carrier covers industrial as well as academic experience, both in France and in the US. He has founded and has been the director, for more than 15 years, of large computer science, artificial intelligence and discrete mathematics laboratories. Now a member of Lebniz Laboratory in Grenoble, he heads a new research group in quantum computation and quantum information, a promising long term research topic, at the encounter of quantum physics and theoretical computer science. He has recently been elected chairman of the Information and Communication Science and Technology board of CNRS in Paris. He considers drawing and painting as a natural complement to scientific research, as another dimension for creativity. The main themes which attract him are inspired by nature. His trees, his feminine nudes and faces always tell something about life, but they also stay a distance away from reality: there is sometimes just a gentle step aside, with moved shapes and shifted shades, sometimes a blunt and far away jump with crude colors and distorted lines. His paintings and drawings show a preference for "no look back, no way back" techniques: watercolor, ink, charcoal. Once on the paper, no line, no color may be hidden, it is there for ever, as a means of satisfying a desire of decisive commitment. (Picture VIII-3 14).
Picture VIII-3 1: Horse-riding across Vercors
Picture VIII-3 2 : Annual parties in the open air
Picture VIII-3 3 : Walk in the mountain with visitors

For example on this picture, one can see Marta RENCZ and her daughter (1st plan), or Janusz RAJSKI, Mc Gill University (1st plan too, with a hat) and his family.

Picture VIII-3 4 : Skiing excursion
Picture VIII-3 5: 1996: Annual party in a restaurant

Picture VIII-3 6: The TIMA football team (that beat CSI 5-0 June 1992)
FOOTBALL TOURNAMENT

Picture VIII-3 7:
Football tournament organized in 2000:
The MCS and SLS teams
Picture VIII-3 8:
For the Mundial 1998, Brazil had many supporters in TIMA (here are pictured the children of R. PEREZ-RIBAS and W. CESARIO, also noticed by France 3 radio-broadcasting)
Picture VIII-3 9:
Annual party 2001 and TIMA football team
Pour fêter l'exposition des sculptures de Sidney Cohen Du 5 au 16 janvier dans la grande Salle de TIMA, le laboratoire est heureux de vous convier à un déjeuner pour l'Epiphanie le mardi 5 janvier à 15 h 30.

Laboratoire TIMA 46 Avenue Felix-Viallet Grenoble

Picture VIII-3 10 :
Sidney COHEN exhibition
Picture VIII-3 11:
Charles PAYAN exhibition
Picture VIII-3 12:
Raoul VELAZCO exhibition

Picture VIII-3 13:
Ali BENYAYHIA exhibition
Picture VIII-3 14:
Varnishing of the exhibition of Philippe JORRAND (right) paintings, with Yves BRUNET (middle), Chairman of INPG and Bernard COURTOIS (left), Director of TIMA