TIMA Laboratory
ANNUAL REPORT 1997
B. COURTOIS
May 1998
ABSTRACT

This is the 1997 annual report of the TIMA Laboratory (Techniques of Informatics and Microelectronics for Computer Architecture). The Laboratory is approximately 100 people large.

The Laboratory is organized in research groups: Integrated Systems Design (ISD), MiCroSysytems (MCS), Quality of Complex integrated Systems (QCS), Reliable Integrated Systems (RIS), System Level Synthesis (SLS), Verification and modeling of Digital Systems (VDS), QuaLiFication of circuits (QLF). The Laboratory is also hosting the CMP Service, serving for chips and microsystems fabrication.

Key achievements in 1997 are the first experiments of XXI, a distributed cosimulator tool allowing parallel execution of SDL-C-MATLAB-VHDL simulators, the reconfiguration of neural networks exposed to space radiations in the Microelectronics and Photonics Test Bed of the Naval Research Laboratories and the development of GaAs-based MEMS technologies in view of the enhancement of RF ICs.

In 1997, the Laboratory organized, or co-organized, or chaired the Programme Committee, of the On-Line Testing Workshop in Crete (M. NICOLAIDIS), of the THERMINIC Workshop in Cannes (B. COURTOIS), and of the VLSI Test Symposium in Monterey (M. NICOLAIDIS). In 1998 and 1999, it will organize, or chair, or co-chair the Programme Committee, of the Codes/CASHE Workshop on codesign in Seattle (A. JERRAYA), of a NATO school on system level synthesis in Borga (J. MERMET and A. JERRAYA), of the DATE Conference and Exhibition in Munich (D. BORRIONE) and of a new event on Design, Test and Manufacturing of MEMS/NOEMS in Paris (B. COURTOIS).

The report is organized into 8 main sections including the Research and Service activities, the Resources and the Technology Transfer activities.

Any further information may be obtained from B. COURTOIS, TIMA, 46 avenue Félix Viallet, 38031 GRENOBLE Cedex, FRANCE.
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I - OVERVIEW - GENERAL INFORMATION

I-1 Organization

Since the late 60s, the members of the Laboratory have dealt with projects and tools on hardware and software:

Hardware:

- Computers:
  + the geo-physical machine GEOPROCESSOR (1970/1975)
  + the PASCAL machine PASCHL (1972/1981)
- Microprocessor-based architectures:
  + electronic exchange system CANOPUS
  + the CORAIL machine
  + the CRESUS project
- Microprocessor type circuits:
  + microsequencer MSQ
  + microprocessor 8 bits NMOS P68
  + microcomputer 4 bits SOS MOM 400
  + the MOSAIC project for the architecture of VLSI systems
  + series line control by LISA microcontroller
  + microprocessor 8 bits POPY
  + microprocessor 8048 CMOS
  + microcontroller COBRA
  + mathematical coprocessor FELIN
  + compiled microprocessor 6502
  + MAPS controller
  + 1553 controller
- AI oriented machines
  + OPALE machine
  + LAIOS lattice
  + SPAN mechanisms
  + SYMBION architecture
- VLSI
  - Macrosystems and Microsystems.

Software:

- Electrical simulation
  + IMAG 2
  + IMAG 3
  + IMAG 4
- Digital simulation
  + CASSANDRE
  + LASCAR
- System simulation
  + LASSO
- Multilevel, mixed-mode simulation
  + CASCADE
- Physical design
  + LUCIE
- Architectural synthesis
  + AMICAL
- Verification
  + PREVAIL.

This experience serves as background to research in the field of the Design and Test of circuits and systems.

In 1997, the Laboratory was organized in 7 research groups, as listed below:

  + Integrated Systems Design (ISD), A. GUYOT
  + MiCroSystems (MCS), J.M. KARAM
  + Quality of Complex integrated Systems (QCS), L. BALME
  + Reliable Integrated Systems (RIS), M. NICOLAIDIS
  + System Level Synthesis (SLS), A.A. JERRAYA
  + Verification and modeling of Digital Systems (VDS), D. BORRIONE
  + QuaLiFication of circuits (QLF), R. VELAZCO

In addition, the Laboratory is hosting the CMP service activity.
I-2 Research themes

Each topic of the research group is briefly described below:

* Integrated Systems Design (A. GUYOT)
  - This research group addresses the following topics:
    - arithmetic operators
    - full custom VLSI design
    - on-line operators
    - application of redundant number systems
    - digital signal processing
    - arithmetic operators testing

* MiCroSystems (J.M. KARAM)
  - This research group addresses the following topics:
    - silicon compatible micromachining
    - CAD and CAT of micromechanical systems
    - microsystems for safety critical applications
    - thermal modeling

* Quality of Complex integrated Systems (L. BALME)
  - This research group addresses the following topics:
    - modelling of complex integrated systems
    - total quality management window concept
    - smart power card

* Reliable Integrated Systems (M. NICOLAUDIS)
  - This research group addresses the following topics:
    - self-checking circuits
    - built-in self test
    - test patterns for regular structures
    - CAD tools for testability
    - radiation hardened/tolerant circuits

* System Level Synthesis (A.A. JERRAYA)
  - This research group addresses the following topics:
    - SDL based hardware software codesign
      - hardware-software co-design
      - system-level design representation
      - system level specification with SDL
      - hardware/Software partitioning
      - virtual prototyping and C-VHDL Cosimulation
    - VHDL based behavioral synthesis
      - scheduling and optimization for the synthesis of control flow dominated design
      - interactive behavioral synthesis
      - linking behavioral synthesis with existing CAD environments
      - behavioral synthesis for structured design methods and design re-use
      - programmable architecture design
      - behavioral synthesis for low power
+ Multilanguage cospecification, codesign and cosimulation

* Verification and modeling of Digital Systems (D. BORRIONE)
  This research group addresses the following topics:
  + hardware description languages
  + specification languages
  + VHDL
  + formal verification
  + model checking
  + proof of correctness
  + automatic diagnosis of design errors

* QuaLiFication of circuits (R. VELAZCO)
  This research group addresses the following topics:
  + methodology and tools for test under radiation
  + design hardening of circuits devoted to space applications
  + design of experiments on board satellites
  + digital implementation of intelligent control (fuzzy logic, neural nets)
I-3 Some past realizations of the Laboratory

The following pictures illustrate some past and recent realizations of the Laboratory.

a) Cooperation with THOMSON led to the design of a self-checking, self-testing circuit (CMOS, 1.2 μ, 2 metallization layers, 650,000 transistors). The circuit is testable at the "transistors, metallizations, etc..." level (1985).

b) The SYCO silicon compiler took as input a behavioural ("Pascal like") description of the algorithms to be implemented in the silicon. b-1 is a 6502 CMOS control section compiled by the CPC specialized control section compiler ; b-2 is a 6502 NMOS data path compiled by the APOLLON specialized datapath compiler (ca 1988).

c) Electron-beam testing has been experimented through two equipments : a CAMECA ST-15 electron-beam tester and a JEOL 35C scanning electron microscope equipped for voltage contrast. These equipments have been served by a SUN and an IBM workstation, respectively (1987 - 1993).

d) The FELIN circuit was a design resulting from a cooperation with the Parallel Algorithmic Laboratory. It is aimed at the calculation of elementary functions like sine, cosine, etc... The circuit involved approximately 100,000 transistors, fully generated by a program describing the circuit (1987).

e) CMP National Service gives the possibility to Research Centers, Universities and Commercial Firms to have their circuits manufactured. The Université Catholique de Louvain, CNET-CNS, THOMSON, MHS, ES2, TCS, AMS have manufactured bipolar, GaAs, NMOS and CMOS circuits for the CMP since 1981. One 4 inches wafer holds 73 CMOS different projects (15 wafers) and one 5 inches wafer holds 40 CMOS projects (5 wafers). Both have been processed by MHS, in 1986 and 1987, respectively.

f) The computing room regrouped computers that were not distributed in offices. Here are several SM 90, a SPS 9, and a MicroVAX. The air conditioned room had been fully remodeled in 1987 (electric power, floor, etc...). Today, all computers are distributed in offices.

g) In the past, computers have been designed. g-1 shows the GEOPROCESSEUR (1970) which resulted from a cooperation with IFP, g-2 depicts the PASCSEILL (1976) language - oriented computer, and g-3 shows the CANOPUS (1980) system which resulted from a cooperation with CNET-LAA. Presently the computer architecture projects are dealing with parallelism and with a logic - numeric integration.

h) ADELAIDE was a project aimed at testing PCB populated by SMT devices. A prototype demonstrated the feasibility of an ATE, which uses extensively anisotropic elastomer conductors. Such a tool would allow a resolution of 10/1000 inches. The project has now been passed to industry.

i) Circuit synthesized by AMICAL (1993). This circuit is a PID synthesized by AMICAL (300 behavioral VHDL lines as input, 4000 RTL VHDL lines as output) feeding a commercial logic synthesis tool generating 50,000 transistors (20 mm², 8μ CMOS). Design time : 1 week. This design results from a hierarchical use of AMICAL. One of its components is a fixed point arithmetic unit.
that has been designed using AMICAL.


k) Microelectronics for Physics. BiCMOS wafer from CMP.

l) Micromachining by CMP. Process at industrial manufacturers, post-process at Central Laboratories.
a - Participation to a THOMSON project

b - 

c - Electron beam testing

d - 

f - computing room

h - SMT PCB tester

Picture I-3 1
1 - 6502 Control section

2 - 6502 Datapath

b - SYCO silicon compiler
1 - GEOPROCESSEUR computer

g - Past computer projects
Circuit synthesized by AMICAL.
1 - Micromachining by CMP

k - Microelectronics for Physics
I-4 Some data on Grenoble's environment

Grenoble offers a very good environment in terms of Education, Research, High Tech Activities, Industry.

* Education

Grenoble has been awarded the "European University" title within the University 2,000 Project.
* 40,000 students
* 5,500 foreign students
* 1,500 science degrees awarded each year
* 1,000 engineers graduate each year
* 600 "Erasmus" scholarship students
* 1 International secondary school

* Research

Grenoble is the first French research center in Engineering Sciences, the second in Physics, the third in Mathematics.
* 8,500 researchers (the largest concentration of CNRS researchers in Engineering Sciences after Paris)
* 1,500 foreign researchers
* 250 laboratories
* 5 European research centers:
  - ESRF, European Synchrotron Radiation Facility
  - ILL, Laue Langevin Institute
  - IRAM, Millimetric Radio Astronomy Institute
  - SNCL, National Service for Intense Magnetic Fields
  - EMBL, European Molecular Biology Laboratory
* 4 National research centers
  - CNRS, National Center for Scientific Research
  - CENG, Grenoble Nuclear Research Center
  - CNET, National Center in Telecommunications Research
  - CRSSA, Research Centre for the Army Health Services
* 1 research center of international proportions acquired every 10 years since 1946

* High tech Activities

* Electronics 470 industrial companies, 13,250 jobs
* Biomedical technologies 104 industrial companies, 2,600 jobs
* Imaging technologies 50 industrial companies, 800 jobs
* 1 Technopole of 65 ha housing 200 companies and 5,000 jobs (ZIRST Meylan)

** Industry **
* 3,500 companies created each year
* 133 foreign-owned capital companies, employing 25,000 people
* 1 Business District to welcome company headquarter and professional services (EUROPOLE)

** Electronics **
* Education: Engineering schools of INPG and UJF
  - ENSEEIHT
  - ENSERG
  - ENSIEG
  - ENSIMAG
  - ENSPG
  - ISTG

* Research Laboratories of CNRS, INPG, UJF
  - CSI
  - LEMO
  - LEPES
  - LMGP
  - LPCS
  - TIMA

* Infrastructures for research and education
  - CIME
  - CMP

* Applied research LETI, a division of the French Atomic Energy Commission (CEA)
  - CNET, a laboratory of France Telecom

* Industry SGS Thomson, Thomson TCS, SILMAG
  Thomson Electronic Tubes, Thomson Consumer Electronics, Thomson LCD, Merlin Gerin, ANACAD,
  AURIS, Dolphin Integration, SOFRADIR, RADIALL

** History **
43 b.c.: 1st mention of CULARO, a small town modestly built by the Celts to get across the Isère river, by Lucius Munatius Plancus in his correspondence to Cicero.
III century a. c. : Construction of the first rampart.

379 : Emperor Gratien promotes CULARO to the rank of chief town city and gives it its name : GRATIANOPOLIS.

VI century : Construction of a Christian funerary complex on the right bank of the Isère river.

1012 : The Saint-Laurent group (right bank) is given to the benedictine monks of Saint Chaffre en Velay : founding of the Saint-Laurent priory and then, the development of a suburb.

c.1140 : Rebuilding of the cathedral and its cloister.

1219 : Flood ; the bridge is taken away.

1228 : Construction of the Collegiate Church Saint André : the "Dauphins" set up their administration at Grenoble.

1339 : Creation of a University in Grenoble, including four sections : medicine, liberal arts (sciences and literature), canon law and civic law.

1391 - 1418 : Construction of the Island Tower, first Town Hall.

1453 : The setting up of the parliament of Grenoble : the town is officially recognised as a regional capital.

1593 - 1606 : Construction of the wall of Lesdiguières.

1709 : Birth of Jacques DE VAUCANSON, biomechanist. His automata (Le Joueur de Flûte, 1738) were aimed at "reproducing means in view to obtain the experimental intelligence of a biological mechanism".

1712 : Birth of Joseph FOURIER, mathematician and prefect of Isère department. In 1811 Joseph FOURIER sets up the Faculty of Sciences. In 1987, the Scientific, Technologic and Medical University of Grenoble will take the name "Université Joseph FOURIER".

1783 : Birth of Henri BEYLE, so-called STENDHAL, novelist.

7 June 1783 : Day of the "Tuiles".

c. 1830 : Construction of the HAXO fortifications.
1869: Invention of the hydro-electric power, the "White Coal", by Aristide BERGES.


1955: Grenoble Nuclear Research Center (CENG).

1963: First laboratory integrated circuit at LETI.

1965: First industrial integrated circuit at SESCOSEM. First computer LAG/INPG-MORS.

1966: Laue Langevin Institute (ILL).


1970: Louis NEEL is Nobel Prize in Physics. Louis NEEL has been President of Institut National Polytechnique de Grenoble (formerly Institut Polytechnique de Grenoble), from 1954 to 1976; he is now Honorary President of INPG.


1985: Nobel Prize awarded to Klaus von Klitzing.

1986: European Synchrotron Radiation Facility (ESRF).

1988: Research Centre for the Army Health Services (CRSSA).

1994: The European Synchrotron Radiation Facility is available to research scientists from virtually all countries.
II – RESEARCH ACTIVITIES

II-1 Integrated Systems Design (ISD)

Group Leader: A. GUYOT
(e-mail: Alain.Guyot@imag.fr)

Members: S. ABOU-SAMRA, Z. APANOVICH,
A. BERNAL NORENA, V. COISSARD, A. GUYOT,
A. MARCHUK, V. TCHOUMATCHENKO,
T. VASSILEVA

Research areas:

The integrated system design group concentrates on two circuit design issues:
. fast, accurate and above all low power arithmetic,
. exploration of new technologies possibilities.

Contracts:

European: GARDEN (Human Capital and Mobility),
GRASS (Esprit III Working Group).
HIPERLOGIC (ESPRIT Reactive Long Term Research).

II-1.1 Low power GaAs digital circuits design methodology

Members: A. BERNAL A. GUYOT

II-1.1.1 Low power GaAs asynchronous applications

GaAs digital circuits have clearly a better power-delay performance than silicon circuits. However the power distribution is quite different from CMOS. In CMOS (Complementary MOSFET), roughly 90% of the power dissipation is dynamic (i.e. due to activity and parasitic capacitances) while in GaAs it is the other way around. Due on one hand to the use of standard Ratiocd Logic and on the other hand to the lack of insulator for the gate of MESFET, roughly 90% of the power is static (independent of the computational activity). Anyway in fast synchronous circuits, whether silicon or gallium arsenide, global clock distribution induces a considerable power dissipation as well as additional delays to compensate the clock skews.

An efficient way to avoid or reduce such troubles is asynchronous design. The absence of global clock signal alleviates timing considerations, eases design migration, provides an automatic adaptation to process parameters and temperature variation and finally gives an average-case

1 Novosibirsk Academy of Sciences, Russia
2 Technical University of Sofia, Bulgaria
instead of a worst case performance. To achieve low static power dissipation in asynchronous applications, two new approach of design called DC$^2$FL and EMDL have been introduced. In Figures II-1 1(a) and 1(b) the schematic of the two structures are shown. In Figures II-1 2(a) and 2(b) the schematic and final layout are shown.

![Figure II-1 1(a) - A DC$^2$FL gate](image1)

![Figure II-1 1(b) - Schematic of a EMDL gate](image2)

![Figure II-1 2 - Asynchronous adder](image3)

(a)  

(b)  

**II-1.1.2 Low-power GaAs static memory cell**

Recently, advances in high speed VLSI circuits and with the development of portable telecommunication and multimedia systems, which demand high clock frequency, GaAs digital circuits are considered as an attractive alternative. However low power dissipation is also mandatory. So, low power GaAs LSI technology is becoming an important area of electronics. In particular, GaAs SRAM is an area where considerable attention has been focused. Some, GaAs SRAM development has been focused on low power applications, especially with very low standby and data retention power. Some remarkable progress in power reduction, performance and temperature tolerance have been also obtained.

Currently, more emphasis has been placed on low-power, high-speed rather than large memory capacity, primarily led by cache applications in high speed microprocessors. Consequently, some of
the developments in GaAs MESFET static memories are focused on small size. Several high-speed on-line GaAs memories are being designed to be applied to high-speed GaAs microprocessors which use small amount of memory on-chip in order to exploit their high speed.

Figure II-1 3 - (a) Cell structure  (b) 1-KB RAM layout  (c) Test chip microphoto

A low power memory cell structure has been developed to implement static RAM in GaAs technology. The new cell present low power dissipation and high operating speed. By the improvement of the structure an address access time of 1ns with a cell power dissipation of 14 µA/cell has been obtained. The RAM operates at only supply voltage of 1V up to 2V. This RAM can be easily used in implementing high-speed cache memory systems with sub 2 ns on-line memories requirements.

The 1-KB RAM was designed and a test chip fabricated using Vitesse III - GaAs technology. The novel high-speed GaAs Two-Single Port static memory cell which allows significant power dissipation reduction by lowering both its operating voltage and leakage currents. High performance and operational margin over a reasonable temperature range are its principal features. The cell structure is presented in Figure II-1 3 (a). The final layout of 1 KB SRAM design which can be used in high speed systems with sub 2 ns on-line memory requirements is presented in Figure II-1 3 (b). In Figure II-1 3(c) a microphotograph of the test-chip is shown.

II-1.1.3 Low-power GaAs modular exponentiation

VLSI circuits that accelerate the encryption and decryption of messages using the RSA encryption technique and circuits capable of performing long word length modulo multiplication at very high speed attract much interest for cryptography applications. For that reason, designer who research to accelerate RSA cryptographic processing are looking the high speed advantages of Gallium Arsenide VLSI technology as an interesting field.

On the one hand, multiplication operation is the main and more frequently function to process hidden information, that means, encryption and decryption process require the exponentiation arithmetic function which is executed as repetitive multiplication. On the other hand, arithmetic operators exhibit in general a great activity and dissipate consequently a significant share of the power supplied to a circuit. Specifically, a multiplier dissipates much more power than an adder when activated due to its design or layout structure is not as regular as an adder.
Due to the ultimate performance of an integrated circuit can be substantially improved by using both compact architectures and full customised macrocells library for its design, particularly true for GaAs circuits where speed performance is critical, the goal of this work is to validate an architecture to execute the modular exponentiation and further to develop low power design GaAs strategies to be used in its design.

![Diagram](image)

**Figure II-1 4 - Basic cell of the modular multiplier**

Currently, an alternative and regular architecture for computing a modular multiplication based on Montgomery's algorithm, useful in performing the RSA Public Key Cryptosystems is being studied. Considering that the ultimate performance of an integrated circuit can be substantially improved by using optimised architectures, we looking for a regular layout structures to combine it with a new low power strategies. That optimisation aims at finding a suitable balance between speed, power consumption and silicon area.

In **Figure II-1 4** the basic cell of the modular multiplier (hardcore of the system) is presented. In **Figure II-1 5 (a)** the Data Path architecture for the modular multiplier is also presented. In order to validate the architecture and an experimental 12-bits modular multiplier prototype has been designed using AMS-CMOS 0.6 μm technology. The CMOS prototype will be used as a reference to evaluate the GaAs advantages. In **Figure II-1 5 (b)** the layout of the 12-bits modular multiplier is presented.

![Diagram](image)

**Figure II-1 5 - Practical Modular Multiplier (a) Data Path Architecture. (b) Hardware System**
II-1.2 3D SOI CMOS design methodology

Members: S.J. ABOU-SAMRA, P. A. AISI, J. ARWEILER, A. GUYOT, B. COURTOIS

II-1.2.1 Technology

In the framework of the ESPRIT IV project HIPERLOGIC a three dimensional SOI CMOS technology for low power - high performance applications is developed at the IMS (Institute for Microelectronics Stuttgart) in the group of Prof. Höflinger. It consists of two layers of transistors (Silicon On Insulator on Silicon On Insulator). This technology uses the symmetrical 0.1μm channel length T-Gate transistor (Figure II-1 6). The T-Gate transistors are produced with the lithography-independent Edge-Defined MOS technology (EDMOS). The basic idea of this lithography-independent nanometer silicon technology is the substitution of the lithography by suitable film deposition techniques. The features that are normally defined by lithography are now defined by the thickness of deposited films, thus allowing smaller and more accurately reproducible gate lengths.

![Image of a symmetrical n-channel T-Gate transistor](image)

Figure II-1 6 - Principle of a symmetrical n-channel T-Gate transistor

The NMOS transistors are fabricated in the first layer of SOI. The PMOS transistors are epitaxially overgrown locally from the drain of a NMOS transistor. Figure II-1 7 is a perspective view of a 3D inverter.

![Image of HIPERLOGIC structure](image)

Figure II-1 7 - HIPERLOGIC structure

The first and most straightforward advantage of the stacking of the PMOS over the NMOS transistors is the substantial gain in density. This leads to reduced interconnections length. In deep submicron technologies, the capacitance introduced by the interconnections becomes predominant comparing to the intrinsic device capacitance. This remark becomes even more relevant for SOI
technologies because intrinsic gate capacitance are smaller in SOI devices than in their bulk counterpart.

This type of three dimensional integration introduces additional constraints on the design rules preventing a gain of a factor two in density. The inter-layer connectivity scheme is illustrated on Figure II-1 8.

![Figure II-1 8 - 3D-SOI inter-layer connectivity](image)

The structure is formed by two layers of Silicon with a layer of polysilicon in-between and another one on the top. Two metal layers are then available for local and global interconnects. The Silicon layers are connected together by a Silicon plug since the upper layer is grown epitaxially departing from the lower one which serves as a seed crystal.

The first Silicon layer is also obtained by local epitaxy, and thus it can be easily grounded by using the bulk as a common ground plane. This saves the area usually devoted to the routing of GND.

There are two layers of polysilicon, one for each level of transistors. The poly-poly contact is a critical technological step, but from the design point of view, this contact is compulsory to achieve substantial gains in terms of density as far as static CMOS is concerned. Also, design methodologies are developed to take better advantage of this contact.

As compared to 2D technology, the additional design rules constraints are due to the intermediate silicon level: indeed, one must be aware of making Metal1 to Poly1 or N-Type Si contacts outside the P-Type Silicon island. The common ground plane is actually not constraining. On the contrary, this saves the routing of the ground metal lines.

**II-1.2.2 Tools and circuits**

A design kit for 3D integration is developed for CADENCE DFM II v.97a. It includes front-end and back-end full custom and standard cell capabilities. A 3D cell library is now available. Performance driven design styles prospections were carried out, and finally static CMOS was retained. Self-dual functions are used wherever possible, as these are very convenient to layout in 3D. Indeed, in a self-dual function, the N-type and the P-type transistors networks can be made identical thus allowing higher gains in 3D. A low power - high speed 16x16 bits multiplier has been designed (Figures II-1 9a and 9b) and simulated. The results are given in the table below. All results are given for a 2 Volts supply.

<table>
<thead>
<tr>
<th></th>
<th>2D SOI</th>
<th>3D SOI on SOI</th>
<th>Gain (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area (mm²)</strong></td>
<td>4.21</td>
<td>3.67</td>
<td>12.8</td>
</tr>
<tr>
<td><strong>Total capacitance (pF)</strong></td>
<td>262.7</td>
<td>188.0</td>
<td>28.4</td>
</tr>
<tr>
<td><strong>Delay (ns)</strong></td>
<td>12.3</td>
<td>9.6</td>
<td>21.9</td>
</tr>
<tr>
<td><strong>Energy/Operation (pJ)</strong></td>
<td>556</td>
<td>387</td>
<td>30.4</td>
</tr>
<tr>
<td><strong>Energy x Delay (pJ/MHz)</strong></td>
<td>6.8</td>
<td>3.7</td>
<td>45.6</td>
</tr>
</tbody>
</table>

**Multiplier results**
II-1.4 Delay and power modelling in arithmetic operation

Members: T. VASSILEVA, V. TCHOUUMATCHENKO, A. GUYOT

Fast arithmetic operators in microprocessors or ASIC circuits, specially in the field of digital signal processing, can not always rely on synthesis with standard cell libraries. The delay and power of non-standard logic can be up to two or three times smaller than the standard cell ones. On the other hand, standard cells delay and power dissipation are well characterised and largely independent of the application thus allowing an accurate performance prediction. This modelling is of course missing for non-standard logic.

The goal of this project is twofold. First provide and characterise models for cells dedicated to arithmetic operations, then optimise operators according to the models. The optimisation aims at finding a suitable balance between speed, power consumption and silicon area.

This project is a part of the Ph.D. thesis of Vassily TCHOUUMATCHENKO.

II-1.5 Design portability

Members: Z. APANOVICH, A. MARCHUK, A. GUYOT

The process of the component miniaturisation due to the technology evolution is very fast. Meanwhile, there exists a huge number of circuits which should be reproduced and reused for still a long time. Design rule scaling method cannot provide process migration, cannot take into consideration additional layers provided by new technologies and it does not work with advanced technologies due to non-linear scaling effects. There exist other methods of technology migration which are based on the recognition of specific fragments of mask layout and updating them by the functionally equivalent fragments in design rules of target technology. It can be done by:

- compaction
- mask layout regeneration starting from transistor level netlist
- mask layout regeneration starting from gate level netlist
- mask layout regeneration starting from macroblock level netlist.

Every method provides new level of flexibility in mask layout optimisation but all the regeneration algorithms are NP-hard by their nature. It results in degradation of the quality of target mask layout
II-1.2.3 Conclusion

TIMA is carrying on the development and support of the design kits for 3D integration. This is done in collaboration with the group of Prof. BAITINGER, at IPVR, Stuttgart. The critical thermal evaluation is conducted with V. SZEKELY / M. RENCZ, from TUB, Budapest. Thermal driven design constraints will be integrated in the design kits as additional design rules.

In TIMA, this project is part of the Ph.D. thesis of Sélim J. ABOU-SAMRA.

II-1.3 Operator for unlimited precision

Members : V. COISSARD, A. GUYOT

The computational speed of computers is expected to increase by a factor of 1000 during the present decade. This gives mathematicians the possibility to solve previously intractable problems. But as the number of arithmetic operations increases, so do the probability of potentially disastrous inaccurate results due to roundoff errors and cancellation with the traditional floating point standard (IEEE 754-85). As usual, the hardware limitation are compensated by enhanced precision software, but at the expense of very long execution time since they execute on totally inadapted arithmetic units.

This project aims to design a processor with an instruction set dedicated to the efficient execution of algorithms in exact arithmetic, that is with no rounding or truncation.

The processor is superscalar, with pipelined functional units dedicated to operations. Numbers are up to 2,048 bits organised as tables of 1 to 16 128-bit digits. Thanks to the use of redundant arithmetic allowing carry propagation free operations, each unit may yield a 128-bit digit result at every clock cycle at peak speed. Since data dependency check is performed at the digit level, the digit result can immediately be fed into another functional unit without waiting for computation completion or passing through the register bank. In 1996 the circuit has been simulated and completely described in VHDL. The processor implement the basic functions of a public domain software package developed by J.-L. ROCH. This circuit design is a part of Vincent COISSARD'S research toward a Ph.D.
with increase of problem size. A natural way to resolve this problem is to decompose full-chip mask layout into fragments of tractable size. This idea of full-chip mask layout decomposition was validated in conjunction with compaction and rerouting strategy of mask layout regeneration. The main steps of the full-chip mask layout transformations are as follows:

1. The decomposition program takes as input full-chip mask layout and extracts the fragments which should be transformed by means of compaction. The size of extracted fragments is controlled by the values of decomposition parameters.

2. Each extracted fragment is then processed by a symbolisation procedure. The resulting mask layout is generated by a compaction procedure which is controlled by constraints extracted during the symbolisation step.

3. The resulting mask layout is generated by a compaction procedure which is controlled by constraints extracted during the symbolisation step.

This strategy was implemented in DECOMP system. The architecture of the DECOMP system is shown at Fig. 26. Wide range of experiments on mask layout decomposition and regeneration has been conducted. For these purposes, all the internal data structures, generated by decomposition and symbolisation procedures were translated into Cadence formats. Block layout regeneration after symbolisation step was done with the Cadence Virtuoso compactor and rerouting was done with the Block Ensemble. All the experiments were made on a commercial 32-bit cryptographic chip of about 65 000 transistors created in the design rules of obsolete one-metal 2.0 technology. It was migrated to two-layer 0.7 ECPD technology.

The first group of experiments has shown that it is always possible to find parameters decomposing mask layout into fragments of tractable size. The difference in sizes of extracted blocks essentially varied and many tiny blocks were generated with small parameters value. See Table II-1. The procedure of hierarchical decomposition can overcome this problem.

<table>
<thead>
<tr>
<th>Parameter of decomposition</th>
<th>Number of blocks after decomposition</th>
<th>Size of the greatest block (nb. of transist.)</th>
<th>Size of the smallest block (nb of transist.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 000</td>
<td>10</td>
<td>15 000</td>
<td>100</td>
</tr>
<tr>
<td>2 000</td>
<td>21</td>
<td>7 500</td>
<td>30</td>
</tr>
<tr>
<td>1 500</td>
<td>37</td>
<td>7 500</td>
<td>20</td>
</tr>
<tr>
<td>400</td>
<td>411</td>
<td>5 000</td>
<td>20</td>
</tr>
<tr>
<td>100</td>
<td>2,250</td>
<td>3 000</td>
<td>10</td>
</tr>
</tbody>
</table>

Table II-1.1 Decomposition of full-chip mask layout

The second group of experiments was done in order to study the relation between the area of final mask layout and the number of extracted blocks. This group of experiments has shown that the area of final layout was getting larger when the number of extracted parts increased. See Table II-1.2. This fact shows the need of an optimising strategy in calculating the relative positions of blocks after symbolisation - compaction.

Original sizes of Block count2 (17 000 rectangles) in 2.0 Russian technology:
width = 590.0 height = 1320.0 area = 778 800

<table>
<thead>
<tr>
<th>Number of subblocks</th>
<th>width</th>
<th>height</th>
<th>area</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>187.5</td>
<td>751.3</td>
<td>140868.75</td>
</tr>
<tr>
<td>5</td>
<td>192.2</td>
<td>724.5</td>
<td>139248.90</td>
</tr>
<tr>
<td>1</td>
<td>183.7</td>
<td>676.1</td>
<td>124199.57</td>
</tr>
</tbody>
</table>

Table II-1.2 Block count2 sizes after decomposition, symbolisation, regeneration in 0.7 ECPD technology
Fig. II-11 - Architecture of the DECOMP system
II-2 MiCroSystems (MCS)

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*R. RIBAS,*  
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*D. VEYCHARD*

*Research areas :*

The research activities of this group address the following :

- the development of micromachining techniques compatible with microelectronics,
- CAD and CAT tools for Microsystems,
- the design of safety critical and highly reliable microsystems, particularly operating in harsh environment.

*Contracts :*

European : BARMINT (ESPRIT-III Basic Research), THERMINIC (COPERNICUS), IMPRESSIVE (FUSE), MIPEG (FUSE)

National : Programme Microsystèmes du CNRS

Memberships : NEXUS, NETPACK, ADEMIS

*Industrial Partners :*

AMS (Austria), BEVERLY (France), MENTOR GRAPHICS (USA), SEMILAB (Hungary), SODERN (France), SCHNEIDER ELECTRIC (France), PML (France).

*Topics :*

One of the main obstacles to start with microsystems is the fact that particular, and hence costly processes are needed. In order to get affordable prices and a high flexibility, microsystems should whenever possible be designed in such a way that they can be realised on existing production lines for micro-electronics, with an additional post-processing for micro-system specific 2D and 3D structures, e.g. through Multi-Project-Wafer services. Furthermore, this approach allows to integrate microelectronics, needed in most microsystems, on the same chip. This is the monolithic solution which should be considered as the normal evolution of ASIC-foundries to microsystem-foundries (foundries strategy).

What is happening today with microsystems can be compared with the VLSI evolution during the early 80s, at the time of MEAD-CONWAY. Design rules easy to understand, basic CAD like MAGIC in the US and LUCIE in France, MOSIS in the US and CMP in France, have permitted

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1 Visiting Engineer from Beverly, France
2 UFRGS, Porto Alegre, Brazil
3 Technical University of Budapest, Hungary
non-specialists to get acquainted with VLSI. The difference between VLSI in the 80s and Microsystems today is that CAD for Microsystems must not be developed from scratch, but should be built on existing CAD systems. On fabrication, the manufacturing should be built on existing microelectronics manufacturing facilities to take advantage of the existing massive investments.

The MCS group within TIMA Laboratory is involved in the development of manufacturing techniques and CAD tools by the wish to make microsystems accessible to non-specialized institutions. In addition, the MCS group answers to the needs of the industry in the design of microsystems for safety critical and harsh environment applications targeting mainly, medical, aerospace and high temperature domains. The MCS group collaborates extensively with both industry, research laboratories and universities, and it put emphasis on the ability to work on medium term industrial projects.

II-2.1 Microelectronics compatible manufacturing techniques of Microsystems

Members: J. M. KARAM, R. RIBAS, D. VEYCHARD

There are two ways to manufacture microsystems: to develop processes specific to microsystems (hence these processes can address requirements specific to microsystems) or to use processes that have been developed for microelectronics. Among those later processes, some can be targeted to microsystems, again to address specific requirements, or it is possible to add special process steps to accommodate microsystems within integrated circuits. This later way will allow to collectively fabricate microsystems including the microelectronics part at a low-cost. This is the way addressed by the MCS group within TIMA.

II-2.1.1 Silicon compatible micromachining

The fabrication of silicon compatible micromechanical structures involves the deposition, doping of the necessary material and the selective etching of the underlying support. Two main methods can be used: bulk micromachining where structures are etched in the substrate, and surface micromachining where the micromechanical layers are formed from layers deposited on the surface.

Some advantages of these micromachining techniques include VLSI integration, low cost and rapid delivery.

Bulk micromachining is a process based on etching wells in the silicon substrate, leaving suspended structures. Using this micromachining technique, devices such as micro-hotplates, infrared sources, thermal flat-panel displays, CMOS thermopiles, thermal converters, gas flow sensors, channels for fibres, and piezoresistive sensors can be developed. In bulk micromachining two techniques can be used: etching from the front-side or etching from the back side.

Works at the MCS group address mostly front-side bulk micromachining. In the back-side bulk micromachining the structures are usually large and alignment is difficult. If the bulk micromachining is performed from the front-side this alignment problem is immediately removed and dimensions can be reduced. The end result after CMOS fabrication is an open in the dioxide and nitride mixture passivation that exposes the bulk silicon surface. These chips are placed into an anisotropic etchant, such as EDP (ethylenediamine-pyrocatechol-water) or TMAH (tetramethylammonium hydroxide) or KOH (potassium hydroxide), and the exposed silicon is anisotropically etched.

After the 1.0μ CMOS (SLP / DLM, from ES2) and the 1.2μ CMOS (DLP/DLM, from AMS) bulk micromachined technologies, the 0.8μ CMOS compatible front-side bulk micromachining has been fully validated. The design rules have been established, and implemented in CAD environment. These technologies have been transferred to the CMP Service, where Multi-Project-Wafer runs
regrouping accelerometers, IR detectors, electro-thermal converters, micro-mirrors, pellistors, gas flow sensors, etc., can be manufactured. Figure II-2 1 shows structures manufactured using the latest technology.

![Image](image_url)

**Figure II-2 1 – Suspended membrane manufactured using 0.8μ CMOS (from AMS) compatible front-side bulk micromachining**

Surface micromachining is based on the deposition of thin films on the surface of the wafer and removing one or more of these layers to release the structures. So a surface micromachining process requires a sacrificial layer which is removed at a later stage (in the post-processing operation) to release the mechanical part. Many materials are used as a sacrificial layer, such as: silicon oxide, polysilicon, porous silicon, aluminum, etc., each requiring a specific etchant. Usually, silicon dioxide sacrificial layers are the most used and are removed by wet etching in HF. There are various types of oxide (Thermal, LPCVD [LTO, PSG, BPSG], PECVD) having each advantages and disadvantages in terms of quality, etch rate, thickness uniformity, etc. The micromechanical layer is normally polysilicon, metals or nitride. In our investigations towards CMOS compatible front-side bulk micromachining, we studied the case of mechanical structures composed from silicon dioxide and metal 2, where a layer of 0.6μ of metal 1 has been etched (sacrificial layer). This technique showed the most promising results. Figure II-2 2 shows a cantilever array realized by surface micromachining after metal etching.

**II-2.1.2 Gallium arsenide micromachining**

In the last two years, the feasibility of front-side bulk micromachining by using GaAs microelectronic technologies has been demonstrated. The open areas to be micromachined, when placed appropriately on the die, allow to fabricate 3D microstructures such as bridges, cantilevers and membranes via additional post-process wet etching respecting the total integrity of the other parts of the die (electronics, passivation).

The latest research works in this field targeted the characterization of several wet etchants in terms of etch rates, selective and preferential etching characteristics in order to produce three kinds of free-standing structures, specifically:

1. GaAs/AlGaAs mesa-shaped structure,
2. triangular GaAs prism-shaped structure and
3. suspended metal/oxide or nitride structure without GaAs material.

Each of these structures is suitable for a specific application and need a specific etching solution to be realized.
II-2.2 CAD and CAT tools for MEMS


Starting from the 70s, Microelectronics development has been made possible because of the use of CAD tools and because of the availability of foundries for Education/Research and for fabless companies, besides large IC manufacturers. Without such similar boosters, Microsystems might easily remain curiosities, top level prototypes manufactured by researchers, but they would not become industrial products.

Long ago, Education and Research in Microelectronics had taken advantage of CAD tools developed in USA and in France: MAGIC in Berkeley, LUCIE in Grenoble. These tools were provided free of charge. Later, most Universities have been provided with commercial CAD tools. Considering the background on CAD for Microelectronics, a few principles should govern the development of CAD for Microsystems :

- CAD for Microsystems should not be fully designed from scratch, but modules available for Microelectronics should be reused when existing ;
• a CAD for Microsystems should look familiar to a user of CAD for Microelectronics;
• the "system" user should be distinguished from the "library" designer;
• but the challenge is to put together a framework where the "library" designer will find tools he has been using for years, besides the tools used by the "system" user.

Also, the ongoing Intellectual Property (IP) issue on electronic cores (business models, alliances like the Virtual Socket Interface) will soon emerge as an (maybe even more acute) microsystem cores IP issue.

II-2.2.1 An integrated microsystem design environment

An integrated framework should allow both the system-level designers and the device designers to work together. The framework should contain elements for the device designer, enabling him to design modules, to simulate them, and finally to put the knowledge in the form of characterised standard cells in a library. The system level user takes profit of this standard cell library that contains multi-level information: (e.g. layout information, behavioural models, FEM-models). He assembles the desired cells, and simulates them at system level. Then, the resulting assembly is handed over to a second set of tools, designed for chip level procedures. Once the final layout is produced, both the system level designer and the device level designer can intervene again to check the features of the resulting microsystem. The Figure II-2.4 shows the global CAD principle.

This duality can be compared to what happened to Microelectronics over the years. From full custom design style, IC design moved to standard cell design, improving the productivity. Today, there are even CAD vendors specializing in providing libraries, to be used in various frameworks. Some manufacturers are even giving up the design of libraries for their processes, relying on these specialized CAD vendors. Microsystem libraries will similarly boost the productivity in designing microsystems. The comparison may even go further. In view of speeding up further the design cycle, sophisticated library cells, called cores, are the central part of an IP business based on reuse. More and more, such cores will be produced by a company, and used by another one. It may be predicted that sooner or later, a kind of Virtual Socket Interface (VSI) will exist for microsystem modules. However the IP issues, being discussed presently for ICs, might be even more acute, since there is probably more IP in a microsystem core than in an IC core.

![Figure II-2.4 – Microsystem CAD structure](image)

Such an integrated framework as depicted in Figure II-2.4 should consider both monolithic and hybrid microsystems. Monolithic microsystems are those where electronic and non-electronic function are co-fabricated. Hybrid microsystems are those where various components are manufactured separately and packaged together.
II-2.2.2 MEMS engineering kit

Similarly to design kits existing to link a CAD framework to a specific process for IC design, a Microsystems Engineering Kit has been defined. The Kit allows a continuous design flow enabling the generation of a schematic driven layout. It includes an extended schematic editor allowing the generation of an extended netlist, an extended DRC and an extended parameter extractor (from the layout level to netlist level) distinguishing electronic and non-electronic parts. An application oriented behavioural simulation can be achieved by

the means of a comprehensive set of HDL-A microsystem library elements (pressure sensors, accelerometers, IR detectors, electro-thermal converters, ISFET, etc.). The schematic driven layout feature is achieved by the means of technology dependent generators for structures, such as bridges, cantilevers, membrane or application oriented structures.

Currently, both CMOS and GaAs compatible bulk micromachining technologies are supported by the kit. The extension to other microsystem technologies is achieved on a custom demand basis. The kit includes an extended design rules checker, a parametrized cell library and a cross-section viewer.

II-2.2.3 MEMS library

The straightforward advances within the latest developments of the mainstream semiconductor industry is the use of already available intellectual property (IP) in the development of systems optimally matched to the end product specifications. The MEMS engineering kit presented above offers an integrated solution allowing a continuous design flow from front-end to back-end. The end objective is to bring to the system level designer, a complete design flow, down to the chip level, anchored on design re-use and reliable system-level simulation, thus leveraging standard IP products for the realization of sophisticated miniature systems, at low cost.

![Figure II-2 5 - Example of MEMS DRC execution](image1)

![Figure II-2 6 - GaAs based IR sensor generator](image2)

The MCS group developed a comprehensive set of MEMS HDL-A library elements. This library includes IR sensors, electro-thermal converters, temperature sensors, accelerometers, humidity sensor, etc. Figure II-2 7 shows an HDL-A model of an accelerometer encapsulated within the Mentor Graphics environment.
II-2.2.4 MEMS testing

Miniaturization, in conjunction with an ability for mixed integration with electronic circuits, are key factors for the success of microsystem technologies. Monolithic systems which combine in a single chip signal processing circuitry with sensors or actuators result in lower manufacturing costs and, most often, in enhanced performance by improving, for example, on signal-to-noise ratio. However, higher integration levels always raise major test concerns which hamper the progress towards developing low cost highly integrated products. In fact, testing and packaging costs for micro electro mechanical devices (MEMS) can already amount for as much as 75% of the total cost. As a consequence, research into adequate ways of testing mixed-domain monolithic systems is now starting.

The goal of this activity is to address MEMS testing issues. Initially, micromachined electromechanical systems realized using CMOS-compatible technologies are considered. These technologies are chosen since they are mature and stable, and most pressure sensors and accelerometers in the market rely on them. They use silicon to implement both electronic and mechanical components by means of a CMOS process-flow followed by a micromachining post-process which allows creation and thermal isolation of suspended mechanical parts. This post-process, most normally bulk or surface micromachining, is compatible with CMOS fabrication processes, and results in microstructures such as membranes, cavities, masses and bridges which are basic microsystem design cells.

An implementation of silicon-compatible microsystems often consists of two sub-systems: an actual gauge and a microstructure which suspends the gauge. Figure 8 shows the most typical gauges which interface with the electrical domain. Gauges can be either passive, when they experiment an impedance change under the effect of a physical magnitude under measurement (e.g. temperature, stress or movement), or active when they generate an output electrical voltage or current (e.g. Seebeck effect). These physical effects are modeled as a function of gauge geometry
(parameters L, W, t, and d) and material properties such as resistivity, permittivity, and Seebeck coefficient.

\[ R = \rho \frac{L}{Wt} \]

\[ \Delta \rho = \pi l \sigma l \]

\[ \frac{\partial C}{\partial z} = \frac{\pi r W}{d} \frac{\partial h}{\partial z} \]

\[ \rho = \rho_0 (1 + TCR(T - T_0)) \]

(a) Resistance  
(b) Piezoresistivity  
(c) Capacitance

\[ V_a = \alpha_a (T_{hot} - T_{cold}) = \alpha_a \Delta T \]

\[ V_b = \alpha_b \Delta T \]

\[ V = (\alpha_a - \alpha_b) \Delta T = \alpha_{ab} \Delta T \]

(d) Seebeck effect

**Figure II-2.8 - Typical gauge principles used for CMOS-compatible microsystems**

Fault classes and failure mechanisms for CMOS-compatible microsystems have been studied. After identifying material and structural parameters which are involved in design and implementation of these parts, a classification of faults has been produced according to the parts and parameters affected. As shown in Table II-2.1, a classification of faults as catastrophic, for which electrical, mechanical or thermal misfunction prevents any system utilization, and parametric, for which changes on geometrical or material parameters alter system performance, results. This classification resembles that commonly used for analog and mixed-signal circuits.

<table>
<thead>
<tr>
<th>GAUGE FAULTS</th>
<th>MICROSTRUCTURE FAULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A. CATASTROPHIC</strong></td>
<td><strong>BREAK</strong></td>
</tr>
<tr>
<td>SHORT FAULTS</td>
<td>break outside gauge</td>
</tr>
<tr>
<td>in one polysilicon level</td>
<td>break around gauge</td>
</tr>
<tr>
<td>between both polysilicon levels</td>
<td>break including gauge fracture</td>
</tr>
<tr>
<td>between poly and metal</td>
<td><strong>STICION</strong></td>
</tr>
<tr>
<td>on one metal level</td>
<td>NON-RELEASED MICROSTRUCTURE</td>
</tr>
<tr>
<td>between both metal levels</td>
<td>ASYMMETRICAL MICROSTRUCTURE</td>
</tr>
<tr>
<td><strong>OPEN FAULTS</strong></td>
<td>thermal asymmetry</td>
</tr>
<tr>
<td>in polysilicon level</td>
<td>mechanical asymmetry</td>
</tr>
<tr>
<td>in metal level</td>
<td></td>
</tr>
<tr>
<td>in poly-metal contact</td>
<td></td>
</tr>
<tr>
<td><strong>B. PARAMETERI</strong></td>
<td><strong>STRUCTURAL</strong></td>
</tr>
<tr>
<td>WIDTH</td>
<td>width</td>
</tr>
<tr>
<td>LENGTH</td>
<td>length</td>
</tr>
<tr>
<td>THICKNESS</td>
<td>thickness</td>
</tr>
<tr>
<td>MATERIAL</td>
<td><strong>MECHANICAL</strong></td>
</tr>
<tr>
<td>polysilicon resistivity</td>
<td>mass density</td>
</tr>
<tr>
<td>metal resistivity</td>
<td>distance microstructure-bulk</td>
</tr>
<tr>
<td>contact resistivity</td>
<td>Young modulus</td>
</tr>
<tr>
<td>TCR coefficient poly</td>
<td><strong>THERMAL</strong></td>
</tr>
<tr>
<td>TCR coefficient metal</td>
<td>thermal conductivity</td>
</tr>
<tr>
<td>piezoresistive coefficient</td>
<td>encapsulation distance</td>
</tr>
<tr>
<td>Seebeck coefficient poly</td>
<td>beam emittance</td>
</tr>
<tr>
<td>Seebeck coefficient metal</td>
<td></td>
</tr>
<tr>
<td>permittivity</td>
<td></td>
</tr>
</tbody>
</table>

**Table II-2.1. Fault classes for CMOS-compatible microsystems**
Failure mechanisms or defects occurring at process-level have been linked to the fault classes above described. Defects occurring during the CMOS process-flow are distinguished from defects occurring during micromachining. Some of these realistic failure mechanisms have been observed in microsystem test structures fabricated via the CMP service using a double-metal double-poly CMOS process-flow followed by silicon bulk micromachining. Figure II-2.9 gives an example of a typical break in a microstructure bridge.

Figure II-2.9 - Break in a bridge-type microstructure

A common fault modelling and fault simulation environment based on the hardware description language HDL-A is used in this work. For fault analysis, HDL-A mutants and saboteurs are simulated using the mixed-mode simulator ELD0. Tools for pre- and post-processing are still needed in this environment in order to achieve automatic fault injection, fault dropping, the translation of non-electrical into electrical input stimuli (in the case of microsensors) and the translation of electrical into non-electrical outputs (in the case of microactuators). Figure II-2.10 summarizes the main features of the fault simulation tool used in this work.

The process of searching input stimuli that activate and propagate faults to microstructures measuring points is assisted in this work by the ELD0-based fault simulation tool. The test generation procedure is based on a sensitivity-guided search process. Sensitivity figures are obtained by simulating the good and the faulty circuits for the given stimulus of the input range of interest. Mechanisms for properly propagating constraints from the microstructures test generation tool to the analogue (and eventually to the digital) test generator(s) need to be created.

Even though a test generation tool is made available for microsystems testing, hard-to-detect faults can prevent that a good tradeoff between fault coverage and testing time is achieved. In these cases, the first idea is to choose an embedded layout line as test point in order to make it fully controllable and observable, thus enhancing the testability of the whole system. This choice is made based on defect-oriented experiments assisted by the fault simulator. The second idea goes further into design for test, building into microsystems self-test capabilities. On-chip test response analysis is to be achieved in the case of microsensors, while the concern in the case of microactuators is the on-chip test generation. The primary goal is to design microsensors and microactuators that can be checked by the same circuitry already available for testing the microsystem electrical (analogue and digital) parts. The oscillation, current and thermal testing techniques have been reused in our microsystems testing environment.

To conclude, the results expected in the near future from the on-going developments briefly discussed above should make it possible to:

- put in phase microelectronics and micromechanics testing, by bridging the gap between defects and fault modelling in non-electrical elements;
- define a CAT platform allowing to jointly simulate realistic faults and generate tests for both electronic (digital and analogue) and micro-mechanical devices, and implement this platform by integrating commercial and university CAD through glue tools for fault injection, fault dropping, etc;
- propose structures for design for testability and built-in self-test of electrical and non-electrical Microsystem components, based on the testing requirements derived from the defect-oriented experiments with fault modelling, fault simulation and test signal generation.

II-2.3 Microsystem design for safety critical applications and harsh environment


Microsystems technology is having a large impact in a wide range of applications mostly safety critical, like in medical, automotive and aerospace domains. The next generations of microsystems will integrate test strategies and diagnostic functions. In addition to these applications, the MCS group addresses the design of microsystems operating in harsh environment (radiations, high temperature, biocompatibility, etc.).

II-2.3.1 Design of the BARMINT Multi-Sensor Chip – Medical Applications

The BARMINT microsystem consists of several different silicon substrates, forming together a so-called vertically stacked Multi Chip Module (MCM-V). In each substrate one or more different functions is implemented. The distribution of the various functions among the different substrates greatly affects the design of the electrical architecture of the microsystem.

The MCM-V (MultiChip Module, Vertically stacked) concept is a technique that offers the possibility to integrate different kinds of chips, using different kind of technologies, into a single package. Using this technology, the BARMINT medical demonstrator can be divided into subsystems. Each subsystem consists of devices that can be produced with the same technology, so
for subsystems a monolithic approach can be used. According to this principle, the BARMINT microsystem can be divided into the following subsystems:

- micropump module, consisting of a thermopneumatic micropump,
- sensor module, containing different types of microsensors,
- module containing fluid tanks,
- VLSI module for signal processing and external communication,
- module of mechanical tests,
- module of thermal tests,
- power supply module.

Within this project, in addition to the CAD task leadership, the MCS group has performed the design of the BARMINT medical demonstrator sensor interface module. This module is located at the bottom of the fluid measurement chamber and includes:

- three piezoresistive pressure sensors,
- three temperature sensors,
- two ion-sensitive field effect transistors (ISFET) for the measurement of chemical activity of the ion species in the fluid.

These sensors are manufactured monolithically with their electronic interface in CMOS compatible bulk micromachining technology in cooperation with CNM. The sensor module chip is divided into three regions by an isolating rim as shown in Figure II-2 11. The different sensors are inside the rim in contact with the pumped fluid. The other two regions are outside the isolating rim and are used to implement the signal conditioning circuitry.

![Figure II-2 11 - Top view o the sensor module layout chip](image)

A differential ISFET measurement configuration has been applied to reduce effectively the temperature dependency as well as common noise compensation. Its consists of two source-and-drain follower circuits and a voltage-to-current converter with a differential input. The reference electrode is grounded since a sample solution can be conductive and the metallic parts of the BARMINT microsystem are also grounded.

The piezoresistive pressure sensors have a Wheatstone bridge configuration. Their interfaces have been kept simple and consist of a V-I converter and a stable bias voltage.
The design of the temperature sensor with current output has been carried out at TUB-DED. The BARMINT sensor module chip will thus provide a common current output from all interfacing circuitry. A multiplexing logic will select the actual sensor interface and its analog signal read by an address decoder.

**Figure II-2 12** shows a SEM of the BARMINT sensor module.

![The BARMINT sensor module](image)

**Figure II-2 12 - The BARMINT sensor module**

### II-2.3.2. Rad-hard read-out electronics for a thermal imaging device – Aerospace applications

The aim of this activity is to develop the read-out electronics for a thermal imaging device, which will be part of the attitude control platform of a satellite. The sensing element is based on a linear array of thermal detectors, organized as individually addressable pixels. The output signal from each one of these pixels must be measured with a precision of 100mV, over the expected lifetime of the satellite (15 years). This is a difficult problem, considering the hostile environment, subject to large temperature variations and radiation exposure. Our on-going research effort focuses on the development of circuit and layout techniques to limit the degradation caused by ionizing radiation (up to 100Krad) to acceptable levels, using standard bulk CMOS technology. The immunity to SEE's (single event effects) has also been assessed, and circumvention techniques have been implemented. The read-out electronics of the thermal imaging system has been designed and fabricated on both standard CMOS (from AMS) as well as radiation hardened (DMILL) technologies. **Figures II-2 13 and II-2 14** show the chips in both technologies.

The development of the rad-hard circuitry is being carried out under contract with SODERN. The qualifications for total dose and latch-up of the read-out electronics in standard CMOS technology has been successfully carried out. The immunity to radiation exceeds 200 Krad in total dose with similar behaviour for latch-up.

Ultimately, the objective is to develop a single chip integrating the detector structures (produced by front-side bulk micro-machining) and the read-out circuitry, for space qualification.
II-2.3.3 CMOS compatible temperature sensor using lateral bipolar transistor for very wide temperature range applications

The P-N diode present in the bipolar transistor emitter-base structure has a temperature dependency that can be exploited to produce a voltage that is proportional to temperature.

The combination of two such voltages yields a voltage proportional to the absolute temperature voltage (PTAT). With an optimized design and careful layout, the sensing devices and the interface circuitry can be monolithically integrated, minimizing other unwanted temperature effects, and the output voltage will be a highly accurate representation of the temperature over a wide range.

The main qualification criteria of a temperature sensor are: accuracy versus temperature, linearity, sensitivity, temperature range, output signal level, absolute calibration and low cost. In this paper, we will present a temperature sensor based on the parasitic bipolar transistor available in CMOS technologies, specifically the CMOS Lateral Bipolar Transistor (CLBT). The other possibility of implementing bipolar transistors is the CMOS Vertical Bipolar Transistor, using the substrate as a collector, a separate well as the base and a diffusion as the emitter, where applications are strictly limited to common collector configurations. Since for the temperature sensor application, it is absolutely necessary to accurately control collector currents, common collector configurations and CVBTs cannot be used.

The sensor consists of two current source generators, $I_{PTAT}$ and $I_{be}$ that are combined in order to obtain a current source intrinsically referenced to the desired temperature range. It has been designed and fabricated using 0.8μ CMOS technology (from AMS foundry). Figure II-2.15 shows the sensor chip.
Figure II-2 15 - The temperature sensor with test structures

The first measurement results obtained from one tested device show a good functionality from -55°C to 177°C. The most important measured characteristics are shown in Table II-2 2.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Current mode</th>
<th>Voltage mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output swing</td>
<td>13 to 91 μA</td>
<td>0.4 to 3.5 volts</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>0.333 - 0.335 μA/°C</td>
<td>12.6 - 12.8 mV/°C</td>
</tr>
<tr>
<td>Accuracy</td>
<td>0.08 - 0.2%/FS rms</td>
<td>0.57 - 1%/FS rms</td>
</tr>
<tr>
<td>Max. Temp. range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current consumption</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply level</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table II-2 2 - Measured performances of the temperature sensor

Figure II-2 16 shows that a better performance was obtained in current mode than in voltage mode, according to the already described Poly-Si resistor temperature coefficient influence in the output current.

Figure II-2 16 - Temperature error characteristics in voltage and current modes
II-2.3.4 CMOS compatible infra red sensor array

Based on self-generating Seebeck effect, thermoelectric IR sensors offer many advantages, among others:

- no biasing is needed since no temperature difference produces zero offset output voltage,
- no cooler is required since the reference temperature (the temperature of the "cold" junctions of thermocouples) is equal to environmental temperature, or the temperature of silicon substrate of thermopile,
- no offset drift,
- the thermopile does not suffer any interference from any chemical or physical signal except those which can generate the temperature difference between the "hot" and "cold" junctions of the thermopile, and light, which can easily be shielded (photoelectric effect).

The fabrication process of integrated IR sensor thermopile arrays is almost fully compatible with the standard CMOS process. Only one post-processing step is needed to form the suspended structures which is supporting the "hot" junctions of thermocouples.

Different structures can be used to support the thermopiles, particularly, bridges, cantilevers and membranes. The bridge structure is the most appropriate for its rigidity and robustness. The thermocouples materials are polysilicon (n or p and p) and aluminum available in the CMOS process. The maximum number of thermocouples is function of the design rules of the used technology fixing the minimal polysilicon strip width and distance between two adjacent strips. The main reason of making the thermopile leads as thin as possible is to minimize the thermal conductance of the structure. In the other hand, when decreasing the thermal conductance, the electrical conductance also decreases and the total ohmic resistance of the thermopile increases. A compromise should be found between these two parameters.

Figure II-2 17 shows an array of IR sensors designed by the MCS group. The bridge has 167 \( \mu \)m width and 1 mm length. It comprises 40 polysilicon / aluminum thermocouples having -63.3 \( \mu \)V/°K as Seebeck coefficient. The measured time constant in the air is 8 ms. The output impedance of one sensor is 136 KΩ. Figure II-2 18 gives the response of one sensor for an IR diode with 150 mA current at 1 cm distance from the surface of the sensor. The measured output is 22 mV after amplification with a gain of 26.

The next generation will use n-polysilicon / p-polysilicon for thermocouples which will increase the Seebeck coefficient to nearly 200 \( \mu \)V/°K.

![Figure II-2 17 - CMOS compatible IR sensor array](image1)

![Figure II-2 18 - Sensor response for an IR incidence](image2)
II-2.3.5 Electro-thermal converter

In cooperation with Schneider Electric, the MCS group evaluated a solution based on an electro-thermal MEMS device which measures the power of a current within an electrical line. The associated time constant should be very large.

In order to reduce the costs and increase the reliability, the MEMS device has been realized monolithically with the electronics.

In order to achieve the specifications, different structures have been modeled and fabricated. The modeling procedure targeted the mechanical as well as the electro-thermal behavior. Different packaging solutions have been investigated and the final prototype has been sent to fabrication.

II-2.3.6 Integration of a miniaturized pressure sensor in a ventricular shunt

In case of bad regulation of Intra-Ventricular Pressure (IVP), the surgeon may implant into the patient's head a valve which shunts the CerebroSpinal Fluid (CSF). Those valves aim to avoid over or under pressure of brain tissues. Many dramatic post-surgical accidents happen when valves, for instance cannot deal with dynamical movements from lying to supine positions. Differential valves control the CSF flow rate as a function of ventricular-peritoneal pressure; peritoneal pressure is highly variable. Unlike other valves, the referential Beverly valve, considered in this project, controls the CSF flow rate as a function ventricular pressure referenced to atmospheric pressure. This pressure is therefore a direct significant measure of IVP.

In this project a microsystem containing a pressure sensor and its read-out electronics will be introduced into the valve. The IVP measurement data will be sent to an external receiver via electromagnetic coupling. By the same way, the device will be power supplied using internal and external coils. Such a system will provide a continuous real time recording of IVP. The surgeon will thus have an objective information on the valve functioning and on critical conditions in which the patient may suffer clinical problems. This device will be useful for both post-surgical clinical diagnosis and further understanding of IVP daily variations and also CRL secretion rhythm.

This project is being carried in cooperation with BEVERLY SA.

II-2.3.7 Design for thermal testability

This activity is pursued in cooperation with the Technical University of Budapest, Department of Electronic devices.
On-line temperature monitoring of safety-critical ICs and systems becomes more and more crucial because of downsizing of integrated circuits and of increased density due to advanced packaging. To prevent erroneous operation temperature sensors should be placed on the critical spots, the outputs of which should be read by means of boundary scanned architectures or modified boundary scanned architectures in case of on-line monitoring.

The goal is to propose means to detect potential thermal problems, in special conjunction with on-line testing of safety-critical systems. For this purpose the idea of Design for Thermal Testability [DfTT] has been proposed. In DfTT circuits temperature sensors are realized inside the ICs besides the critical circuit elements, enabling on-line temperature checking of certain spots of the circuit. If the temperature of the monitored spots increases above a certain temperature limit, the system can take actions to interact, e.g. by decreasing the operating frequency, switching off temporarily parts of the circuits, etc.
Two issues must be addressed: the design of appropriate thermal sensors, and the way to integrate these sensors in circuits and boards, as a complement to other testability features. These thermal sensors can be applied in addition to current sensors, used for production testing (Iddq testing) and for on-line temperature monitoring of self-checking circuits. Similarly to current sensors, thermal sensors provide the following advantageous features:

- the manufacturer can carry out a thermal production testing, in order to find those chips which operate on higher temperatures than their normal operating temperature, this way discovering possible mounting defects, considerably increasing the overall reliability,

- continuous on-line testing is possible, when the system, parallel with system operation, observes the temperature of the components and interacts in case of danger.

An integrated microsensor for measuring temperatures can be produced in several different ways. The types of temperature sensors that are of interest for thermal testing purposes are:

- thermostats
- thermocouples
- transistors and diodes

All the three types can be fabricated with the technologies of an IC process. The selection of the best principle must be based on the achievable accuracy, complexity of the necessary signal processing, low power consumption, small physical dimension and small sensitivity to disturbances caused by other devices in the system.

Thermal sensors to be used for thermal monitoring of circuits and systems should meet special requirements:

- compatibility with the target process (without any additional fabrication steps),
- a reasonably low need of silicon area (equivalent to 10-20 simple gates),
- low power consumption (in the order of 1 mW or less),
- a temperature range of 0-120 (0-150)°C,
- favorably digital output signal (e.g. a square wave the frequency of which carries the temperature information).

On the other hand there are only moderate requirements in some parameters which are crucial in the case of sensors for general use:

- linearity (as the problem is usually whether the temperature exceeds a given margin or not),
- accuracy and long-term stability. In our opinion an incertitude of 1-2 °C is allowable regarding the fact that the temperature error margin is soft. When a margin of let us say 125 °C is declared we could not state that at 126 °C the device will be certainly destroyed while at 124 °C there is no danger. The margin always contains some "reserve of security" much bigger than 1-2 °C.

Comparing these requirements with the features of different temperature sensors, it can be stated that there are suitable solutions for thermal monitoring of CMOS digital VLSI circuits.

Having a digital (frequency) output thermal sensor, the boundary scan is the most suitable architecture to scan the internal temperature of several chips equipped with a thermal sensor. A counter of 12-14 bits length, some glue logic, an extension of the BSC instruction decoder and three additional instructions are the only extra needs to fulfill this goal. In the case a chip contains more temperature sensors, the multiplexing is needed. This multiplexing however can be also controlled via the boundary-scan path. This way the rough image of the chip's internal temperature distribution
(the thermal signature) can be grabbed which allows a more sophisticated evaluation of the thermal state than in case of a single data.

Various kinds of temperature sensors have been designed and tested. Implementation details must also be addressed for production testing or for on-line monitoring.

Production testing

In connection to production testing three basic issues need to be addressed: where to put the thermal sensors (placement strategies), how to read the temperatures (testing strategies) and how to evaluate the testing outputs (evaluation strategies).

Placement strategies

The designer has to make decisions about how to place the temperature sensors in order to reach the best fault detection properties while the area overhead is kept on a reasonably value. There is a choice of solutions referring to the different requirements. The typical approaches are:

(i) To use one temperature sensor per chip, not taking care to their internal (on-chip) position. The sensor can appear as an element of a standard cell library in this case. The placement will be made by the standard place/route tools, no special measures have to be devoted in order to include the sensor.

As a result of this the chip (the package) functions as a thermometer (beside its normal function). Wherever it is placed (in a packaged form on a PC board or as naked chip in a MCM) the temperature can be remotely measured in a pure electrical way. Overheating of the chip can be observed.

The weakness is that the measured temperature is only an average value for the chip. Suspicious alterations of the in-chip temperature distribution cannot be monitored. Possible hot areas of the chip cannot be diagnosed.

(ii) To use one temperature sensor but on a prescribed place. When the chip contains one power block (as in case of a smart power device) it is obvious to place the sensor to the expected hottest point of the chip (the middle of the power device area).

The design procedure requires manual steps in this case. The merits are the same as in case of (i) but with the further advantage that probably the hottest area of the chip is observed.

(iii) To use a number of sensors on the chip. In one hand some regular arrangements can be taken into account (sensor matrix of $2 \times 2$ or $4 \times 4$ cells). The other possibility is to match the arrangement with the chip’s structure by placing a sensor beside each circuit element or block having considerable dissipation.

In this case the design requires manual steps. The area overhead will be larger, but a rough image of the internal temperature distribution can be obtained. Such a temperature distribution is usually called a «thermal signature». This latter may serve as a test measure: the deviation from the nominal distribution may indicate some kind of defects which cause excess dissipation in some circuit blocks.
Testing strategies

The boundary scan is the most suitable architecture to scan several chips each equipped with a thermal sensor. In the case a chip includes several thermal sensors, then a multiplexing system is necessary. This way the «thermal signature» can be evaluated in the same way as other test vectors are evaluated. Such thermal sensors can be the companions of current sensors, often used for Idq production testing. Depending on specific applications, other kinds of sensors might be used the same way. It might also be devised a special device that would include several kinds of sensors, some being used for the actual application. The basic scheme would be as pictured in Figure II-2 19.

![Diagram](image)

**Figure II-2 19 - Boundary scan technique including thermal sensors, current sensors, etc. (not to scale !)**

Evaluation strategies

The first and most simple evaluation method is to observe whether the measured temperature exceeds the allowable one for the given device or not. The test system has to scan the temperature of all sensors and to compare them to the (individually determined) maximum ratings. Warning actions can be launched as well if a temperature although less than but nears rapidly to the limit. This can be done during burn-in for production testing, or even during on-line monitoring.

Evaluation of the thermal signature is a more complex task. It should be underlined that the thermal signature differs from the signature of the digital test procedures. The latter is a compressed test result having a unique bit-pattern for a defined input vector sequence while the thermal signature can be regarded as a result of the spatial sampling of an analog function.

Even in the case when only one sensor is inserted onto a chip, at the board level (or MCM level) a thermal signature can be obtained. The number of the measured temperature values is equal to the number of the IC packages on the board provided with temperature sensor.
On-line monitoring

The boundary scan architecture may also be used for on-line monitoring of the thermal sensors. In this case the thermal sensors become a detection mechanism as other on-line detection mechanisms, and the boundary scan needs to be extended to be used for on-line testing.

In order to check the outputs of the thermal sensors by means of \( B^2 \) UBIIST checkers, a dedicated circuitry which can on-line check the outputs of the thermal sensors without interfering with the concurrent check of other functional blocks is needed.

Each thermal sensor is to be provided with (self-checking) circuitry such that the outputs of the whole are encoded, usually in a double-rail code, exactly like a self-checking part would be. These outputs can then feed a (global) checker. Formally, these thermal sensors have to be self-exercising SCD, similarly to current sensors when used for on-line testing, but the design of such thermal sensors is still an open question. Other kinds of sensors may also be required for production testing. Such a global scheme is pictured in Figure II-2 20.

![Diagram](image)

**Figure II-2 20 - Self-Checking circuit with thermal sensors, current sensors, etc...**

Further work

Further developments are needed in order to complete the digital output temperature sensor with the self-exercising SCD capability for on-line monitoring. Another issue to be solved is the calibration of the sensors in this case and the storage of the (eventually individual) temperature margin of error detection.

Other questions to be solved are placement strategies (where to put the temperature sensors in order to reach the best fault detection properties), evaluation strategies (for a set of sensors), the identification of faults leading to temperature detectability, the evaluation of fault latency (time between fault occurrence and detection), etc.
II-3 Quality of Complex integrated Systems (QCS)

Group Leader : L. BALME
(e-mail : Louis.Balme@imag.fr)

Members : I. BACIVAROV1, L. BALME,
R. PISTORIUS, G. TKEBUCHAV2

Research areas :

The research activities of QCS group address the following:
. systemic analysis and modelling of the quality and the dependability of complex integrated systems.
. the development of computerized models including applications to electronics, computers, telecom and aerospace, systems.

Contracts :


Industrial Partners :

Hydroquebec (Canada), Yuasa (Japan).

Topics :

Because of the increasing complexity of today's industrial products, the design and manufacture of high quality products is becoming a crucial preoccupation of many companies in the world.

Complexity is the combined result of 4 different factors :

1/ The disappearance of traditional boundaries between technological fields such as mechanics, electronics, software and new materials. In a modern product, it is more and more difficult to identify subparts belonging exclusively to a specific technology.

2/ The interdependence of the sub-parts. The integrity of a product and therefore, its long term reliability, can be threatened by another product, much smaller, far less powerful, without any physical connection. This issue is particularly true for EMI/EMC for which an European Directive entitled "Electro-magnetic Compatibility and Interference" (89/336 EEC) was decided in 1989, with a transition period until the end of 1995.

As a result of this situation, the generally accepted law whereby, in order to make a total product of high quality, one only needs to make parts of high quality is no longer true.

1 - Visiting Professor from POLYTECHNICA UNIVERSITY, Bucharest, Romania
2 - Visiting Professor from Tbilisi State University, Georgia
3/ **The software integration.** In most of the today's products, in addition to managing the hardware, software has become an integral part of the product, with a fundamental difference compared with other technical sub-parts: software is a direct output of the human brain, with no intermediary transformation phases and with a very high risk of conceptual failure. Because writing software is a purely logical exercise, one could consider that there is nothing intrinsically uncertain about it. It is now demonstrated how the process of successive failures of a program can also be considered just as random as that of a hardware device, leading to the idea of a use of a probability-based reliability measure.

4/ **The human dependability.** Long term reliability is more and more often a parameter also dependent on the environmental use of the product. Nowadays products have to be considered as part of a more complex system, where the user himself and the environment of the product have a fundamental influence on its long term reliability.

QCS team within TIMA Laboratory is fully involved in the development of basic and applied research around the concept of quality of complex integrated systems, by:
- basic research: development of computerized models simulating and predicting the long term reliability of complex systems,
- applied research: development of applications in the area of Smart Power Card project.

II-3.1 **Smart power card**

*Topic leader: R. PISTORIUS*

*Members: I. BACIVAROV, L. BALME, R. PISTORIUS*

The majority of portable electronic products incorporate power-management circuitry, designed to operate from a few basic battery types (primary or secondary batteries). This is true for consumer electronics (pocket calculators, cameras and video cameras, walkman, cellular telephones, etc) as well as professional electronic products (wireless tools, note books etc.). As consequence of the incredible growth of the portable electronic market, especially for computing and telecommunications, an equivalent growth in battery demand has been generated.

Following to the sophistication of the associated electronics, new battery technologies have emerged to serve the high-volume markets. Today, only rechargeable batteries are used in high-volume applications due to their low weight and the long operating time. These batteries represent also for economy and ecological reasons a significant improvement in the battery development.

The "Accumulateur à Electrolyte Polymère tout solide" technology called ACEP is one of these new technologies. It was discovered by Dr. M. ARMAND from the *Laboratoire d'Ionique et d'Electrochimie du Solide de Grenoble*, a laboratory of INPG-CNRS. It gathers the thin film technology with highly energetic materials and thus allows to create a new generation of all solid miniaturized batteries. This invention opened great new possibilities in various sectors. Smart Power Card is one of these in the field of microelectronics.

Smart Power Card is a portable stand-alone power source device integrating an ACEP battery made of an all solid thin film of conducting polymer, and a control system which pilots battery status indicators and/or I/O data. The same control system can be used for the surveillance of an external device or equipment.
Figure II-3 1 - SPC internal architecture

Figure II-3 2 - SPC external layout
The Smart Power Card concept is protected by a French patent (Nr. 2672713) entitled "Composant d'alimentation du type carte de crédit" deposited in February 1991 and extended (PCT/FR 92/00124) to Europe, US, Japan, South Korea and Canada in co-ownership between INPG and ACEP Inc., a joint venture of HYDRO-QUEBEC (Canada) and YUASA (Japan), owning the exploitation rights of the ACEP battery technology. These events were followed by a world patent (Nr. WO 92/151 40) in 1992. At the end of 1995, the US patent (Nr. US 5 449 994) and the European patent (Nr. BE 0 524 304) were obtained.

The feasibility study on Smart Power Card was carried out during 1990, the building of a first prototype using PCB technology was finalized during 1992-1993. In line with the SPC architecture, a joint development between INTBL Corp. and DURACELL Inc. led to the specifications of the Smart Battery Data (SBD) and System Management Bus (SMB).

Depending on the microelectronic system powered, Smart Power Card brings innovative solutions to:

**II-3.1.1 Secondary batteries for consumer and professional electronics**

The battery technology advances from nickel cadmium (NiCd) to nickel metal hydride (NiMH), and lithium ion (Li-ion) to lithium polymer and zinc air. While NiMH batteries continue to gain market share at the expense of NiCd due to higher power density and environmental aspects, the growing availability of rechargeable Li-ion batteries is adding another variable to the equation. As Li-ion batteries offer greater volumetric and gravimetric power density than equivalent NiCd and NiMH batteries, they will be a solution to the needs of the consumer and professional electronics market that is expecting:

- a highly efficient battery: ACEP or similar Li-Ion batteries
- a physical standard format: the ISO smart card format with connecteur have been chosen for SPC,
- a reliable battery giving key informations to the user: charge level, real time consumption and life capital are the 3 parameters shown to the user on micro LCD in the Smart Power Card.

In line with these features, a new generation of Li-ion or NiMH smart batteries can be developed and integrated into the Smart Power Card resulting in micro and mini intelligent rechargeable batteries in the PCMCIA format as shown in the following figure.

![RIMBA: Rechargeable Intelligent Micro Battery](image)

Figure II-3 3 - RIMBA external layout
II-3.1.2 Multipurpose smart IC cards as defined by the ISO standards

The fast growing market of smart IC cards is expecting an integrated reliable power supply providing energy to IC cards while respecting ISO thickness (0.76 mm). The ACEP thin film technology applied in the Smart Power Card concept allows to integrate power supply on smart cards and thus opens great new fields of applications. In 1994 new progresses have been made concerning the application of the SPC concept, particularly in the management and the surveillance of complex integrated systems.

Furthermore, the second ultraminiaturized generation of SPC should be finalized by the end of 1997.

A combination of SPC integrating an ACEP battery that can be substituted by other Li-ion batteries incorporating a solid or liquid electrolyte, or even by a NiMH battery, and a multifunctional microsystem on a smart card in PCMCIA format, with keyboard and LCD, will bring innovative solutions to high-security transaction applications (financial, medical etc.) or tracking and monitoring applications a.s.o.

The following figure illustrates such a smart card.

**UT - HITESCA**

![UT-HITESCA Diagram]

**UT-HITESCA: Ultra Thin - High Technology Smart Card**

Figure II-34 - UT-HITESCA external layout

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II-3.2 Dependability analysis of complex components and systems

**Topic leader: I. C. BACIVAROV**

**Members:** I.C. BACIVAROV, L.BALME

II-3.2.1 Dependability modeling and evaluation of complex systems

The ever-increasing complexity of modern electronic and communication components and systems and the importance of the operating duties they have to accomplish calls for systematic research concerning their dependability (reliability, maintainability, safety) analysis and evaluation, based on an equally important theoretical acquisition.
In order to optimize a complex system from the dependability point of view several of these components must be considered; their importance varies as a function of the system type and functional criticity.

The main objectives of this work are the development of efficient models and algorithms for the computer-aided dependability (especially reliability and safety) analysis of complex, high functional importance systems.

In the first phase of our research two problems were studied, namely:

(a) computer-aided structural analysis (using minimal cut set/tie set approach) for complex systems described by their reliability graph (with application to distributed systems);

(b) computer-aided availability/safety evaluation for systems with renewal, modeled by their fault trees.

Some solutions in order to improve the effectiveness of the Failure Modes and Effects Analysis (FMEA) and the Fault Tree Analysis (FTA) techniques using new approaches, including those based on the artificial intelligence, as well the extension of these techniques for the case of the software systems were also investigated.

1997 Developments

Development of scientific and educational software (computer programs), mainly to support computer-aided quality and dependability training/education on the following topics: Statistical Quality Control (based on ISO 2859-1/2/3; Statistical Process Control; Reliability analysis based on cause-consequence diagrams; Reliability Optimization; Fault Tolerant Electronic Systems (redundant structures) a.o.

II-3.2.2 Reliability testing of semiconductor devices

The risk of failure resulting from the combined effects of high temperature, humidity and electrical bias continues to be important for semiconductor devices and requires testing at these stress factors. At the same time, the component manufacture must have reliable information on the behaviour of his own products at the kind of stress used for screening.

As a result of our researches, based on the modeling of the physical phenomena involved, design curves at temperature cycling both for screening and qualification testing were obtained for several types of semiconductor devices.

A model for the stress (temperature and voltage) dependence of the semiconductor device reliability was developed taking into account the physical aspects of the failure mechanisms involved; this model is useful for the design of reliability accelerated tests.

We have also investigated the influence of humidity on semiconductor device reliability, with two main purposes: to emphasize the role of humidity in the failure process as a stress factor and to model the reliability - humidity relationship. On this basis an original model, a generalized Arrhenius relation was derived. It is important to mention that this model can be also used for the superposition of many stress factors: thermal cycling, pressure and mechanical stress.
1997 Developments

The researches concerning the reliability of electronic components were successfully extended to the failure mode and mechanisms analysis and to the reliability testing of Surface Mounted Devices (SMD) and focused on the Surface Mounted Electronic Assemblies (SMEA).

II-3.2.3 Reliability prediction based on a synergetic approach

To design the reliability of electronic systems used in such fields as aerospace, defence or transport, one must know accurately the reliability of the involved electronic components. It seems that the usual reliability prediction procedures (e.g. Mil-Hdbk 217) do not supply the necessary prediction accuracy and new procedures are desirable, starting from the failure physics.

Based on our researches, a new methodology was proposed, which could be used: (I) to predict the failure rate of a batch of electronic components at the design phase of the manufacturing process; (II) to model the influence of the operational stress on the failure rate; (III) to verify the failure rate value with accelerated life tests.

Because a large number of process parameters and stress factors -which are interdependent- are involved, the synergies between these parameters are taken into account.

This new methodology contains three procedures and take into account the synergies existing between the technological factors, the stress factors in an operating environment and the stress factors at the accelerated stress tests, respectively. One main point of this methodology is the assessment of failure-risk coefficients (FRC) based on a fuzzy logic for the potential failure mechanisms.

Basically, this synergetic approach can be used for any product. In the first phase of our researches, this methodology was developed for the semiconductor devices, because the semiconductor device manufacturing process is one of the most complex in today industries. Consequently, the lognormal distribution, known as suitable to describe the failure mechanisms of semiconductor devices was used.

II-3.3 Wavelets approach to complex integrated systems

Topic leader: G. TKEBUCHAVA

Members: L. BALME, G. TKEBUCHAVA

Research areas:

The research activity addresses the following:

a) Characterisation of some functional spaces, arising in complex integrated systems by means of wavelets

b) Quality of complex integrated systems

With the rapid development of computerised scientific instruments comes a wide variety of important problems for data analysis and signal processing. In fields ranging from Econometrics to Computer Graphics to Medical Imaging to Computer Vision one must recover a signal, curve, image, spectrum, or density from incomplete, indirect and noisy data.
Wavelets give the opportunity to qualitatively examine data or function or a variety of scales. They also allow to focus in local features of data series in situation, where traditional approaches such as Fourier analysis smear out some of local detail.

Based on our research we look for the optimally conditions which provide the existence of wavelets with requisite properties. The characterisation of function spaces by means of wavelets and splines give the possibility to solve many problems arising in complex integrated systems, such that recovering, minimax data compression problem, statistical estimation problem.

**Project status:**

Under development

**II-3.4 European programme in quality of complex systems (EPIQCS)**

*Topic leader: L. BALME*

*Members 1: I. BACIVAROV, L. BALME*

**II-3.4.1 - Presentation**

In order to cover new industrial needs in the mastering of quality and a dependability of complex integrated systems, an original European Post-graduate Programme specialised in the Management of Quality in Complex Integrated Systems has been created in 1991, with the collaboration of the Consortium Linking Universities of Science and Technology for Education and Research (CLUSTER) and the European Program COMETT II, by several major Technical Universities and Industrial Groups:

**Universities:**

**Key Members:**
- Ecole Nationale Supérieure d'Arts et Métiers, Paris, France
- Institut National Polytechnique de Grenoble, France
- Technische Hochschule, Darmstadt, Germany
- Universidad Politecnica, Escuela Tecnica Superior de Ingenieros Industriales, Madrid, Spain.

**Associated Members:**
- University POLYTECHNICA, Bucharest, Romania
  - Ecole Nationale de l'Industrie Minérale, Rabat, Morocco.

**Industrial partners:**

Several Industrial Partners, Quality and Professional Associations are involved in the definition of the courses as well as in the management of the Programme:

**Key Members:**
- BULL S.A., Paris, France
- CSEM, Centre Suisse d'Electronique et de Microélectronique S.A., Neuchâtel, Switzerland
- DASSAULT Aviation, Paris, France

1 List of EPIQCS members only involved in research activity within TIMA Laboratory. Complete list of Steering Committee members and previous research works available upon request from L. BALME.
The CLUSTER organisation is composed of 10 Universities:

- Ecole Polytechnique Fédérale de Lausanne, Switzerland
- Eindhoven University of Technology, The Netherlands
- Imperial College, London, England
- Institut National Polytechnique de Grenoble, France
- Politecnico di Torino, Italy
- Royal Institute of Technology, Stockholm, Sweden
- Technische Universität, Darmstadt, Germany
- Trinity College, Dublin, Ireland
- Universität (TH) Karlsruhe, Germany
- Université Catholique de Louvain-la-Neuve, Belgium.

II-3.4.2 - EPIQCS objectives and organisation

EPIQCS is a voluntary, non profit European Association gathering Technical Universities, Business Schools as well as Industries, Service Companies and European & National Quality Associations.

The aims of the association are:

- Issue the European Master's Degree specialised in Quality of Complex Integrated Systems. The European Master's Degree EPIQCS is recognised by the Universities as well as by the Industrial Partners and the Quality Associations, members of EPIQCS Programme.

- Assist any of its members in the evaluation of linguistic and technical skills of candidates to Quality Degrees and Certificates of Competence.

The European Master's Degree specialised in Quality of Complex Integrated Systems is accessible to any individual candidate as well as to candidates presented by Universities, Companies and Quality Associations who fulfill the following requirements:

A) Initial requirements

a) Education

Engineer degree, master degree, business school degree or equivalent.

b) Language

Fluent in the language of the country of practice and English.
B) Complementary requirements

a) Common Core Syllabus on Total Quality Management

Candidates must have followed a complementary training devoted to Total Quality Management, composed of at least 200 hours of courses, practical training and case studies and total syllabus having been approved by the EPIQCS Steering Committee.

b) Specialised Options

In the different options offered by EPIQCS, candidates, after having completed the common-core syllabus, must have followed Specialised Courses composed of at least 180 hours of courses, practical training and case studies, and approved by the EPIQCS Steering Committee.

c) Professional Thesis

Finally, candidates must obtain a Professional Thesis which must be situated at the level of graduated studies.
The Professional Thesis must show the ability of the applicant to build an original approach in the resolution of a complex problem belonging to the quality of complex integrated systems.
A large involvement of the Industrial Partners is requested in the management of the Professional Thesis, giving to the work a large feature of application, without sacrificing the fundamental and theoretical basis typical of academic work.
The Professional Thesis must be prepared for a period of at least 9 months, preferentially after completion of the common core syllabus and the specialised option, under the management of two tutors, one from Industry, one from University, nominated by the Director of the Degree.

C) Issue of the European Master's Degree specialised in Quality of Complex Integrated Systems

On the evidence brought by the candidate that he/she fulfills the above requirements, a Jury composed of at least 3 members of the EPIQCS Steering Committee, 2 of whom belonging to the University issue the Certificate of Competence named "European Master's Degree specialised in Quality of Complex Integrated Systems", in different options.

II-3.4.3 - EPIQCS results

Until now, EPIQCS has issued 111 degrees to postgraduate students from Grenoble and Madrid.

The current EPIQCS research works are dealing with advanced quality assurance modelling in ICs manufacturing, quality assurance in aeronautics CAD-CAM and RAMs modelling applied to service industries.

Y. JANIN has presented his research work in view of the EPIQCS professional thesis on the theme: Quality Assurance in Man Machine Interface at Sextant Avionique.
II-4 Reliable Integrated Systems (RIS)

Group Leader: M. NICOLAIDIS
(e-mail: Michael.Nicolaidis@imag.fr)

Members: A. ABDELHAY, I. ALZAHER-NOUFAL, L. ANGHEL,
S. BOUTOBA, T. CALIN, L. F. COSTA, N. DJIDI,
M. A. NAAL, M. NICOLAIDIS, I. RAYANE,
J. VELASCO-MEDINA, N. ZAIDAN,
A. R. ZOLFAGHARI, E. SIMEU

Research areas:

This group investigates:
- On-Line Testing techniques for VLSI including, Self-Checking Circuits, UBIST, On-Line Current Monitoring, Perturbation Hardened Circuits, and Fail-Safe Design
- Off-Line Testing techniques such as BIST, Idq Testing, Synthesis for Testability, Analog and Mixed Signal Test.

Contracts:

MEDEA AT 401, AMATIST

II-4.1 On-line testing for VLSI

Members: I. ALZAHER-NOUFAL, L. ANGHEL, T. CALIN,
L. F. COSTA, M. NICOLAIDIS, I. RAYANE,
N. ZAIDAN, A. R. ZOLFAGHARI, E. SIMEU

As VLSI process achieved in the past quite good levels of reliability, these techniques was basically destined to specific applications requiring very high reliability or evolving in hostile environments (such as fault tolerant computing, safety critical applications, aerospace, etc.). We are now in a turning point where technological evolution is accompanied with a drastic reduction of reliability. In fact, progress in technological scaling allows the integration of hundreds of millions of transistors into a single chip, moving quickly to the multi-billion transistor capacities. The integration of complex systems into a single chip that may include heterogeneous parts such as logic, SRAM, DRAM, non-volatile memories, analog and even micromechanical and optical parts, is becoming a reality. Achieving acceptable reliability levels for these complex products is one of the most critical issues that need to be faced. However, the increased operation speeds and noise margins reduction that accompanies the technological scaling, are reducing continuously the reliability of deep submicron ICs face to the various internal sources of noise. This process is now approaching a point where it will be impossible to produce ICs that are free from these effects. A more significant problem is related to the single-event upsets (SEUs). The latest data show that up to 20 neutrons/sq cm/hr reach the Earth's surface with an energy higher than 10MeV. This energy level is not a concern for today's CMOS processes. But below 0.1um, or for low voltage applications (2.2 V or less), the frequency of errors induced by cosmic neutrons will become unacceptable. This means that circuits that have tested thoroughly after fabrication and do not present any structural or parametric defects, will exhibit a high rate of errors during system operation. These errors concern both memories and logic. Under this context, fault tolerant approaches must be used at any single application. Since fault tolerant design on system level results on a development and production cost that most of applications can not afford, the only viable solution is to modify the design
practice and CAD tools in order to generate soft-error-robust designs. As the device shrinking will progress further, and device behavior will become statistical (that is the device will behave correctly with a probability which is becoming increasingly different from 1), design increasingly robust to soft-error must be employed.

Concerning large memory arrays, cost efficient solutions based on error detecting/correcting codes have been used extensively in the past and may be used to cope with this problem for both stand alone and embedded memories. An alternative solution proposed recently consists on using a Built-In Current Sensor per memory column and a parity bit per word. It allows soft error detection and correction by means of lower hardware cost and zero latency, but requires a more complex design style.

The above methods will require an excessive hardware cost if they are applied to small memory arrays and distributed memory cells (e.g. latches, flip-flops, registers). In this case, an alternative solution will consist on the use of perturbation-hardened memory cells. Solutions insensitive to single node perturbations of any strength have been proposed recently. A 100% hardware overhead is required for a memory cell, while the cost is 50% for a flip-flop. Although this cost can be seen quite high, in situations and fabrication processes where logic parts are not sensitive to soft errors, replacing all latches and flip-flops with these elements will result on low cost soft-error-hardened designs.

However, deeper submicron scaling and increased operation speeds, will require in the near future the protection of logic parts too. Fault tolerant designs based on massive redundancy (e.g. TMR) are not of interest due to their high cost. Perturbation-hardened logic is another alternative, but a duplication cost is required. This cost will become acceptable when device size reduction and operation speed increase will result on statistical device behavior and require increasingly robust designs to cope with high soft-error rates. However, for the near future, this cost is not acceptable in a majority of applications. Due to the transient nature of the faults, a combination of concurrent error detection and retry can cope with. Self-checking design can be used for this purpose. Self-checking circuits achieving the fault secure property guaranty concurrent error detection of all errors produced by single faults.

Various developments on this domain performed within the group are presented below.

II-4.1.1 Self-checking (S-C) circuits

Members: I. ALZAHER-NOUFAL, L. F. COSTA, M. NICOLAIDIS, A. R. ZOLFAGHARI

Periodic off-line testing of VLSI circuits may be used to ensure hardware failure detection. However, errors produced by hardware faults will remain undetected until the test phase. Also, off-line testing is not effective against transient faults. On the other hand, concurrent error detection techniques are able to detect errors due to both hardware faults and transient faults as and when they occur. Concurrent error detection based on software encoding techniques needs special software development and will significantly decrease the system speed. Alternatively, hardware encoding based on special-designed self-checking circuits may be used. One advantage of self-checking circuits is that they may be designed to cover well known models of hardware faults.

A self-checking block is composed by a functional block which generates encoded outputs and a checker which verifies these outputs. The checker delivers a two output error indication signal (01 and 10 mean correct functioning and the other values mean error detection). The objective of designing self-checking circuits is to achieve the totally self-checking goal, i.e. the first erroneous output of the functional block must signalized by the checker. To ensure this goal, functional
blocks and checkers must verify well defined mathematical properties introduced by W. C. Carter and later defined by D. A. Anderson. J. E. Smith and G. Metze have defined the largest class of functional circuits (i.e. strongly fault secure circuits) and, more recently, we have defined the largest class of checkers (i.e. strongly code disjoint checkers) necessary to ensure the TSC goal.

Complex self-checking systems can be designed by assembling several self-checking blocks. In that case a global double-rail checker is used in order to reduce the error indications of the different self-checking blocks into a single error indication.

Self-checking design solutions and design tools are in progress in the group, evolving versus a comprehensive CAD environment for self-checking design.

II-4.1.1 Implementation techniques and tools for self-checking data paths

Recent investigations in the group led to the development of low hardware cost TSC data paths. These developments include the carry checking / parity prediction scheme for adders, ALUs, and parity prediction for shifters and barrel shifters. Other developments concern the design of fault secure parity prediction multipliers and dividers. A comprehensive framework of CAD tools for self-checking data path design is developed. It includes various macroblock generators that generate self-checking adders and ALUs based on the above solutions. They support a vast variety of ripple-carry, skip-carry, carry lookahead and conditional sum adders and ALUs, various single-position and multiple-position shifters, regular array dividers, regular array multipliers, and fast multipliers using Wallace trees and fast carry propagate adders, with non-recoded or recoded operands (Booth). Low-cost S-C Adders, ALUs and Shifters are generated by the tools. The cost for multipliers is quite higher (35% for Booth multipliers and 47% for multipliers with non-recoded operands). These solutions are used for small and medium multipliers. For large multipliers (larger than 16x16 for Booth multipliers, or larger than 8x8 for non-recoded operands), techniques based on residue arithmetic codes result on lower cost, which can be as low as 5% for large multipliers (e.g. 64x64 or larger). Our tools allow to generate these solutions for a wide range of multiplier structures, such as regular array multipliers, and fast multipliers using Wallace trees and fast carry propagate adders, with non-recoded or recoded operands (Booth). The tool is first analyzing the multiplier structure in order to determine the residue code that guaranties the fault secure property, and then it generates the self-checking multiplier as well as the translator parts required to make it compatible with parity checked self-checking data paths and memories. These tools together with generators for self-checking checkers blocks and register files are organized into a CAD framework for self-checking data path design that results on low-cost fault secure data paths (typically 20% overhead form medium size data paths and lower for larger ones).

II-4.1.1.2 Synthesis of self-checking multilevel circuits

This topic is becoming very important. Tools that synthesize low cost multilevel combinational circuits and FSMs will allow (together with the tools for generation of self-checking data paths) the design of cost effective self-checking VLSI circuits, making these techniques very attractive for industrial use.

PLAs were widely used in the past to automate the design of VLSI circuits. However, with the development of efficient tools for synthesis of multilevel circuits, PLAs are loosing interest. In order to have a complete set of tools that automate the design of self-checking circuits, we need to develop tools for synthesis of multilevel combinational and sequential self-checking circuits. Some investigations by a few research groups on this area have already been done. However, the extra hardware required for the synthesized circuits is not low enough to make these first tools attractive for industrial applications.

In fact, there is no single self-checking solution that always lead to the best result. Our objective on this project is to develop various tools leading to various self-checking solutions. The tool will try all the solutions for each target circuit and will select the one resulting on the lower hardware cost.
II-4.1.2 Perturbation hardened circuits

Members: T. CALIN, M. NICOLAIDIS

This project Previous works consider the design of perturbation hardened memories and more precisely SEU hardened ones. They basically used NMOS or PMOS gates to implement additional storage elements and feedback circuit that restore the logic state of the upset node. Using NMOS or PMOS latches introduce significant power dissipation. Thus, the technique can not be used to implement circuits that include an important number of latches or to implement memory arrays. Also these designs use critically ratioed inverters to achieve upset immunity. Their characteristics change with statistical process parameters, operating temperature and radiation total dose, having as effect the reduction of the upset immunity. Finally these designs are very expensive in silicon area.

The new solutions obtained in this project have none of these drawbacks. They are implemented in standard CMOS process, they do not require specific size proportioning for the transistors, they have the same speed and same power dissipation as standard memory cells. The area of the new cells is twice the area of a standard RAM cell. they can be used to replace the latches of a circuit resulting on an SEU hardened design. They can also be used as memory cells to build memory arrays of any size, resulting on low cost SEU hardened single-port or multi-port RAMs.

The project is now progressing on the direction of perturbation tolerant combinational and sequential circuits. The goal is to provide solutions that are very robust with respect to soft errors, in order to cope with very high error rates corresponding to very deep submicron scaling in future VLSI processes. These design techniques should be adaptive in order to increase the soft-error robustness to cope with increasing error rates resulting from the continues evolution of technology on deeper submicron scaling.

II.4.1.3 Model-based numerical redundancy generation for concurrent checking

Members: A. ABDELHAY, E. SIMEU

The basic principle of this approach is to build a concurrent error indication signal using inherent analytical (rather than physical) redundancy, contained in the static and dynamic relationships among the system input and measured signals. In other words, residuals are generated using the available mathematical knowledge on the monitored system. The residuals express the deviation of the input and available measurements provided by the actual system with respect to the system nominal model. This deviation is close to zero in normal operation, different from zero in the faulty situation. According to the size and the system environment, two main strategies of residual generation are considered: hardware and software. In the hardware approach residual generation is performed by adding dedicated circuitry for concurrent error detection. This strategy allows for parallelism of detection tasks. Every critical element in a large plant may provide the requested detailed information on its current health status to the plant supervisor. For more complex systems including intelligent module, algorithm-based techniques are suggested and may be implemented without additional hardware. In accordance with the kind of quantity used for analytical model-based residual generation, the wide variety of possible methods can however brought down to few basic concepts:

methods using non measurable state variable x(1), methods using non measurable systems parameters Q, and the methods using non measurable characteristic quantity n(u(t), x(t), Q).
II.4.1.4 On-line fault detection for analog systems

Members: I. RAYANE, E. SIMEU

In contrast to the previous project using algorithm-based fault tolerance, the error indication signal generator is directly hard-wired into the system using additional detection circuitry. Residuals are generated on-line by means of dedicated additional hardware into the system data flow graph. Using the nominal state model of linear analog systems, checksum codes have recently been proposed in the literature, as a mean for concurrent error detection in a particular class of linear analog systems: state variable systems. In such systems, the state variables are assumed to be accessible. This hypothesis only recovers a particular class of linear systems since, for the majority of real systems, the state variables are not accessible. We suggest a technique of redundancy equation generation based on the replacement of the unknown state variables by measured output signals. Further to the classical projection on the parity space, we perform an original elimination of unknown based on the analysis of the Kroneker invariant for available nodes and aggregation of equations. In our approach redundant hardware is inserted in the circuit data flow graph. The goal concurrent checking is extended to a larger class of linear analog systems than in previous methods while the hardware cost remains comparable.

II.4.1.5 On-line current monitoring

Members: L. ANGHEL, T. CALIN, M. NICOLAIDIS

Because current monitoring can cover faults creating undetermined levels and thus may escape detection by logic monitoring techniques, the use of Built-In Current Sensors (BICS) for on-line current monitoring is of high interest.

II.4.1.5.1 Concurrent current monitoring

For concurrent current monitoring, fast BICS able to operate on the operation speed of the circuit, and adds a diode to bypass the BICS during the transient phase of the circuit, where large transient currents have to be driven. The whole system was integrated in a standard CMOS process.

Some problems related with the on-line current monitoring are:
- The BICS must be as fast as the monitored circuit and still offer a good resolution. This task is not very easy knowing that the Built-In Current Sensors are integrated in the same IC as the monitoring blocks, and maybe the IC process is not adapted for fabricating fast and accurate BICSes.
- Inserting a BICS in the current path of a circuit may affect circuit performance adversely.
- The BICS is activated when the current reaches its steady state. However, the output signals of a circuit reach their logic levels prior the steady state of the current. This means that the clock must be slow down to allow the current reaching its steady state.

These problems are more serious in CMOS process which is not particularly adapted for designing fast BICSes with high resolution and does not offer efficient bipolar devices able to drive large transient currents. This project investigates ways for solving these problems.

II.4.1.5.2 Periodic current monitoring

Most of these problems can be avoided if instead of concurrent current monitoring one uses periodic current monitoring. In this situation one can slow down the circuit clock for short periods of time and perform current monitoring. Since the clock speed is reduced, slower BICSes can be used and the current decay delay is no more a concern. Also, during the normal speed operation, a bipolar device can be switched on saturation mode to reduce performance lost. The periodic current monitoring can be performed either by using the normal operation inputs of the circuit, in this case
the operation of the system is not stopped but only slowed, or by applying an external test sequence for increasing test efficiency.

The drawback of this technique is that errors produced between two test phases are not detected. For permanent faults (defects), the technique can achieve a quite high level of protection if the following assumption holds:
Assumption: the failure mechanisms are developing slowly, so that, between the manifestation of a defect by means of abnormal current dissipation and the occurrence of a functional fault, a large time interval elapses (or better, the probability for this time interval to be shorter than the period between two test phases is very low).

From this assumption defects are detected by the periodic test phase before their manifestation as functional faults and thus periodic test offers a perfect protection.

The on-line current testing techniques (periodic or concurrent), proposed above for permanent faults induced by circuit aging, can also be used for permanent faults induced by the radiation total dose. The effects of total dose consist on transistor threshold shifts and leakage current increasing. Both effects involve abnormally high current consumption which enables fault detection based on current monitoring. This application is well adapted for periodic current monitoring since the slow cumulative process of the total dose is shifting gradually the transistor thresholds and leakage currents.

The project investigates the best solutions for implementing these ideas.

II.4.1.5.3. Soft-error detection

Soft errors such as for instance upsets induced by heavy ions or electromagnetic radiation, induce abnormal activity in the circuit. It is reflected on abnormal activity on the power bus. Then, a BICS can be used to detect the abnormal power bus activity.

The BICSes for concurrent current monitoring considered above are synchronous to the circuit clock. However transient faults are asynchronous events and require using asynchronous BICS. Such a BICS has been studied and used to design upset tolerant RAMs.

The technique uses an asynchronous BICS to monitor the power lines of each column of the RAM. A parity bit per word is also used. When an upset occurs one of the BICSes detects the upset and indicates the affected column. The RAM is then read and the error is corrected by inverting the corresponding bit of the word with inconsistent parity. The test results of the prototype RAM show the efficiency of the technique for detecting and correcting the upsets. Furthermore these results show no measurable speed and noise immunity. Note that the asynchronous BICS can also detect permanent faults in the RAM, achieving a complete fault coverage.

II.4.1.6 Fail-safe circuits

Members: N. ZAIDAN, M. NICOLAIDIS

Fail-safe systems are implemented using a processing part checked using some kind of hardware or software redundancy and by a fail-safe interface which transforms the outputs of the processing part into fail-safe signals (i.e. signals which are either correct or safe). Conventionally, the fail-safe interface is implemented using specific fail-safe discrete components. Such implementations have high cost and are very cumbersome. This work presents VLSI implementable fail-safe interfaces for self-checking systems using duplication or other error-detecting code techniques, and for fault tolerant systems based on triplication. With respect to a scheme that we have proposed in the past, the new scheme uses concurrent checking techniques instead of periodic testing based on BIST implementation.
II-4.2. Off-line testing techniques


Techniques destined to fabrication test are addressed here. Progress in technological scaling allows the integration into a single chip of hundreds of millions of transistors, moving quickly to the multi-billion transistor capacities. The integration of complex systems into a single chip, that may include heterogeneous parts such as logic, SRAM, DRAM, non-volatile memories, analog and even micromechanical and optical parts, is becoming a reality. Achieving acceptable reliability levels for these complex products is one of the most critical issues that need to be faced. Testability is therefore a key factor that could limit these trends if not addressed adequately. At these levels of complexity external testing is becoming unfeasible due to ATPG limitations (reduced controllability/observability due to rapidly increasing #devices/pin and sequential depth). At the same time, the scan approach is losing interest due to the increasing length of scan chains (and thus test length), and low test application speed. At-speed test is a major limitation at a context where increasing clock frequencies (moving quickly to the multi-GHz domain), are making timing faults predominant. Automatic Test Equipment (ATE) is another important limitation, since, although its very high cost, it does not offer the memory capacities/depth and test application speed, required for testing nowadays ICs (development and production cycles are constraining ATE to use two-generations old IC technologies). In addition, several testers must be used to cope with the heterogeneous parts integrated into a single chip, increasing the test cost drastically. Under these constraints, the only realistic issue is to extend the BIST practice beyond memory testing. This requires new developments on logic BIST for increasing fault coverage while containing hardware cost, and extension of BIST approaches to the analog and eventually micromechanical domains.

Analog BIST, BIST and Built-In Self-Repair for Memories, Built-In Idq testing, and Synthesis of testable systems are considered in this framework.

II-4.2.1 BIST and built-in self-repair for memories

Members: S. BOUTOBZA, N. DJIDI, M. NICOLAIDIS

Large static and dynamic RAM arrays are embedded in modern ICs. They often represent the largest part of the chip area. Since, in addition, memories are very dense they include the largest part of transistors of the chip. Because they are designed to be as tight on the technology as is permitted by the physical limits of the technology they are more susceptible to failures than standard logic. Memories therefore will represent the larger amount of defects in such chips. Thus, achieving low defect level in memory parts is essential for achieving low defect level for the whole chip. BIST solutions and tools able to uncover the real defects corresponding to the given memory design and fabrication process is of high importance. Memory BIST synthesis tools targeting this problem are considered in this project. These tools will address both standard memory BIST and transparent memory BIST. This last is of high importance, since it preserves the memory contents (thus allowing periodic testing in the field), and increases coverage of unmodelled faults.

At the same time, as large memory arrays will concentrate the majority of the defects of the chip, defective memory blocks will affect chip yield dramatically. Built-In Self-Repair hardware is necessary to obtain acceptable levels of manufacturing yield, or increased product life through self-repair in the field. One of the aspects of this project concerns the development of solutions and tools for low cost/high self-repair capabilities Built-In Self-Repair hardware.
II-4.2.2 Testing of analog circuits

Members: T. CALIN, M. NICOLAIDIS, J. VELASCO-MEDINA, I. RAYANE

This project concerns the development of innovative test techniques for analog and mixed signal circuits. In this phase the efforts are concentrated on a new test technique based on current level stimuli, in opposition to the conventional techniques based on voltage level stimuli. Our preliminary investigations show that this technique allows to detect faults that are undetectable or difficult to detect when using a conventional (voltage level stimuli) technique. In addition DFT or BIST implementation has considerable advantages such as low hardware cost and no functional penalty. These advantages are due to the fact that a current stimuli can be injected to a node without requiring any isolation of the node from other signal sources. Thus no switches have to be inserted in the normal signal paths, avoiding functional perturbation and high hardware cost. DFT will be implemented by creating connections to the selected nodes. The BIST implementations use a current generator and several current mirrors and switches to inject the current stimuli to the selected nodes.

II-4.2.3 Built-In Iddq testing

Members: L. ANGHEL, T. CALIN, M. NICOLAIDIS

Iddq Testing was shown to be a necessary complement of functional testing for defect level reduction and quality improvement of ICs. This technique is based on the fact that the steady state current of static CMOS circuits is several orders lower than the current dissipation created by a large majority of manufacturing faults. This situation is changing with the introduction of deep submicron technologies where the steady state current dissipation is increased by several orders of magnitude, reaching the levels of currents encountered in defective circuits. Due to this situation Iddq testing has to be abandoned in the next generations of CMOS circuits, unless new solutions are devised. Built-In Current Sensors can offer one possible alternative, since we can partition the circuit in smaller parts with reduced Iddq current. A BICS will be used to monitor the Iddq of each part.

The project is studying BICS structures that are suitable for this application (sensitivity, cost and circuit performance impact). The exploitation of the Built-In Current-Sensors for performing both on-line testing and fabrication testing is also investigated to share their cost and provide low cost test solutions.

It is worthy to note that these kind of solutions could eventually expand the applicability of Iddq testing for one or two process generations, but on the long term this technique has to be abandoned as deeper submicron scaling will bring closer defective current levels and static current dissipation.

II-4.2.4 Synthesis of testable systems

Members: M. A. NAAL, E. SIMEU

High-level synthesis consists in generating an RTL-level description of a digital system from its behavioral specification while satisfying a set of designer specified constraints. Control scheduling, functional units and register allocation and operation binding are the tree major tasks executed in synthesis procedure with the objective of optimization of both area and speed constraints. Traditionally, testability considerations are not in the synthesis level, the additional test dedicated circuitry is defined and inserted later in RTL level. This would likely lead to a hard to test design. Also, common test techniques such as Built-In Self-Test and scan design generally require speed performance degradation and considerable area cost. This cost may become quite higher if the circuit the test circuitry is inserted at the later stages of the design process. To avoid this difficulty,
testability considerations have to be incorporated into earlier design stage, during the high-level synthesis process. As well as area and speed considerations, testability of the design is taken into account the three major task in high level synthesis. At the present phase, the project is concentrated on the exploitation of the transparency properties of functional units to guarantee the testability of data path by means of reasonable speed degradation and area overhead. The test procedures are implemented in the controller which is assumed to be self-testable.
II-5 System Level Synthesis (SLS)

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Members: S. ARAB, E. BERREBI, W. CESARIO, P. COSTE,
J.M. DAVEAU, J. FREHEL, Ph. GUILLAUME, F. HESSEL,
Ph. LEMARREC, C. LIEM, G. MARCHIORO, I. MOUSSA,
F. NAÇABAL, M. ROMDHANI, R. SUESCUN, Z. SUGAR,
N. C. VALDERRAMA, N. ZERGAÏNOH

Research areas:

This group investigates flexible and modular methodologies for the specification, design and
synthesis of heterogeneous systems including hardware and software. The main research topics are:
- SDL based hardware software codesign
- VHDL based behavioral synthesis
- Multilanguage cospecification, codesign and cosimulation

Contracts:

AEROSPATIALE, FRANCE TELECOM, SGS-THOMSON, PSA, ESPRIT-CODAC, ESPRIT
COMITY, ARCOS, ATAME, MEDEA SMT.

II-5.1 System level synthesis

The integration of modular and flexible components is becoming a bottle neck when designing
modern embarqued electronic systems. For instance, the Airbus A340 includes more than 100
embarqued computers running 20 MB software. In order to master this growing complexity,
modular and flexible design methods acting at an early stage of the design process are then
essential. Indeed, evidence suggests that most important design decisions are made early in the
design process where a poor decision can jeopardise an entire project.

The use of separate tools and methodologies for the design and specification of hardware and
software leads to the well-known 90/50 rule. This rule states that 90% of ASICs work first time
according to their logic specification. Unfortunately, about 50% of these ASICs need to be
reworked because they fail when inserted into their environment. The complexity of today's design
and in particular heterogeneous systems implies that global system approaches are essential in order
to solve this problem. It is now commonly admitted that most of these failures could be avoided if
circuit design was integrated with system design.

II-5.1.1 Hardware-software co-design

The main objective of this work is to develop COSMOS, a co-design methodology and tools aimed
at the design and synthesis of complex mixed hardware-software systems. The system design
process starts with a system-level specification that may be given in an existing language such as
SDL, State Charts, C, VHDL. Our philosophy is to allow the designer to use one or more of these
languages and to translate these descriptions into a common intermediate form, called SOLAR,

1 Permanent visitor from SGS Thomson
2 Industrial Ph.D
capable of modeling the main concepts handled by system-level specification languages (concurrency, high-level communication, synchronization and exceptions) and HDL. This intermediate form then acts as an input to the system-level synthesis tools.

As shown in Figure II-5.1, the design process in the COSMOS environment is decomposed into four refinement steps: system-level specification, system-level partitioning, communication synthesis (including channel binding and channel mapping), and architecture generation (including virtual prototyping and architecture mapping).

All the intermediate models (between system-level specification and C/VHDL) are represented in a design representation called SOLAR. SOLAR is an intermediate form for system-level concepts, which allows several levels of description.

The first step in COSMOS is the translation of the initial description into SOLAR. At this level, a system is represented as a set of communicating processes. The next step in the design flow is partitioning. The goal is to distribute the previous model into a set of communicating modules that will be mapped onto separate processors in the final prototype. This step produces a refined model composed of a set of communicating and heterogeneous processes organized in a graph where the nodes may be either processors or communication units. This step also fixes which technology (hardware or software) will be used for the implementation of each unit. This model needs to be refined in order to fix the communication models. The communication synthesis is composed of two operations. The first one, called channel binding, selects an implementation protocol for each communication unit. The second one, called channel mapping, distributes the protocol among the processors and specific communication controllers. The result is a set of interconnected processes communicating via signals and having the control of the communication distributed among the processes.

The final step is the architecture generation step. It starts with a set of interconnected hardware/software sub-systems (output of communication synthesis) and makes use of two methods in order to produce a prototype. The first method produces a virtual prototype that can be used for simulation. The virtual prototype is an abstract architecture represented by VHDL for the hardware elements and by C for the software. This description is finally mapped onto a multi-processor architecture.

Of course the design process will include lots of feedback loops in order to redesign parts or the full system. At any stage of the design, the user can cancel one or several design steps in order to explore new choices.

II-5.1.2 System-level design representation

Members: R. SUESCUN, M. ROMDHANI, J.M. DAVEAU, G. MARCHIORO

Most of the existing co-design systems are based on a single paradigm or language. Discrete languages such as SDL, StateChart, C, VHDL, C++, are used for the specification of both hardware and software. Experience with formal specification languages has shown that there is no unique universal specification language for all kind applications. The use of specification languages has to be selectively targeted. Some of these languages are more suitable for state-based specification (e.g. SDL or StateChart), some others are more suited for dataflow (SPW, COSSAP), specific languages like MATLAB and MATRIX are represented for continuous model, while many others are more suitable for algorithmic specifications (e.g. C or ADA). In addition when a large system has to be designed by separate groups, they may have different cultures and expertises with different environments. Therefore, in this project, we are targetting multi-language specification. Thus when describing a complex heterogeneous system, we can use the most suitable format for the
specification of each sub-system according to its application field and to the culture of the corresponding designers.

In order to cope with multilanguage specifications two key technologies are required:

a) Cosimulation for the validation of heterogeneous specification

b) Languages composition format for synthesis

For the validation of multi-paradigm specification we are developing a cosimulation environment able to handle several system level specification languages.

In order to handle multiformat specification for synthesis we defined SOLAR, a design representation for high level concepts in system synthesis. It is composed of a data representation model and a textual language. Although human readable, SOLAR is not a hardware description language, but an intermediate format only. Solar embodies a series of new concepts which we feel are essential for the next generation of complex hardware systems specification and synthesis. The main motivation behind the development of SOLAR is to link CASE tools and IC CAD tools, thereby allowing mixed hardware/software systems design and synthesis. The goal is to use this representation for the design of complex systems, and more precisely, a network of communicating systems. In order to achieve these goals SOLAR supports High-Level concepts such as hierarchical and interacting FSMs and high-level communication.

![Diagram of SOLAR system model]

**Figure II-5 1 - COSMOS: A global view**

The SOLAR system model is designed to accommodate the properties of all system-level specification languages (SDL, CSP, OCCAM, ESTEREL, StateChart, SpecChart, C, VHDL, etc.) that are relevant to synthesis. Of course, some restrictions on the permissible input will apply in order to have predictable and coherent results. This includes only allowing subsets of the
description languages to be used. The objectives of SOLAR are twofold. Firstly, the identification of a basic data-structure that will allow all of the aforementioned requirements to be accommodated. Secondly, the development of system-level synthesis tools, including partitioning and communication synthesis, that will produce a set of interconnected FSMs that may feed existing silicon compilers.

As stated above, SOLAR has been defined to ease the link between CASE tools and IC CAD tools, thereby allowing mixed hardware/software systems' design and synthesis. The next diagram below shows a framework example where such a representation may be useful. Although textual, SOLAR is not intended to be a new specification language. Such languages already exist. For example, the behavior of the hardware may be more easily described in a dedicated HDL such as VHDL. On the other hand, system software specifications can be readily represented in existing languages, such as ESTELLE, LOTOS and SDL for communication protocols, CSP and OCCAM for concurrent systems, ESTEREL and StateChart for real-time systems and so on. What SOLAR provides is an intermediate, unifying format for several such languages, that allows mixed hardware/software designs to be represented in a form suitable for their eventual synthesis.

![Diagram of SOLAR framework]

**Figure II-5 2 - Solar Framework**

Where SOLAR differs from other system-level representations is in its ability to accommodate system-level communication concepts such as communicating protocols, message passing and channels of communication, thereby allowing it to model most communication schemes. The channel model mixes the principles of monitors and message passing, it is known as the remote procedure call model. The channel in SOLAR allows communication between any number of processes.

During the synthesis process, COSMOS uses an external library of ChannelUnits. A ChannelUnit corresponds to either a standard protocol or a customized protocol described by the user. During partitioning and communication synthesis an abstract model of the channel is used. At the architecture mapping step, an implementation of the channel is needed. This implementation may be the result of an early synthesis step using COSMOS or another design method. It may also correspond to an existing architecture.
Results:

A prototype of a SOLAR based environment exists. Interfaces to SDL, StateChart, SAO, C and VHDL have been or are being developed. SOLAR is used for the development of COSMOS.

II-5.1.3 System level specification with SDL

Members: J.M. DAVEAU, N. ZERGAINOH

The SDL language is dedicated to the specification and the validation of communication protocols and distributed systems. In this work we introduce a new approach for the generation of C/VHDL code from SDL specifications. The benefits from this work is the realisation of an SDL to SOLAR translator using the GEODE api.

Our approach overcome the main known problem encountered by previous work which is the communication between different processes. We allow SDL communication to be translated into VHDL for synthesis. This is made possible by the use of the SOLAR form that support a powerful communication model which enable the representation in a synthesis oriented manner of most communication schemes. The SDL specification is translated into our intermediate form. This step implies a mapping of SDL concept into SOLAR. This intermediate form allows the refinement of the system in order to obtain the desired solution. The main refinement step, called communication synthesis, is aimed at fixing the protocol and the interface used by the different processes to communicate. This refinement step is aimed at closing the gap between the abstraction of system level communications and their realisation. The refined specification is translated into C or VHDL for synthesis using existing compiler or CAD tools. Current experiments include the specification in SDL and the co-synthesis of the TCP/IP over ATM protocol.

Our approach support a large subset of SDL, including all concepts that have a possible implementation in hardware. The SDL code is smaller thesis the corresponding C-VHDL models. The increase of the code size vary between 7 and 9 times, and is strongly related to the complexity of the communication involved in the system. This is due to the fact that SDL abstract communication scheme is expanded during the communication synthesis stage. Simulation time grows of a factor 20 when going from an SDL to a VHDL simulation. In these experiments SDL appeared to be adapted to the description of communicating systems but lacks high level control flow instructions and can’t manipulate data efficiently.

<table>
<thead>
<tr>
<th>design</th>
<th>processes/ states</th>
<th>SDL lines</th>
<th>VHDL lines</th>
<th>% increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>PID</td>
<td>4/34</td>
<td>331</td>
<td>2403</td>
<td>726 %</td>
</tr>
<tr>
<td>FUZZY</td>
<td>9/16</td>
<td>560</td>
<td>4765</td>
<td>850 %</td>
</tr>
<tr>
<td>ATM</td>
<td>9/20</td>
<td>794</td>
<td>7210</td>
<td>908 %</td>
</tr>
</tbody>
</table>

SDL to VHDL translation results

II-5.1.4 Hardware/software partitioning

Members: G. MARCHIORO, J.M. DAVEAU, N. ZERGAINOH, R. SUESCUN

Partitioning can be seen as a mapping of functional sub-systems onto abstract processors. During this step a behavior may be distributed among several abstract processors. Each abstract processor may include several behaviors. A partitioning system may be either automatic or interactive. The partitioning starts with two inputs: a system specification and a library of communication models.
The output is a new model composed of a set of processors and a set of communication units. The library may be restricted to predefined models or extended with user defined models.

The partitioning step also determines which technology will be used for the implementation of each processor. For example, a design unit may be implemented in pure hardware, in software running on an operating system or in micro-code adapted for a standard microprocessor. The choice is based on criteria such as execution time, rate of use, re-programmability, re-use of existing components and technology limitation.

This work develops a new methodology for hardware/software co-design that implements an interactive transformational partitioning approach capable of handling distributed systems and multiprocessor target architectures. The transformational partitioning approach presented here allows to link a system-level specification to a hardware/software architecture in a short design time with fast and large exploration of the design space. The main application domain of this work is the design of distributed architectures made of software processors (e.g. Instruction-level programs) and hardware processors (e.g. ASICs). In contrast to the classical co-design approach implemented by most of existing co-design systems, this approach deals with a flexible target architectures composed of processors communicating through a complex network. The main contribution of this work is the application of the transformational approach to hardware/software co-design of multiprocessor architecture.

In the transformational methodology presented here, the user starts the design process with a system-level specification and an architectural solution in mind and realizes refinements to transform the initial specification into the architectural solution. Each incremental refinement step fixes some implementation detail, preparing the specification to the implementation. As can be seen in the figure below, the initial specification is given in SDL. This specification is converted to an intermediate model called Solar, more adapted to the synthesis algorithms. The intermediate model is refined and implemented on a distributed C/VHDL model.

The transformation of the specification into an architecture is made through three sets of primitives, called functional decomposition, structural reorganization and communication transformation. The functional decomposition primitives acts on the state tables to allow refined behavioral descriptions. The structural reorganization primitives acts on design units to allow refined structure of the system. The communication transformation primitives acts on channel units to allow refined communication protocols. The figure below presents these three sets of transformational primitives. These primitives are executed automatically but the designer decide the sequence of activation to achieve the desired solution.
In order to help the user for fast exploration of the design space, estimation methods are provided. On the design analysis step a dynamic profiling algorithm was implemented to verify the frequency of execution of each system-level instruction during a representative simulation. In the micro-architectural modeling step, software and hardware estimation algorithms were implemented, permitting the validation of the implementation based on system-level metrics of cost and performance.

Results:

The use of this approach allows a fast and a large exploration of the design space, reducing the implementation costs, increasing the system performance or dealing with another optimization criteria selected by the designer. The first prototype of this transformational approach was implemented in the Cosmos co-design environment. Current work includes the experimentation of this method on a large ATM network application.

II-5.1.5 Virtual prototyping and C-VHDL cosimulation

Members: C. VALDERRAMA, F. NAÇABAL, R. SUESCUN

A virtual prototype is an executable description of the system implementation. In COSMOS, a virtual prototype is composed of three kinds of modules: Software modules in C, Hardware (HW) modules in VHDL, and communication components that may be described in C or in VHDL.

In COSMOS, virtual prototyping corresponds to the translation of SOLAR into executable code (VHDL and/or C). Each sub-system is translated independently. The output of virtual prototyping is an heterogeneous architecture represented by VHDL for the hardware elements (virtual hardware processors), C for the software elements (virtual software processors), and communication controllers (library components).

Results:

* Development of C-VHDL co-simulation tool and methodology called VCI.
  VCI HAS BEEN TRANSFERRED TO SGS-THOMSON WHERE IT IS BEEING PRODUCTISED AND USED BY SEVERAL DIVISIONS IN GRENOBLE AND BRISTOL.
* Development of S2CV, a tool for C, VHDL generation from SOLAR.
* Definition of software scheduling algorithms.
II-5.2 Architectural synthesis based on VHDL

A lot of work has already been carried out in the domain of behavioral synthesis. Most known scheduling and allocation techniques have been applied in high level synthesis. Although behavioral silicon compilation has achieved large steps towards the automatization of VLSI design, very few systems are currently being used in industry. One of the main problems has been the lack of integration within existing design methodologies and environments.

The goal of this work is to develop AMICAL a behavioral synthesis tool that combines behavioral synthesis with methodologies allowing design re-use. AMICAL is based on pragmatic concepts allowing:

1- a close interaction with the designer
2- to handle complex and heterogeneous design through hierarchical design and design re-use
3- an easy integration within CAD environments and design methodologies.

Starting with a pure VHDL input, AMICAL produces a full specification for existing logic and RTL synthesis tools.

Classical synthesis systems usually run in an almost automatic push-button manner, therefore their performances lie on the algorithms implemented. The designer has little freedom in orienting the result. Moreover existing behavioral synthesis tools usually restrict the functional unit concept to modules executing predefined operations of the initial behavioral specification. This kind of push-button behavioral compiler that restricts component to predefined arithmetic and logic operators is convenient for narrow application domain (e.g. regular DSP operators such as filters), but suits less for non regular designs such as complex ASICs that make use of existing designs such as memories with complex protocols, I/O units or more generally complex sub-systems. What is really needed for the design of complex ASICs starting from behavioral description is an interactive environment allowing the user to refine his design through an iterative design process.

AMICAL gets around these limitations of classical behavioral compilers. In addition to a pure automatic execution mode, it allows interactivity. Moreover AMICAL brings a generalisation of the concept of functional unit leading to the use of co-processors as functional units. When using AMICAL for the synthesis of complex design, we found this approach very practical. It allows non experienced designers to perform quick synthesis through an automatic design flow. On the other hand, it allows experienced designers to exploit personal knowledge, by mixing manual and automatic execution, the architect can reach a solution close to the one he expects. Another advantage of AMICAL is that it enables hierarchical design through component re-use.

The AMICAL design-flow is illustrated by the Figure II-5.3. The two kinds of information required for synthesis are a behavioural specification and a functional unit library. AMICAL then generates a register transfer level (RTL) description that can feed existing RTL and logic synthesis and simulation tools.

The behavioural description model allows to handle very large designs based on hierarchical specification. The basic idea behind this model is that a complex system is generally composed of a set of sub-systems performing specific tasks. A high-level specification of such a system needs only to describe the sequencing of these tasks, consequently the coordination of the different sub-systems. Each sub-system is modelled as a functional module designed (or selected) to perform a set of specific operations. Therefore the behavioural specification may be seen as a coordination of the activities of the different sub-systems. The decomposition of a system specification into a global control and detailed tasks allows to handle very complex design through hierarchy.
AMICAL is based on a flexible architecture model allowing hierarchy and design re-use. The target architecture of AMICAL is composed of a top controller, a set of functional units and a communication network. These last two constitute the data-path. The communication network is composed of buses, multiplexers and registers. The network is built in order to allow the communication between functional units, and with the external world. The number of buses and multiplexers is fixed according to the parallel transfers required by the architecture.

The behavioural description is given as a standard VHDL file following a specific style. The use of complex sub-systems is made through procedure and function calls. For each procedure or function used, the library must include at least one functional unit able to execute the corresponding operation. In Figure II-5 3, the VHDL description makes call to a DCT function and uses a memory with a complex protocol (mread, mwrite). The library includes a memory, an ALU, and a DSP processor able to execute these operations. Of course, for each operation we may have several modules able to execute it. The system will select automatically the best solution. During the different steps involved in the behavioural synthesis, the functional units are used as black boxes. These may correspond to already designed complex systems. The different steps involved in the synthesis process are: scheduling, allocation and architecture generation.

Results:

The behavioural synthesis system AMICAL is pragmatic and seems to correspond to designers' needs. The most important feature of AMICAL is the fact that it combines traditional behavioural level synthesis algorithms with the ability to allow designer intervention at almost any stage of the synthesis process. The use of powerful architecture allows AMICAL to handle complex design. Several large examples, including the MPEG-AUDIO decoder, an answering machine and a PID have also been used for AMICAL evaluation. The PID circuit makes use of several complex operators including a fixed point unit that have been compiled with AMICAL itself. More recently two very large designs have been achieved using AMICAL. A motion estimator for an MPEG2 video decoder has been designed in cooperation with SGS-Thomson. This design makes use of two memory units with sophisticated protocols, of a DSP processor designed by CATHEDRAL and of 2 clocks of different frequencies. The other design is an adaptative speed controller aimed to drive up to 18 motors. The design makes use of a fuzzy logic model to implement the adaptative control. These experiments have shown that the use of AMICAL allows an increase of productivity by a factor of 5 to 10.
II-5.2.1 Scheduling and optimization for the synthesis of control flow dominated design

*Member: Z. SUGAR*

Scheduling is one of the central tasks in high level synthesis, it consists on partitioning the design behavior into control steps such that all operations in a control step execute in clock cycle. We consider the problem of scheduling descriptions represented by control flow graphs.

Path-based scheduling algorithms (PBS) have proved themselves to be much more efficient than classical approaches when dealing with descriptions of control-flow dominated circuits. The first application of PBS to synthesis was made by Camposano and was based on algorithms first proposed for microcode compaction.

**Results:**

Around PBS, we have developed two heuristics named Dynamic Loop Scheduling (DLS), and Pipeline Path-based Scheduling (PPS). DLS comes to reduce the complexity of PBS which is exponential, by resolving the problem of path explosion by cutting the path on the fly. PPS concentrates on optimizing the execution of loops. In real time applications, loops are the most time critical part. PPS uses a new technique for pipelining loops in order to identify any parallelism that may exist beyond loop boundaries.

II-5.2.2 Interactive behavioral synthesis

*Member: W. CESARIO, Z. SUGAR, R. SUESCUN, I. MOUSSA*

The goal of this work is to make behavioral synthesis flexible and practical for architecture exploration.

The central objective of this work is to give support for a flexible hardware synthesis flow. This flexible flow is essential when hardware synthesis process could benefit from the designer’s expertise. Designers’ productivity will boost if we provide tools that allow them to interfere on the synthesis process only when/if they find it necessary. Current CAD tools for hardware synthesis are in almost all cases “push-button” style, i.e., they restrict designer intervention to the task of giving the designing constraints to be used in the synthesis process. Our adaptable synthesis tools enable the use of a modular and flexible design methodology (see Figure II-5 1). This flexibility has three axes: the design flow, the datapath and the controller. It adds one degree of freedom in the design process by giving the designer the possibility of choosing the tools and their sequence to define an appropriate synthesis path.

Design flow flexibility is supported by tools we have done for the new AMICAL high-level synthesis system (hatched in Figure II-5 1). They could handle all the different design paths represented in Figure II-5 4. Micro-scheduling also works with a design only partially treated by the resource allocation/binding module. Datapath flexibility is provided by connection allocation/binding module: it will produce bus-based and mux-based datapath styles. We have already demonstrated how important is the choice of the interconnection scheme in the final synthesis result. Now, we want to show that the capacity of choosing tools/synthesis paths will also play a fundamental role in the quality of the synthesis results. Finally, controller flexibility allows the utilization of totally/partially specified datapaths and even previously synthesized ones.
Results:

Experimental results have shown that the quality of the synthesized datapath (using the traditional design flow) is in great part dependent of the interconnection scheme used. Interconnect optimization directives are present in the allocation/binding and micro-scheduling modules since these problems are strongly related. In a more general way, the quality of the resulting design will depend on the style of the FSM/datapath model and the level of integration with the RTL synthesis tool. Better integration could be achieved using our flexible design flow and our design model, which will lead to better synthesis results. In terms of productivity, an important aspect is IP reuse. If possible, proved and tested datapaths should be reused in other systems which different specifications to reduce the design cycle time.

II-5.2.3. Linking behavioral synthesis with existing CAD environments

* Member: R. SUESCUN, Z. SUGAR

The goal of this work is to define methods and tools in order to ease the link between AMICAL and existing CAD environments. This work addresses three tasks:

* Generation of efficient RTL VHDL for lower level synthesis. Experiments have shown that the quality of the behavioral synthesis depends heavily on the quality of the RTL produced.

* Generation of understandable RTL VHDL. This is mandatory in order to allow the designer to understand the produced solution. Most existing behavioral synthesis tools produce unreadable RTL models.

* Link the RTL model to the initial VHDL description. This is needed in order to allow for interactive synthesis scheme.

Results:

This work constitutes the back-end of AMICAL. Several tools have already been developed and used for the synthesis of real-life designs.
II-5.2.4 Behavioral synthesis for structured design methods and design re-use

Member: I. MOUSSA, E. BERREBI, J. FREHEL

In order to cope with designs of increasing size and complexity, it is then clear that we need improvements of the design quality and designers' productivity. This may be achieved in two ways that can be combined:

1) Using more structured design methodologies for an extensive re-use of existing components and sub-systems. It seems that 70% of new designs correspond to existing components that cannot be re-used because of a lack of methodologies and tools.

2) Providing higher level design tools allowing to start from a higher level of abstraction. After the success and the widespread acceptance of logic and RTL synthesis, the next step is behavioural synthesis, commonly called architectural or high-level synthesis.

The goal of this work is to combine structured design methodology and AMICAL in order to design complex heterogeneous systems.

Structured design methodology allows to handle very complex design with hierarchical approach. Hierarchical design proceeds by partitioning a system into modules. The implementation details of these modules are hidden. Proper partitioning allows independence between the design of the different parts. The decomposition is generally guided by structuring rules aimed to hide local design decisions, such that only the interface of each module is visible.

The design of complex modules such as an integrated system on chip may need the use of different behavioral synthesis tools corresponding to the different functions implemented by the system. Complex and intensive data computation may need throughput oriented synthesis tools such as cathedral whereas the design of complex control function is made using AMICAL. Of course the system may include blocks described at the RTL and netlist level.

Results:

Several complex designs have already been designed using this approach. A motion estimator circuit has been designed using AMICAL. This design makes use of 2 memories with sophisticated protocol and a DSP processor designed by CATHEDRAL. An ATM shaper circuit has also been designed. The shaper includes 2 million transistors and is composed of 6 complex functions that required the invocation of behavioral synthesis.

II-5.2.5. Programmable architecture design

Member: C. LIEM, F. NAÇABAL

This work is concerned with methodologies for the development of new ASIP architectures. Starting from a set of behavioral level descriptions of typical functions for the application domain, the objective is to determine an instruction-set optimized for the application. In turn, this instruction-set implies the definition of the data path programme sequencer, memory structure, peripherals, etc.

Given that a compiler maps an application to a processor architecture, the compiler could be used as an analysis tool to develop better architectures in the areas of data or control-flow efficiency. The instruction-set of an ASIP is the hardware/software interface and the level at which many trade-offs between speed, flexibility, hardware complexity, and compiler efficiency can be made.
This work looks at applications from a compiler perspective in an attempt to characterize the hardware resource needs for efficient functionality. Naturally, these analyses also lead to better code generation approaches.

Results:

An array transformation prototype has been developed and tested with an existing compiler system. Initial results for a set of DSP benchmarks are very encouraging: 23% code-size reduction and 39% speedup.

II-5.2.6 Behavioral synthesis for low power

Member: Ph. GUILLAUME

The goal of this work is to deal with power issues at the early stage of the design, i.e. during architectural synthesis. While the largest gain is expected at the architectural level, the estimation is most critical here. The goal is to take into account the power consumption evaluation and optimization during the early stages of the design process. At this level the library elements are large cores and complex macro-blocks. We need a macroscopic model for power. Our approach considers the number of switching elements in each library element for each clock cycle. Besides, each component is characterized by a switching level when Idle. This model allows to estimate with a large precision the power consumption at the clock cycle. The dynamic nature of power consumption can also be handled by using a kind of power simulation at the clock cycle level. We are planning to use this estimation for guiding the synthesis process in order to select the best solution (allocation, scheduling) in terms of power.

II-5.3 Multilanguage design

Member: M. ROMDHANI, F. HESSEL, Ph. LEMARREC, P. COSTE, C. VALDERRAMA

The design of a complex system may require the cooperation of several teams belonging to different cultures and using different languages. New specification and design methods are needed to handle these cases where different languages and methods need to be used within the same design. These are multilanguage specification design and verification methods.

The main problems of multilanguage specification are:
1. How decide the best-suited paradigm for each part of global specification,
2. How to compose these subsystem specifications in a unified format suitable for codesign,
3. How verify if the subsystem specifications and the unified format correspond with the requirements and contrain of global specification.

Most codesign systems starting from abstract level using a single language for specification. Several systems specification languages have been used: VHDL (COBRA system), FDS (PTOLEMY system), HardwareC (VULCAN II system), SDL (COSMOS system) and SpecCharts (SpecSyn system). Few recent codesign tools are based on multilanguage. However they generally start from a low-level prototype when Hw/Sw partitioning is already made. Most of these systems start from C-VHDL (COWARE, EAGLE I) or C-Verilog. The only systems that start with a multilanguage paradigm are the new PTOLEMY version with the Star Model and the RAPIDE environment. The first is still restricted to DSP applications.

The specification of such large design may lead each group to use a different language which is more suitable for the specification of the subsystem they are designing according to its application domain. In this case, the problems of interfacing and multilanguage validation need to be solved.
There are two main approaches for multilanguage validation: the compositional approach and cosimulation based approach.

The compositional approach (Figure II-5 5) aims at integrating the partial specifications into a unified representation that is used to the verification of the global behavior. This allows to operate full coherence and consistency checking, to identify requirements traceability links, flexibility, and to facilitate the integration of new specification languages.

The cosimulation is an engineering solution to multilanguage validation that performs just a shallow integration of the partial specifications. The cosimulation based approach consists in interconnecting the simulation environments associated to each of the partial specification.

Figure II-5 5 - Multilanguage Composition  Figure II-5 6 - Multilanguage Cosimulation

The goal of this work is to provide:

1. Modeling strategies allowing to compose existing language for complex systems specifications. The goal is to be able to use the same specification for cosimulation and cosimulation.
2. Methods and tools for codesign starting from multilanguage specification. We will use Solar as a unified format the specification of language composition and as an intermediate model for codesign.
3. A distributed cosimulation environment will be developed for validation. The goal is to run concurrent specifications dedicated simulator for the simulation of the different modules. The inter-simulator communication will be generated automatically starting from the composition model.

Results:

We already developed XXI, a distributed cosimulation tool. This approach is based on a communication network protocol that is used as a cosimulation bus. Each simulator communicates with one another through of the cosimulation bus. The cosimulation bus is in charge of transferring data between the different simulators and your implementation was based on standard system facilities, typically using UNIX socket-based communication.

The XXI tool takes as input a user defined configuration file (Figure II-5 2), which describes the interfaces between the partial specification. This file is described in the SOLAR format. Based on the information provided by the configuration file, the interface generation process produces automatically the interface between the subsystem and the cosimulation bus, enabling the different tools to cosimulate.

The current version of XXI allows parallel-execution of SDL-C-Matlab-VHDL simulators and it is possible to run on a single CPU or across networks on different platforms without additional implementation effort.
II-6 Verification and Modeling of Digital Systems (VDS)

Group Leader: D. BORRIONE
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Members: D. BORRIONE, H. BOUAMAMA, J. DUSHINA,
C. LE FAOU, J. MERMET, A. MORAWIEC,
P. OSTIER, F. VESTMAN, G. VITRY, A. WAHBA

Research areas:

The research activities of this group address:
. the formal verification and diagnosis of design errors in digital systems designs described in
  standard hardware description languages.

Contracts:

CHARME (ESPRIT Basic Research Working Group), MEDEA-SMT, CAPES/COFECUB, DRET

Industrial Partners:

Bull, SGS-Thomson, Thomson-TCS

Topics:

Specification Languages, Hardware Description Languages, VHDL, Verilog, Formal Verification,
Proof of Correctness, Model Checking, Automatic Diagnosis of Design Errors

II-6.1 Formal verification from standard hardware descriptions

Members: D. BORRIONE, H. BOUAMAMA, C. LE FAOU, P. OSTIER, F. VESTMAN

The inclusion of integrated circuits in safety-critical applications requires that the correctness of
hardware (and hardware/software) designs be ensured by rigorous methods. Moreover, the cost of
design iterations, and the loss of market shares in case of late detection of errors makes it mandatory
to achieve error-free designs. While simulation is still the most commonly used validation
 technique, the application of formal methods can provide a valuable alternative, by ensuring
complete correctness (and not correctness of test cases considered representative of all the possible
ones), and by freeing the designer from the time-consuming development of stimuli and
interpretation of simulation results.

The objective is to develop mathematical models and verification techniques that can prove the
correctness of a design, and provide automatic diagnosis when design errors have been proved to
exist. Many aspects of hardware behavior have to be considered, and no single verification
paradigm can apply to all of them: so we consider binary equivalence checkers at logic level, as
well as general purpose theorem proving at more abstract levels for the proof of correctness;

1 Until June 1997
2 Since November 1997
symbolic model checking as well as theorem proving for the proof of properties. In order to include formal verification in the design methodology, as a complementary technique to the other usual CAD tools, standard HDL inputs must be accepted. Our group has been one of the first to promote the formal verification of VHDL descriptions, and is very much involved in the VHDL standardization activities. In 1997, we started a theoretical study of the Verilog semantics, in view of proposing a unified semantic model for VHDL and Verilog.

II-6.1.1 The PREVAIL environment

PREVAIL is a multi-HDL, multi-tool formal verification environment, which presents to the designer a unified interactive graphical user interface (see Fig. II-6.1). It is the result of a cooperative effort between Université de Provence - Marseille, Université Joseph Fourier - Grenoble and Technische Hochschule Darmstadt (Germany).

![Figure II-6.1 Architecture of the Prevail system](image)

Initially, two HDL's could be used as input language: SMAX and VHDL. SMAX had been designed in Darmstadt using the CONLAN definition method (which includes formalized syntax and semantics); it was specially intended for reasoning at the bit-vector level, with appropriate first order logic semantics, on combinational circuits and synchronized unit delay Finite State Machines (FSM). It is semantically equivalent to a subset of VHDL. With the standardization of Verilog, and the general adoption of standard languages in design teams, non standard languages such as SMAX have progressively been abandoned, despite their sometimes better qualities.

As in most verification systems with a VHDL front-end, only a subset of the standard VHDL is recognized. Basically, the "P-VHDL" subset of PREVAIL corresponds to a synthesizable subset
extended with generic parameters. No effort has been made to conform to a particular synthesis tool subset; rather we kept or discarded each construct based on its semantic expressiveness, trying to retain as large and consistent a subset as possible.

The underlying common semantic framework is the Finite State Machine model, with repetition, hierarchy, and genericity. All types are assumed to be discrete (including integers and enumerated symbolic types, and arrays). Generic models are models where the number of sub-components or the data path width is kept a parameter. Hierarchical models must be fully configured.

In PREVAIL, a "Proof-oriented Internal Format" (PIF) is the data structure representing the common scheme mentioned above. The SMAX Intermediate Format is a subset of PIF (for instance, PIF includes repetitive statements, which must be formally expanded in the SMAX Intermediate Format). The environment can be extended to other HDL's, either by providing source to source translators, or by implementing source to PIF compilers.

Due to the modest size of our group, we decided to use existing compiler front-ends, whenever possible. Thus in 1997 PREVAIL relied on the SMAX compiler from Darmstadt, and the VTIP\(^1\) software for VHDL'87. These two front-ends will be abandoned in 1998, due to the lack of support of their original developers.

The next version of PREVAIL will replace VTIP by LVS\(^2\), with the advantage that LVS parses VHDL'93. Both VTIP and LVS produce an internal data structure that can be browsed using a library of functions; however, these two data structures are significantly different, and our initial attempt to use the same overall compiler to produce the PIF structure from either VTIP or LVS using a switch proved to be inefficient. A complete re-design of VHDL2PIF, our proprietary second level compiler front-end, is necessary.

II-6.1.2 Verification tools at logic level

Several proof systems are embedded in the PREVAIL environment. The control of the verification steps and the selection of the appropriate prover are the responsibility of the designer.

LOVERT is both a tautology checker, and a FSM equivalence checker, implemented by the group of H. Eveking (at Technische Hochschule Darmstadt) on the principles of Coudert and Madre (when they were at Bull). LOVERT was the first verification tool included in PREVAIL, several years ago, and is mentioned here for completeness. It is built over an OBDD package developed at Technische Hochschule Darmstadt. Like all BDD-based tools, it applies to components where generic parameters, if any, have been fixed to constant values.

SMOCK is a proprietary symbolic model checker inspired by the seminal work of Ed Clarke's group (at Carnegie-Mellon University), which checks formulas written in CTL-P, i.e. CTL extended with modalities looking back to the past. SMOCK is built over the same OBDD package as LOVERT. The work on SMOCK started in 1992, and the development ended in 1994.

The performance of these tools can no longer compete with that of verification software built on the top of more modern BDD packages. Logic level verification has now become available on the industrial market, and is no longer a topic in which we feel we can make a significant contribution. Our approach is now to establish links with efficient freely available verification tools, based on sound semantical analyses, as discussed in section II-6.1.5 below.

\(^1\)VTIP was distributed by Compass, now Avanti!
\(^2\)LVS is distributed by Leda
II-6.1.3 Verification by theorem proving

When specifications are given by arithmetic functions, or when the object to verify is a parameterized function or library module that must be proven correct for all admissible values of its parameters in an unbounded set, elaborate reasoning capabilities, including induction, are needed. To this end, the NQTHM general purpose theorem prover of Boyer and Moore has been integrated in PREVAIL. We chose this system for its powerful proof strategies, and its capabilities to handle large hardware proofs automatically.

The current translator is applied to behavioral descriptions, and imposes restrictions on procedure and loop statements. It transforms VHDL subprograms and processes to a functional representation within the logic of Boyer and Moore extended with the "Ground-VHDL-Logic". "Ground-VHDL-Logic" is a library of shell definitions, functions and lemmas, built on top of the "Ground-Zero-Logic" which comes with the prover; it models the VHDL primitives and their characteristic properties. Its definitions and lemmas are part of the object code of the PIF2NQTHM translator.

II-6.1.4 Automatic diagnosis

When a design has been found erroneous, the designer faces the difficult and time consuming task of locating and correcting the error. We have developed prototype automatic diagnostic tools for logic level designs, which locate the error and suggest a correction with a 100% hit ratio in the case of a single component or connection error: CCDS is the diagnoser for combinational circuits, and SCDS for sequential circuits. Section II.6.3 discusses the diagnosis of design errors.

II-6.1.5 Verilog-VHDL interoperability

With the advent of both VHDL and Verilog as standard hardware description languages, designers face the problem that different groups of people prefer one or the other language, and two concurrent communities have emerged, which can hardly communicate and benefit from the work of the other. In particular, big designs require to re-use previous models. It should be possible to re-use a sub-circuit independently of the HDL in which it is written. Previous efforts to provide automatic translation from one language to the other are based on syntax-directed techniques, and impose very strong limitations on the source description. Yet, both language reference manuals and all users oriented books give simulation semantics in words, and the task of deciding whether two descriptions will always give the same behavior is far from obvious.

We started to tackle this problem from a semantical perspective, with an emphasis on ensuring the compatibility between synthesis and simulation semantics. Our objective is to establish firm grounds for the definition of RTL synthesis subsets, and allow the formal verification of model equivalence, where one description is written in VHDL and the other in Verilog. We thus restrict ourselves to the modeling of the current de facto "synthesizable subsets" of both Verilog and VHDL, while participating to the IEEE working group which defines the standard synthesizable subset of VHDL.

To ease the manipulation of structured designs, and put the emphasis on component re-usability, we chose as basic model a hierarchical finite state machine model (HFSM for short): it extends the Mealy FSM model with the existence of local variables, transfer functions to the local variables, and the notion of embedded local HFSM's (a Mealy machine is a flat simple case HFSM). The extraction of the HFSM model of a Verilog description is relatively straightforward; it is more difficult from VHDL, due to the lack of syntactic distinction between registers and wires. We have defined a set of writing rules, and an algorithm, to guarantee the identification of the minimum number of memorizing variables in a VHDL description.
The central role of the semantic representation is shown in Figure II-6.2. The HFSM models of a description #1 written in VHDL and of a description #2 written in Verilog are first extracted. A BDD representation of these models can be constructed, which allows their equivalence verification. Either model can also be expanded to the input format of a logic synthesis tool, which produces a logic network; the synthesis result is translated back into a flat FSM model which can be translated back into either Verilog or VHDL source.

The data structure to represent the HFSM model is a restriction of PIF that we call "SMP", where all generic parameters (if any) are instanciated, and loops are unrolled. To demonstrate our ideas, we implemented a first partial translator from SMP to Blif-mv, the input format of Berkeley's VIS system, which takes Verilog as input. This notably gives the possibility to have a VHDL input to VIS, and to verify the equivalence of two descriptions, one written in each language. The current prototype takes scalar data types. Its extension to vectors is rather complex, due to the lack of memory declarations in VHDL; it is an on-going effort.

II-6.2 Formal verification of high-level synthesis results

Members : J. DUSHINA, D. BORRIONE

Large designs increasingly rely on the inclusion of previously designed sub-components, and on the use of high-level synthesis tools. It is therefore of utmost importance that the components being reused be thoroughly verified, and that formal methods be developed to proof-check the very first steps of high-level synthesis. This is the purpose of this research, which takes as high-level synthesis case study the Amical system, and is therefore conducted in close cooperation with the "System Level Synthesis" group of TIMA.

The initial HW/SW system description is assumed to be given by an abstract algorithm (written in behavioral VHDL in our case), where variables hold mathematical values for which no encoding is
yet defined, and "execution steps" are not yet given a fixed number of clock cycles. We have defined a model, called "FSMC" (Finite State Machine with Co-processors), which is an extension of the Finite State Machine with Data-path model conventionally used in high-level synthesis, to represent the hierarchical decomposition of a specification in terms of a network of co-processors with decentralized control. The formal definition of a FSMC extends the traditional Finite State Machine (FSM) model with an abstraction of the notion of state (Abstract State Machine, ASM), whereby the state of the operative part is kept symbolic, and only the state of the control part is being traversed. The first high level synthesis steps produce an abstract architecture, which is explicitly modelled as the product of two models: a FSM for the control part and an ASM for the operative part, interconnected by commands and status signals.

Rather than prove globally that the synthesis result implements the behavioral specification, which would lead to the creation of huge conditional expressions, we perform the verification on a step by step basis. At each control step, the commands generated by the control part are interpreted in the data path to produce the symbolic expressions of the register, status and output assignments performed in the operative part. These symbolic expressions are compared against the specified ones. A first partial prototype, taking as input the Solar intermediate form produced by Amical from a VHDL specification, has been implemented in Prolog.

II-6.3 Automatic diagnosis of simple design errors

Members : A. WAHBA, D. BORRIONE, H. BOUAMAMA

Automatic diagnosis is a natural complement to formal verification. When an implementation is found to be erroneous, most advanced verifiers provide counterexamples, in the form of input patterns that witness the error. The tedious work of finding the error and correcting it is left for designers, who use these counterexamples to simulate their designs. The place of the diagnosis in the design life cycle is shown in Fig. II-6.3.

![Diagram](https://via.placeholder.com/150)

**Figure II-6.3 - The place of the diagnosis in the design life cycle**

We have developed two prototype tools to automatically locate the error, and propose a correction in bit and bit-vector level designs: CCDS (Combinational Circuits Diagnostic System) and SCDS (Sequential Circuits Diagnostic System). The specification may be described in any style. The implementation is assumed to be a logic network.

Both tools are composed of three cooperating basic modules (see Fig. II-6.4): a generator of special
a three valued logic simulator and a diagnosis engine that contains all the diagnostic rules.

Figure II-6.4 - The three basic modules of the diagnosis system

The principle of the diagnosis algorithm is as follows. Initially all the circuit gates are suspected (i.e. the error may be situated at any gate). The pattern generator selects one of these gates and generates a special pair of test patterns for it. This pair is sent to the simulator, and the specification and the implementation are simulated. The simulation result is sent to the diagnosis engine, that applies the diagnosis rules to limit the number of suspected locations. The reduced set of suspected locations is then sent back to the pattern generator which, in turn, selects another suspected gate and the whole operation is repeated, until the error is located precisely.

II-6.3.1 Error model and basic assumptions

Simple design errors, classified into gate errors and connection errors, are summarized in Table II 6.1. The simple design error assumption is not appropriate for debugging synthesis software. But in the case of manual modifications (fine level optimizations, or manual "patches" due to late changes in the specification, which are still common), this hypothesis is relevant.

CCDS can diagnose both classes in combinational circuits. SCDS treats only gate errors in sequential circuits. These tools work under the following assumptions:

1. One error, at most, exists in the cone of influence of each primary output.
2. The error is one of the types listed in Table II-6.1.
3. The implementation is given as a network of single output components (of which elementary AND, OR, NOR, NAND, XOR gates are special cases); but libraries of complex gates (AND-OR, AND-NOR ...) are also admissible.
4. The error does not introduce extra loops in the implementation.

The diagnosis problem in its general form is known to be NP-complete. To limit its complexity, we use the principle of the diagnosis by error hypotheses. An error type is assumed and the diagnosis is made considering only this type. If the error is not found another type is selected and so on, until the error is found.

The backbone of the diagnosis algorithm is the backward propagation technique. The implementation is simulated under the application of the specially generated test patterns, and it is then scanned from its primary outputs back towards its primary inputs. Diagnostic rules are applied during this scan to limit the number of gates to examine and the number of suspected locations of the circuit.
Table II-6 1. Simple Design Errors

In 1997, the extension of the CCDS prototype to process complex gates read from a library was completed, and the performances of the new tool were re-evaluated on the ISCAS benchmarks. Thousands of experiments were made with a randomly replaced simple or complex gate. In all the experiments the error was found after the application of a small number of test patterns, and it was found that the unified diagnostic method generalized to complex gates was more efficient than the previous method where patterns specialized to each elementary gate type had to be generated. Details can be found in the PhD thesis of Ayman Wabba.

In addition, our group acted as advisor to student projects, where the objective was to re-program parts of the Prolog prototype in C++. Preliminary experiments showed that between one and two orders of magnitude reduction could be expected in the execution time of the simulator; conversely, the performance improvement of the diagnosis engine was small.

II-6.4 Formal verification in practice

Members : J. MERMET, A. MORAWIEC

II-6.4.1 Survey of formal hardware verification tools developed in Europe

A survey on hardware formal verification tools developed in Europe has been established in the project supported by DGA/DRET. This survey gives an overview of the formal methods used in the most significant European research works in this domain. It introduces a classification scheme for the existing commercial or prototype verification tools, which is based on the different verification aspects: type of the circuit to verify, abstraction level, verification objective, mathematical model, formal proof technique, input formalism, diagnostic method incorporated and the others. The most significant features of the methods and tools are summarized, and some advantages and drawbacks are discussed in the related publications.

The work on the survey was funded by DRET Project N 96-050.
II-6.4.2 Abstraction of VHDL models towards system level

The objective of the work is to automatically generate the abstraction of the VHDL models in order to move the design description to the system level and to improve the design/simulation performance. The model transformation for abstraction purposes will proceed in two steps:

1. Optimisation of the VHDL model.
Here the initial VHDL model is translated to an equivalent VHDL model which is simplified and optimised. The optimisation consists in replacing inefficient hardware description language constructs by more efficient ones from the simulation time perspective. Also some modelling optimisations can be performed to improve the simulation performance of the model (e.g. appropriate partition of the design into processes, sensitivity list construction, use of shared variables for internal buses, removal of intermediate signals and variables where possible, etc.). Some programming language concepts for improving performance can also be successfully used like in-line functions or loop unrolling.

Formal hardware verification methods are adjusted to prove the equivalence between the initial and the optimised model. Two categories of formal verification will be performed: (1) definitive verification that a particular abstraction mechanism provides a functional implication of the original description; (2) dynamic equivalence checking for ad hoc and specific transformations.

2. C++ Model Abstraction.
From the previously optimised VHDL model, a C++ model is generated which abstracts the functionality without losing simulation performance. The C++ hardware model of the system can cooperate with the system's software part described using the same language. The VHDL concepts like signals and types are implemented as corresponding C++ classes. The following abstraction mechanisms are explored:

1. Structural abstraction: the internal structure of the design is not of interest for the designer at the higher level of abstraction where only the external behavior of the design might be observed. The components (modules) of the designs are merged together while preserving only their functionality and removing all component interface details.

2. Temporal abstraction
   a. Functional model: The model can be abstracted by separation and removal of detailed timing information (introduced e.g. in VITAL models). The model preserved the initial functionality of the design.

   b. Cycle based model: the design is partitioned into a combinatorial and a sequential part. The combinatorial part is optimised to decrease the number of events to be handled in the simulation. In particular delta-delays are removed from the model.

   c. Cycle accurate model (machine instructions): the basic time granularity is the execution of a single processor instruction (this execution can consist in several clock cycles and phases).

3. Data abstraction: it consists in replacing all low level data types and operations used at the implementation level of the design by more abstract concepts. As an example, comparison and arithmetic operations on bit vector types can be replaced by integer operations.

The application of Decision Diagrams as a high level design data representation will be explored to be used for efficient evaluation of the function of the design. Also an interface between the HW and SW parts will be investigated.
II-7 Qualification of circuits (QLF)

Group Leader: R. VELAZCO
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Members: Ph. CHEYNET, M. OLMOS, J.C. RUBIO, S. REZGUI,
F. PERRENOT, J.G. RIOUX, A. BOFILL

Research areas:

This research group addresses the following topics:
+ methodology and tools for test under radiation
+ design hardening of circuits devoted to space applications
+ design of experiments on board satellites
+ digital implementation of intelligent control (fuzzy logic, neural nets)

Contracts and projects:

CNES, CEA/DAM, MPTB (Microelectronics and photonics Test Bed), STRV (Space Technology Research Vehicle), ALFA (America Latina Formation Académique, CAPES-COFECUB.

Topics:

Testing and qualification of integrated circuits, test in harsh environments, radiation tests, design hardening with respect to Single Event Upsets, digital implementation of intelligent control strategies, study of the robustness of fuzzy logic and artificial neural network approaches, design and exploitation of on-board satellite experiments.

II-7.1 Summary

The QLF group has joined TIMA in 1997. Research activities of the group deal with the study of the behaviour in harsh environment for digital circuit and systems. The main stress considered is radiation of nuclear and space environments, but it is interesting to mention that particles reaching the Earth's surface from the Sun, up to now innocuous for microelectronics circuits, have sufficient energy to flip bits in memories and corrupt logic inside processors for parts manufactured with 0.3 μm and supply voltages drop to less than 2.2 Volts. This can constitute a threat to avionics control systems (at 30,000 feet, the neutron activity is 4 to 8 times higher than the ground), and in the future to systems operating in ground.

One of the important issues of these researches, is the prediction of failures in flight. The refinement of forecasting error rate strategies needs both to perform ground test by means of simulated radiation environment (particle accelerators) and to compare ground test results to data obtained from experiments aboard of spacecrafts. Two different satellite experiments were developed in collaboration with CNES with the goal of studying the behaviour in space of various commercial circuits (COTS) including memories, general purpose microprocessors and dedicated processors. One
of them deals with satellite image texture analysis by means of an Artificial Neural Network designed by CEA/DAM. This experiment is presently on board of a scientific satellite launched November 1997 by Naval Research Laboratories (NRL-Washington). The second one, designed in collaboration with NASA, aims at studying the robustness of a dedicated fuzzy controller (the WARP processor from SGS-Thomson).

One of the critical effects of raduations can be drastically attenuated by a proper design of memory cells. A patent developed at QLF has been transferred to Matra MHS to manufacture a Digital Signal Processor, the DSP/RT, suitable for space applications. Ground tests performed on this circuit have proved its immunity to Single Event Upsets. The DSP/RT will be commercially available mid 1998.

II-7.2 Development of a test bed suitable for the qualification of integrated circuits devoted to operate in harsh environment

Members: R. VELAZCO, Ph. CHEYNET, A. BOFILL

With the miniaturization, integrated circuits become more and more sensitive to perturbations resulting from the effects of the environment (temperature, radiation, EMC,...). This activity concerns the design of a test system which facilitates the realization and exploitation of qualification tests for all kind of circuits, from a simple register bench to complex components such as processors.

Screening tests are mandatory to predict error rates. They consist in exposing the studied parts, eventually operating in vacuum, to simulated stress conditions. The hardware and software developments related with such tests must take into account the random nature of event occurrence, both in time and space. On one hand this entails on-line error detection, on the other hand this makes mandatory the need for development of ad hoc hardware mechanisms related with critical errors detection (sequencing loss, system crashes, latches) and recovering. Most of commercially available functional testers have these capabilities, potentially offering a powerful solution to qualification test implementation for all circuit types. Nevertheless, two main drawbacks must be mentioned:

- functional testers cannot fit inside most of vacuum chambers available at generally used radiation facilities. The alternative consisting in using them outside the chamber connected to the device under test (DUT) inside the enclosure, may lead to serious signal propagation problems,

- test stimuli are defined by a set of binary patterns corresponding to circuit pins values at each clock period. For complex circuits (processors for instance) the development and debugging at this low-level of such test programs can be a difficult task. Note that these constraints may also apply for testing under other type of conditions such as temperature, magnetic perturbation, vibrations, or other type of harsh environments.

We have designed and prototyped a system, called THESIC (Testbed for Harsh Environments Studies on Integrated Circuits) devoted to harsh environment test implementations and particularly to Single Event Effect (upset and latchup) tests. A simplified version of this system is currently used to perform radiation tests qualification for complex parts candidates to space applications of European and American space agencies.

The THESIC system comprises mainly (Figure II-7 1):

- a motherboard, performing the following tasks: control all operation related with the DUT test (power on/off, current consumption control, test stimuli download, starting /stopping test cycles; receiving, pre-processing and transmitting data to/from user interface computer,
• a daughterboard, implementing a suitable architecture where the DUTs will be exposed to
environment effects while exercised by the chosen test stimuli,
• a computer, for user interface (on-line monitoring of test execution, result displaying on
"understandable" format), and memory mass purposes (storing experiment historic for ulterior
analysis).

The motherboard is built around a microcontroller (the 80C51 from Intel). It comprises an EEPROM
where the micro-controller system software is stored, an SRAM for DUTs programs/stimuli and
digital-analog analog-digital converters for DUT’s current consumption or other measurements
monitoring. Note that current consumption limit can be modified during a test experiment (this
condition is mandatory for Single Event Latchup testing, where the latchup threshold is looked for).
Communication with user interface computer is done through a serial link.

The daughterboard, testbed for the DUTs, has a totally free architecture, but must adapt to motherboard
protocol interface. To cope with a wide range of different types, two modes were provided: (a) slave
DUT mode, in which all test operations are performed by the motherboard, and (b) asynchronous
master DUT mode, in which the daughterboard has its own processor (under test or not) programmed
to implement the test strategy including test result transmission to the motherboard (by interruption
activation). In both modes communication is achieved through a memory area resident in
daughterboard (Memory Mapped Interface, MMI) and accessible to the motherboard.

![Diagram of motherboard setup]

**Figure II-7 1 - Building blocks of THESIC, the proposed system for qualification tests**

The first mode is well suited, for instance, to memory testing. The MMI being in the memory space of
the 8051, the execution of an appropriate program allows to easily implement all currently used
memory testing strategies. Note that a register bufferisation allows to extend the 8051 address bus to
16 bits, with the obvious consequences at operating test frequency.

The second mode can be used for all circuits, including memories. The principle is to design a
daughterboard comprising a processor which will ensure DUT test control and communications with
the motherboard by means of asynchronous interruptions. When the circuit under test is a processor,
this strategy has some limitation considering that errors perturbing test control operation can have
consequences difficult to be predicted and/or understandable through the analysis of corrupted data. As
an example, malfunctions leading to sequence loss will result in "black out" situations at the
motherboard level (which during the test is waiting for daughterboard interrumpion indicating power consumption problems or "test results available"). To cope with such critical errors, a programmable software watchdog was implemented in the motherboard.

An example of a THESIS daughterboard designed and developed to test a digital signal processor and a commercial SRAM memory candidates to a Nanosat developed by INTA (Spanish Space Agency) is given Figure II-7.2.

![Figure II-7.2 - Block diagram of the DSP daughter board](image)

A particular effort was invested on the development of friendly and powerful user interface capable to provide the operator with on-line test result data. Indeed, getting comprehensive information about detected errors is essential to efficiently reoriented a given experiment depending on collected pre-processed information. For instance, in radiation tests, changed in beam energy or fluencies may be required depending the abundance of errors, thus avoiding expensive needless beam time.

A snapshot of a significant Thesic screen is given Figure II-7.3. The main window is devoted to motherboard configuration (threshold current consumption, watchdog time-out period) and to dispatch DUTs information about errors to appropriate sub-windows. Statistics about detected errors are permanently displayed (upper right corner). Two significant and original features of the developed user interface are: (a) the on-line visualization for representative indicators of DUT sensitivity to the studied environment, and (b) the possibility of replaying a given test session. Sensitivity to radiation is generally given as a "event cross section" curve, representing the number of error (normalized by the particle fluency) vs. particle energy. Such curves can be displayed and updated in real-time offering powerful insight on the behavior a the tested component (lower left window).

The replay function (upper-left window) makes possible to analyze off-beam the occurrence and location of errors occurring during a particular test experiment.

We have chosen to illustrate in an eloquent manner this project by means of a picture taken during its use on the field. Photo depicted in Figure II-7.4, shows the THESIS hardware within the vacuum chamber available at the cyclotron 68" of LBL facility. The motherboard shown in the background is fixed to a moving stage support allowing to perform the alignment DUT-beam. It communicates to an external PC through a serial link connection. The daughterboard, in the foreground, was designed to evaluate the behavior under radiation of an architecture built around a Transputer, a neural co-processor and different SRAMS. During a radiation test, target DUTs are successively aligned with the beam.
II-7.3 Memory cells suitable for the design of SEU-tolerant VLSI circuits

Members: R. VELAZCO, M. NICOLAIDIS, T. CALIN, J-G RIOUX

Manufacturing SEU-immune circuits using standard CMOS processing with no additional masks is the main goal of design hardening techniques. The basic idea is to provide memory elements with an appropriate feedback devoted to restoring data when corrupted by an ion hit for instance. Obviously, the main problem is how to organise the extra transistors used to realize this feedback, that will result in new sensitive nodes, without affecting the latch SEU sensitivity.

The major advantage of design hardening is to preserve latch write speed, other approaches such as resistive hardening, seriously degrades latch performances, particularly at low temperature. Compared with SOI and SOS technologies, design hardening does not require new fabrication processes or masks.
We have designed a new SEU-tolerant memory cells, called HIT cell (Heavy Ion Tolerant cell). During the design phase the following criteria were considered:
- the memory cell should be used without any additional buffer, to build data latches as well as SRAMS,
- the number of transistors should be minimized,
- static power consumption has to be reduced,
- recovery time after upset should be short,
- total dose effects must be taken into account.

THE HIT CELL

The HIT cell is composed of 12 transistors organized as two storage structures interconnected by feedback paths. To cope with single upsets specific transistor ratios were used. The read/write operation needs a single phase read/write clock R/W and differential inputs D and D'. The output Q and its complement Q' are both available. Read operations are performed by precharging to VDD data lines D and D'. To modify the state of the cell, the read/write signal should go high while the new values 0 and 1 are presented respectively at inputs D and D'.

The electrical scheme of the HIT cell is given in Figure II-7 5. Starting from the logical state shown in Figure II-7 5 (output nodes Q and Q' are assumed to be at 1 and 0 respectively), it is quite easy to show that the HIT Cell operates as a memory element, (it can perform memorisation and write and read operations) tolerating single perturbations (upsets) on each of its sensitive drains (Q, Q', L and M) and double upsets on drains Q, Q'.

![Diagram of the HIT cell](image)

**Figure II-7 5 - The HIT cell memory**

A test chip including five register banks built respectively from standard memory cells, HIT cell and, design hardened memory cells proposed in the literature was designed. The circuit, manufactured by Thomson-TCS, has been validated using the heavy ion facility available at Lawrence Berkeley Labs (Berkeley, USA). Experimental results confirmed the immunity to SEU of HIT cells.

The HIT cells have been transferred to Matra MHS for the design hardening of a Radiation Tolerant Digital Signal Processor (DSP/RT). This circuit, presently commercialized by TEMIC, was obtained by replacing by appropriate versions of HIT cells, all the memory elements of the ADSP 21020 (Digital Signal Processor from Analog Devices). Radiation tests performed in collaboration with the

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1 French patent n° 093/03333, 18 March 1993
ESA proved that this strategy allows to achieve a very high SEU tolerance for a circuit manufactured using a standard CMOS process.

Current projects of QLF group include the study of a new design hardened memory cell, suitable to be implemented in circuits manufactured by means of sub-micronic process.

II-7.4 Study of the behaviour of digital implementations of intelligent control in space: development of on-board satellite experiments

Members: R. VELAZCO, Ph. CHEYNET, M. OLMOS, F. PERRENOT

Artificial neural networks (ANN) are adaptive and redundant information processing systems that offer attractive solutions to problems sometimes difficult to be tackled by classical approaches. The main goal of this project is to provide data showing that, due to the intrinsic robustness of neural network approaches to the space radiation environment, image texture analysis can be achieved directly onboard the satellite by means of ad hoc neural digital implementations. On-board image processing could be the preferred solution to some communication issues, such as limited bandwidth. We have considered an actual problem: on-board satellite classification of SPOT image textures in four classes (industrial area, residential area, scrubland, sea) of which examples are given Figure II-7.6:

![Image of four textures: "Garrigue", Sea, Industrial Area, Residential Area]

Figure II-7.6 - Examples of the four different textures to be recognised

Calculations needed to evaluate the response of a given neural network can be performed either using general purpose computers or by dedicated hardware either digital, analog or hybrid. The advantages of digital neural implementations over analog ones are the flexibility (the network parameters and/or structure can be modified without modifications to the hardware), the accuracy (practically unlimited in digital and 4 bits equivalent in analog) and the noise immunity (analog implementations are sensitive to voltage drops). Presently, many commercially available circuits are capable of dealing with real-time constraints required by on-board satellite processing for problems, such as image analysis, for which the neural approach provides an efficient solution.

The natural redundancy of neural networks and the form of the activation function of neuron responses, make them somewhat fault tolerant, particularly with respect to perturbations in synaptic weights or input patterns. Most of the published work on this topic demonstrated this robustness by injecting limited (gaussian) noise on software models. Our work has shown that this robustness can be extended to single-event upsets (SEU) induced on the network parameters and/or input data. Ground tests performed on digital architectures comprising general purpose micro-processors as well as dedicated neural processors, have confirmed this SEU tolerance.
The neural network for SPOT image texture analysis, designed at CEA/DAM and trained with a standard algorithm (Back-Propagation) on a training set of 10,000 input images, was implemented on a digital architecture consisting of a Transputer (RISC microprocessor from INMOS / SGS-Thomson with parallelism capabilities) and a dedicated neural coprocessor (the L-Neuro 1.0™ chip from Philips). Figure II-7 7 gives the main features of the board architecture. The Transputer executes a program which mimics the network structure, preparing data needed to compute the state of each neuron. The weighted sum calculations are performed by the L-Neuro 1.0 coprocessor, having previously loaded its internal RAM with the necessary data (weights, thresholds) and the internal registers with the state of the input neurons.

To obtain ground test data on the network robustness, we have irradiated those circuits of the board where information related to the network operation is stored. The main SEU-sensitive area was the memory portions where network program, parameters or inputs are stored. Performed heavy ion tests have shown that: (i) the particular neural network used is robust (90% of upsets are tolerated) with respect to upsets which makes it suitable for on board satellite image processing, (ii) some upsets (4% in the studied case) improve the performance in a significant way. Retraining the neural network with a Metropolis algorithm taking into account the addresses of those particular bits leads to more robust networks, (iii) the quasi-immunity with respect to accumulated upsets on input patterns, makes possible the use of SRAMS, (even if very large areas should contain significant data), and (iv) upsets on the program code itself are tolerated to some extent (20%), but this property could be a result not related to the neural networks, but probably to the processor used to implement it.

![Figure II-7 7 - Experiment block diagram](image-url)

Two «neural experiments» designed at TIMA, in collaboration with the CNES (French Space Agency) and the CEA (French agency for Atomic Energy) were included in a project of Naval Research Laboratories (Washington D-C): the «Microelectronics and Photonics Test Bed (MPTB)». An American scientific satellite holding 24 experiments devoted to evaluate the behavior of modern electronic and photonic devices, 2 of them being the neural boards of TIMA, was successfully
launched in November 1997. The goal of the TIMA experiments is to obtain data about the behavior in real radiative environment of the neural boards implemented by means of commercial circuits. The results of the MPTB project could allow a more wide use of neural network approaches in space. The neural boards will process the contents of images taken by SPOT satellite, looking for the 4 predetermined textures above mentioned. All deviation between the expected and the actually identified textures will be transmitted to the Earth for remote analysis. As SPOT image comprises typically 300 million pixels, its partial processing on-board satellite will drastically improve its utilization, particularly for applications such as measuring the extent of natural catastrophes (earthquake, flood) or tracking a cyclone, for which real-time cartography can be effectively provided by neural networks. The two experiments designed by QLF group can also be used to evaluate the behavior of other programs (based or not on neural network approaches). Indeed, one of the constraints was the possibility to reprogram (by sending the appropriate commands and data from the Earth control) one or the two boards on-board MPTB satellite. Researchers who would like to exercise data processing strategies in harsh environment are invited to contact the TIMA laboratory to analyze and eventually adapt their problems to the MPTB "space laboratory".

The MPTB project was successfully launched November 1997. Analysed telemetries proved on one hand that the two experiments are operational, on the other hand that the executed ANN has tolerated all the SEUs which occurred on different circuits of the implemented architecture.

II-75. **Study of the robustness of digital fuzzy control**

*Members: R. VELAZCO, Ph. CHEYNET, M. OLMOs, J-C RUBIO, S. REZGUI*

In this project is investigated the intrinsic robustness with respect to Single Event Upset, of fuzzy control digital implementations. A commercial circuit dedicated to fuzzy control was used to implement the control part of a future ESA Mars instrument deployment vehicle. Upset fault injection experiments show the fault tolerance properties of the studied application.

Fuzzy control offers powerful solutions to a wide range of control problems. Some of them are difficult to be tackled by classical approaches because they resist appropriate mathematical modelling or require a highly non-linear reaction. Another typical difficulty arises when unexpected inputs push the controller far off the operating point where the underlying mathematical model becomes invalid. Fuzzy control shows good performances even in those cases, and it therefore has also been applied in space before.

We have investigated the effects of upsets on a fuzzy application built around a commercially available fuzzy processor, the WARP-2.0 (Weight Associative Rule Processor) from SGS-Thomsson. Upsets were injected into a fuzzy model, designed for driving the motors of a Mars Instrument Deployment Device (IDD), to estimate its reliability in the destination environment.

Upsets simulations were performed on a bread-board including the WARP 2.0 which was developed as a prototype for an experiment in collaboration with CNES and NASA to be boarded on a scientific satellite: the Space Technology Research Vehicle (STRV-2) sponsored by the Defense Evaluation and Research Agency, (DERA, U.K.).

**Studied fuzzy processor**

The architecture of the chosen processor, the WARP 2.0, consists of 3 parts: an input stage, a processing stage, and an output stage. The input stage maps sensors or other inputs, such as switches, thumbwheels, etc. (8 bits digital input port) to the appropriate membership functions and truth values
(Alpha Calculator, using the Antecedent Memory). The processing stage invokes each appropriate rule and generates a result for each one, then combines the results of all rules (Inference Unit, using the program and consequent memories). Finally, the output stage converts the combined result back into a specific control output value (Defuzzifier) and exports it by a digital way (8 bits Output port).

The WARP 2.0 processor has two operation modes:
- 8 inputs, each with 8 Membership Functions (MFs), and 4 outputs; or:
- 4 inputs, each with 16 MFs and 4 outputs.

Running WARP 2.0 involves a downloading phase and an on-line phase. The downloading phase allows the configuration of the processor in terms of I/O number, universe of discourse, MFs, and rules. During this phase, WARP 2.0 loads the micro-code in its internal memory. This micro-code which drives the on line phase is generated by a compiler provided by SGS-Thomson. After that, WARP 2.0 is ready to run (on-line phase), processing inputs and producing the related outputs according to the configuration set in the downloading phase.

**Application under test**

The exploration of planet Mars is a challenging task. The IDD robots (rovers) sent to MARS have to fulfil special requirements. They must be very light, as they are transported by a lander on the surface of the planet. The equipment on the rover is used only for the collection of probes or experiments, therefore there is no sensor available for autonomous navigation. Due to the harsh climate conditions the rovers drive only during the day. The communication between the rover via the lander and the control tower on earth is done once a day in a very narrow time gap. Thus have to be short and effective. The Institute for Space Simulation (DLR, Cologne) has developed a 7 kg rover for such experiments. Based on a 3D image received from the lander, the operator on earth sends a number of commands defining the path of the vehicle. The proper execution of the given actions can only be verified a day later when the next 3D image is available. As the whole exploration on Mars takes only a week or two, it is very important that the trajectories sent are followed by the vehicle and thus only a reduced number of corrections is needed.

The application loaded on the WARP processor is the control process of steering the wheels of the Mars rover. The operator sends a trajectory to be followed by the rover. The geometric co-ordinates have to be converted into varying speeds and distances for each wheel of the rover. But wheels will slip on sand or slopes, and the motors may not exactly turn at the calculated speeds. Rather than to model these differences between geometric theory and sandy reality, we chose to implement the corrections on simple fuzzy controllers. Therefore the command is the same to all fuzzy controllers - 2 for each wheel- but the output a number of pulses for the motor is different for each wheel. The rules were determined by test runs of a prototype vehicle under typical conditions.

Two different fuzzy controllers, named FLC1 and FLC2 hereafter, were studied for the above presented application. Each fuzzy controller has 2 inputs and 1 output. The first fuzzy controller uses a reduced number of both membership functions and rules. It comprises 3 MFs for each input and output, and 9 rules. The second one has 8 MFs for each input and output and 64 rules. The linguistic labels for the input were chosen the same, thus we have symmetrical inputs (see also discussion). **Figure II-78** shows the distribution and the shape of the MFs associated to the linguistic labels in the universe of discourse of the inputs and output.
Figure II-78 - A simplified fuzzy controller (FLC1) for the Mars rover

Experimental set-up and obtained results

The hardware we developed to perform the upset injection experiments and the ground tests is based on THESIC system principles. It is composed of a "daughter board" built around the WARP fuzzy controller, a "mother board" based on a 8051 micro-controller for the control of daughterboard operation during the test under radiation and a PC for user interface. The daughterboard comprises mainly the WARP 2.0, logic glue, and clock system. Logic glue adapts the signals of the fuzzy controller to the bus of the mother board. The clock system uses a 12 MHz quartz (the maximum frequency allowed for WARP is 40 MHz).

Evidence of the approach robustness with respect to upsets in the memories storing the fuzzy model, can be obtained by injecting errors using the experimental setup above described. For each of the bits of the WARP microcode associated with a fuzzy model, the completion of the following steps allows to identify the upset sensitive area within the WARP memories:

1 - inverting one bit of the WARP microcode,
2 - downloading the corrupted microcode within WARP,
3 - processing the outputs for the chosen pattern set,
4 - comparing the outputs with the expected values.

The injected errors provoked three types of behaviours:
A: correct value for all the tested inputs,
B: wrong values for at least one of the tested inputs,
C: no response (within a fixed time-out).

The main robustness features of the two studied fuzzy controllers (FLC1 and FLC2) extracted from obtained results, can be synthetised as:

- 257 bits (resp. 1118 bits) may be flipped without consequences at the controller behaviour. SEUs on 41% (resp. 33%) of the memory containing relevant data (FLC microcode) are totally effectless.

- 356 bits (resp. 2235 bits) should result in erroneous rover wheel's commands. However, upsets on part of these bits could be considered as tolerated because they result in a deviation considered neglectable with respect to the reference command value. For the studied fuzzy controllers, 18% (resp. 29%) of the 5889 (rep. 32095) provoked errors when processing 108 (resp. 256) inputs coming from sensors. But the error deviation is less than 10%. For the rover control, commands is output can be considered tolerable. Detailed analysis of the obtained output set leading to determine the "wrongness" or the "quality" of the error will be presented in the final paper.
- SEUs on only 5 of the 30 bits of a register bench used to define the WARP configuration, result in system crashes (loose of WARP control). This unexpected robustness of a potentially critical area, probably due to an architectural reason, is presently under study.

**Robustness mechanisms**

We have attempt to identify the mechanisms inherent to fuzzy control strategy which leads to its robustness with respect to upsets errors. They depend on both the memory corrupted and the format used to store the fuzzy model. For the WARP architecture upsets on the membership function memory provoke: (a) changes in the slope of or (b) shifts of the abcisse of the MFs top. This leads to a "mutant" fuzzy model. From our experiments, the more serious consequences arise when such "mutant" model presents "holes" in the univers of discours (c). Figure II-7.9 illustrate these cases.

**Figure II-7.9 - Fuzzy model modifications due to upsets**
III - SERVICE ACTIVITY

The Laboratory is hosting the CMP Service Activity¹

**CMP**

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**Introduction**

The CMP project (Circuits Multi Projets) is a project undertaken since 1981 by the Laboratory. In 1984, the service became a "Unité de Service et de Recherche", depending on CNRS and INPG. This project allows the Universities, Research Laboratories and Companies to fabricate the Integrated Circuits, Multi Chips Modules and Microsystems they have designed. Fabrication is for prototypes or low volume production. The originality of the project consisted initially in the regrouping, on the same slice of silicon, of a large number of circuits. Thus accessible costs of fabrication are obtained.

Since 1981, more than 2500 circuits for Research, Education and Industry have been fabricated for more than 240 Institutions in France and in 40 foreign countries.

For each project, the operations to be achieved are the following:

- collection of circuits described in a common language
- checking of the circuits (syntax checking and design rules checking)
- assembly in Macro-blocks (sets of chips)
- generation of the entry connections for the manufacturer
- subcontracting the fabrication of the circuits
- subcontracting packaging of the chips
- delivery of chips to the users.

In parallel CMP distributes the design rules for each technology and the standard cell libraries for each specific software tool (design kits). CMP handles more than 50 different design kits (corresponding to different technologies and different CAD tools), which are sent to customers upon signature of a Confidentiality and Licence Agreement. About 400 customers have already signed the agreements and received the kits.

**Development since 1981**

Since 1981, about 250 fabrication runs have been undertaken. The number of manufactured circuits per year has passed from 8 in 1981 to 114 in 1992, 251 in 1994 and 333 in 1997. The complexity of the circuits has passed from several thousands transistors in 1981 to more than a hundred thousand transistors since 1985. NMOS technologies were used from 1981 to 1986 and CMOS from 1984 up to now. Access to Multi Chips Modules was open as early as 1992. GaAs technology was introduced in 1993. And manufacturing of Microsystems was offered since 1995.

¹ A specific report is available upon request.
During the last years, activities have been widely increased. This is reflected by Table I "CMP Development since 1989" and by Table II: "Progression in number of circuits, participating Institutions, number of runs and total silicon area". These figures show the global expansion of CMP over the last years: roughly in five years the participation (number of circuits and number of participants) has tripled and the silicon area, number of runs and number of offered technologies has doubled. Table III (a and b) lists all the centers having submitted circuits to the CMP Service and Table IV (a and b) depicts the evolution of CMP runs between 1981 and 1997.

**Participation of Industry**

CMP opened the service to Industry in 1990. In 1997, 84 industrial circuits, for 36 Industrial Companies or National Research Laboratories, were fabricated. This means that more than 25% of the circuits were industrial circuits. They were manufactured for prototyping or small volume production. In particular 47 circuits were manufactured for small volume production (14% of the total number of circuits) for 20 Institutions. Table V shows the development of small volume production during the five last years.

**CMP projects in 1997**

In 1997 a total of 112 Institutions (Universities, Research Laboratories and Industrial Companies) submitted 333 circuits for education, research and industrial purposes. Technologies used were CMOS DLM \(1.0 \ mu\), \(0.7 \ mu\) of ATTEL ES2, CMOS DLP \(1.2 \ mu\), \(0.8 \ mu\) of AMS, BiCMOS DLP DLM \(1.2 \ mu\), \(0.8 \ mu\) of AMS, GaAs \(0.6 \ mu\) of VSC and GaAs HEMT \(0.2 \ mu\) of PML. Table VI shows the distribution of circuits per category (Education, Research and Industry, from France and foreign countries), and Table VII depicts the number of circuits per technology.

**Micromachining Program**

CMP has been the first non-US multi-project-wafer service to introduce Microsystems manufacturing. In 1997, manufacturing of Microsystems, by compatible front-side bulk micromachining, was possible through the three following technologies offered by CMP: CMOS DLP DLM \(1.2 \ mu\) from AMS, BiCMOS DLP DLM \(1.2 \ mu\) from AMS and GaAs HEMT \(0.2 \ mu\) from PML. In addition, access to Diffractive Optical Elements (DOE) from CSEM, Switzerland, was also introduced. Several projects went to fab, for Universities and Industry, including suspended planar inductors, accelerometers, electro-thermal converters, IR detectors, etc.

New versions of the MEMS Engineering kits for the main EDA vendors (Mentor Graphics, etc.) were released and distributed.

**Multi Chip Modules**

CMP opened a Multi Chip Modules service in 1992. Contacts were established with MCMs manufacturers (DASSAULT ELECTRONIQUE, THOMSON-CSF MICROELECTRONIQUE, BULL, Montpellier Technologies) to offer the different MCM technologies (MCM-C, MCM-D and

---

AMS: Austria Mikro Systeme International  
DLM: Double Layer Metal  
DLP: Double Layer Polysilicon  
EDIF: Electronic Design Interchange Format  
PML: Philips Microwave Limel-Brevannes  
SMIs: Small and Medium sized Industries  
VSC: Vitesse Semiconductor Corporation
MCM-L). In 1997, an industrial MCM project was started and the first prototypes were issued and tested.

**CAD tools offers**

In order to facilitate chip design, CMP distributes and supports several CAD softwares, specially for PC tools, for both Universities and SMIs\(^2\), depending on the geographical location, type of customers, etc. CMP widespeads information on free software tools available from other services or Universities and distributes design kits for these tools. In the same way CMP has agreements with workstation based tool vendors and PC tool vendors to offer these tools when necessary.

**Participation to OMI**

The Open Microprocessor System Initiative, as part of ESPRIT Programme, was launched by the Commission of the European Communities (CEC) in 1991. The OMI programme aims to identify and to take into account technological advances and trends in the market such as the move to on-chip systems integration. In 1997 CMP was involved in the three following projects:

- **EUROMIC (EUropean OMI Centres):** The role of the EUROMIC consortium was to select technologies which could fit with OMI objectives and set up a network of services in order to fulfill the SMEs needs. The project ended in June 1997.

- **OMILIBRES (OMI LIBrary REPresentation Standards):** The project aimed at defining and prototyping a standardised library data representation for core and supercell model information. It was terminated at the end of 1997.

- **ASSISTEC:** started in November 1997, the project aims to provide a comprehensive support service to companies wishing to trade Intellectual Property (IP) in the micro-electronic area. The assistance offered focuses on the "pre-licensing" activities, providing advice on the preparation and valuation of IP, the identification of markets and strategic partners, and the process of licensing and negotiation.

**Other activities**

The CMP project calls upon the multiple competences of all members of the Research group: development of software tools (to check or correct various syntax descriptions), determination of the rules of multitechnological design, working with the formats used for circuit descriptions (a translator EDIF-GDS2-EDIF was achieved in 1990 for UNIX and VMS systems), library implementation for several softwares and several technologies: from 1992 to 1996 CMP developed library kits for AMS (1.2 \(\mu\) and 0.8 \(\mu\) CMOS, 1.2\(\mu\) and 0.8 \(\mu\) BiCMOS) on CADENCE and COMPASS softwares. Library kits for PC computers were also developed, for ATMELE BS2 1.2 \(\mu\), 1.0 \(\mu\) and 0.7 \(\mu\) CMOS on TANNER/L-Edit and EXEMPLAR/GALILEO softwares.

In 1997 CMP developed:

- a design kit for AMS 0.8\(\mu\) and 0.6\(\mu\) CMOS DLP/DLM on COMPASS tools,

- a high speed low power programmable analog-digital converter.

**Conclusion**

France has been a pioneer country in this type of infrastructure since chip fabrication for Universities has been started in 1981 by CMP; the elementary CAD software LUCIE has been provided to 36 Academic Institutions in France and foreign countries in the 80s (see Table VIII: distribution of the LUCIE system), industrial CAD software has been distributed to Universities in
1986 by CNPM, testing equipment has been centrally purchased in 1988. As early as 1990, CMP had opened chip fabrication to Industry.

The increasing number of participating Institutions, the extensions of the Micromachining program and the high level reached by industrial participation and low volume requests have been the most significant developments of CMP in 1997.
<table>
<thead>
<tr>
<th>Year</th>
<th>Nb of runs</th>
<th>Area in mm²</th>
<th>Nb of circuits</th>
<th>Institutions</th>
<th>Technologies</th>
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<tbody>
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<td>1989</td>
<td>5</td>
<td>617</td>
<td>92</td>
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<td>ES2 2μ</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>more integration</td>
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<tr>
<td>1990</td>
<td>9</td>
<td>1259</td>
<td>129</td>
<td>26</td>
<td>ES2 2μ, 1.5μ</td>
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<td></td>
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<td></td>
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<td></td>
<td>TCS Bipolar</td>
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<td>more integration</td>
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<tr>
<td>1991</td>
<td>13</td>
<td>1695</td>
<td>137</td>
<td>30</td>
<td>ES2 2μ, 1.5μ, 1.2μ</td>
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<tr>
<td></td>
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<td></td>
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<td>TCS Bipolar</td>
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<td>1992</td>
<td>22</td>
<td>1841</td>
<td>114</td>
<td>38</td>
<td>ES2 1.5μ, 1.2μ</td>
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**TABLE I - CMP Development since 1989**
TABLE II - Progression in number of circuits, participating Institutions, number of runs and total silicon area
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TABLE III a - French Institutions having submitted circuits to CMP (total : 98)

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Total in 1997: 44 runs
9 technologies 333 circuits 4 160 mm2

TABLE IV b - CMP runs in 1997

Total since 1981: 247 runs
2452 circuits: 1113 Research circuits. 1049 Educational circuits. 290 Industrial circuits
TABLE V - small volume production:
number of Institutions (left)
number of circuits (right)

TABLE VI - Circuits per category in 1997

TABLE VII - Circuits per technology in 1997
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<tr>
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<tr>
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<td>Torino (Italy)</td>
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<tr>
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**TABLE VIII - Distribution of the LUCIE system**
IV - RESOURCES

IV-1 Human resources

IV-1.1 Members of the Laboratory

Table IV-1 I presents a list of the researchers and engineers involved in the Laboratory, Table IV-1 II presents the researchers from Industry working in the Laboratory, Table IV-1 III lists researchers (visitors, trainees) who stayed in the Laboratory during 1997, Table IV-1 IV lists researchers working in other institutions, but enrolled with the Laboratory for a thesis.

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<tr>
<td>Alzaher-oufai</td>
<td>Issam Ph.D student</td>
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<tr>
<td>Ambiard</td>
<td>Paul Associate Professor – UJF/UFR:IMAG</td>
</tr>
<tr>
<td>Amielh</td>
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<td>Angheil</td>
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<tr>
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<td>SUGAR Zoltan</td>
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**TABLE IV-1** Members of the Laboratory (for 1997)

- Ph.D student: involved in doctorate degree
- DGA = Military Service
- IR = « Ingénieur de Recherches »
- DR = « Directeur de Recherche »
- CIFRE = Support from ANRT for Industry-University cooperation
- CR = « Chargé de Recherche »
- EN = Education Nationale
- IE = « Ingénieur d'Études »
### TABLE IV-11 - Researchers from Industry working in the Laboratory (for 1997)

<table>
<thead>
<tr>
<th>Visitors</th>
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<td>Tunisia</td>
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<td>3 months</td>
</tr>
<tr>
<td>APANOVITCH</td>
<td>Zinaida</td>
<td>Russia</td>
<td></td>
<td>6 months</td>
</tr>
<tr>
<td>ARATO</td>
<td>Peter</td>
<td>Hungary</td>
<td></td>
<td>1 week</td>
</tr>
<tr>
<td>BACIVAROV</td>
<td>Ioan</td>
<td>Romania</td>
<td></td>
<td>2 weeks</td>
</tr>
<tr>
<td>BENMOMHAMMED</td>
<td>Mohamed</td>
<td>Algeria</td>
<td></td>
<td>3 weeks</td>
</tr>
<tr>
<td>BRZOBHATY</td>
<td>Jaromir</td>
<td>Czech. Republic</td>
<td></td>
<td>1 week</td>
</tr>
<tr>
<td>BURIAN</td>
<td>Zdenek</td>
<td>Czech. Republic</td>
<td></td>
<td>1 month</td>
</tr>
<tr>
<td>DJEMAL</td>
<td>Ridha</td>
<td>Tunisia</td>
<td></td>
<td>1 month</td>
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<tr>
<td>HAMZA</td>
<td>Ridha</td>
<td>France (Beverly SA)</td>
<td></td>
<td>10,5 months</td>
</tr>
<tr>
<td>HLAVICKA</td>
<td>Jan</td>
<td>Czech. Republic</td>
<td></td>
<td>2 weeks</td>
</tr>
<tr>
<td>HOFMANN</td>
<td>Klaus</td>
<td>Germany</td>
<td></td>
<td>1 week</td>
</tr>
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<td>HUSAK</td>
<td>Miroslav</td>
<td>Czech. Republic</td>
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<td>3 weeks</td>
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<td>JAWORSKI</td>
<td>Zbigniew</td>
<td>Poland</td>
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<td>JEMAI</td>
<td>Abderrazak</td>
<td>Tunisia</td>
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<td>KLEIMYNOV</td>
<td>Serguei</td>
<td>Russia</td>
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<td>KUCEROVA</td>
<td>Jana</td>
<td>Czech. Republic</td>
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<td>1 week</td>
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<td>KUZMICZ</td>
<td>Wieslaw</td>
<td>Poland</td>
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<tr>
<td>LUBASZEWSKI</td>
<td>Marcelo</td>
<td>Brazil</td>
<td></td>
<td>2 weeks</td>
</tr>
<tr>
<td>PIESTRAK</td>
<td>Stanislaw</td>
<td>Poland</td>
<td></td>
<td>5 weeks</td>
</tr>
<tr>
<td>PLESKACZ</td>
<td>Wihold</td>
<td>Poland</td>
<td></td>
<td>1 week</td>
</tr>
<tr>
<td>RENCZ</td>
<td>Marta</td>
<td>Hungary</td>
<td></td>
<td>1 month</td>
</tr>
<tr>
<td>SINGH</td>
<td>Adit</td>
<td>USA</td>
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<td>1 week</td>
</tr>
<tr>
<td>STERIAN</td>
<td>Paul</td>
<td>Romania</td>
<td></td>
<td>2 weeks</td>
</tr>
<tr>
<td>SDNITSON</td>
<td>Alexander</td>
<td>Estonian</td>
<td></td>
<td>1 month</td>
</tr>
<tr>
<td>TKEBUCHAVA</td>
<td>George</td>
<td>Georgia</td>
<td></td>
<td>6.5 months</td>
</tr>
<tr>
<td>VASSILEVA</td>
<td>Tania</td>
<td>Bulgaria</td>
<td></td>
<td>2 months</td>
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<tr>
<td>VRBA</td>
<td>Radimir</td>
<td>Czech. Republic</td>
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<td>1 week</td>
</tr>
<tr>
<td>VYTLACIL</td>
<td>Dalibor</td>
<td>Czech. Republic</td>
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<th>Trainees</th>
<th>Name</th>
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<th>Nationality</th>
<th>Country of Origin :</th>
<th>Duration for 1997</th>
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<td>Harry</td>
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<td>France (ENISE)</td>
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<td>4 months</td>
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<tr>
<td>AGUILAR</td>
<td>Cristina</td>
<td>Spanish</td>
<td>Spain</td>
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<tr>
<td>AISA</td>
<td>Pieralejandro</td>
<td>Italian/French</td>
<td>Italy</td>
<td></td>
<td>3 months</td>
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<tr>
<td>ALI</td>
<td>Abakar</td>
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<td>Cameroon Republic</td>
<td></td>
<td>3 months</td>
</tr>
<tr>
<td>ARWEILER</td>
<td>Jens</td>
<td>German</td>
<td>Germany</td>
<td></td>
<td>4 months</td>
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<tr>
<td>AYACHE</td>
<td>François</td>
<td>French</td>
<td>France (ESIEE)</td>
<td></td>
<td>5 months</td>
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<tr>
<td>AZENNOURD</td>
<td>Younes</td>
<td>Moroccan</td>
<td>Morocco</td>
<td></td>
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</tr>
<tr>
<td>BENAMAR</td>
<td>Youssef</td>
<td>Moroccan</td>
<td>France (ENSERG)</td>
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<td>5 months</td>
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<tr>
<td>BENNOURI</td>
<td>Nabil</td>
<td>Moroccan</td>
<td>France (ENSERG)</td>
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<td>7 months</td>
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<th>Name</th>
<th>Name</th>
<th>Language</th>
<th>Country</th>
<th>Duration</th>
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<td>BLANQUEZ Oscar</td>
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<td>9 months</td>
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<td>BOFILL Adria</td>
<td>Spanish</td>
<td>Spain</td>
<td>5 months</td>
<td></td>
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<tr>
<td>BRYGILEVYCH Volodymyr</td>
<td>Ukrainian</td>
<td>Poland</td>
<td>2 weeks</td>
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<td>CALABRESE Antonietta</td>
<td>Italian</td>
<td>France (ENSERG)</td>
<td>2.5 months</td>
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<tr>
<td>CASTILLEJO Amaud</td>
<td>French</td>
<td>France (UJF)</td>
<td>9 months</td>
<td></td>
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<tr>
<td>CHARVIN Guillaume</td>
<td>French</td>
<td>France (UPMF)</td>
<td>2.5 months</td>
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<tr>
<td>CHICH Oxana</td>
<td>Bielorussian</td>
<td>France (UJF)</td>
<td>6 months</td>
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<td>CHRISTOFOROU Georges</td>
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<td>Greece</td>
<td>1 month</td>
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<tr>
<td>DANSON Amévi</td>
<td>Togolese</td>
<td>France (JUT)</td>
<td>2.5 months</td>
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<tr>
<td>GAULIER Sylvain</td>
<td>French</td>
<td>France (UJF)</td>
<td>4 months</td>
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<td>GEORGELIN Philippe</td>
<td>French</td>
<td>France (UJF)</td>
<td>3 months</td>
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<td>GIRERD Stéphane</td>
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<td>France (ISTG)</td>
<td>6 months</td>
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<td>GRELLETY Cyril</td>
<td>French</td>
<td>France (ISTG)</td>
<td>6 months</td>
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<td>GRENIER Laurence</td>
<td>French</td>
<td>France (Lycée L.M)</td>
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<td>GRODE Jesper</td>
<td>Danish</td>
<td>Denmark</td>
<td>6 months</td>
<td></td>
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<tr>
<td>GRUSON Yannick</td>
<td>French</td>
<td>France (LPMO)</td>
<td>1 week</td>
<td></td>
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<tr>
<td>GUINA Mircea</td>
<td>Romanian</td>
<td>Romania</td>
<td>3 months</td>
<td></td>
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<tr>
<td>JEANNOT Jean-Claude</td>
<td>French</td>
<td>France (LPMO)</td>
<td>1 week</td>
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<td>JORGENSEN Kristian-Philip</td>
<td>Danish</td>
<td>Denmark</td>
<td>7 months</td>
<td></td>
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<tr>
<td>KARAKOLAH Daoud</td>
<td>Syrian</td>
<td>France (ENSERG)</td>
<td>2 months</td>
<td></td>
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<tr>
<td>KIRSCHNER Michal</td>
<td>Czech.</td>
<td>Czech. Republic</td>
<td>1 month</td>
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<tr>
<td>LE POITVIN Christophe</td>
<td>French</td>
<td>France (U. Paris VII)</td>
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<td>LIATENI Karim</td>
<td>French</td>
<td>France (UJF)</td>
<td>6 months</td>
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<td>MAYER Christian</td>
<td>French</td>
<td>France (ENSERG)</td>
<td>7 months</td>
<td></td>
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<tr>
<td>MHANI Ahmed</td>
<td>Moroccan</td>
<td>France (UJF)</td>
<td>1 month</td>
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<tr>
<td>MONTANÉ Enric</td>
<td>Spanish</td>
<td>Spain</td>
<td>2 months</td>
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<tr>
<td>MTIBAA Abdellatif</td>
<td>Tunisian</td>
<td>Tunisia</td>
<td>1 month</td>
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<td>NADAL Rafael</td>
<td>Spanish</td>
<td>Spain</td>
<td>3.5 months</td>
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<tr>
<td>NASTAC Dumitru-Iulian</td>
<td>Romanian</td>
<td>Romania</td>
<td>3 months</td>
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<tr>
<td>OLMOS Marcos</td>
<td>Spanish</td>
<td>Spain</td>
<td>9 months</td>
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<tr>
<td>OREE Vishwamitra</td>
<td>Mauritian</td>
<td>France (ENSERG)</td>
<td>2 months</td>
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<tr>
<td>PALAN Bohuslav</td>
<td>Czech</td>
<td>Czech. Republic</td>
<td>1.5 months</td>
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<td>PERRENOT François</td>
<td>French</td>
<td>France (UJF)</td>
<td>6 months</td>
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<tr>
<td>PETERS Arno</td>
<td>Dutch</td>
<td>The Netherlands</td>
<td>2 weeks</td>
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<td>RAWSKI Mariusz</td>
<td>Polish</td>
<td>Poland</td>
<td>3 weeks</td>
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<tr>
<td>ROUX Sébastien</td>
<td>French</td>
<td>France (UJF)</td>
<td>4 months</td>
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<td>RUBIO Juan-Carlos</td>
<td>Spanish</td>
<td>Spain</td>
<td>10 months</td>
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<td>SAGMEISTER Patricia</td>
<td>German</td>
<td>Germany</td>
<td>1 week</td>
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<td>SARHAN Ayman</td>
<td>French</td>
<td>France (UPMF)</td>
<td>3 months</td>
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<td>SCHNEIDER Stefan</td>
<td>German</td>
<td>Germany</td>
<td>1 month</td>
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<tr>
<td>SEGURA Josep</td>
<td>Spanish</td>
<td>France (CNAM &amp; ESRF)</td>
<td>6.5 months</td>
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<tr>
<td>SOLTYSIAK Jean-Claude</td>
<td>French</td>
<td>France (CNAM)</td>
<td>4 months</td>
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<td>STRUNGRARU Cozana</td>
<td>Romanian</td>
<td>Romania</td>
<td>1 month</td>
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<td>TOMASZEWICZ Pawel</td>
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<td>Poland</td>
<td>3 weeks</td>
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<td>VESTMAN Frederik</td>
<td>Swedish</td>
<td>Sweden</td>
<td>5 months</td>
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**TABLE IV-1 (II): Visitors and Trainees (for 1997)**
<table>
<thead>
<tr>
<th>Name</th>
<th>FirstName</th>
<th>Affiliation</th>
</tr>
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<tbody>
<tr>
<td>CHAAHOUB</td>
<td>Faouzi</td>
<td>Rockwell Semiconductor Systems, Newport Beach, CA, USA</td>
</tr>
<tr>
<td>CLERMIDY</td>
<td>Fabien</td>
<td>CEA Saclay, France</td>
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<tr>
<td>KODRNIJA</td>
<td>Marc</td>
<td>SGS-Thomson, Grenoble, France</td>
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<tr>
<td>OUDINOT</td>
<td>Jean</td>
<td>Mentor Graphics, Paris, France</td>
</tr>
<tr>
<td>TCHOUMATCHENKO</td>
<td>Vassiliy</td>
<td>UNIV. of Sofia, Bulgaria</td>
</tr>
</tbody>
</table>

**TABLE IV-1 IV**: Researchers working in other institutions, but enroled with the Laboratory for their thesis in Grenoble
IV-1.2 Biographies of staff members
Paul AMBLARD

Born on February 25th, 1951
Married, 3 children

1972  Master of Science in Mathematics
1984  PhD Computer Science

Position

Assistant Professor (Maître de Conférences) at University Joseph Fourier, Grenoble, UFR Informatique et Mathématiques Appliquées

Previous Positions

From 1973 to 1982  Teacher of Mathematics in secondary schools
From 1984  Assistant Professor at University Joseph Fourier
In October 1997  Joined TIMA Laboratory
Mabrouka-Sabiha ARAB

Born June 15th, 1959
Married, 2 children
French and Algerian

1984 Master Degree in Computer Sciences applied to management, University Joseph Fourier
1985 DEA degree in Computer applied to Social Sciences, University Pierre Mendes-France
1993 Ph.D. in Computer applied to Social Sciences, University Pierre Mendes-France

Position

Contractual researcher with TIMA laboratory since September 1997

Current responsibilities

* Member of the System Level Synthesis Group at TIMA
* Participation to the development of COSMOS (co-design tool for embedded systems)
* Management of the COMITY and CODAC ESPRIT projects

Previous Positions

Contractual researcher with CRISS laboratory, University Pierre Mendes-France
involved in:
- ESPRIT project EPSILON (Artificial Intelligence)
- ESPRIT project BUSINESS CLASS (Software Engineering)
- ESPRIT project SCALE (Software Engineering)

Teacher in computer at University Pierre Mendes-France
involved in:
- COST action #15 : Many-valued logics applied to Computer Sciences.
Louis J. BALME

Born August 23rd, 1951 in Grenoble, France
Married, 3 children
French

Education

1972 : Master's Degree - Economics and Politics - IEP Grenoble
1975 : Master's Degree - Electronics - Institut National Polytechnique - Grenoble (INPG)
1976 : PhD Electronics - INPG
"Applications of Spectral Bioimpedometry to EEG and cerebral imagery"
1990 : Habilitation à Diriger des Recherches (French National Authorization to Supervise Research)

Position

* Associate Professor in Electronics at Institut National Polytechnique de Grenoble (INPG)

Current Responsibilities

* Professor in Signal Processing, Information Theory and Quality of Complex Systems (RAMs)
* Responsible for Quality Complex integrated Systems research group at TIMA Laboratory
* Secretary General of the European Programme in Quality of Complex Integrated Systems
* Member of the Editorial Board of the Journal of Quality Engineering (USA)

Previous Positions

* Director of Corporate Relations of INPG (1984-1991)
* President and CEO of SYMAG Computers (1979-1984)
* Assistant Professor INPG (1974-1979)

Miscellaneous

* Registered European Quality Consultant (since 1993)
* Consultant KEYO Corporation (1984-1987)
* President of Synergy Commission at the French computer Industry Association (1984-1987)
* Director of the INPG Master's Degree "Quality of Computers Systems" (1989-1992)
* Vice-President of Merlin Gerin - INPG Economic Interest Grouping (1989-1992)
* Gold Medal from the International Inventors Exhibition - Brussels 1986
Dominique BORRIONE

Born February 20th, 1950
Married, 2 children
French

1970: B. S. in Applied Mathematics, Aix-Marseille University
1971: DEA in Computer Science, University of Grenoble
1976: PhD in Computer Science, University of Grenoble
1981: Doctorat d’Etat in Computer Science, University of Grenoble

Position

Professor at Université Joseph Fourier, Grenoble

Past Responsibilities

Director of the ARTEMIS Laboratory (1991-995)

Current Responsibilities

Leader of the Verification and Modeling of Digital Systems Group

* Has served in many Conference and Workshop Committees
* Invited Scientist at U.C. Berkeley (Jan.-Aug. 1996)
* Currently: Program Committee Chairperson for the conference DATE'99
* IFIP Silver Core
Jean-Pierre BOYER

Born February 21st, 1976
Single
French

Education

1994 : Baccalauréat degree in Mathematics and Technologies.

Position

Contractual technician with TIMA Laboratory since September 1998.

Current responsibilities

Operating systems supervisor at TIMA Laboratory.
Sébastien COLIN

Born July 4th, 1973
Single
French

Education

1992 : Baccalaureat degree in Mathematics and Technics
1995 : DUT in Electrical Engineering and Industrial Computer Science, Electronics option, at I.U.T. 1, Grenoble

Position

Contractual technician with CMP since August 1996

Current responsibilities

Data preparation ICs at CMP.
Bernard COURTOIS

Born April 17th, 1948
Married, 2 children
French

Education

1967 - Baccalaureat degree - Mathematics
1968 - Baccalaureat degree - Philosophy
1967 - 1970 Mathematics in Paris
1970 - 1973 National School for Informatics and Applied Mathematics in Grenoble
1973 - Engineer degree
1976 - Doctor-Engineer degree
1981 - Docteur d'Etat degree

Position

"Directeur de Recherches" CNRS

Current responsibilities

* Director of TIMA Laboratory
* Director of CMP Service

Miscellaneous

* Has authored or co-authored many scientific papers
* Has served in many Committees of Conferences & Workshops
* Has served as a reviewer of research proposals to CEC, NATO, NSF, SERC
* Doctor Honoris Causa of the Technical University of BUDAPEST
* IEEE Golden Core.
Hubert DELORI

Born December 26th, 1946
Married, 5 children
French

Education

1964    Baccalaureat degree - Mathematics
1964-1967 Mathematiques Supérieures & Mathématiques Spéciales, Lycée Janson de Sailly, Paris
1967-1970 Engineer studies at Ecole Centrale de Lyon
1970    Engineer degree from Ecole Centrale de Lyon.

Position

"Ingénieur de Recherche 1ère classe" at CNRS (Centre National de la Recherche Scientifique).

Past activities

1970    Programming at IBM Corbeil-Essonnes.
1972    Teaching in Mathematics and Statistics in Algeria (for the military service).
1973    Engineer at "Cabinet Roland Olivier": working in statistics for a national inquiry about agriculture in Algeria.
1975    Education of physically handicapped young people for social re-insertion.
1978    Engineer at ICARE (Informatique Communale Alpes Rhône) at the town hall of Saint Etienne : responsible of the working of the informatics applications.
1979    Complementary studying in System Programming at "Institut de Programmation de Grenoble" (1 year).
1983    Engineer at CMP (Circuits Multi Projets).

Current responsibilities

Sylvaine EYRAUD

Born March 23rd, 1970
Married, 1 child
French

Education

1989 : Baccalaureat degree in Mathematics and Natural Sciences
1991 : DUT in Computer Sciences
1994 : "Diplôme d'Études Supérieures Techniques d'informatique d'entreprises" (informatics for companies)

Position

Contractual technician with CMP since February 1993.

Current responsibilities

* Management and distribution of design kits for CMP
* Database responsible at CMP.
Alain GUYOT

Born September 11th, 1945
Married, 3 children
French

1970 - Master in Computer Science from Grenoble University
1975 - Ph.D in Computer Science from Grenoble University
1991 - "Habilitation à diriger des Recherches"

Position

Assistant Professor (Maitre de Conférences) at ENSIMAG (Ecole Nationale
Supérieure d'Informatique et de Mathématiques Appliquées de Grenoble) since 1986

Past activities

* Teacher in computer architecture and VLSI design mainly at ENSIMAG and Grenoble
  University since 1971
* Visiting scholar or invited professor with the CSL group in Stanford University (Prof.
  M. Flynn), Microelectronic group in Telecom University, Paris (Prof. Jutand) and LEG-
  EPFL in Lausanne (Prof. M. Declercq)
* Participated in 1980 to the starting of the CMP foundry service
* Author or co-author of more than 50 scientific publications in Journals, Conference
  Proceedings, or Research Reports
* Served as a reviewer for ESSCIRC, VLSI, Computer Arithmetic, EUROASIC, IEEE
  TC, CAVE and other conferences.

Current responsibilities

* Responsibility of the Integrated Systems Design Group
Ahmed Amine JERRAYA

Born August 1st, 1955
Married, 1 child
French and Tunisian

Education

1980 Engineer degree, Faculté des Sciences de Tunis, Tunisie.
1981 DEA, Computer Science, Institut Polytechnique de Grenoble, (INPG), France
1983 Doctor-Engineer degree, Computer Science, INPG.
1989 Doctorat d'Etat degree, INPG.

Position

Research director with CNRS, the French National Center for Scientific Research. Section : Computer Science.

Past Activities

- Participated to the LUCIE system, highly successful layout tools, distributed in the early 80s to 20 Laboratories in France and 17 abroad.
- Led the APOLLON/SYCO projects, early architectural synthesis tools.
- Led the AMICAL project, a highly successful architectural synthesis tool that is being transferred to industry.

Current Responsibilities

- Leader of the System Level Synthesis Group of TIMA at INPG.

Miscellaneous

- Award of "President de la République" in Tunisia, 1980, Best Computer Science Engineer Degree
- Served in the Program Committee of ICCAD, DATE, EDAC, High-Level Synthesis Workshop, EuroDac, EuroVHDL, VHDL International, APCHDL, CODES Workshop and ICCD.
- Several tutorials in international conferences (EuroVHDL, EuroVHDL-EURODAC, APCHDL)
- Spent one year at Bell Northern Research in Ottawa, Canada
- Technical Program and Organization Chairperson of ISSS'95 Conference, Cannes, France
- Program Chair of RSP'96 Workshop
- General Chair of ISSS'96 Conference, La Jolla, CA, USA
- Program co-chair of CODES/CASHE'98, Seatle, USA
- Co-Director of NATO ASI School on system level synthesis, II CIOCCO, Italy
Born November 14th, 1969
Single
Lebanese

Education

1987 - 1989  Mathématiques supérieures & spéciales, Ecole Supérieure d'Ingénieurs de Beyrouth (ESIB), Lebanon

1993  Engineer degree, Ecole Supérieure d'Ingénieurs en Electrotechnique et Electronique (ESIEE), Paris, France

1993  DEA Microelectronics, University of Paris VII, France

1996  Doctor degree in Microelectronics, Institut National Polytechnique de Grenoble (INPG), France
"Methods and Tools for the Design and Manufacturing of Microsystems"

Position

Researcher with TIMA laboratory since January 1994

Current Responsibilities

Leader of the MiCroSystems group

Miscellaneous

* Responsible of microsystem development activities at the CMP Service
* Expert for the UK government funding body EPSRC on research involving microsystems
* Member of many Committees of Conferences and Workshops
* IEEE member
Nadim KRIM

Born October 3rd, 1965
Single
French

Education

- 1987-1988 Master in"Computer Science"

Professional activities

1993-present at CMP:
- CAD tools and Macro cells Manager
- Coordinator of the EUROMIC project
- French responsible for the OMI Inter University Network
- CAD Manager for the CAD activities development of the CMP Service

1992: R&D engineer, EDF-GDF Research Center, Paris


Claude LE FAOU

Born May 20th 1938
Married, two children
French

Education

1956
Baccalaureat degree - Mathematics
1956 - 1959
Mathématiques Supérieures & Mathématiques Spéciales, Lycée Saint-Louis, Paris
1959 - 1962
Engineer studies at "Institut National Polytechnique de Grenoble"
1962
Engineer degree from INPG. Speciality: "Radioélectricité"

Position

"Ingénieur de Recherche" at CNRS (Centre National de la Recherche Scientifique)

Past activities

1964-1966
Engineer in a private research Laboratory (LEAD) : Electronical design of a very high rapidity plotter

1966-1971
Engineer at “Institut National Polytechnique de Grenoble”, Computer Science Department : Design and development of simulation programs at circuit level : IMAG1, IMAG2

1971
Research Engineer at CNRS

1971-1981
Research and development in the field of Electrical Simulation. Design and development of IMAG3, IMAG4

1974-1983
Co-management of research team (15-20 persons) at IMAG laboratory

1981-1987
Technical management of CASCADE project : CAD system for VLSI circuits and systems (20-25 persons)

1983-1987
Staff member of ARTEMIS Laboratory

1987-1989
Visiting Researcher at UFRGS, Porto Alegre, Brazil

1989-1994
Research and development on man machine interface for integration of verification tools

1990-1994
Joint Director of ARTEMIS Laboratory

Current responsibilities

Administrator of the research group VDS at TIMA Laboratory.
Jean MERMET

Born: February 24th, 1942
Married, 2 children
French

Education

1958 Baccalaureat C, La Réunion
1958 Baccalaureat A, Grenoble
1959 Baccalaureat in Mathematics, Lyon
1959 Baccalaureat in Phyllosophy, Bordeaux
1966 Engineer degree, ENSIMAG, Grenoble University
1967 Master degree in Mathematics, Grenoble University
1970 "Docteur-Ingénieur, Grenoble University
1973 "Docteur d'Etat", Grenoble University
1977 DESS degree in Economy, Grenoble University

Position

"Directeur de Recherches" CNRS

Previous positions

- July 1966 to August 1968 Research Engineer
- May 1974 to May 1978 "Délégué aux Relations Industrielles en Rhône-Alpes"
- June 1980 to June 1983 Head Department ENSIMAG of IMAG
- February 1983 to October 1985 European CERES Project Manager
- January 1984 to December 1987 Director of ARTEMIS Laboratory
- January 1988 to December 1989 "Directeur Scientifique et des Applications de la Recherche" of the Mediterranean Institute of Technology
- October 1988 Director of "UMS 815" CNRS
- Since July 1991 European CAD Standardization initiative

Responsibilities

- Founder and General Secretary of Association MICADO (1974 to 1986)
- Expert to the CEC (2 years)
- Member of the Board of INPG (1 mandate)
- Member of the Scientific Council of INPG (2 mandates)
- Member of IFIP WG 5.2 et WG 10.2 (since 1976)
- Co-Chair of the IEEE VHDL Analysis and Standardization Group (since 1990)
- Chairman of the European (JESSI) HDL Standardization Group (since 1990)
- General Chair of EuroVHDL Conference (1992, 1993)
- General Chair of the EuroDAC Conference (1994)
- General Chair of the APCHDL Conference (1995)
- General Chair of the EDA Standards Summer School (1996)

Miscellaneous

- COMPUTER Society Golden Core Member (1996)
- Meritinous Service Award IEEE (1995)
Imed MOUSSA

Born January 3rd, 1966
Single
Tunisian

Education

TIMA Laboratory, National Polytechnic Institute of Grenoble (INPG)
Ph. D. Thesis : Application of Gallium Arsenide (GaAs) Integrated
Circuits for High Speed Communication Systems and High performance
Computing

1991-1992 : M.S. degree Microelectronics (DEA)
University Blaise Pascal, France.
M.S. Thesis : Characterisation of III-V Semiconductor Technologies

1990-1991 : Electrical and Telecommunication Engineering Degree
National Engineering School of Tunis,
(Ecole Nationale d’Ingénieurs de Tunis ENIT) Tunisia

Position

Working with TIMA laboratory and SGS- Thomson.
VLSI circuit design for ATM applications.

Previous positions

1992 -1996 :

- ASIC design experience obtained through the following project at 3
different laboratories in Europe :
  1 - 16x16 bit redundant divider : Designed at TIMA laboratory using
      full custom methodolgy. (Digital 0.8 um GaAs process from
      Vitesse).
  2 - Datapath Generator : for high speed technology : Developed
      using high level description and AMICAL behavioral synthesis
      tool.
      Designed at CMA laboratory in SPAIN and TIMA laboratory.
  3 - 2.5 Gb/s ATM Label Translator: Features efficient searching
      algorithm able of translating the virtual address of an ATM cell
      (28 bits) in less than 170 ns. Supporting 10K to 30K simultaneous
      connections.
      Implemented using H-GaAs-III (Vitesse).
      300-500 Mhz Clock frequency. 35 K transistors.

March 1994-July 1994 : Research Visitor, University of Las-Palmas, SPAIN :
Center of Microelectronic Application CMA.

January 1995 - June 1995 : Research Visitor, Technical University of DENMARK :
Centre for Broadband Telecommunication CBT.
Salvador MIR

Born September 21st, 1963
Single
Spanish

Education

1987 - Industrial Engineering degree - Electrical, Polytechnic University of Catalonia, Barcelona, Spain
1989 - Master degree - Computer Science, University of Manchester, United Kingdom.
1993 - Ph.D. degree - Computer Science, University of Manchester, United Kingdom

Position

Contractual researcher in TIMA since December 1997

Past activities

1993 - 1994 Postdoctoral researcher with TIMA
1995 Contractual researcher with TIMA
1996 - 1997 Contractual researcher with Centro Nacional de Microelectrónica, Seville, Spain

Miscellaneous

* Has published 30 scientific papers in international journals, conferences and workshops
* Award from Association of Industrial Engineers of Catalonia, Spain, to the best Work Graduation Dissertation in Industrial Engineering, Barcelona, 1988
Mihail NICOLAIDIS

Born April 22nd, 1954
Single
French and Greek

Education

1978 Engineer degree - Mecanical-Electrical, Ecole Polytechnique de l'Université de Thessaloniki.
1981 DEA Electronical, Institut Polytechnique de Grenoble (ENSERG).
1984 Doctor-Engineer degree - Data processing
Design of self-testing integrated circuits for analytical failures hypotheses.

Position

"Directeur de Recherche" at CNRS

Current responsibilities

* Responsible of the Reliable Integrated Systems Group of TIMA Laboratory
* General Co-Chair of 1997 IEEE International On-Line Testing Workshop
* Program Co-Chair of 1997 IEEE VLSI Test Symposium
* Program Chair of 1998 IEEE VLSI Test Symposium
* 2nd Vice-Chair of IEEE Computer Society Test Technology Technical Committee (TTTC)
* Chair of Technical Activities TTTC.
Pierre OSTIER

Born February 5th, 1968
Single, two children
French

Education

1992    DEA in Computer Science, INPG, Grenoble, France.
1997    PhD in Computer Science, University of Grenoble, France.

Position

Contractual Research Engineer with VDS.

Current responsibilities

- Integration of formal tools for hardware verification and diagnosis in the Prevail environment.

- System administration of VDS machines.
Jean-François PAILLOTIN

Born October 6th, 1955
Single
French

Education

1978 - Licence Telecommunications - Reims University
1979 - Licence Computer Sciences - UJF Grenoble
1980 - Master Degree Computer Sciences - UJF Grenoble
1981 - DEA Computer Sciences - INP Grenoble
1984 - Doctorate Computer Sciences - INP Grenoble.

Position

Present position: "Ingénieur de Recherche" National Education

Before:
* LCS researcher, INP Grenoble
* Assistant Teacher at IUT of Computer Sciences, Grenoble
* Assistant Teacher at UJF.

Current responsibilities

* Technical responsible since 1985 for the CMP (Circuits Multi Projets): national
  Service for manufacturing integrated circuits for all the French Universities and
  Research Laboratories (about 2000 integrated circuits fabricated since 1981)
* ATMEL ES2, VSC and PML runs responsible
* ACMO (Agent Chargé de la Mise en Œuvre de l’hygiène et de la sécurité)
Education

1994 : DEUG A (Mathematics and Computer science), University of Rennes I
1997 : Engineer degree from I.F.S.I.C - University of Rennes I
       Speciality: "Computer Architecture"

Position

Contractual Engineer with CMP since March 1997

Current responsibilities

Design-kit developments and support
Emmanuel SIMEU

Born December 25th, 1959
Married, 2 children
French and Cameroonian

Education

1987 Engineer degree -Electrical- University of Casablanca (Morroco)

Position

Associate Professor (Maître de Conférences) at ISTG (Institut des Sciences et Techniques de Grenoble).

Current responsibilities

Member of the Reliable Integrated Systems Group

Previous Positions

Associate Professor at ISAR (Institut Supérieur d'Automatique et de Robotique de Valence) (1992-1995).

Researcher in LAG (Laboratoire d'Automatique de Grenoble) (1988 - 1995)
Researcher in CNET-CNS Grenoble (SITAR Project 1989 - 1992)
Rodolphe SUESCUN

Born May 30th, 1972
Single
French

Education

1994      Engineer degree, Ecole Nationale Supérieure d'Informatique et de
          Mathématiques Appliquées de Grenoble (ENSIMAG), Grenoble
1995      DEA in Microelectronics, Université Joseph Fourier, Grenoble.

Position

Contractual engineer with TIMA Laboratory since October 1996.

Current responsibilities

Development and support within the AMICAL project.
Zoltan SUGAR

Born November 25th, 1969
Single
Hungarian

Education

1994 Master of Science degree in microelectronics at the Technical University of Budapest, Hungary

Position

Contractual researcher with TIMA Laboratory

Current responsibilities

Research and development within the MUSIC project
Kholdoun Torki

Born February 21\textsuperscript{th} 1961
Married
Tunisian

Education

1985: "Maîtrise" degree in physics and electronics, University of Constantine.
1986: DEA microelectronics, INPG, Grenoble.
1990: Ph.D. degree, INPG, Grenoble.

Position

Engineer at CNRS since 1994.
Contractual engineer with CMP-TIMA Laboratory since June 1990.

Current Responsibilities:

* Managing design-kit developments for different foundries under different CAD/CAE systems
* Participation and technical responsibilities in promoting microelectronics for SMEs
* Contact person at CMP for the AMS and SGS-Thomson foundries
Born December 14th, 1952  
Single  
French and Uruguayan

**Education**

1976-1979  National School for Informatics and Applied Mathematics in Grenoble  
1979  Engineer degree  
1982  Doctor Engineer degree  
1990  Docteur d'Etat degree

**Position**

"Chargé de Recherches" at CNRS since 1984  
Researcher with TIMA since 1996

**Current Responsibilities:**

* Leader of the "Qualification of Circuits" group of TIMA laboratory  
* Responsible of two french experiments on board scientific satellite : Projects MPTB (Microelectronics and Photonics Testbed, with CNES and Naval Research Labs) and STRV (Space Technology Research Vehicle, with CNES and NASA)  
* Coordinator of two ALFA projects (program America Latina Formation Académique of CEE) and responsible for TIMA of a third one as well as a CAPES-COFECUB project.  
* Member of the Scientific Committee of TIMA since 1998
Gérard VITRY

Born August 5th, 1947
Married, 2 children
French

1973 : "Programmeur Expert en Systèmes Informatiques" - Grenoble

Position

"Ingénieur d'Etudes" at CNRS

Current Responsibilities:

* System Engineer
* Web administrator
Nacer-Eddine ZERGAINOH

Born May 18th, 1963
Married
Algerian and French (under way)

Education

1984  Baccalaureat degree, Mathematics
1989  Engineer degree, Electrical Engineering-Telecom, ENITA.
1991  DEA degree, Signal Processing-Automatic, LSS-Supelec, University Paris XI, France
1996  PhD degree, Electronics-Computer Engineering, University of Paris XI, France

Position

Assistant Professor in Computer Engineering and Architecture, Institute of Sciences and Technique (ISTG), Joseph Fourier University, Grenoble.

Past Activities

♦ Participated to the European Esprit-Polyglot Project.
♦ Participated to the European Prometheus Project.
♦ Teacher in telecom and computer (ESIGITEL, EPITA, Paris XIII University).
♦ Contractual engineer of research with LIMSI-CNRS Laboratory Gif/Yvette.

Current responsibilities

♦ Researcher in System Level Synthesis Group of TIMA Laboratory.

His research interests include system-level design and CAD issues, parallel algorithms and architectures, and real time operating system. Currently, his research focuses on communication protocols synthesis, interface specification methods, and on developing libraries to assist embedded system programmers.

Miscellaneous

♦ Has authored or co-authored several scientific papers.
### IV-1.3 Curriculum vitae of Doctorate candidates

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<tr>
<th>Name</th>
<th>ABDELHAY, Ahmad</th>
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<td>Previous degrees</td>
<td>Electronic Engineering Degree (1987), Syria</td>
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<td>DEA in Microelectronics (1996), INPT (ENSEEIHT), Toulouse, France</td>
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<td>Research interests</td>
<td>System level testing, integrated cores testing, design for testability and build-in-self-test</td>
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<td>December 1998</td>
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<td>B. Sc in Physics (1994), Liverpool Univ., UK</td>
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<td>DEA (M.Sc.) in Microelectronics (1995), Grenoble, France</td>
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<td>Research interests</td>
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<td>Electronic Engineer (1995), ENSERG, Grenoble, France</td>
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<td>DEA degree (1995), UJF, Grenoble, France</td>
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<td>Research interests</td>
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<td>2001</td>
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<tr>
<td>Previous degrees</td>
<td>Electronics Engineer (1996), Politechnica University of Bucarest (Romania)</td>
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<td>DEA in Microelectronics (1997), Politechnica University of Bucarest (Romania)</td>
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<td>Research interests</td>
<td>IDDQ Tests in Deep Submicron CMOS Technologies</td>
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<td>M.Sc. in Electrical Engineering, Sao Paulo University, Brazil</td>
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<td>Research interests</td>
<td>CMOS-GaAs digital integrated circuits design</td>
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<td>Present employment</td>
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<td>Engineer (1993), DEA in integrated Electronic Devices (1993), Ecole Centrale de Lyon, France</td>
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<td>Research interests</td>
<td>High-level synthesis</td>
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<td>Present employment</td>
<td>CIFRE contract with SGS-Thomson Microelectronics</td>
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<td>Name</td>
<td>BIANCHI, Andres</td>
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<td>Electronic Engineer (1995), UCC, Cordoba, Argentine</td>
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<td>Research interests</td>
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<td>Research interests</td>
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<td>Electronic Engineering (1995) Algiers, Algeria</td>
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<td>DEA in Signal Image Parole(1997) ENSERG, Grenoble</td>
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<td>Research interest</td>
<td>Generic tools for Built In self Test</td>
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<td>M.Sc. in Electrical Engineering, Technical Univ.of</td>
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<td>Research interests</td>
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<td>Research interests</td>
<td>Radiation-tolerant CMOS circuit design, current</td>
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<td>testing, self-testing microsystem architectures</td>
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<td>Research interests</td>
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<td>November 1998</td>
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<td>Research interests</td>
<td>ANN and Fuzzy Logic robustness, For on-board satellite board OS fault tolerance</td>
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<td>Research interests</td>
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Name : DJIDI, Nabil

Expected date of degree : 2001
Previous degrees : Engineer on Electronics, Politechnical School of Algeria (1995)
                  : Engineer on Microelectronics, INPG, Grenoble (1997)
                  : DEA on Automatic, INPG, Grenoble (1996)
Research interest : BIST and built self-repair
Present employment : French/Algerian scholarship

Name : DUSINA, Julia

Expected date of degree : 1998
Previous degrees : System Engineering degree, Tallinn Technical University,
                  : Estonia (1990)
                  : DEA Informatics, UJF, Grenoble, France (1995)
Research interests : Formal verification, high-level synthesis
Present employment : /

Name : GOY, Jérôme

Expected date of degree : 2000
Previous degrees : Electronic Engineering Degree (1997), ENSERG, Grenoble,
                  : France
                  : DEA degree (1997), UJF, Grenoble, France
Research interests : Image sensors, Analog circuits design
Present employment : /

Name : GUILLAUME, Philippe

Expected date of degree : May 1998
Previous degrees : DEA in Microelectronics, LIRMM, Montpellier, France
Research interests : Low power estimation and design in the area of high-level
                  : synthesis
Present employment : CIFRE Contract with SGS-Thomson

Name : HESSEL, Fabiano Passuelo

Expected date of degree : 1999
Previous degrees : Computer Sc. degree (1991), Brazil
                  : Master in Computer Science (1995), Brazil
Research interests : Hardware/software codesign, high level synthesis
Present employment : CAPES (Brazil) scholarship

Name : JUNEIDI, Zein

Expected date of degree : 2001
Previous degrees : Computer sciences Engineering degree (1993), ISSAT (Syria)
                  : DEA in Informatics (1997) ENSIMAG ,Grenoble
Research interests : developing of CAD tools for Microsystems
Present employment : Syrian Government Scholarship
Name : KODRNJA, Marc

Expected date of degree : Completed
Previous degrees : Microelectronic Engineer (1990), Paris-Sud University, Orsay, France; DEA in Microelectronics (1993), UJF, Grenoble, France
Research interests : Analog voltage controlled oscillators and phase locked loop
Present employment : CIFRE scholarship (with SGS-Thomson)

Name : LE MARREC, Philippe

Expected date of degree : 1999
Previous degrees : DEA in Microelectronics (1996), UJF, Grenoble, France
Research interests : High-Level Synthesis, Cosimulation Multi-levels and Multi-languages
Present employment : French Government Scholarship

Name : LIEM, Clifford

Expected date of degree : Completed
Previous degrees : Bachelor of Science, Physics (1989), St. Francis Xavier Univ. (Canada)
Master of Electrical Engineering (1991), Carleton Univ. (Canada)
Research interests : Retargetable code generation, embedded processors
Present employment : Canadian Government Scholarship

Name : MARCHIORO, Gilberto Fernandes

Expected date of degree : September 1998
Previous degrees : Computer Science degree (1987), Brazil
Master in Computer Science (1991), Brazil
Research interests : Hardware/Software Co-Design, High Level Synthesis
Present employment : CAPES (Brazil) scholarship

Name : MARTINEZ, Sergio

Expected date of degree : 2000
Previous degrees : M.Sc. in Electronics, Philips International Institute, Netherlands
M.Sc. in Control Engineering, ITESM, Mexico
Research interests : Microsystem design for critical application and harsh environment
Present employment : Scholarship from Mexican’s government

Name : MOHAMED, Firas

Expected date of degree : Completed
Previous degrees : DEA on Informatics (1993), Univ. of Montpellier (France)
Research interests : A.I. for analog circuits diagnosis
Present employment : Syrian Government Scholarship
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<td>Research interests</td>
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<td>Research interests</td>
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<td>Germany (1 year)</td>
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<td>Name</td>
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<td>Research interests</td>
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<td>Research interests</td>
<td>Synthesis for standard cell and FPGA</td>
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<td>Present employment</td>
<td>Assistant Professor at Technical Univ. of Sofia, Bulgaria</td>
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<td>Previous degrees</td>
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<td>Research interests</td>
<td>System level synthesis, co-design</td>
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<td>Expected date of degree</td>
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<td>Previous degrees</td>
<td>Electrical Engineer (1985), Univ. del Valle, Cali, Columbia</td>
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<td></td>
<td>DEA Microelectronics (1995), Univ. Joseph Fourier, Grenoble, France</td>
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<td>Research interests</td>
<td>Design and test of mixed-signal ICs - BIST architectures for sensor-based microsystems</td>
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<td>Expected date of degree</td>
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<td>Research interests</td>
<td>Radiation hardened circuits, on-line analog self-test, integrated detectors</td>
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<td>Present employment</td>
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<td>Research interests</td>
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<td>Research interests</td>
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IV-2  TIMA network and computer equipment

IV-2.1 Computer equipment

This equipment is made up of servers, workstations, X terminals, and personal computers. Laser printers are also available, as well as other peripherals like CD-ROM and Hexabyte drives. The list follows:

Servers (Sun):
2 Sparc Ultra
1 Sparc SS20

Workstations (Sun):
1 SparcUltra 1
4 Sparc SS10/30
2 Sparc 10/51
1 Sparc 20/50
1 Sparc SS 5
2 Sparc 4

Micro Computers PC:
1 Pentium II 300
3 PC Portables Pentium
40 PC Pentium (133 -> 233)
1 PC 486 DX4 100

Micro Computers Macintoshes:
1 Quadra 800 (Apple)
1 Performa 630 (Apple)
1 Mac LC 630 (Apple)
1 Power Mac 6100/60 (Apple)
1 Power Mac 7200/90 (Apple)
1 Power Mac 8100 (Apple)
1 Power Mac 8200/120 (Apple)
1 PowerBook 160 (Apple)
2 PowerBook 170 (Apple)
1 PowerBook 180 (Apple)
3 PowerBook 540 (Apple)
2 PowerBook 5300 cs (Apple)

X Terminals:
4 NCD Xplora 15 (NCD)
1 NCD Xplora 17 (NCD)
3 NCD 19 (NCD)
4 NCD 19r (NCD)
1 TATUNG 17 (TATUNG)
5 NCD 15b (NCD)
5 NCD 15r (NCD)
IV-2.2 Network wiring and topology

In summer 1992, the network has been completely restructured, physical support (wiring) and topology. The thick Ethernet (10b5) bus has been replaced by a star topology based on Unshielded Twisted Pair (IEEE 802.3/10bT) Ethernet wiring network. The AppleTalk network has been also restructured: a star topology PhoneNet network on Unshielded Twisted Pair has replaced the former LocalTalk bus. Apart from its evolutive feature, this new wiring allows each room of the laboratory to be indifferently connected to any kind of existing resources (AppleTalk/PhoneNet, Ethernet/10bT, RS232 server/concentrator serial lines), through RJ45 connectors.

IV-2.3 Network equipment

The new wiring and topology choice has implied the acquisition of some active network equipments, for both Ethernet and AppleTalk/PhoneNet networks, and for their interconnection. This equipment is detailed in the following:

1. SNMP Hub (from 3Com)
2. SNMP Hubs (David Expressnet from David Systems)
3. 2 MR9T HUB (Cabletron)
4. 1 Ethernet-AppleTalk Gateway (GatorBox from Cayman)
5. 1 PhoneNet StarController (from Farallon)
6. AUI/10bT Micro Transceivers (Allied Telesys)
7. PhoneNet StarConnectors (from Farallon)

IV-2.4 Interconnections, protocols, and services

TIMA network is interconnected with all other laboratories and schools of Felix Viallet site (downtown) with optic fiber wiring via a Cisco Ethernet router. This Router also allows this site to be connected to the ARAMIS network ("Association Rhône-Alpine des Moyens d'Interconnexion Scientifique" : the Rhône-Alpes region branch of French national scientific research network), through French Telecoms specialized lines (4 Mb/s). The main used protocol is Internet. This makes TIMA able to reach (and be reached by) any site in the world. Full Internet services are available (telnet, ftp, electronic mail, Usenet news,...).

IV-2.5 Interconnection schemes

Four schemes are given in the following pages in order to illustrate TIMA network and its external interconnections. The first scheme, "TIMA NETWORK", illustrates our own network and its link to one of the Ethernet router lines. The second scheme, "TIMA NETWORK, domaine universitaire", shows our campus network and its link to University Joseph-Fourier. The third scheme, "INPG, Site Viallet" - reprinted by courtesy of C. Rubat du Mérac, INPG network responsible - shows how all of the laboratories (including TIMA) and schools of Felix Viallet site are interconnected and how they are connected to ARAMIS network. The last scheme, "ARAMIS NETWORK" gives an overview of the different components of ARAMIS network.

IV-2.6 Contacts

Network, Server/WStations, MacIntoshes : Jean-Pierre Boyer (Jean-Pierre.Boyer@imag.fr)
TIMA NETWORK
SITE VIALLET

ARAMIS

France - Telecom

IP - Router
CISCO AGS+
18 Ethernet Lines

Optic Fiber

Optic Fiber Transceiver

Optic Fiber/Aui Repeater

Switch 14 10baseT
2 100baseT

TIMA NETWORK   TIMA NETWORK
EXTENSION

Figure IV-2 1
TIMA NETWORK
SITE VIALLET

Switch 14 10baseT
2 100baseT

Hub 1 10baseT
12 10baseT

Hub 1 10baseT
12 10baseT

Hub 1 10baseT
12 10baseT

Ethernet
AppleTalk
Gateway

PhoneNet
StarController

AppleTalk / PhoneNet Network
(MacIntoshes & Laser Printers)

Servers (Sun), PC, X Terminals
(NCD, Tatung), MacIntoshes (Ethernet)
Laser Printers (Ethernet)

Figure IV-22
TIMA NETWORK
SITE VIALLET - EXTENSION

Switch  14 10baseT
         2 100baseT

Switch  14 10baseT
         1 100baseT

Hub  1 10baseT
    12 10baseT

Hub  1 10baseT
    12 10baseT

Hub  1 10baseT
    12 10baseT

Unshielded Twisted Pair

Servers (Sun), PC, X Terminals
(NCD, Tatung), Macintoshes (Ethernet)
Laser Printers (Ethernet)

Figure IV-23
TIMA NETWORK
DOMAINE UNIVERSITAIRE

ujf.ujf-grenoble.fr

LOCAL HUBS

Unshielded Twisted Pair

-MAC - WORKSTATIONS -

WORKSTATION SUN

HUB

SERVER

-MAC - WORKSTATIONS - X TERMINALS -

Ethernet Network

Figure IV-2 4
Figure IV-25
RENATER

Ecole d'Architecture / ENT
Ecole Normale Supérieure
Centre Léon Bérard
Campus de la Doua
U2 Louis Lumière
U3 Jean Moulin
Ecole Centrale
IPL (ICP1)
Cemagref
INSERM
INRETS
ARCHAMPS
ASIDEV

SAINT-ETIENNE
Université Jean Monet
Ecole des Mines

OYONNAX
Ecole Supérieure de Plasturgie

L'ISLE-D'ABEAU
Centre Universitaire
UJF / IUT

BOURG-en-BRESSE
IUT - A

CHAMBERY
Université de Savoie

ROANNE
ARDiP

VALENCE
Pôle Universitaire
CS UJF

Fait au CICG (Février 1997)

Figure IV-26
IV-3 Financial resources

Some data are given below on financial aspects. They are provided for 1989-1997 budget years, to allow comparisons.

In 1989, the budget of the Laboratory has been 9 118 kFF (excluding VAT). This amount does not include salaries of government employees, like CNRS researchers and Professors.

This budget comes from research funds provided by CNRS or Universities (INPG and UJF), from contracts signed with industrial firms or CEC, and from "exceptional" funds or "exceptional" invoices (emitted for example against services). Those funds are accounted by either CNRS, or INPG or UJF. The Table IV-3 I gives the distribution, and the Figure IV-3 I represents it. It is to be noted that the input for contracts represent the total amount of the contracts which are signed in 1989, even if the contract will last for several years.

The contractual part represents approx. 80 % of the budget in 1989. The Table IV-3 II gives the list of contracts signed in 1989. The CEC part represents approx. 80 % of the contracts.

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<td>Exceptional invoices</td>
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<td>Contracts signed in 1989</td>
<td>335</td>
<td>6 840</td>
<td>0</td>
<td>7 175</td>
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<td><strong>TOTAL</strong></td>
<td>1 144</td>
<td>7 966</td>
<td>8</td>
<td>9 118</td>
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TABLE IV-3 I - Budget 1989 (kFF, excluding VAT)
Figure IV-3 1 - Budget 1989

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<td><strong>Total</strong></td>
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TABLE IV-3 II - Contracts signed in 1989 (kFF, excluding VAT)
In 1990, the budget has been 8,582 kFF (excluding VAT). The Table IV-3 III gives the distribution, and the Figure IV-3 2 represents it. Again, the input for contracts represents the total amount of contracts signed in 1990, even if those contracts last for several years.

In 1990, the contractual part represents approximately 43% of the budget. The Table IV-3 IV gives the list of contracts signed in 1990.

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**TABLE IV-3 III - Budget 1990 (kFF, excluding VAT)**

![Figure IV-3 2 - Budget 1990](image.png)
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<tr>
<td>CNES</td>
<td>500</td>
</tr>
<tr>
<td>TMS</td>
<td>240</td>
</tr>
<tr>
<td>MATRA ESPACE</td>
<td>292</td>
</tr>
<tr>
<td>IBM</td>
<td>285</td>
</tr>
<tr>
<td>CNES</td>
<td>150</td>
</tr>
<tr>
<td>GCIS</td>
<td>945</td>
</tr>
<tr>
<td>MIAT / JESSI AC6</td>
<td>1315</td>
</tr>
<tr>
<td></td>
<td>3727</td>
</tr>
</tbody>
</table>

**TABLE IV-3 IV - Contracts signed in 1990 (kFF, excluding VAT)**

The key issue when comparing data for 1989 and for 1990 is that the CEC EUROCHIP contract is financially important for 1989. In 1990, the part of industrial contracts has been increased. Those data are nevertheless partially sounded, because of the criterion consisting in account a contract once, the year it is signed.
In 1991, the budget has been 9,322 kFF (excluding VAT). The Table IV-3 V gives the distribution, and the Figure IV-3 3 represents it. In 1991, the contractual part represents approximately 44%. The CEC part represents 60% through ESPRIT Basic Research, and the JESSI part represents 38%. The Table IV-3 VI gives the list of contracts signed in 1991.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>165</td>
<td>0</td>
<td>265</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>712</td>
<td>2,238</td>
<td>0</td>
<td>2,950</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1,884</td>
<td>85</td>
<td>0</td>
<td>1,969</td>
</tr>
<tr>
<td>Contracts signed in 1991</td>
<td>0</td>
<td>4,138</td>
<td>0</td>
<td>4,138</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2,696</td>
<td>6,625</td>
<td>0</td>
<td>9,322</td>
</tr>
</tbody>
</table>

**TABLE IV-3 V - Budget 1991 (kFF, excluding VAT)**

---

**Figure IV-3 3 - Budget 1991**
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / ASICS</td>
<td>154</td>
</tr>
<tr>
<td>CEC / EUROCHIP</td>
<td>2352</td>
</tr>
<tr>
<td>MICE / JESSI AC6</td>
<td>855</td>
</tr>
<tr>
<td>MICE / JESSI AE11</td>
<td>727</td>
</tr>
<tr>
<td>HEWLETT PACKARD</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>4138</td>
</tr>
</tbody>
</table>

**TABLE IV-3 VI - Contracts signed in 1991 (kFF, excluding VAT)**
In 1992, the budget has been 12,118 kFF (excluding VAT). The Table IV-3 VII gives the distribution, and the Figure IV-3 4 represents it. In 1992, the contractual part represents approximately 54%. The CBC part represents 68% through ESPRIT Basic Research, and the JESSI part represents 32%.

The Table IV-3 VIII gives the list of contracts signed in 1992.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>208</td>
<td>147</td>
<td>0</td>
<td>355</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>160</td>
<td>2,370</td>
<td>0</td>
<td>2,530</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2,511</td>
<td>116</td>
<td>0</td>
<td>2,627</td>
</tr>
<tr>
<td>Contracts signed in 1992</td>
<td>0</td>
<td>6,606</td>
<td>0</td>
<td>6,606</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2,879</td>
<td>9,239</td>
<td>0</td>
<td>12,118</td>
</tr>
</tbody>
</table>

**TABLE IV-3 VII - Budget 1992 (kFF, excluding VAT)**

**Figure IV-3 4 - Budget 1992**
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>4,484</td>
</tr>
<tr>
<td>CEC / ARCHIMEDES</td>
<td>712</td>
</tr>
<tr>
<td>CEC / FASED</td>
<td>126</td>
</tr>
<tr>
<td>MICE / JESSI AC6</td>
<td>880</td>
</tr>
<tr>
<td>MICE / JESSI AE11</td>
<td>404</td>
</tr>
<tr>
<td></td>
<td>6,606</td>
</tr>
</tbody>
</table>

TABLE IV-3 VIII - Contracts signed in 1992 (kFF, excluding VAT)
In 1993, the budget has been 17 403 kFF (excluding VAT). The Table IV-3 IX gives the distribution, and the Figure IV-3 5 represents it. In 1993, the contractual part represents approximately 64 %. The CEC part represents 61 %, and the JESSI part represents 36 %. The Table IV-3 X gives the list of contracts signed in 1993.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>166</td>
<td>568</td>
<td>0</td>
<td>734</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>171</td>
<td>2 321</td>
<td>0</td>
<td>2 492</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2 859</td>
<td>247</td>
<td>0</td>
<td>3 106</td>
</tr>
<tr>
<td>Contracts signed in 1993</td>
<td>99</td>
<td>10 972</td>
<td>0</td>
<td>11 071</td>
</tr>
<tr>
<td>TOTAL</td>
<td>3 295</td>
<td>14 108</td>
<td>0</td>
<td>17 403</td>
</tr>
</tbody>
</table>

**TABLE IV-3 IX - Budget 1993 (kFF, excluding VAT)**

![Figure IV-3 5 - Budget 1993](image)
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>4258</td>
</tr>
<tr>
<td>CEC / NSF - CLC</td>
<td>325</td>
</tr>
<tr>
<td>CEC / NSF - NDIMST</td>
<td>119</td>
</tr>
<tr>
<td>CEC / COPERNICUS 93 n°9093</td>
<td>97</td>
</tr>
<tr>
<td>CEC / ARCHIMEDES</td>
<td>915</td>
</tr>
<tr>
<td>CEC / HCM - GARDEN</td>
<td>137</td>
</tr>
<tr>
<td>CEC / CHIPSHOP</td>
<td>743</td>
</tr>
<tr>
<td>CEC / EEMCN</td>
<td>73</td>
</tr>
<tr>
<td>CEC / EDAC-EUROASIC 93-94</td>
<td>99</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC6</td>
<td>880</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC8</td>
<td>1860</td>
</tr>
<tr>
<td>MIPTCE / JESSI AB11</td>
<td>414</td>
</tr>
<tr>
<td>SGS-THOMSON / JESSI AC8</td>
<td>801</td>
</tr>
<tr>
<td>CNET / SOLIST</td>
<td>350</td>
</tr>
<tr>
<td></td>
<td>11071</td>
</tr>
</tbody>
</table>

**TABLE IV-3 X - Contracts signed in 1993 (kFF, excluding VAT)**
In 1994, the budget has been 19 253 kFF (excluding VAT). The Table IV-3 XI gives the distribution, and the Figure IV-3 6 represents it. In 1994, the contractual part represents approximately 74 %. The CEC part represents 52 %, and the JESSI part represents 32 %. The Table IV-3 XII gives the list of contracts signed in 1994.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>185</td>
<td>518</td>
<td>0</td>
<td>0</td>
<td>703</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>40</td>
<td>1 824</td>
<td>0</td>
<td>0</td>
<td>1 864</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1 935</td>
<td>454</td>
<td>0</td>
<td>0</td>
<td>2 389</td>
</tr>
<tr>
<td>Contracts signed in 1994</td>
<td>0</td>
<td>13 431</td>
<td>565</td>
<td>300</td>
<td>14 296</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2 160</td>
<td>16 227</td>
<td>565</td>
<td>300</td>
<td>19 252</td>
</tr>
</tbody>
</table>

**TABLE IV-3 XI - Budget 1994 (kFF, excluding VAT)**

![Figure IV-3 6 - Budget 1994](image)
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>3 866</td>
</tr>
<tr>
<td>CEC / BARMINT</td>
<td>799</td>
</tr>
<tr>
<td>CEC / COPERNICUS THERMINIC</td>
<td>565</td>
</tr>
<tr>
<td>CEC / COPERNICUS FUTEG</td>
<td>299</td>
</tr>
<tr>
<td>CEC / AMATIST</td>
<td>1 092</td>
</tr>
<tr>
<td>CEC / GRASS</td>
<td>142</td>
</tr>
<tr>
<td>CEC / CHIPSHOP</td>
<td>701</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC6</td>
<td>1 103</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC8</td>
<td>2 887</td>
</tr>
<tr>
<td>MIPTCE / JESSI AE11</td>
<td>526</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>570</td>
</tr>
<tr>
<td>SGS-THOMSON / CIFRE</td>
<td>90</td>
</tr>
<tr>
<td>CNET / PSYCOS</td>
<td>1 200</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>300</td>
</tr>
<tr>
<td>DRET /ASTER INGENIERIE</td>
<td>156</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>14 296</strong></td>
</tr>
</tbody>
</table>

**TABLE IV-3 XII - Contracts signed in 1994 (kFF, excluding VAT)**
In 1995, the budget has been 15,018 kFF (excluding VAT). The Table IV-3 XIII gives the distribution, and the Figure IV-3 7 represents it. In 1995, the contractual part represents approximately 37%.

The CEC part represents 18%, and the JESSI part represents 65%.

The Table IV-3 XIV gives the list of contracts signed in 1995.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>235</td>
<td>600</td>
<td>62</td>
<td>0</td>
<td>897</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>17</td>
<td>2010</td>
<td>0</td>
<td>0</td>
<td>2027</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>5089</td>
<td>1381</td>
<td>0</td>
<td>0</td>
<td>6470</td>
</tr>
<tr>
<td>Contracts signed in 1995</td>
<td>0</td>
<td>4994</td>
<td>0</td>
<td>630</td>
<td>5624</td>
</tr>
</tbody>
</table>

| TOTAL          | 5341 | 8985 | 62  | 630 | 15018 |

TABLE IV-3 XIII - Budget 1995 (kFF, excluding VAT)

Figure IV-3 7 - Budget 1995
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / CHIPSHOP</td>
<td>350</td>
</tr>
<tr>
<td>CEC / KIT 106 ARCOS</td>
<td>124</td>
</tr>
<tr>
<td>CEC / KIT 107 ATAME</td>
<td>110</td>
</tr>
<tr>
<td>CEC / OMI</td>
<td>442</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC6</td>
<td>808</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC8</td>
<td>1788</td>
</tr>
<tr>
<td>SGS-THOMSON / JESSI AE102/103</td>
<td>1032</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>340</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>300</td>
</tr>
<tr>
<td>SODERN</td>
<td>330</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>5624</strong></td>
</tr>
</tbody>
</table>

**TABLE IV-3 XIV** - Contracts signed in 1995 (kFF, excluding VAT)
In 1996, the budget has been 19,211 kFF (excluding VAT). The Table IV-3 XV gives the distribution, and the Figure IV-3 8 represents it. In 1996, the contractual part represents approximately 46%.

The CEC part represents 45%, and the JESSI part represents 40%.

The Table IV-3 XVI gives the list of contracts signed in 1996.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>65</td>
<td>520</td>
<td>63</td>
<td>0</td>
<td>648</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>13</td>
<td>1 774</td>
<td>0</td>
<td>0</td>
<td>1 787</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>5 603</td>
<td>2 338</td>
<td>0</td>
<td>54</td>
<td>7 995</td>
</tr>
<tr>
<td>Contracts signed in 1996</td>
<td>0</td>
<td>2 656</td>
<td>5 188</td>
<td>937</td>
<td>8 781</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>5 681</strong></td>
<td><strong>7 288</strong></td>
<td><strong>5 251</strong></td>
<td><strong>991</strong></td>
<td><strong>19 211</strong></td>
</tr>
</tbody>
</table>

**TABLE IV-3 XV - Budget 1996 (kFF, excluding VAT)**

![Diagram showing budget distribution](image)

**Figure IV-3 8 - Budget 1996**
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / COMITY</td>
<td>1388</td>
</tr>
<tr>
<td>CEC / HIPERLOGIC</td>
<td>1300</td>
</tr>
<tr>
<td>CEC / OMIL-EUROMIC</td>
<td>424</td>
</tr>
<tr>
<td>CEC / OMIL-LIBRES</td>
<td>358</td>
</tr>
<tr>
<td>CEC / SYSLINK</td>
<td>520</td>
</tr>
<tr>
<td>MIPT / JESSI AC3</td>
<td>1322</td>
</tr>
<tr>
<td>MIPT / JESSI AC8</td>
<td>2232</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>387</td>
</tr>
<tr>
<td>BEVERLY / FUSE</td>
<td>58</td>
</tr>
<tr>
<td>MG-ANACAD</td>
<td>280</td>
</tr>
<tr>
<td>SCLUMBERGER</td>
<td>212</td>
</tr>
<tr>
<td>DGA/DRET</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>8781</td>
</tr>
</tbody>
</table>

**TABLE IV-3 XVI - Contracts signed in 1996 (kFF, excluding VAT)**
In 1997, the budget has been 17,447 kFF (excluding VAT). The Table IV-3 XVII gives the distribution, and the Figure IV-3 9 represents it. In 1997, the contractual part represents approximately 36%.

The CEC part represents 23%, and the MEDEA part represents 41%.

The Table IV-3 XVIII gives the list of contracts signed in 1997.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>TOTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>128</td>
<td>519</td>
<td>63</td>
<td>0</td>
<td>710</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>200</td>
<td>374</td>
<td>13</td>
<td>0</td>
<td>587</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2299</td>
<td>1591</td>
<td>0</td>
<td>5853</td>
<td>9743</td>
</tr>
<tr>
<td>Contracts signed in 1997</td>
<td>0</td>
<td>2696</td>
<td>2977</td>
<td>734</td>
<td>6407</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2627</td>
<td>5180</td>
<td>3053</td>
<td>6587</td>
<td>17447</td>
</tr>
</tbody>
</table>

**TABLE IV-3 XVII - Budget 1997 (kFF, excluding VAT)**

Figure IV-3 9 - Budget 1997
<table>
<thead>
<tr>
<th>CONTRACT</th>
<th>AMOUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEVERLY</td>
<td>73 800</td>
</tr>
<tr>
<td>SCHNEIDER</td>
<td>175 000</td>
</tr>
<tr>
<td>SODERN</td>
<td>120 000</td>
</tr>
<tr>
<td>SODERN</td>
<td>94 020</td>
</tr>
<tr>
<td>ECSI</td>
<td>72 000</td>
</tr>
<tr>
<td>CNES</td>
<td>200 000</td>
</tr>
<tr>
<td>CNET</td>
<td>800 000</td>
</tr>
<tr>
<td>PEUGEOT</td>
<td>400 000</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>90 000</td>
</tr>
<tr>
<td>SGS-THOMSON</td>
<td>90 000</td>
</tr>
<tr>
<td>CEC/ASSISTEC</td>
<td>401 375</td>
</tr>
<tr>
<td>MEDEA/AT-401</td>
<td>663 350</td>
</tr>
<tr>
<td>CEA</td>
<td>252 000</td>
</tr>
<tr>
<td>CEC/CODAC</td>
<td>987 350</td>
</tr>
<tr>
<td>MEDEA/AT-403</td>
<td>1 990 050</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>6 409 015</strong></td>
</tr>
</tbody>
</table>

*TABLE IV-3 XVIII - Contracts signed in 1997 (kFF, excluding VAT)*
If we consider 1989, 1990, 1991, 1992, 1993, 1994, 1995, 1996, 1997 together, then we get the global data given in Table IV-3 XIX and represented by Figure IV-3 10. Such data are more representative of the reality. Now, we get a part of the contracts which is 53% of the budget. From 1991, the average percentages of EC and JESSI/MEDEA shares are respectively 47% and 41%.

![Pie chart showing distribution of budget components: 4% research, 43% exceptional, 53% contracts.]

**Figure IV-3 10 - Budget 1989 - 1997**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>4,868</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>18,696</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>36,084</td>
</tr>
<tr>
<td>Contracts</td>
<td>67,827</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>127,475</strong></td>
</tr>
</tbody>
</table>

**TABLE IV-3 XIX - Budget 1989-1997 (kFF, excluding VAT)**
V - COOPERATIVE ACTIVITIES

Public Institutions:

MAE ("Ministère des Affaires Etrangères"), MIPT (SERICS) ("Ministère de l'Industrie, de la Poste et des Télécommunications" - "Service des Industries de Communication et de Service"), France Télécom (CNET) (France Télécom - "Centre National d'Etudes des Télécommunications"), Ministère de la Défense (DGA-DRET) (Ministère de la Défense - "Direction Générale pour l'Armement - Direction de la Recherche et de la Technologie")

Industrial contracts:

SGS THOMSON, AEROSPATIALE, SODERN, MENTOR GRAPHICS, ANACAD, BEVERLY, SCHLUMBERGER, PEUGEOT, SCHNEIDER, CNES, CEA.

V-2 European Projects

V-2.1 Summary

In the past, members of the Laboratory participated to CEC Projects like CASCADE and CVT. Presently, or recently, the Laboratory participates or has been participating to the following projects:

ESPRIT PROJECTS:

ESPRIT I : ADVICE, AIDA, SPAN
ESPRIT II BASIC RESEARCH : ASCIS, EUROCHIP
ESPRIT III BASIC RESEARCH : ARCHIMEDES, FASED, BARMINT, AMATIST, GRASS
ESPRIT III RESEARCH AND DEVELOPMENT : CHIPSHOP
ESPRIT III KIT : ARCOS, ATAME
ESPRIT IV KIT : DETERMIN, LICDST
ESPRIT IV LTR : HIPERLOGIC
ESPRIT IV RESEARCH AND DEVELOPMENT : COMITY
ESPRIT IV OMI : IUN2, EUROMIC, OMILIBRES, CODAC, ASSISTEC
ESPRIT IV BEST PRACTICE : SYSLINK
CEC/NSF Cooperation : NDIIMST, CSILS

JESSI PROJECTS : AC6, AE11, AC8, AC3, AE102, AE103

MEDEA PROJECTS : AT 401, AT 403

COMETT PROJECTS:
  COMETT I : COMET
  COMETT II : EUROSYSTEMS, EPIQCS

EUREKA PROJECT:
  EUREKA : MITHRA

TEMPUS PROJECTS:
  TEMPUS : - Advanced JEP for Microelectronics Design Methodology,  
            - MECC,  
            - Initiation of Formal Training in CAEE in Romanian Universities,  
            - Computer-aided Methods and Technical Management in Electrical Engineering Education  
            - Digital System Design Based on PLD-Technology  
            - Education for Quality Control in Electrical Industry Equator  
            - Postgraduate Education in ASIC Design  
            - EUROQUALROM: European Education in Quality for Romania  
            - Microelectronics education

COPERNICUS (PECO) PROJECTS:
  COPERNICUS (ex PECO) : - EDAC-EAST: Attendance of Central and Eastern European Engineers and Researchers to the EDAC Conference  
                         - Design of VLSI self-checking digital circuits  
                         - Developing design automation technique in ASIC and VLSI Design  
                         - CAD/CAT tools integration for sensor-based microsystems  
                         - Dependability Analysis of Complex Electronic Components and Systems  
                         - East European Microelectronics Cooperation Network of support and competence centres of Central and Eastern  
                         - Functional test generation and diagnosis (FUTEG)  
                         - EUROEAST: Extension of EUROCHIP services to Central and Eastern European Countries  
                         - THERMINIC: New Methods for Thermal Investigation of Integrated Circuits
ADVICE

(CSELT, British Telecom, CNET, TIMA, Trinity College), 1984-1989 (ADVICE I)

Automatic Design Validation of Integrated Circuits using Electron Beam

Currently, the e-beam probe is the only viable method for obtaining timing resolution and voltage information from the internal nodes of single and multilevel VLSI circuits. However, the systems available at present are essentially manually operated and the procedure for fault diagnosis can be extremely time consuming. By making use of CAD software, the ADVICE project will enable the diagnostic investigation to be automated, thereby significantly reducing the circuit development time.

The Laboratory is mainly involved in CAD-EBT interface, controllability using e-beam and diagnostic tools.

AIDA

(SIEMENS, ICL, SGS THOMSON, TIMA, University of Manchester), 1986-1990

Advanced Integrated-circuit Design Aids

The objective of the project is to master the complexity of VLSI chips (more than one million transistors within the next few years) by obtaining a drastic improvement in design methods. CAD tools, new methods and concepts will be defined, proved on experimental software and finally developed into industrial tools integrated into the existing CAD environments of the partners. AIDA intends to explore the application of modern programming techniques and knowledge-base engineering to CAD tool development. It will constitute a design assistant that proposes solutions rather than merely records and validates the designer's ideas. This will allow the designer to apply his creativity where it is most efficient, leading to improved design quality. Modern programming techniques will be applied (e.g. those developed for expert systems to VLSI-CAD tools).

More specifically, the Laboratory is in charge of exploring the design of structured control-sections and/or structured datapaths in order to make them self-checking and give them built-in testability.
SPAN

(THORM-EMI, CIMSA-SINTRA, CTI, INESC, PCS, TI MA, University College London), 1987-1990

Parallel Computer Systems for Integrated Numeric and Symbolic Processing

The objective of the Project is to investigate programming languages and parallel architectures for the integration of symbolic and numeric processing, and to develop a common virtual machine. The project is organized in distinct layers: application software packages, high level languages and tools, the "virtual machine" kernel system, and parallel architectures. The Laboratory is specifically involved in the architecture of a Prolog system, integrating numeric processing.

At the time of writing this report, proposals are being submitted to the ESPRIT II Programme, mainly on fault-tolerant, real time, embedded architectures.

**ESPRIT-II Basic Research**

ASCIS


Architecture Synthesis for Complex Integrated Systems

The research in ASCIS is aimed at addressing future ICs which will contain the equivalent in logic of 16 million memory cells. Currently complex systems are mapped into Silicon starting from an architectural description level. However, the bottle-neck in such mega-chip designs lies not in realizing the layout from this register-transfer level description, but in mapping the behaviour intended into a suitable architecture. Therefore, in order to fully exploit the integration complexity of future fabrication technologies it is crucial to provide a specification at the highest system level. Problems related to this change of specification level are fundamental in nature.

The topics to be addressed are the system definition, the system partitioning, the mapping of subsystems into architectures, and the architectural synthesis of control sections. The Laboratory will focus on behavioral partitioning, architectural exploration and cooperative data paths.

EUROCHIP

(GMD, CMP, IMEC, University of Lyngby, RAL), 1989-1994

Service organisation of the VLSI Design Action

This service will provide European Universities with a number of services including access to chip manufacture and procurement of additional worksations, test equipment and CAD software. CMP is a member of the Service Organisation.
ARCHIMEDES

(TIMA, Univ. of Karlsruhe, Montpellier, Hannover, Bologna, Barcelona, & INESC), 1992-1995

ARCHitectural MEthodologies for aDVanced tE sting of VLSI Systems.

This project takes place in the framework of: “Algorithms for design methodologies for complex circuits and digital optical systems” (area V - Basic Research). The objective is to develop methodologies in order that the advances allowed by the technology and the use of powerfull CAD tools will not be jeopardized by the testing bottleneck.

The project goes deeper in the research by considering:
- architectural synthesis
- on-line and off-line testing together
- built-in test of analog parts
- defect modeling, from process simulation to circuit simulation
- IC defects-based back annotation of circuit faults
- combined detection techniques (voltage and current testing)
- IC defects-based fault models for analogue building blocks
- advanced fault simulation of CMOS compatible designs (BiCMOS)
- optimized built-in test generation for BIST
- automatic design rule checking for self-checking circuits.

FASED

(IMS, TIMA, Politecnico di Milano), 1992-1994

Failsafe Integrated Digital Electronics with Semicustoms

Electronic components are increasingly being employed in safety critical systems. The introduction of application specific VLSI circuits to these areas is hampered by long design times and consequently high cost of self-checking and fail-safe integrated circuits. In this proposed basic research action, these issues are to be addressed by extending the use of semicustom technologies to fail-safe circuits.

BARMINT


BAasic Research for Microsystems INTEGRATION

Microsystems that integrate data processing along with sensors and actuators will face an important development during the next years. The objective of the BARMINT project is to participate to the development of microsystems along three main axes: a) the tools for top-down design that bring methods for developing microsystems in a way similar to present ASICs, b) the technological compatibilities between silicon based VLSI, micromachined silicon in micromechanics, integrated optics obtained by
micromachining of silicon or of special polymers, and chemical sensors with membranes, c) the assembly operations that focus on typical compatibility problems for including various components within a single multichip microsystem.

AMATIST

(CNM Sevilla, MESA Institute - Univ. of Twente, TIMA, Univ. of Cantabria, Univ. of Lancaster, Univ. of Pavia),
1994-1997

Analogue & Mixed-signal Advanced Test for Improving System-Level Testability

This project intends to develop new concepts enabling to improve the performance of mixed-signal integrated systems through the incorporation of on-line test functionality. This will be carried out by addressing three different issues: a) the introduction of circuit architectures which can be used to ensure a continuous signal monitoring during the system field operation, b) the development of Design-For-Testability and off-line test generation methods especially tailored to the systems under study, and c) the validation of the new architectures and methods by using them to implement actual integrated applications.

GRASS (Working Group)

(Univ. de Las Palmas de Gran Canarias, TIMA, Middlesex University, Techn. Univ. of Denmark, EPFL, Fraunhofer-Gesellschaft Erlangen),
1994-1997

Gallium arsenide Research action on ASic Synthesis

The emerging commercial markets in the communication, computer, automotive and broadcast industries will produce an increase of more than 30% every year in both the digital and analogue GaAs device markets. The aim of this project is to improve the knowledge of European researchers on mixed mode Gallium Arsenide VLSI integrated circuit design, and to generate facilities for allowing the reliable design of such circuits. Effort is targeted for fast digital signal processing and other very high speed applications such as broadband telecommunications, hardware accelerators and workstations. It aims at delivering a design environment with the same level of performance in quality and design time for GaAs as is available for silicon to ASIC designers in Telecom and Information Processing fields.

ESPRIT-III Research and Development

CHIPSHOP

(SCME, FhG-IIS, LETI, CMP, CNR-PF, IAM, GAME, INESC, INTRACOM, ElektronikCentralen, CNM, Nordic VLSI, ERA, ULVC),
1992-1994

A low-cost IC prototyping production service for small and medium sized enterprises.

CHIPSHOP is a pan-European initiative supported by the Commission of the European Communities in the framework of the ESPRIT programme to provide MPW services to
SMEs from EC and EFTA countries, in connection with the JESSI-SMI Project and with Special Actions in Greece, Portugal, Italy and Spain. Chip fabrication is carried out by 5 different foundries and testing interfaces: CMP in France, Fraunhofer-Institute for Integrated Circuits (FhG-IIS) in Erlangen in Germany, CNM in Spain, Nordic VLSI in Norway, ElektronikCentralen in Denmark and CSATA in Italy. CMOS and BiCMOS technologies will be offered to support analog, digital, mixed, high voltage and high frequency applications. CHIPSHOP offers more services besides prototype fabrication: testing, small volume production, CAD software, FPGA migration.

**ESPRIT-III KIT ("Keep-In-Touch")**

**ARCOS**

(IMEC, TIMA, University of Sao Paulo),
1995-1997

**ARChitectural synthesis of COnplex Systems on silicon**

The main goal of the project is to assess, optimise and transfer a new design methodology for complex systems on ASICs by using high level synthesis techniques. This goal will be reached by selecting several relevant applications, defined by the non-EU site and perform the complete design process as a driving test vehicle for the software developments of the high level synthesis systems CATHEDRAL and AMICAL. During this project, experts of different fields will work together, i.e. algorithm developers, hardware architects and CAD software specialists. It is clearly understood that today the combination of expertise from these three gravitation centres is what makes human designer teams (and their designs) successful. At the start of this project, two powerful high level synthesis environments are made available by the EU-sites. These include CATHEDRAL, a high level synthesis environment for the realisation of data flow dominated DSP algorithms and AMICAL, a high level synthesis environment for architecture synthesis of control oriented applications. The research activities proposed in this project will produce new tools that will be integrated in the existing environment, leading to more powerful compilers. These new activities result from the feedback that is collected from application studies that will be undertaken by the non-EU site.

**ATAME**

(IMEC, TIMA, Polytechnical Univ. of Madrid, Institute of Microelectronics - Singapore National University),
1995-1997

**Advanced Telecom And Multimedia design technology Environment**

The activities in this project are aimed at improving the design productivity for the implementation of telecommunication and multimedia systems in hardware and software. Due to the competitiveness in these application fields, reducing both the design time as well as the risk of re-design is of key importance. The goal of the project is to apply advanced design technology tools to new product developments, such that optimized designs can be delivered in a minimal time. Thereby the key point is that it is not possible to use a single software technique to accomplish every task, but to achieve the closest possible integration of powerful, specialized software design tools.
ESPRIT-IV KIT ("Keep-In-Touch")

DETERMIN

(Technical University of Budapest, TIMA),
1998-2001

DEvelopment of Tools and Expertise for the thermal investigation of ICs and microsystems
based on the results of the THERMINIC project

In the framework of this KIT project the Partners will continue the cooperation started in
the THERMINIC CP940922 COPERNICUS project.
The scientific and technical objectives of the DETERMIN project on the basis of the
THERMINIC project can be summarised as follows:
- to step forward in the development of novel measurement and simulation tools based
  on the results of the THERMINIC,
- to carry on with the thermal characterisation of IC packages with the help of the
  thermal benchmark chip developed in the THERMINIC project,
- to study further the feasibility of integrating temperature sensors into safety-critical,
  self-checking systems and to develop self-checking versions of the temperature
  sensors developed in the framework of the THERMINIC project.
- to exploit new ideas in the field of IDDQ testing,
- to continue the series of the THERMINIC workshops.

ESPRIT-IV KIT ("Keep-In-Touch")

LICDST

(LIRMM, PUC-RS, Univ. Autonoma de Barcelona, ES2, TIMA),
1997-1999

Library Free Integrated Circuit Design for Submicron Technologies

This project will concentrate the research effort in low level synthesis, specially by
improving the current state-of-the-art in this field, developing strategies for library free
mapping, virtual libraries, automatic layout synthesis for submicron technologies and
performance optimization.
For that, the following activities must be developed by the partners:
- Circuit partition;
- Library free technology mapping;
- Accurate power and timing models for performance prediction and characterization;
- Critical path extraction for timing/power estimation;
- Test vector generation;
- Automatic layout synthesis;
- Layout style definition for submicron technologies;
- Specific compactor improvement for the linear-matrix layout style;
- Global router for the « sea-of-macrocells » approach;
- Gate resizing and/or buffer insertion.
ESPRIT-IV Long Term Research

HIPERLOGIC

(IMS, TIMA, IMC, IPVR, TUB), 1996-1999

Thousand MOPS per MilliWatt CMOS High PERformance LOGIC

This project is a REACTIVE LONG TERM RESEARCH project for the Information Technology Program.
Objectives and Industrial Relevance: The HIPERLOGIC project proposed is expected to extend the limits of today's best performance/power ratios by a factor of 1000. The HIPERLOGIC project will yield an innovative masterslice chip structure of high functional density. The objectives of high system performance at low power consumption will be achieved due to an innovative silicon-on-insulator CMOS process with three-dimensional integration and a circuit design optimally tuned to this technology.

The key issues of the project are:
- 3D SOI technology
- .1μm device modelling and characterisation
- System architecture and synthesis

ESPRIT-IV Research and Development

COMITY

(VERILOG, AEROSPATIALE, BMW, INTRACOM, C-LAB, DIT/UPM, ISI, TIMA), 1997-1999

Codesign Method and Integrated Tools for Advanced Embedded Systems

The main goal of the COMITY project is to improve and promote an engineering methodology with an associated toolset for the entire design cycle of complex embedded systems. COMITY will provide system designers and software and hardware designers with modelling techniques at multiple levels of abstraction, and by using a common framework based on virtual prototyping to explore architectural solutions and trade-offs before software and hardware being fabricated. The major expected impacts are a drastic reduction of the time-to-market and development costs, with a better mastery of requirements changes and technological solutions. The project results will consist in a complete solution for system prototyping and HW-SW engineering, applicable from early stage in the development process. The toolset will be made of both mature and industry-proven technologies, and advanced solutions resulting from R&D institutes. It will be customized and validated by industrial experiments for the three following application domains: aerospace, automotive and telecom.

ESPRIT-IV OMG

IUNZ

(CMP, UNED, Archimedes, IMEC, OMIMO, Sussex University, TODITEC and UPM), 1995-1996
Inter University Network

The IUN2 project is part of a OMI global dissemination strategy that connects Universities all over the world interested in the OMI activities. The partners will achieve this goal using their strong links with the academic world. Up to now more than 300 European institutions are members of the IUN2 project. This network will be extended to non-EU European Countries as well as the rest of the world. The partners will promote the use and fast dissemination of technologies emerging from the OMI initiative.

EUROMIC

(CMP, FhG, IMEC, OMIMO, Sussex University and UPM),
1996-1997

EUropean OMI Centres

The EUROMIC project aims to act as a gateway to foster relationships between all members of the OMI community. The goal of this project is to allow European industries to fabricate their integrated systems at a reduced cost in an easy and fast way. To achieve it they will set up a network of OMI user support nodes which provide services to meet the needs of SMEs including training, design support, licensing issues, manufacturing and promotion of best practices in application systems design. The network will act as a brokerage service between users and suppliers of microprocessor technology.

OMILIBRES

(CMP, Alcatel Mietec, Compass, Mentor, Nokia, SIDSA, Telefonica I+D, Thomson-CSF and Viewlogic),
1996-1997

OMI LIBRARY REPRESENTATION STANDARDS

The OMILIBRES project aims at defining and prototyping a standardised library data representation for core and supercell model information. The standardised database could comply with the overall criteria of reusability of the models, modularity of the information and extension of the data representation in order to integrate the objectives of the OMI programme.

CODAC

(IMEC, CoWARE, ARM, Alcatel-Mietec, SGS-Thomson, Alcatel-Bell, INTRACOM, TIMA),
1997-1998

Co-design for Applications with Embedded Cores

The main objective of the project is to develop and consolidate a new generation of methods and tools for the design of embedded systems on silicon. A key issue of this environment is the synthesis of hardware/software interfaces at different levels of abstraction and the capability of efficiently integrating processor core models at different levels of abstraction in the design flow. The objective is to build a generic
system design environment, called CoWARE, which will be available on the market. The CoWARE design environment and methodology will be validated for the realisation of complex systems that require rapid integration, reuse of emerging system building blocks and probability of design specifications over several product families. The third objective of this project is to pave the path to the commercialisation of this new generation system design tools by transferring the technology to a start-up company, CoWARE N.V., that will focus on tool delivery for hardware/software synthesis and co-simulation and support fabless processor core vendors.

(IPRIAS Ltd., DOLPHIN INTEGRATION, SEND, SYNDESIS Ltd, TIMA),
1997-1999

Assistance to SMES in the pre-licence phase of the exploitation of their intellectual property

The goal of this project is to provide a comprehensive support service to companies wishing to trade Intellectual Property (IP) in the micro-electronic area. This service helps enterprises, especially Small and Medium-sized Enterprises (SMEs), to prepare and exploit their IP (e.g. through licensing). The team will offers special assistance in access to private finance, access to foundries and manufacturing services and in the pre-license phase: strengthening access to partners, preparation assistance, negotiation guide-lines, simpler contracts and IPR licensing for "standardised" components, etc.

ESPRIT-IV Best Practice

SYSLINK

(GMD, Politecnico di Torino, TIMA),
1995-1997

Linking System Designers and CAD Developers in Europe

SYSLINK is a consortium of three institutions. The main objective of this Dissemination Activity (DA) is to disseminate the results of the ESD projects, both of Application Experiments (AE) and of Demonstration Projects (DP) to the electronic system design community in Europe. For this purpose, there is first a collection process of information on methods, tools, approaches and experiences in the area of electronic system design; this may include novel design methods and tools from CAD vendors and stable prototypes from European research activities. The main results expected from this activity are to build up a broad level of know-how on electronic system design methods and tools including their merits and shortcomings with respect to a wide area of practical application. The expected impact is that such knowledge will serve to considerable improve the quality and efficiency of system design products on a large scale. Also the project should contribute to shorten the learning curve for new system designers resulting in shorter time-to-market products at a higher level of product quality.
CEC/NSF Cooperation

**NDIMST**

(University of Texas at Austin, TIMA),
1993-1995

New Directions In Mixed Signal Test

The objective of the proposed cooperation is to find new approaches to deriving high quality tests for mixed-signal circuits. Much of the work in test has been focused on digital circuits. With the increasing levels of integration, and applications such as automotive, notebook computers, and communications, analog and digital functions are being integrated on a single chip. Appropriate fault models and efficient test generation algorithms need to be generated for mixed-signal circuits if we are to produce defect-free chips, and on-line detection.

**CSLS**

(University of California at Irvine, TIMA),
1994

Circuit and System-Level Synthesis

The goal of this cooperation is to develop a global solution for behavioral and System-Level Synthesis. This cooperation will be based on the integration of SpecChart, the system-level synthesis tool developed at Irvine, and AMICAL, the behavioral synthesis tool developed at Grenoble. This integration will produce a unified synthesis environment for circuit and system design.

**JESSI**


Industrial partners :

- Philips, Eindhoven/Hamburg
- Siemens, Munich
- SNI, Munich
- EZM, Villach
- SGS Thomson, Grenoble
- Thomson-CSF/TMS
- Alcatel/Bell, Antwerp

Associated partners :

- University of Karlsruhe together with "Forschungszentrum-Informatik" in Karlsruhe
- University of Hannover
- Technical University of München
- University of Erlangen-Nürnberg
- TIMA
- Twente University of Technology, Enschede, The Netherlands
- Bennetts Associates, Southampton.

Industrial partners :
Bosch, Reutlingen
SGS-Thomson, Grenoble
Siemens, München
SEL-Alcatel, Stuttgart
Porsche, Weinhach

Associated partners :
University of Hannover
TIMA

AC8 : Integrating AMICAL within industrial CAD environment, 1993-1994

Industrial partners :
AHL
Bosch
Bull
Philips
Siemens
Siemens-Nixdorf
SGS-Thomson
Synthesia
Thomson-TCS

Associated partners :
TIMA

AC3 : HDL, Component Modeling and Libraries

Industrial partners :
Anacad
Bosch
Bull
CNET
IBM France
SGS-Thomson
SPEED
Thomson-SCTF
Thomson TCS

Associated partners :
TIMA

AE102/AE103 : Conception de circuits ATM, 1996-1998

Industrial partners :
SGS-Thomson
Italtel
Telefonica I+D

Associated partners :
TIMA
MEDEA PROJECTS

AT 401 : High Quality Design in Deep Submicron Technology

(SGS THOMSON Microelectronics, Philips, Siemens, TIMA), 1997

High Quality Design in Deep Submicron Technology

The project targets to develop new design tools and methods, new characterization tools and methods. Technological challenges in system on a chip designs: design complexity management, optimum use of silicon performances, decrease of time to market.

AT 403 : System level Methods and Tools

(SGS-THOMSON, ALCATEL, BULL, PHILIPS, COWARE, EONIC, EDC, IMEC METASYMBIOSE, UPMC, TIMA), 1997

System level Methods and Tools

The project targets the necessary methods, design flows and tools to support development of complex VLSI, representative of the "System-on-a-Chip" approach, where both HW and SW parts have to be designed and optimised concurrently. In this sense, the project will support the development of innovative circuits, including Multimedia, Communication, Smart-cards and Automotive applications. The goal of this project is to develop methods, design flows and prototypes, usable by partners plus some selected users and to prove the industrial value of the methods and to make the next step towards productisation of the design flows and prototypes.

COMETT I

COMET

(IMEC, TIMA, Universities of Darmstadt, Limerick, Lyngby, Madrid), 1988-1990

Consortium for microelectronic training

This project is aimed at providing education on ASICs at several levels and for several interest groups, but especially for the SMIs in each country.

COMETT II

(University of Darmstadt, IMEC, University of Lyngby, TIMA)

This project is a complete programme for advanced microelectronics system design fulfilling the future trends of European industry.
EPIQCS: MASTERS DEGREE SPECIALIZED IN QUALITY OF COMPLEX INTEGRATED SYSTEMS

(INPG, Imperial College of London, Universities of Darmstadt and Eindhoven)

This project aims at providing a Masters Degree in cooperation with 3 main academic partners and numerous industrial partners. The 4 platforms will be specialized in Software, Telecom, Hardware and Space.

MITHRA

(BROSSARD, BERTIN, ITMI, SEIV, LAMM, ELKRON, OLMAT, SEPA, EPFL, CERBERUS, TIMA),
1988-1990

MITHRA deals with integrated electronics for surveillance mobile robots. It is a project in which industrial firms from France, Italy and Switzerland are participating. Several research laboratories from INPG and LAMM at Montpellier are also participating. The experience of the Laboratory might be used to design circuits to replace several printed circuits boards.

TEMPUS

ADVANCED JOINT EUROPEAN PROGRAMME FOR MICROELECTRONICS DESIGN METHODOLOGY

(University of Darmstadt, Technical University of Budapest, IMEC, University of Lyngby, TIMA, Institute of Electron Technology of Warsaw)

This is a transeuropean programme on microelectronics.

MECC (Management, Electronics, Computer science)


This is a transeuropean programme on management, electronics, computer science.
INITIATION OF FORMAL TRAINING IN COMPUTER AIDED ELECTRICAL ENGINEERING IN ROMANIAN UNIVERSITIES

(TIMA, ENSIEG/INPG, Univ. of Bucuresti, Bath, Genova, Cassino, Paris 6 & 11, Graz, EDF, Politecnico di Torino)

This is a transeuropean programme for the development of education capabilities at higher education level in applied sciences in engineering areas.

COMPUTER-AIDED METHODS AND TECHNICAL MANAGEMENT IN ELECTRICAL ENGINEERING EDUCATION

(Technical Univ. Budapest, Univ. Karlsruhe, Univ. Erlangen-Nürnberg, University College London, TIMA, Univ. of Pisa, Techn. Univ. of Delft, MOTOROLA GmbH, TEXAS INSTRUMENTS DEUTSCHLAND, HEWLETT PACKARD, DIGITAL EQUIPMENT, IBM)

This is a transeuropean programme for updating technical and technical-management studies.

DIGITAL SYSTEM DESIGN BASED ON PLD-TECHNOLOGY

(Technische Hochschule Darmstadt, TIMA, Tallinn Technical Univ.)

This is a transeuropean programme for introducing into university education the methodology and concepts of designing semicustom ASICs.

EDUCATION FOR QUALITY CONTROL IN ELECTRICAL INDUSTRY (EQUATOR)

(Technical Univ. of Brno, Czech Technical University of Prague, Technical Univ. of Ostrava, Leeds Metropolitan Univ., Bournemouth Univ., TIMA, Univ. of Hull)

The objective of this project is to upgrade the university education, new degree courses for Quality management, training courses, students and lecturers mobility.

POSTGRADUATE EDUCATION IN ASIC DESIGN

(Warsaw Univ. of Technology, Technical Univ. of Lodz, Univ. of Mining and Metallurgy of Cracow, TIMA, Technische Hochschule Darmstadt, Eindhoven Univ. of Technology, Helsinki Univ. of Technology)

Preparation of the teaching staff for a centre for postgraduate training in ASIC design.

EUROQUALROM: EUROPEAN EDUCATION IN QUALITY FOR ROMANIA

(Univ. "POLITEHNICA" of Bucharest, Academy for Economic Studies of Bucharest, Univ. of Oradea, Univ. of Pitești, TIMA, "Ecole Nationale Supérieure des Arts et Métiers" of Paris, Univ. Aberta of Lisbon, Univ. Politecnica de Catalunya of Barcelona, Univ. of Piraeus, Politecnico di Torino, Univ. of Angers, Univ. of Paisley, Romanian Foundation for Quality Promotion of Bucharest, Romanian Society for Quality Assurance of Bucharest, Erasmus Univ. of Rotterdam)
The project EUROQUALROM has as main objective the modernisation of the existing courses and teaching methods in the field of quality and the upgrading/restructuring of long cycle curricula (under-graduate studies) to include quality assurance and quality management for industry (focused on electrical engineering).

**MICROELECTRONICS EDUCATION (MOBILITY SCHEME FOR SCIENTISTS)**

Grant received by S. PIESTRAK from Technical University of Wroclaw, Poland.

**COPERNICUS**

COPERNICUS : Cooperation in science and technology with Central and Eastern European countries.

*European Conferences, workshops and training seminars:*

**EDAC-FAST : ATTENDANCE OF CENTRAL AND EASTERN EUROPEAN ENGINEERS AND RESEARCHERS TO THE EDAC CONFERENCE**

*Mobility scheme for scientists :*

**DESIGN OF VLSI SELF-CHECKING DIGITAL CIRCUITS**

(Stanislaw PIESTRAK, Technical University Wroclaw, Poland)

**DEVELOPING DESIGN AUTOMATION TECHNIQUE IN ASIC AND VLSI DESIGN**

(Tania VASSILEVA, Technical University Sofia, Bulgaria)

**CAD/CAT TOOLS INTEGRATION FOR SENSOR-BASED MICROSYSTEMS**

(Teodor CALIN, Polytechnical Institute of Bucharest, Romania)

**DEPENDABILITY ANALYSIS OF COMPLEX ELECTRONIC COMPONENTS AND SYSTEMS**

(Ioan BACIVAROV, Polytechnical Institute of Bucharest, Romania)

*Pan European Scientific Networks :*

**EAST EUROPEAN MICROELECTRONICS COOPERATION NETWORK OF SUPPORT AND COMPETENCE CENTRES OF CENTRAL AND EASTERN EUROPEAN COUNTRIES**

Joint Research Proposals:

FUNCTIONAL TEST GENERATION AND DIAGNOSIS (FUTEG)

(Technical University of Tallinn - Estonia, Kaunas University of Technology - Lituanian, Institute of Computer Systems Bratislava, Technical University of Budapest, TIMA, FhG-IIS-EAS Dresden)
1994-1997

The focus of the project is directed towards the investigation of functional and behavioral test generation and diagnosis at the system level. The different partners will put in common their expertises in this area, in order to provide different approaches to this topic. These approaches will be validated by experiments and comparatively analyzed. Finally, their integration into a combined methodology is intended. This project, which manpower is 25 persons-year, over a duration of 36 months, is expected to start in January 1994.

EUROEAST: EXTENSION OF EUROCHIP SERVICES TO CENTRAL AND EASTERN EUROPEAN COUNTRIES

(GMD, CMP, DTH, IMEC, RAL, Polytechn. Bucharest, ITME Warsaw, Warsaw University, Silesian Tech. Univ., Slovak Tech. Univ.)

NEW METHODS FOR THERMAL INVESTIGATION OF INTEGRATED CIRCUITS (THERMINIC)

(Technical University of Budapest, Hungary, Technical University of Lodz, Poland, Technical University of L'viv, Ukraine, SEMILAB Budapest, Hungary, TIMA)
1995-1997

One of the greatest challenges of our days in microelectronics are the overheating problems. The increase in the power density in integrated circuits, caused by the actual small features sizes, moreover the advent of 3D packages cause severe heat dissipation problems. This project intends to treat this problem in its complexity and approximate it in different ways, resulting in the development of new thermal monitoring methods and elements as well as new thermal investigation methods and tools.

HUMAN CAPITAL AND MOBILITY

GARDEN

(Univ. de Las Palmas de Gran Canarias, TIMA, PHILIPS Electr. Laboratories, Middlesex University, Techn. Univ. of Denmark, EIDG. Technische Hochschule at Zurich, Fraunhofer Institut für Angewandte Festkörperphysik at Freiburg, Fraunhofer Institut für Integrierte Schaltungen at Erlangen, GIGA at Brondby, Thomson CSF)

Gallium Arsenide Reliable Design ENvironment

This project aims at delivering a design environment with the same level of performance in quality and design time for GaAs as available for silicon, to ASIC
designers in Telecom and Information Processing fields. This goal will be achieved by two actions. Firstly, a research and cooperation network: "The European Network on Gallium Arsenide VLSI Design", will be established within the Human Capital and Mobility Programme of the European Community. Secondly, a research and development project will be launched again through the Human Capital and Mobility Programme, which will center cooperation between laboratories in the network and will provide mobility for advanced research and training at each other sites according to special capabilities and expertise.

**LATIN AMERICA HIGHER EDUCATION (Amérique Latine Formation Académique : ALFA)**

**HUERTA**

(Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil ; Universidade Federal do Rio de Janeiro/COPPE, Rio de Janeiro, Brazil ; Universidad del Valle/INTEDI, Cali, Colombia ; Universidad Autonoma Metropolitana, Mexico, Mexico ; Univ. Catholique de Louvain, Louvain La Neuve, Belgium ; TIMA ; Technische Hochschule Darmstadt, Darmstadt, Germany ; Universidade de Aveiro, Aveiro, Portugal)

Higher University Education and Research Training Action

This package concerns two projects. The B1 project, entitled « Design, Synthesis and Test of Digital Systems » aims at defining a mobility scheme for PhD and MSc students from Latin America, as well as providing high-level training sessions for Professors in order to disseminate the most recent information on technologies and tools related to the design, synthesis and test of digital systems. The B2 project, entitled « Synthesis of Testable Circuits and Systems », aims at defining common research projects related to high-level synthesis for testability, a current hot research topic. Both projects aim at facilitating the technology transfer between the EU and LA in the field of microelectronics, which is crucial for the technological development of LA countries, expected to have a strong impact from the social and economical points of view. The three LA countries involved in the HUERTA network will constitute a kernel for scientific and technological information dissemination in the remaining of Latin America.

**ELACIAC**

(Universidad Nacional de Rosario, Instituto de Física de Rosario, Rosario, Argentina ; Universidad de Chile, Facultad de Ciencias Físicas y Matemáticas, Departamento de Ingeniería Eléctrica, Santiago, Chile ; Escuela de Ingeniería "Mcal. Antonio José Sucre", La Paz, Bolivia ; Universidad de Guadalajara, Centro Universitario de Ciencias Exactas de Ingeniería, Mexico ; TIMA ; School of Engineering, University of Wales Cardiff, UK ; Technische Universität Clausthal, Institut für Elektrische Informationstechnik, Germany ; Universidad Politécnica de Madrid, Departamento de Señales Sistemas y Radiocomunicaciones, Madrid, Spain)

European-Latino American Cooperation for Intelligent Automation and Control.

This project specifies the organization of technical meetings within the ELACIAC network to devise a common research project titled "NIACS: Novel Intelligent Automation and Control Systems". The objective of the ELACIAC network is to
merge and enhance the experience of the cooperating institutions in order to
develop innovative approaches, methods and tools for increasing the efficiency of
Automation and Control Techniques. The research work will be based on results of
ongoing or accomplished national, Latin-American, or European Research projects
and will be carried out in close collaboration with industrial endorse.

V-3 International cooperation agreements

The Laboratory is engaged, or has been recently engaged, in a number of cooperations, some of
them being officially recognized. They are listed below. These cooperations allow to remote
researchers at the cooperative location for in-deep fruitful exchanges of results, to organize joint
research and Workshops.

Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB,
with R. REIS, on the automatic design of integrated circuits.

Universidade Federal do Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB,
with A. MESQUITA, on high level synthesis and test of integrated circuits.

Ecole Nationale d'Ingénieurs de Monastir (ENIM), Monastir, Tunisia
This cooperation takes place in the framework of a project sponsored by the French ministry for
education and research and the Tunisian ministry for research and technology, cooperation
program which name is "Réseaux Formation-Recherche franco-tunisiens", with S. NASRI, on
computer-aided design of communication-dedicated circuits.

Technical University of Budapest, Hungary
This cooperation takes place in the framework of BALATON, between France and Hungary. The
project deals with thermal investigations of ICs and systems, with the Department of Electron
Devices: V. SZEKELY and M. RENCZ. Renewal of this action has been approved for 1998.

Warsaw University of Technology, Poland
French-Polish scientific and technological cooperation joint projects for year 1997. This
cooperation allows short and long visits to France and Poland.

European Molecular Biology Laboratory, Heidelberg, Germany
This cooperation is carried out with C. BOULIN on the design of microsystems for molecular
biology analysis.

University of California at Berkeley, USA
A research project entitled « Multi-standard verification environment for digital system design »
is supported by the France-Berkeley Fund. This cooperation is carried out with the group of
Robert BRAYTON, on the topic of model checking from Verilog and VHDL.

Universidad Politecnica de Catalunya (UPC/ETSI), Spain
This cooperation (PICASSO) is carried out with J. CABESTANY on the study of Robustness of
Digital Implementation of artificial neural networks, with exchanges of students and researchers
between TIMA and UPC.
Faculté des Sciences de Monastir, Tunisia
This cooperation takes place in the framework of TEMPR3A, between France and Tunisia. The project deals with FPGA to ASIC retargeting, with Electronic and Microelectronic Laboratory: M. ABID.

V-4 National cooperation

A network of French Laboratories had been set up in 1995 by the Ministry for Research and Education in the field of CAD for integrated circuits and systems. These Laboratories are CSI in Grenoble, ENST in Paris, IEMN in Lille (Villeneuve d'Ascq), LIRMM in Montpellier, MASI in Paris, and TIMA in Grenoble acting as the contractor to the Ministry. On January 1998, the initial network has been completed by more laboratories, namely ENSEA, INSa Toulouse, IRESTE, IRISA, IS, LAMI, LASTI, LCIS, LESTEA, LIM, LIP, to constitute a group of Laboratories supported by CNRS. The group is leaded by TIMA. The main topics for research are the design of mixed systems (hardware-software, microelectromechanical-analog), and CAD for deep submicron.

V-5 International activities

This section gives an overview of national and international activities to which participated recently the members of the Laboratory.

Participation to Committees for Conferences and Workshops

- European Design for Testability Workshop : 1990 (Segovia), 1992 (Brugge), 1996 (Montpellier), 1998 (Sitges)
- ICCAD : 1991-1993 (Santa Clara), 1994 (San Jose), 1995 (Santa Clara), 1996-1997 (San Jose)
- European Solid-State Circuits Conference : 1986 (Delft), 1990 (Grenoble), 1995 (Lille), 1997 (Southampton)
- International Conference on Microelectronics : 1991 (Cairo), 1992 (Monastir), 1993 (Dahran)
- European workshop on Dependable Computing: 1989 (Toulouse)
- CEC CAVE (CAD for VLSI in Europe) workshops: 1983-1988
- Memory Testing: 1993-1995 (San Jose), 1996 (Singapore), 1997 (San Jose)
- High Level Synthesis Workshop: 1994 (Niagara Falls), 1995 (Cannes), 1996 (La Jolla)
- EuroDAC-EuroVHDL: 1994 (Grenoble), 1995 (Brighton), 1996 (Geneva)
- Workshop on Hardware-Software Codesign: 1994 (Grenoble)
- Simulation in Electronics: 1994 (Santander)
- Asia Pacific Conference on Hardware Description Languages: 1993 (Brisbane), 1994 (Toyohashi), 1996 (Bangalore), 1997 (Taiwan), 1998 (Seoul)
- International Conference on Probabilistic Safety Assessment and Management: 1991 (Beverly Hills), 1996 (Greece)
- European Safety and Reliability Conference: 1996 (Greece)
- International Conference on ASIC: 1996 (Shanghai), 1998 (Beijing)
- IEEE Multi-Chip Module Conference: 1995-1997 (Santa Cruz)
- MCM Test: 1995-1998 (Napa Valley)
- High Level Design Validation and Test Workshop: 1996-1998 (Oakland)
- SPIE Conference on Micromachining and Microfabrication: 1996-1997 (Austin)
- Diseño de Circuitos Integrados y Sistemas: 1996 (Barcelona), 1997 (Sevilla)
- Low Dimensional Structures and Devices: 1995 (Singapore), 1997 (Lisbon)
- Reconfigurable Architectures Workshop: 1997 (Geneva), 1998 (Orlando)
- IEEE International Conference on Electronics, Circuits and Systems: 1998 (Lisbon)
- INTERPACK’97 Conference: 1997 (Mauna Lani), 1999 (Honolulu)
- MICRO SYSTEM Technologies: 1998 (Postdam)
- IC/Package Design Integration: 1998 (Santa Cruz)
- International Conference On Computers and Information Technology: 1998 (Dhaka)
- DATE, Design Automation and Test in Europe: 1998 (Paris)
- IFIP WG10.2 International Working Conference "The fusion of hardware design and verification": 1988 (Glasgow)
- IFIP TC10 Conference "Design Methodologies for VLSI and Computer Architecture": 1988 (Fisa)
- "VHDL Forum for CAD in Europe" : 1989 to 1998 (annual)
- IFIP WG10.2 Advanced Research Workshop on Correct Hardware Design Methodologies : 1992 (Torino), 1993 (Arles)
- IFIP WG10.5 Advanced Research Working Conference on "Correct Hardware Design and Verification Methods" : 1995 (Frankfurt)
- Radiation Effects on Circuits and Systems (RADECSS) : 1997 (Cannes)
- Nuclear and Space Radiation Effects Conference (NSREC) : 1997 (Snowmass)
- Design and Diagnostics of Electronic Circuits and Systems Workshop : 1998 (Szczyrk)
- IEEE International Workshop on Design, Test and Applications : 1998 (Dubrovnik)

European representation (or liaison) to Conferences and Workshops

- Built-In-Self-Test Workshop (several issues)
- Asian Test Symposium (several issues)
- High-Level Design Validation and Test Workshop (several issues)
- VLSI Design (several issues)
- MCM Conference (several issues)
- IC/Design Package Integration (1998)
- INTERPACK (1999)
- Memory Technology, Design and Testing (several issues)
- International Workshop on System Test and Diagnosis (1998)
- ICCAD (1996-1997)

Participation to Editorial Boards of Journals

- CDTA
- Journal of Microelectronic Systems Integration
- IEEE Design and Test of Computers Magazine
- Quality Engineering Journal
- Reliability Engineering & System Safety
- Quality Observer
- Journal of The Brazilian Microelectronics Society
- Computational Mechanics Publications
- Microelectronics Journal
- IEEE Press Book Series
- Formal Methods in Design

Organisation of Conferences

- Electron and Optical Beam Testing of Integrated Circuits : 1987 (Grenoble, General Chair), 1989 (Duisburg, Program Chair), 1991 (Como, Program Chair), 1993 (Zurich, Program Chair), 1995 (Wuppertal, Program Chair)
- EUROCHIP Workshop on VLSI Design Training (General Chair): 1991-1992 (Grenoble), 1993 (Toledo), 1994 (Dresden)
- European Conference on Design Automation / EUROASIC : 1993 (Paris, General Chair)
- European Conference on Design Automation / European Test Conference / EUROASIC : 1994 (Paris, Program Co-Chair)
- Rapid System Prototyping Workshop: 1994 (Grenoble, General Chair), 1996 (Thessaloniki, Program Chair)
- International Symposium on System Synthesis: 1995 (Cannes, Program Chair), 1996 (La Jolla, General Chair)
- IEEE Mixed-Signal Test Workshop: 1995 (Grenoble, General Chair)
- IEEE Workshop on On-Line Testing: 1995 (Nice, General Chair), 1996 (Biarritz, General Chair) 1997 (Crete, General Chair)
- Workshop on Thermal Investigations in ICs ans Systems: 1995 (Grenoble, General Chair), 1996 (Budapest, General Chair), 1997-1998 (Cannes, General Chair)
- VLSI Test Symposium: 1995-1996 (Princeton, Vice-Program Chair), 1997 (Monterey, Program co-Chair), 1998 (Monterey, Program Chair)
- Euro-VHDL: 1996 (Geneva, Program Chair)
- Microelectronics Education: 1996 (Grenoble, Co-Program Chair)
- Colloque CAO de circuits intégrés et systèmes: 1996 (Grenoble – Villard de Lans, Organizer)
- NATO ASI Course on Low Power Design in Deep Submicron Electronics, 1996 (Lucca, Organizer)
- Copernicus Summer School: EDA standards, 1997 (Prague, Organizer)
- Design, Test and Microfabrication of MEMS/MOEMS: 1999 (Paris, General Chair)
- MEDEA-ESPRIT Workshop on Hardware-Software Co-design: 1998 (Grenoble, Chair)
- DATE, Design Automation and Test in Europe: 1999 (Munich, Program Chair)
- Codas/CASHE: 1998 (Seattle, Co-Chair), 1999 (Italy, Co-General Chair)
- Modeling and Simulation of Microsystems, Semiconductors, Sensors and Actuators: 1999 (Puerto Rico, Co-Chair)
- NATO ASI Course on System Level Design: 1998 (Organizers)

Participation to Societies and Working Groups

- Member of IEEE European Test Technology Technical Committee
- Vice-Chair of Technical Activities of the IEEE Test Technology Technical Committee
- Chairman of the European Design and Automation Association (1994-1995)
- Chair of Thermal Testing Activities of the IEEE Test Technology Technical Committee
- Chair of IFIP 10.5 Working Group
- Member of IEEE WG 1076.6: VHDL subset for Synthesis

Others activities

- Review of papers for numerous Journals and Conferences
- Review of research proposals for CEC, NSF, NATO, SERC

V-6 Awards and distinctions

- IEEE Meritorious service awards (1993)
- Doctor Honoris Causa of the Technical University of Budapest (1994)
- IEEE Computer Society's Golden Core member (1996)
- Best Paper Award ED&TC, 1995
As part of the international activities, Ahmed JERRAYA helps in preparing a New-Year’s cake at the SASIMI Workshop (OSAKA, 1997)
Picture V-6 1:
Bernard COURTOIS is being awarded Doctor Honoris Causa of the Technical University of Budapest

Picture V-6 2:
Later, the President of INPG, Maurice RENAUD, congratulates him by remitting a sash, made to the colours of the city of Budapest
VI - TECHNOLOGY TRANSFER ACTIVITIES

Besides their research and service activities, TIMA staff members are also concerned with technology transfer activities. For that purpose, they are regularly solicited to serve as consultant for technical and educational tasks, mainly by industrial companies, but also by foreign universities. Some results of these tasks have already been evoked throughout this report for the sake of consistency of the different sections, others only appear in this section.

Up to now, the transfer technology activities have taken the forms detailed in the following:

VI-1 Technical tasks

VI-1.1 Industrial Transfers

- Standard Mirror Board (SMB) developments, resulting from the research work made within the ADELAIDE project have been transferred to the IMD French company, which is commercialising them now on the market. Details can be found in section II of this report, description of the Quality of Complex System Group.

- The AMICAL architectural synthesis system is currently under industrial transfer process: several companies have expressed their interest. Details are given in section II of the report, description of the System Level Synthesis Group.

- The VCI Co-simulation tool has been transferred to SGS-Thomson where it is being productized and used in several divisions in Grenoble and Bristol.

- Hit cells: Heavy ion tolerant memory cells, to Matra MHS/TEMIC. Hit memory cells were used to design a radiation hardened version of a digital signal processor: the DSP/RT. The DSP/RT circuits will be commercialised second half 1998.

VI-1.2 Patents

The following patents have recently been taken:

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transparent Testing of Integrated Circuits</td>
<td>M. Nicolaidis</td>
<td>03/92</td>
</tr>
<tr>
<td>Implementation Techniques of Self-Checking Arithmetic Operators and Data Paths based on Double-Rail and Parity Code</td>
<td>M. Nicolaidis</td>
<td>04/92</td>
</tr>
<tr>
<td>Standard Mirror Board (FR 92/12549)</td>
<td>Ch. Vaucher</td>
<td>12/92</td>
</tr>
<tr>
<td>Standard Mirror Board (FR 93/09571)</td>
<td>Ch. Vaucher</td>
<td>09/93</td>
</tr>
<tr>
<td>SEU Tolerant RAM</td>
<td>F. L. Vargas &amp; M. Nicolaidis</td>
<td>06/94</td>
</tr>
<tr>
<td>Supply component of the credit card type - US patent 5449994</td>
<td>L. Balme</td>
<td>09/95</td>
</tr>
<tr>
<td>Sup. comp. of the credit card type - European patent BE0524304</td>
<td>L. Balme</td>
<td>12/95</td>
</tr>
<tr>
<td>CMOS Compatible Inertial Sensor - VK 1255003 (co-invention with David Moore, Jurgen Daniel, Cambridge University)</td>
<td>J.M. Karam</td>
<td>10/96</td>
</tr>
</tbody>
</table>
VI-1.3 Industrial Circuit Fabrication

In addition to its service activity for university and research laboratory circuit fabrication, CMP is offering circuit fabrication services for industrial circuit prototyping and low volume production. Thus 86 industrial prototypes (32% up compared to 1996) coming from 36 Industrial Companies or National Research Laboratories were fabricated in 1997.

Starting from 1993, about 300 industrial prototype circuits have been fabricated, in CMOS, BICMOS, and GaAs technologies, for 60 companies and 10 universities/research laboratories. Moreover 48 small volume productions have been fabricated in 1997 (12% of the fabricated circuits), compared to 39 in 1996 and 24 in 1995.

Prices are negotiated directly by CMP with the manufacturer, depending on each request.

VI-1.4 Consulting

The following consulting tasks have recently been achieved:

<table>
<thead>
<tr>
<th>Company</th>
<th>TIMA member</th>
<th>Duration</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMS (Austria)</td>
<td>K. Torki</td>
<td>8 months</td>
<td>91-93</td>
</tr>
<tr>
<td>IN2P3/LAL (France)</td>
<td>K. Torki</td>
<td>5 days</td>
<td>04/92</td>
</tr>
<tr>
<td>Alcatel/Alsthom (France)</td>
<td>M. Nicolaidis</td>
<td>2 days</td>
<td>07/94</td>
</tr>
<tr>
<td>Mentor Graphics Corp.</td>
<td>M. Nicolaidis</td>
<td>10 days</td>
<td>96-97</td>
</tr>
</tbody>
</table>

VI-2 Educational Tasks

Dealing with problems risen by advanced technologies, and proposing advanced design and test methodologies, TIMA staff members are, as a matter of course, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the Laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into five categories: course organization, seminars, support of or participation in foreign university teaching programs, participation in EU educational and technology transfer programs, and finally direction of Ph.D. students employed by French industrial companies (CIFRE program).

VI-2.1 Courses Organization

The following table lists courses that have been organized by members of the Laboratory, at different institution request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA staff or externally.
<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Organizer</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT</td>
<td>Paris</td>
<td>02/92</td>
<td>2 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>HP</td>
<td>Grenoble</td>
<td>06/92</td>
<td>1 day</td>
<td>M. Marzouki</td>
<td>Board Testing</td>
</tr>
<tr>
<td>MFQ</td>
<td>Paris</td>
<td>12/92</td>
<td>3 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Grenoble</td>
<td>12/92</td>
<td>5 days</td>
<td>A. Guyot</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Grenoble</td>
<td>06/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Tokyo</td>
<td>10/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Singapore</td>
<td>12/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>04/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/Chipshop</td>
<td>Grenoble</td>
<td>04/94</td>
<td>3 days</td>
<td>K. Torki</td>
<td>VLSI Design on PC platforms</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Irvine-CA</td>
<td>11/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>12/94</td>
<td>2 days</td>
<td>M. Lubaszewski</td>
<td>Mixed-Signal Testing</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/94</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>ST Course</td>
<td>Grenoble</td>
<td>04/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Synthesis</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Grenoble</td>
<td>10/96</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
</tr>
<tr>
<td>Internat. Course</td>
<td>Tokyo</td>
<td>12/97</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>HW-SW Codesign</td>
</tr>
</tbody>
</table>

**VI-2.2 Courses and Seminars**

Advanced courses and seminars are a practical way of sensitizing graduate students to state-of-the-art problems and research subjects. The attendance is also often composed by young and senior researchers who want to exchange ideas and views on specific problems of their own field or some related research domains.

In addition to internal seminars, the Laboratory regularly invites people from Grenoble academic and industrial environment to attend the talks given by our visiting researchers. These people have recently had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. A. J. Van de Goor</td>
<td>Delft U. of Technology</td>
<td>07/92</td>
<td>Tests for SRAMs and FIFOs</td>
</tr>
<tr>
<td>Prof. A. J. Van de Goor</td>
<td>Delft U. of Technology</td>
<td>07/92</td>
<td>Tests for neighborhood pattern sensitive faults</td>
</tr>
<tr>
<td>Dr. G. Venkatesh</td>
<td>ASIC Technologies, Bangalore</td>
<td>09/92</td>
<td>HLS of Asynchronous Speed Independent Controllers</td>
</tr>
<tr>
<td>Prof. D. Kinniment</td>
<td>U. Newcastle Upon Tyne</td>
<td>11/92</td>
<td>Correct Interactive Transformational Synthesis of DSP Hardware</td>
</tr>
<tr>
<td>Prof. F. J. Kurdahi</td>
<td>U. California, Irvine</td>
<td>03/93</td>
<td>Architectural Synthesis of DSP Systems</td>
</tr>
<tr>
<td>Prof. M. Soma</td>
<td>U. Washington, Seattle</td>
<td>04/93</td>
<td>Mixed-Signal Testing and DFT</td>
</tr>
<tr>
<td>Prof. A. Ivanov</td>
<td>U. British Columbia, Vancouver</td>
<td>06/93</td>
<td>BIST Compaction Schemes based on Multiple Signature Checking</td>
</tr>
<tr>
<td>Prof. J. A. Abraham</td>
<td>U. Texas, Austin</td>
<td>06/93</td>
<td>Testing of Analog Circuits</td>
</tr>
<tr>
<td>Prof. E. Aas</td>
<td>The Norwegian Inst. of Technology</td>
<td>07/93</td>
<td>Probabilistic Model of Design Quality</td>
</tr>
<tr>
<td>Mr. J. O'Leary</td>
<td>Cornell U., Ithaca, NY</td>
<td>11/93</td>
<td>Retargeting a Hardware Compiler Proof</td>
</tr>
<tr>
<td>Dr. Y. A. Zorian</td>
<td>AT&amp;T Bell Labs, NJ</td>
<td>03/94</td>
<td>Multi-Chip Module Testing</td>
</tr>
</tbody>
</table>

Cont'd
<table>
<thead>
<tr>
<th>Name</th>
<th>Institution</th>
<th>Year</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dr. A. Richardson</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>Defect Oriented Testability Analysis and Analog DFT</td>
</tr>
<tr>
<td>Mr. Th. Olbrich</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>BIST and Diagnostics in Safety Critical Microsystems</td>
</tr>
<tr>
<td>Dr. M. Slamani</td>
<td>Ecole Polytechnique de Montreal, Canada</td>
<td>07/94</td>
<td>BIST, Fault Diagnosis and Testability Analysis in Analog ICs based on Sensitivity Concept</td>
</tr>
<tr>
<td>H. Morel &amp; B. Allard</td>
<td>Centre de Génie Electr., Lyon</td>
<td>10/94</td>
<td>Utilisation des graphes de liens et des réseaux de Péri pour la simulation des systèmes de l'électronique de puissance</td>
</tr>
<tr>
<td>Dr. Rajeev Murgai</td>
<td>FUJITSU Labs of Americ Inc., San José</td>
<td>03/95</td>
<td>Decomposition of Logic Functions for Minimum Transition Activity</td>
</tr>
</tbody>
</table>
| Prof. N. Yevtushenko & Prof. A. Matrosova | Tomsk State Univ., Russia                        | 04/95| - Testing strategies for communicating FSMs  
- Random simulation  
- Design for testability                                      |
| Prof. G. de Micheli    | Stanford Univ.                                   | 05/95| An algebraic approach to system-level modeling and synthesis                                   |
| Prof. G. de Micheli    | Stanford Univ.                                   | 05/95| Optimal synthesis of gated clocks for low power finite state machines                         |
| Prof. V. Uskov         | Moscow State Tech.U.                             | 06/95| Multipurpose CAD System GRAPH-PA                                                                |
| Dr. A. Oraloglu        | San Diego Univ.                                  | 07/95| Microarchitectural synthesis of self-testable ICs                                              |
| Prof. P. Quinton       | IRISA-Rennes                                     | 01/96| Conception de circuits réguliers avec le langage ALPHA                                          |
| Prof. B. Robic         | Jozeff Stefan Institute Ljubljana                | 01/96| Dataflow graphs: partitioning and embedding                                                     |
| Dr. R. Bergamaschi     | IBM T.J. Watson Res. Center, Yorktown Heights    | 03/96| Observable time windows: verifying the results of high-level synthesis                          |
| Dr. R. Kumar           | FZI, Karlsruhe Univ.                             | 04/96| A formal approach to hardware synthesis                                                         |
| Prof. J. Staunstrup    | Techn. Univ., Lyngby                             | 06/96| A formal approach to hardware design                                                           |
| Prof. A. Ivanov        | Vancouver Univ.                                 | 06/96| Space compactors for BIST                                                                      |
| Dr. R. Roy             | NEC, Princeton                                   | 09/96| Low power design: estimation and synthesis Techniques                                            |
| Dr. S. Piestrak        | Wroclaw Univ.                                   | 02/97| Arithmétique des résidus: applications et conception de matériaux                                 |
| Dr. G. Bois            | Politechn. School of Montreal                   | 07/97| H/S co-design of high performance DSP embedded systems based on reconfigurable architectures    |
| Prof. P. Arato         | Techn. Univ., Budapest                          | 07/97| A high level synthesis concept in research and curriculum at TU Budapest                       |
| Dr. P. Wodey           | ISIMA, Clermont-Ferrand                         | 01/98| Méthodologie et outils de codesign à partir de E-LOTOS                                         |
| R. Douence             | IRISA, Rennes                                   | 04/98| Architectures logicielles et wright                                                            |
Picture VI-2.1 1 (c)

Picture VI-2.1 1 (a,b,c) : AMICAL seminars (Tokyo, October 1993 and Singapore, December 1993) and International Course on Hardware-Software codesign (Tokyo, December 1997)
Concerning participation to external seminars, the following table lists the courses and seminars given by members of the Laboratory on their specific research work, following the invitation of various institutions.

<table>
<thead>
<tr>
<th>Institution</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Speaker</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENSL-LIP</td>
<td>Lyon</td>
<td>01/92</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line Operators</td>
</tr>
<tr>
<td>ENST</td>
<td>Paris</td>
<td>06/92</td>
<td>3h</td>
<td>A. Guyot</td>
<td>On-line Operators</td>
</tr>
<tr>
<td>EPFL</td>
<td>Lausanne</td>
<td>12/92</td>
<td>6h</td>
<td>M. Nicolaidis</td>
<td>Regular Structure Test and BIST - On-line Testing</td>
</tr>
<tr>
<td>ENST-ARCS</td>
<td>Paris</td>
<td>05/93</td>
<td>3h</td>
<td>A. Guyot</td>
<td>On-line Arithmetic Operators</td>
</tr>
<tr>
<td>EPFL</td>
<td>Lausanne</td>
<td>09/93</td>
<td>6h</td>
<td>M. Nicolaidis</td>
<td>Regular Structure Test and BIST - On-line Testing</td>
</tr>
<tr>
<td>CERN</td>
<td>Geneva</td>
<td>01/94</td>
<td>1h</td>
<td>M. Lubaszewski</td>
<td>On-line test extension to IEEE 1149.1</td>
</tr>
<tr>
<td>AFCET</td>
<td>Paris</td>
<td>02/94</td>
<td>1h</td>
<td>M. Marzouki</td>
<td>Boundary Scan Board and MCMs Test</td>
</tr>
<tr>
<td>UF RJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>IC Test - Main Methods</td>
</tr>
<tr>
<td>UFMG</td>
<td>Belo Hor.</td>
<td>09/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>BS Test</td>
</tr>
<tr>
<td>Telebras/CPqD</td>
<td>Campinas</td>
<td>12/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>BS Test</td>
</tr>
<tr>
<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>A. Jerriya</td>
<td>Codesign</td>
</tr>
<tr>
<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>A. Jerriya</td>
<td>Behavioral synthesis</td>
</tr>
<tr>
<td>UFRGS</td>
<td>P. Alegre</td>
<td>11/94</td>
<td>2h</td>
<td>A. Jerriya</td>
<td>Behavioral synthesis</td>
</tr>
<tr>
<td>ENST</td>
<td>Paris</td>
<td>03/95</td>
<td>1h</td>
<td>A. Jerriya</td>
<td>Codesign</td>
</tr>
<tr>
<td>CL Inc</td>
<td>Austin</td>
<td>04/96</td>
<td>1h</td>
<td>D. Borrione</td>
<td>Formal validation of VHDL packages</td>
</tr>
<tr>
<td>Fujitsu Lab.</td>
<td>Sta Clara</td>
<td>04/96</td>
<td>3h</td>
<td>D. Borrione</td>
<td>Formal verification in the PREVAIL system</td>
</tr>
<tr>
<td>SRI</td>
<td>Stanford</td>
<td>07/96</td>
<td>1h</td>
<td>D. Borrione</td>
<td>Integrating formal methods and CAD</td>
</tr>
<tr>
<td>UC Berkeley</td>
<td>Berkeley</td>
<td>08/96</td>
<td>1h</td>
<td>D. Borrione</td>
<td>Automatic diagnosis of simple design errors</td>
</tr>
</tbody>
</table>

VI-2.3 Support of Universities Teaching Programs

The Laboratory has established for many years solid contacts with other research institutions and universities throughout the world. Exchange of students and post-doctoral fellows are very common, and TIMA members are often invited to participate in foreign university teaching programs. The following table lists this kind of activities during the recent academic years.

<table>
<thead>
<tr>
<th>University</th>
<th>Country</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tallinn Technical Univ.</td>
<td>Estonia</td>
<td>05/93</td>
<td>9h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>12/93</td>
<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Inst. for Microel. Stutt</td>
<td>Germany</td>
<td>02/94</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line arithmetic operators</td>
</tr>
<tr>
<td>Politechnica Bucharest</td>
<td>Romania</td>
<td>05/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>CMOS VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>06/94</td>
<td>3h</td>
<td>M. Marzouki</td>
<td>Partial Boundary Scan Test</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>12/94</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>02/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Architecture and arithmetics</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>11/95</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>01/95</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Arithmetics</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>02/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>CMOS circuitry</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>03/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>Operators</td>
</tr>
<tr>
<td>Univ. de Las Palmas</td>
<td>Canarias</td>
<td>05/95</td>
<td>4h</td>
<td>A. Guyot</td>
<td>Garden Ws.: Operators in GaAs</td>
</tr>
</tbody>
</table>
VI-2.4 Participation in EU Educational Programs

TIMA Laboratory activities have a strong European profile. In addition to numerous research projects listed in other sections of this report, the following table indicates the involvement of TIMA staff members in educational programs launched by the European Union. This involvement take the form of organizing and/or teaching courses.

<table>
<thead>
<tr>
<th>Framework</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTTT Comett II</td>
<td>Greece</td>
<td>02/92</td>
<td>15h.</td>
<td>A. Guyot</td>
<td>VLSI Design Course teaching</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>France</td>
<td>12/92</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Germany</td>
<td>02/94</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>JTTT Comett II</td>
<td>Italy</td>
<td>02/94</td>
<td>1h</td>
<td>M. Nicolaidis</td>
<td>European School on High Reliability Integrated Systems</td>
</tr>
<tr>
<td>JTTT Comett II</td>
<td>Greece</td>
<td>12/94</td>
<td>15h.</td>
<td>M. Nicolaidis</td>
<td>Advanced Course on VLSI Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>08/94</td>
<td>6h</td>
<td>A. Jerraya</td>
<td>System Design</td>
</tr>
<tr>
<td>Comett</td>
<td>Austria</td>
<td>04/95</td>
<td>3days</td>
<td>C. Liem</td>
<td>Reconfigurable architecture</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>09/95</td>
<td>5days</td>
<td>Jerraya/Kission</td>
<td>System design</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Denmark</td>
<td>08/95</td>
<td>5days</td>
<td>A. Jerraya</td>
<td>Co-design</td>
</tr>
<tr>
<td>Comett</td>
<td>Netherlands</td>
<td>09/95</td>
<td>3days</td>
<td>Kission/Rahm</td>
<td>AMICAL</td>
</tr>
<tr>
<td>EUROPRACTICE COURSE</td>
<td>Germany</td>
<td>09/97</td>
<td>3h</td>
<td>R. Velazco</td>
<td>On-Line Testing for VLSI</td>
</tr>
<tr>
<td>EUROPRACTICE COURSE</td>
<td>Germany</td>
<td>09/97</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>Test Technology for Digital and Mixed-Signal ASICs and MCMs</td>
</tr>
</tbody>
</table>

VI-2.5 University/Industry Joint Research Programs

A French national program, called CIFRE, allows French companies to receive French Ph.D. students. The thesis director must belong to a French University or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company.

TIMA staff members have been asked by companies to direct several Ph.D. theses in the CIFRE framework. The most recent ones are listed in the table below.
<table>
<thead>
<tr>
<th>Company</th>
<th>Student</th>
<th>Director</th>
<th>Dur.</th>
<th>Research Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMD</td>
<td>Ch. Vaucher</td>
<td>L. Bahme</td>
<td>90-93</td>
<td>PCB Testing</td>
</tr>
<tr>
<td>Hewlett Packard</td>
<td>P. Dulieux-Verguin</td>
<td>B. Courtois</td>
<td>91-94</td>
<td>Failure Analysis of ICs by Liquid Crystals</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>M. Kodnja</td>
<td>A. Guyot</td>
<td>92-95</td>
<td>Analog Voltage Controlled Oscillators and Phase-Locked Loops</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>F. Lemery</td>
<td>M. Marzouki</td>
<td>92-95</td>
<td>Analog and Mixed Macromodeling</td>
</tr>
<tr>
<td>IMD</td>
<td>A. Benali</td>
<td>L. Bahme</td>
<td>92-95</td>
<td>Electro-optic ATE</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>E. Berrebi</td>
<td>A. Jerraya</td>
<td>93-96</td>
<td>Heterogeneous System Design</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>F. Naçabal</td>
<td>A. Jerraya</td>
<td>95-96</td>
<td>Heterogeneous System Design</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>Ph. Guillaume</td>
<td>A. Jerraya</td>
<td>96-98</td>
<td>Low-power</td>
</tr>
</tbody>
</table>
VII - PUBLICATIONS 1996-1997

VII-1 Books and magazines

1996

BACIVAROV I.*, BALME L.
Quality effort in Europe
Special issue of the Journal of Quality Engineering, Vol. 8, no.4, 1996
Publication by Marcel DEKKER Inc., New York, USA
Guest Editors
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* POLITECNICA Univ., Bucharest, Romania

BACIVAROV I.*, BALME L.
European programme in quality of complex integrated systems
Special issue of the Journal of Quality Engineering on the Quality Effort in Europe,
Vol. 8, no.4, Publication by Marcel DEKKER Inc., New York, USA, 1996
---------
* POLITECNICA Univ., Bucharest, Romania

BALME L., JENNI J.F.*
Management et certification de la qualité
WEKA Editions, Zürich, Switzerland, 1996
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* Société Générale de Surveillance, Geneva, Switzerland

BEN ISMAIL T., DAVEAU J.M., O'BRIEN K.*, JERRAYA A.
A system-level communication synthesis approach for hardware/software systems
Int'l Journal Microprocessors and Microsystems, Special Issue on Hardware/Software Codesign,
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* LEDA S.A., Meylan, France

BEN ISMAIL T., MARCHIORO G., JERRAYA A.
Découpage de systèmes VLSI à partir d'une spécification de haut niveau
TSI (Techniques et Sciences de l' Informatiques), Hermes, 1996

BEN ISMAIL T., O'BRIEN K.*, JERRAYA A.
PARTIF: an interactive system level partitionning
---------
* LEDA S.A., Meylan, France

CALIN T., NICOLAIDIS M. VE LAZ CO* R.
Upset hardened memory design for submicron CMOS technology
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* LSR Laboratory, Grenoble, France
DAVEAU J.M., MARCHIORO G.F., BEN ISMAIL T., JERRAYA A.
COSMOS: an SDL based hardware/software codesign environment
Current Issue in Electronic Modelling, Vol. 8, Co-design and co-verification,
December 1996

JERRAYA A., DING H., KISSION P., RAHMOUNI M.
Behavioral synthesis and component re-use with VHDL
Kluwer Publishers, 1996

KAMARTNOS G.*, GUILLAUMOT N.**, COURTOIS B., Editors
Proceedings of the 1st European Workshop on Microelectronics Education, Grenoble,
France, 5-6 February 1996

* LPCS-ENSSERG, Grenoble, France
** CIME, Grenoble, France

KAMINSKA B.*, COURTOIS B.
IEEE Design & Test of Computers
Special Issue on Design and Test of Analog and Mixed-Signal Circuits
Guest Editors, Summer 1996

* Ecole Polytechnique de Montréal, Canada

KAMINSKA B.*, COURTOIS B.
JETTA - Journal of Electronic Testing, Theory and Applications
Special Issue on Analog and Mixed-Signal Testing
Guest Editors, Volume 9, August/October 1996

* Ecole Polytechnique de Montréal, Canada

KISSION P., JERRAYA A.
Behavioral design allowing modularity and component reuse
Journal of Microelectronic System Integration, Vol. 4, No 4, 1996

KRIM N., RIESCO T.*, LISTER P.**, HESS K.***, PYPE P.****, GORE T.*****,
PÉREZ J.******
EUROMIC: European OMI Centres
In Embedded Microprocessor Systems, Edited by C. Müller-Schloer, F. Geerinckx,

* UPM, Madrid, Spain
** Univ. of Sussex, Brighton, UK
*** PhG, Munich, Germany
**** IMEC, Leuven, Belgium
***** OMMO, Brussels, Belgium
****** UNED, Madrid, Spain

* Engineering School of Geneva, Switzerland


* University of Nantes, France


* Technical Univ. of Brno, Czech Republic


NICOLAIDIS M. Theory of transparent BIST for RAMs. IEEE Transactions on Computers, October 1996
PAULIN P.*, CORNERO M.*, LIEM C., NACABAL F., DONAWA C.**, SUTARWALA S***, MAY T.***, VALDERRAMA C.
Trends in embedded systems technology: an industrial perspective
In Hardware/Software Co-Design, Edited by M.G. Sami, G. De Micheli, Kluwer
Academic Publishers, 1996

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* SGS-Thomson Microelectronics, Crolles, France
** IBM Toronto Labs, Compiler Development, North York, Ontario, Canada
*** BNR, Ottawa, Ontario, Canada

Méthodes et langages pour la spécification des systèmes complexes: définir les systèmes électroniques, de la conception à la maintenance
In "Revue d'Electricité et de l'Electronique" (REE), N°3, March 1996

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* Dassault Aviation, France
** IRESTE, France
*** ENST, France
**** Aérospatiale, France
***** ASTER Ingénierie

RENAUDIN M.*, EL HASSAN B.*, GUYOT A.
A new asynchronous pipelined scheme: application of the design of a self-timed ring divider

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* CNET-CNS, Meylan, France

ROMDHANI M., de CHAZELLES* P., JEFFROY* A., SAHRAOUI A.E.K.**, JERRAYA A.
Co-specification for co-design in the development of avionics systems
In IFAC Journal of Control Engineering Practice, Elsevier Publishers, Vol. 4, n° 6, 1996

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* Aérospatiale, Toulouse, France
** LAAS/CNRS, Toulouse, France

SIMEU E., GEORGES D. *
Modeling and control of an eddy current brake
Elsevier Science Ltd Publishers

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* LAG/ENSIEG, Grenoble, France

SZEKELY V.*, MARTA Cs*, RENCZ M.*, BENEDEK Zs.*, COURTOIS B.
Design for thermal testability (DFTT) and a CMOS realization

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* Technical University of Budapest, Hungary
SZEKELY V.*, RENCZ M.*, COURTOIS B.
Sensors and Actuators - A-Physical
Special Issue on Thermal Investigations of ICs and Microstructures
(THERMINIC Workshop 95), Vol. A55 No1, July 1996
Guest Editors

*Technical University of Budapest, Hungary

VAUCHER C.*, BALME L., BENALI A.
The PPM myth in board assembly
Quality Effort in Europe, Special issue of the Journal of Quality Engineering
Vol. 8, №4, Publication by Marcel DEKKER Inc., New York, USA, 1996

* IMD, Bandol, France

WAHBA A., BORRIONE D.
A method for automatic design error location and correction in combinational logic circuits

SEU-hardened storage cell validation using a pulsed laser

* LSR Laboratory, Grenoble, France
** The Aerospace Corporation, Los Angeles, USA

WOLFGANG E.*, COURTOIS B., BALK L.J.*, Editors
Proceedings of the 5th European Conference on Electron and Optical Beam Testing of
Electronic Devices, August 27-30, 1995, Wuppertal, Germany
Special Issue of Microelectronic Engineering Journal, Vol. 31, Numbers 1-4 Special
Issues, Elsevier, February 1996

* SIEMENS AG, Munich, Germany
** Wuppertal University, Germany

1997

ABID M.*, JERRAYA A.
Towards hardware-software co-design: a case study of robot arm controller
Journal of Microelectronic Systems Integration
Vol. 5, №3, September 1997

* ENIM, Monastir, Tunisia

BALME L., LEUNI J.F.*
Quality function deployment
Editions WEKA, Zürich, February 1997

* Société Générale de Surveillance, Geneva, Switzerland
BALME L., JENNI J.F.*
Management de configuration
Editions WEKA, Zürich, June 1997

* Société Générale de Surveillance, Geneva, Switzerland

BALME L., JENNI J.F.*
Les plans d’expériences
Editions WEKA, Zürich, October 1997

* Société Générale de Surveillance, Geneva, Switzerland

BALME L., JENNI J.F.*
Analyse des modes de défaillance et de leur criticité
Editions WEKA, Zürich, December 1997

* Société Générale de Surveillance, Geneva, Switzerland

DAVEAU J.M., MARCHIORO G.F., BEN ISMAIL T., JERRAYA A.
Large protocol selection and interface generation for HW-SW codesign
In IEEE Transactions on VLSI system, Special Issue on design automation of complex
integrated systems, Vol. 5, N° 1, March 1997

GOOSSENS G.*, VAN PRAET J.*, LANNEER D.*, GEURTS W.*, KIFI A**, LIEM C.,
PAULIN P.***
Embedded software in real-time signal processing systems: design technologies
In Proceedings of the IEEE Special Issue on Hardware/Software Co-Design,
Vol. 85, N° 3, March 1997

* Target Compiler Technologies, Leuven, Belgium
** IMEC, Leuven, Belgium
*** SGS-Thomson Microelectronics, Crolles, France

GUYOT A., ABOU-SAMRA
Modeling power consumption in arithmetic operators
Microelectronic Engineering, N°39, 1997

JEMAI A.*, KISSION P., JERRAYA A.A.
Combining architectural simulation and behavioral synthesis

*ENSI-INSAT, Tunis, Tunisia

JERRAYA A., GOOSSENS G.*
IEEE Transactions on VLSI Systems
Special Issue on Design Automation of Complex Integrated Systems
Vol.5, N°1, March 1997
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**TRS31, Auteville, France

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**U.S. Air Force SMC/AXE, El Segundo, CA 90245-4683

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*LEIBNIZ, IMAG, Grenoble, France
**CEA, Grenoble, France
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*****Polytechnic University of Catalunya, Spain

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* Technical University of Budapest, Hungary
** Darmstadt University of Technology, Germany

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** Technical University of Lodz, Poland
*** State Polytechnic of Lviv, Ukraine
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* LIP6, Université Pierre & Marie Curie, Paris

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*** University of Barcelona, Spain

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*Center of Satellite Engineering Research, Univ. of Surrey, UK.
**CNES, Toulouse, France

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13-14 mai 1998, Toulouse, France

*CEA, Bruyères-le-Châtel, France
**CNES, Toulouse, France
***NKL, Washington, USA

COURTOIS B.
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* NIST, Gaithersburg, USA

DAVEAU J.M., MARCHIORO G., JERRAYA A.
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DUARTE R.O., NICOLAI DIS M.
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Paris, France, 23-26 February 1998

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Paris, France, 23-26 February 1998
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* ENSI-INSAT, Tunis, Tunisia

KARAM J.M.
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The International Conference on Advanced Microsystems for Automotive
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Berlin, Germany, 26-27 March 1998

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MME'98, Ulvik in Hardanger, Norway, June 3-5 1998

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Electro mechanical systems development
The First International Conference on Modeling and Simulation of Microsystems,
Semiconductors, Sensors and Actuators, MSM'98
Santa Clara Marriott, California, USA, April 5-8, 1998
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*Mentor Graphics Corporation, Oregon, USA
**Technical University of Budapest, Budapest, Hungary
***Darmstadt University of Technology, Darmstadt, Germany
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Microsystems testing : an approach and open problems
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* DELET/UFRGS, Brazil

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United Kingdom, 1998

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Conference on Intellectual Property in Electronics (IP’97)
Santa Clara, CA, USA, 17-18 March 1998

* OMIMO, Brussels, Belgium

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*Technical University of Budapest

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*Technical University of Budapest

TORKI K.
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*German National Research Center for Informatic Technology (GNRCIT),
St. Augustin, Germany
**CNES, Toulouse, France
***University Politecnico of Catalufía, Spain

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**CNES, Toulouse, France

VELAZCO R., CHEYNET Ph., BOFILL A., ECOFFET R.**
THESIC: A testbed suitable for the qualification of integrated circuits devoted to operate in harsh environment
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*CNES, Toulouse, France

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COURTOIS B.
TBA
Invited paper at the IEEE 22nd International Conference on Microelectronics (MIEL’99),
Nis, Yugoslavia, 19-22 September 1999

National Workshops

1996

KARAM J.M.
Fabrication collective de microsystèmes - Accès en technologie et outils de simulation
FORUM ISHM 96
Paris, France, 2-3 April 1996

KARAM J.M.
Services MCM du CMP
NETPACK Meeting, FORUM ISHM 96
Paris, France, 2-3 April 1996

MOHAMED F., MARZOUKI M.
La logique floue pour le test et le diagnostic des circuits
Rencontres Francophones sur la Logique Floue et ses Applications
Nancy, France, 4-5 December 1996
1998

KARAM J.M.
Microsystèmes
7e Congrès International Electronique Automobile
Toulouse, France, 10-11 March 1998

VII – 3 Theses

1996

BEN ISMAIL Tarık
Synthèse au niveau système et conception de systèmes mixtes logiciels/matériels
Thèse de Doctorat INPG - 9 January 1996

STEFANI Robert
Application de la Norme ISO 9000 aux entreprises de service fortement dépendantes de leur système d'information
Thèse Professionnelle INPG, Mastère spécialisé Qualité des Systèmes Intégrés Complexes,
Option Systèmes Informatiques - 10 January 1996

TOUATI Mohamed Hédi
Test et diagnostic de cartes et de MCMs partiellement boundary scan
Thèse de Doctorat INPG - 24 January 1996

KISSION Polen
Exploitation de la hiérarchie et de la réutilisation de blocs existants par la synthèse de haut niveau
Thèse de Doctorat INPG - 25 January 1996

DING Hong
Synthèse architecturale interactive et flexible
Thèse de Doctorat INPG - 2 April 1996

KARAM Jean-Michel
Méthodes et outils pour la conception et la fabrication de microsystèmes
Thèse de Doctorat INPG - 20 May 1996

MOUSSA Imed
Application des circuits numériques en arséniure de gallium dans les systèmes à haut débit de communication et dans les calculateurs performants
Thèse de Doctorat INPG - 10 June 1996

CHANGUEIL Adel
Prototypage rapide d'architectures mixtes logiciel/matériel à partir de modèles mixtes C-VHDL
Thèse de Doctorat INPG - 22 October 1996
DEHARBE David
Vérification formelle de propriétés temporelles : étude et application au langage VHDL
Thèse de Doctorat UJF - 15 November 1996

VIJAYARAGHAVAN Vijay
Exploration des liens entre la synthèse de haut niveau (HLS) et la synthèse au niveau transferts de registres (RTL)
Thèse de Doctorat INPG, 29 November 1996

BENALI Aadil
Contribution à l’amélioration de la qualité du test de circuits imprimés nus : exploitation des informations CAO, par des techniques de traitement d’images, en vue de la génération des données du test électrique
Thèse de Doctorat INPG - 3 December 1996

ROMDHANI Mohamed
Ingénierie des systèmes complexes avec la méthode de conception concurrente co-design matériel/logiciel. Application aux calculeurs embarqués
Thèse de Doctorat INPG - 9 December 1996

1997

VACHER André
Calcul câblé d’une transformée de Fourier à très grand nombre d’échantillons, éventuellement multi-dimensionnelle
Thèse de Doctorat INPG - 8 January 1997

PARET Jean-Marc
Étude et mise au point de la méthodologie de conception et de fabrication collective de microsystèmes sur silicium
Thèse de Doctorat INPG - 13 January 1997

RAHMOUNI Maher
Ordonnancement et optimisations pour la synthèse de haut niveau des circuits de contrôle
Thèse de Doctorat INPG - 21 February 1997

WAHBA Ayman
Diagnostic des erreurs de conception dans les circuits digitaux : le cas des erreurs simples
Thèse de Doctorat UJF - 7 May 1997

DE OLIVEIRA DUARTE Ricardo
Techniques de conception et outils de CAO pour la génération des parties opératives auto-contrôlables
Thèse de Doctorat INPG - 30 June 1997
MOHAMED Firas
Approche à base de logique floue pour le test et le diagnostic des circuits analogiques
Thèse de Doctorat INPG - 3 July 1997

LIEM Clifford
Compilateurs multicibles et outils pour les processeurs embarqués dans le cadre d'applications industrielles
Thèse de Doctorat INPG - 18 July 1997

Elisabeth BERREBI
Méthodologie pour l'application industrielle de la synthèse comportementale
Thèse de Doctorat INPG - 11 December 1997

Marc KODRNJA
Etude de VCO pour les circuits à fréquence intermédiaire, analyse et simulation du bruit de phase
Thèse de Doctorat INPG - 12 December 1997

Jean-Marc DAVEAU
Spécifications systèmes et synthèses de la communication pour le co-design logiciel/matériel
Thèse de Doctorat INPG - 19 December 1997

1998

François NAÇABAL
Outils pour l'exploration d'architectures programmables embarquées dans le cadre d'applications industrielles
Thèse de Doctorat INPG - 28 February 1998

VII – 4 Patents

1996

KARAM I.M., MOORE D.*, DANIEL J.*
CMOS compatible inertial sensor
UK Patent 1255003, October 1996

* Cambridge University
VIII - MISCELLANEOUS

VIII.1 What did they do after graduating from the Laboratory (1984-1997)?

Below is the list of researchers which graduated from TIMA Laboratory, from 1984.

The first affiliation corresponds to their affiliation right after the thesis. Eventually, successive affiliations are provided.

From 1984 to 1997, 90 theses have been defended.

It might be noticed that (apart from foreign students who returned in their country) several members of the group have been or are working abroad.

**DERANTONIAN Henri**
- Génération automatique de parties contrôles de microprocesseurs sous forme de PLA spécialisés.
- **BULL - Grenoble**

**NICOLAIDIS Michael**
- Conception de circuits intégrés ou testables pour des hypothèses de pannes analytiques.
- **CNRS - TIMA Laboratory - Grenoble**

**LAURENT Jacques**
- Projet ACIME : Analyse des Circuits Intégrés par Microscopie Electronique.
- **CNRS - TIMA Laboratory - Grenoble**
- Next: **CNRS - IMAG - Grenoble**

**HMIMID Mohamed**
- Assemblage et génération automatique des dispositifs périphériques de PLA complexes.
- **SIEMENS - Munich - Germany**

**SAHBATOU Mohamed Djameleddine**
- Une méthode de conception de microprocesseurs CMOS : application au 8048 (INTEL)

**CHUQUILLANQUI Samuel**
- Une nouvelle approche pour l'optimisation topologique et l'automatisation du dessin des masques de PLA complexes.
- **BULL Systèmes - Les Clayes Sous Bois**
- Next : **THOMSON THOM'6 - Paris**
- Next : **GEC ALSTHOM - Paris la Défense**
- Next : **GEC ALSTHOM Transport - Saint-Ouen**
BOURCIER Emile  
Conception et réalisation du simulateur de langage de description de circuits intégrés IRENÉ C.  
SGS THOMSON - Grenoble

JANSCH Ingrid  
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Porto Alegre University - Brazil

BERGHER Laurent  
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Next : Thomson TCEC - Grenoble

IANESELLI Jean-Christophe  
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MERLIN GERIN - Meylan

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Mécanismes prédictifs d’évaluation des caractéristiques géométriques des circuits VLSI.  

SCHOELLKOPF Jean-Pierre  
SILICIEL : Contributions à l'architecture des circuits intégrés et à la compilation du silicium.  
BULL Systèmes - Les Clayes Sous Bois  
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BERTRAND François  
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MARTINEZ François  
CIRENE : Compilateur du langage IRENÉ  

GUIGUET Isabelle  
Liaison d'un microscope électronique à balayage aux outils CAO de description des circuits intégrés.  
APSIS - Meylan

PEREZ SEGOVIA Thomas  
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MARINE Souheil
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BASCHIERA Daniel
Modélisation de pannes et méthodes de test de circuits intégrés CMOS
TRT - Paris
Next : NORSKDATA - Norway
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ALIOUAT Mahklouf
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Next: University of Geneva, Switzerland

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DANG Weidong
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VARINOT Patrice
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Next : MATRA - Paris

HOCHET Bertrand
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EPFL - Lausanne - Switzerland
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ROUGEAUX François-René
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Next : IBM - Montpellier

SOULAI Mohamed
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CAISSO Jean-Paul
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Mc GILL University - Montreal - Canada
Next : MATRA-MHS – Nantes
Next : SGS-Thomson – Roussé – France

BEKKARA Noureddine
Optimisation et compromis surface-vitesse dans le compilateur de silicium SYCO
SGS THOMSON - Grenoble

DUPRAT Jean
LAIOS : un réseau multiprocesseur orienté intelligence artificielle
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MHAYA Noureddine
Compilateur de parties contrôle de microprocesseurs
IFATEC - Versailles
Next: IFATEC - Montigny-Le-Bretonneux

FERNANDES Antonio Otavio
Test des PLAs optimisés topologiquement
University of Belo Horizonte - Brazil

ZYSMAN Eytan
Conception de parties contrôles de circuits VLSI - Application au coprocesseur arithmétique
FELIN
EPFL - Lausanne - Switzerland

BERGER-SABBATEL Gilles
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CNRS - TIMA Laboratory - Grenoble
Next : LGI Laboratory - Grenoble

MICOLLET Dominique
Etude de la contrôleabilité de circuits intégrés par faisceaux d’électrons
University of Dijon
MOISAN Frédéric
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Direction des Constructions et des Armes Navales (DCAN) - Brest

HORNIE Armand
Contribution à la définition et à la mise en œuvre de NAUTILE
Thèse de Doctorat INPG - Juin 1989
APSYS - Meylan
Next : BULL - Echirolles

DARLAE François
Contribution au test des circuits intégrés CMOS : étude du test des pannes stuck-on et stuck-open
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EPFL - Lausanne - Switzerland
Next : Ecole Polytechnique de Montréal - Canada
Next : SGS Thomson - Grenoble
Died in plane crash in July 1996

NORAZ Serge
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MERLIN GERIN - Meylan

BONDUCNO Philippe
Contribution à NAUTILE : un environnement pour la compilation de silicium
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IBM - Corbeil

JERRAYA Ahmed Amine
Participation à la compilation de silicium et au compilateur SYCO
Thèse d'Etat - 19 décembre 1989
CNRS - TIMA Laboratory - Grenoble

TORKI Kholdoun
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CMP - Grenoble

PIRSO Alain
Conception et simulation d'architectures parallèles et distribuées pour le traitement d'images
Thèse de Doctorat INPG - 4 mai 1990
CENG Division LETI - Grenoble
Next : SGS-Thomson/TCEC - Meylan - France
Next : SYNOPSIS - Mountain View - California - USA

SAVART Denis
Analyse de défaillance de circuits intégrés VLSI par testeur à faisceau d'électrons
Thèse de Doctorat INPG - 27 juin 1990
IMAGERIE INFORMATIQUE - Grenoble
BALME Louis  
Habilitation à diriger des recherches. 21 mai 1990  
On secondment to SGS, Geneva, from 1.1.1991  
Next: TIMA Laboratory

CHAUMONTET Gilles  
Etude de faisabilité d'un micro-controleur de très haute sécurité  
Thèse de Doctorat INPG - 26 octobre 1990  
Centre de Compétence en Conception de Circuits Intégrés (C4I), Archamps

MARZOUKI Meryem  
Approches à base de connaissances pour le test de circuits VLSI : application à la validation de prototypes dans le cas d'un test sans contact  
Thèse de Doctorat INPG - 6 février 1991  
CNRS - TIMA Laboratory – Grenoble  
Next: LIP6 Laboratory – Paris

CONARD Didier  
Traitement d'images en analyse de défaillances de circuits intégrés par faisceau d'électrons  
Thèse de Doctorat INPG - 11 février 1991  
INFSI Society (ARM Group) – Paris, France  
Next: OCE Graphics – Créteil – France

COURT Thierry  
Conception d'une famille de coprocesseurs parallèles intégrés pour le traitement d'images  
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I2S - Bordeaux

COLLETTE Thierry  
Architecture et validation comportementale en VHDL d'un calculateur parallèle dédié à la vision  
Thèse de Doctorat INPG - 14 septembre 1992  
CEA/LETI/DEIN - Gif sur Yvette

CASTRO ALVES Vladimir  
Modélisation de pannes et algorithmes de test pour mémoires RAMs multi-port  
Thèse de Doctorat INPG - 10 décembre 1992  
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble  
Next: Lecturer at Aveiro University - Portugal  
Next: Professor at UFRJ - Rio de Janeiro - Brazil

JEMAI Abderrazak  
Etude d'un processeur RISC pour un système symbolique parallèle  
Thèse de Doctorat INPG - 22 juin 1992  
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble  
Next : ENSI – Tunis – Tunisia

PARK Inhag  
AMICAL : un assistant pour la synthèse et l'exploitation architecturale des circuits de commande  
Thèse de Doctorat INPG - 3 juillet 1992  
DAS/ETRI - Daejon, Research Laboratory in Korea
BOURAoui Rachid
Calcul sur les grands nombres et VLSI : application au PGCD, au PGCD étendu et à la distance euclidienne
Thèse de Doctorat INPG - 15 janvier 1993
Bell Northern Research (BNR) – Ottawa - Canada
Next: Plaintree Systems Inc. – Stittsville – Ontario - Canada

O'Brien Kevin
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LED A S.A. – Meylan - France

KUSUMAPUTRI-HORNIK Yustina
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BEN OTHMAN Mohamed Tahar
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Thèse de Doctorat INPG - 8 septembre 1993
Dean of the Faculty of Science & Engineering, Univ. of Science & Technology - Sana’a - Yemen Republic

VAUCHER Christophe
Le test haute résolution de circuits imprimés nus
Thèse de Doctorat INPG - 25 novembre 1993
IMD, Grenoble, and TIMA Laboratory
Next: IMD Bandol, France
Next: Consultant Engineer, True Test Techniques & Training (T4) – Bandol, France

HAMDI Belgacem
Outils CAO pour la génération automatique de parties opératives auto-contrôlables
Thèse de Doctorat INPG - 18 Avril 1994

AICHOUCHI Mohamed
Étude des liens entre la synthèse architecturale et la synthèse au niveau transfert de registres
Thèse de Doctorat INPG - 20 juin 1994
Post-doctoral position at École Polytechnique de Montréal - Canada
CADABRA – Ottawa - Canada
Newbridge Networks Corporation – Kanata – Ottawa - Canada

LUBASZEWSKI Marcelo
Le test unifié de cartes appliqué à la conception de systèmes fiables
Thèse de Doctorat INPG - 20 juin 1994
Professor at the UFRGS - Porto Alegre University - Brazil

KEBICHI Omar
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Thèse de Doctorat INPG - 15 juillet 1994
Engineer/researcher at TIMA Laboratory - Grenoble
Next: Mentor Graphics – Portland - USA
KOLARIK Vladimir
Techniques avancées de test de circuits analogiques et mixtes analogiques-numériques
Thèse de Doctorat INPG - 31 octobre 1994
University of Brno - Czech Republic

BEDERR Hakim
Contribution à la conception en vue du test d'opérateurs à structure itérative
Thèse de Doctorat INPG - 23 novembre 1994
Post-Doctoral position at AT&T Bell Laboratories – Princeton - USA
Next: Texas Instruments - Villeneuve Loubet - France

VERGUIN Pascale
Industrialisation d'une méthode de localisation de défauts sur circuits intégrés par cristaux liquides
Thèse de Doctorat INPG - 20 décembre 1994
Primary school teacher

MONTALVO Luis
Systèmes de numération pour la conception de diviseurs rapides
Thèse de Doctorat INPG, 13 mars 1995
University of Minnesota – Minneapolis – USA
Next : Post-doctoral position at CNET – Meylan - France

VARGAS Fabian Luis.
Amélioration de la sûreté de fonctionnement des systèmes spatiaux basée sur le contrôle de courant
Thèse de Doctorat INPG, 5 mai 1995
Associated Researcher at U.F.R.G.S. - Porto Alegre University - Brazil
Next: Prof. at Pontificia Universidade Catolica do Rio Grande do Sul - Porto Alegre - Brazil

BOUDJIT Mokhtar
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SKAF Ali
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Thèse de Doctorat INPG, 11 septembre 1995
Lecturer at Aveiro University, Portugal
Next : HIIAST Institute - Damascus University - Syria

LEMERY François
Modélisation comportementale des circuits analogiques et mixtes
Thèse de Doctorat INPG, 20 décembre 1995
SGS-Thomson Crolles - Central R&D - France

BEN ISMAIL Tarek
Synthèse au niveau système et conception de systèmes mixtes logiciels/matériels
Thèse de Doctorat INPG, 9 janvier 1996
Hewlett Packard - Bristol, UK
STEFANI Robert
Application de la Norme ISO 9000 aux entreprises de service fortement dépendantes de leur système d'information
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AFAQ Auditor, Bagneux (Paris), France

TOUATI Mohamed Hédi
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Thèse de Doctorat INPG - 24 janvier 1996
Northern Telecom – Ottawa – Canada

KISSION Poleu
Exploitation de la hiérarchie et de la réutilisation de blocs existants par la synthèse de haut niveau
Thèse de Doctorat INPG - 25 janvier 1996
Researcher at TIMA Laboratory - Grenoble
Next: ANACAD – Meylan – France

DING Hong
Synthèse architecturale interactive et flexible
Thèse de Doctorat INPG - 2 avril 1996
Post-Doctoral position at "Ecole Polytechnique de Montréal" - Canada
Next: Nortel Semiconductors – Ottawa – Canada

KARAM Jean-Michel
Méthodes et outils pour la conception et la fabrication des microsystèmes
Thèse de Doctorat INPG - 20 mai 1996
Researcher at TIMA Laboratory - Grenoble

MOUSSA Imed
Applications des circuits numériques en arsénure de gallium dans les systèmes à haut débit de communication et dans les calculateurs performants
Thèse de Doctorat INPG - 10 juin 1996
Engineer at TIMA Laboratory - Grenoble

CHANGUEUL Adel
Prototypage rapide d'architectures mixtes logiciels/matériels à partir de modèles mixtes C-VHDL
Thèse de Doctorat INPG - 22 octobre 1996
Associate Professor at ENIM – Monastir - Tunisia

BENALI Aaïl
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IMD Marcoussis - France

DEHARBE David
Vérification formelle de propriétés temporelles : étude et application au langage VHDL
Thèse de Doctorat UJJF - 15 novembre 1996
Carnegie Mellon University – Pittsburgh – USA
VIJAYARAGHAVAN Vijay
Exploration des liens entre la synthèse de haut niveau (HLS) et la synthèse au niveau transferts de registres (RTL)
Thèse de Doctorat INPG - 29 novembre 1996
SYNOPSYS – Mountain View – USA

ROMDHANI Mohamed
Ingénierie des systèmes complexes avec la méthode de conception concurrente co-design matériel/logiciel, application aux calculateurs embarqués
Thèse de Doctorat INPG - 9 décembre 1996
Contracted Researcher at TIMA
Next: Associate Professor at INSAT – Tunis - Tunisia

VACHER André
Calcul câblé d'une transformée de Fourier à très grand nombre d'échantillons, éventuellement multidimensionnelle
Thèse de Doctorat INPG - 8 janvier 1997
Teacher at Lycée de Meylan - France

PARET Jean-Marc
Étude et mise au point de la méthodologie de conception et de fabrication collective de microsystèmes sur silicium
Thèse de Doctorat INPG - 13 janvier 1997
ALPLOG – Grenoble - France

RAHMOUNI Maber
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Thèse de Doctorat INPG - 21 février 1997
Hewlett Packard – Bristol - UK

WAHBA Ayman
Diagnostic des erreurs de conception dans les circuits digitaux: le cas des erreurs simples
Thèse de Doctorat UJF - 7 mai 1997
Associate Professor at Ain Shams University – Cairo - Egypt

OLIVEIRA DUARTE Ricardo
Techniques de conception et outils de CAO pour la génération des parties opératives auto-contrôlables
Thèse de Doctorat INPG – 30 juin 1997
Post-doctoral position at University of Belo Horizonte - Brazil ("Univ. Federale de Minas Gerais")

MOHAMED Firas
Approche à base de logique floue pour le test et le diagnostic des circuits analogiques
Thèse de Doctorat INPG – 3 juillet 1997

LIEM Clifford Benjamin
Compilateurs multicibles et outils pour les processeurs embarqués dans le cadre d'applications industrielles
Thèse de Doctorat INPG – 18 juillet 1997
Improv Systems Inc. – Santa Clara – California – USA
BERREBI Elisabeth
Méthodologie pour l'application industrielle de la synthèse comportementale
Thèse de Doctorat INPG – 11 décembre 1997
SGS-Thomson – Crolles - France

KODRNA Marc
Étude des oscillateurs contrôlés en tension pour les circuits à Fréquence Intermédiaire – Analyse et simulation du bruit des oscillateurs
Thèse de Doctorat INPG – 12 décembre 1997
SGS-Thomson – Grenoble - France

DAVEAU Jean-Marc
Spécifications systèmes et synthèse de la communication pour le co-design logiciel/matériel
Thèse de Doctorat INPG – 19 décembre 1997
Post-doctoral position at IBM New York

NACABAL François
Outils pour l'exploration d'architectures programmables embarquées dans le cadre d'applications industrielles
Thèse de Doctorat INPG – 27 février 1998
SGS-Thomson – Crolles - France
VIII.2 Press articles in 1997

In the following are collected copies of articles that appeared in Newspapers in 1997.
SUMMARY

✓ Réseaux de neurones en orbite

✓ 0.25 μm CMOS Process Eligible For Prototyping To Schools, Labs

✓ Intellectual Property

✓ Les réseaux de neurones blindent l'électronique spatiale

✓ Simuler des capteurs avant de lancer la production, c'est possible !

✓ Les principales filières technologiques

✓ « Cerveaux artificiels » dans l'espace

✓ Start-up issue du laboratoire TIMA-CMP

✓ Processus CMOS 0.25 μm pour Recherche et Education

Hubert CURIEN, Minister for Research and Technology, in Grenoble in 1986 (Daniel BLOCH, Chairman of INPG in 1986).
✓ Microelectronics Education

IEEE DESIGN & TEST OF COMPUTERS Vol. 14 n°4
October/December 1997

✓ En collaboration avec SGS-Thomson

ELECTRONIQUE INTERNATIONAL HEBDO n°286
27 November 1997

✓ From War Zone to Boardroom in 8 years

ELECTRONIC NEWS Vol. 43 n°2195
24 November 1997

✓ L’accès aux microsystèmes – MEMSCAP

ELECTRONIQUE INTERNATIONAL HEBDO n°285
20 November 1997

✓ Première société privée de conception de microsystèmes en France

ELECTRONIQUE INTERNATIONAL HEBDO n°283
6 November 1997

✓ Réseaux de neurones : des « cerveaux artificiels » dans l’espace

LE JOURNAL DU CNRS n°95
November 1997

✓ Les microsystèmes arrivent à maturité

L’USINE NOUVELLE (hors série)
October 1997

✓ Propriété intellectuelle : les briques virtuelles font revivre la conception

INDUSTRIES & TECHNIQUES n°785
September 1997

✓ LDSD97 success in Portugal

III-Vs REVIEW Vol. 10 n°5
August 1997

✓ Vers un standard européen pour les formats d’échanges de données en CAO

ELECTRONIQUE n°70
May 1997

✓ Le CMOS standard s’adapte aux contraintes de l’espace

ELECTRONIQUE INTERNATIONAL HEBDO n°262
24 April 1997

✓ MEMS the next word in auto parts

ELECTRONIC ENGINEERING TIMES
31 March 1997

✓ CAO de microsystèmes

INDUSTRIES ET TECHNIQUES n°780
March 1997

✓ Ils font bouger l’électronique française ... Moteurs technologiques

ELECTRONIQUE INTERNATIONAL HEBDO n°254
27 February 1997

✓ Micromachining gallium arsenide

MICROMACHINE DEVICES Vol. 2 n°1
January 1997

✓ Dialogue entre chercheurs et industriels

LE DAUPHINÉ LIBÉRÉ
18 January 1997

✓ L’INPG reconnu internationalement

LE DAUPHINÉ LIBÉRÉ
15 January 1997

✓ « Ouvrir les portes des fondeurs aux PME »

LA TRIBUNE
15 January 1997
Réseaux de neurones en orbite

En novembre dernier, un satellite scientifique américain, appelé MPTB, a emmené en orbite deux expériences portant sur des réseaux de neurones artificiels. But de l’expérience, fruit d’une collaboration entre le CNRS, le CNES et le CEA : étudier leur résistance à un environnement hostile, ici des rayons cosmiques qui peuvent changer l’état de bits d’information stockée dans des circuits intégrés. Raoul Velasco, chercheur CNRS au Laboratoire TIMA, espère ainsi montrer le profit que tireraient les missions spatiales à utiliser ces techniques. Calculés sur le fonctionnement du cerveau, les réseaux de neurones sont des systèmes parallèles et distribués de traitement de l’information. Implémentés sur des architectures standard, ils sont plus robustes que des ordinateurs classiques, organisés autour d’une unité centrale. Eternel problème de hiérarchie : touche la tête, et l’ensemble en est affecté. Mais les réseaux de neurones balaient cette belle organisation : composés d’un grand nombre de processeurs effectuant la même tâche, ils peuvent voir certains de leurs « neurones » détruits sans que le calcul soit affecté. On peut faire le parallèle avec le cerveau où chaque jour des milliers de neurones meurent sans effets apparents. Le réseau emporté par MPTB a été conçu pour isoler des textures particulières dans une photo. Les premiers résultats envoyés de MPTB confirment ce qu’attendaient les chercheurs du TIMA. Saluons la vaillance de cette machine, qui tolère environ 90% des modifications de bits provoquées par les radiations ! Un nouveau projet est en discussion, pour évaluer l’utilisation des réseaux de neurones dans la compression de données.

(1) Méthodologies des Photonics Test Bed.
(2) Laboratoire Technics de l’Informatique pour la micro-électronique et l’architecture d’ordinateurs de Grenoble.
0.25-μm CMOS Process Eligible For Prototyping To Schools, Labs

In cooperation with SGS-Thomson Microelectronics, Circuits Multi-Projets (CMP) has unveiled a high-performance deep submicron 0.25-μm CMOS process. The HCMOS7 process is available for prototyping to educational institutions and research laboratories, on a cooperation basis. No commercial designs are ready as of yet, but it’s expected that commercial versions will become available on a commercial basis for small volume production in the near future.

Gate length of the HCMOS7 shallow trench isolation process is 0.25 μm drawn, and 0.2 μm effective. It has up to six metal-layer levels with fully stackable contacts and vias. Power supply is 2.5 V, and threshold voltage is $V_{TN} = 0.5$ V, $V_{TP} = -0.5$ V. Full custom designs are supported using Virtuoso layout editor and LAS synthesizer. The layout verifications (DRC, ERC, extraction, LVS) are fully supported for Diva and Dracula. Transistor-level simulations are only supported under Eldo Level 59. Standard-cell designs are supported using Verilog/VHDL descriptions for synthesis and simulation. Synthesis is supported under Synergy or Synopsys, while simulation is supported under Verilog-XL, Leapfrog, and VSS. Among the various CAD software versions supported are: Cadence/OPUS version 4.3.4.50.106; Cadence/Dracula version 4.3.0996; and Eldo version 4.4.1. re

Circuits Multi-Projets, 46 avenue Felix Viallet, 38031 Grenoble Cedex, France; phone: +33 4 76 57 45 00; fax: +33 4 76 47 38 14; e-mail: cmp@archi.imag.fr; Internet: tima-cmp.imag.fr.

Edited by Roger Engelke
A new project, Assistec, supported by the European Commission under the ESPRIT program, has just been launched that aims to assist European small and medium-size enterprises (SMEs) in preparing their intellectual property (IP) for exploitation. The project, led by iprlas, a company specializing in the commercialization of intellectual property in the electronics and semiconductor industries, is designed to help SMEs by providing hands-on assistance from experts operating in this new market.

DO TAKE: This project is probably unique in the world and could be of great value to businesses in Europe. The IP market is set to grow at a compound annual rate of 65 percent for the next five years at least and is therefore a major emerging market. This is also a market in which small companies such as design houses can play a big part—provided the right legal infrastructure exists. To date, most of the benefits of collaborative European projects seem to have gone to large companies such as Siemens, Philips, and SGS-Thomson. Assistec could begin to redress the balance with its focus on smaller companies.

The deadline for applications is the end of March 1998, and the organizers expect that there will be several hundred potential candidates. In addition to the direct benefits to the participants, the commission will publish a number of "how to" guides based on case studies and on the experiences of the project members. These will be available to all companies.

Many smaller companies realize they are in possession of hot technology but do not know how to capitalize on it. Larger companies interested in buying IP are often reluctant to buy from small companies because they fear the small company will be unable to withstand a liability lawsuit. This project could go some distance to solving some of these problems. Europe has a larger number of independent design houses than other regions. These houses could be about to enter the IP market in a big way.

The assistance offered will focus on "prelicensing" activities, providing advice on the preparation and valuation of IP, the identification of markets and strategic partners, and the process of licensing and negotiation. Dataquest research suggests that these are the areas in which small companies have the greatest difficulties. A group of companies has been assembled with appropriate skills in both technical and commercial aspects from the United Kingdom, France, Germany, and Greece. The project has identified several types of IP, including software development tools, application software for embedded systems, system protocols, and interfacing. In other words, the remit is wider than semiconductor-implemented hardware forms of IP such as VHDL coded modules. In fact, much intellectual property exists in the form of algorithms or mathematical representations that are independent of any implementation method. The project should raise awareness of this.
Les réseaux de neurones blindent l’électronique spatiale

Une fois n’est pas coutume, c’est un laboratoire français, le CNRS-Tima, qui donne des leçons aux Américains en matière d’électronique spatiale. L’objectif est le suivant: faire aboutir des projets de constellations de satellites télécoms. On se hâte, en effet, à de vifs problèmes à mesure que l’électronique des produits se miniaturise. Dans l’espace, les microprocesseurs sont soumis à de fortes radiations cosmiques, elles-mêmes responsables de nombreux dysfonctionnements. Raoul Velazco, chercheur au laboratoire CNRS-Tima, a eu l’idée de recourir à l’intelligence artificielle, en particulier aux réseaux de neurones. Selon lui, « pour accomplir certaines tâches, les réseaux neuronaux se révèlent bien plus robustes et efficaces que les ordinateurs séquentiels ». Cette affirmation se fonde sur une longue série de tests effectués au sein d’un accélérateur de particules. Des essais qui se sont révélés concluants, puisque les réseaux de neurones tolèrent actuellement jusqu’à 80% d’erreurs, appelées « upsets ».


Tima ne compte pas s’arrêter pas en si bon chemin. Le laboratoire a déposé un brevet international pour « durcir » n’importe quel composant électronique. Pour cet organisme, « on pourrait faire une espèce de mutant de Pentium en agissant uniquement sur le design, sans changer ni la physique ni la chimie de fabrication. Il suffit pour cela de remplacer tous les points mémoires du circuit par des points mémoires spéciaux, appelés Hits (Heavy Ion Tolerant) ». Le procédé, commercialisé par la société Temic, est appliqué sur un circuit DSP/RT (Digital Signal Processors/Radiation Tolerant). Une bonne nouvelle pour les agences spatiales...

Erick Hauhnsen
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<th>Pression</th>
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<td>fax 01 43 74 20 98</td>
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<td>fax 01 69 28 44 29</td>
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<td>tél. 03 21 65 25 10</td>
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<td>fax 03 21 65 26 90</td>
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<td>tél. 04 75 79 67 53</td>
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<td>(département de Léo)</td>
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<td>tél. 03 81 48 43 43</td>
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<td>tél. 04 76 88 58 86</td>
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ELECTRONIQUE INTERNATIONAL HEDO N°293 – 5 February 1998

**SIMULER DES CAPTEURS AVANT DE LANCER LA PRODUCTION, C'EST POSSIBLE!**

En coopération avec Mentor Graphics, Memscap, société créée par essaimage de Timain, fournit des kits de conception pour les microsystèmes spécifiques aux technologies supportées (technologies d'usinage en volume et en surfaces compatibles ou non avec la microélectronique). Ces kits comportent des règles pour les dessins des masques, des modèles de simulation, des générateurs de dessin pour les structures, des outils pour la vérification de la gravure anisotrope et pour la visualisation en couleur au niveau du dessin des masques ainsi qu'un lien avec les simulateurs par éléments finis (SEM). Ce lien s'effectue par le biais d'un outil de génération de modèles comportementaux (C'est-à-dire en HDL-A) à partir du modèle en éléments finis (SEM). Ce outil, qui représente un travail de 24 hommes-année, a été transféré récemment de l'université de Darmstadt par Memscap. "Ce kit permet à des non spécialistes de pouvoir intégrer des microsystèmes dans leurs systèmes à bas coût", note J.M. Karam, fondateur de Memscap.
Les technologies de micro-usinage sur silicium sont les plus courantes pour réaliser des capteurs très intégrés.

Le centre suisse de microélectronique (CSEM), le groupe microsystèmes du CMP (circuits multiprojets) et le Léti sont les principaux centres permettant aux industriels de réaliser des capteurs sur mesure. La mise en place, au cours des dernières années, de services de fabrication collective (plusieurs circuits sur une même tranche) permet aux petites et moyennes entreprises de faire fabriquer leurs capteurs sur mesure. Les services vont de l'aide à la conception jusqu'à la production en petites séries ou en volume du capteur. Ces laboratoires proposent chacun différentes filières technologiques adaptées à différents types de capteurs. L'usinage du quartz pour la réalisation de structures résonantes (proposé par le Léti et Sextant Avionique au travers d'Europapractice) ainsi que par le groupe microsystèmes du CMP), du verre pour la fabrication de lentilles diffractives (proposé par le CSEM) et du fer-nickel sur substrat silicium pour la réalisation de capteurs inductifs constitués de bobines (proposé également par le CSEM) sont des filières dédiées à des capteurs relativement "magnétiques". L'usinage du silicium fournit, par contre, un large éventail de possibilités pour la réalisation de capteurs de grandeurs physiques : pression, accélération, température, infrarouge, etc. et permet, de plus, d'entrer dans l'ère des microsystèmes (capteurs et électronique de traitement associée). Deux technologies sont en compétition : l'usinage en volume et l'usinage en surface. Chacune a ses avantages et ses inconvénients (voir tableau). L'usinage en volume est proposé entre autres par le Léti, le CSEM et au travers du groupe microsystèmes du CMP. Il permet de réaliser des poutres et des membranes suspendues en gravant le silicium en profondeur sur plusieurs dizaines de microns. Ces dernières sont alors isolées mécaniquement et thermiquement du substrat. L'isolation mécanique permet, elle, de réaliser des capteurs infrarouges. Le procédé d'usinage en volume reste toutefois délicat à mettre en œuvre. Pour gravir rapidement le silicium en profondeur (pour construire les poutres et les membranes suspendues), il faut, en effet, s'éloigner des procédés classiques de gravure chimique utilisés en microélectronique, trop lents. Cette gravure (isotope ou amiante) se fait alors par des solutions chimiques très fortes comme l'hydroxyde de potassium (KOH) ou l'hydroxyde de tétraméthylammonium (TMAH), de nature toxique. L'usinage en surface (proposé par le Léti et le CSEM) vise, lui, à construire le capteur à partir de procédés classiques : des couches minces sont déposées sur le substrat silicium (oxyde, silicium polycristallin, métal, tungstène...) puis gravées. Cette filière permet de réaliser des membranes suspendues très fines et de petites masses mobiles qui sont adaptées aux capteurs de pression et d'accélération mais aussi à des actionneurs électromécaniques (une structure en couches minces présente très peu de couple moteur). Les couches déposées étant minces et la distance entre membrane et substrat très faible (inférieure à 1 μm dans certains cas), les capteurs de ce type sont généralement à un principe de détection capacitive.

(*) Europapractice est un programme européen qui propose une offre de service pour faciliter la diffusion des circuits spécifiques, MCM et microsystèmes. Le regroupement français chargé de la fabrication de microsystèmes sur mesure est constitué de Sextant Avionique, du Léti, du Laas et de la Sagem.

<table>
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<td>Avantages</td>
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<td>Inconvénients</td>
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<td>Type de capteur</td>
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L'accès aux technologies du Léti peut se faire via Europapractice et Troné's Microsystèmes. L'accès aux services du groupe microsystèmes du CMP se fait via Memscap, qui devrait bientôt proposer également l'accès à des techniques de micro-usinage du GaAs.
Réseaux neuronaux

"Cerveaux artificiels" dans l'espace

Pour aller plus loin dans les compétences des ordinateurs, on a développé des approches neurales, qui pourraient s'avérer robustes dans des environnements hostiles tel l'espace. Le point sur les expériences en cours.

Bien que les calculatrices deviennent de plus en plus performantes, leur "intelligence" reste encore loin d'atteindre celle d'un cerveau biologique. Pour comprendre certains des mécanismes du cerveau et pour imiter son modèle de traitement, des biologistes et des mathématiciens ont étudié depuis les années 40 ce qu'on appelle les "neureones artificiels". Pourtant, les premières implantations de circuit intégré neuronaux ne sont apparues qu'au cours des années 80. Certains de ces circuits peuvent comporter un très grand nombre de processeurs identiques interconnectés, sans accomplissant la même tâche comme les neurones biologiques du cerveau. Dans un calculateur "classique", dérivé du modèle de Von Neumann, la pièce maîtresse est l'unité centrale. Il résulte de ce contrôle centralisé qu'une défaillance dans cette unité aura probablement pour résultat de mettre hors service l'ensemble du calculateur, alors que la défaillance d'un ou plusieurs neurones artificiels ne perturbera pas le fonctionnement du réseau de neurones. Cela n'est pas étonnant puisque un réseau de neurones imite le fonctionnement d'un cerveau biologique, dans lequel des milliers de neurones sont détruits chaque jour sans effet apparent.

Des réseaux de neurones pour accomplir certaines tâches à bord de satellites

Dans l'espace, les instruments utilisant des dispositifs microélectroniques sont exposés à un environnement radiatif sévère de radiations provenant des coûts de Van Allen ou du cosmic. "En raison de leur miniaturisation de plus en plus poussée, les perturbations dans les systèmes électroniques deviennent de plus en plus fréquentes" affirme Renaud Velasco, chercheur CNRS à TIMA (Techniques de l'Informatique et de la Microélectronique pour l'Architectore d'ordinateurs). "Dû à leur robustesse intrinsèque vis-à-vis des erreurs, il apparaît que pour certaines fonctions, les réseaux de neurones artificiels sont plus à même d'un fonctionne-

Exemple de photo prise par le satellite SPOT. (Document : CNES).

ment fiable sur les satellites que les approches plus classiques". Les tests effectués avec des accélérateurs de particules sur une architecture digitale adaptée à l'implantation d'approches neurales, pourraient être pertinentes. En effet, en raison de la haute rédundance de traitements, le réseau neuronal testé n'est réellement capable de tolérer jusqu'à 90 % d'erreurs appelées "upset" (inversion d'un bit d'information mémoire dans un circuit). Ces erreurs d'upset apparaissent lorsque des particules chargées (ions lourds, protons) présentes dans l'espace, traverse des zones sensibles d'un circuit intégré embarqué à bord d'un véhicule spatial.

Deux cartes digitales permettant d'épurer de ces neurones artificiels ont été conçues par TIMA en collaboration avec le CNES et le CEA, et sont incluses dans le projet MPTB (Microelectronics and Photonics Test Bed) du Naval Research Laboratories (Washington DC) et du Naval Research Laboratory (Washington DC).

Un satellite scientifique américain emboîtant les 24 expériences du projet MPTB, dont deux d'entre elles sont les cartes neuronomes de TIMA, a été lancé avec succès en novembre 1997. L'objectif des expérimentations de TIMA est d'obtenir des données sur le comportement des algébristes et circuits neuronomes dans un environnement radiatif très intense. Les résultats des expériences de TIMA au sein du projet MPTB, pourraient permettre une plus grande utilisation dans l'espace d'approches basées sur des neurones artificiels. Le problème limitant des neuronomes artificiels est celui de la reconnaissance de quatre textures précédement (mat, épaisse, ville et zone industrielle) dans des photos prises par le satellite SPOT. Tout dépend de ces textures testées et utilisées dans le projet MPTB par l'Architecte de l'ordinateur.
au sol pour une analyse à distance. "Une image SPOT comprend typiquement 300 millions de pixels ; son traitement partiel à bord du satellite améliore fortement son utilisation, particulièrement pour des applications telles que la prévention de catastrophes naturelles". Il faut remarquer que les deux expériences de TIMA à bord de MPTB peuvent également être utilisées pour évaluer le comportement en environnement radieux d'autres programmes (basés ou non sur l'approche des réseaux neuronaux). En effet, l'une des contraintes établies par Raoul Velasco est la possibilité de programmer (par l'envoi de commandes et de données appropriées) par la station de contrôle au sol, une ou deux des cartes de TIMA à bord du satellite MPTB.

Au moment de la rédaction de cet article, les premiers résultats de vol ont été transmis et satisfont pleinement aux attentes. L'expérience était réprogrammable, les chercheurs ou industriels qui voudraient évaluer des stratégies de traitements de données dans un environnement sévère, sont invités à prendre contact avec le laboratoire TIMA pour analyser et éventuellement adapter leur problème au "laboratoire spatial" MPTB.

Avant même d'avoir reçu les premiers signes de vie des cartes neurales à bord de MPTB, les chercheurs de TIMA ont été contactés par la NASA pour participer à de nouvelles expérimentations destinées à l'analyse du comportement de composants commerciaux complexes dans l'espace : projet STRV2 (Space Technology Research Vehicle). Les expérimentations TIMA incluent dans STRV2 qui sera lancé en 1999 par Ariane 5, ont pour objectif l'évaluation de la stratégie à utiliser pour commander le mouvement d'un robot marin (projet européen "InterMars").

* TIMA est un laboratoire de recherche du CNRS, d'environ 100 personnels, associé à l'IPNPG (Institut National Polytechnique de Grenoble) et à l'UPJF (Université Joseph Fourier). Les deux groupes de recherche de TIMA travaillent sur les outils et les méthodologies de CADS, la conception de circuits intégrés et les techniques de test associées à la conception de ces circuits.
Start-up issue du laboratoire TIMA-CMP (commun à l'INPG, à l'université Joseph Fourier et au CNRS), la nouvelle société Memscap est la première entreprise française à se lancer dans la conception et la commercialisation de composants microsystèmes. Elle vient de conclure un contrat avec le CNES pour des applications spatiales et va prochainement créer une filiale aux États-Unis et deux au Proche-Orient. Memscap vise un chiffre d'affaires de 50 MF dans les cinq ans. Contact : Jean-Michel Karam, tél. : 04 76 57 45 00 (Grenoble).
Processus Cmos
0,25 μm pour
Recherche et
Education

En coopération avec
SGS-Thomson Micro-
electronics, CMP
(Circuits Multi-Projets)

annonce un processus Cmos submicro-
nique pour prototypage pour la Recherche
et l’Enseignement. Le process HCMOS7
présente les caractéristiques suivantes :
grille 0,25 μm (traîne) et 0,2 μm (effet fil);
jusqu’à six niveaux de métal ; alimentation
2,5 V ; tensions VTN = 0,5 V et VTP
= -0,5 V ; Ion : TN @ 2,5V : 600 µA/µm ;
Ion : TP @ 2,5V : 300 µA/µm. Les concep-
tions à la demande utilisent l’éditeur
Virtuso, les outils de vérification Dracula
e et Diva de Cadence et le simulateur Eldo,
les cellules standards font appel à la syn-
thèse/simulation Verilog/VHDL de
Cadence ou de Synopsys et au place-
ment/routage CellG de Cadence.
Aylor:

“Achieving a multidisciplined graduate is not just a microelectronics problem. It’s really a school of engineering problem.”

Courtois:

“Technology is too dynamic... Take the transition to deep submicron. How can we get our hands on everything we need to educate students about it?”

becoming much more important. We’re looking at increases to 50 or 60 watts.

Felinsmith: The curriculum needs restructuring. Industry wants grads who know how to do system-level design, say, 100,000 gates. They’ve got to know not just schematics, but design languages like VHDL and Verilog. Only 25 percent of all designs are currently done in VHDL, but in three to four years—when it counts—that’s likely to be more like 60 percent or more.

D&T: So what specifically is wrong with the curriculum and what are the challenges associated with changing it?

Cavallaro: It still reflects the 1980s generation design—when we all learned VLSI and custom chips. Industry is now worried about higher-level issues.

Hines: People want to put complex systems on a chip, so we have to go beyond a single discipline like VLSI or logic design. But we learned, and it’s still true, that change doesn’t happen in zero time. Universities must very quickly put into place mechanisms and curricula to address the problems, and they’ve got to do it collaboratively. How do we get the mechanical engineers to work with the electrical engineers and computer scientists with the thermal people to do the analog design?

Cavallaro: This multidisciplinary approach is even more important as we transition from VLSI to microelectromechanical systems. But it might be too early to worry about MEMS. The tools aren’t there yet.

Courtois: We already have a VLSI-MEMS split even without the tools. The tools may not be completely there, but they’re close, and we’ve been able to move some microelectronics people to design MEMS. We’re beginning to overcome the split using CAD.

Pina: What about rapid prototyping skills? The designs that come from NSF-sponsored VLSI classes are about 70 percent analog, which you can’t really simulate.

Aylor: Achieving a multidisciplined graduate is not just a microelectronics problem. I’m sure chemical engineers worry about what they’re going to do in electronics. It’s really a school of engineering problem. People are trying to break down the stovepipes of chemical, electrical, and mechanical. The problem I see is how to define a core curriculum. Until we know exactly what it is we have to teach in four years, we can’t possibly expect to organize anything across disciplines.

Hines: Engineers come out at a master’s level specialized in some way, which is why industry hires them. We need to figure out how to provide the balance of training for engineers within the current ground rules and guidelines for the basic 120 to 124 credit hour curriculum and provide additional materials to integrate these engineers across disciplines. We should work with the ABET community to see how we can fit the right pieces and snippets of material into the existing structure.

D&T: Ours is one of the most rapidly changing technologies at the moment, so industry is hiring our guys right at the bachelor’s level. I almost wish they wouldn’t because they’re not ready yet. If we could get everyone, especially students, to think along the lines of six years, we could be as broad and general in the four years as we’d like and then spend the next two being specialized. Students could pick up a lit-
En collaboration avec SGS-Thomson, le CMP (Circuits Multi-Projets) de Grenoble ouvre un service de réalisation de prototypes de circuits intégrés en technologie Cmos 0.25µm. Il sera ouvert aux laboratoires de recherche et aux universités.
Jean-Michel Karam
From War Zone To Boardroom In 8 Years

By Chad Fasca

GRENoble, FRANCE—Jean-Michel Karam, a high technology entrepreneur at 28 years old, has gone from the war zone to the boardroom in roughly eight years.

In 1990, he left Lebanon, then in the midst of a 17-year war, to study engineering in France. He arrived that year in Paris at age 20. Seven years later in 1997, he has just founded a high tech company—Memscap.

The company’s main area of business is the design and development of Micro Electro Mechanical Systems (MEMS) technology, referred to in Europe as Microsystem Technology and in Japan as Micro Machines. The MEMS market comprises telecommunications, aerospace, medical and automotive industry applications, and Memscap will not be shy in approaching this market with a special emphasis on CAD tools and intellectual property (IP).

The technology for MEMS is said to have already caught the eye of the likes of Delco, Motorola, Xerox, Bosch, Semicon (a Norwegian company), and Daimler-Benz, most of which have captured research and development programs.

“Today in MEMS, if you’re a system company (you fabricate phones, toys...) and you need to integrate a MEMS device realizing a function, you need to hire engineers, to develop a technology and to invest a lot before you can get your component within your system. Memscap will offer to these systems houses a low cost solution, since they will just need to get a fully characterized MEMS component from our IP library and plug it in their systems,” said Dr. Karam.

In terms of CAD products, Memscap plans to offer engineering kits that extend the capabilities of currently available IC design frameworks to systems engineers. Still in its corporate infancy, Memscap has not waited to make partners in the industry. The company has already established a partnership with Mentor Graphics Corp. in the area of CAD tools.

Mentor Graphics will provide the toolset, while Memscap will provide the technology specific MEMS kits, which, according to Dr. Karam, incorporate MEMS libraries, behavioral and layout level language, extended design rules and integrated tools for model generation. One of the tools, successfully transferred from Technical University in Varmstadt, Germany, is HDL-A; soon Memscap expects to add VHDL-AMS and Verilog-A standards for its system-level verification and manufacturability analysis.

In addition to the kits, Memscap will provide component engineers with a selected toolset, including field solvers and translators—mainly through exclusive agreements with OEMs. It has been said that the company has reached an agreement with Intelinse in this area but this could not be confirmed. It is through these partnerships that Memscap plans to address other market segments like high temperature and space environments. CAD for MEMS is only one focus of the company. According to Dr. Karam, the other focus is MEMS and analog and mixed signal IP. The company is cooperating with the industry and universities to build its intellectual property base.

Memscap is a commercial spin-off from TIMA-CMP, where Dr. Karam founded the Microsystems (MEMS research) group in 1995 under the stewardship of laboratory director Bernard Coutots. TIMA represents the research arm of the laboratory, while CMP forms the services arm, and is a broker in ICs and systems fabrication for a number of technologies involved in prototyping and low volume production. Together, TIMA-CMP is a research and service unit of the French National Scientific Research Center (CNRS). The laboratory also falls under the direction of the French Ministry of Education and Research and has links to two universities, the National Polytechnical Institute of Grenoble and the Joseph Fourier University.

Dr. Karam’s group at TIMA has been primarily industry-driven. Given the close contact fostered between the group and industry interests, he has developed quite a few contacts which facilitated the spin-off. Also a factor in the decision, was Dr. Karam’s own restlessness.

“Bernard gave me my chance, so I launched the Microsystems (MEMS) group, and worked hard to get this group at the level it is today. And now that the group is sufficiently strong... I thought that the best thing is to realize my dream of launching a company as a spin-off on the research activities of my group,” he said.

Now a seven-engineer company, he predicts $10 million in turn-over by 2001 for Memscap. Although the industry is not heavily tracked, Ernst and Young is said to have released a study gauging MEMS as a $14 billion industry.
**L'accès aux microsystèmes**

**MEMSCAP**

MEMscap, créée il y a quelques semaines par essai-mage de Tima-CMP, laboratoire du CNRS, est le premier fourisseur privé de composants virtuels et réels de microsystèmes en Europe. La société prévoit d'être bénéficiaire dès la première année et va ouvrir d'embée une filiale commerciale aux États-Unis. Si elle tient ses promesses, MEMscap aura prouvé que les microsystèmes sont enfin devenus une réalité industrielle.
Première société privée de conception de microsystèmes en France

La société grenobloise Memscap, nouvellement créée, est la première société privée de conception et de commercialisation de microsystèmes en France. Elle vise 50 MF de chiffre d’affaires d’ici 5 ans.

Jean-Michel Karam, responsable du groupe microsystèmes au laboratoire Tima-CMP (voir notre numéro du 12 décembre 1996), vient de créer, par assujettissement, ce qui est à notre connaissance la première société privée française de conception et de commercialisation de composants microsystèmes (jusqu’ici, en effet, le développement des microsystèmes pour le marché libre est le fruit de laboratoires publics). Basée à Grenoble, la société, baptisée Memscap, aura deux activités principales. Elle proposera des microsystèmes particulièrement dédiés aux environnements extrêmes et aux applications radiofréquences (voir tableau), mais aussi des outils d’aide à la conception de microsystèmes. Memscap ne dispose d’aucun moyen de production, ses microsystèmes seront fabriqués par des fournisseurs extérieurs.


Memscap affirme être déjà en contact avec des clients pour ses microsystèmes. Elle a reçu le soutien du Cnes (division composants et assemblage) sur des évaluations de technologies des microsystèmes pour les applications spatiales. Des discussions sont, par ailleurs, en cours sur différents projets associant un financement de l’Anvar. Enfin, pour viser d’emblée un marché mondial, la société va mettre en place une filiale aux États-Unis et d’autres au Proche-Orient.

« La société démarrera avec un capital privé de 400 kF (planifié à 1 MF d’ici trois mois). L’objectif est d’atteindre 50 à 60 MF de chiffre d’affaires dans les cinq ans. Nous serons bénéficiaires dès la première année », nous a confié Jean-Michel Karam.
RÉSEAUX DE NEURONES

Des « cerveaux artificiels » dans l’espace

Si les ordinateurs sont de plus en plus performants, leur « intelligence » n’est pas pour autant comparable à celle d’un cerveau. C’est à la fois pour tenter de comprendre les mécanismes du cerveau et pour imiter sa façon de calculer que des biologistes et des mathématiciens se sont penchés, dès les années quarante, sur l’étude des neurones artificiels. Les premiers ordinateurs neuronaux n’ont pourtant vu le jour que dans les années quatre-vingt. Ils se composent d’un très grand nombre de processeurs identiques, reliés entre eux, et qui effectuent tous la même tâche, comme les neurones d’un cerveau. Dans un ordinateur séquentiel classique, la pièce maîtresse est l’unité centrale. Si la moindre erreur se glisse dans celle-ci, l’ordinateur est hors d’usage, alors que la défaillance de quelques neurones artificiels ne gêne pas le fonctionnement du réseau. De même, des milliers de neurones sont détruits chaque jour dans le cerveau sans que l’effet s’en fasse sentir. « Dans l’espace, les instruments de microélectronique sont mis à rude épreuve du fait de l’intensité des radiations cosmiques. Et avec la miniaturisation des circuits, les perturbations dans les systèmes électroniques sont de plus en plus fréquentes », précise Raoul Velazco, chargé de recherche au CNRS, au sein du Laboratoire techniques de l’Informatique et de la microélectronique pour l’architecture d’ordinateurs (Tima) à Grenoble. « Or, poursuit Raoul Velazco, du fait de leur plus grande résistance au rayonnement, il apparaît que les réseaux de neurones artificiels sont plus aptes à être embarqués dans l’espace que les ordinateurs séquentiels. » Les essais effectués en laboratoire, notamment dans des accélérateurs de particules, le prouvent. Grâce à leur grand nombre d’interconnexions et de processeurs, les réseaux neuronaux tolèrent, en effet, jusqu’à 80 % de fautes (inversion des bits d’information) induites par les radiations sans que leur fonctionnement en soit perturbé. Deux « cartes neuronales » mises au point par Raoul Velazco et Robin Rolland, ingénieur d’études au CNRS, en collaboration avec le Centre national d’études spatiales, le Commissariat à l’énergie atomique et le Naval Research Labs (Washington), vont être installées à bord du satellite scientifique MPTB (Microelectronics and Photonics Test Bed) qui devrait être lancé avant fin 1997 et qui embarquera un total de 24 expériences, pour la plupart américaines. Objectif : tester pendant trois ans le fonctionnement des deux « cartes » mises au point par Tima en ambiances radiatives réelles. « Cette expérience permettra sans doute de généraliser l’utilisation dans l’espace des réseaux de neurones artificiels de façon à réaliser, en dépit des radiations, les études in situ », souligne Raoul Velazco. Ainsi, au cours de la mission, les deux cartes électroniques de Tima analyseront directement...
le contenu des images prises par le satellite Spot. « Une image satellite faisant 300 millions de bits, son traitement sera plus rapide s’il peut être réalisé à bord plutôt qu’au sol », poursuit-il. Toutefois, ces cartes électroniques peuvent avoir d’autres applications. Raoul Velazco lance donc un appel aux chercheurs qui souhaiteraient expérimenter d’autres types de mesures ou de contrôle comme, par exemple, l’arrimage de véhicules spatiaux sans intervention humaine. Avant même le lancement du satellite MPTEB, les chercheurs grenoblois ont été à nouveau sollicités par la Nasa pour une deuxième expérience embarquée (en 1999), qui préparera l’expédition, au début du deuxième millénaire, d’un robot sur la planète Mars.

En attendant de véritables missions dans l’espace pour les « cerveaux artificiels » du laboratoire Tima...

Laurence Menu

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Les microsystèmes arrivent à maturité

Automobile, médical, électroménager, les microsystèmes font partie de la vie courante. Ils trouvent leur place dans des applications où la sécurité est une préoccupation majeure.

On appelle « micromachines » ou « microsystèmes », ces puces électroniques d’un nouveau genre revêtent une dimension de la vie quotidienne. Elles sont présentes dans les airbags de nos véhicules, dans les patchs médicaux sur les plaies, et même dans les fers à repasser, ou encore dans les machines à laver le linge.

Le microsystème, c'est ce qui permet d'ajouter de l'intelligence dans les objets du quotidien, assure François Baillieul, professeur et président du comité scientifique microélectronique et informatique de l'Ésiee (Ecole supérieure d'ingénieurs en électronique et électricité). Cette démarche s'adresse plus particulièrement aux PME, auxquelles elle entend offrir un apprentissage pratique grâce à ses moyens internes (salles blanches, laboratoires, lignes de production et de composants, etc.), et, bien entendu, à ses élèves. L'École fait partie des organismes à la pointe des développements en microsystèmes.

Dans la grande famille des puces, les microsystèmes ont cette particularité d'être directement interfacés avec le monde physique. Ils sont en effet composées d'un capteur et/ou d'une partie électronique de traitement et/ou d'un actionneur et/ou d'une alimentation. Pour les plus complexes, on les appelle microsystèmes autonomes, capables de réagir à des stimuli extérieurs.

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L'importance du service
Il y a tout juste deux ans, un rapport de synthèse du CEA-Leti sur le moins que l'industrie montrerait une forte capacité de l'industrie française en matière de développement de microsystèmes. « La situation en l'architecture et le CMP (Circuits multiprojets). Deux sociétés liées aux laboratoires du CNRS de Grenoble. Ils ont une importante activité de services auprès des entreprises. « Nous sommes la première société de services en Europe à réaliser des microsystèmes, assure Bernard Courtois. Cette notion de service est très importante dans ce domaine relativement neutre. »

France devrait évoluer rapidement, souligne tard les auteurs. C'est chose faite. « Nous avons participé à l'un des derniers à dix-neuf projets », explique Bernard Courtois, directeur de Tima (Technique informatique et microélectronique pour

Deux grands marchés
Tel qu'il se présente actuellement, le marché des microsystèmes se divise grosso modo en deux. D'un côté, il y a les puces relativement simples et donc peu chères, qui s'adressent à des secteurs de forts volumes. Il s'agit de l'automobile (airbags, contrôle de l'injection, etc.), de l'électroménager (niveau de remplissage, contrôle de la consommation, etc.), de la péri-informatique (téléphone-Portable et d'impres- sion) ou de l'environnement (déter- teurs de gaz). De l'autre côté, ce sont des systèmes beaucoup plus complexes, avec un coût en proportion. C'est le médicale (chirurgie à inversion minima, principalement), mais aussi et encore l'automobile (suspension active, par exemple).

Ce sont, bien sûr, d'abord les marchés de forts volumes qui sont visés par les industriels. Les puces ne comportent souvent qu'un élément sensible (le capteur) et guère plus d'une autre fonction.

Dans l'automobile, les accéléromètres pour airbags arrivent en tête, avec les capteurs de pression pour l'injection et des Marchés supérieurs.

DES LOGICIELS ADAPTÉS POUR LA CONCEPTION

On construit un microsystème sur le papier, rien de plus aisé.

L'industrialiser, voilà qui est plus ardu. « Si des logiciels de CAO adaptés ne sont pas disponibles pour concevoir les puces, les microsystèmes resteront du domaine des laboratoires, » assure Bernard Courtois, directeur de Tima. Le passage à l'industrialisation nécessite des outils qui simplifient la conception de circuits et qui la généralisent. De tels logiciels commencent à voir le jour, issus pour une part des laboratoires, dont Tima, mais aussi de Mentor Graphics, numéro 2 mondial de la CAO électronique, ou encore du grenoblois Dolphin Integration, un spécialiste des circuits complexes. »

Cont'd
à 10 millions de pièces par an. Les grands du domaine sont les équipementiers Delco et Bosch, ou encore le fabricant de semi-conducteurs Analog Devices.

Dans le médical, ce sont les capteurs de pression sanguine qui viennent en tête, avec un marché estimé en 1995 à 20 millions de pièces par an. Parmi les principaux fabricants, tous américains, on note Motorola et Texas Instruments.

En péri-informatique, deux secteurs représentent les plus forts volumes. Les têtes d’impression pour la technologie jet d’encre sont fabriquées principalement par des sociétés comme Hewlett-Packard, Canon, Xerox ou Olivetti. Le marché est estimé à 8 millions de têtes par an. Les têtes de lecture-écriture pour disques durs sont l’apanage d’IBM, de Corner et de la start-up française Silmaz. Le grenoblois envisage à lui seul de produire 25 millions de pièces cette année et trois fois plus l’an prochain.

Motorola s’est pour sa part spécialisé dans les systèmes de détection de gaz. Le géant d’Austin a même créé une division pour cela il y a deux ans, Sensors. Les premiers produits sortent de la ligne de fabrication de Toulouse. Ils permettent de déterminer des molécules de CO avec une précision allant de 10 à 100 ppm. D’autres capteurs devraient suivre, notamment pour la détection du méthane.

**Le domaine de la sécurité**

Dans le haut de gamme, les réalisations ne sont pas moins nombreuses.

Les laboratoires Fourier ont réalisé un patch actif qui comporte un microcontrôleur, un capteur, une électrode et une alimentation. Il ouvre de grands horizons aux traitements ambulatoires. Le patient n’est plus astreint à des homéopathes contraignants. Les débits sont programmables et modulables. L’injection des molécules se fait de manière continue.

L’Etsic a réalisé pour Sub un dispositif destiné à remplacer la traditionnelle goutte de mercure, en passe d’être interdite, dans les fers à repasser, et qui sert à cuire le contact lorsque le fer n’est plus en position de travail.

Le laboratoire Tima de Grenoble a travaillé avec la société montpelliéraine Beverly sur le développement d’un capteur pour le contrôle de la pression du fluide cérébro-spinal afin d’éviter les accidents cérébraux en cas de sur- ou de sous-pression, après, par exemple, une opération chirurgicale. La pression est surveillée et mesurée grâce à une électronique intégrée. La transmission vers l’extérieur se fait par couplage électromagnétique. Le médecin est ainsi informé en continu de l’état du patient.

S’il fallait résumer en un mot la finalité de l’existence des microsystèmes, ce serait celui de sécurité. Ils ont un bel avenir devant eux !

*J.P. V.*
Jean Mermet, représentant de l'alliance VSI (Virtual Socket Interface)

Propriété intellectuelle : les briques virtuelles font revivre la conception

Jean Mermet, directeur de recherche au CNRS au sein du laboratoire Tina, à Grenoble, et directeur de l'Ecsi, support de l'alliance VSI en France.

Industries et Techniques : La notion de propriété intellectuelle est loin d’être nouvelle. Le secteur électronique donne pourtant l’impression de la découvrir brutal. Pourquoi ? Jean Mermet : La propriété intellectuelle n’est pas non plus une idée nouvelle en électronique, mais les fabricants de circuits l’ont longtemps verrouillée en contrôlant toutes les étapes de conception et de fabrication, où en partageant ce contrôle avec des donneurs d’ordres souhaitant bien évidemment garder la maîtrise de leur produit. Dans les deux cas, l’innovation provenait d’une société et d’une seule, souvent d’une simple équipe de conception, et ne diffusait pratiquement pas dans l’industrie. Les choses ont commencé à changer quand l’écart entre les progrès réalisés dans les techniques fabrication des circuits (+60% par an) et ceux que connaissent les outils de conception (20% par an) est devenu non seulement évident mais gênant. En effet, la faiblesse relative des outils de conception ne peut être compensée qu’en réalisant une proportion de plus en plus grande de parties déjà conçues, aussi bien au plan matériel que logiciel. Autrement dit, en ayant recours à la propriété intellectuelle, limitée à l’entreprise même dans un premier temps, mais puisée à l’extérieur dans un second.

I&T : La réutilisation de composants pose-t-elle des problèmes spécifiques ? J.M : La réutilisation de composants virtuels sous formes de blocs fonctionnels n’est possible que s’ils ont été conçus dans ce but. Cela induit un surcoût, important en phase initiale, mais nécessaire pour que des designs émanant de n’importe quel point du globe et de n’importe quelle entreprise ou individu puissent être proposés sur Internet, choisis et enfin mélangés au sein d’un nouveau design. À terme, la conception de “systèmes sur une puce” se fera un peu comme celle des logiciels aujourd’hui. Nous en sommes loin, mais c’est précisément le but de l’alliance VSI (Virtual Socket Interface) que je représente en Europe.

I&T : Quels premiers résultats tangibles l’alliance VSI peut-elle mettre à son actif ? J.M : Six groupes de travail se partagent la tâche à accomplir. Les thèmes choisis recouvrent la conception au niveau systéme, la protection de la propriété industrielle, le tandem implantation et vérification, les tests de fabrication, l’intégration des bus sur la puce et enfin le mode mixte numérique-analogique. Les groupes de travail chargés de ces deux derniers thèmes viennent de publier des spécifications...
LDSD 97 success in Portugal

Mohamed Henini, Conference Chairman

There has been tremendous growth in LDSD since the first meeting in Singapore in 1995 and it was interesting to consider developments and changes. LDSD is now of fundamental importance for electronics, optoelectronics, and photonics applications. This year's conference in Lisbon, Portugal, again featured a strong interdisciplinary technical program involving all aspects of the technology from material growth to device applications.

The statistics show that there was an increase in the number of participants attending LDSD97 and submitted papers. This number reflects the fact that LDSD has been making up a firm basis not only as a research and development area, but also as a mainstream technology in the semiconductor industry.

The meeting was attended by over 200 participants drawn from a large number of countries.

There was an excellent technical program consisting of nine invited papers, and well over 170 contributed oral and poster papers. We had an exceptionally good response to our Call for Papers from all over the world, and a really hard time to select papers out of 350 submissions.

The invited talks were given by: Dr S. Nakamura (Nichia Chemical Industries Ltd, Japan) who discussed the major developments in wide-gap III-V nitride semiconductors; Dr P. M. Campbell (Naval Research Laboratories, USA) who reviewed the principles and applications of the proximal probe-based nano-fabrication technique; Prof. R. M. Biefeld (Sandia National Labs, USA) who reported on mid-infrared emitters in the 3–6 μm range; Dr M. Abe (Fujitsu, Japan) who spoke on the HEMT technology which is expanding its application into personal mobile communications and other areas; Prof. W. Kowalsky (University of Braunschweig, Germany) who showed the potential of the organic semiconductor materials for photon and electronic device applications; Dr P. D. J. Calcott (Defence Research Agency, UK) who gave a detailed account of the recent research activities on porous silicon; Dr K. Ismail (IBM, USA) whose talk concerned the evolution of the Si/SiGe material system; and Dr J. Benoit (BERTIN & Cie, France) and Dr B. Courtois (MPC, France) who discussed several aspects of microsystems and their applications in new markets.

In addition to the invited talks, there were 58 oral contributed talks and over 120 posters. These posters were displayed during the whole conference so that poster presenters could explain their work and this provided the usual lively debate. The following papers were of particular merit.

R. Beccard et al. (Germany) presented a class of multiwafer MOVPE reactors which have proven to produce high quality GaN based materials. Excellent thickness homogeneities, very good doping uniformities, and quantum well structures with very sharp interfaces were demonstrated.

Optical properties of the first fully monolithic MBE grown II-VI microcavity LED structure emitting at 502 nm were reported by P. Uuismaa et al. (Finland). A CdZnSe quantum well was placed in a ZnSSe A-cavity between MgZnSSe/ZnSSe distributed Bragg reflectors. Electrical injection tests showed a very narrow spectral width of 6 nm. The authors believe that in spite of the technological problems related to device fabrication, the MgZnSSe/ZnSSe/CdZnSe material system has

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Scanning electron micrograph of an array of highly uniform and ultra sharp tips produced in n-type <100> single crystal silicon using isotropic plasma etching. Tips are 2 μm high and have a radius in the sub 10 nm region. Each tip is capable of producing an emission current of 5 mA under continuous operation.
the potential for fabricating high efficiency surface emitting devices.

M. Suzuki et al. (Japan) described a new concept of thin film processing in materials synthesis based on particle–surface interaction during deposition. Practical applications of various thin films to automobiles were presented, including thin film polarizers of obliquely co-deposited thin films, giant magnetoresistive sensors for speed sensors, and structural and optical properties of organic/inorganic superlattices.

Ultra-sharp single crystal silicon emitters with radius <10 nm have been fabricated by S. E. Huq et al. (UK) in gated configuration using a combination of high resolution electron beam lithography and plasma dry etching. Their electrical measurements confirmed that the emitters can be operated well below 100 volts gate bias producing high emission current. Microfabricated silicon tips are becoming increasingly important for use as field emitters. Applications include high resolution and low power field emission displays, and radiation resistant ultra high speed vacuum microelectronic and microwave devices.

S. Faard et al. (Canada) have successfully grown red-emitting quantum dot (QD) lasers by MBE using self-assembled growth mechanism. They found that the external efficiencies of the QDs were comparable or even better than the one measured on a standard GaAs quantum well. Using simple broad area laser devices, their QD lasers operate at room temperature with threshold current densities of a few kA/cm².

The flexibility of hydride vapour phase epitaxy (HVPE) for fabricating nanostructures was demonstrated by E. R. Messmer et al. (Sweden). They reported (i) improved optical characteristics of etched wires after regrowth, (ii) improved electrical characteristics of reactive ion etched wires after regrowth, and (iii) selective growth of InP templates on maskless GaAs substrate for nanostructure fabrication.

R. P. Ribas et al. (France) discussed the GaAs front-side bulk micro-machining using the 0.2 μm HEMT MMIC technology. Several chemical solutions have been used and it was found that citric acid is the most appropriate etching solution to suspend the GaAs/AlGaAs mesa-shaped structure, while the H₃PO₄ : H₂O₂ : H₂O and NH₄OH : H₂O₂ : H₂O preferential etching systems are very suitable for the triangular prism-shaped structures. They have also demonstrated that they can add specific micromachining based post-process in order to accommodate microsystems within GaAs integrated circuits.

Hybrid arrays of thirty-one LEDs were designed by A. Rys et al. (USA) for a modern spectrometer for consumer and medical applications. Arrays for the 800–950 nm spectral range were fabricated from commercially available GaAs-based LED chips. Arrays for the 1100–1650 nm were constructed from InGaAsP quaternary alloy for surface emitting infrared LEDs. Custom made chips provided the surface emitting LEDs with high radiance and superior far-field patterns. A temperature sensor and a photodiode were also incorporated on the hybrid circuit to control the temperature and light intensity of the diodes.

D. H. Zhang et al. (Singapore) have shown that high quality GaAs/InGaAs/AlGaAs VCSELs could be grown by MBE at a constant temperature. The layer thickness in the whole device structure, including the active region, and the n- and p-type distributed Bragg reflectors, were monitored and controlled by a system including an infrared pyrometer. The devices with a pattern of 15 × 15 μm² showed a threshold current of 0.7 mA and a maximum output power of 800 μW at a laser wavelength of 945 nm at room temperature continuous wave operation.

LEDs with an unconventional design were made on patterned GaAs (311)A oriented substrates by P. O. Vaccaro et al. (Japan). A lateral p-n junction was formed in the GaAs-silicon doped epilayers grown by MBE. Their devices showed good electroluminescence at room temperature. The use of a lateral p–n junction allow direct injection of electrons and holes in the active layer of devices such as lasers diodes without having to overcome the large band gap layers used for optical confinement, and would improve modulation speed and power conversion efficiency.

O. K. Kwon et al. (Korea) have studied the effect of design parameters on non-biased optical (NOB) bistable devices using multiple quantum wells nipi-diode structures. It was found that by optimising the stack pairs the performance of the NOB device was significantly enhanced with a large signal contrast ratio, low power dissipation, and low drive voltage, while maintaining low switching energy.

Contrary to the conventional externally biased devices, NOB devices in an array are electrically independent of each other and a more densely packed optical bistable array can be realised in a simple layout. The authors claim that this scheme will be useful in all-optical switching and processing devices for optical interconnection.

The whole meeting was complemented by an active social programme, and exhibition of equipments from several companies. A highlight of the social programme was the setting, magnificent food and entertainment provided for the conference banquet at the famous Estoril Casino on the Estoril coast. A pleasant opportunity to learn something more about the history and landscapes of Lisbon and Lisbon coast.

In conclusion the meeting introduced many new areas to the audience and raised a number of interesting points in our minds. In particular I emphasise the issues of blue lasers and fabrication of nanoparticle scale devices. A major extra quality of this meeting was that both senior and enthusiastic junior researchers could equally present their work. This was an excellent meeting, the format and numbers encouraged a friendly and intimate atmosphere.

Finally, I would like to express my gratitude to all who have contributed to this conference. I am also grateful to the members of the organising and International Committees who provided valuable assistance at different stages of the process.
VERS UN STANDARD EUROPÉEN POUR LES FORMATS D’ÉCHANGES DE DONNÉES EN CAO
Dans le cadre du projet OMI (Open microprocessor systems initiative) du programme Esprit, Alcatel Mietec, Compass, Mentor Graphics, Nokia, SIDSA, Telefonica I+D, Thomson-CSF et Viewlogic se sont associés pour produire un modèle pour l'échange de données entre outils de conception électronique. Le modèle couvrira les bibliothèques d’Asic au niveau portes ainsi que les cellules contenant la propriété intellectuelle. CMP Service à Grenoble offrira une assistance technique dont la coordination sera assurée par l’ECSTI (European CAD standardisation initiative). La durée du projet est d’un an.
Le CMOS standard s'adapte aux contraintes

En analysant très finement les contraintes liées à l'utilisation d'une technologie CMOS standard aux contraintes de l'espace, l'équipe Tima-CMP de Grenoble devance les besoins des prochaines générations de satellites.

Il sera désormais possible d'utiliser une technologie CMOS standard pour réaliser des circuits électroniques et des microsystèmes répondant aux contraintes de l'espace. L'utilisation d'une telle technologie à la place des actuelles technologies SOI a l'avantage de réduire les coûts d'un facteur de près de 3\(^3\). « Nous sommes face à une modification structurelle des besoins : les satellites sont de plus en plus tournés vers les applications commerciales (réseaux de télécommunications, images). Or, dans ce domaine, les technologies et les besoins évoluent sans cesse, ces satellites deviennent rapidement obsolètes. » Aujourd'hui, il est ainsi plus rationnel de tableer sur une durée de vie de 5 ans, et non plus de 15 ans comme par le passé. Nous sommes donc contraints de trouver des solutions pour que les satellites aient moins cher. Cela passe par l'utilisation de microsystèmes (diminution du poids) et de technologies CMOS standard. Voilà pourquoi nous avons retenu la technologie CMOS à barrière d'isolation par jonction. Nous avons également étudié la tenue aux radiations de cette technologie en descendant à un niveau physique très bas pour définir des règles de bonne adéquance, le but étant que les circuits gardent leurs caractéristiques sur 5 ans lorsqu'ils subissent des radiations de 200 krad\(^4\), sans être bénêtrés, souligne Filipe Vinci Dos Santos, responsable de projets au groupe Microsystèmes du CMP\(^5\).

La conception de circuits tenant aux radiations exige aussi quelques précautions, surtout pour les circuits numériques, puisque les ions lourds –des particules chargées de l'espace– peuvent induire une erreur sur un mot binaire. Aussi faut-il utiliser des techniques de vérifications pour détecter tout changement binaire sur un mot ou sur une opération\(^6\). Le CMP a déjà fourni de tels circuits à Sodern. Cette société française spécialisée dans la fabrication d'équipements spatiaux vient d'ailleurs de l'utiliser pour réaliser un système assurant l'autopositionnement de satellites en orbite autour de la terre (il sera intégré au satellite Stentor réalisé sous l'égide du CNes).

LE SYSTÈME DE SODERN EN TECHNOLOGIE STANDARD CMOS

Ce système destiné au positionnement de satellite est composé de deux circuits : un capteur infrarouge composé d'un réseau de 4 paires de thermopiles sur silicium qui fournit une "image" de la terre et d'un circuit assurant l'interface entre les thermopiles et le système de gestion de positionnement du satellite. Les thermopiles sont réalisées par un procédé suspendu en silicium. Elles sont basées sur l'effet de Seebeck (une différence de température induit une différence de tension). Lorsque la puce reçoit l'image de la terre, des ondes infrarouges viennent l'arroser. La détection de l'image de ces dernières se fait sur la thermopile grâce à 40 thermocouples répartis sur le pont. Il suffit donc d'adresser chaque thermocouple pour reconstituer l'image. Pour ce faire, le circuit électronique comprend un multiplexeur analogique à 32 voies qui permet d'adresser chacun des thermocouples et un amplificateur faible bruit. Le multiplexeur est caractérisé par un temps d'établissement de 0,5 \(\mu s\) et fonctionne à une fréquence de 100 \(Hz\). Il consomme 104 \(mW\).

L'amplificateur faible bruit, quant à lui, est caractérisé par une bande passante de 5 MHz au gain unité, un bruit de 10 nV/\(\sqrt{Hz}\) et une consommation de 50 \(mW\). Une version monolithique incluant les thermopiles et l'ASIC est en cours de développement pour démontrer qu'il est possible de faire un véritable microsystème en utilisant des technologies standard. Nous travaillons également au développement de technologies BiCMOS ainsi qu'à d'autres types de capteurs, notamment les capteurs à base de transistors photosensibles qui permettent de réaliser des viseurs d'étalons pour l'espace\(^7\) mais aussi des caméras faible coût pour la visuconférence par exemple », nous a révélé Jean-Michel Karam, chef du groupe microsystème au CMP.

(*) Les capteurs de types APS (active pixel sensor) présentent plusieurs avantages par rapport aux capteurs CCD. Ils sont en effet faciles à intégrer en technologie CMOS, consomment moins et ont un niveau de bruit plus faible. Utilisant des phototransistors, ils nécessitent par conséquent plus de silicium que les capteurs CCD. Le rapport entre la surface activée et la surface utilisée est d'environ 20% actuellement (22% pour la NASA). L’objectif est d’atteindre les 50%.
(1) La technologie SOI, par exemple celle de Matra-MHS (appelée DMILL), peut être accessi-
sible par Europractice (droit d'entrée 97 500 F) et est annoncée à 4 485 F par mm². Le CMP, en utili-
sant une technologie CMos standard, annonce un coût de 1 600 F/mm². Notons par contre que les
caractéristiques de la technologie DMILL sont à
prion prises trop bonnes pour les satellites en orbite autour de la terre: la DMILL de Matra-MHS, qui
est une technologie SOI, tient des doses pouvant
atteindre jusqu'à 350 krad, alors qu'un satellite géo-
stationnaire subit des doses de 100 krad. A noter que
les circuits décisifs (normes militaires) ne représentent
plus que 4% des ventes mondiales de semi-conduc-
teurs. (Source: CMP).

(2) La méthodologie de test ESA:SCC BS22900 a
ici été choisie. Le circuit tient en fait des doses de
800 krad.

(3) Rappelons que le CMP (Grenoble) a été permi
tes premiers à introduire le concept de fabrication col-
llective. Il fournit aux industriels un service de
 conception, de prototypage et de fabrication de
 microsystèmes à faible coût (1 500 F/mm² pour
15 échantillons).

(4) Pour la partie numérique, des structures paral-
lèles doivent être mises en œuvre pour s'assurer de la
bonne validité du mot ou d'une opération binaire
(une addition est faite deux fois et les résultats sont
comparés).
The increasing prevalence of electronics in automotive design is starting to drive electronic design automation (EDA) software in some new directions. Though there is little unique about automotive electronics, EDA vendors will be challenged to meet some specific needs.

Perhaps the most fundamental issue is that electronic and mechanical design are inevitably linked in the automotive world. Every electronic component is part of some kind of mechanical-electrical sub-system and sometimes the electronic circuitry is so closely tied to mechanical parts that it's hard to tell where one ends and the other begins.

That's especially the case with micro-electromechanical systems (MEMS), which are becoming increasingly commonplace in automotive design. MEMS devices include tiny sensors, actuators, accelerometers and other devices that are usually fabricated using silicon technology.

While most MEMS devices are discrete, in the future some will reside on chips with digital and analog circuitry. That prospect calls for a whole new generation of design tools that combines aspects of EDA and mechanical CAD.

"The electrical engineer is a minority in the car world," noted Gerry Cilibariss, executive engineer at Chrysler's Small Car Platform division (Auburn Hills, Mich.). "Most of the resources and the tools are oriented to the mechanical design of the car. We have to make certain we understand what the mechanical guys are doing—it's our job to communicate with them."

That communication may be the weakest link in the automotive EDA world right now. "We are actually uninterested," said James Sickkinnen, a development engineer working on MEMS devices at Delco Electronics Corp. (Kokomo, Ind.). "We have two vastly different worlds that are going to have to come together."

Siekkinen is working on MEMS devices such as air-bag accelerometers, fuel pressure sensors and manifold pressure sensors. This design starts in the mechanical CAD world with the Ansys finite-element analysis software from Swanson Analysis Systems (Houston, Pa.). For physical design, however, Sickkinnen's group turns to the IC Graph product from Mentor Graphics Corp. (Wilsonville, Ore.).

There is no integration between these tools; what's more, IC designers and sensor designers have totally different styles, said Sickkinnen. The guys doing IC design can do a functional block-level layout, whereas we're doing things off the top of our heads," he said. "We sort of have design rules, but we break them when we see fit. The IC layout tools with a MEMS library developed in France.

The kit uses HDL-A, a version of analog VHDL developed by Mentor's Anacard subsidiary, to model electromechanical systems. It offers process-independent layout generators for bridges, membranes, cantilevers and generic structures.

"I don't think we're going to be buying it right now, but at some point we're going to have to look at this [kit] pretty closely," said Sickkinnen. He said he's looked at other MEMS tools and feels this is the first integrated solution from a large enough company to offer good support.

At Delco, the MEMS devices Lewis said that the ADXL chips include a fair amount of analog circuitry and just a few digital gates. Because the dynamic range is 60 dB to 80 dB, analog blocks are fairly simple and straightforward, such as amplifiers and buffers. In terms of area, he said, about two-thirds of the chip is now electronic circuitry, down from five-sixths or so with the early devices.

The design has started at a low level of abstraction. "We tried doing some behavioral modeling work, but it turns out the shortcomings hit so quickly we pretty much right away went to the full transistor level," said Lewis. Analog Devices' internal Adice analog simulator has some improved behavioral modeling capabilities, as do commercial simulators, so analog behavioral modeling is a good possibility for the future, Lewis said.

But modeling the accelerometer still poses a big problem. "The biggest issue has to do with being able to model the sensor and get the mechanical and electrostatic behavior quickly and being able to generate a good enough model so we can do system-level tradeoffs," Lewis said. "We found all sorts of interesting second- and third-order effects over time and if we had a better sense of modeling, we'd be even further ahead."

To design accelerometers, Analog Devices' designers work mostly with Ansys. They get approximations of mechanical and electrostatic properties and develop a Spice-compatible model for use with a full-chip simulation. "The initial one took a long time, but what we do now is take that core model and modify it with the differences between the beams," said Lewis.

The chip-level simulation is a challenge, he noted, because it must analyze events occurring over many milliseconds of time. Plus, it's a full-transistor-level simulation.

For chip layout, Analog Devices uses the Virtuoso product from Cadence Design Systems (San Jose, Calif.). This full-custom layout editor works for MEMS devices on silicon, but it's not ideal, Lewis noted. "The shapes you make for some of these structures are nothing you'd make a transistor look like."

MEMS ENGINEERING KIT COMBINES EDA, MECHANICAL CAD

A new generation of tools seeks to bridge electro-mechanical gap

MEMS WILL

RESIDE ON CHIPS

WITH DIGITAL

AND ANALOG

CIRCUITRY

guys do things completely by design rules."

To use Ansys, engineers identify materials' properties and performance requirements and build a mesh so the tool can run a 3-D field solution. The tool can predict the amount of mechanical movement in the structure, the stress and strain and other important characteristics. But none of this information is automatically transferred to IC Graph.

Seeking a more integrated solution, Sickkinnen has been looking at a new product suite offered by Mentor and Circuits Multi-Projects (Grenoble, France). The MAP/Mentor Graphics MEMS Engineering Kit combines Mentor Graphics schematic, analog behavioral simulation and IC layout tools with a MEMS library developed in France.

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CONTINUED ON PAGE 145
MEMS THE NEXT WORD IN AUTOMOTIVE PARTS

he said. “One of the big problems with design-rule checking is that you’re allowed to check one in a layer spacing. But we have many different minimum spacings and we just can’t check them in a straightforward way.”

To overcome some of these design tool limitations, Analog Devices is working with Microcosm (Cary, N.C.) as a contractor under the DARPA Composite CAD program (see Jan. 20, page 4). Lewis said Analog Devices will seek to integrate its tools with the MemCAD product from Microcosm, which is aimed at MEMS design but takes a very broad perspective in terms of applications. To this end, Analog Devices hopes to help Microcosm focus more closely on its needs and “do a smaller subset better,” Lewis said.

There are, however, automotive designers focusing purely on ASIC or IC design and they’re putting their own demands on EDA tools. Because chips must fit inside constrained spaces, compactness is a driving issue. And cost, generally related to compactness or density, is also crucial because of the high volumes involved.

Delco is designing high-density communications ICs for such applications as digital-audio broadcasting and digital receivers, and is using a behavioral synthesis tool originally developed at the General Motors Research Center (Warren, Mich.). This tool, Autocircuit, is primarily aimed at data-path-intensive designs.

Recently, Delco licensed Autocircuit to Datasys Inc. (Pittsburgh), which incorporated the technology into RapidPath, a product it announced in September 1996. While Autocircuit is aimed primarily at area optimization, Datasys has added timing optimization to make it more applicable outside the automotive realm. Autocircuit recently produced first-pass silicon success on two ASICs for digital/audio broadcasting, both 500,000 to 1 million transistors, fabricated in 0.5-micron technology. “I think the real success story here is that a system engineer can target first-pass silicon success without a lot of IC background,” said Terry Beale, advanced project engineer at Delco.

Before using Autocircuit, Beale noted, Delco engineers spent approximately nine months writing a register-transfer level (RTL) Verilog description of the first of these communications ICs. After they started working with Autocircuit, they were able to reduce the design behaviorally in about three weeks. They did a comparison with the layout generated from Autocircuit to that generated from RTL synthesis and concluded that Autocircuit produced a more efficient layout.

In benchmarks against the Synopsys Behavioral Compiler, Autocircuit was 50 percent better in data-path-dominated designs, according to Tom Fuhrman, staff research engineer at GM’s Research and Development Center. One reason is that Autocircuit directly targets the Epos data path compilers from Cascade Design Automation (Bellevue, Wash.).

Control logic goes through the Synopsys Design Compiler or Cascade’s Finesse synthesis tool.

“There really was no commercial synthesis tool that took advantage of row-column, bit-sliced layout structures for data path design,” said Fuhrman. “That’s real important for automotive design, with the emphasis on small die size and cost reduction.”

Complete system

At some point, all the devices produced by automotive designers have to come together into a complete system or subsystem and that’s where Fuhrman’s group takes over at Chrysler. His organization is responsible for all of the electrical systems in a car. At the moment, one key challenge is finding a better way to define and track requirements that are ultimately passed along to subcontractors.

“We’re trying to become more disciplined in developing requirements, and we’re instituting systems engineering into our process,” he said. Recently, his group has purchased the RDD-100 tool from Ascent Logic.

As an example, Chrysler has used Saber to model the operation of automobile headlamps. Both mechanical and electrical issues are involved. Writing the Mast models isn’t necessarily an easy task; a cooperative effort through the Society of Automotive Engineers is trying to ease the task by developing a common pool of models. Participants include Chrysler, GM and Ford, along with Analog. “All the car companies use basically the same suppliers and we don’t want to maintain three or four different kinds of models for exactly the same product,” said Cilibrasi.

MEMS BEING DEVELOPED

Inc. (Andover, Mass.). The Saber analog simulator from Analogy Inc. (Beaverton, Ore.) is heavily used for analysis—but not necessarily for electronics. “We don’t do much analog circuit design,” said Cilibrasi.

“We use Saber to model things like alternators or motors in a vehicle and switches and relays.”

One reason that Saber can be used for such purposes is that it provides extensive behavioral modeling capabilities through its Mast language. Thus, the modeling that Cilibrasi does is “as high level as possible” and is far above Spice-level modeling.

For mechanical CAD, Chrysler engineers make heavy use of the Catia tool from Dassault Systems (Suresnes, France). There’s a connection between this tool and Logical Cable, a Mentor Graphics product for designing wire harnesses. Called E3L Cable, the interface lets Chrysler engineers spatially locate modules using Catia and then feed that information into a schematic.

Even though there’s a good set of tools, more needs to be done to build the kind of design environment Cilibrasi wants. “We’d like to be able to take a design proposal and automatically run it through requirements. Right now people do a simulation on Saber and feel proud they have a good accurate simulation. Then they stop; they don’t run simulation through all the scenarios thought of during the requirements planning. We need to bridge that gap.”
CAO de microsystèmes

Le "Design Kit Merr" de Mentor Graphics serait le premier environnement de CAO complet permettant l'intégration de microcapteurs et d'ASIC sur la même puce de silicium. Il comprend une bibliothèque étendue de modèles (accéléromètres, capteurs de pression, capteurs magnétiques ou chimiques...) développés en HCL-A. Son simulateur mixte Continuum analyse et vérifie le système complet au niveau mécanique et électronique. Il en découle une grande précision de fonctionnement.
They are moving the French electronics industry

DOSSIER

André-Jacques ALBERTON-HERVÉ
déjà de Suisse

In March 1967, André-Jacques Alberton-Hervé, creator of Grenoble's Sootec, founded the company Sotelec, which, in 5 years, has almost doubled its workforce and turnover, and now employs more than 650 people. At the same time, Sotelec has been awarded several major contracts, including the construction of a new industrial park in Grenoble, which will provide 150 new jobs.

Joël MONNIER
directeur de la recherche centrale de SGS-Thomson Microelectronics

At the heart of research and development, SGS-Thomson has developed its expertise in a wide range of technologies, including compound semiconductors, for which it has a world-class capacity. The company's strategy focuses on vertically integrating its R&D and production sites, which it is doing with the purchase of a new factory in Grenoble.

Michel UGON
directeur de la R&D du CEA Rennes

Michel Ugon is not interested in being a one-man band. He has a team of 20 people working in the field of semiconductor physics, electronics, and communications. The company is currently involved in developing a new type of photonic device, which promises to be a game-changer in the field of telecommunications.

Michel Karam
responsable du groupe Micro-systemes au CMP

Jean Michel Karam is a developer of microcontroller technology, with a special interest in the creation of new devices. He has worked on developing a new type of microcontroller, which he believes has the potential to revolutionize the electronics industry.

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Report from FRANCE

Micromachining gallium arsenide

French researchers from CMP in Grenoble and Exeo Centrale de Lyon reported at the recent SEMICON/Southwest-SPIE micromachining symposium on processes that have been employed for gallium arsenide micromachining. They discussed:
- Pros and cons of GaAs as a micromechanical material
- Data on GaAs mechanical, thermal, and piezo properties as well as GaAs chemical etchants
- MESFET and HEMT compatible micromachining.

The following is a summary.

**GaAs etching: Wet vs. dry**
As with silicon, etching processes used for GaAs microstructuring can be either wet or dry. Liquid-based etching process can be enhanced galvanically or by an external supply of electrons (anodic etching). Processes that are basically chemical but need surface excitation (plasma induced etching, RIE, and reactive ion beam etching) fall under dry etching.

Most wet etchants for GaAs contain an oxidizing agent (usually Br₂, H₂O₂ or HNO₃), a complexing agent, and a diluant, such as water. The oxidized layer is often insoluble in water, but is made soluble by a complexing agent such as H₂SO₄, HCl, NH₃OH, NaOH, HF, or citric acid.

GaAs has a zinc blend structure; its etching mechanisms differ significantly from those of diamond-structured silicon. Etching rate depends on whether the surface plane atoms are gallium or arsenic. Etching rate also depends on orientation, increasing as (111)Ga < (100), (111)As < (110). When wet etching is limited by reaction rate, MESAs can be undercut in the 011-direction to form suspended structures. For diffusion-limited processes, the etch rate dependence on orientation almost disappears.

**Fabrication of suspended structures** by preferential etching can be achieved when the reverse MESA slopes join each other to create a freestanding cantilever (Fig. 1). This requires the use of etch-rate-limited etch systems (see table).

To achieve a good suspension structure, the etched walls must be of perfect reverse MESA shape and have a sufficiently low angle. The most suitable etchants are: Br₂, CH₃OH (etch rate: 6 μm/min), H₃PO₄, H₂O₂, CH₃OH (2 μm/min), H₃PO₄, H₂O₂, H₂O (1 μm/min), and H₂SO₄, H₂O₂, H₂O (14.6 μm/min).

Enhanced etching at mask edges and at n-doped zones is a common phenomenon that makes it difficult to achieve well-defined and reproducible structures. This should be considered when choosing an etchant and designing the mask. The H₃PO₄, H₂O₂, H₂O system is reported to be quite suitable since it exhibits a slow etching rate with excellent reproducibility, no doping-concentration dependence, and compatibility with photore sist as a mask.

**Dry etching** in contrast to wet etching, dry etching does not undercut the mask for GaAs. It offers high aspect ratios, high-purity etchants, no masking phenomena due to bubbles or surface diffusion, and fewer capillary problems in flushing away reactive species and reaction products.

On the other hand, most GaAs dry etching produces a damaged surface layer with built-in stresses. The most common techniques for dry etching GaAs are reactive ion etching (RIE), reactive ion etching.
Micromachining gallium arsenide continues from page 7

beam etching (RIE), and chemically assisted ion beam etching (CAIBE). Typical etchant gases include SiCl$_4$/SF$_6$/Cl$_2$/Ar, and BC$_3}$/Ar.

Devices and microstructures. The French researchers described two GaAs microstructure applications. The first was aimed at a sensor integrated with a Vitesse MESFET. The Vitesse MESFET foundry process (four metal-level) yields a 0.6 µm effective gate length transistor with an ion-implanted channel, source, and drain. Two operating temperature ranges are observed, the wider being

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Common etch-rate-limited systems for GaAs microstructuring

<table>
<thead>
<tr>
<th>System</th>
<th>Proportions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Br$_2$/C$_2$H$_5$OH</td>
<td>(4.96)</td>
</tr>
<tr>
<td>H$_2$PO$_4$/H$_2$O/H$_2$O</td>
<td>(1.9:1)</td>
</tr>
<tr>
<td>H$_2$SO$_4$/H$_2$O/H$_2$O</td>
<td>(1.8:1)</td>
</tr>
<tr>
<td>HCl/H$_2$O/H$_2$O</td>
<td>(1.19:1)</td>
</tr>
<tr>
<td>K$_2$Cr$_2$O$_7$/HCl/H$_2$SO$_4$</td>
<td>(2.1:2)</td>
</tr>
<tr>
<td>K$_2$Cr$_2$O$_7$/HCl/CH$_3$COOH</td>
<td>(1:1:1)</td>
</tr>
<tr>
<td>NH$_4$OH/H$_2$O/H$_2$O</td>
<td>(1:1.8)</td>
</tr>
<tr>
<td>Citric acid/H$_2$O$_2$/H$_2$O</td>
<td>(5 g:2 ml:5 ml)</td>
</tr>
</tbody>
</table>

-55°C to 125°C.

The simplest way reported for obtaining suspended structures in conjunction with the Vitesse process is to use preferential etching as described above. This technique demand no extra masking and no more than a simple dip in an etch solution. Post-process etching is performed with phosphoric acid.

Designs for mechanical structures such as bridges and cantilevers have been integrated with device circuitry, fabricated, and successfully tested using the MESFET process. For post-process etching, sufficiently large openings in the mask must be realized to obtain openings reaching all the way to the GaAs substrate. Post-process etching characteristics cannot all be estimated in advance, and a number of different structures were used to obtain at least several well-suspended structures. Other effects that can be examined include those due to ion implantation, doping, and piezoresistance.

The second application involves using a Philips Microwave Lifting process for a sophisticated GaAs/InGaAs/AlGaAs two-level metal HEMT transistor that can work above 80 GHz. A free-standing beam was produced by post-process wet etching with H$_2$O$_2$/NH$_4$OH. Designs with MEMS devices and integrated circuits have been fabricated over many runs, proving the reproducibility of the results.

VILLARD-DE-LANS ▼
INFORMATIQUE
Dialogue entre chercheurs et industriels

De l'avis de Bernard Courtois, organisateur du colloque "CAO de circuits intégrés et systèmes" qui vient de s'achever à Villard-de-Lans, il n'y avait pas eu un tel dialogue de qualité, d'ailleurs "très apprécié", entre l'université et l'industrie depuis plusieurs années.

Point d'orgue de ce dialogue, initié dans le cadre d'actions du ministère de l'Éducation nationale, de l'Enseignement supérieur et de la Recherche, un débat auxquels assistaient chercheurs et représentants de la plupart des industriels ou utilisateurs de CAO (conception assistée par ordinateur) électronique.

Une coopération difficile

A cette occasion, Michel Robert, chargé de mission auprès du ministère, a rappelé, devant 160 personnes, que le dernier comité interministériel de l'automne avait retenu 7 axes de développement, notamment concernant l'industrie électronique et le traitement de l'information. Conformément aux décisions adoptées, les réponses aux appels d'offres lancés doivent être formulées conjointement par l'industrie et la recherche.

Belle initiative. Toutefois, au cours d'un dialogue direct entre les uns et les autres il est apparu que, contrairement à ce qui semble se passer dans d'autres pays, la coopération université-industrie n'est pas toujours facile en France où les projets de CAO exigent beaucoup de moyens en hommes. Un produit de la recherche en électronique comme un logiciel est rarement utilisable directement par un industriel. Des efforts doivent donc être faits par les deux parties.

Un éventuel centre de diffusion

Il faut savoir que ces logiciels de CAO sont aujourd'hui des produits extrêmement complexes. Ils se sont à concevoir en effet des configurations de circuits intégrés qui rassemblent la bagatelle de 3 voire 7 millions de transistors sur 220 ou 324 millimètres carrés comme cela se pratique au sein de S.G.S-Thomson. C'est ce qu'a souligné Joseph Borrel, vice-président recherche et développement de la société. Au cours du débat, l'idée a été émise de l'éventuelle création d'un centre de diffusion dont le rôle consisterait à diffuser auprès de l'industrie les logiciels provenant directement de la recherche. Mais qui financerait ?

En tout état de cause et même si la coopération université/recherche est difficile, certains exemples prouvent qu'elle peut s'efficaciser avec succès. À Grenoble, un partenariat exemplaire a déjà permis que des logiciels du laboratoire TIMA (Techniques de l'informatique et de la micro-électronique pour l'architecture), dirigé par Bernard Courtois, soient utilisés par S.G.S-Thomson. D'autre part, des personnels de S.G.S-Thomson travaillent actuellement au sein de TIMA.

N.B.
L’UNIVERSITÉ

L’INPG reconnu internationalement

Au cours de la cérémonie de présentation des vœux par Maurice Renaud

"L’INPG (Institut national polytechnique de Grenoble) occupe une place enviable dans le milieu des universités françaises", c’est son président, Maurice Renaud qui le dit. Des propos tenus à l’occasion d’une cérémonie de présentation de vœux pour cette nouvelle année qui verra l’élection, fin mars, d’un nouveau président.

La grille d’évaluation des universités place en effet les enseignantschercheurs de l’établissement au même rang que ceux d’Orsay pour l’encadrement des thèses (0,5 par an et par enseignant), soit "une productivité deux à trois fois plus forte que la moyenne des universités scientifiques".

D’autres "signes tangibles" témoi-
« Ouvrir les portes des fondeurs aux PME »

Jean-Michel Karam est chef du groupe Microsystèmes de TIMA-CMP, une unité de service et de recherche du CNRS. Cette unité fonctionne comme un courtier en microtechnologies.

« La Tribune ». - On constate un certain retard des PME-PMI françaises dans le domaine des microsystèmes. Pourquoi ?

Jean-Michel Karam. - Jusqu'en 1995, les PME-PMI n'avaient pas les moyens d'accéder à des fonderies de silicium. Ce qui explique que le développement des microsystèmes s'est effectué dans de grandes structures comme Sagam, Sextant Avionique, Motorola et Schlumberger.

Que peut leur apporter un programme communautaire comme Esprit-Europractice ?

Ce programme lancé, il y a un environ, consiste à ouvrir aux petites entreprises les portes des fondeurs. L'idée est bonne, même si elle n'est pas nouvelle. En revanche, la pratique est mauvaise : il manque dans Europractice des programmes pour la CAO (conception assistée par ordinateur) des microsystèmes. Cela accroît la complexité de conception des produits. En comparaison avec les moyens importants engagés par le programme Esprit, il y a eu un nombre très réduit de lots en fabrication collective.

Qu'est-ce qui fait l'originalité de l'offre du centre Circuit Multï-Projets (CMP) ?

Ce centre, qui dépend du TIMA-CNRS (Techniques de l'informatique et de la microélectronique pour l'architecture d'ordinateur), donne aux PME-PMI un accès aux fonderies de silicium par bas coûts, un savoir-faire et des outils de CAO électronique très performants. En 1996, nous avons lancé trois lots en fabrication collective. Dix-huit microsystèmes ont été fondus chez le français ES2-Atmel, puis gravés dans des laboratoires dédiés comme celui de l'ESIEE à Paris ou le LEAME à Lyon. Les délais de fabrication sont de trois à quatre mois et le prix de la perte est de 1 500 francs par millimètre carré. Elle inclut, en outre, la fourniture de 15 prototypes.

Quels sont vos projets sur le plan industriel et technologique ?

Au niveau industriel, nous avons cinq à six projets à réaliser, de la conception jusqu'au prototype. Côté recherche, nous avons déposé un brevet sur un capteur d'accélération qui intéresse notamment les marchés de l'automobile, par exemple pour les suspensions actives. Par ailleurs, nous avons développé un nouveau capteur de température en technologie CMOS 0,8 micron qui a la particularité de supporter des températures comprises entre -50 et 150°C. Il peut être utilisé par exemple pour mesurer la pression des pneus.

E.K./TCA

Coups de puce européens

Pour aider les PME-PMI européennes à s'intéresser enfin aux microsystèmes, la Communauté européenne aide les « first users » (premiers utilisateurs). Elle finance la partie innovation technologique de leur projet au sein du programme Esprit-Fuse. D'autre part, le projet Esprit-Europractice indemnifie financièrement certains fondeurs de silicium, les fabricants de puces électroniques, à ouvrir leurs portes à de petites productions, pouvant aller de 500 à 1 000 pièces. En France, Sagam et Sextant Avionique ont été sélectionnés pour ce programme. Ils bénéficient du soutien technique de deux laboratoires publics : le LAAS/CNRS de Toulouse et le Léti/CEA à Grenoble. Ce dernier est d'ailleurs en charge de la promotion d'Europractice et du plan européen. À ce jour, une trentaine de projets ont été signés. Dont trois profitent à des entreprises françaises sises en France. Dix-sept autres projets français ont de bonnes chances de démarrer avant fin 1997.

E.K./TCA
VIII.3 Social life

Recently, the Laboratory had the pleasure to congratulate some of its members for marriage and births.

Have got married:

- Lydie HEUSCH (SANZ) 25 May 1991
- Masaki NITO 8 June 1991
- Mokhtar BOUDJIT 13 June 1992
- Pascale VERGUIN (DULIEUX) 4 July 1992
- Francois MARTIN 15 August 1992
- Ahmed Amine JERRAYA 26 September 1993
- Patricia SCIMONE (CHASSAT) 17 June 1995
- Sylvaine EYRAUD (LAYE) 24 June 1995
- Clifford LIEM 10 August 1996
- Kholdoun TORKI 22 July 1997

The following will be descendants of Laboratory's members:

- Emeric AMIELH 12 June 1991
- Luc BERGER SABBATEL 13 July 1991
- Aurelie GARNIER 7 September 1991
- Anna KOLARIK 20 September 1991
- Florian HEUSCH 2 November 1991
- Moussab BEN OTHMAN 21 November 1992
- Thail CASTRO ALVES 2 October 1993
- Natasha LUBASZEWSKI 3 May 1993
- Aladin SKAF 2 August 1994
- Gabriel GARNIER 28 August 1994
- Andressa LUBASZEWSKI 11 December 1994
- Lydia JERRAYA 3 February 1996
- Ceyla SIMEU 14 March 1996
- Jeanne DING 7 April 1996
- Lucas PEREZ-RIBAS 1 August 1996
- Carolina OLIVEIRA-DUARTE 15 September 1996
- Laurence SCIMONE 10 October 1996
- Paola VALDERRAMA 15 April 1997
- Gabriela LAPRESA RIBAS 23 September 1997
- Stephanie WANDER 10 November 1997
- Chloe EYRAUD 31 January 1998
- Manon COISSARD 13 February 1998

Some have even found their wife/husband in the Laboratory itself:


As for funds, the Laboratory has recurrent social events and exceptional social events. The mechouli's party is a traditional annual party. The Laboratory has been a few times horse-riding, even those being very beginners. Visitors are often taken for walks in the mountain. The following pictures are examples of this social life.
Picture VIII-3 1: Horse-riding across Vercors
Picture VIII-3 2: Annual parties in the open air
Picture VIII-3 3: Walk in the mountain with visitors

For example on this picture, one can see Marta RENCZ and her daughter (1st plan), or Janusz RAJSKI, Mc Gill University (1st plan too, with a hat) and his family.

Picture VIII-3 4: Skllng excursion
Picture VIII-3 5: 1996: Annual party in a restaurant

Picture VIII-3 6: The TIMA football team (that beat CSI 5-0 June 1992)
Picture VIII-3 7 : Marathonian Philippe KACZMAREK, accountant of TIMA-CMP

In Paris Marathon of 24 April 1994 (42.195 km), 18483 participants, among those 15961 completed the race, and Ph. KACZMAREK arrived 1228th... His position in his category (senior) has been 757th among 7515.