TIMA Laboratory
ANNUAL REPORT 1995
B. COURTOIS - March 1996
ABSTRACT

This is the 1995 annual report of the TIMA Laboratory (Techniques of Informatics and Microelectronics for Computer Architecture). The Laboratory is approximately 70 people large.

The Laboratory is organized in research groups: Analog Test Methods (ATM), Diagnosis of Complex Systems (DCS), Integrated Systems Design (ISD), MiCroSystems (MCS), Quality of Complex integrated Systems (QCS), Reliable Integrated Systems (RIS), System Level Synthesis (SLS). The Laboratory is also hosting the CMP Service, serving chips and microsystems fabrication.

Key achievements in 1995 have been the industrial use of AMICAL at SGS-Thomson and the introduction of CAD and foundry services for Microsystems. A remarkable event is starting January 1996: the group led by D. BORRIONE on Formal Verification has joined the Laboratory, increasing the synergy between design-test-verification. The Laboratory is organizing in 1996 the On-Line Testing Workshop in Biarritz, the THERMINIC Workshop on Thermal Investigations in Budapest, and the Symposium on System Synthesis in San Diego.

This year, the report is organized into 8 main sections including the Research and Service activities, the Resources and the Technology Transfer activities.

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I - OVERVIEW - GENERAL INFORMATION

I-1 Organization

Since 1971 this research organization targeted successively the design of the following pieces of hardware:

- Computers:
  + the geo-physical machine GEOPROCESSOR (1970/1975)
  + the PASCAL machine PASCHILL (1972/1981)

- Group microprocessor architectures:
  + electronic exchange system CANOPUS
  + the CORAIL machine
  + the CRESUS project

- Microprocessor type circuits:
  + microsequencer MSQ
  + microprocessor 8 bits NMOS P68
  + microcomputer 4 bits SOS MOM 400
  + the MOSAIC project for the architecture of VLSI systems
  + series line control by LISA microcontroller
  + microprocessor 8 bits POPY
  + microprocessor 8048 CMOS
  + microcontroller COBRA
  + mathematical coprocessor FELIN
  + compiled microprocessor 6502
  + MAPS controller
  + 1553 controller

- AI oriented machines
  + OPALE machine
  + LAIOS lattice
  + SPAN mechanisms
  + SYMBION architecture

- VLSI

- Macrosystems and Microsystems.

In 1995, the Laboratory was organized in 7 research groups, as listed below:

+ Analog Test Methods (ATM), B. COURTOIS / M. LUBASZEWSKI
+ Diagnosis of Complex Systems (DCS), M. MARZOUKI
+ Integrated Systems Design (ISD), A. GUYCT
+ MicroSystems (MCS), J.M. KARAM
+ Quality of Complex integrated Systems (QCS), L. BALME
+ Reliable Integrated Systems (RIS), M. NICOLAIDIS
+ System Level Synthesis (SLS), A.A. JERRAYA

In addition, the Laboratory is hosting the CMP service activity.
I-2 Research themes

Each topic of the research group is briefly described below:

* Analog Test Methods (B. COURTOIS, M. LUBASZEWSKI)
  This research group addresses the following topics:
  + unified testing of mixed-signal integrated circuits
  + analogue built-in self-test
  + boundary scan for mixed-signal on-line testing
  + automatic test pattern generation

* Diagnosis of Complex Systems (M. MARZOUKI)
  This research group addresses the following topics:
  + knowledge-based approaches and non-classic logic for test and diagnosis
  + MCM and partial boundary scan board test and diagnosis
  + mixed-system behavioral modeling
  + analog fault diagnosis
  + synthesis for testability

* Integrated Systems Design (A. GUYOT)
  This research group addresses the following topics:
  + arithmetic operators
  + full custom VLSI design
  + on-line operators
  + application of redundant number systems
  + digital signal processing
  + arithmetic operators testing

* MiCroSystems (J.M. KARAM)
  This research group addresses the following topics:
  + silicon compatible micromachining
  + CAD tools for micromechanical systems
  + microsystems for safety critical applications
  + thermal modeling

* Quality of Complex integrated Systems (L. BALME)
  This research group addresses the following topics:
  + modelling of complex integrated systems
  + total quality management window concept
  + surface mounted technology
  + automatic testing equipment
  + smart power card

* Reliable Integrated Systems (M. NICOLAIIDIS)
  This research group addresses the following topics:
  + self-checking circuits
  + built-in self test
  + test patterns for regular structures
  + CAD tools for testability
  + Radiation hardened/tolerant circuits
* System Level Synthesis (A.A. JERRAYA)
  This research group addresses the following topics:
  + hardware/software co-design
    - multiformat specification
    - partitioning
    - communication synthesis
    - multilanguage co-simulation
  + behavioral synthesis based on VHDL
    - scheduling
    - flexible and interactive synthesis
    - design re-use of complex cores
    - low-power design
I-3 Some past and recent realizations of the Laboratory

The following pictures illustrate some past and recent realizations of the Laboratory.

a) Cooperation with THOMSON led to the design of a self-checking, self-testing circuit (CMOS, 1.2 µ, 2 metallization layers, 650,000 transistors). The circuit is testable at the "transistors, metallizations, etc..." level (1985).

b) The SYCO silicon compiler took as input a behavioural ("Pascal like") description of the algorithms to be implemented in the silicon. b-1 is a 6502 CMOS control section compiled by the CPC specialized control section compiler; b-2 is a 6502 NMOS data path compiled by the APOLLON specialized datapath compiler (ca 1988).

c) Electron-beam testing has been experimented through two equipments: a CAMECA ST-15 electron-beam tester and a JEOL 35C scanning electron microscope equipped for voltage contrast. Those equipments have been served by a SUN and an IBM workstation, respectively (1987 - 1993).

d) The FELIN circuit was a design resulting from a cooperation with the Parallel Algorithmic Laboratory. It is aimed at the calculation of elementary functions like sine, cosine, etc... The circuit involved approximately 100,000 transistors, fully generated by a program describing the circuit (1987).

e) CMP National Service gives the possibility to Research Centers, Universities and Commercial Firms to have their circuits manufactured. The Université Catholique de Louvain, CNET-CNS, THOMSON, MIIS, ES2, TCS, AMS have manufactured bipolar, GaAs, NMOS and CMOS circuits for the CMP since 1981. One 4 inches wafer holds 73 CMOS different projects (15 wafers) and one 5 inches wafer holds 40 CMOS projects (5 wafers). Both have been processed by MHS, in 1986 and 1987, respectively.

f) The computing room regrouped computers that were not distributed in offices. Here are several SM 90, a SPS 9, and a MicroVAX. The air conditioned room had been fully remodeled in 1987 (electric power, floor, etc...). Today, all computers are distributed in offices.

g) In the past, computers have been designed. g-1 shows the GEOPROCESSEUR (1970) which resulted from a cooperation with IFP, g-2 depicts the PASCILL (1976) language oriented computer, and g-3 shows the CANOPUS (1980) system which resulted from a cooperation with CNET-LAA. Presently the computer architecture projects are dealing with parallelism and with a logic - numeric integration.

h) ADELAIDE was a project aimed at testing PCB populated by SMT devices. A prototype demonstrated the feasibility of an ATE, which uses extensively anisotropic elastomer conductors. Such a tool would allow a resolution of 10/1000 inches. The project has now been passed to industry.

i) Circuit synthesized by AMICAL (1993). This circuit is a PID synthesized by AMICAL (300 behavioral VHDL lines as input, 4000 RTL VHDL lines as output) feeding a commercial logic synthesis tool generating 50,000 transistors (20 mm², .8µ CMOS). Design time: 1 week. This design results from a hierarchical use of AMICAL. One of its components is a fixed point arithmetic unit that has been designed using AMICAL.

k) Microelectronics for Physics. BiCMOS wafer from CMP.

I) Micromachining by CMP. Process at industrial manufacturers, post-process at Central Laboratories.
a - Participation to a THOMSON project

c - Electron beam testing

d - FELIN project

e - CMP service

f - computing room

h - SMT PCB tester

Picture 1
1 - 6502 Control section

2 - 6502 Datapath

b - SYCO silicon compiler
1 - GEOPROCESSEUR computer

2 - PASCHLL computer

3 - CANOPUS Distributed system

g - Past computer projects
i - Circuit synthesized by AMICAL.

j - GaAs wafer from CMP.
k - Microelectronics for Physics

I - Micromachining by CMP
I-4 Some data on Grenoble’s environment

Grenoble offers a very good environment in terms of Education, Research, High Tech Activities, Industry.

• Education

Grenoble has been awarded the "European University" title within the University 2,000 Project.

* 40,000 students
* 5,500 foreign students
* 1,500 science degrees awarded each year
* 1,000 engineers graduate each year
* 600 "Erasmus" scholarship students
* 1 International secondary school

• Research

Grenoble is the first French research center in Engineering Sciences, the second in Physics, the third in Mathematics.

* 8,500 researchers (the largest concentration of CNRS researchers in Engineering Sciences after Paris)
* 1,500 foreign researchers
* 250 laboratories
* 5 European research centers:
  - ESRF, European Synchrotron Radiation Facility
  - ILL, Latie Langevin Institute
  - IRAM, Millimetric Radio Astronomy Institute
  - SNCl, National Service for Intense Magnetic Fields
  - EMBL, European Molecular Biology Laboratory

* 4 National research centers
  - CNRS, National Center for Scientific Research
  - CENG, Grenoble Nuclear Research Center
  - CNET, National Center in Telecommunications Research
  - CRSSSA, Research Centre for the Army Health Services

* 1 research center of international proportions acquired every 10 years since 1946

• High tech Activities

* Electronics
  470 industrial companies, 13,250 jobs

* Biomedical technologies
  104 industrial companies, 2,600 jobs

* Imaging technologies
  50 industrial companies, 800 jobs
1 Technopole of 65 ha housing 200 companies and 5,000 jobs (ZIRST Meylan)

**Industry**

* 3,500 companies created each year
* 133 foreign-owned capital companies, employing 25,000 people
* 1 Business District to welcome company headquarters and professional services (EUROPOLE)

**Electronics**

* Education: Engineering schools of INPG and UJF
  - ENSERG
  - ENSIEG
  - ENSPG
  - ENSEEQ

* Research
  Laboratories of CNRS, INPG, UJF
  - ARTEMIS
  - CSI
  - LEMO
  - LEPES
  - LMGP
  - LPCS
  - TIMA

* Infrastructures for research and education
  - CIME
  - CMP

* Applied research
  LETI, a division of the French Atomic Energy Commission (CEA)

  CNFET, a laboratory of France Telecom

**Industry**

SGS Thomson, Thomson Specific Components, Thomson Electronic Tubes, Thomson Consumer Electronics, Thomson LCD, Merlin Gerin, ANACAD, AURIS, Dolphin Integration, SOFRADIR, RADIALL

**History**

43 b. c.: 1st mention of CULARO, a small town modestly built by the Celts to get across the Isère river, by Lucius Munatius Plancus in his correspondence to Ciceron.

III century a. c.: Construction of the first rampart.

379: Emperor Gratian promotes CULARO to the rank of chief town city and gives it its name: GRATIANOPOLIS.
VI century: Construction of a Christian funerary complex on the right bank of the Isère river.

1012: The Saint-Laurent group (right bank) is given to the Benedictine monks of Saint Chaffre en Velay: founding of the Saint-Laurent priory and then, the development of a suburb.

c.1140: Rebuilding of the cathedral and its cloister.

1219: Flood; the bridge is taken away.

1228: Construction of the Collegiate Church Saint André: the "Dauphins" set up their administration at Grenoble.

1339: Creation of a University in Grenoble, including four sections: medicine, liberal arts (sciences and literature), canon law and civic law.

1391 - 1418: Construction of the Island Tower, first Town Hall.

1453: The setting up of the parliament of Grenoble: the town is officially recognised as a regional capital.

1593 - 1606: Construction of the wall of Lesdiguières.

1709: Birth of Jacques DE VAUCANSON, biomechanist. His automata (Le Joueur de Flûte, 1738) were aimed at "reproducing means in view to obtain the experimental intelligence of a biological mechanism".

1712: Birth of Joseph FOURIER, mathematician and prefect of Isère department. In 1811 Joseph FOURIER sets up the Faculty of Sciences. In 1987, the Scientific, Technologic and Medical University of Grenoble will take the name "Université Joseph FOURIER".

1783: Birth of Henri BEYLE, so-called STENDHAL, novelist.

7 June 1783: Day of the "Tuiles".

c. 1830: Construction of the HAXO fortifications.

1869: Invention of the hydro-electric power, the "White Coal", by Aristide BERGES.


1955: Grenoble Nuclear Research Center (CENG).

1963: First laboratory integrated circuit at LETI.

1965: First industrial integrated circuit at SESCOSEM. First computer LAG/INPG-MORS.

1966: Latie Langevin Institute (ILL).

1970: Louis NEEL is Nobel Prize in Physics. Louis NEEL has been President of Institut National Polytechnique de Grenoble (formerly Institut Polytechnique de Grenoble), from 1954 to 1976; he is now Honorary President of INPG.


1985: Nobel Prize awarded to Klaus von Klitzing.

1986: European Synchrotron Radiation Facility (ESRF).

1988: Research Centre for the Army Health Services (CRSSA).

1994: The European Synchrotron Radiation Facility is available to research scientists from virtually all countries.

[Image: Arikido Berges established high-pressure water wells in 1869 and 1881 in order to supply inhabitants manufactured paper pulp in Luxey (near Grenoble). Picture lent by the Museum of the White Dock in Luxey (Pierre Gréat)]
II - RESEARCH ACTIVITIES

II-1 Analogue Test Methods (ATM)

Group Leaders: B. COURTOIS / M. LUBASZEWSKI
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(e-mail for M. Lubaszewski: Marcelo.Lubaszewski@imag.fr)

Members: B. COURTOIS, V. KOLARIK*, M. LUBASZEWSKI**, S. MIR, C. NIELSEN,

Research areas:
This group investigates the testability of analogue and mixed-signal circuits and boards.

Contracts:
European: ARCHIMEDES (ESPRIT-III Basic Research),
AMATIST (ESPRIT-III Basic Research),
NDIMST (ESPRIT/NSF cooperation).

Topics:
This group investigates several advanced topics in testing of analogue and mixed-signal circuits and systems, such as design for on-line/off-line test, built-in self-test, fault-tolerance and test pattern generation.

II-1.1. Unified Testing of Fully Differential Integrated Circuits

Members: V. KOLARIK*, S. MIR, M. LUBASZEWSKI**, C. NIELSEN
and B. COURTOIS

II-1.1.1. Self-Testing and Self-Checking Circuits

The use of fully differential circuits in analogue designs has contributed both to increase the dynamic range and to ease the design. In addition it leads to a first order cancellation of the charge injection offset and capacitance/voltage coefficients. Thus this class of circuits is widely used in high performance designs where the primary issue is the high linearity and/or the signal-to-noise ratio (eg. continuous filters, switched-capacitor filters, A/D converters).

Taking into account that all signals crossing a fully differential linear circuit are symmetrical with respect to the analogue ground (middle of power rails), a balance property is defined. This property is such that:
- the inputs and outputs of every circuit stage belong to the space of common mode signals that do not exceed a given tolerance (right figure 1), and
- the operational amplifier inputs are virtually connected to the analogue ground (left figure 1).

* Now with the Technical University of Brno - Czech Republic.
** Also with the Federal University of Rio Grande do Sul - Brazil.
Figure 1: Fully differential circuit stage (on the left), differential code space (on the right)

Considering the balance property of fully differential circuits and the other properties necessary for self-testing and self-checking circuits, solutions for the following problems are searched:

- the choice of observation nodes to ensure the off-line detection and diagnosis of faults internal to the functional parts of the circuit;
- the choice of input stimuli to ensure the off-line detection and diagnosis of faults affecting the functional circuit and the checker;
- the choice of observation nodes to ensure the on-line detection of faults affecting the behaviour of the functional parts of the circuit; and,
- the design of analogue checkers that do not introduce important performance degradation, that do not result in high surface overheads and that generate error indications compliant with those of digital checkers.

A switched-capacitor biquadratic filter was implemented using the AMS 1.2µm CMOS technology as the means to validate the self-testing and self-checking properties of fully differential circuits. The design includes fault-free copies (with and without checker) and many faulty copies of the filter (all with checker) in order to evaluate both the fault coverage and the performance degradation introduced by our analogue testing strategy. A very small analogue checker was used that is primarily aimed for on-line testing and that results in less than 3% surface overhead. Although the filter design has presented a problem in terms of analogue ground deviation, after some external compensation all the fault simulation results could be obtained in practice by observing the error indicators of the fabricated chips. The checker connection to the biquadratic filter produced a worst case performance degradation of about 2% for the range of normal operation frequencies.

Since our ultimate goal is to ensure through an unified strategy all the tests necessary during the circuit's lifetime, the design of waveform generators for BIST and the possibility of sharing the checkers between the off-line and the on-line testing phases are also investigated.

II-1.1.2. Self-Exercising Analogue Checkers with Absolute and Relative Tolerances

The design of checkers suitable for concurrent error detection in analogue and mixed-signal circuits is addressed. These checkers can on-line test duplicated and differential analogue functional circuits and comply with existing digital self-checking parts.

In order to take into account the imperfections resulting from the implementation of the checking circuitry, we define a coded sampled-signal composed of successive samples. Each sample falls in one of the following regions: code sample, proxy sample and noncode sample. Although a proxy sample is not exact, it is acceptable during a certain time interval before a precise off-line testing or tuning procedure is applied. Since the proxy sample value is close to the correct one, the checker does not go outside the safe operation region.

In general the design of a checker can be based on a comparator replicated in time or in space. We bring in an intermediate solution based on a voltage comparator with a duplicated input stage and a single output stage (see the figure 2). The input signal is first preamplified by two amplifiers with
different offset values $+\varepsilon$ and $-\varepsilon$. The results, $x_1$ and $x_2$, are subtracted and compared with the reference $x_1$. Different implementations were studied. The first one is based on an operational amplifier in an open-loop configuration, and the second one is based on a chain of inverters followed by a latch.

![Diagram](image.png)

**Figure 2**: Window comparator with duplicated input stage

In order to ensure that the first erroneous output of the functional circuit is signalled via the checker (totally self-checking goal), the checker must be designed such that it signals its own faults, or it maps noncode inputs into noncode outputs even when it is affected by undetected faults. In order to achieve this property, we propose that a checker off-line testing phase is integrated into the circuit. This testing phase would periodically apply two noncode samples to the checking circuitry inputs.

The analogue checkers so far considered implement an absolute acceptance window of width $2\varepsilon$. In this case, the deviation accepted for a coded signal is the same for large and for small signal values. While this approach is acceptable for signals that have a small range of amplitudes, it can become too constraining for signals with a larger swing. For large signals, errors would be signalled even for small relative deviations. To avoid this problem, the acceptance window must be made relative to signal amplitude. An important advantage of implementing this new functionality is that error detection can be directly linked to relative deviations of circuit components since it does not depend on signal amplitude. A sample-and-compare checker for testing relative deviations in differential signals and the modifications which are required for implementing its counterpart for duplicated signals have been proposed.

In respect to the checkers based on full duplication and on time replication, the partial space replication employed in our absolute tolerance checkers is a suitable approach for saving silicon surface and for improving the comparison speed. Nevertheless, a lower bound for the window width exists, below which the comparison slows down rapidly. For analogue applications requiring a small voltage swing, an absolute tolerance checker is in general a practical solution. If the analogue circuit has large swings, it may be necessary to move to relative tolerance checkers. In any case, the choice of checker strongly depends on each particular application. Although relative tolerance checkers appear to present advantages with respect to absolute tolerance checkers, it is necessary in practical implementations to provide means of dealing with glitches which can occur for very small signals.

### II-1.2. Analogue Built-In Self-Test


#### II-1.2.1. Frequency-based BIST for Analogue Circuit Testing

Including a programmable frequency generator at the integrated circuit level will greatly simplify the requirements from an external tester during the manufacturing process and facilitate the chip test in the field. Since our off-line analogue circuit testing approach is based on injecting a sinewave signal at the circuit input and observe the circuit output, the relationship between the input and the output

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*Ecole Polytechnique of the University of Montreal - Canada
**Federal University of Rio Grande do Sul - Brazil.
signals is frequency-dependant. Thus the frequency precision of the input test signal is critical to the reliability of the test and must be checked. To validate the oscillation frequency, a frequency-based BIST is needed. Note that this same kind of BIST can be applied to any circuit with frequency variation, for example, a voltage-controlled oscillator, a frequency multiplier, etc.

The goal of this activity is to propose a new technique for testing analogue circuits based on employing an embedded sine-wave generator with a dedicated frequency BIST (f-BIST). Several types of oscillators have been investigated: relaxation oscillators, switched-capacitor oscillators, current conveyor based oscillators, etc. For these many possible implementations, three types of BIST have been investigated.

The first one is an extension of the Translation-BIST, which is based on the frequency conversion to a DC voltage. The second f-BIST that we propose is more digital-oriented and is based on zero-crossing counting. The third approach is based on a fully differential implementation of the oscillator and the check of its balance by means of an analogue checker.

We have carried out some experiments and the results show that every of the three proposed f-BIST approaches fit very well specific low and medium-frequency applications. Research must continue in order to propose a BIST solution for high-frequency circuits.

II-1.2.2. Analogue Built-in Block Observer

Research on digital BIST has led in the past to the proposal of multifunctional structures capable of scanning test data, generating test patterns and compacting test responses. These structures were called Built-In Logic Block Observers and are simply known as BILBOs.

In the realm of analogue circuits, some few works have recently presented isolated structures for either scanning analogue signals, or generating AC-test frequencies, or compacting analogue circuit responses, but not all. In order to recreate the digital BILBO versatility in the analogue domain, a novel multifunctional BIST structure is proposed in this work for use in analogue systems. It is called Analogue Built-in Block Observer and is denoted as ABILBO.

Working principles
The ABILBO structure is based on two analogue integrators. Since the ABILBO operational amplifiers have duplicated input stages, the two ABILBO stages can work as voltage followers and then perform analogue scan operations. Programmable switches can properly interconnect the integrators with few other components, such that either a sine-wave oscillator or a double-integration signature analyser results. The quadrature oscillator can be digitally programmed to generate different signal amplitudes and frequencies. A digital signature can be obtained by computing the time for the analyser output to reach a predefined reference voltage. Both integrators can be reset by shorting their integration capacitors.

Theoretical analysis
The ABILBO time constants, given by the RC characteristic of its integrators, determine the frequency of oscillation in test generation mode, and impact the testing time, the detection of parametric deviations, the valid test stimuli space, and the probability of false rejection in signature analysis mode. It can be shown that the worst-case probability of aliasing in signature compaction mode is given by the worst-case amplitude/frequency output deviation admitted for a fault-free circuit. The coverage of ABILBO faults is dependent on the frequencies used for testing and on the RC characteristic of the integrators.

Experimental results
Because the switched-capacitor (SC) technique is suitable for the integration of analogue circuits and can provide easy programmability of time constants, it was used for illustrating the general idea of a flexible BILBO structure for use in analogue systems. A SC ABILBO was implemented in protoboard and used for testing a low pass filter. Our experiments confirmed the theoretical predictions: a very high coverage was obtained for deviations in the passive components of the filter and faults in the ABILBO structure were also detected.
ABILBO integration at system level

In general, for low complexity circuits, few different test parameters will be required and programming the ABILBO structures will not need much additional hardware. For more complex circuits, where partitioning is required to improve fault coverage and fault diagnosability, the same ABILBOs can be used for testing every resulting subcircuit. In this case, a number of different oscillator frequencies and amplitudes, a number of different signature analyser time constants and direct controllability and observability of internal nodes (via analogue scan) may be required. In case the hardware overhead becomes unaffordable at the circuit level, this analogue test circuitry may be shared by several analogue integrated circuits mounted on the same board. Then the ABILBOs and programming circuitry must be embedded in a board test master circuit.

Since integrators are often found in analogue circuits, the available functional hardware can be shared with the testing circuitry. Then the ABILBO structures, when in functional mode, would be part of the functional circuitry. A typical situation where hardware sharing can be considered is the case of filters based on a cascade of biquads. The cascading of biquads is an usual technique for the design of high order filters. It can be shown that the basic component used for implementing this kind of filter (a programmable biquad cell) can easily accommodate all ABILBO testing capabilities. In this case, the resulting hardware overhead becomes extremely low.

Work Status

We are presently working on the masks for implementation on silicon of the ABILBO structure presented. In future, continuous-time implementations for the ABILBO structure will be searched for their use for high frequency testing investigations.

II-1.3. Design of Reliable Fail-Safe Mixed-Signal Systems

Members: M. LUBASZEWSKI, S. MIR and B. COURTOIS

The general scheme of a mixed-signal integrated circuit designed for unified testing is given in figure 3. For the integration of the off-line and on-line testing at the circuit and board levels, the unification of the boundary scan and the UBIST techniques is considered. This results in the B2UBIST (Boundary scan Board Unified BIST) technique.

The boundary scan architecture can be used to start the off-line test of those UBIST circuits mounted on the board and to perform the off-line test of board interconnects. The on-line test at the circuit level will be carried out by the UBIST technique, while at the board level the propagation of error indicators will be achieved by the boundary scan path connecting all circuits on the board.

Depending on the speed requirements for the application, the propagation/compression of error indicators across the board will be accomplished by cascading them through circuit global checker (figure 4a), or by verifying them simultaneously by means of a specific board checker (figure 4b), or by using a mixed parallel-cascaded architecture. The on-line testing of board interconnects requires the integration of specific checkers at the input interfaces of UBIST circuits and the augmentation of the input and output interfaces in order to accommodate the codes in use.

If analogue checkers of mixed-signal circuits generate digital outputs, then the scheme of figure 3 will fully comply with the approaches for propagation/compression of board error indicators. For the on-line test of analogue interconnects, layout rules must be considered so as to reduce the probability of shorts involving differential nodes.

A solution to overcome the low reliability of self-checking systems can be found in a technique for fault-tolerance. Such a technique should ensure the competitiveness of self-checking systems with regard to their reliability, while preserving their inherent safety. Considering that a self-checking system is capable of signalling its own faults by means of an error indicator, fault tolerance and a continuing mission could be ensured by a duplicated system. Such approach has already been proposed for digital circuits, but remains unexplored for analogue and mixed-signal applications.
II-1.4. Automatic Test Pattern Generation for Linear Analogue Circuits

Members: S. MIR, M. LUBASZEWSKI and B. COURTOIS

This work is concerned with the generation of test patterns for linear analogue circuits. Over the recent years, the growing importance of mixed-signal systems has emphasised the lack of tools which can address the test of the analogue parts. Few works aimed at test generation for analogue circuits have been published until now.
Test Generation Procedure

An analogue test generation procedure is currently under development in the research group. The work has been initially targeted to linear analogue circuits which include both frequency-dependent (e.g. active filter) and frequency-independent (e.g. difference amplifier) circuits.

The transfer function of the linear circuit together with a list of the faults to be analysed and the test measures that can be considered are given to the system. The faults that can be considered include AC hard/soft faults in all circuit components. The system computes the effect of all faults in the test measures.

Next, the procedure automatically selects a minimal set of test measures and a minimal set of frequency tests which guarantee maximum fault coverage and maximal diagnosis for the faults in the fault list. Faults which result in non-linear behaviour of the circuit can also be considered if their effect is frequency-dependent.

Evaluation of the Procedure

Currently, a tool has been produced using the Sicstus Prolog environment for rapid prototyping. The tool has been applied to several self-test approaches which have been used worldwide for analogue circuits. With this, it has been possible to validate the prototype tool at the same time that the potential of the different self-test approaches with respect to both fault detection and fault diagnosis has been evaluated.

As an example, consider the biquadratic filter of figure 5. An input signal \( I \) is filtered by the circuit and the output signal \( Y \) is produced. The case of hard faults (shorts and opens) in all passive components is considered as an example. The circuit is frequency-dependent and therefore most faults are not observable in the whole frequency range.

\[
\begin{align*}
R &= 10K \\
C &= 20nF
\end{align*}
\]

\[ \text{Figure 5 - Example of biquadratic filter} \]

A known method for the self-test of analogue circuits consists on embedding special circuitry which detects deviations of circuit parameters during an off-line test. Examples of these detectors include gain and phase detectors as shown in the example of figure 6. The input \( I \) and output \( Y \) from the circuit of figure 5 are fed to the detectors. The test circuitry compares the gain and phase of the circuit with nominal tolerance values of gain and phase deviations for a given input \( I \).
Figure 6 - Typical off-line test approach

The fault detection and fault diagnosability of these approaches can then be evaluated by means of the ATPG tool developed. TABLE 1(a) shows the results of the test procedure when a gain deviation detector is considered at the output of the circuit. A fault is detected if the gain deviation exceeds in +/- 100 mVolts the nominal value. It can be seen that four frequencies are required to detect all faults and to achieve maximum fault diagnosis with this approach. TABLE 1(b) shows the results when a phase deviation detector is used instead. A fault is detected when the phase deviation exceeds +/- 10 degrees. In this case, one fault is not detectable at all.

<table>
<thead>
<tr>
<th>Frequency test</th>
<th>{130, 339, 2001, 3348}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equivalent faults</td>
<td>{R1o, R2s, R9s, C2s, R5o, C6s, R11o, R13o}</td>
</tr>
<tr>
<td>Undetectable faults</td>
<td>{R5s, C6s, R11s, R13o}</td>
</tr>
<tr>
<td>Threshold</td>
<td>100 mV difference at output Y</td>
</tr>
<tr>
<td>CPU time</td>
<td>14 sec.</td>
</tr>
</tbody>
</table>

(a)

<table>
<thead>
<tr>
<th>Frequency test</th>
<th>{69, 222, 3035, 22325}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equivalent faults</td>
<td>{R1o, R2s, R9s, R5s, C6s, R11o, R13o}</td>
</tr>
<tr>
<td>Undetectable faults</td>
<td>{R1o, R5o, C6s, R11o, R13o}</td>
</tr>
<tr>
<td>Threshold</td>
<td>10 degrees difference at output Y</td>
</tr>
<tr>
<td>CPU time</td>
<td>14 sec.</td>
</tr>
</tbody>
</table>

(b)

TABLE I - Test sets generated:
(a) for gain detector, and
(b) for phase detector
Further work

Further work is still required in a number of directions. First, the system procedure must be improved in order to automatically deal with faults which result in non-linear behaviour and to improve the facilities for specifying test measures. Optimal fault diagnosis is currently not guaranteed if several test measures are considered at the same time. Next, work is required in order to provide a facility which can capture the transfer function of an analogue circuit from the circuit schematics. Further work can also be considered to extend the test generation procedure to automatically cope with sampled circuits. Finally, integration of the tool in a real test environment is the ultimate goal of this work.
II-2 Diagnosis of Complex Systems (DCS)

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Members: A. BIASIZZO*, V. CASTRO ALVES**, F. LEMERY, A. LOPES ANTUNES, W. MAROUFI,
M. MARZOUKI, F. MOHAMED, F. MORGADO DIAS,
F. NOVAK*, A. RIBEIRO ANTUNES**, B. SALLAY, E. SIMEU, M.H. TOUATI

Contracts:
FUTEG (EC - COPERNICUS N. 9624), PROTEUS (French-Slovenian Proteus action N. 95010),
CAPES/COFECUB (French-Brazilian project N. 144/94), Cooperation with SGS-Thomson R&D

Research fields:
Knowledge-Based, Multi-Level and Non-Classic Logic Approaches for System Testing and Diagnosis, Mixed-System Modeling, Analog system diagnosis and simulation, MCM and Partial BS Board Test and Diagnosis, Synthesis for Testability, HW/SW co-design for test.

II-2.1. Summary

The DCS group has started in 1992 its own activities. Research activities of the group deal with new approaches of test and diagnosis of VLSI circuits and electronic systems in general. Starting from 1993, analog and mixed-signal systems have been studied from the modeling and simulation point of view in the one hand, and from the test and diagnosis point of view in the other hand. In 1994, a new activity has been started on synthesis for testability. 1995 has shown major developments on diagnosis and simulation of analog systems, and on synthesis for testability. Activities in mixed-signal behavioral modeling have been completed, as well as activities in test and diagnosis of partial Boundary Scan boards and MCMs. Two PhD theses were defended, in December 1995 (François Lemery) and January 1996 (Mohamed Hédi Touati). Three DBA degrees were obtained (Ana Lopes Antunes, Walid Maroufi and Fernando Morgado). One PhD thesis has been started (W. Maroufi). Starting from December 1995, a new permanent staff member has joined the group (Emmanuel Simeu, Associate Professor with UJF/ISTG Engineering School).

II-2.2. Partial Boundary Scan Boards and MCMs

Members: M. MARZOUKI, F. MOHAMED, F. MORGADO DIAS,
B. SALLAY, M.H. TOUATI

II-2.2.1 Introduction

In this activity, the considered systems are partial boundary scan (BS) boards and multichip modules (MCMs).

The developed methodology allows to unify the test and diagnosis of system components and interconnects. It is based on a scheduling approach to test simultaneously both BS components and non BS clusters, as well as interconnects. Logical stuck-at faults, short and open faults are addressed.

Diagnosis is achieved thanks to a novel approach combining structural description and qualitative reasoning to generate fault candidates. A fuzzy logic-based strategy for best test point finding is used to enhance the diagnosis accuracy and efficiency.

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** Federal University of Rio de Janeiro
This methodology, which can be applied to both MCMs and PCBs, has been implemented in a software named TANDEM, nicely interfaced to commercial ATPGs. Obtained experimental results validate this methodology.

II-2.2.2. Test generation and scheduling

A methodology for the simultaneous testing of non BS clusters and the system interconnects was previously developed. Its characteristics are:

- it identifies the following fault types: (1) faulty cluster circuits, (2) interconnect shorts and opens inside clusters, (3) shorts between clusters, (4) shorts between clusters and full BS parts, (5) interconnect shorts and opens on full BS parts, and (6) faulty BS circuits.
- it unifies the circuit and interconnect test of a cluster, since the testing of a cluster's internal nodes and its outputs usually can only be carried out by means of the activation of the function performed by the cluster circuits.
- whenever feasible, it tests multiple clusters and BS interconnects in parallel in order to avoid inefficient accesses to the board scan path. BS circuits are checked in a later step, since the same accessibility means are necessary for testing clusters and BS interconnects.
- it uses as far as possible the same test sequences for both fault detection and first fault diagnosis processes.
- it applies the same test and diagnosis procedure for board manufacturing, prototype debugging and maintenance.

Developments achieved in 1995 are mainly related to test generation for a given non BS cluster, made up of a number of interconnected non-BS circuits.

It is assumed that the internal structure of these circuits is not necessarily known, the only information required being that a set of test vectors or test sequences is given for each circuit. The test scheduling problem at the cluster level can then be formulated as follows:

Given the knowledge of a set of test vectors or test vector sequences, and their fault coverage with respect to the logical stuck-at fault model for each circuit of the cluster, and given the knowledge of how these circuits are interconnected to form the cluster, the objective is to generate a set of test vector sequences to be applied to the whole cluster in order to ensure both detection of faulty circuits inside a cluster and faults (opens or shorts) on interconnections inside a cluster.

This test scheduling problem at the cluster level can also be seen as a conventional board (only made up of non boundary scan circuits) test scheduling problem. This problem is normally tackled using functional test generation methods. However, the context of boundary scan testing, as well as the fault models that we need to take into account, implies that a structural test generation method must be adopted.

A very simple method has been defined for this purpose. This method is based on a matrix representation of the stuck-at coverage on primary inputs and outputs obtained with the test patterns available for each circuit. Then, with the knowledge of the cluster structure (how the circuits are interconnected), we define for each circuit the constraints on the upstream and downstream circuits to make it observable and controllable, and we can obtain, by combining the matrices, a scheduled test sequence that can test the whole cluster.

This method has been automated and integrated to the whole TANDEM software. Results obtained for combinational clusters with TANDEM have been compared against results obtained with a commercial ATPG (System HILO). To be able to use System HILO in this context, the circuits composing the various clusters have been flattened. TABLE II shows this comparison, for different kinds of clusters made up of interconnected ISCAS'85 benchmarks.

While very powerful for combinational clusters, this method could not give very good results for sequential clusters (made up of circuits interconnected in such a way that feedback loops and memory elements are allowed). A different method, based on a constraint propagation process, has been defined.
TABLE II - Cluster test result comparison pattern generation

II-2.2.3. Diagnosis inside a faulty cluster

The methodology for partial BS system diagnosis encompasses the following steps: first, a preliminary diagnosis is achieved, resulting in the generation of a set of fault candidates among the system modules. These estimations of faultiness are then updated using qualitative information (Qualitative Reasoning Theory); each module of the either combinational or sequential system is given a faultiness estimation, which can be one of the following: {Correct, Likely_Correct, Assumed_Correct, Tending_to_Correct, Ambiguous, Tending_to_Faulty, Assumed_Faulty, Likely_Faulty, Faulty}, depending on the results obtained with different test sessions, and these estimations are then updated according to defined qualitative rules.

Since a high level of ambiguity can remain at the end of this process, the diagnosis accuracy is enhanced using a semi-qualitative approach allowing to identify the best test point to further observe. This approach relies on the fuzzy entropy of the whole system. A cost function is computed for that purpose. This cost function gives a topological evaluation of the importance of each node in the diagnosis process. The approach described in this section has been automated, and has given good experimental results, for both combinational clusters (TABLE III) and sequential ones (TABLE IV).

TABLE III - Diagnosis results for combinational clusters
TABLE IV - Diagnosis results for sequential clusters

In both cases, ISCAS benchmarks have been used as systems, each gate or memory element being considered as a black box component of the system. The discrimination efficiency of the method is calculated as follows: $\text{Eff}=100\times1/N^*\left(N-(k-1)\right)$, where $N$ is the total number of components in the system, and $k$ the rank of the faults site (the faulty component's output) in the list of proposed nodes to observe.

II-2.2.4. The TANDEM Software

The whole test and diagnosis methodology for partial BS boards and MCMs is summarized in figure 7.

![Figure 7 - Test and Diagnosis of partial BS boards and MCMs](image)

This has been implemented in a software named TANDEM (Test ANd Diagnosis Embedded Modules), written in C and running under the Unix system in the X-Window graphic environment. TANDEM is interfaced with commercial tools, through the following supported hardware description languages: GHDL (GenRad Hardware Description Language), VERILOG, VHDL (and BSDL), and
NDL (Netlist Description language, used by Sunrise Test Systems Tools). Figure 8 gives a flavor of TANDEM user interface.

Figure 8 - TANDEM's user interface

II-2.3. Analog and Mixed-Signal Systems

Members: A. BIASIZZO, F. LEMERY, M. MARZOUKI, F. MOHAMED, F. NOVAK, E. SIMEU, M.H. TOUATI

The group also deals with analog and mixed-signal systems, for the purposes of behavioral modelling, simulation, test and diagnosis.

II-2.3.1. Behavioral modeling and simulation

1995 has seen the completion of a set of tools for the CAD of analog and mixed-signal behavioral models. The following tools have been defined, developed and integrated:

- A high-level functional library, composed by mixed-signal models for large systems. It includes several behavioral models described in the HDL-A language. These models have been successfully used for the simulation at different hierarchical levels of an air-bag system.

- A low-level functional library, composed by analog models to be used for op-amp macro-modeling. It has been validated through a new SGS-Thomson design.
- A characterization tool, allowing to measure complex performances of analog circuits, and to rapidly generate their macro-model parameters. This is particularly useful for a whole system validation, after the integration of its different blocks.

- A characterization library (currently limited to op-amps), which contains a set of parameterized measuring procedures, mainly based on test benches and extraction functions. This library is used by the characterization tool.

- A user interface, integrated in the SGS-Thomson CAD framework, which allows the designer to define his own characterization procedures, to be added to the characterization library.

- A set of automatic translators from one behavioral language to another (FAS, MAST, CFAS, HDL-A are considered).

This set of tools have been integrated in a framework (figure 9), and is being used at SGS-Thomson.

**Figure 9 - Analog and Mixed-Signal behavioral modeling environment**

**II-2.3.2 Diagnosis and simulation**

Given the intrinsic complexity of analog systems, specially the continuous values of signals as opposed to discrete one for digital systems, approaches like model-based reasoning and non-classic logic should allow to define and tune notions like the "acceptance window" for different parameter values, thus providing an adequate paradigm for soft fault diagnosis.

After studying and comparing different approaches embedded in different systems, fuzzy logic has appeared as adapted to our purposes. The group has then defined a fuzzy logic based expert system, named FLAMES (A Fuzzy Logic ATMS and Model-based Expert System), principally aiming at diagnosing faulty analog devices. Fuzzy intervals are used instead of crisp ones or fuzzy numbers, in order to overcome the known problems related to analog system diagnosis, mainly imprecision and uncertainty.

FLAMES is made up of the following units (figure 10) :
Figure 10 - FLAMES a global view

- A fuzzy ATMS (FLAMES's kernel) which propagates fuzzy intervals and assumptions
- A database of models which will be used for diagnosis based on the model-based reasoning approach
- A knowledge base made up of fuzzy qualitative rules and component fault models
- A best search strategy unit, that helps finding best test points to probe
- A learning module: the system could use its previous diagnosis to learn from experience
- A general fuzzy decision-making unit added to FLAMES in order to give it the ability to test the functional verification of circuits, to help in the design and in best test strategies

<table>
<thead>
<tr>
<th>$f$/[Hz]</th>
<th>CLP(R) [V]</th>
<th>SPICE [V]</th>
<th>FLAMES [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>(3.5690, 1.0885) 10^{-2}</td>
<td>(3.50935, 1.088039) 10^{-2}</td>
<td>(3.50898, 3.50898, 0.0) 10^{-2}</td>
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<tr>
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<td>(5.89956, -4.702675) 10^{-1}</td>
<td>(5.89707, 5.89707, 0.0) 10^{-1}</td>
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</tr>
</tbody>
</table>

Figure 11 - Comparison between CLP(R), SPICE, and FLAMES
Some units of FLAMES have been developed in the C++ language on Unix workstations, and good experimental results have already been obtained and published on analog diagnosis. These developments have also led to a comparison against a model-based system developed at the Jozef Stefan Institute of Ljubljana, and against SPICE. This comparison shows that FLAMES capability to propagate different kinds of tolerances can be used for the purpose of simulation (figure 11). This comparison has been made on a commercial broad-band filter designed in Slovenia.

II-2.4. Synthesis For Testability

Members: V. CASTRO ALVES, A. LOPES ANTUNES, W. MAROUFI, M. MARZOUKI, A. RIBEIRO ANTUNES, E. SIMEU

II-2.4.1 Global definition of the SFT approach

While test synthesis is the process of automatic generation of a particular test structure, high-level synthesis for testability (SFT) is a much more complex process that can be viewed as the automatic generation of testable architectures, which involves in one hand the choice of the suitable test structures to be allocated, according to a set of constraints dealing with cost and performances, and in the other hand, SFT involves a global test scheduling process. The SFT approach has been defined to be used with the HLS system AMICAL developed by the SLS group.

Given AMICAL steps, and since our objective is to use a systematic approach with as much design and DFT reuse as possible, it appears that our SFT approach should most efficiently interact with the HLS system during the allocation step.

The AMICAL allocation step is then transformed into an allocation for testability step, which encompasses the following phases:

- Functional unit allocation for test
- Trade-off database feeding
- Trade-off decision making
- Top controller testability ensuring
- Additional test structure generation
- Test plan generation
- Test controller synthesis
- Micro-scheduling
- Register placement
- Connection allocation
- Evaluation of the global test architecture

All these phases are then replacing the previous allocation step of the HLS process. After this step, AMICAL normally performs architecture generation. The SFT approach will perform instead a testable architecture generation step, which, in addition to normal architecture generation, includes the two remaining phases:

- Linking the test controller to the test environment
- Generating boundary scan architecture

Some of these steps have already been achieved, and are detailed in the sequel.

II-2.4.2. Case study of synthesis or BIST

During AMICAL synthesis process two target architectures can be chosen: a BUS-based architecture and a MUX-based architecture. The first one normally leads to more compact implementations while the second one is often used when speed is critical. In both architectures the final testable circuit is composed of five main blocks that are described in the following.
II-2.4.3 Synthesis of BS-compliant architecture

We refer here to the synthesis of BS-compliant architectures, i.e. the introduction of BS features at the RT-Level of the design description.

We have designed a tool that takes as input a VHDL description of a circuit at the RT-Level, together with some optional requirements from the designer, and generates as output a BS-compliant circuit described in VHDL at the RT-Level too.

The first part of the tool is a user interface, organized as a hierarchy of menus, which allows to assess the optional BS features required by the designer, and the related information when necessary. These optional features can be the addition of the Test Reset (TRST) pin to the TAP controller, and a list of optional instructions, which could be either the ones proposed in the IEEE 1149.1a version of the standard (IDCODE, USERCODE, RUNBIST, HIGHZ, CLAMP, INTEST), and/or other specific instructions to be defined by the designer (7 ones are allowed in the current version of the tool, in addition to the 3 mandatory ones and the 6 previously listed optional ones).

The second part of the tool achieves the analysis of the input circuit description, in order to generate an internal data structure containing information related to the input and output ports of the original circuit.

The third part of the tool is in charge of the actual BS architecture generation. This is achieved through a parameterized function, which generates the mandatory features of the BS standard (including the TAP itself), together with the instruction registers, data registers, and signals required by the implementation of the optional features, which are the parameters of this function, generated thanks to the user interface.

This tool has been implemented in the C language and runs under UNIX on SUN SparcStations.

II-2.4.4. The Boundary Scan Controller

The interest of designing a Boundary Scan management and control module is not specific to High-Level Synthesis for Testability purposes. Some work has already been done from the early 90s to
- Data-path: during the scheduling, allocation and binding processes, a trade-off between area, performance, test length and fault-coverage is to be performed. This way, depending on the global trade-off and on the available libraries, some FUs will be chosen BISTable while the other will not. In this last case, a general purpose embedded Test Pattern Generator will be in charge of generating and applying test patterns at the FUs inputs.
- Control-Part: as stated previously the control part is implemented as finite state machine. Presently AMICAL generates a transition state table during the scheduling phase, which is later on synthesized.
- On-chip Test Controller: this controller is responsible for the control, sequencing and application of the testing phases.
- Programmable Test Pattern Generator: this unit is responsible for generating test patterns for all FUs and registers.
- Test Response Checker: this unit is responsible for checking the test results of all FUs and registers.

Architectural modification rules have been defined for both Bus-based and Mux-based architectures, together with test access choice rules to select appropriated test points and perform binding, after the additional test resources have been included. Figure 12 and figure 13 show both schematic diagrams that are obtained with both architectures for the data path. The architecture and the necessary signals for the On-chip Test Controller have also been defined.

Figure 12 - Schematic's diagram of BISTed BUS-based architecture
ensure the management and control of BS testing either from an external test equipment or for embedded products, i.e. whole systems of boundary scannable boards with test, diagnosis and maintenance processor included. Some of these products are even commercially available.

However, when replaced in the context of High-Level Synthesis For Testability, it has appeared that what was needed is a more flexible module, which functionalities can be programmable from its simplest form (e.g. a boundary scan controller which only acts as an interface between a boundary scannable device and an external test processor, in charge of serial/parallel and parallel/serial conversion), to its most elaborated form (e.g. generation of TAP signals as well as launching, control and result exploitation of BS test algorithms in different BS modes, either mandatory or optional), without any predetermined choice.

The Boundary Scan Controller (BSC) that has been designed is then made up of two parts, the one dedicated to interfacing tasks between the unit under test (UUT) and the external processor, and the other being a programmable controlling part, in charge of the initialization, launching and control of the BS test algorithms. The main tasks of the interfacing part are the following:

- Parallel to Serial conversion of the data coming from the external processor
- Serial to Parallel conversion of the data coming from the UUT boundary scan chain
- Sending and receiving serial data to and from the UUT BS chain
- Sending the TMS signal to the TAP controller according to the current BS test algorithm
- Sending read and write commands to the processor when needed via the command bus
- Sending interruption signals to the processor when needed
- Sending information on the test completion and results to the processor

The programmable controlling part is in charge of the following tasks:

- Initialization of a BS test sequence, and specification of the UUT BS chain characteristics: number of BS circuits in the chain, size of the instruction registers, size of the data registers, etc.
- Launching of a BS test algorithm (TAP signals and instruction and data registers configuration)
- Control of the execution of a BS test algorithm
- Reading the results of a BS test algorithm

Unlike other boundary scan controller implementations, we have chosen to restrict the role of our BSC, thus it is not in charge of the test pattern generation and test result interpretation tasks themselves: this is left in our case to the processor (or even to the BS circuits when they are self-testable), since, as previously stated, our BSC has been specified to interact with other parts of a whole system, in a HL-SFT or even in a HW/SW co-design for testability context.
II-3 Integrated Systems Design (ISD)

Group Leader : A. GUYOT
(e-mail : Alain.Guyot@imag.fr)

Members : S. ABOU-SAMRA, Z. APANOVIČ*, A. BERNAL NORENA
I. BOUTAMINE, V. COISSARD, L. MONTALVO,
I. MOUSSA, R. PEREZ-RIBAS, A. SKAF,
V. TCHOUMATCHENKO**, A. VACHER

Research areas :

The integrated system design group concentrates on circuit design issues.
It investigates the use of redundant notation in the design of VLSI circuits for high speed or high
precision arithmetic operators.
It explores also the problems posed by new design styles or new technologies.

Contracts :

European : GARDEN (Human Capital and Mobility),
GRASS (Esprit III Working Group).
HIPERLOGIC (ESPRIT Reactive Long Term Research).

II.3.1 On-line functions generator

Members : J.C. BAJARD, J.M MULLER (from LIP, Lyon), A. SKAF, A. GUYOT,

Fast evaluation of polynomials is a major goal in computer science, because most algorithms of
numerical analysis need polynomials and also because any continuous function, including every
elementary function, can be approximated as accurately as desired by a polynomial (theorem due to
Weierstrass). So most of the scientific computers offer some support for evaluation of polynomials by
the Horner's scheme, that means sequentially:

\[ P(x) = \sum_{i=0}^{n} a_i x^i = (((...(...a_n x+a_{n-1})x+a_{n-2})x+...+a_0)x+. ... +a_0) \]

The circuit below uses on-line operators binomers, and takes advantage of their inherent parallelism. A
circuit for exponential, trigonometric and hyperbolic functions with a precision of 32 digits and a delay
of 11 clock cycles has been designed in 1.2μ CMOS.
The CORDIC scheme for elementary functions is very elegant but becomes difficult when redundant
notations, mandatory for on-line operators, are used. Redundant notation leads to the loss of accurate
comparison. This loss must be compensated either in time (more steps) or in area (more operators).
Nevertheless the complex exponential function does not suffer the same problems. A general purpose
elementary functions on-line processor, based on complex exponential, has been designed, processed in
1.2μ CMOS and tested.
Details of the algorithms and circuit design are provided in Ali SKAF's PhD dissertation, defended
September 11, 1995

* Institute of Informatics Systems, Russian Academy of Science, Novosibirsk, Russia
** University of Sofia, Bulgaria
Figure 14: On-line polynomer

Figure 15: On line complex exponential function
II.3.2. **On-line operators for digital signal processing**

*Members: A. Vacher, A. Guyot*

For on-line algorithms, the operands as well as the result flow through the operators serially with a small latency. On-line operators make pipelining possible down to the digit level, thus allowing a high degree of functional parallelism. Besides, serial transmissions relieve the routing problem. The benefits of on-line circuits in the field of digital signal processing have been widely publicised. Chaining on-line operators for a long series of operations may be significantly faster than other approaches. The need for faster Fourier transform on a larger number of samples is paramount among physicists. This research investigates the area/performance ratio of several approaches for multidimensional FFT through simulation or design, namely:

1. Taking advantage of serial operation to adjust the precision during the computation in order to minimize errors.
2. The impact of mixing fully serial (on-line) and parallel-serial operators.
3. The impact of folding or spreading.
4. The utilization of radix-2, radix-4 and radix-8 butterflies.

André Vacher will defend his PhD thesis in June 1996.

![Figure 16: The parallel FFT](image)

II.3.3 **Design of testable operators**

*Members: H. Bederr, M. Nicolaidis from RIS Group, Tima, A. Guyot*

The test of the above mentioned on-line operators is a part of the research of test algorithms for regular structures carried out in the Reliable Integrated System Group of TIMA. It has been shown that due to their low observability and controllability as well as their sequential behaviour, on-line operators like multiplication, division or square root extraction are difficult to test. This study has shown that on-line operators are C-Testable. Two sets of test vectors have been derived: the first set demand a small modification of the operators to increase observability. The second set tests operators without modification, except for the addition of a test state to the simple automaton that controls the operation.

Part of this study was included in Hakim Bederr's PhD thesis, defended November 30, 1994.

This project will continue with the test and design for testability of self-timed operators.
II.3.4. **Fast arithmetic divider**

*Memb: L. MONTALVO, A. SKAF, A. GUYOT*

The speed of computers will always rely on the speed of hardware arithmetic operators. But according to Moore's and Amdahl's laws, more and more transistors can be devoted to a unique function. Some arithmetic operators, like inversion, division, square-root extraction, etc., rely on algorithms that are inherently sequential due to a decision taken on each partial result. Fast implementations are based on carry-propagation-free addition/subtraction. Going to higher-order radices allows to get several quotient bits at a time but in turn leads to a complex decision table and consequently to a long critical path. Mixing the notations (different notations for partial remainder, divisor and quotient) gives more design freedom. The theory of hybrid notation division algorithm has been developed. This theory allows to build dividers by choosing the radix and the redundancy of the quotient and partial remainder digits. Most of the division algorithms currently used are merely particular cases of this theory.

A radix-2, at the same time minimally and maximally redundant, as well as two radix-4, one minimally and the other one maximally redundant have been designed in 1.2\(\mu\), 1.0\(\mu\) and 0.5\(\mu\) full custom CMOS as well as with a technology independent macrocell generator. Experimental results confirm that radix-2 division is faster than radix 4 division but radix-4 division is definitely smaller.

This study has been described in Luis Aníbal MONTALVO's PhD Thesis, defended March 13, 1995

![Figure 17: Hybrid radix-4 divider](image)

II.3.5. **Self timed arithmetic operator**

*Memb: M. RENAUDIN (from CNET), A. GUYOT*

Asynchronous circuits have been investigated at "CNET" in Grenoble through a collaboration with "Telecom Bretagne" for more than three years. The goal of this work is to explore the application of self-timed operators in digital signal processing, in order to obtain lower power dissipation, no clock distribution and fast processing. The collaboration between CNET and TIMA intends to investigate self timed or asynchronous arithmetic operators.
New asynchronous adder structures with high performances and low cost have been designed. The potentialities in terms of speed and complexity of Asynchronous Carry Select Adders, Carry Skip Adders, Carry Look Ahead Adders have been compared. All the structures use DCVS Logic circuitry optimised for speed-power trade-off.

A parallel multiplier-accumulator, devoted to high speed digital signal and video processing has also been designed. It can run at up to 100 MHz and operates in asynchronous or synchronous mode. Last but not least, division and square-root extraction algorithms have to be adapted to a self-timed ring architecture. The layout of the 32 bit self-timed ring divider is presented below in Figure 18. It has been fabricated at the SGS-Thomson Crolles plant, near Grenoble, in three-metal .5 µm CMOS technology (3.3 Volts). It completes a 32-bit division in 105 ns, slightly slower than predicted by simulation.

The design methodology of asynchronous arithmetic circuits was presented in Bachar El HASSAN’s PhD thesis, defended September 26, 1995.

Figure 18 : Self-timed divider-square root extractor

II.3.6. GaAs circuits design methodology

Members : I. MOUSSA, A. GUYOT

This project was started in 1993 when Thomson-TCS established the only European digital GaAs foundry in the suburb of Grenoble. GaAs technology has been for a long time considered as the future state-of-the-art technology for very high speed systems. As compared to silicon, GaAs exhibits higher electron mobility, higher bulk resistivity, higher radiation hardness, wider temperature range and compatibility with optical communications. On the other hand, investment in silicon technology is about three orders of magnitude larger than investment in GaAs technologies.

The project compares the merit of Direct Coupled FET Logic (DCFL) and Source follower DCFL (SDFCL) design styles. Layout techniques are compared and tested through the design of a high speed combinational divider in 0.8µm processed by Thomson TCS in Grenoble. The delay is about 12ns for an 16x16 bits division. Synthesis of GaAs datapath and control part is investigated through the design of an ATM switch module. Very high bandwidth has motivated the choice of high speed technology. The circuit will be processed by Vitesse in 1996. Expected performances are 2.5 Gb/s bandwidth and 300 MHz clock frequency with an 0.6 µm GaAs technology.

Imed MOUSSA will defend his thesis June 10, 1996.
II.3.7. Low-power self-timed GaAs circuits design

Members: R. PEREZ-RIBAS, A. BERNAL NORENA, S. ABOU-SAMRA, A. GUYOT

GaAs digital circuits have clearly a better power-delay performance than silicon circuits. However, the power distribution is quite different from CMOS. In CMOS (Complementary MOSFET), roughly 90% of the power dissipation is dynamic (i.e., due to activity and parasitic capacitances) while in GaAs it is the other way around. Due on one hand to the use of standard Radial Logic and on the other hand to the lack of insulator for the gate of MESFET, roughly 90% of the power is static (independent of the computational activity). Anyway in fast synchronous circuits, whether silicon or gallium arsenide, global clock distribution induces a considerable power dissipation as well as additional delays to compensate the clock skews.

An efficient way to avoid or reduce such troubles is asynchronous design. The absence of global clock signal alleviates timing considerations, eases design migration, provides an automatic adaptation to process parameters and temperature variation and finally gives an average-case instead of a worst case performance.

However the power consumption reduction observed in CMOS asynchronous circuits is not obvious for Gallium Arsenide.

A device level modelling has also been carried out leading to a phenomenological MESFET model. Experiments were carried out on both HGaAs-II (8μ) and HGaAs-III (6μ) technologies (Vitesse Semiconductor) in order to validate and improve this model by accounting for several second order effects such as the DIBL effect or the Schottky gate forward conduction.

This research was started in October 1994.

II.3.8. Operator for unlimited precision

Members: V. COISSARD, J.L. ROCH (from LMC laboratory), A. GUYOT

The computational speed of computers is expected to increase by a factor of 1000 during the present decade. This gives mathematicians the possibility to solve previously intractable problems. But as the number of arithmetic operations increases, so do the probability of potentially disastrous inaccurate results due to roundoff errors and cancellation with the traditional floating point standard (IEEE 754-85). To overcome this problem, extended scientific programming languages has been developed, where high precision arithmetic is simulated in software rather than with a coprocessor.

This project goal is the realisation of a number crunching coprocessor with no truncation nor rounding to support both extended precision and exact arithmetic.
The instruction set of the coprocessor includes the four basic operations plus shift, format conversion and comparison on numbers with up to several hundreds of digits. The hardware also supports housekeeping operations like memory management for variable size numbers and automatic processing of overflow.
This project is a part of the PhD thesis of Vincent Coissard.

II.3.9. Delay and power modelling in arithmetic operation

Members: T. VASSILEVA (Technical University of Sofia), V. TCHOUAMATCHENKO (Technical University of Sofia), A. GUYOT

Fast arithmetic operators in microprocessors or ASIC circuits, specially in the field of digital signal processing, can not always rely on synthesis with standard cell libraries. The delay and power of non-standard logic can be up to two or three times smaller than the standard cell ones. On the other hand, standard cells delay and power dissipation are well characterised and largely independent of the application thus allowing an accurate performance prediction. This modelling is of course missing for non-standard logic.
The goal of this project is twofold. First provide and characterise models for cells dedicated to arithmetic operations, then optimise operators according to the models. The optimization aims at finding a suitable balance between speed, power consumption and silicon area.
This project is a part of the PhD thesis of Vassily Tchoumatchenko.

II.3.10. 3D CMOS design methodology

Members: S. ABOU-SAMRA, B. COURTOIS, A. GUYOT

This project is a REACTIVE LONG TERM RESEARCH project for the Information Technology Program. The name HIPERLOGIC stands for "Thousand MOPS per MilliWatt CMOS High Performance LOGIC".
Objectives and Industrial Relevance: The HIPERLOGIC project proposed is expected to extend the limits of today's best performance/power ratios by a factor of 1000. The HIPERLOGIC project will yield an innovative masterslice chip structure of high functional density. The objectives of high system performance at low power consumption will be achieved due to an innovative silicon-on-insulator CMOS process with three-dimensional integration and a circuit design optimally tuned to this technology.
This project is part of the PhD thesis of Sélim Abou-Samra.

II.3.11. Design portability

Members: Z. APANOVICH and A. MARCHUK from the Russian Academy of Sciences, A. GUYOT

This project addresses the problem of design rule migration for full-chip mask layout. For full chip flat mask layout, ad-hoc decomposition methods become necessary to make possible an efficient utilization of existing methods for small blocks mask layout compaction or extraction-regeneration.
Investigations on this subject started as a result of scientific contacts between TIMA and the Institute of Informatics Systems of the Russian Academy of Sciences (Novosibirsk, Russia) where experiments has been conducted. A chip of about 50 000 transistors was migrated from a Russian 2.0μ 1-metal CMOS technology into a 1.2μ 2-metal CMOS technology and was manufactured in cooperation with CMP at TIMA Laboratory. This experiment has shown that technology migration based on mask layout decomposition resulted into area improvement by a factor of 4 while improvements by scaling was estimated to be closer to 1.5. The main source of area reduction appeared to be within interblock rerouting after macroblock level technology migration. Based on these experiments, a for-staged strategy for solving the problem of full-chip mask layout technology migration was proposed:
- Full-chip mask layout decomposition into macroblock mask layouts with a mask layout of interblock wiring;
- Macroblock level technology migration;
- Symbolisation of interblock wiring, electrophysical analysis of power supply rails and signal nets and their regeneration in the target technology;
- Full chip mask layout regeneration for the target technology.
II-4  MiCroSystems (MCS)

Group Leader: J. M. KARAM
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Members:  M. BAUGE, R. A. BIANCHI, H. BOUTAMINE,
M. DUMITRESCU\(^1\), I. FEDTSHENKO\(^2\),
M. FURMANCZYK\(^3\), R. HAMZA, M. HOLJO,
J. M. KARAM, M. KOORT\(^2\), T. C. NGUYEN, W. OELS,
M. ORLIKOWSKI\(^3\), P. MAERTEN, S. PAQUET,
J. M. PARET, R. MIMOUNE, M. RENČZ\(^4\),
A. RICHARDSON\(^5\), F. V. SANTOS,
F. Van STEENKISTE, T. TROMELIN, R. WISSING,
W. WOJCIAK\(^3\), M. ZUBERT\(^3\)

Research areas:

The research activities of this group address the following:

- the development of micromachining techniques compatible with microelectronics,
- the establishment of a Microsystem CAD strategy consecrated by the development of a set of tools integrated in a design environment allowing continuous design flow,
- safety critical and highly reliable microsystems, particularly operating in medical and aerospace applications.

Contracts:

European: BARMINT (ESPRIT-III Basic Research), THERMINIC (COPERNICUS)
French: MICROMED (GDR Microsystèmes CNRS)

Memberships: NEXUS, NETPACK, ADEMIS

Industrial Partners:

AMS (Austria), ANACAD (France), BS2 (France), MENTOR GRAPHICS (France), SEMILAB
(Hungary), SODERN (France).

Topics:

One of the main obstacles to start with microsystems is the fact that particular, and hence costly processes are needed. In order to get affordable prices and a high flexibility, microsystems should whenever possible be designed in such a way that they can be realised on existing production lines for micro-electronics, with an additional post-processing for micro-system specific 2D and 3D structures, e.g. through Multi-Project-Wafer services. Furthermore, this approach allows to integrate microelectronics, needed in most microsystems, on the same chip. This is the monolithic solution which should be considered as the normal evolution of ASIC-foundries to microsystem-foundries (foundries strategy).

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(1) On leave from Bucharest University, Romania
(2) On leave from Tallinn Technical University, Estonia
(3) On leave from Technical University of Lodz, Poland
(4) Technical University of Budapest, Hungary
(5) Lancaster University, UK
What is happening today with microsystems can be compared with the VLSI evolution during the early 80s, at the time of MEAD-CONWAY. Design rules easy to understand, basic CAD like MAGIC in the US and LUCIE in France, MOSIS in the US and CMP in France, have permitted non-specialists to get acquainted with VLSI. The difference between VLSI in the 80s and Microsystems today is that CAD for Microsystems must not be developed from scratch, but should be built on existing CAD systems. On fabrication, the manufacturing should be built on existing microelectronics manufacturing facilities to take advantage of the existing massive investments.

The MCS group within TIMA Laboratory is involved in the development of fabrication techniques, CAD tools and microsystem design architecture by the wish to make microsystems accessible to non-specialized institutions. The MCS group collaborates extensively with both industry, research laboratories and universities, and emphasis on the ability to work on medium term industrial projects.

II.4.1. Microelectronics compatible manufacturing techniques of Microsystems

Members : M. HOLJO, J. M. KARAM, J. M. PARET

There are two ways to manufacture microsystems: to develop processes specific to microsystems (hence these processes can address requirements specific to microsystems) or to use processes that have been developed for microelectronics. Among those later processes, some can be targeted to microsystems, again to address specific requirements, or it is possible to add special process steps to accommodate microsystems within integrated circuits. This later way will allow to collectively fabricate microsystems including the microelectronics part at a low-cost. This is the way addressed by the MCS group within TIMA.

II.4.1.1. Silicon compatible micromachining

The fabrication of silicon compatible micromechanical structures involves the deposition, doping of the necessary material and the selective etching of the underlying support. Two main methods can be used: bulk micromachining where structures are etched in the substrate, and surface micromachining where the micromechanical layers are formed from layers deposited on the surface.

Some advantages of these micromachining techniques include VLSI integration, low cost and rapid delivery.

Bulk micromachining is a process based on etching wells in the silicon substrate, leaving suspended structures. Using this micromachining technique, devices such as micro-hotplates, infrared sources, thermal flat-panel displays, CMOS thermopiles, thermal converters, gas flow sensors, channels for fibres, and piezoresistive sensors can be developed. In bulk micromachining two techniques can be used: etching from the front-side or etching from the back side.

Works at the MCS group address mostly front-side bulk micromachining. In the back-side bulk micromachining the structures are usually large and alignment is difficult. If the bulk micromachining is performed from the front-side this alignment problem is immediately removed and dimensions can be reduced. The end result after CMOS fabrication is an open in the dioxide and nitride mixture passivation that exposes the bulk silicon surface. These chips are placed into an anisotropic etchant, such as EDP (ethylene diamine-pyrocatechol-water) or TMAH (tetramethylammonium hydroxide) or KOH (potassium hydroxide), and the exposed silicon is anisotropically etched.

The 1.0µ CMOS (SLP / DLM, from ES2) compatible front-side bulk micromachining technique has been fully validated. The design rules have been established, and implemented in CAD environment. This technology has been now transferred to the CMP Service, where the post-processing operation (EDP etching) is subcontracted to ESIEE-Paris. This technology could be illustrated by figure 20 which shows a suspended microbridge with an inverter. The designer is restricted to use thin polysilicon layer, but can use thick glass and metal layers as free standing structural elements.

Designs regrouping mechanical structures, such as bridges, membranes, cantilevers, pixels, and integrated circuits have been fabricated and successfully tested. Figure 21 shows structures that are used to perform piezoresistive sensors, thermopiles, gas sensors, gas flow sensors, thermal based sensors, thermal pixels, resonant sensors, electro-thermal actuators, and others.
Figure 20. Cross-sectional view of the microbridge with an inverter obtained by CMOS compatible front-side bulk micromachining

Figure 21: Structures realized using a 1.0μ CMOS double layer metal technology (DLM) from ES2

The 1.2μ CMOS (DLP / DLM, from AMS) compatible front-side bulk micromachining technique is under validation. This technology offers mixed electronics cell library requested by sensor and actuator interfaces.

Surface micromachining is based on the deposition of thin films on the surface of the wafer and removing one or more of these layers to release the structures. So a surface micromachining process requires a sacrificial layer which is removed at a later stage (in the post-processing operation) to release the mechanical part. Many materials are used as a sacrificial layer, such as: silicon oxide, polysilicon, porous silicon, aluminium, ... each requiring a specific etchant. Usually, silicon dioxide
sacrificial layers are the most used and are removed by wet etching in HF. There are various types of oxide (Thermal, LPCVD [LTO, PSG, BPSG], PECVD) having each advantages and disadvantages in term of quality, etch rate, thickness uniformity etc. The micromechanical layer is normally polysilicon or nitride. Another typical sacrificial layer is polysilicon which has the advantage to be etched by EDP without any supplementary mask. In that case, nitride/ glasses / metals are used to realize the mechanical layer. This the way targeted by the MCS group.

II.4.1.2. Gallium arsenide micromachining

GaAs is for many people regarded as being too difficult and expensive for a sensor or actuator application. It is a fact that GaAs is not cheap in comparison with silicon and also cannot currently be produced with as high purity and few crystalline defects as Si. Therefore, it is preferable to use GaAs where and when one can take advantage of the good properties that it possesses. Possible applications could be where high working-temperature, high frequency, integrated optoelectronics or piezoelectricity are demanded.

As for silicon, Gallium arsenide based microsystems should be manufactured on industrial production lines, with an additional post-processing for microsystem specific structures. Thus, the MCS group investigates micromachining techniques using the Philips Microwave Limeil (PML) HEMT (High Electron Mobility Transistor) and the Vitesse MESFET (METal Schottky Field Effect Transistor) foundry processes.

The use of reverse mesa-shape in the [011] direction makes it possible to create bridges and cantilevers, but it is impossible to fabricate membranes for the same reason. The post-process etch has been performed with phosphoric acid. The resulting suspended structure is depicted in figure 22.

Figure 22. Cross-sectional view of a microbridge with a MESFET using the Vitesse process

Designs regrouping mechanical structures, such as bridges, cantilevers, and integrated circuits have been fabricated and successfully tested using the MESFET process. (figure 23).

Micromachining techniques using the Philips Microwave Limeil (PML) HEMT are under evaluation.
II-4.2 CAD tools for MEMS


Besides foundry facilities, CAD tools are also required to move Microsystems from research prototypes to an industrial market.

In microelectronics, CAD has already attained a highly sophisticated and professional level, where complete fabrication sequences are simulated and the device and system operation is completely tested before manufacturing. In comparison, the art of microsystem design and modelling is still in its infancy. However, at least for the numerical simulation of the operation of single microsystem components, such as mechanical resonators, thermo-elements, elastic diaphragms, reliable simulation tools are available.

For the different engineering disciplines (like electronics, mechanics, optics, etc) a lot of CAD-tools for the design, simulation and verification of specific devices are available, but there is no CAD-environment within which we could perform a (micro-)system simulation due to the different nature of the devices.

In general there are two different approaches to overcome this limitation: the first possibility would be to develop a new framework tailored for microsystem-engineering. The second approach, much more realistic, would be to use the existing CAD-tools which contain the most promising features, and to extend these tools so that they can be used for the simulation and verification of microsystems and of the devices involved. These tools are assembled with libraries in a microsystem design environment allowing a continuous design flow. The approach is driven by the wish to make microsystems accessible to a large community of people, including SMEs and non-specialised academic institutions.

In this area, the MCS group addresses the following developments:
to adapt and extend existing tools for microsystem technology (MST) and make them available as stand-alone tools,
- to develop libraries where models are available in the form of (generic) standard cells described at different levels (symbolic, system/behavioural, layout),
- to assemble tools and libraries in a microsystem design environment allowing a continuous design flow.

The CAD environment considers both monolithic and hybrid solutions, answering hence to the both the SME's strategy (hybrid) as to the foundries strategy (monolithic). While the former considers the present state of the art and thus should be available, the monolithic approach aims the co-fabrication of electronic and non-electronic functions: existing industrial production lines shall be extended and adapted to allow micro-system technology (MST).

The environment allows a continuous design flow which can be seen or considered according to two points of view: the view of a non-specialised system-level designer desiring to create a new microsystem with devices from at least two rather different areas, e.g. micro-mechanical and electronics, and the view of a device designer having expert knowledge on his domain of work, knowledge he would like to make available.

The environment hence contains elements for the device designer, enabling him to design modules, to simulate them, and finally to put the knowledge in the form of characterised standard cells in the library.

The system level user takes profit of this standard cell library that contains multi-level information (e.g. layout information, behavioural models, FEM-models). He assembles the desired cells, and simulates them at system level. Then, the resulting assembly is handed over to a second set of tools, designed for chip level procedures. Once the final layout is produced, both the system level designer and the device level designer can intervene again to check the features of the resulting microsystem.

The figure 24 shows the principle of the design environment allowing a continuous design flow.

Figure 24. The design environment principle
Modelling of microsystems comprises several levels. The MCS group developments address the different levels: layout, process, device and system.

II-4.2.1. The MEMS Design Kit

Currently available CAD tools, such as Cadence DF2 or Mentor Framework, need modifications or extensions before they can be used for the automated design of micromachined devices.

Developments towards a CADENCE OPUS design kit has been achieved to allow the generation of the layout including electronic and non-electronic parts. The kit includes an extended schematic editor allowing the generation of an extended netlist, an extended DRC and an extended parameter extractor (from layout to netlist) distinguishing electronic and non-electronic parts. A netlist is generated allowing an electrical simulation where bridges, cantilevers and membranes are considered as a resistance, and a behavioural simulation where these structures are represented by a model in the language HDLA/ELDO from ANACAD.

The design rules for 1.0μ CMOS compatible front-side bulk micromachining have been defined by the CMP and implemented into CAD environment.

The design rules strictly concerning the conductive layers such as metal and polysilicon, are kept unchanged for the simple reason that their electrical functionality is not altered even on suspended parts.

More difficult to define were the design rules imposed by the properties of the anisotropic etching; three main criteria are consecutive to it:

- getting the open areas by superposition of the four layers: active area, contact, via and passivation opening. Their configuration determines the geometry of the materials constituting the suspended area, and essentially the different silicon oxides surrounding the polysilicon from which are depending several physical characteristics such as solidity of the suspended part, protection of the polysilicon during the anisotropic etching, thermal conductivity (depends on oxide thickness)...  
- relative positioning between open area and conductive layers, transistor layers, etc  
- relative positioning of open areas between themselves, from which depends on course the suspended parts shapes, but more especially the necessary etching time to get them.

These design rules are delivered to designers upon signature of a Confidentiality and Licence Agreement (CLA). Figure 25 shows a design rules example corresponding to the active area layer.

layer : 80.  
name : METAL 1.

<table>
<thead>
<tr>
<th>Rule Number</th>
<th>Parameter</th>
<th>min. dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>M800</td>
<td>METAL 1 stripes inside microstructure areas have to follow all the normal ES2 ECPD10 design rules, and also microstructure area specific rules</td>
<td></td>
</tr>
<tr>
<td>M801</td>
<td>diagonal edges of metal 1 margin to microstructure area</td>
<td>1</td>
</tr>
<tr>
<td>M802</td>
<td>metal 1 can cut a microstructure area border only perpendicularly</td>
<td></td>
</tr>
<tr>
<td>M803</td>
<td>metal 1 spacing to active area</td>
<td>3</td>
</tr>
<tr>
<td>M804</td>
<td>no coincidence between metal 1 and active area</td>
<td></td>
</tr>
<tr>
<td>M805</td>
<td>metal 1 spacing to open contact</td>
<td>3</td>
</tr>
<tr>
<td>M806</td>
<td>no coincidence between metal 1 and open contact</td>
<td></td>
</tr>
<tr>
<td>M807</td>
<td>overlap of poly contact</td>
<td>0.75</td>
</tr>
</tbody>
</table>
The following figure shows a DRC example applied to a microsystem integrating a microstructure as well as electronics.

The microstructure library development is based on the creation of parameterized cells. Indeed, the user must be able to adapt the size of the cell in order to obtain the desired physical properties, without having in mind the problems of post-process etching, spacing between open area masks. Parameterized cells permit to control automatically these secondary features so that the designer only has to specify the essential characteristics.

Figure 26. Example of DRC execution: microstructure rules, electronic rules, and rules relative to spacing between electronics and microstructures are checked in the same time

The library currently contains different parametrized microstructures, among them, cantilevers, membranes and bridges. The following figure shows an instantiation of a parametrized cantilever. The parameter associated to the cantilever structure are:
• l_canti: the length of the suspended cantilever
• w_canti: the width of the suspended cantilever
• poly_to_edge: the distance between the top of polysilicon and the cantilever, important for the piezoresistive response of this layer.
• poly_to_side: the distance between the sides of the polysilicon and the lateral edges of the cantilever to adjust the width of oxide around the polysilicon.
• contact_to_poly: the non suspended part of polysilicon to adjust the margin till the cavity of the etch and to calculate the thermal dissipation of this part of polysilicon.

Figure 27. Instanciation of the cantilever parameter cell

Similar works addressing MENTOR Framework are in progress and will be available through CMP in Q2 96. The following figure shows an instanciation of a bridge using MENTOR Framework.

Figure 28. Instanciation of the bridge parameter cell

11.4.2.2. The anisotropic etching simulator

Since the design kit described above targets particularly monolithic microsystems where the structures are processed together with the electronics, one of the more important factors is the etching time
necessary to liberate the suspended part, because the longer it is, the more the electronics parts risk to be damaged. This time mainly depends on the characteristics of the etchant, the shapes of the open areas constituting the microstructure and their relative positioning; these physical parameters determine the sequence of planes apparition within the silicon substrate, which is to be known in detail if we want to predict the etching time [5]. This tool is complementary to the microsystem design kit. It is based on a geometrical anisotropic etching model, in contrast with the complex atomistic models that require huge data space [6]. The simulator firstly needs the etch rates of the different silicon crystallographic planes, which depend on the exact composition of the chemical agents and their temperature. The following figure shows etch rate diagrams of particular KOH and EDP solutions, in cylindrical coordinates. They represent the etching speed of planes in mm/minute (indicated by graduations) in function of their angle with the (100) plane.

![Figure 29. Etch rate diagrams for silicon relative to KOH 40% (at 50°C) and EDP (at 80°C)](image)

The available program provides a two dimensional simulation: the entry file contains the polygon points representing the surface of the open areas, and the result is a two dimensional view representing, at different time points, the intersection of the limiting planes of the etching front with the (100) plane of the wafer. The number of time points and the etching time have to be specified. The next simulation results correspond to the diagrams of the figure 29. The figure 30 shows a 50 minutes simulation of a cantilever structure etching by EDP. The progressive liberation of the beam is visualized by the limiting planes intersections at five different steps. The first two time points prove the existence of (320) planes during the KOH attack. Figure 31 shows the same structure etched by EDP with 10 time steps represented.

![Figure 30. KOH and EDP anisotropic etching simulations for a cantilever structure](image)
Figure 31. EDP anisotropic etching simulations for micro-bridge (which is not totally etched) and membrane structures. 
Simulated etching times are respectively 120mn and 180 mn.

These simulation results have been confirmed by comparison with the experiments. Their analysis permits to decompose the etching of the validated three microstructures into one phase (cantilever) or two phases (membrane and microbridge). Let us take the example of the microbridge EDP etching: the first phase consists on the etching of (110) planes until merging of the two primitive cavities and formation of convex corners which induce the appearance of (311) facets (second phase). This phase generally lasts longer than the first, this is why the corresponding zones, which consist for micro-bridge of two diagonally opposite rectangles (see figure 31), are called "slowly etched areas". We kept this term within the extended DRC in which the previous analysis has been integrated.

II-4.2.3. Electro-thermal simulation

This simulator has been developed by the Technical University of Budapest (TUB), department of Electron Devices, in cooperation with the MCS group.

One of the greatest challenges of our days in microelectronics are the overheating problems. The increase in the power density in integrated circuits, caused by the actual small feature sizes, moreover the advent of 3D packages cause severe heat dissipation problems.

The proposed simulation tool is based on simultaneous electro-thermal circuit simulation. It has been coupled to Cadence DFII framework. At present, a self-consistent, steady-state electro-thermal simulation can be achieved without any iteration loop according to the following tasks:

- extraction of active (dissipating) regions of the actual design.
- inquiry for information about the estimated chip size (and other details of assembly) needed for the thermal simulation tool,
- calculation of the thermal resistance matrix by THERMANAL, a Fast Fourier Transform based simulator,
- inquiry of the details of the electrical operating conditions needed for circuit simulation,
- netlist generation for circuit simulation. The extracted netlist is combined with the thermal resistance values already extracted,
- circuit simulation by the electro-thermal simulation engine TRANS-TRAN,
- extraction of self-consistent dissipation values from the TRANS-TRAN simulation results,
- calculation of the temperature distribution by THERMANAL, using the dissipation values taken from the self-consistent electro-thermal simulation,
- display of the surface temperature distribution by the means of isotherm contours over the chip layout in Cadence DFII, or by the means of the graphical post-processor of THERMANAL.
II-4.2.4. Optics simulation

In specific applications, microsystems can integrate optical waveguides, optical fibres, or optical devices in which propagation is an essential part. Thus, the modelling of the optical propagation is necessary.

The MCS group started developments towards an optics simulator dedicated to the phenomena occurring in microsystems, particularly addressing specific applications based on micro-optomechanical systems where III-V compounds show advantages over silicon, or other applications where silicon-based microsystems need to be mounted with optical devices.

The software approach is modular - consisting of pre-processors, solvers and post-processors - and offers the flexibility needed for expansion. A Beam Propagation Method (BPM) together with some general Mode Solvers (MS) has been implemented.

In order to be able to analyse the great variety of possible optical structures involved in microsystems structures, a whole method package should be built (containing at least a ray optics approximation tool, a sufficiently general MS, a sufficiently powerful BPM and a Transfer Matrix Method (TMM) tool). This is the aim of this project.

To link the optics simulator with the other tools and thus to ensure a continuous design flow, a library of macrocells should be built. This library would contain optical sources, such as LEDs, laser diodes and optical detectors. These devices will play the role of converters of electrical signals to optical signals and the opposite, and thus represent an interface between the optics simulator and the electrical simulators as it is illustrated in the figure 32.

**Figure 32 - Link between optics and the electrical simulators**

II-4.2.5. Microsystem standard cell library

Automatic synthesis of complete microsystems is not yet possible: digital electronics can be mapped automatically to hardware, analogue and mixed electronics as well as micro-mechanical structures and so on cannot. Therefore, a set of these elements should be made available to the user in the form of (generic) standard cells described both in the form of process-level layout (GDS2/CIF) and in the form of simulation models (HDL-A) as required during the microsystems design phase. These models can be assembled by the user, together with modules he produces himself, either as input for automated synthesis, as specifications for specialists, or as elements just needed at the system-level to show the functionality (e.g. external mechanical elements, functional model of the environment of the microsystem).

Several microsystem models have been developed which includes pressure sensors, magnetic sensors, ISFETs, IR sensors, electro-thermal converters, electro-thermo-pneumatic micropump and humidity sensors. These models have been developed using HDL-A / ELDQ language by ANACAD / MENTOR GRAPHICS.
II-4.3 Microsystem design for safety critical applications


Microsystems technology is having a large impact in a wide range of applications mostly safety critical, like in medical, automotive and aerospace domains. The next generations of microsystems will integrate test strategies and diagnostic functions.

In this domain, the MCS group benefits from the background in test techniques within TIMA laboratory to ensure the migration of available techniques from the VLSI domain to the microsystem domain.

II-4.3.1. Design of the Integrated Electronics for the BARMINT Medical Demonstrator

The BARMINT microsystem consists of several different silicon substrates, forming together a so-called vertically stacked Multi Chip Module (MCM-V). In each substrate one or more different functions is implemented. The distribution of the various functions among the different substrates greatly affects the design of the electrical architecture of the microsystem.

The MCM-V (MultiChip Module, Vertically stacked) concept is a technique that offers the possibility to integrate different kinds of chips, using different kind of technologies, into a single package. An example of a vertically stacked multichip module is given in figure 33. In this multichip module each chip (produced by a certain technology) is sealed on a standard substrate, which can be made of epoxy or silicon. On each substrate a thin metal film interconnection pattern is deposited. These interconnections lead to the edges of the substrate and give the possibility to make vertical connections between the different vertically stacked substrates. The vertical connections have to be made as a last step in the production of the multichip module by electrochemical deposition of a metal and a laser writing technique. To achieve electrical interconnection between the chip and the substrate, several different bonding techniques can be used. In the BARMINT microsystem the wedge bonding technique using gold wires has been chosen.

![Diagram](image)

**Figure 33. Integrating different chips into one package using the MCM-V technique.**

In a MCM-V package the different chip/substrate assemblies are glued on top of one another. After that, the complete system is encapsulated using an epoxy resin as a moulding glue. The encapsulated system is trimmed to a cube with smooth surfaces using a diamond saw. Finally the vertical electrical interconnections are made as described above.

The MCM-V packaging technology gives the opportunity to divide the BARMINT medical demonstrator into subsystems. Each subsystem consists of devices that can be produced with the same technology, so for subsystems a monolithic approach can be used. Afterwards, the different subsystems can be integrated into one package using the MCM concept. According to this principle, the BARMINT microsystem can be divided into the following subsystems:
• micropump module, consisting of a thermopneumatic micropump,
• sensor module, containing different types of microsensors,
• module containing fluid tanks,
• VLSI module for signal processing and external communication,
• module of mechanical tests,
• module of thermal tests,
• power supply module.

Within this project, in addition to the CAD task leadership, the MCS group has developed the complete concept of the electrical architecture for the medical demonstrator (Figure 34 and 35). The temperature, pressure and chemical sensors in the BARMINT microsystem are interfaced by analog signal conditioning circuits that provide current-mode output signals and have programmable characteristics. The current-mode approach for the sensor interfaces has been chosen, because it is perfectly adapted to the selected AD converter for the BARMINT microsystem. Moreover, when developing the concepts for the sensor interface circuits, it became clear that circuits with current-mode output signals offer several advantages when compared to circuits with a voltage output signal. Besides, currents can be easily multiplexed.

The electrical properties of temperature sensors, piezoresistive pressure sensors and ISFET chemical sensors have been investigated. For each type of sensor, an interface has been developed that gives maximal compensation for the non-idealities of the sensor. Besides, the interfaces have been optimized for use in the BARMINT microsystem, which implies the restriction to a CMOS process and a low power consumption. As sensors often have unpredictable specifications, a high degree of flexibility is also required for a sensor interface. In that way, the characteristics can be adapted to the actual specifications of the sensor.

The analog interface circuits for the sensors of the BARMINT microsystem have been equipped with digital control facilities for both addressing and adapting their characteristics. This means that cross-sensitivities, offset and drift can be digitally eliminated, by programming the control inputs of the analog interface. In order to achieve this high degree of flexibility, programmable current mirrors have been implemented in the analog interfaces.

The selected AD conversion technique for the sensor signals of the BARMINT microsystem is based on a sigma-delta oversampling modulator and is current-driven. This type of AD converter has several advantages, which makes it very suitable for sensor applications. Its accuracy is rather independent of component accuracies or process characteristics. Furthermore, as the output signal of the converter is only a semi-digital bitstream, the circuit of the converter can be kept very simple and no communication protocol is necessary. However, a semi-digital bitstream offers the same advantages as a fully digital signal, which includes high immunity to noise and disturbances.

The data acquisition of the sensors, the control of the actuator and the programming of the sensor interfaces is arranged by a common bus configuration. The common bus is controlled by a microcontroller that has to be located in the microsystem. We proposed to minimize the number of data processing tasks, in order to decrease complexity and power consumption of the microcontroller. As the BARMINT microsystem is connected to an external host computer, several data processing tasks can be displaced to this computer.

In order to minimize the number of connections between the different modules of the microsystem, the common bus uses serial communication. Besides, multiplexing techniques have been used on the sensor module to limit the number of AD converters. Each module of the BARMINT microsystem is therefore equipped with address decoders and serial-to-parallel converters.

Since the excessive power consumption of the pump makes complete integration of its driving circuitry unfeasible, we proposed, therefore, an alternative configuration for controlling the micropump.

Besides, additional test functions will be implemented in each sub-module. The high degree of complexity and the physical inaccessibility of the BARMINT microsystem requires the use of automatic test functions and design for testability.
II-4.3.2. Rad-hard read-out electronics for a thermal imaging device

The aim of this activity is to develop the read-out electronics for a thermal imaging device, which will be part of the attitude control platform of a satellite. The sensing element is based on a linear array of thermal detectors, organized as individually addressable pixels. The output signal from each one of these pixels must be measured with a precision of 100mV, over the expected lifetime of the satellite (15 years). This is a difficult problem, considering the hostile environment, subject to large temperature variations and radiation exposure. Our on-going research effort focuses on the development of circuit and layout techniques to limit the degradation caused by ionizing radiation (up to 100Krad) to acceptable levels, using standard bulk CMOS technology. Figure 36 shows the layout of the read-out electronics of the thermal imaging system.

![Figure 36. Layout of the read-out electronics for the thermal imaging system](image)

The immunity to SEEs (single event effects) is also being assessed, and circumvention techniques have been implemented. Ultimately, the objective is to develop a single chip integrating the detector structures (produced by front-side bulk micro-machining) and the read-out circuitry, for space qualification. The development of the rad-hard circuitry is being carried out under contract with SODERN.
II-5 Quality of Complex integrated Systems (QCS)

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Research areas :


Contracts :


Industrial Partners :

Bull (France), CSEM (Switzerland), Dassault (France), European Spatial Agency (Europe), Hydroquebec (Canada), IMD (France), SGS (Switzerland), SGS-Thomson Microelectronics (France), Yuasa (Japan).

Topics :

Because of the increasing complexity of today's industrial products, the design and manufacture of high quality products is becoming a crucial preoccupation of many companies in the world.

Complexity is the combined result of 4 different factors :

1/ The disappearance of traditional boundaries between technological fields such as mechanics, electronics, software and new materials. In a modern product, it is more and more difficult to identify subparts belonging exclusively to a specific technology.

2/ The interdependence of the sub-parts. The integrity of a product and therefore, its long term reliability, can be threatened by another product, much smaller, far less powerful, without any physical connection. This issue is particularly true for EMI/EMC for which an European Directive entitled "Electro-magnetic Compatibility and Interference" (89/336 EEC) was decided in 1989, with a transition period until the end of 1995.

As a result of this situation, the generally accepted law whereby, in order to make a total product of high quality, one only needs to make parts of high quality is no longer true.

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3/ The software integration. In most of the today's products, in addition to managing the hardware, software has become an integral part of the product, with a fundamental difference compared with other technical sub-parts: software is a direct output of the human brain, with no intermediary transformation phases and with a very high risk of conceptual failure. Because writing software is a purely logical exercise, one could consider that there is nothing intrinsically uncertain about it. It is now demonstrated how the process of successive failures of a program can also be considered just as random as that of a hardware device, leading to the idea of a use of a probability-based reliability measure.

4/ The human dependability. Long term reliability is more and more often a parameter also dependent on the environmental use of the product. Nowadays products have to be considered as part of a more complex system, where the user himself and the environment of the product have a fundamental influence on its long term reliability.

QCS team within TIMA Laboratory is fully involved in the development of basic and applied research around the concept of quality of complex integrated systems, by:
- basic research: development of computerized models simulating and predicting the long term reliability of complex systems,
- applied research: development of applications in the area of SMT ATE and Smart Power Card project.

II-5.1 Smart power card

*Topic leader:* L. BALME

*Members:* L. BACIVAROV, L. BALME

The general tendency in microelectronics is to equip systems with their own power supply (primary or secondary battery). This is true for consumer electronics (pocket calculators, cameras and video cameras, walkman, cellular telephones, etc) as well as professional uses (wireless tools, note books for example).

In this type of use, secondary batteries represent a significant improvement, but still insufficient compared with the sophistication of the associated electronics.

The "Accumulateur à Electrolyte Polymère tout solide" technology called ACEP, was discovered by Dr M. ARMAND from the Laboratoire d'Ionique et d'Electrochimie du Solide de Grenoble, a laboratory of INPG-CNRS. It gathers the thin film technology with highly energetic materials and thus allows to create a new generation of all solid miniaturized batteries. This invention opened great new possibilities in various sectors. Smart Power Card is one of these in the field of microelectronics.

Smart Power Card is a portable stand-alone power source device integrating an ACEP battery made of an all solid thin film of conducting polymer, and a control system which pilots battery status indicators and/or data I/O. The same control system can be used for the surveillance of an external device or equipment.

Depending on the microelectronic system powered, Smart Power Card brings innovative solutions to:

II-5.1.1. Secondary batteries for consumer and professional electronics

This market is expecting:
- a highly efficient battery: ACEP
- a physical standard format: the ISO smart card format with connector have been chosen for Smart Power Card,
- a reliable battery giving key informations to the user: charge level, real time consumption and life capital are the 3 parameters shown to the user on micro LCD in the Smart Power Card.

II-5.1.2 Multipurpose smart IC cards as defined by the ISO standards

This fast growing market is expecting an integrated reliable power supply providing energy to IC cards while respecting ISO thickness (0.76 mm). The ACEP thin film technology allows to integrate power on
smart cards and thus opens great new fields of applications, particularly in the management and the surveillance of complex integrated systems.

The Smart Power Card concept is protected by a French patent entitled "Composant d'alimentation du type carte de crédit" deposited in February 1991 and extended (Europe, US, Japan, South Korea, Canada) in co-ownership between INPG and ACEP Inc. (the company owning the exploitation rights of the ACEP battery technology, joint venture between HYDRO-QUEBEC (Canada) and YUASA (Japan).

The feasibility study on Smart Power Card was carried out during 1990, the building of a first prototype using PCB technology was finalized during 1992-1993.

II-5.1.3 Recent developments

- New progresses have been made in 1994 in order to apply SPC concept and architecture to the management and the surveillance of complex integrated systems. The second ultraminiaturized generation of SPC should be finalized by the end of 1996.

- Acceptance of the US patent (US # 07-937.900)

- External event: joint development between INTEL Corp. and DURACELL Inc. of the Smart Battery Data (SBD) and System Management Bus (SMB) specifications which are in line with SPC architecture.

![Figure 37 - SPC internal architecture](image-url)
II-5.2 Automatic test equipment (bare boards (ADELAIDE) and loaded boards (ISMB))

Topic leader: Ch. VAUCHER

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II-5.2.1 - Bare board testing (ADELAIDE)

Introduction

ADELAIDE (ADVanced ELAstomer using Integrated DEvice) is a project dealing with the test of bare printed Circuits boards (PCBs).

More and more, it becomes easier to manufacture a product than to test it. It is true in electronics and especially in bare board manufacturing.

We currently can see a flood of 20 mil pitch components in mass production (New RAM chips). We begin to see 16 mil and 12.5 mil pitch components in small quantities. LCD driver PCB connectors pitch is now industrially 10 mil.

Though, today, bare Printed Circuit Boards (PCB) can not be tested in a reliable and cost effective way under the pitch of 20 mil.

Two dimensions must be considered:
- the technical dimension: it is very difficult to electrically (thus mechanically) access boards when they contain at least one component with less than 20 mil pitch.
- the economical dimension: it is very expensive (when possible) to access boards under 25 mil pitch.

TIMA has developed, in partnership with IMD, several methods to interface in a very reliable and cheap way complex boards with any kind of bare board testers.

Different fields of research were approached:
- ADELAIDE / mirror boards. This has been develop to accurately and reliably access the PCB to be tested.
- ADELAIDE / netlist automatic extractor, to automatically generate the test points list of a PCB, assuming a 100% fault coverage.
- Loaded board testing (ISMB for In Situ Mirror Boards): to access and test loaded boards.
ADELAIDE / Mirror Boards

**Standard Mirror Boards**

In 1988, we started to develop a testing equipment using anisotropic conductive elastomers. The original idea was to build a complete transgrid board of the PCB to be tested. On one side, there was the image of the side to be tested, and on the other side, there were spread test points, easily accessible by a standard bed of nails (the minimum distance between two test points was 50 mil), and, in between, a layer of elastomer, made of micro conductive cylinders, with anisotropic conductivity. The basic concept was successfully tested in a laboratory, but difficult to apply to industrial ATE for the following reasons:

- the use of conductive rubber requires very good planeity and controlled pressure everywhere. This is very difficult to achieve, because of the variable thickness of a PCB, and the warpage.
- the mirror board is long to build, expensive, and therefore not suitable for small and medium range production runs. Furthermore, it is as complex as the PCB to be tested.
- the conductive rubber is expensive and was rapidly damaged.
- there were contact problems with boards using solder resist.

Consequently, we decided to improve the method, considering this experience, and the experience of the standard way of fixturing. We also did not want to change the habits of the PCB manufacturers, because of the level of investment involved.

We decided to split the test points into two categories:
- standard test points, (50 mil minimum pitch)
- complex test points (under 50 mil pitch). One must consider that these points can only be Surface Mounted Test Points (through-hole components have a pitch greater than 50 mil). That is to say that they are organised in standard lines.

Standard test points are easy to reach with a standard bed of nails.

So we thought that if we found a solution that would allow mixing the standard bed of nails fixture and a means of accessing fine pitch lines, it would be the final solution.

We decided to apply the technology of the mirror board to these standard lines. We defined what we call Standard Mirror Boards (or SMBs), as shown in the figure 39 hereafter.

On one side is part of the image of the pads to be accessed. On the other side, we find test pads whose minimum pitch is 50 mil, that is to say easily accessible by standard bed of nail fixtures. Test points are in fact artificially STAGGERED.

The SMB pad's length is very small, and is comparable to the length of the pads to be accessed. Indeed, the contact zone on one Standard Mirror Board needs to be very small (0.1 mm² is enough).

Their thickness is about 20 mil (0.5 mm): regarding the standard travel of a spring probe (used with the bed of nails), 4 mm, we can assume that we can use the same pins as for standard test points.

The SMBs are mounted in a matter of seconds on the TOP plate of the traditional fixture, using a thin epoxy plate, called Support-Card, on which are fixed the SMBs. The Support-Card is drilled in the same operation as the Top plate.

All the disadvantages we found with the complete transgrid board version disappear, keeping their advantages:
- the contact between one SMB and the PCB to be tested is very local (a few mm), thus it is very reliable.
- to access all kinds of PCBs it is only necessary to build a dozen of references (one per pitch). So the SMBs are standard (thus very cheap), and can be ex-stock.
- we only use very little conductive rubber (only where it is necessary), so it is very cost effective.

Further more, the elastomer is protected by spacers, and is not damaged, because always compressed by the same amount.
- SMBs are re-usable on other fixtures.
Furthermore, this technology brings the following new advantages:
- fully compatible with all test systems and traditional fixtures.
- reliable access on very thin pads, up to 4 mil width.
- using inner-component ETP's location --> reducing the problems when 2 components are very close.
- spreading test points allows the use of standard 50 mil pins.
- reducing the number of plates needed.
- artificially increasing the grid density by a factor of 2, because of the spread test point locations, thus avoiding having to buy a double density grid tester.

On a Global Mirror Board, test points can be spread further than on Standard Mirror Boards, for instance in an area where there are only a few test points, therefore eliminating local density problems.

Global Mirror Boards

This is the evolution of Standard Mirror Boards, that has been developed from 1994 on. For extra-high density boards, it is sometimes interesting to use a Global Mirror Board (GMB) instead of Standard Mirror Boards (SMB).

A Global Mirror Board is specific to the Printed Circuit Board (PCB) to be tested. It optimises the concept of the Mirror Board Technology to a dedicated board.
Figure 40 - Global Mirror Board architecture

ADELAIDE / Netlist automatic extractor

Introduction
The aim of this project is to define a custom optimized data-base for bare PCB testing. The work must consider 3 parts:
- test pattern modelling: the modelling is linked to the PCB multi-layer representation;
- test pattern recognition: the recognition is based on image processing algorithms;
- link between image processing and test pattern modelling.

Today's limitations
Nowadays, most CAD and CAM tools accept only the Gerber RS-274 D format. As the Gerber format was created as a means of communicating only graphical information to a photo plotter to produce film, PWB (Printed Wiring Board) test data are usually lost. Theoretically, the solution is to adopt a more suitable data transfer method using for example IPC D 350 or the IPC D 356 specifications.

As we have to test PCBs, we must extract test information from Gerber files. The nowadays utilities can't process Gerber files as well as one would need. To explain why, 2 dimensions must be considered:
- lack of design rules in Gerber format: polygons are filled with a large number of draws. Or only what we need is the polygon outline and a fill code. An other lack in Gerber format is that there is no rules specifying where and when one must use flash command instead of a draw or a sum of draws.
- software limitations: to extract full test data from Gerber files, a software must resolve 2 questions:
  - finding all component footprints (1) since TPs are a part of them: among component footprints, TPs are net-ends only (2);
  - calculating the link between recognised TPs.

NB: (1) copper networks (or nets) aim only to drive current from one footprint to another. (2) One may keep in mind that there is some TPs which are not component pads: in-situ through hole TPs or power plane accesses are some examples.
The standard TP research is based on flashes. Software put a TP everywhere a flash is plotted. In other words, the TP list is the list of all flashes of a Gerber file (excluding thermal and target flashes). The lack of rules has 2 consequences:
- some plots represented by flashes may not be real TPs (vias for example). In this case, we will have more TPs (at least twice or three times more) leading to a more complex and thus more expensive fixture.
- software can not have an exhaustive TP list if some TPs are not represented by flashes. Unfortunately, more than 50% of SMD pads are drawn and not flashed because of their small width or because they are representing net extremities.

The standard Netlist generation is based on vectorial calculations. The algorithm is simple. Assume we want to extract a net. The start point is always a flash. The end point is also a flash. The aim is, thus, to find all flashes which are inter-connected by draws. The algorithm goes from a flash and follows up draws until finding another flash. This tracking must consider all directions encountered. The final database contain the list of network, each network is the sum of flashes and the draws linking them. This algorithm may fail when a net presents only one TP (other TPs are missed) or when drawn areas are complicated (the program loss into polygons during vectorial net tracking).

Image processing techniques for test pattern generation
IMD Test Systems div. and TIMA laboratory challenge to find a new solution to generate a reliable Netlist including a good TP list. This solution needs to be independent from Gerber inefficiencies or any other CAD format.

We had the original idea to convert Gerber files to Bitmap image to avoid its limitations. The idea is pretty well but we have to demonstrate its validity by developing a software. The principle of this software is as follows:
- converting the Gerber file (or CAD file) to a Bitmap image: similar to a display on the screen. This program is easy to build (we need to know the Gerber format only).
- reconverting the Bitmap image to a new CAD file (specific database or Gerber) using image processing and pattern recognition to find out all flashes. We, thus, achieve the task of automatic re-conversion of drawn pads to flashes. The different processes of this vectorization software are: coding, linearisation, pattern recognition, post process.

The coding principle is based on tracking connected image pixels. The first step consists of coding the Bitmap image by the corresponding transition table. The second step consists of connected object (pixels) reconstitution. We scan line by line and search for vertical re-covering. An object is defined as a block of segments (horizontal pixels gathered by proximity) connected one to the other. To optimize the coding we need to define different transitions: simple transition, junction and scission.

To code all the image we can use two methods. The first is based on a one and only scan of the Bitmap image. This method is quicker but requires a lot of RAM memory. The second method is based on several scans. This method is slower but do not require a lot of RAM since we track only one net (object reconstituted by connected segments) at a time (the first method requires to load all unfinished nets on the RAM). Furthermore, tracking net by net gives us the Netlist safely and directly.

![Bitmap image before the first net acquisition](image1.png)

![Bitmap image after the first net acquisition](image2.png)

**Figure 41- Net acquisition on a Bitmap image**
How we can track net by net? The algorithm consists of searching (from the bottom of the Bitmap image for instance) the first black pixel and then tracking connected pixels. Each read pixel is rewrote white on the image. So at the end of the current net acquisition, this net disappears from the Bitmap image (black pixels are reconverted white). We restart the scan from the bottom and so on. The figure 41 shows the image before and after a net acquisition.

As soon as a net is (acquired) into the RAM, it is treated: linearisation and pattern recognition. The linearisation process consists of three steps. The first step is a skeleton extraction of the object. The second step is the linearisation of the pixel list constituting the skeleton. The third step is calculating the width of linear segments. For the skeleton linearisation we chose an algorithm based on Freeman codes. The goal of the pattern recognition is shape and thus TP recognition. Therefore, we must extract geometrical shapes that are within the net coding. The algorithm is based on 2 kinds of process. The first process is a geographical study. The aim of this step is to know the TP specification (net-end or not net-end, primary TP or secondary TP). This process takes advantage of absolute dimension and surface considerations. The second process consists of a pattern recognition to know the exact shape of the TP. Since there is not a big number of pixels to process (first process works as a filter), the process is not very sensitive to the algorithm type.

The post-process is very useful to eliminate redundancies which can happen when extracting TPs. It aims at separating single TP (capacitor or resistance pad, via) from a complex TP among a group of TPs (SMD pads, connector pads...).

**ADELAIDE project status:**
The research and development phase is now finished for ADELAIDE / Mirror boards.
Commercialization is done by IMD, a French company (ZAC de la Fontaine de Jouvene, 8 rue Joly de Bannerville, 91460 Marcoussis, France, Tel.: (33) 1 69 80 93 71, Fax: (33) 1 69 80 93 50).
This product is now used in the USA (Ex: Photocircuits), Europe (SAGEM, EXACTA, EUROTEST, etc...), Taiwan (Taiwan Hong Kong Co), and soon in Japan.
The research and development phase will be finished for ADELAIDE / Netlist Automatic extractor, within next fall, as far as Aadi Benali will be graduated.

**II-5.2.2 - Loaded board testing (ISMB for In Situ Mirror Boards)**

**Introduction**

Loaded boards are traditionally accessed through a "bed of nail", that is to say a fixture where are inserted spring probes, that will contact a dedicated area on the board, called "test point". Each spring probe is wire-wrap and linked to the ATE (cf fig. Traditional fixturing):

![Traditional fixturing](image1)

**Figure 42 - In Situ Mirror Board (ISMB) architecture**

One can find very often several hundred test points on a fixture, each occupying an area of more than 2 mm², that is to say, for a fixture containing 1000 test points, 20 cm² of board surface only dedicated to test!
For some customer, it is still acceptable, but for the other ones, like in automotive industry, mobile phones or computers, where the room available is also a question of feasibility of the product, it is not accepted anymore.

After having developed the Mirror Board concept for bare board testing, it was natural to imagine an application for loaded board testing. Instead of accessing the pads on the bare board, we imagined to directly access the components leads, eliminating the need of adding many test points on the board.

We developed a new version of SMBs, we call ISMB (In Situ Mirror Boards) (cf Fig. ISMB fixture). ISMB are mounted on a dedicated mechanic. ISMB can be use on a fixture in addition to standard test pins.

The first trials we made showed a relative reliability, because of the metal on metal contact: we achieved only several hundreds cycles without any problems. Further, we observed the deposition of metal oxides (lead oxide, etc...), and other materials like solder residues, that lead to bad contacts. We tried to think about a material that would chemically eliminate these residues, and we had the idea to use polymeric materials.

The use of polymeric materials

Research in the last decade has brought to light a new class of polymeric materials with very attractive properties: these materials are able now to combine the electrical conductivity and the mechanical properties of the plastic physical state. From the attractive polymers, polyvinylidine seems to be the most interesting. Polyvinylidine is obtained from oxidation of aniline leading to the emeraldine, the most conductive form. Polyvinylidine can be synthesized chemically or electrochemically. The obtained polymer can be blended with specific olefins to obtain various physico-chemical properties such as plasticity, plasticity and surface acidity.

In addition, electrochemically obtained form leads to electrically-conductive polymer with good adhesion.

Therefore, we patented a method using polymeric materials. We then developed the right polymer material in order to establish reliable contact, with the following properties:
- metallic conductivity
- elasticity
- chemical action (oxide depassivation, etc...)
- industrial deposition

The trials we lead with a big telephone company, showed results that were encouraging, but not satisfying. Nevertheless, a new idea raises from this, and a new patent was taken early December, which has to stay disclosed till next year.

Project status:

On development.

II-5.3 Dependability Analysis of Complex Components and Systems

Topic leader: I. C. BACIVAROV

Members: I.C. BACIVAROV, L.BALME, M. L. SORDAGE

II-5.3.1 Dependability modeling and evaluation of complex systems

The ever-increasing complexity of modern electronic and communication components and systems and the importance of the operating duties they have to accomplish calls for systematic research concerning their dependability (reliability, maintainability, safety) analysis and evaluation, based on an equally important theoretical acquisition.

In order to optimize a complex system from the dependability point of view several of these components must be considered; their importance varies as a function of the system type and functional criticality.
The main objectives of this work are the development of efficient models and algorithms for the computer-aided dependability (especially reliability and safety) analysis of complex, high functional importance systems.

In the first phase of our research two problems were studied, namely:

(a) computer-aided structural analysis (using minimal cut set/tie set approach) for complex systems described by their reliability graph (with application to distributed systems);

(b) computer-aided availability/safety evaluation for systems with renewal, modeled by their fault trees.

Some solutions in order to improve the effectiveness of the Failure Modes and Effects Analysis (FMEA) and the Fault Tree Analysis (FTA) techniques using new approaches, including those based on the artificial intelligence, as well the extension of these techniques for the case of the software systems were also investigated.

1995 Developments

Development of scientific and educational software (computer programs), mainly to support computer-aided quality and dependability training/education on the following topics: Statistical Quality Control (based on MIL-STD 105E; Statistical Process Control; Reliability analysis based on cause-consequence diagrams; Reliability Optimization; Fault Tolerant Electronic Systems (redundant structures) a.o.

II-5.3.2 Reliability testing of semiconductor devices

The risk of failure resulting from the combined effects of high temperature, humidity and electrical bias continues to be important for semiconductor devices and requires testing at these stress factors.

At the same time, the component manufacture must have reliable information on the behaviour of his own products at the kind of stress used for screening.

As a result of our researches, based on the modeling of the physical phenomena involved, design curves at temperature cycling both for screening and qualification testing were obtained for several types of semiconductor devices.

A model for the stress (temperature and voltage) dependence of the semiconductor device reliability was developed taking into account the physical aspects of the failure mechanisms involved; this model is useful for the design of reliability accelerated tests.

We have also investigated the influence of humidity on semiconductor device reliability, with two main purposes: to emphasize the role of humidity in the failure process as a stress factor and to model the reliability - humidity relationship. On this basis an original model, a generalized Arrhenius relation was derived. It is important to mention that this model can be also used for the superposition of many stress factors: thermal cycling, pressure and mechanical stress.

1995 Developments

The researches concerning the reliability of electronic components were extended to the failure mode and mechanisms analysis and to the reliability testing of Surface Mounted Devices (SMD) and focused on the Surface Mounted Electronic Assemblies (SMEA).

II-5.3.3 Reliability prediction based on a synergetic approach

To design the reliability of electronic systems used in such fields as aerospace, defence or transport, one must know accurately the reliability of the involved electronic components. It seems that the usual reliability prediction procedures (e.g. MIL-Hdbk 217) do not supply the necessary prediction accuracy and new procedures are desirable, starting from the failure physics.

Based on our researches, a new methodology was proposed, which could be used: (I) to predict the failure rate of a batch of electronic components at the design phase of the manufacturing process; (II) to
model the influence of the operational stress on the failure rate; (III) to verify the failure rate value with accelerated life tests.

Because a large number of process parameters and stress factors—which are interdependent—are involved, the synergies between these parameters are taken into account.

This new methodology contains three procedures and take into account the synergies existing between the technological factors, the stress factors in an operating environment and the stress factors at the accelerated stress tests, respectively. One main point of this methodology is the assessment of failure-risk coefficients (FRC) based on a fuzzy logic for the potential failure mechanisms.

Basically, this synergetic approach can be used for any product. In the first phase of our researches, this methodology was developed for the semiconductor devices, because the semiconductor device manufacturing process is one of the most complex in today industries. Consequently, the lognormal distribution, known as suitable to describe the failure mechanisms of semiconductor devices was used.

II-5.3.4 Other recent developments

- Coordination of the Special Issue on "Quality Effort in Europe" (L. Balme and I. Bacivarov - Guest Editors) of the international journal "Quality Engineering" (M. Dekker, USA), vol.8, No. 4,- to appear in 1996.
- The new permanent column "European Events in Quality" published by "Quality Engineering" (coordinated by I. Bacivarov, QE Editor for Europe) analysing the scientific (research programmes, conferences, symposia etc), managerial, educational a.o. European events in quality and dependability.
- Coordination of the session "Reliability Prediction" (I Bacivarov, Chair) of the joint International Conference on Probabilistic Safety Assessment and Management (PSAMIII) and European Safety and Reliability Conference (ESREL'96), Crete, Greece.

II-5.4 European programme in quality of complex systems (EPIQCS)

*Topic leader: L. BALME*

*Members*: I. BACIVAROV, L. BALME, J. KAESTLI, M.L. SORDAGE,
C. GUILLERMOU, R. STEFANI

II-5.4.1 - Presentation

In order to cover new industrial needs in the mastering of quality and dependability of complex integrated systems, an original European Post-graduate Programme specified in the Management of Quality in Complex Integrated Systems has been created in 1991, with the collaboration of the Consortium Linking Universities of Science and Technology for Education and Research (CLUSTER) and the European Program COMETT II, by several major Technical Universities and Industrial Groups:

Universities:

**Key Members:**
- Ecole Nationale Supérieure d’Arts et Métiers, Paris, France
- Institut National Polytechnique de Grenoble, France
- Technische Hochschule, Darmstadt, Germany
- Universidad Politecnica, Escuela Tecnica Superior de Ingenieros Industriales, Madrid, Spain.

**Associated Members:**
- University POLYTECHNICA, Bucharest, Romania
- Ecole Nationale de l’Industrie Minérale, Rabat, Morocco.

* List of EPIQCS members only involved in research activity within TIMA Laboratory. Complete list of Steering Committee members and previous research works available upon request from L. BALME.
**Industrial partners:**

Several Industrial Partners, Quality and Professional Associations are involved in the definition of the courses as well as in the management of the Programme:

**Key Members:**
- BULL S.A., Paris, France
- CSEM, Centre Suisse d'Électronique et de Microélectronique S.A., Neuchâtel, Switzerland
- DASSAULT Aviation, Paris, France
- ESA, European Space Agency, Noordwijk, The Netherlands
- Grupo CIAT, Madrid, Spain
- Société Générale de Surveillance, Geneva, Switzerland
- European Foundation for Quality Management (EFQM), Brussels, Belgium
- European Organisation for Quality (EOQ), Bern, Switzerland
- Deutsche Gesellschaft für Qualität, Frankfurt am Main, Germany
- Mouvement Français pour la Qualité, Paris, France
- Conférence des Grandes Écoles, Paris, France.

The CLUSTER organisation is composed of 10 Universities:
- Ecole Polytechnique Fédérale de Lausanne, Switzerland
- Eindhoven University of Technology, The Netherlands
- Imperial College, London, England
- Institut National Polytechnique de Grenoble, France
- Politecnico di Torino, Italy
- Royal Institute of Technology, Stockholm, Sweden
- Technische Universität, Darmstadt, Germany
- Trinity College, Dublin, Ireland
- Universität (TH) Karlsruhe, Germany
- Université Catholique de Louvain-la-Neuve, Belgium.

**II-5.4.2 - EPIQCS objectives and organisation**

EPIQCS is a voluntary, non profit European Association gathering Technical Universities, Business Schools as well as Industries, Service Companies and European & National Quality Associations.

The aims of the association are:

- Issue the European Master's Degree specialised in Quality of Complex Integrated Systems. The European Master's Degree EPIQCS is recognised by the Universities as well as by the Industrial Partners and the Quality Associations, members of EPIQCS Programme.

- Assist any of its members in the evaluation of linguistic and technical skills of candidates to Quality Degrees and Certificates of Competence.

The European Master's Degree specialised in Quality of Complex Integrated Systems is accessible to any individual candidate as well as to candidates presented by Universities, Companies and Quality Associations who fulfil the following requirements:

**A) Initial requirements**

a) Education

Engineer degree, master degree, business school degree or equivalent.

b) Language

Fluent in the language of the country of practice and English.
B) Complementary requirements

a) Common Core Syllabus on Total Quality Management

Candidates must have followed a complementary training devoted to Total Quality Management, composed of at least 200 hours of courses, practical training and case studies and total syllabus having been approved by the EPIQCS Steering Committee.

b) Specialised Options

In the different options offered by EPIQCS, candidates, after having completed the common-core syllabus, must have followed Specialised Courses composed of at least 180 hours of courses, practical training and case studies, and approved by the EPIQCS Steering Committee.

c) Professional Thesis

Finally, candidates must obtain a Professional Thesis which must be situated at the level of graduated studies.

The Professional Thesis must show the ability of the applicant to build an original approach in the resolution of a complex problem belonging to the quality of complex integrated systems.

A large involvement of the Industrial Partners is requested in the management of the Professional Thesis, giving to the work a large feature of application, without sacrificing the fundamental and theoretical basis typical of academic work.

The Professional Thesis must be prepared for a period of at least 9 months, preferentially after completion of the common-core syllabus and the specialised option, under the management of two tutors, one from Industry, one from University, nominated by the Director of the Degree.

C) Issue of the European Master's Degree specialised in Quality of Complex Integrated Systems

On the evidence brought by the candidate that he/she fulfills the above requirements, a Jury composed of at least 3 members of the EPIQCS Steering Committee, 2 of whom belonging to the University issue the Certificate of Competence named: "European Master's Degree specialised in Quality of Complex Integrated Systems", in different options.

II-5.4.3 - EPIQCS results

Until now, EPIQCS has issued 64 degrees, to postgraduate students from Grenoble and Madrid.

The current EPIQCS research works are dealing with the application of ISO 9000 to service industries strongly dependent on their information system, advanced quality assurance modelling in ICs manufacturing, quality assurance in aeronautics CAD-CAM and RAMs modelling applied to service industries.
II-6 Reliable Integrated Systems (RIS)

*Group Leader*: M. NICOLAIDIS  
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*Members*:  M. BOUDJIT, T. CALIN, L. F. COSTA,  
O. KEBICHI, B. MAAREF, M. NICOLAIDIS,  
R. OLIVEIRA-DUARTE, F. VARGAS

Research areas:

This group investigates self-checking circuits, UBISt techniques, BIST techniques, CAD tools for testability, current testing, reliable circuits for space applications, system level test generation.

Contracts:

European:  
JESSI AC6, JESSI AC11, ARCHIMEDES (ESPRIT-III Basic Research), FIDES (ESPRIT-III Basic Research Working Group).

II-6.1. **Self-checking circuits**

*Members*:  M. BOUDJIT, O. KEBICHI, M. NICOLAIDIS, F. VARGAS

Periodic off-line testing of VLSI circuits may be used to ensure hardware failure detection. However, errors produced by hardware faults will remain undetected until the test phase. Also, off-line testing is not effective against transient faults. On the other hand, concurrent error detection techniques are able to detect errors due to both hardware faults and transient faults as and when they occur. Concurrent error detection based on software encoding techniques needs special software development and will significantly decrease the system speed. Alternatively, hardware encoding based on special-designed self-checking circuits may be used. One advantage of self-checking circuits is that they may be designed to cover well known models of hardware faults.

A self-checking block is composed by a functional block which generates encoded outputs and a checker which verifies these outputs. The checker delivers a two output error indication signal (01 and 10 mean correct functioning and the other values mean error detection). The objective of designing self-checking circuits is to achieve the totally self-checking goal, i.e. the first erroneous output of the functional block must signalized by the checker. To ensure this goal, functional blocks and checkers must verify well defined mathematical properties introduced by W. C. Carter and later defined by D. A. Anderson, J. E. Smith and G. Metze have defined the largest class of functional circuits (i.e. strongly fault secure circuits) and, more recently, we have defined the largest class of checkers (i.e. strongly code disjoint checkers) necessary to ensure the TSC goal.

Complex self-checking systems can be designed by assembling several self-checking blocks. In that case a global double-rail checker is used in order to reduce the error indications of the different self-checking blocks into a single error indication.

Several projects are in development in this area concerning the development of new efficient designs of self-checking functional blocks like PLAs, adders, ALUs, RAMs, ROMs, ..., and the development of tools for automatic generation of such circuits.

II-6.1.1. **Implementation techniques and tools for self-checking data paths**

Recent investigations in the group led to the development of low hardware cost TSC data paths. These developments include the carry checking / parity prediction scheme for adders, ALUs, multipliers and dividers and parity prediction for shifters and barrel shifters. Other developments in collaboration with UPC and AT&T Bell Labs, concern the design of fault secure parity prediction
multipliers and dividers, as well as highly reliable low cost parity prediction multipliers and dividers. These schemes allow to implement low cost self-checking data paths, compatible with parity checked memory systems. Thus, the obtained TSC data paths based on parity checking require low extra hardware.

A self-checking data path generator based on these solutions is under development.

II-6.1.3. Synthesis of self-checking multilevel circuits

We believe that this topic is nowadays the most important topic in the area of self-checking circuits. Tools that synthesize low cost multilevel circuits will allow (together with the generators of self-checking data paths) the design of cost effective self-checking VLSI circuits, making these techniques very attractive for industrial use.

PLAs were widely used in the past to automatize the design of VLSI circuits. However, with the development of efficient tools for synthesis of multilevel circuits, PLAs are losing interest. In order to have a complete set of tools that automatize the design of self-checking circuits, we need to develop tools for synthesis of combinational and sequential multilevel self-checking circuits.

Some investigations by a few research groups on this area have already been done. However, the extra hardware required for the synthesized circuits is not low enough to make these first tools attractive for industrial applications.

We believe that there is no single self-checking solution that always leads to the best result. Our objective on this starting project is to develop various tools leading to various self-checking solutions. The tool will try all the solutions for each target circuit and will select the one resulting on the lower hardware cost.

II-6.1.4. Fast output code space computation and self-checking properties verification

A tool allowing fast computation of the output code spaces of embedded blocks in complex self-checking systems has been developed. The output code spaces can be used in order to verify the self-checking properties of embedded functional blocks and checkers. Experiments of output code space computation have been done over a complex system and self-checking properties verification for self-checking PLAs and for Berger code checkers has been performed for a set of Benchmark PLAs.

II-6.1.5. Theory of analog self-checking circuits

This topic analyses the fundamental constraints involved by the implementation of analog/mixed signals functional block and checkers and it shows that the design of TSC or SCD checkers cannot be accomplished. To cope with this problem, a technique based on the concept of self-exercising checkers is proposed and is illustrated in the case of current/voltage checkers and voltage comparators.

II-6.2. Unified BIST (UBIST) techniques

Members: M. BOUDJIT, O. KEBICHI, M. NICOLAIDIS

We have developed a technique allowing to merge self-checking and BIST designs. This technique ensures all tests needed for integrated circuits, e.g. off-line test (design verification, manufacturing, maintenance test) and on-line concurrent error detection.

II-6.2.1. UBIST RAM implementation

Previously we have proposed the bases of the UBIST technique, as well as efficient UBIST implementations for microprocessor sequencing parts.

Our latest development on UBIST addresses RAM blocks. A self-checking RAM implementation is developed. It requires low area overhead and allows to check both the word array and the decoder (usually only the word array is checked). This design is combined with a transparent (i.e. state preserving) BIST implementation. The two implementations are merged according to the UBIST technique.
II-6.3. BIST techniques

Members: O. KEBICHI, B. MAAREF, M. NICOLAIDIS

This project is aimed at developing new BIST techniques and tools for automatic generation of BISTed circuits. In the present phase the project is concentrated on memories.

II-6.3.1. BIST for single-port RAMs

In earlier developments we have proposed an efficient architecture for BISTed RAMs. This work was one of the very first works on RAM BIST. It uses a hierarchical decomposition of the RAM test algorithms and uses a particular block to implement each level of hierarchy. It results in a BIST implementations requiring low area overhead. For a more efficient implementation  we have introduced the design of Up/Down LFSRs. Recently we have developed a tool allowing the automatic generation of BISTed RAMs based on this architecture and implementing the Marinescu's RAM test algorithm.

II-6.3.2. Fault modeling, test patterns and BIST for multi-port RAMs

We have shown that, due to the concurrent writes on several RAM words the standard coupling fault model is not accurate for multiport RAMs.

New fault models (complex couplings and concurrent couplings) have been defined to cope with this problem.

Algorithms allowing to detect all single and multiple complex couplings and concurrent couplings have been developed. The topological reduction of these algorithms has been developed to obtain a $O(n)$ test length.

An efficient BIST architecture has been proposed and an automatic generator of BISTed multiport RAMs has been developed for Thomson (TMS) by using the GDT CAD tools and the CSAM (TMS ASIC compiled function library). This tool uses the test algorithms for multi-port RAMs developed in the group.

II-6.3.3. Transparent BIST for RAMs

RAM transparent BIST allows to test a RAM without destroying its contents. This technique allows to use the BIST circuitry in order to test periodically the RAM in the context of the application execution.

We have developed a technique allowing to transform any RAM test algorithm to a transparent one. We have introduced a symmetric property for RAM fault models and we have shown that if the fault model verifies this property, then, the transparent test algorithms offer the same fault coverage as the standard algorithms. We have shown that all the complete RAM fault models as well as the fault models resulting by topological reduction of the standard models are symmetric. Most of the other known reduced fault models are symmetric, only one of these reduced fault models (proposed by Papachristou) has been discovered not to be symmetric. Thus, for modeled faults, transparent BIST offers the same fault coverage as the standard BIST. However, for unmodeled faults, transparent BIST is superior, since the data background changes at each test phase.

We have proposed a transparent BIST architecture and we have developed a tool allowing automatic generation of transparent BISTed RAMs.

II-6.4. Current testing

Members: F. VARGAS, R. OLIVEIRA-DUARTE, T. CALIN, M. NICOLAIDIS

II-6.4.1. Iddq current computation based on quality requirements

In the literature, Iddq computation supposes that the faulty device resistance value is known. However, it is very difficult to have data concerning this value. Furthermore, it is likely that the
resistance value of faulty devices can take values within a broad range (indeed from zero to infinite). In this work, we consider that the faulty device resistance can take any possible value. Then the computation of the Iddq current is given as following: the designer determines the quality required for the circuit signals (a range of electrical values guaranteeing desired noise margins). Then, our technique determines the reference current for the Built-In Current Sensor (BICS) that allows the detection of any fault which does not meet these requirements. Alternatively, the technique can determine the reference current using as quality parameter the total circuit delay.

A tool for automatic Iddq estimation, QUIEST (QUIescent ESTimation), has been developed. This tool was implemented in C and in SKILL languages, and it was installed in the CADENCE CAD framework. The designer provides as inputs for QUIEST the desired quality parameters in terms of maximum gate output voltage degradation under which the circuit is considered to be good. The implemented tool has a library of Iddq models for the ES2 standard cells available in the CADENCE framework. QUIEST uses HSPICE to simulate these models. At the end of the process, QUIEST provides the minimum Iddq estimated, with respect to the quality parameters provided by the designer, for the circuit in development.

II-6.4.2. On-line current monitoring

When integrated circuits are intended to be used in space, they must provide protection against radiation. Types of radiations like ionization (total-dose), displacement damage, single-event upset (SEU) or soft-error and their effects on electronic systems must be considered. This research project is mainly concerned with the reliability improvement of bulk/epi and SOS/SOI static CMOS circuits with respect to total-dose and in particular, it is also concerned with the reliability improvement of SRAMs with respect to heavy-ion strikes (SEUs):

I) Total-dose: in the past, the design of circuits that are reliable in total-dose environments has been based on fault avoidance techniques (radiation-hardened circuits). Fault detection (the other fundamental technique for designing reliable electronic systems) has not been explored for faults induced by total-dose. In this topic, we propose an approach based on current testing for concurrent checking of these faults in static CMOS circuits. It performs concurrent monitoring of static current by means of Built-In Current Sensors (BICS) and detects the leakage current (Iddq) which accompanies the parametric shifts. In addition to this fundamental benefit, using BICS allows the selection of high-quality circuits during manufacturing testing, resulting in higher mean time to failure.

II) SEUs: conventional techniques use SEU-hardened designs and error detecting and correcting (EDAC) codes for RAMs and memory elements. In this topic, we propose a new technique to improve the reliability of SRAMs used in space radiation environments. This new technique deals with the SRAM power-bus monitoring by using Built-In Current Sensor (BICS) circuits that detect fast transient current in the memory power-bus. This transient current is the result of a single-event upset (SEU) in the memory and it is generated during the inversion of the data stored in the memory cell being upset. The current checking is performed on the SRAM columns and is combined with a single-parity-bit per RAM word, so that abnormal current detection can be followed by error correction.

The techniques described above have also the advantage to perform concurrent checking for permanent faults due to the fabrication process and/or to circuit aging (i.e. bridging faults, gate-oxide shorts, etc.) as well as for soft faults induced by electromagnetic noise. Therefore they are very suitable for designing highly reliable systems.

The proposed techniques have been validated through fabrication and testing of a fault tolerant RAM prototype.

II-6.5. Upset hardened circuits

Members: T. CALIN, M. NICOLAIDIS

This project is concerned with the design of SEU-hardening techniques for latches, flip-flops and memory arrays. Two ways are usually used for hardening circuits: the selection and adoption of the
process (e.g. SOS, SOI) and the design itself. This project is mainly concerned with design
techniques for hardening integrated circuits, process-related issues are only documented.

Existing upset hardened implementations of memory elements in CMOS technology have some
important drawbacks:

- use of extra/expensive manufacturing process steps to implement high resistance elements in the
memory cell. These specific extra steps make the process very expensive. Furthermore, due to
problems related to the RC constants, this technique can be used only for small and medium size
memories.

- use of NMOS or PMOS gates to implement additional storage elements and feedback circuit that
restore the logic state of the upset node. Using NMOS or PMOS latches introduce significant power
dissipation. Thus, the technique can not be used to implement circuits that include an important
number of latches or to implement memory arrays. Also these designs use critically ratioed inverters
to achieve upset immunity. Their characteristics change with statistical process parameters, operating
temperature and radiation total dose, having as effect the reduction of the upset immunity. Finally
these designs are very expensive in silicon area.

The new solutions obtained in this project have none of these drawbacks. They are implemented in
standard CMOS process, they do not require specific size proportioning for the transistors, they have the
same speed and same power dissipation as standard memory cells. The area of the new cells is
twice the area of a standard RAM cell, they can be used to replace the latches of a circuit resulting on
an SEU hardened design. They can also be used as memory cells to built memory arrays of any size,
resulting on low cost SEU hardened single-port or multi-port RAMs.

II.6.6. Fail-safe circuits

Members: L. F. COSTA, M. NICOLAITIS

Fail-safe systems are implemented using a processing part checked using some kind of hardware or
software redundancy and by a fail-safe interface which transforms the outputs of the processing part
into fail-safe signals (i.e. signals which are either correct or safe). Conventionally, the fail-safe
interface is implemented using specific fail-safe discrete components. Such implementations have
high cost and are very cumbersome. This work presents VLSI implementable fail-safe interfaces for
self-checking systems using duplication or other error-detecting code techniques, and for fault tolerant
systems based on triplication. With respect to a scheme that we have proposed in the past, the new
scheme uses concurrent checking techniques instead of periodic testing based on BIST
implementation.

II.6.7. Automatic test pattern generation

Members: M. BOUDJIT, M. NICOLAITIS

II-6.7.1. System level ATPG

This tool starts from a two-level description of the combinational part of the blocks of complex VLSI
systems. An efficient algorithm is used to transform this description to another one named E-group
nonconcurrent two-level circuit description. This description allows concurrency within any group of
product terms having equal outputs. Based on this description, we have developed algorithms
allowing ultra fast backward and forward propagation within complex VLSI systems. Experimental
results over complex systems shown that the tool is drastically more efficient than existing ATPG
tools.

II-6.7.2. Test for path delay faults

This work is done in collaboration with the NCSR Democritos and the University of Athens. In this
work it has been shown that the set of paths of a circuit can be viewed as a vectorial space having
bases with cardinality equal to the total number of gate inputs plus the number of primary outputs minus the number of gates. The delay of any path of the circuit can be computed, by using linear equations over the delays of the paths of any of the existing bases. Thus, only a small number of paths has to be tested, improving drastically the ATPG and the fabrication test process for path delay faults.
II-7 System-Level Synthesis (SLS)

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Research areas:

This group investigates hardware-software co-design, system level modeling, partitioning, communication synthesis, behavioral synthesis based on VHDL and, structured design methodology for high-level synthesis.

Contracts:

JESSI AC 8, AEROSPATIALE, FRANCE TELECOM, SGS-THOMSON, ESPRIT-NSF, DRET.

II-7.1. System level synthesis

The integration of modular and flexible components is becoming a bottle neck when designing modern embarqued electronic systems. For instance, the Airbus A340 includes more than 100 embarqued computers running 20 MB software. In order to master this growing complexity, modular and flexible design methods acting at an early stage of the design process are then essential. Indeed, evidence suggests that most important design decisions are made early in the design process where a poor decision can jeopardise an entire project.

The use of separate tools and methodologies for the design and specification of hardware and software leads to the well-known 90/50 rule. This rule states that 90% of ASICs work first time according to their logic specification. Unfortunately, about 50% of these ASICs need to be reworked because they fail when inserted into their environment. The complexity of today's design and in particular heterogeneous systems implies that global system approaches are essential in order to solve this problem. It is now commonly admitted that most of these failures could be avoided if circuit design was integrated with system design.

II-7.1.1. Hardware-software co-design

The main objective of this work is to develop COSMOS, a co-design methodology and tools aimed at the design and synthesis of complex mixed hardware-software systems. The system design process starts with a system-level specification that may be given in an existing language such as SDL, StateCharts, C, VHDL. Our philosophy is to allow the designer to use one or more of these languages and to translate these descriptions into a common intermediate form, called SOLAR, capable of modeling the main concepts handled by system-level specification languages (concurrency, high-level communication, synchronization and exceptions) and HDL. This intermediate form then acts as an input to the system-level synthesis tools.

As shown in Figure 43, the design process in the COSMOS environment is decomposed into four refinement steps: system-level specification, system-level partitioning, communication synthesis (including channel binding and channel mapping), and architecture generation (including virtual prototyping and architecture mapping).

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All the intermediate models (between system-level specification and C/VHDL) are represented in a design representation called SOLAR. SOLAR is an intermediate form for system-level concepts, which allows several levels of description.

The first step in COSMOS is the translation of the initial description into SOLAR. At this level, a system is represented as a set of communicating processes. The next step in the design flow is partitioning. The goal is to distribute the previous model into a set of communicating modules that will be mapped onto separate processors in the final prototype. This step produces a refined model composed of a set of communicating and heterogeneous processes organized in a graph where the nodes may be either processors or communication units. This step also fixes which technology (hardware or software) will be used for the implementation of each unit. This model needs to be refined in order to fix the communication models. The communication synthesis is composed of two operations. The first one, called channel binding, selects an implementation protocol for each communication unit. The second one, called channel mapping, distributes the protocol among the processors and specific communication controllers. The result is a set of interconnected processes communicating via signals and having the control of the communication distributed among the processes.

The final step is the architecture generation step. It starts with a set of interconnected hardware/software sub-systems (output of communication synthesis) and makes use of two methods in order to produce a prototype. The first method produces a virtual prototype that can be used for simulation. The virtual prototype is an abstract architecture represented by VHDL for the hardware elements and by C for the software. This description is finally mapped onto a multi-processor architecture.

Of course the design process will include lots of feedback loops in order to redesign parts or the full system. At any stage of the design, the user can cancel one or several design steps in order to explore new choices.

II-7.1.2. Multi-paradigm System-level modeling

Members: M. RODHANI, J.M. DAVEAU, G. MARCHIORO, T. BEN ISMAIL

Most of the existing co-design systems are based on a single paradigm or language. Discrete languages such as SDL, Statechart, C, VHDL, C++, are used for the specification of both hardware and software. Experience with formal specification languages has shown that there is no unique universal specification language for all kind applications. The use of specification languages has to be selectively targeted. Some of these languages are more suitable for state-based specification (e.g., SDL or Statechart), some others are more suited for dataflow (Lustre or Signal) while many others are more suitable for algorithmic specifications (e.g. C or ADA). In addition when a large system has to be designed by separate groups, they may have different cultures and expertise with different environments. Therefore, in this project, we are targeting multi-language specification. Thus when designing a complex heterogeneous system, we can use the most suitable format for the specification of each sub-system according to its application field and to the culture of the corresponding designers.

In order to handle multiformat specification we defined SOLAR, a design representation for high level concepts in system synthesis. It is composed of a data representation model and a textual language. Although human readable, SOLAR is not a hardware description language, but an intermediate format only. Solar embodies a series of new concepts which we feel are essential for the next generation of complex hardware systems specification and synthesis. The main motivation behind the development of SOLAR is to link CASE tools and IC CAD tools, thereby allowing mixed hardware/software systems' design and synthesis. The goal is to use this representation for the design of complex systems, and more precisely, a network of communicating systems. In order to achieve these goals SOLAR supports High-Level concepts such as hierarchical and interacting FSMs and high-level communication.
The SOLAR system model is designed to accommodate the properties of all system-level specification languages (SDL, CSP, OCCAM, Esterel, StateCharts, SpecCharts, C, VHDL, etc.) that are relevant to synthesis. Of course, some restrictions on the permissible input will apply in order to have predictable and coherent results. This includes only allowing subsets of the description languages to be used. The objectives of SOLAR are twofold. Firstly, the identification of a basic data-structure that will allow all of the aforementioned requirements to be accommodated. Secondly, the development of system-level synthesis tools, including partitioning and communication synthesis, that will produce a set of interconnected FSMs that may feed existing silicon compilers.

As stated above, SOLAR has been defined to ease the link between CASE tools and IC CAD tools, thereby allowing mixed hardware/software systems' design and synthesis. The next diagram below shows a framework example where such a representation may be useful. Although textual, SOLAR is not intended to be a new specification language. Such languages already exist. For example, the behavior of the hardware may be more easily described in a dedicated HDL such as VHDL. On the other hand, system software specifications can be readily represented in existing languages, such as Esterel, LOTOS and SDL for communication protocols, CSP and OCCAM for concurrent systems, Esterel and StateCharts for real time systems and so on. What SOLAR provides is an intermediate, unifying format for several such languages, that allows mixed hardware/software designs to be represented in a form suitable for their eventual synthesis.
Figure 44: Solar Framework

Where SOLAR differs from other system-level level representations is in its ability to accommodate system-level communication concepts such as communicating protocols, message passing and channels of communication, thereby allowing it to model most communication schemes. The channel model mixes the principles of monitors and message passing, it is known as the remote procedure call model. The channel in SOLAR allows communication between any number of processes.

During the synthesis process, COSMOS uses an external library of ChannelUnits. A ChannelUnit corresponds to either a standard protocol or a customized protocol described by the user. During partitioning and communication synthesis an abstract model of the channel is used. At the architecture mapping step, an implementation of the channel is needed. This implementation may be the result of an early synthesis step using COSMOS or another design method. It may also correspond to an existing architecture.

Results:

A prototype of a SOLAR based environment exists. Interfaces to SDL, StateChart, SAO, C and VHDL have been or are being developed. SOLAR is used for the development of COSMOS.

II-7.1.3. Hardware/Software Partitioning

Members: T. BEN ISMAIL, G. MARCHIORO, M. ROMDHANI

Partitioning can be seen as a mapping of functional sub-systems onto abstract processors. During this step a behavior may be distributed among several abstract processors. Each abstract processor may include several behaviors. A partitioning system may be either automatic or interactive. The partitioning starts with two inputs: a system specification and a library of communication models. The output is a new model composed of a set of processors and a set of communication units. The library may be restricted to predefined models or extended with user defined models.

The partitioning step also determines which technology will be used for the implementation of each processor. For example, a design unit may be implemented in pure hardware, in software running on an operating system or in micro-code adapted for a standard microprocessor. The choice is based on criteria such as execution time, rate of use, re-programmability, re-use of existing components and technology limitation.
Results:

In COSMOS, this step is achieved by a partitioning tool box called PARTIF. PARTIF starts with a set of communicating processes organized in a hierarchical manner and described in SOLAR. Each process represents an extended FSM. Another input to PARTIF is a library of SOLAR communication models. The result of system-level partitioning is a set of communicating and heterogeneous processors organized in a graph where the nodes may be either design units or channel units and where the vertices of the graph may be signals or channel accesses.

PARTIF allows an interactive partitioning by means of five system-level transformations primitives. The first three primitives MOVE, MERGE, and CLUSTER allow the reordering of processes within the hierarchy and the merging of processes to form a single process. The following two primitives are SPLIT and CUT. These allow splitting up one design unit to form inter-dependent design units for distribution purposes.

II-7.1.4. Communication synthesis

Members: J.M. DAVEAU, T. BEN ISMAIL

The objective of communication synthesis is to transform a system containing a set of processes communicating via high-level primitives through channels into a set of interconnected processes communicating via signals and having the control of this communication distributed among the processes. As stated above, this activity may be decomposed into two tasks: channel binding and channel mapping.

The channel binding algorithm is assumed to choose the appropriate set of channel units from the library of communication models to carry out the desired communication. The main function of this step is to assign a communication unit for each communication primitive.

A channel unit, taken from this library, is selected in order to provide the desired services required by the communicating design units. This is similar to the binding/allocation of functional units in classic high-level synthesis tools. The communication between the sub-systems may be executed by one of the schemes (synchronous, asynchronous, serial, parallel, etc.) described in the library. The choice of a given channel unit will not only depend on the communication to be executed but also on the performances required and the implementation technology of the communicating design units. The result of channel binding is an hyper-graph where the edges are either abstract processors or channel unit instances and the vertices correspond to channel accesses.

Results:

A communication synthesis methodology has been developed. It combines both channel selection and interface synthesis (channel mapping).

II-7.1.5: Virtual Prototyping

Members: C. VALDERRAMA, F. NACABAL

A virtual prototype is an executable description of the system implementation. In COSMOS, a virtual prototype is composed of three kinds of modules: Software modules in C, Hardware (HW) modules in VHDL, and communication components that may be described in C or in VHDL.

The goal of this work is the definition of a joint environment co-synthesis and co-simulation. This poses the following challenges:
1- communication between the HW and SW modules,
2- coherence between the results of co-simulation and co-synthesis and
3- support for multiple platforms aimed at co-simulation and co-synthesis.
In COSMOS, virtual prototyping corresponds to the translation of SOLAR into executable code (VHDL and/or C). Each sub-system is translated independently. The output of virtual prototyping is an heterogeneous architecture represented by VHDL for the hardware elements (virtual hardware processors), C for the software elements (virtual software processors), and communication controllers (library components).

Results:

* Development of C-VHDL co-simulation tool and methodology called VCI.
  
  VCI HAS BEEN TRANSFERRED TO SGS-THOMSON WHERE IT IS BEEING
  PRODUCTISED AND USED BY SEVERAL DIVISIONS IN GRENOBLE AND
  BRISTOL.

* Development of S2CV, a tool for C, VHDL generation from SOLAR.

II-7.1.6. Prototyping

  Members: A. CHANGUEL, M. ROMDHANI

Prototyping is the mapping of a virtual prototype onto an architecture that implements the specification. The architecture mapping may be achieved using standard code generators to transform software parts into assembler code and hardware synthesis tools in order to translate hardware parts into ASICs or virtual hardware processors (emulators). The result is an architecture composed of hardware components, software components and communication components.

COSMOS uses a modular and flexible architectural model. The general model is composed of three kinds of components: (1) Software components, (2) Hardware components, and (3) communication components. This model serves as a platform onto which a mixed hardware/software system is mapped.

Communication modules come from a channel unit library, they correspond to existing communication models that may be as simple as handshake or as complex as a layered network. For example, a communication controller may correspond to an existing interface circuit, an ASIC or some micro-code executing on a dedicated microprocessor.

The proposed architecture model is general enough to represent a large class of existing hardware/software platforms. It allows different implementations of mixed hardware/software systems. A typical architecture will be composed of hardware modules, software modules, and communication modules linked with buses.

Results:

Several application examples are experienced using this model. This includes an 18 motor adaptative control system and a demonstrator for AEROSPATIALE.

II-7.2. Architectural synthesis based on VHDL

A lot of work has already been carried out in the domain of behavioral synthesis. Most known scheduling and allocation techniques have been applied in high level synthesis. Although behavioral silicon compilation has achieved large steps towards the automatization of VLSI design, very few systems are currently being used in industry. One of the main problems has been the lack of integration within existing design methodologies and environments.

The goal of this work is to develop AMICAL, a behavioral synthesis tool that combines behavioral synthesis with methodologies allowing design re-use. AMICAL is based on pragmatic concepts allowing:

1- a close interaction with the designer
2- to handle complex and heterogeneous design through hierarchical design and design re-use
3- an easy integration within CAD environments and design methodologies.
Starting with a pure VHDL input, AMICAL produces a full specification for existing logic and RTL synthesis tools.

Classical synthesis systems usually run in an almost automatic push-button manner, therefore their performances lie on the algorithms implemented. The designer has little freedom in orienting the result. Moreover existing behavioral synthesis tools usually restrict the functional unit concept to modules executing predefined operations of the initial behavioral specification. This kind of push-button behavioral compiler that restricts component to predefined arithmetic and logic operators is convenient for narrow application domain (e.g. regular DSP operators such as filters), but suits less for non regular designs such as complex ASICs that make use of existing designs such as memories with complex protocols, I/O units or more generally complex sub-systems. What is really needed for the design of complex ASICs starting from behavioral description is an interactive environment allowing the user to refine his design through an iterative design process.

AMICAL gets around these limitations of classical behavioral compilers. In addition to a pure automatic execution mode, it allows interactivity. Moreover AMICAL brings a generalisation of the concept of functional unit leading to the use of co-processors as functional units. When using AMICAL for the synthesis of complex design, we found this approach very practical. It allows non experienced designers to perform quick synthesis through an automatic design flow. On the other hand, it allows experienced designers to exploit personal knowledge, by mixing manual and automatic execution, the architect can reach a solution close to the one he expects. Another advantage of AMICAL is that it enables hierarchical design through component re-use.

The AMICAL design-flow is illustrated by the figure 45. The two kinds of information required for synthesis are a behavioural specification and a functional unit library. AMICAL then generates a register transfer level (RTL) description that can feed existing RTL and logic synthesis and simulation tools.

The behavioural description model allows to handle very large designs based on hierarchical specification. The basic idea behind this model is that a complex system is generally composed of a set of sub-systems performing specific tasks. A high-level specification of such a system needs only to describe the sequencing of these tasks, consequently the coordination of the different sub-systems. Each sub-system is modelled as a functional module designed (or selected) to perform a set of specific operations. Therefore the behavioural specification may be seen as a coordination of the activities of the different sub-systems. The decomposition of a system specification into a global control and detailed tasks allows to handle very complex design through hierarchy.

AMICAL is based on a flexible architecture model allowing hierarchy and design re-use. The target architecture of AMICAL is composed of a top controller, a set of functional units and a communication network. These last two constitute the data-path. The communication network is composed of buses, multiplexers and registers. The network is built in order to allow the communication between functional units, and with the external world. The number of buses and multiplexers is fixed according to the parallel transfers required by the architecture.

The behavioural description is given as a standard VHDL file following a specific style. The use of complex sub-systems is made through procedure and function calls. For each procedure or function used, the library must include at least one functional unit able to execute the corresponding operation. In figure 45, the VHDL description makes call to a DCT function and uses a memory with a complex protocol (mread, mwrite). The library includes a memory, an ALU, and a DSP processor able to execute these operations. Of course, for each operation we may have several modules able to execute it. The system will select automatically the best solution. During the different steps involved in the behavioural synthesis, the functional units are used as black boxes. These may correspond to already designed complex systems. The different steps involved in the synthesis process are: scheduling, allocation and architecture generation.
Results:

The behavioural synthesis system AMICAL is pragmatic and seems to correspond to designers' needs. The most important feature of AMICAL is the fact that it combines traditional behavioural level synthesis algorithms with the ability to allow designer intervention at almost any stage of the synthesis process. The use of powerful architecture allows AMICAL to handle complex design. Several large examples, including the MPEG-AUDIO decoder, an answering machine and a PID have also been used for AMICAL evaluation. The PID circuit makes use of several complex operators including a fixed point unit that have been compiled with AMICAL itself. More recently two very large designs have been achieved using AMICAL. A motion estimator for an MPEG2 video decoder has been designed in cooperation with SGS-Thomson. This design makes use of two memory units with sophisticated protocols, of a DSP processor designed by CATHEDRAL and of 2 clocks of different frequencies. The other design is an adaptable speed controller aimed to drive up to 18 motors. The design makes use of a fuzzy logic model to implement the adaptive control. These experiments have shown that the use of AMICAL allows an increase of productivity by a factor of 5 to 10.

II-7.2.1. Scheduling and Optimization for the Synthesis of Control Flow Dominated Design

Member: M. RAHMOUNI

Scheduling is one of the central tasks in high level synthesis, it consists on partitioning the design behavior into control steps such that all operations in a control step execute in clock cycle. We consider the problem of scheduling descriptions represented by control flow graphs.

Path-based scheduling algorithms (PBS) have proved themselves to be much more efficient than classical approaches when dealing with descriptions of control-low dominated circuits. The first application of PBS to synthesis was made by Camposano and was based on algorithms first proposed for microcode compaction.

Results:

Around PBS, we have developed two heuristics named Dynamic Loop Scheduling (DLS), and Pipeline Path-based Scheduling (PPS). DLS comes to reduce the complexity of PBS which is exponential, by resolving the problem of path explosion by cutting the path on the fly. PPS concentrates on optimizing the execution of loops. In real time applications, loops are the most time critical part. PPS uses a new technique for pipelining loops in order to identify any parallelism that may exist beyond loop boundaries.
II-7.2.2. Interactive behavioral synthesis

Member: H. DING, W. CESARIO, P. KISSION

The goal of this work is to make behavioral synthesis flexible and practical for architecture exploration.

AMICAL is organized as an interactive environment with the ability to allow designer intervention at almost any stage of the synthesis process. The designer can simultaneously view both the control section and the data-path as well as their inter-relation. For each synthesis step, the designer can choose between automatic, manual or step-by-step execution. If either of the latter two modes is selected, AMICAL verifies that all modifications comply with a set of rules corresponding to the particular synthesis task. AMICAL also generates a statistical evaluation of each design configuration. In addition, all of the synthesis steps are performed in real-time making the system truly interactive. The combination of automatic and manual synthesis allows a quick and broad exploration of the design space in real time.

Additionally the user can select between several architectural styles for the data-path (Bus-based, Mux-based), for the controller (Mixed FSM, programmable controller) and for synchronization (different pipelining scheme).

Results:

A full interactive synthesis environment has been developed. It is being used for the design of industrial complex CMOS circuits.

II-7.2.3. Linking behavioral synthesis with existing CAD environments

Member: V. VIJAYA RAGHAVAN, R. PISTORIUS, P. KISSION

The goal of this work is to define methods and tools in order to ease the link between AMICAL and existing CAD environments. This work addresses three tasks:

* Mixing synthesizable and non synthesizable specification. This is made through a powerful programmable personalisation method allowing to combine the output of AMICAL with the non synthesizable parts of the design.

* Pre-Floor planning: Decomposition of the output of AMICAL into regular datapaths and suited for data-path compilers and control blocks suited for logic synthesis.

* Libraries: A library of abstract components is used. End user libraries are supported for both fixed and generic components which may correspond to mega-cores.

Results:

This work constitutes the back-end of AMICAL. Several tools have already been developed and used for the synthesis of real-life designs.

II-7.2.4. Behavioral synthesis for structured design methods and design re-use

Member: P. KISSION, E. BERREBI

In order to cope with designs of increasing size and complexity, it is then clear that we need improvements of the design quality and designers' productivity. This may be achieved in two ways that can be combined:

1) Using more structured design methodologies for an extensive re-use of existing components and sub-systems. It seems that 70% of new designs correspond to existing components that cannot be reused because of a lack of methodologies and tools.
-2) Providing higher level design tools allowing to start from a higher level of abstraction. After the success and the widespread acceptance of logic and RTL synthesis, the next step is behavioural synthesis, commonly called architectural or high-level synthesis.

The goal of this work is to combine structured design methodology and AMICAL in order to design complex heterogeneous systems.

![Diagram of structured design methodology]

**Figure 46 - Use of structured design methodology for high-level synthesis**

Structured design methodology allows to handle very complex design with hierarchical approach. Hierarchical design proceeds by partitioning a system into modules. The implementation details of these modules are hidden. Proper partitioning allows independence between the design of the different parts. The decomposition is generally guided by structuring rules aimed to hide local design decisions, such that only the interface of each module is visible.

The main steps involved in structured design methodology for high-level design are shown by figure 46. They include a system-level analysis and partitioning step and a high-level design step. The system-level analysis and partitioning step starts with the high-level specification; its aim is:

1) To structure the design in order to produce a hierarchical decomposition of the initial specification. This leads to the isolation of sub-systems that will be designed independently as well as that of sub-functions that will be executed on specific functional units.

2) To select the components to be used; these may either be standard existing functional units or specific modules that have to be designed.

These two aspects are inter-related. The hierarchical decomposition may be influenced by the set of already existing components. On the other side, the selection of the components is influenced by the hierarchical decomposition of the design.

**Results:**
This methodology has been used successfully for the design of several large examples.

II-7.2.5. Methodology for the design of complex and heterogeneous design using behavioral synthesis

Members: E. BERREBI, P. KISSION, J. FREHEL

The design of complex modules such as an integrated system on chip may need the use of different behavioral synthesis tools corresponding to the different functions implemented by the system. Complex and intensive data computation may need throughput oriented synthesis tools such as cathedral whereas the design of complex control function is made using AMICAL. Of course the system may include blocks described at the RTL and netlist level.

This work is aimed at the definition of full design scheme allowing to combine several synthesis tools.

Results:

A complex design has already been designed using this approach. A motion estimator circuit has been designed using AMICAL. This design makes use of 2 memories with sophisticated protocol and a DSP processor designed by CATHEDRAL.

II-7.2.6. Behavioral synthesis of reprogrammable design

Members: M. RAHMOUNI, P. KISSION, H. DING, C. LIEM

In order to allow late changes when designing the chip architecture, the controller needs to be programmable. In the present version of AMICAL, a non-progammmable system-level controller can be described as a flat FSM. The goal of this work is to develop an extension of AMICAL, which will allow to generate a programmable controller.

AMICAL produces a system composed of a complex datapath and a controller. The data path may include complex functional units. These are described as a co-processor, executing complex procedures and functions. This model allows for design re-use and a recursive design methodology, i.e. a design produced by AMICAL may be used as a component in a more complex design. The main problem when extending AMICAL for the generation of programmable controllers will be to handle these complex functional units.

II-7.2.7. Programmable Architecture Design

Member: C. LIEM

This work is concerned with methodologies for the development of new ASIP architectures. Starting from a set of behavioral level descriptions of typical functions for the application domain, the objective is to determine an instruction-set optimized for the application. In turn, this instruction-set implies the definition of the data path programme sequencer, memory structure, peripherals, etc.

Given that a compiler maps an application to a processor architecture, the compiler could be used as an analysis tool to develop better architectures in the areas of data or control-flow efficiency. The instruction-set of an ASIP is the hardware/software interface and the level at which many trade-offs between speed, flexibility, hardware complexity, and compiler efficiency can be made.

This work looks at applications from a compiler perspective in an attempt to characterize the hardware resource needs for efficient functionality. Naturally, these analyses also lead to better code generation approaches.

Results:
An array transformation prototype has been developed and tested with an existing compiler system. Initial results for a set of DSP benchmarks are very encouraging: 23% code-size reduction and 39% speedup.

II-7.2.8. Behavioral synthesis for low power

*Member: Ph. GUILLAUME*

The goal of this work is to deal with power issues at the early stage of the design, i.e. during architectural synthesis. While the largest gain is expected at the architectural level, the estimation is most critical here. The goal is to take into account the power consumption evaluation and optimization during the early stages of the design process. At this level the library elements are large cores and complex macro-blocks. We need a macroscopic model for power. Our approach considers the number of switching elements in each library element for each clock cycle. Besides, each component is characterized by a switching level when Idle. This model allows to estimate with a large precision the power consumption at the clock cycle. The dynamic nature of power consumption can also be handled by using a kind of power simulation at the clock cycle level. We are planning to use this estimation for guiding the synthesis process in order to select the best solution (allocation, scheduling) in terms of power.
III - SERVICE ACTIVITY

The Laboratory is hosting the CMP Service Activity (1)

CMP

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*Introduction*

The CMP project (Circuits Multi Projets) is a project undertaken since 1981 by the Laboratory. In 1984, the service became a "Unité de Service et de Recherche", depending on CNRS and INPG. This project allows the Universities, Research Laboratories and Companies to fabricate the integrated circuits that they have designed. The originality of the project consisted originally in the regrouping, on the same slice of silicon, of a large number of circuits. Thus accessible costs of fabrication are obtained.

In addition since 1981, about 1800 circuits for Research, Education and Industry have been fabricated for use in France and also other countries.

For each project, the operations to be achieved are the following:
- collection of circuits described in a common language
- checking of the circuits (syntax checking and design rules checking)
- assembly in Macro-blocks (sets of chips)
- generation of the entry connections for the manufacture:
- subcontracting the fabrication of the circuits
- subcontracting packaging of the chips
- delivery of chips to the users.

In parallel CMP distributes to the users the design rules and the standard cell libraries for each specific software tool (design kits). About 130 design kits have been distributed to one hundred customers in France and other countries in 1995.

*Development since 1981*

Since 1981, 160 MPC projects have been undertaken. The number of manufactured circuits per year has passed from 8 in 1981 to 114 in 1992, 251 in 1994 and 298 in 1995. The complexity of the circuits has passed from several thousands transistors in 1981 to more than a hundred thousand transistors since 1985. NMOS technologies were used from 1981 to 1986 and CMOS from 1984 up to now. During the five last years, activities have been widely increased. This is reflected by TABLE V "CMP Development since 1989" and by TABLE VI: "Progression in number of circuits, participating Institutions, number of runs and total silicon area". In four years the number of circuits and the number of participating Institutions have been multiplied by 2.6, the total silicon area has doubled and 11 technologies are offered instead of 5. TABLE VII (a and b) lists the centers
having submitted circuits to the CMP Service and TABLE VIII (a, b and c) depicts the evolution of CMP projects between 1981 and 1995.

**CMP projects in 1995**

In 1995 a total of 95 Institutions (Universities, Research Laboratories and Industrial Companies) submitted 298 circuits for education, research and industrial purposes. Compared to 1994 the increasing is 19% (number of circuits) and 26% (number of Institutions). Technologies used were CMOS DLM(3) 1.5 μ, 1.2 μ, 1.0 μ, 0.7 μ of ATMEIL ES2, CMOS DLP(4) DLM 1.2 μ, 0.8 μ of AMS(4), BICMOS DLP DLM 1.2 μ, 0.8 μ of AMS, Bipolar Gate Array of TCS(4), GaAs 0.6 μ of VSC(4) and GaAs HEMT 0.2 μ of PML(4).

**Micromachining Program**

CMP has introduced in 1995 Micro Electro Mechanical Systems (MEMS) fabrication based on CMOS 1.0 μ DLM/SLP(4) (from ATMEIL ES2) compatible bulk front side micromachining (the post-processing operation is performed by EDP(4) etching at ESIEE(4)). MEMS like cantilevers, membranes, microbridges, etc... may be processed together with electronics. Design rules have been defined, available to designers upon signature of a Confidentiality and Licence Agreement. A CADENCE OPUS design kit is also available to allow the generation of the layout including electronic and non-electronic parts. The kit includes an extended DRC and an extended parameter extractor (from layout to netlist) distinguishing electronic and non-electronic parts. More than one hundred Institutions already applied for the design kit. In the same way a MENTOR GRAPHICS design kit is due to be introduced late Q2 96.

The first MPW MEMS run will be launched at the beginning of 1996; it will regroup 10 projects including a flow sensor, an electro thermal converter, an IR source, several IR sensors, several accumulators and a pellistor.

Other CMOS processes, such as CMOS 1.2 μ DLM/DLP (from AMS) compatible bulk micromachining are under final evaluation and will be introduced early 1996. Gallium Arsenide test structures are under evaluation and have been performed using PML high electron mobility transistor (HEMT) and the VITESSE MESFET foundry processes followed by selective etching. Other techniques, such as silicon surface micromachining, LIGA (X and UV) and Quartz techniques will be introduced gradually.

**Opening to Industry**

CMP opened the service to companies in 1990, and in 1995 CMP fabricated 38 industrial prototypes for 17 companies (mainly small and medium sized industrial companies). In the same way for several years CMP extended its capabilities to small volume production (from tens to thousands pieces).

Indeed requests for such quantities exist which are often not commercially attractive for most of the silicon vendors whose equipments are dedicated to higher volumes. Thus 24 small volume productions were fabricated in 1995 (8% of the fabricated circuits), compared to 12 in 1994 (5 %) and 3 in 1993 (2 %).

**Advanced processes**

In 1994, CMP introduced two very advanced industrial processes: CMOS 0.5 μ Triple Layer Metal from SGS-Thomson / France Telecom fabricated at Crolles near Grenoble, and the MMIC GaAs 0.2 μ (based on pseudomorphic High Electron Mobility Transistors) from Philips Microwave Limeil (PML), near Paris. In 1995 took place the first runs in CMOS 0.5μ, MMIC GaAs 0.2 μ and BICMOS 0.8 μ from AMS. Access to new technologies for high performance systems (Multi Chip Modules) continued to be provided.

**CAD tools offers**

In order to facilitate chip design, CMP distributes and supports several CAD softwares for both Universities and SMIs depending on the geographical location, type of customers, etc... CMP widespreads information on free software tools available from other services or Universities and
distributes design kits for these tools. In the same way CMP has agreements with workstation based tool vendors and PC tool vendors to offer these tools when necessary.

Other activities

The CMP project calls upon the multiple competences of all members of the Research group: development of software tools (to check or correct various syntax descriptions), determination of the rules of multitechnological design, working with EDIF format (a translator EDIF-GDS2-EDIF was achieved in 1990 for UNIX and VMS systems), library implementation for several softwares and several technologies: since 1992, CMP developed library kits for AMS (1.2 μ and 0.8 μ CMOS, 1.2μ and 0.8 μ BiCMOS) on CADENCE and COMPASS softwares. Library kits for PC computers were also developed, for ATMEG ES2 1.2 μ, 1.0 μ and 0.7 μ CMOS on TANNER/L-Edit and EXEMPLAR/GALILEO softwares.

Support

The CMP has been supported in 1995 by the Ministry for National Education and Higher Education and Research (MENESR, through the CNFM), the National Research Center (CNRS/SP2I), and the Ministry for Industry (MIPT, through the SERICS). CMP has participated in 1995 to European Initiatives, aimed at serving European Universities and SMIs (EUROCHIP and CHIPSHOP projects).

Conclusion

France has been a pioneer country in this type of infrastructure since chip fabrication for Universities has been started in 1981 by CMP; the elementary CAD software LUCIE has been provided to 36 Academic Institutions in France and foreign countries in the 80s (see TABLE IX: distribution of the LUCIE system), industrial CAD software has been distributed to Universities in 1986 by CNFM, testing equipment has been centrally purchased in 1988. As early as 1990, CMP had opened chip fabrication to Industry.

Through the use of advanced processes, the large portfolio of technologies offered, the introduction of Micromachining, the opening to Industry and the increasing in participation, CMP has pursued in 1995 its development towards a complete and up to date service in ICs and Microsystems, for prototyping and small volume, at an international scale.

(1) A specific report is available upon request.

(2) Until end of July

(3) Until end of September

(4) AMS : Austria Mikro Systeme International
CNFM : Comité National de Formation en Microélectronique
CNRS : Centre National de la Recherche Scientifique
DLM : Double Layer Metal
DLP : Double Layer Polysilicon
EDIF : Electronic Design Interchange Format
EDP : Ethylene Diamine Pyrocatechol-water
ESIEE : Ecole Supérieure d'Ingénieurs en Electrotechnique et Electronique
LIRMM : Laboratoire d'Informatique, Robotique et Microélectronique de Montpellier
MENESR : Ministère de l'Education Nationale, de l'Enseignement Supérieur et de la Recherche
MIPT : Ministère de l'Industrie, des Postes et Télécommunications
PML : Philips Microwave Limel-Brevannes
SLP : Single Layer Polysilicon
SMIs : Small and Medium sized Industries
SPT : Sciences pour l'Ingénieur
TCS : Thomson Composants Spécifiques
VSC : Vitesse Semiconductors Corporation
<table>
<thead>
<tr>
<th>YEAR</th>
<th>RUNS</th>
<th>AREA</th>
<th>CIRCUITS</th>
<th>INSTIT.</th>
<th>TECHNOLOGIES</th>
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<td>92</td>
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<td></td>
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<td>more integration</td>
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<td>1259 mm²</td>
<td>129</td>
<td>26</td>
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<td></td>
<td></td>
<td>TCS Bip</td>
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<td></td>
<td></td>
<td>TCS Bip</td>
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<td></td>
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<td></td>
<td></td>
<td>AMS 2μ 2M2P</td>
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<td>AMS 2μ 2M2P, AMS 1.2μ 2M2P</td>
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<td>AMS 1.2μ 2M2P (BiCMOS)</td>
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<td>VSC 0.6μ Dig. GaAs</td>
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<td>STM 0.5μ TLM</td>
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<td>AMS 0.8μ 2M 2P</td>
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<td>AMS 0.8μ 2M 2P (BiCMOS)</td>
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<td>PML 0.2μ HEMT GaAs</td>
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</table>

**TABLE V: CMP Development since 1989**
TABLE VI: Progression in number of circuits, participating Institutions, number of runs and total silicon area
LAPP
ISACOM
Etablissement Technique Central de l'Armement (ETCA)
Centre de Compétence en Conception de Circuits Intégrés (C4i)
R.E.M.F Radio Communications et Avionique S.A
Ecole Nationale Supérieure de Micro Mécanique
Ecole Nationale d'Ingénieurs de Brest (ENIB)
Ecole Nationale des Télécommunications de Bretagne
Ecole Nationale Supérieure d'Electronique et ses Applications
Ecole Supérieure d'Électricité
Ecole Centrale de Lyon
Institut National des Télécommunications
Ecole Supérieure d'Electricité
Ecole Nat. Sup. d'Electron. et de Radio Electricité
DEA de Microélectronique
Ecole Nat. Sup. d'Ingén. Electriestiens
Institut Universitaire de Technologie
Conception de Systèmes Intégrés
Techniques de l'Informatique et de la Microélec. pour l'Architecture d'Ordinateurs
Labo. Traitement d'Images et de Rec. des Formes
Unité de Génie Matériel (Laboratoire Génie Informatique)
Thomson-CSF Semiconducteurs Spécifiques
Institut des Sciences Nucléaires
Ecole Nat. Sup. d'Inf. et de Mathém. Appliqués de Grenoble (ENSIMAG)
Laboratoire de Physique des Composants à Semiconducteurs (LPSC)
LETI CENG
Midi Inongerie
Ecole Nationale Supérieure de Sciences Appliquées et Technologie (ENSSAT)
Institut Universitaire de Technologie de Séarat
Institut Supérieur d'Électronique du Nord
Laboratoire Image, Signal et Acoustique (LISA)
Centre de Physique des Particules de Marseille (CPPM)
Ecole Supérieure Ingénieurs de Marseille (ESIM - ISMEA)
Université de Metz, UFR Sci. F.A
Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier
Ecole Sup. d'Ing. en Electrotech. et Electronique
Institut d'Electronique Fondamentale
Laboratoire de Recherche en Informatique
Laboratoire de l'Accélérateur Linéaire
Laboratoire pour l'Utilisation du Rayonnement Electromagnétique (LURE)
Thomson LCR
Ecole Polytechnique
Centre de Microélectronique de Paris Ile de France (CEMIP)
Labo. de Méthodes et Archi. de Syst. Informatiques
Institut de Programmation
Ecole Nat. Sup. des Télécommunications
Ecole Normale Supérieure
Institut Supérieur d'Électronique de Paris
Laboratoire de Physique Nucléaire et de Hautes Énergies
Université Pierre & Marie Curie, Dept d'Electronique
DEA de Microélectronique (PARIS 7)
Institut de Rech. en Informat. et Syst. Aléatoires
Institut National Sciences Appliquées (INSA)
Institut Nat. de Recherche en Informat. et Automat.
Mixed Silicon Structures (MS2)
ATMEL ES2
Centre d'Etudes Nucléaires (CEN)
Leroy Automatique Industrielle
Université Louis Pasteur
Lab. d'Électronique et de Physiques des Systèmes Instrumentaux (LEPSI)
Ecole Nationale Supérieure d'Électronique et de Radiodélectricité de Bordeaux (ENSEMB)
Laboratoire de Microélectronique (IXL)
**TABLE VIIa - French Institutions having submitted circuits to CMP (total : 79)**

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<th>FOREIGN COUNTRIES</th>
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<th>COUNTRY</th>
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<td>ALGERIA</td>
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<td>Telecom Australia Research Laboratories</td>
<td>Victoria</td>
<td>AUSTRALIA</td>
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<td>Adeladle</td>
<td>AUSTRALIA</td>
</tr>
<tr>
<td>Macquarie University</td>
<td>Sydney</td>
<td>AUSTRALIA</td>
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<tr>
<td>Thomas NEUROTH</td>
<td>Vienna</td>
<td>AUSTRIA</td>
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<tr>
<td>EUROPRACTICE - ICMS</td>
<td>Louvain la Neuve</td>
<td>BELGIUM</td>
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<td>Université Catholique de Louvain la Neuve</td>
<td>Porto Alegre</td>
<td>BRAZIL</td>
</tr>
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<td>Sao Paulo</td>
<td>BRAZIL</td>
</tr>
<tr>
<td>Laboratorio de Microelectronica, EPUSP-DEE</td>
<td>Guaratinguetá</td>
<td>BRAZIL</td>
</tr>
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<td>Laboratorium de Sistemas Integravens, EPUSP</td>
<td>Campinas</td>
<td>BRAZIL</td>
</tr>
<tr>
<td>CNI/ULB Teletrons</td>
<td>Brasilia</td>
<td>BRAZIL</td>
</tr>
<tr>
<td>Universidade de Brasilia, LPCI, Dept Engenharia Eletrica</td>
<td>Florianopolis</td>
<td>BRASIL</td>
</tr>
<tr>
<td>Universidade Federal de Santa Catarina LINSE/EEL/CTC</td>
<td>Montreal</td>
<td>CANADA</td>
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<td>Ecole Polytechnique</td>
<td>Beijing</td>
<td>CHINA</td>
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<td>University of Science &amp; Tech. of China</td>
<td>Cali</td>
<td>COLOMBIA</td>
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<td>Lyngby</td>
<td>DENMARK</td>
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<td>Tranbjerg</td>
<td>DENMARK</td>
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<td>JyskbTelefon</td>
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<td>Espoo</td>
<td>FINLAND</td>
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<tr>
<td>Helsinki Univ. of Technology</td>
<td>Kauniainen</td>
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<td>Ylenia Electronica</td>
<td>Augsburg</td>
<td>GERMANY</td>
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<td>Fachhochschule Augsburg</td>
<td>Erlangen</td>
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<td>Inst. für Matem. Maschin. &amp; Datenverarbeit.</td>
<td>Bonn</td>
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<td>Bandung</td>
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<td>Tehran</td>
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<tr>
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<td>Hafif</td>
<td>ISRAEL</td>
</tr>
<tr>
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<td>Tirat Hacarmel</td>
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<td>Pisa</td>
<td>ITALY</td>
</tr>
<tr>
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<td>ITALY</td>
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<td>Trieste</td>
<td>ITALY</td>
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<td>ITALY</td>
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cont’d
TABLE VIIIb - Foreign Institutions having submitted circuits to CMP (93)

Institutions having submitted circuit(s) to CMP:

France: 79
Foreign Countries: 93
Total: 172
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<th>Gate mic</th>
<th>$\lambda$ mic</th>
<th>Inst Res</th>
<th>Cir Ed</th>
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<td>ECDM20</td>
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Total in 1994: 32 Projects

10 technologies 251 circuits 3,625 mm²

TABLE VIIIb - CMP projects in 1994
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**Total in 1995**: 34 Projects

**11 technologies 298 circuits 3 817 mm2**

**TABLE VIIIe - CMP projects in 1995**

**CMP projects, total since 1981**: 160 Projects

**1 765 circuits: 815 Research circuits, 809 Education circuits, 141 Industrial circuits**
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<td>Barcelone (Spain)</td>
<td>&quot;</td>
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<tr>
<td>IMAG</td>
<td>Lausanne (Switzerland)</td>
<td>&quot;</td>
</tr>
<tr>
<td>Commissariat aux Energies Nouvelles</td>
<td>Erlangen (Germany)</td>
<td>&quot;</td>
</tr>
<tr>
<td>Ecole Centrale de Lyon</td>
<td>Grenoble</td>
<td>&quot;</td>
</tr>
<tr>
<td>University of Patras</td>
<td>Algiers (Algeria)</td>
<td>&quot;</td>
</tr>
<tr>
<td>Chengdu Institute of Radio Engineering (China)</td>
<td>Lyon</td>
<td>&quot;</td>
</tr>
<tr>
<td>Université des Sciences et de la Technologie</td>
<td>Parnas (Greece)</td>
<td>&quot;</td>
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<tr>
<td>University of Bandung (Indonesia)</td>
<td>Chengdu (China)</td>
<td>&quot;</td>
</tr>
<tr>
<td>University of Athens</td>
<td>Oran (Algeria)</td>
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<tr>
<td>Univ. Federal do Rio Grande do Sul (Brazil)</td>
<td>Bandung (Indonesia)</td>
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<tr>
<td>Inst Supérieur du Nord</td>
<td>Athens (Greece)</td>
<td>&quot;</td>
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<tr>
<td>Lab Automatique et de Microélectronique</td>
<td>Porto Alegre (Brazil)</td>
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<tr>
<td>Eco. Nat Sup de physique</td>
<td>Lille</td>
<td>&quot;</td>
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<tr>
<td>I.R.I.S.A.</td>
<td>Montpellier</td>
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<tr>
<td>IMAG</td>
<td>Marseille</td>
<td>&quot;</td>
</tr>
<tr>
<td>Eco Nat Sup d'électronique et de radioélectricité</td>
<td>Rennes</td>
<td>&quot;</td>
</tr>
<tr>
<td>Inst Electronique Fondamentale Orsay</td>
<td>Grenoble</td>
<td>&quot;</td>
</tr>
<tr>
<td>Inst Physique nucléaire</td>
<td>Grenoble</td>
<td>&quot;</td>
</tr>
<tr>
<td>INESC</td>
<td>Paris</td>
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<td>IMAG</td>
<td>Villeurbanne</td>
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<td>ESE</td>
<td>Lisbon (Portugal)</td>
<td>&quot;</td>
</tr>
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<td>IEF</td>
<td>Grenoble</td>
<td>&quot;</td>
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<td>ENPM</td>
<td>Rennes</td>
<td>&quot;</td>
</tr>
<tr>
<td>Université Louis Pasteur</td>
<td>Orsay</td>
<td>&quot;</td>
</tr>
<tr>
<td>compatible</td>
<td>Marseille</td>
<td>&quot;</td>
</tr>
<tr>
<td>Universidad del Valle</td>
<td>Strasbourg</td>
<td>&quot;</td>
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<tr>
<td>Electrotechnicka Fakulta</td>
<td>Cali (Colombia)</td>
<td>&quot;</td>
</tr>
<tr>
<td>University of Petroleum and Minerals (Saudi Arabia)</td>
<td>Bratislava (Czechoslovakia)</td>
<td>&quot;</td>
</tr>
<tr>
<td></td>
<td>Dhahran (Saudi Arabia)</td>
<td>&quot;</td>
</tr>
</tbody>
</table>

**TABLE IX : Distribution of the LUCIE system**
## IV - RESOURCES

### IV-1 Human resources

#### IV-1.1 Members of the Laboratory

Table X presents a list of the researchers and engineers involved in the Laboratory, Table XI presents the researchers from Industry working in the Laboratory, Table XII lists researchers who stayed in the Laboratory during 1995, Table XIII lists researchers working in other institutions, but enrolled with the Laboratory for a thesis, and Table XIV lists researchers whose advisor is a member of the Laboratory for their foreign thesis.

| ABOU-SAMRA | Sélim Joseph | Researcher ND |
| AMIELH | Isabelle | Contracted Secretary |
| ANTUNES | Ana | DEA |
| BALME | Louis | Associate Professor |
| BENALI | Audil | Res. ND / CIFRE IMD |
| BENIS | Chantal | Contracted Secretary |
| BEN ISMAIL | Tarek | Researcher ND |
| BERNAL | Alvaro | Researcher ND |
| BERREBI | Elisabeth | Res. ND / CIFRE SGS-Thomson |
| BIANCHI | André | DEA |
| BLANQUEZ | Oscar | DEA |
| BOUDJIT | Mokhtar | Researcher ND |
| BOUTAMINE | Hicham | Researcher ND |
| CALIN | Todor | Researcher ND |
| CESARIO | Wander | Researcher ND |
| CHAHAOUB | Faouzi | Researcher ND |
| CHANGUEL | Adel | Researcher ND |
| COISSARD | Vincent | Researcher ND |
| COSTA | Luiz Fernando | Researcher ND |
| COURTOIS | Bernard | DR - CNRS |
| DAVEAU | Jean-Marc | Researcher ND |
| DELORI | Hubert | Engineer - CNRS |
| DIAS | Fernando | DEA |
| DING | Hong | Researcher ND |
| DURAND-VIEL | Corinne | Contracted secretary |
| ESSALIHINE | Isabelle | Contracted secretary |
| EYRAUD | Sylvaine | Contracted Tech |
| GARNIER | Christophe | Contracted Engineer |
| GUILLAUME | Philippe | Researcher ND |
| GUYOT | Alain | Professor - ENSIMAG |
| JERRAYA | Ahmed | CR. CNRS |
| KACZMAREK | Philippe | Accountant CNRS |
| KARAM | Jean-Michel | Contracted Researcher |
| KEBICHI | Omar | Contracted Engineer |
| KISSION | Polen | Researcher ND and ATER |
| KODRUA | Marc | Res. ND / CIFRE SGS-Thomson |
| KRI | Nedim | Contracted Engineer |
| LJEM | Cliff | Researcher ND |
| LUBASZEWSKI | Marcelo | Associate Researcher |
| MAAREF | Brahim | DEA |
| MAROUFI | Waki | Researcher ND |

cont'd
MARCHIORO Gilberto
MARZOUKI Meryem
MERCIER Benoît
MIR Salvador
MOHAMED Firas
MONTALVO Luis
MOUSSA Imed
NACABAL François
NICOLAIDIS Michel
OLIVEIRA-DUARTE Ricardo
PAILLOTIN Jean-François
PAREKHJI Rubin
PARET Jean-Marc
PEREZ-RIBAS Renato
PISTORIUS Richard
RAKHOUMI Maher
RAYANE Iyad
ROMdhANI Mohamed
SCIMONE Patricia
SIMEU Emmanuel
SKAF Ali
TORKI Khaled
TOUATI Mohamed
VACHER André
VARGAS Carlos
VELASCO MEDINA Fabian Luis
VIJAYA RAGHAVAN Jaime
VINCI DOS SANTOS Vijay

TABLE X - Members of the Laboratory (for 1995)

DEA = involved in Ph.D. degree
ND = involved in Doctorate degree
DE = involved in "Thèse d'État" degree
ATER = Teaching and Research Assistant

FREHEL Jean

TABLE XI - Researchers from Industry working in the Laboratory (for 1995)

<table>
<thead>
<tr>
<th>Visitors</th>
<th>NAME</th>
<th>FIRST NAME</th>
<th>COUNTRY (and origin if French)</th>
<th>DURATION FOR 1995</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABID</td>
<td>Mohamed</td>
<td>Tunisia</td>
<td>3 months</td>
<td></td>
</tr>
<tr>
<td>BACIVAROV</td>
<td>Ioan</td>
<td>Romania</td>
<td>2 months</td>
<td></td>
</tr>
<tr>
<td>BENEDEK</td>
<td>Zsolt</td>
<td>Hungary</td>
<td>2 months cont'd</td>
<td></td>
</tr>
<tr>
<td>NAME</td>
<td>FIRST NAME</td>
<td>COUNTRY</td>
<td>DURATION FOR 1995</td>
<td></td>
</tr>
<tr>
<td>-------------------</td>
<td>------------</td>
<td>--------------------------</td>
<td>-------------------</td>
<td></td>
</tr>
<tr>
<td>BENMOHAMMED</td>
<td>Mohamed</td>
<td>Algeria</td>
<td>6 months</td>
<td></td>
</tr>
<tr>
<td>CAI</td>
<td>Hong Xue</td>
<td>China</td>
<td>4 months</td>
<td></td>
</tr>
<tr>
<td>DIMITROV</td>
<td>Dimiter</td>
<td>Bulgaria</td>
<td>2 weeks</td>
<td></td>
</tr>
<tr>
<td>FARKAS</td>
<td>Gabor</td>
<td>Hungary</td>
<td>2 weeks</td>
<td></td>
</tr>
<tr>
<td>FERNANDES</td>
<td>Antonio</td>
<td>Brazil</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>FJALIKOWSKI</td>
<td>Antoni</td>
<td>Poland</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>KACCHROVA</td>
<td>Lilia</td>
<td>Russia</td>
<td>1 month</td>
<td></td>
</tr>
<tr>
<td>KOV</td>
<td>Andrzei</td>
<td>Poland</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>LUBA</td>
<td>Tadeusz</td>
<td>Poland</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>MATROSOVA</td>
<td>Anjela</td>
<td>Russia</td>
<td>2 weeks</td>
<td></td>
</tr>
<tr>
<td>MILLER</td>
<td>Michael</td>
<td>Canada</td>
<td>6 months</td>
<td></td>
</tr>
<tr>
<td>NAJII</td>
<td>Brahim</td>
<td>Morocco</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>NAPIERALSKI</td>
<td>Andrzei</td>
<td>Poland</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>NASRI</td>
<td>Salem</td>
<td>Tunisia</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>PFEITZNER</td>
<td>Andrzei</td>
<td>Poland</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>PLESKACZ</td>
<td>Witold</td>
<td>Poland</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>POPPE</td>
<td>Andreas</td>
<td>Hungary</td>
<td>2 months</td>
<td></td>
</tr>
<tr>
<td>REIS</td>
<td>Ricardo</td>
<td>Brazil</td>
<td>1 week</td>
<td></td>
</tr>
<tr>
<td>RENCZ</td>
<td>Marta</td>
<td>Hungary</td>
<td>1 month</td>
<td></td>
</tr>
<tr>
<td>UBAR</td>
<td>Raimund</td>
<td>Estonia</td>
<td>2 months</td>
<td></td>
</tr>
<tr>
<td>USKOV</td>
<td>Vladimir</td>
<td>Russia</td>
<td>1 month</td>
<td></td>
</tr>
<tr>
<td>VAINOMAA</td>
<td>Kaido</td>
<td>Estonia</td>
<td>1 month</td>
<td></td>
</tr>
<tr>
<td>VASSILEVA</td>
<td>Tania</td>
<td>Bulgaria</td>
<td>1 month</td>
<td></td>
</tr>
<tr>
<td>WANG</td>
<td>Jiang Chong</td>
<td>Brazil</td>
<td>3 weeks</td>
<td></td>
</tr>
<tr>
<td>YEVTVUSHENKO</td>
<td>Nina</td>
<td>Russia</td>
<td>2 weeks</td>
<td></td>
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</table>

Trainees

<table>
<thead>
<tr>
<th>FIRST NAME</th>
<th>COUNTRY</th>
<th>DURATION FOR 1995</th>
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<tbody>
<tr>
<td>AL-MOHANNADI</td>
<td>Khalid</td>
<td>Qatar</td>
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<tr>
<td>BAUGE</td>
<td>Mark</td>
<td>France (ESIEE)</td>
</tr>
<tr>
<td>BRAUER</td>
<td>Michael</td>
<td>Germany</td>
</tr>
<tr>
<td>CSENDES</td>
<td>Alpar</td>
<td>Hungary</td>
</tr>
<tr>
<td>DIMBATH</td>
<td>Roland</td>
<td>Germany</td>
</tr>
<tr>
<td>FEDTSENKO</td>
<td>Igor</td>
<td>Estonia</td>
</tr>
<tr>
<td>FÜRGETEG</td>
<td>Csaba</td>
<td>Hungary</td>
</tr>
<tr>
<td>GILLINGSRUD</td>
<td>Oyvind</td>
<td>Norway</td>
</tr>
<tr>
<td>HAJAS</td>
<td>Gabor</td>
<td>Hungary</td>
</tr>
<tr>
<td>HAMZA</td>
<td>Richa</td>
<td>France (ENSERG)</td>
</tr>
<tr>
<td>HÖLJÖ</td>
<td>Mikael</td>
<td>Sweden</td>
</tr>
<tr>
<td>IVASK</td>
<td>Eero</td>
<td>Estonia</td>
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<td>JERVAN</td>
<td>Gert</td>
<td>Estonia</td>
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<td>KANAN</td>
<td>Riad</td>
<td>Jordan</td>
</tr>
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<td>KOCSIS</td>
<td>Tamás</td>
<td>Hungary</td>
</tr>
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<td>KOHARI</td>
<td>Zsolt</td>
<td>Hungary</td>
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<td>KOORT</td>
<td>Marko</td>
<td>Estonia</td>
</tr>
<tr>
<td>KOWALCZYK</td>
<td>Arkadiusz</td>
<td>Hungary</td>
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<td>LEVERING</td>
<td>Volker</td>
<td>Germany</td>
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<td>LIPTAK-FEGO</td>
<td>Laszlo</td>
<td>Hungary</td>
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<td>MARCIE</td>
<td>David</td>
<td>Canada</td>
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<tr>
<td>MARKUS</td>
<td>Anit</td>
<td>Estonia</td>
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<tr>
<td>MARTA</td>
<td>Csaba</td>
<td>Hungary</td>
</tr>
<tr>
<td>MAEREN</td>
<td>Pascal</td>
<td>Belgium</td>
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<tr>
<td>MIMOUNE</td>
<td>Réda</td>
<td>France (ENSERG)</td>
</tr>
<tr>
<td>MORTENSEN</td>
<td>Lars Bo</td>
<td>Denmark</td>
</tr>
<tr>
<td>MORVAY</td>
<td>Balazs</td>
<td>Hungary</td>
</tr>
<tr>
<td>MITIBAA</td>
<td>Abdellatif</td>
<td>Tunisia</td>
</tr>
<tr>
<td>NGUYEN</td>
<td>Van Phuong</td>
<td>France (UIF)</td>
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<table>
<thead>
<tr>
<th>Name</th>
<th>Country</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>NIELSEN</td>
<td>Denmark</td>
<td>1 month</td>
</tr>
<tr>
<td>OELS</td>
<td>Germany</td>
<td>6 months</td>
</tr>
<tr>
<td>ÖZDEN</td>
<td>The Netherlands</td>
<td>2 months</td>
</tr>
<tr>
<td>PAHÚ</td>
<td>Hungary</td>
<td>2 months</td>
</tr>
<tr>
<td>PAOMETS</td>
<td>Estonia</td>
<td>1.5 months</td>
</tr>
<tr>
<td>PAQUET</td>
<td>France (ENSERG)</td>
<td>3 months</td>
</tr>
<tr>
<td>PEDERSEN</td>
<td>Denmark</td>
<td>3.5 months</td>
</tr>
<tr>
<td>FIRMÉZ</td>
<td>Brazil</td>
<td>5 months</td>
</tr>
<tr>
<td>POLDRE</td>
<td>Estonia</td>
<td>1 week</td>
</tr>
<tr>
<td>RAIK</td>
<td>Estonia</td>
<td>1.5 month</td>
</tr>
<tr>
<td>SALLYAY</td>
<td>Hungary</td>
<td>3 months</td>
</tr>
<tr>
<td>TCHIOUMATCHENKO</td>
<td>Bulgaria</td>
<td>2 months</td>
</tr>
<tr>
<td>TEILLAS</td>
<td>Estonia</td>
<td>2 months</td>
</tr>
<tr>
<td>THEISEN</td>
<td>Germany</td>
<td>2 months</td>
</tr>
<tr>
<td>TROMELIN</td>
<td>France (ENSERG)</td>
<td>3 months</td>
</tr>
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<td>TRUONG</td>
<td>France (ENSERG)</td>
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<tr>
<td>VAN STEENKISTE</td>
<td>Belgium</td>
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<td>WISSING</td>
<td>The Netherlands</td>
<td>7 months</td>
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<tr>
<td>ZENS</td>
<td>Germany</td>
<td>4 months</td>
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**TABLE XII : Visitors and Trainees (for 1995)**

<table>
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<tr>
<th>Name</th>
<th>Country</th>
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</thead>
<tbody>
<tr>
<td>GUILLERMOS</td>
<td>DASSAULT - St Cloud - France</td>
</tr>
<tr>
<td>KAESLTI</td>
<td>Société Générale de Surveillance - Genève - Switzerland</td>
</tr>
<tr>
<td>LEMERY</td>
<td>SGS-Thomson - Grenoble - France</td>
</tr>
<tr>
<td>SORGAGE</td>
<td>SGS-Thomson - Puyvessin - France</td>
</tr>
<tr>
<td>STEFANI</td>
<td>AFAQ- Paris - France</td>
</tr>
</tbody>
</table>

**TABLE XIII : Researchers working in other institutions, but enrolled with the Laboratory for their thesis in Grenoble**

<table>
<thead>
<tr>
<th>Name</th>
<th>Country</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABID</td>
<td>UNIV. of Monastir - Tunisia</td>
</tr>
<tr>
<td>BENMOHAMMED</td>
<td>UNIV. of Sidi Bel Abbes - Algeria</td>
</tr>
<tr>
<td>TCHIOUMATCHENKO</td>
<td>UNIV. of Sofia - Bulgaria</td>
</tr>
</tbody>
</table>

**TABLE XIV : Researchers whose advisor is a member of the Laboratory for their thesis abroad**
IV-1.2 Biographies of staff members
Louis J. BALME

Born August 23rd, 1951 in Grenoble, France
Married, 3 children
French

Education

1972 : Master's Degree - Economics and Politics - IEP Grenoble
1975 : Master's Degree - Electronics - Institut National Polytechnique - Grenoble (INPG)
1976 : PhD Electronics - INPG
"Applications of Spectral Bioimpedometry to EEG and cerebral imagery"
1990 : Habilitation à Diriger des Recherches (French National Authorization to Supervise Research)

Position

* Associate Professor in Electronics at Institut National Polytechnique de Grenoble (INPG)

Current Responsibilities

* Professor in Signal Processing, Information Theory and Quality of Complex Systems (RAMs)
* Responsible for Quality Complex integrated Systems research group at TIMA Laboratory
* Secretary General of the European Programme in Quality of Complex Integrated Systems
* Member of the Editorial Board of the Journal of Quality Engineering (USA)

Previous Positions

* Director of Corporate Relations of INPG (1984-1991)
* President and CEO of SYMAG Computers (1979-1984)
* Assistant Professor INPG (1974-1979)

Miscellaneous

* Registered European Quality Consultant (since 1993)
* Consultant KEYO Corporation (1984-1987)
* President of Synergy Commission at the French computer Industry Association (1984-1987)
* Director of the INPG Master's Degree "Quality of Computers Systems" (1989-1992)
* Vice-President of Merlin Gerin - INPG Economic Interest Grouping (1989-1992)
* 44 publications
* 7 PhDs Management
* 16 Professional Theses Management
* Gold Medal from the International Inventors Exhibition - Brussels 1986
Bernard COURTOIS

Born April 17th, 1948
Married, 2 children
French

Education

1967 - Baccalaureat degree - Mathematics
1968 - Baccalaureat degree - Philosophy
1967 - 1970 Mathematics in Paris
1970 - 1973 National School for Informatics and Applied Mathematics in Grenoble
1973 - Engineer degree
1976 - Doctor-Engineer degree
1981 - Docteur d'État degree

Position

"Directeur de Recherches" CNRS

Current responsibilities

* Director of TTMA Laboratory
* Director of CMP Service

Miscellaneous

* Has authored or co-authored many scientific papers
* Has served in many Committees of Conferences & Workshops
* Has served as a reviewer of research proposals to CEC, NATO, NSF, SERC.
Hubert DELORI

Born December 26th, 1946
Married, 5 children
French

Education

1964  Baccalaureat degree - Mathematics
1964-1967  Mathematiques Supérieures & Mathematiques Spéciales, Lycée Janson de Sailly, Paris
1967-1970  Engineer studies at Ecole Centrale de Lyon
1970  Engineer degree from Ecole Centrale de Lyon.

Position

"Ingénieur de Recherche" at CNRS (Centre National de la Recherche Scientifique).

Past activities

1970  Programming at IBM Corbeil-Essonnes.
1972  Teaching in Mathematics and Statistics in Algeria (for the military service).
1973  Engineer at "Cabinet Roland Olivier" : working in statistics for a national inquiry about agriculture in Algeria.
1975  Education of physically handicapped young people for social re-insertion.
1978  Engineer at ICARE (Informatique Communale Alpes Rhône) at the town hall of Saint Étienne : responsible of the working of the informatics applications.
1979  Complementary studying in System Programming at "Institut de Programmation de Grenoble" (1 year).
1983  Engineer at CMP (Circuits Multi Projets) in the group of Prof. Anceau.

Current responsibilities

Technical responsible of the CMP (Circuits Multi Projets) Service: National Service for manufacturing integrated circuits for all the French Universities and Research Laboratories.
Sylvaine EYRAUD

Born March 23rd, 1970
Married
French

Education

1989 : Baccalaureat degree in Mathematics and Natural Sciences
1991 : DUT in Computer Sciences
1994 : "Diplôme d'Études Supérieures Techniques d'informatique d'entreprises" (informatics for companies)

Position

Contractual technician with CMP since February 1993.

Current responsibilities

* Management and distribution of design kits for CMP
* Database responsible at CMP.
Christophe GARNIER

Born November 26th, 1964
Married
French

Education

1988 - DEA Electronics, University of Strasbourg, France
1991 - Ph.D. degree (Microelectronics) "New self-aligned technology for MESFET
and TEGFET on GaAs and AlGaAs digital circuits".

Position

Contractual engineer with CMP since January 1991

Current responsibilities

* SGS-Thomson BiCMOS runs
* GaAs runs
* MCM activity.
Alain GUYOT

Born September 11th, 1945
Married, 3 children
French

Education

1970 - Master in Computer Science from Grenoble University
1975 - Ph.D in Computer Science from Grenoble University
1991 - "Habilitation à diriger des Recherches"

Position

Assistant Professor (Maître de Conférences) at ENSIMAG (Ecole Nationale
Supérieure d'Informatique et de Mathématiques Appliquées de Grenoble) since 1986

Past activities

* Teacher in computer architecture and VLSI design mainly at ENSIMAG and Grenoble
  University since 1971
* Visiting scholar or invited professor with the CSL group in Stanford University (Prof.
  M. Flynn), Microelectronic group in Telecom University, Paris (Prof. Jutand) and LBG-
  EPFL in Lausanne (Prof. M. Declercq)
* Participated in 1980 to the starting of the CMP foundry service
* Author or co-author of more than 50 scientific publications in Journals, Conference
  Proceedings, or Research Reports
* Served as a reviewer for ESSCIRC, VLSI, Computer Arithmetic, EUROASIC, IEEE
  TC, CAVE and other conferences.

Current responsibilities

* Responsibility of the Integrated Systems Design Group
* Currently responsible of the project "OCAPI" aimed at the design of a family of
  integrated arithmetic processors, partially supported by the GCIS.
Ahmed Amine JERAYA

Born August 1st, 1955  
Married, 1 child  
French and Tunisian

Education

1980  Engineer degree, Faculté des Sciences de Tunis, Tunisie.
1981  DEA, Computer Science, Institut Polytechnique de Grenoble, (INPG), France
1983  Doctor-Engineer degree, Computer Science, INPG.
1989  Doctorat d'Etat degree, INPG.

Position

Researcher with CNRS, the French National Center for Scientific Research. Section: Computer Science.

Past Activities

- Participated to the LUCIE system, highly successful layout tools, distributed in the early 80s to 20 Laboratories in France and 17 abroad.
- Participated to the definition of the symbolic layout STYX system in the mid 80s, that is still in use with SGS-Thomson.
- Led the APOLLON/SYCO projects, early architectural synthesis tools.
- Led the AMICAL project, a highly successful architectural synthesis tool that is being transferred to industry.

Current Responsibilities

- Leader of the System Level Synthesis Group of TIMA at INPG.

Miscellaneous

- Award of "President de la République" in Tunisia, 1980, Best Computer Science Engineer Degree.
- Served in the Program Committee of EDAC, High-Level Synthesis Workshop, EuroDac, EuroVHDL, VHDL International, APCHDL, CODES Workshop and ICCD.
- Several tutorials in international conferences (EuroVHDL, EuroVHDL-EURODAC, APCHDL)
- Spent one year at Bell Northern Research in Ottawa, Canada
- Technical Program and Organization Chairperson of ISSS'95 Conference
- Program Chair of RSP'96 Workshop
- General Chair of 9th International Symposium on System Synthesis, La Jolla, CA, USA
Jean Michel KARAM

Born November 14th, 1969
Single
Lebanese

Education

1987 - 1989 Mathématiques supérieures & spéciales, Ecole Supérieure d'Ingénieurs de Beyrouth (ESIB), Lebanon

1993 Engineer degree, Ecole Supérieure d'Ingénieurs en Electrotechnique et Electronique (ESIEE), Paris, France

1993 DEA Microelectronics, University of Paris VII, France

Position

Researcher with TIMA laboratory since January 1994

Current Responsibilities

Leader of the MicroSystems group

Miscellaneous

* Researcher with TIMC laboratory (in share with TIMA laboratory)
* Responsible of microsystem development activities at the CMP Service
* Expert for the UK government funding body EPSRC on research involving microsystems
* Author or co-author of more than 20 scientific papers
* Member of many Committees of Conferences and Workshops
* Guest-editor of a Special Issue on Nanotechnology and Microtechnology of the Microelectronics Journal, 1996
* IEEE member
Omar KEBICHI

Born September 11th, 1965
Married
Algerian

Education

1989 : Engineer degree in Electronics, Blida University (Algeria)

1990 : DEA Microelectronics, Institut National Polytechnique de Grenoble (INPG), France

1994 : Ph. D. degree in Microelectronics, Institut National Polytechnique de Grenoble (INPG), France
Thesis : "Techniques and CAD Tools for Automatic Generation of BIST and DFT for RAMs"

Position

Contractual research engineer with TIMA/INPG Laboratory since Sept. 94

Current responsibilities

Participation to JESSI AC6, European project

Miscellaneous

* Several publications in international conferences and journals
* Teaching in DEA
* Program Committee Member of the 1st IEEE Int. On-Line Testing Workshop
Nadim KRIM

Born October 3rd, 1965  
Single  
French

Education

1988 : Master degree in computer science  
1989 : DESS microelectronics, PARIS VI Univ. (MASI), PARIS

Position

Contractual engineer with TIMA Laboratory since October 1993.

Current Responsibilities

* CAD Manager at CMP  
* OMI Responsible for IUN2 and EUROMIC projects

Miscellaneous

Marcelo LUBASZEWSKI

Born April 16th, 1964
Married, 2 children
Brazilian

Education

1986 - Engineer degree - Electrical, Federal University of Rio Grande do Sul, Brazil
1990 - Master degree - Computer Science, Federal University of Rio Grande do Sul, Brazil
1994 - PhD degree - Computer Science, INP Grenoble, France
"The Unified Board Testing applied to the Design of Reliable Systems"

Position

Professor at the Electrical Engineering Department of Federal University of Rio Grande do Sul, Brazil, researcher associated to TIMA/INPG

Current Responsibilities

* TIMA technical responsible (in share with B. COURTOIS and M. NICOLAIDIS) for ARCHIMEDES project (#7107 - ESPRIT III - CEC)

* TIMA technical responsible (in share with B. COURTOIS) for AMATIST project (#8820 - ESPRIT III - CEC)

* Leader (in share with B. COURTOIS) of the Analogue Testing Methods group

Miscellaneous

* Courses and lectures on testing in the framework of cooperation with industries
* Technical activities in cooperative projects with the USA, Canada and Brazil
Meryem MARZOUKI

Born April 17th, 1961
Married
French and Tunisian

Education

1986 - Engineer degree (Computer Science) - University of Tunis, Tunisia
1987 - DEA (Computer Science) - INPG, Grenoble, France
1991 - Ph.D. degree (Computer Science) - INPG, Grenoble. "KBS approaches to VLSI circuit testing : application to prototype validation by contactless testing".

Position

Contractual researcher with TIMA Laboratory (August 1986-October 1992)
"Chargée de Recherches" with the CNRS (since October 1992)

Past responsibilities

* Responsible for SEM-based fault location project of the GCIS/CNRS national programme.
* Responsible for ICs certification methodologies project (research contract with CNES).
* TIMA Technical Responsible for ADVICE project (# 271 - ESPRIT I - CEC).

Current responsibilities

Benoit MERCIER

Born June 10th, 1966
Single
French

Education

1988     Master degree in Electronics - University of REIMS
1990     Engineer degree in an Electronics-Microelectronics option.
         I.S.E.N -Lille- France.

Past Activities

         I.N.S.E.T- Yamoussoukro - Ivory Coast.

Position

Contractual Engineer with CMP

Current Activities

* SGS-Thomson 0.5 μ runs
* Design kits development
* COMPASS tools.
Mihail NICOLAIIDIS

Born April 22nd, 1954
Single
French and Greek

Education

1978 Engineer degree - Mechanical-Electrical, Ecole Polytechnique de l'Université de Thessaloniki.
1984 Doctor-Engineer degree - Data processing
Design of self-testing integrated circuits for analytical failures hypotheses.

Position

"Directeur de Recherche" at CNRS

Current responsibilities

Responsible of the Reliable Integrated Systems Group of TIMA Laboratory.
Jean-François PAILLOTIN

Born October 6th, 1955
Single
French

Education

1978 - Licence Telecommunications - Reims University
1979 - Licence Computer Sciences - UJF Grenoble
1980 - Master Degree Computer Sciences - UJF Grenoble
1981 - DEA Computer Sciences - INP Grenoble
1984 - Doctorate Computer Sciences - INP Grenoble.

Position

Present position : "Ingénieur de Recherche" National Education

Before :

* LCS researcher, INP Grenoble
* Assistant Teacher at IUT of Computer Sciences, Grenoble
* Assistant Teacher at UJF.

Current responsibilities

* Technical responsible since 1985 for the CMP (Circuits Multi Projets) : national service for manufacturing integrated circuits for all the french Universities and Research Laboratories (about 1800 integrated circuits fabricated since 1981).
* ATMEL ES2, VSC and PML runs responsible.
Richard PISTORIUS

Born October 31st, 1967
Single
German

Education

1993 : Engineer Degree in Microelectronics, IRISA, Rennes, France and "Universität des Saarlandes", Saarbrücken, Germany

Past activities

1993-1994 : Complementary studies in Economics at "Technische Universität", Munich, Germany (1 year)

Position

Contractual engineer with TIMA Laboratory since November 1994.

Current responsibilities

Support and development within the AMICAL project.
System engineer at TIMA Laboratory.
Emmanuel SIMEU

Born December 25th, 1959
Married, 2 children
French and Cameroonian

Education

1987- Engineer degree - Electrical- University of Casablanca (Morocco)
1988- DEA degree in Automatic Control and Signal Processing, Institut National
Polytechnique de Grenoble.

1992- Ph.D in Automatic Control and System Theory, Institut National
Polytechnique de Grenoble.

Position

Assistant Professor (Maître de Conférences) at ISTG (Institut des Sciences et
Techniques de Grenoble).

Current responsibilities

Member of the Diagnosis of Complex Systems Group.

Previous Positions

Assistant Professor at ISAR (Institut Supérieur d'Automatique et de Robotique

Researcher in LAG (Laboratoire d'Automatique de Grenoble) (1988 - 1995)
Researcher in CNET-CNS Grenoble (SITAR Project 1989 - 1992)
Kholdoun TORKI

Born February 21\textsuperscript{th} 1961
Single
Tunisian

\textbf{Education}

1985 : "Maîtrise" degree in physics and electronics, University of Constantine.
1986 : DEA microelectronics, INPG, Grenoble.
1990 : Ph.D. degree, INPG, Grenoble.

\textbf{Position}

Engineer at CNRS since 1994.
Contractual engineer with CMP-TIMA Laboratory since June 1990.

\textbf{Current Responsibilities:}

* Managing design-kit developments for different foundries under different CAD/CAE systems
* Participation and technical responsibilities in promoting microelectronics for SMEs
* Contact person at CMP for the AMS foundry
<table>
<thead>
<tr>
<th>Name</th>
<th>BERNAL N., Alvaro</th>
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<td>Expected date of degree</td>
<td>1998</td>
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<tr>
<td>Previous degrees</td>
<td>M.Sc. in Electrical Engineering, Sao Paulo University, Brazil</td>
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<td>Research interests</td>
<td>CMOS-GaAs digital integrated circuits design</td>
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<td>Scholarship from Colombian's government</td>
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<tr>
<td>Research interests</td>
<td>DEA in Microelectronics (1990), U.J.F., Grenoble (France)</td>
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<td>Present employment</td>
<td>Built-In Self-Test, Self-Checking circuits</td>
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<tr>
<td>Previous degrees</td>
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<tr>
<td>Research interests</td>
<td>Technology migration</td>
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<tr>
<td>Previous degrees</td>
<td>Engineer in Electronics and Telecommunications (1977), Politehnica University of Bucharest, Romania</td>
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<tr>
<td>Research interests</td>
<td>Radiation-tolerant CMOS circuit design, current testing, self-testing microsystem architectures</td>
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<td>Present employment</td>
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<tr>
<td>Previous degrees</td>
<td>Engineer in Electronics (1989), Master degree in Microelectronics (1994), Univ. Sao Paulo, Brazil</td>
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<tr>
<td>Research interests</td>
<td>High-level synthesis</td>
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<tr>
<td>Present employment</td>
<td>CAPES (Brazil) scholarship</td>
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<th>Name</th>
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<td>Previous degrees</td>
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<tr>
<td>Research interests</td>
<td>CAD tools for analog circuits</td>
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<td>Present employment</td>
<td>Scholarship from Morocco's government</td>
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<td>Electronics Engineer (1993), ENIM, Monastir, Tunisia; DEA in Microelectronics, (1993), INPG, Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>High level synthesis (HW/SW co-design)</td>
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<td>Present employment</td>
<td>Scholarship from Tunisian's government</td>
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### IV-1.3 Curriculum vitae of Doctorate candidates

<table>
<thead>
<tr>
<th>Name</th>
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<tr>
<td>Expected date of degree</td>
<td>1996 (&quot;Thèse d'Etat&quot;)</td>
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<td>Research interests</td>
<td>Hardware/Software Co-Design</td>
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<td>Present employment</td>
<td>ENIM (École Nationale d'Ingénieurs de Monastir), Tunisia</td>
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<tr>
<th>Name</th>
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<td>Expected date of degree</td>
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<tr>
<td>Previous degrees</td>
<td>B. Sc in Physics (1994), Liverpool Univ., UK</td>
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<td></td>
<td>DEA (M.Sc.) in Microelectronics (1995), Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>3D CMOS on SOI design methodology</td>
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<td>Present employment</td>
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<td>Previous degrees</td>
<td>Electronic Engineer (1992), ENSERG, Grenoble, France</td>
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<td></td>
<td>DEA degree (1992), ENSERG, Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>Image Processing - test of bare circuits</td>
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<tr>
<td>Present employment</td>
<td>IMD, Grenoble (France)</td>
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<th>Name</th>
<th>BEN ISMAI, Tarek</th>
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<td>Previous degrees</td>
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<td>Research interests</td>
<td>Partitioning, system-level synthesis</td>
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<td>Present employment</td>
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<td>Previous degrees</td>
<td>Computer Science Engineering (1983), INI, Alger, Algeria</td>
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<td>Magister in Computer Sc. (1988), Alger, Algeria</td>
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<tr>
<td>Research interests</td>
<td>Silicon compiler, high-level synthesis</td>
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<td>Present employment</td>
<td>Institute of Computer Science, Univ. of Sidi Bel-Abbes, Algeria</td>
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<th>Name</th>
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<td>March 1997</td>
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<tr>
<td>Previous degrees</td>
<td>Engineer (1993), DEA in integrated Electronic Devices (1993), Ecole Centrale de Lyon, France</td>
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<tr>
<td>Research interests</td>
<td>High-level synthesis</td>
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<td>Present employment</td>
<td>CIFRE contract with SGS-Thomson Microelectronics</td>
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</tbody>
</table>
Name: COISSARD, Vincent

Expected date of degree: 1997
Previous degrees: DEA in Microelectronics (1993), UJF, Grenoble, France
Research interests: Arithmetic coprocessor design
Present employment: MESR (French Ministry for Research and Higher Education) scholarship

Name: COSTA, Luiz Fernando

Expected date of degree: September 1996
Previous degrees: Electrical Engineering Degree, Master Computer Science (1985), (UFMG, Belo Horizonte, Brazil); DEA Microelectronics (1993), UJF, Grenoble, France
Research interests: Built-In Self-Test, self-checking circuits
Present employment: Brazilian government scholarship (CNPq)

Name: DAVEAU, Jean-Marc

Expected date of degree: 1997
Research interests: High level synthesis
Present employment: / 

Name: DING, Hong

Expected date of degree: June 1996
Previous degrees: Bachelor Computer Science & Engineering (1984), University of Xi'an Jiaotong (China)
Master Computer Science & Engineering (1990), University of Xi'an Jiaotong (China)
DEA Microelectronics (1992), UJF, Grenoble, France
Research interests: High-level synthesis
Present employment: / 

Name: GUILLEMOU, Christophe

Expected date of degree: 1996
Previous degrees: IDEEN Engineer
Research interests: Quality Assurance in aeronautics CAD-CAM at Dassault Aviation
Present employment: DASSAULT AVIATION (France)

Name: GUILLAUME, Philippe

Expected date of degree: May 1998
Previous degrees: DEA in Microelectronics, LIRMM, Montpellier, France
Research interests: Low power estimation and design in the area of high-level synthesis
Present employment: CIFRE Contract with SGS-Thomson
<table>
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<tr>
<th>Name</th>
<th>KAESTLI, Jacques</th>
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<td>Expected date of degree</td>
<td>1998</td>
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<td>EPFL Engineer</td>
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<td>Research interests</td>
<td>RAMs modelling applied to service industries</td>
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<td>Present employment</td>
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<td>Research interests</td>
<td>Built-In Self-Test, Self-Checking for VLSI circuits, CAD for testability</td>
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<td>MST in Sciences and Techniques for Computer Systems, 1991, UJF, Grenoble, France</td>
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<td>DEA in Microelectronics (1992), UJF, Grenoble, France</td>
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<td>Research interests</td>
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<td>1996</td>
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<td>Previous degrees</td>
<td>Microelectronic Engineer (1990), Paris-Sud University, Orsay, France</td>
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<td>Research interests</td>
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<td>Engineer (1991), Ecole Centrale de Lyon, France</td>
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<td>DEA &quot;Devices of integrated electronic&quot; (1991), INSA-UCBL-ECL</td>
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<td>Research interests</td>
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<td>Bachelor of Science, Physics (1989), St. Francis Xavier Univ. (Canada)</td>
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<td>Master of Electrical Engineering (1991), Carleton Univ. (Canada)</td>
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<td>Research interests</td>
<td>Retargetable code generation, embedded processors</td>
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<td>Canadian Government Scholarship</td>
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</table>
Name : MARCHIORO, Gilberto Fernandes

Expected date of degree : September 1997
Previous degrees : Computer Science degree (1987), Brazil
                  Master in Computer Science (1991), Brazil
Research interests : Hardware/Software Co-Design, High Level Synthesis
Present employment : CAPES (Brazil) scholarship

Name : MAROUFI, Walid

Expected date of degree : 1998
Previous degrees : Electric Engineering degree, ENIM, Monastir, Tunisia, 1994
                  DEA in Microelectronics, UJF, Grenoble, France, 1995
Research interests : High-level synthesis for testability
Present employment : French government scholarship

Name : MOHAMED, Firas

Expected date of degree : 1996
Previous degrees : DEA on Informatics (1993), Univ. of Montpellier (France)
Research interests : A.I. for analog circuits diagnosis
Present employment : Syrian Government Scholarship

Name : MONTALVO, Luis

Expected date of degree : Completed
Previous degrees : Engineer in Electronics and Telecommunications (1982),
                  National Polytechnique Institute, Quito, Ecuador
                  Master of Science in Computer Engineering (1986),
                  Ohio University, USA
Research interests : Computer Arithmetic
Present employment : Professor at the Electrical Engineering Department of the
                    National Polytechnique Institute, Quito, Ecuador

Name : MOUSSA, Imed

Expected date of degree : June 1996
Previous degrees : Engineer on Electronics and Telecommunications (1990),
                  National Engineers University, Tunisia
                  EA (Etudes Approfondies) in Telecommunications (1991),
                  National Engineers University, Tunisia
                  DEA on Electronics and Systems (1992), Clermont II Univ.,
                  France
Research interests : Computer Arithmetic on GaAs Technology
Present employment : /

Name : NACABAL, François

Expected date of degree : March 1998
Previous degrees : DEA in Microelectronics and Microinformatics (1993),
                  Univ. Paris VI
Research interests : Performance analysis of embedded software for DSP digital
                    signal processing
Present employment : CIFRE contract with SGS-Thomson
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<td>Research interests</td>
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<td>Research interests</td>
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<td>Research interests</td>
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<td>Research interests</td>
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<td>Previous degrees</td>
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<td>Research interests</td>
<td>:Advanced Quality Assurance modelling in ICs manufacturing</td>
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<td>Present employment</td>
<td>:SGS-Thomson (France)</td>
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</table>
Name : STEFANI Robert
Expected date of degree : Completed
Previous degrees : BULL Engineer
Research interests : Application of ISO 9000 to service industries strongly dependent on their information system
Present employment : /

Name : TCHIOUMATCHENKO, Vassily
Expected date of degree : June 1999
Previous degrees : DEA in Microelectronics (1995), Engineering degree, Technical University of Sofia, Bulgaria
Research interests : Synthesis for standard cell and FPGA
Present employment : Assistant Professor at Technical Univ. of Sofia, Bulgaria

Name : TOUATI, Mohamed Hédi
Expected date of degree : Completed
Previous degrees : DEA degree (1992), USTI-LIRMM, Montpellier, France
Research interests : Test and diagnosis of partial boundary scan boards
Present employment : /

Name : VACHER, André
Expected date of degree : June 1996
Previous degrees : DEA in Microelectronics (1992), UJF, Grenoble, France
- Master degree - Electronic, Electrical Engineering and Automatic - Scientific and Medical University, Grenoble, France
Research interests : Integrated circuits for calculation of Fast Fourier Transform
Present employment : French State employee (CNRS, Laboratory of Cristallography), retraining period

Name : VALDERRAMA, Carlos Alberto
Expected date of degree : June 1997
Previous degrees : Electronic Electrical Engineer (1989), National Univ. of Cordoba (Argentina); Master of Science degree (1993), Federal Univ. of Rio de Janeiro (Brazil)
Research interests : System level synthesis, codesign
Present employment : CNPq (Brazil) scholarship

Name : VARGAS, Fabian Luis
Expected date of degree : Completed
Research interests : Radiation hardened systems for space applications, current testing for CMOS circuits, DFT for RAMs.
Present employment : CPGCC-UFRGS, Porto Alegre - RS , Brazil
<table>
<thead>
<tr>
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<td>Research interests</td>
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<td></td>
<td>for sensor-based microsystems</td>
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<td>Present employment</td>
<td>Scholarship from Colombian government</td>
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<td>DEA Microelectronics (1993), UJF, Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>Linking high level synthesis (AMICAL) with industrial CAD systems</td>
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<tr>
<td>Present employment</td>
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</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>VINCI DOS SANTOS, Filipe</th>
</tr>
</thead>
<tbody>
<tr>
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<td>September 1997</td>
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<tr>
<td></td>
<td>Federal University of Rio de Janeiro, Brazil</td>
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<tr>
<td>Research interests</td>
<td>Radiation hardened circuits, on-line analog self-test, integrated detectors</td>
</tr>
<tr>
<td>Present employment</td>
<td>CAPES (Brazil) scholarship</td>
</tr>
</tbody>
</table>
IV-2 TIMA network and computer equipment

IV-2.1 Computer equipment

This equipment is made up of servers, workstations, X terminals, and personal computers. Laser printers are also available, as well as other peripherals like CD-ROM and Hexabyte drivers. The list follows:

**Server**:
1 Sparc SS20 (Sun)

**Workstations**:
2 Sparc SS10/30
2 Sparc IPC (Stn)
1 Sparc IPX (Sun)
1 Sparc I+ (Sun)

**Micro Computers**:
1 Mac+ (Apple)
1 Classic II (Apple)
4 Mac II (Apple)
5 Mac IIci (Apple)
2 Mac LC (Apple)
6 Mac LC III (Apple)
1 Performa 630 (Apple)
1 Mac LC 630 (Apple)
1 Power Mac 6100/60 (Apple)
1 Power Mac 7200/90 (Apple)
1 PowerBook 160 (Apple)
1 PowerBook 170 (Apple)
1 PowerBook 180 (Apple)
2 PowerBook 540 (Apple)
1 Z433D (Zenith Data System)
2 PC ASC

**X Terminals**:
1 NCD 19 (NCD)
4 NCD 19r (NCD)
1 TATUNG 17 (TATUNG)
5 NCD 15b (NCD)
15 NCD 15r (NCD)

IV-2.2 Network wiring and topology

In summer 1992, the network has been completely restructured, physical support (wiring) and topology. The thick Ethernet (10b5) bus has been replaced by a star topology based on Unshielded Twisted Pair (IEEE 802.3/10bT) Ethernet wiring network. The AppleTalk network has been also restructured: a star topology PhoneNet network on Unshielded Twisted Pair has replaced the former LocalTalk bus. Apart from its evolutive feature, this new wiring allows each room of the laboratory to be indifferently connected to any kind of existing resources (Appletalk/PhoneNet, Ethernet/10bT, RS232 server/concentrator serial lines), through RJ45 connectors.
IV-2.3 Network equipment

The new wiring and topology choice has implied the acquisition of some active network equipments, for both Ethernet and Appletalk/PhoneNet networks, and for their interconnection. This equipment is detailed in the following:

3 SNMP Hubs (David Expressnet from David Systems)
2 MR9T HUB (Cabletron)
1 Ethernet-Appletalk Gateway (GatorBox from Cayman)
1 PhoneNet StarController (from Farallon)
AUI/10bT Micro Transceivers (Allied Telesys)
PhoneNet StarConnectors (from Farallon)

IV-2.4 Interconnections, protocols, and services

TIMA network is interconnected with all other laboratories and schools of Felix Viallet site (downtown) with optic fiber wiring via a Cisco Ethernet router. This Router also allows this site to be connected to the ARAMIS network ("Association Rhône-Alpine des Moyens d'Interconnexion Scientifique" : the Rhône-Alpes region branch of French national scientific research network), through French Telecoms specialized lines (2 Mb/s). The main used protocol is Internet. This makes TIMA able to reach (and be reached by) any site in the world. Full Internet services are available (telnet, ftp, electronic mail, Usenet news,...).

IV-2.5 Interconnection schemas

Three schemas are given in the following pages in order to illustrate TIMA network and its external interconnections. The first schema (TIMA NETWORK) illustrates our own network and its link to one of the Ethernet router lines. The second schema (INPG - Site Viallet) - reprinted by courtesy of Claire Rubat du Mérac, INPG network responsible - shows how all of the laboratories (including TIMA) and schools of Felix Viallet site are interconnected, and how they are connected to ARAMIS network. The last schema (ARAMIS network) - reprinted by courtesy of Pierre Laforgue, IMAG network responsible, and the CICG - gives an overview of the different components of ARAMIS network.

IV-2.6 Contacts

Network, Server/WStations, MacIntoshes: Richard Pistorius (Richard.Pistorius@imag.fr)
IV-3 Financial resources

Some data are given below on financial aspects. They are provided for 1989-1995 budget years, to allow comparisons.

In 1989, the budget of the Laboratory has been 9 118 kFF (excluding VAT). This amount does not include salaries of government employees, like CNRS researchers and Professors.

This budget comes from research funds provided by CNRS or Universities (INPG and UJF), from contracts signed with industrial firms or CEC, and from "exceptional" funds or "exceptional" invoices (omitted for example against services). Those funds are accounted by either CNRS, or INPG or UJF. The Table XV gives the distribution, and the Figure 50 represents it. It is to be noted that the input for contracts represent the total amount of the contracts which are signed in 1989, even if the contract will last for several years.

The contractual part represents approx. 80 % of the budget in 1989. The Table XVI gives the list of contracts signed in 1989. The CEC part represents approx. 80 % of the contracts.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>182</td>
<td>8</td>
<td>290</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>140</td>
<td>705</td>
<td>-</td>
<td>845</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>569</td>
<td>239</td>
<td>-</td>
<td>808</td>
</tr>
<tr>
<td>Contracts signed in 1989</td>
<td>335</td>
<td>6 840</td>
<td>-</td>
<td>7 175</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>1 144</strong></td>
<td><strong>7 966</strong></td>
<td><strong>8</strong></td>
<td><strong>9 118</strong></td>
</tr>
</tbody>
</table>

TABLE XV - Budget 1989 (kFF, excluding VAT)
Figure 50 - Budget 1989

<table>
<thead>
<tr>
<th>Contract</th>
<th>Amount</th>
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<tbody>
<tr>
<td>CEC EUROCHIP</td>
<td>4,293</td>
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<tr>
<td>CEC ASICS</td>
<td>1,853</td>
</tr>
<tr>
<td>SGS - Thomson</td>
<td>579</td>
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<tr>
<td>CSEE</td>
<td>115</td>
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<tr>
<td>GCIS</td>
<td>335</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>7,175</strong></td>
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</table>

TABLE XVI - Contracts signed in 1989 (kFF, excluding VAT)
In 1990, the budget has been 8,582 kFF (excluding VAT). The Table XVII gives the distribution, and the Figure 51 represents it. Again, the input for contracts represents the total amount of contracts signed in 1990, even if those contracts last for several years.

In 1990, the contractual part represents approximately 43% of the budget. The Table XVIII gives the list of contracts signed in 1990.

<table>
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<tr>
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<th>UJF</th>
<th>Total</th>
</tr>
</thead>
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<tr>
<td>Research funds</td>
<td>100</td>
<td>162</td>
<td>3</td>
<td>265</td>
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<tr>
<td>Exceptional funds</td>
<td>210</td>
<td>3404</td>
<td>-</td>
<td>3,614</td>
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<tr>
<td>Exceptional invoices</td>
<td>766</td>
<td>210</td>
<td>-</td>
<td>976</td>
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<tr>
<td>Contracts signed in 1990</td>
<td>-</td>
<td>2782</td>
<td>-</td>
<td>3,727</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td>2,196</td>
<td>6,558</td>
<td>-</td>
<td>8,582</td>
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</table>

**TABLE XVII - Budget 1990 (kFF, excluding VAT)**

![Figure 51 - Budget 1990](image-url)
<table>
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<th>Contract</th>
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<tbody>
<tr>
<td>CNES</td>
<td>500</td>
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<td>TMS</td>
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<td>MATRA ESPACE (CNES)</td>
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<td>IBM</td>
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<td>CNES</td>
<td>150</td>
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<td>GCIS</td>
<td>945</td>
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<td>MIAT (JESSI)</td>
<td>1,315</td>
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<tr>
<td><strong>Total</strong></td>
<td><strong>3,727</strong></td>
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</tbody>
</table>

TABLE XVIII - Contracts signed in 1990 (kFF, excluding VAT)

The key issue when comparing data for 1989 and for 1990 is that the CEC EUROCHIIP contract is financially important for 1989. In 1990, the part of industrial contracts has been increased. Those data are nevertheless partially sounded, because of the criterion consisting in account a contract once, the year it is signed.
In 1991, the budget has been 9,322 kFF (excluding VAT). The Table XIX gives the distribution, and the Figure 52 represents it. In 1991, the contractual part represents approximately 44%. The CEC part represents 60% through ESPRIT Basic Research, and the JESSI part represents 38%. The Table XX gives the list of contracts signed in 1991.

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<tr>
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<td>Contracts signed in 1991</td>
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<td>-</td>
<td>4,138</td>
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<td><strong>TOTAL</strong></td>
<td>2,696</td>
<td>6,626</td>
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<td>9,322</td>
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**TABLE XIX - Budget 1991 (kFF, excluding VAT)**

![Figure 52 - Budget 1991](image)
<table>
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<th>Contract</th>
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<tr>
<td>CEC ASICS</td>
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<td>CEC EUROCHIP</td>
<td>2352</td>
</tr>
<tr>
<td>HEWLETT PACKARD</td>
<td>50</td>
</tr>
<tr>
<td>JESSI MICE / AC 6</td>
<td>855</td>
</tr>
<tr>
<td>JESSI MICE / AC 11</td>
<td>727</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td><strong>4138</strong></td>
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</table>

**TABLE XX - Contracts signed in 1991 (kFF, excluding VAT)**

In 1992, the budget has been 12,118 kFF (excluding VAT). The **Table XXI** gives the distribution, and the **Figure 53** represents it. In 1992, the contractual part represents approximately 54%. The CEC part represents 68% through ESPRIT Basic Research, and the JESSI part represents 32%. The **Table XXII** gives the list of contracts signed in 1992.

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<tr>
<td>Research funds</td>
<td>208</td>
<td>147</td>
<td>-</td>
<td>355</td>
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<td>160</td>
<td>2370</td>
<td>-</td>
<td>2530</td>
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<tr>
<td>Exceptional invoices</td>
<td>2511</td>
<td>116</td>
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<td>2627</td>
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<td>-</td>
<td>6606</td>
<td>-</td>
<td>6606</td>
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<td><strong>TOTAL</strong></td>
<td><strong>2879</strong></td>
<td><strong>9239</strong></td>
<td>-</td>
<td><strong>12118</strong></td>
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**TABLE XXI - Budget 1992 (kFF, excluding VAT)**
Figure 53 - Budget 1992

<table>
<thead>
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<th>Contract</th>
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<tr>
<td>CEC EUROCHIP</td>
<td>4 484</td>
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<tr>
<td>CEC ARCHIMEDES</td>
<td>712</td>
</tr>
<tr>
<td>JESSI MICE / AC 6</td>
<td>880</td>
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<tr>
<td>JESSI MICE / AC 11</td>
<td>404</td>
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<tr>
<td>CEC FASED</td>
<td>126</td>
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<td></td>
<td>6 606</td>
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TABLE XXII - Contracts signed in 1992 (kFF, excluding VAT)
In 1993, the budget has been 17,403 kFF (excluding VAT). The Table XXIII gives the distribution, and the Figure 54 represents it. In 1993, the contractual part represents approximately 64%. The CEC part represents 61%, and the JESSI part represents 36%. The Table XXIV gives the list of contracts signed in 1993.

<table>
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<tr>
<td>Research funds</td>
<td>166</td>
<td>568</td>
<td>-</td>
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<td>171</td>
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<td>2492</td>
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<tr>
<td>Exceptional invoices</td>
<td>2859</td>
<td>247</td>
<td>-</td>
<td>3106</td>
</tr>
<tr>
<td>Contracts signed in 1993</td>
<td>99</td>
<td>10972</td>
<td>-</td>
<td>11071</td>
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<td><strong>TOTAL</strong></td>
<td><strong>3295</strong></td>
<td><strong>14108</strong></td>
<td>-</td>
<td><strong>17403</strong></td>
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</table>

**TABLE XXIII - Budget 1993 (kFF, excluding VAT)**

**Figure 54 - Budget 1993**
<table>
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<tr>
<td>CEC / EUROCHIP</td>
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<tr>
<td>CEC / NSF - CLC</td>
<td>325</td>
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<tr>
<td>CEC / NSF - NDIMST</td>
<td>119</td>
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<tr>
<td>CEC / COPERNICUS 93 n°9093</td>
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<tr>
<td>CEC / ARCHIMEDES</td>
<td>915</td>
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<td>CEC / HCM - GARDEN</td>
<td>137</td>
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<td>CEC / CHIPSHOP</td>
<td>743</td>
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<td>CEC / EEMCN</td>
<td>73</td>
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<td>CEC / EDAC-EUROASIC 93-94</td>
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<td>MIPTCE / JESSI AC 6</td>
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</tr>
<tr>
<td>MIPTCE / JESSI AC 8</td>
<td>1 860</td>
</tr>
<tr>
<td>MIPTCE / JESSI AE 11</td>
<td>414</td>
</tr>
<tr>
<td>SGS-THOMSON / JESSI AC8</td>
<td>801</td>
</tr>
<tr>
<td>CNET / SOLIST</td>
<td>350</td>
</tr>
<tr>
<td></td>
<td>11 071</td>
</tr>
</tbody>
</table>

**TABLE XXIV** - Contracts signed in 1993 (kFF, excluding VAT)
In 1994, the budget has been 19,253 kFF (excluding VAT). The Table XXV gives the distribution, and the Figure 55 represents it. In 1994, the contractual part represents approximately 74%. The CEC part represents 52%, and the JESSI part represents 32%. The Table XXVI gives the list of contracts signed in 1994.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>185</td>
<td>518</td>
<td>0</td>
<td>0</td>
<td>703</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>40</td>
<td>1824</td>
<td>0</td>
<td>0</td>
<td>1864</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1935</td>
<td>454</td>
<td>0</td>
<td>0</td>
<td>2389</td>
</tr>
<tr>
<td>Contracts signed in 1994</td>
<td>0</td>
<td>13,431</td>
<td>565</td>
<td>300</td>
<td>14,296</td>
</tr>
<tr>
<td>TOTAL</td>
<td>2,160</td>
<td>16,227</td>
<td>565</td>
<td>300</td>
<td>19,252</td>
</tr>
</tbody>
</table>

**TABLE XXV - Budget 1994 (kFF, excluding VAT)**

![Budget 1994 Pie Chart](image)
<table>
<thead>
<tr>
<th>Company</th>
<th>Amount (kFF, excluding VAT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>3,866</td>
</tr>
<tr>
<td>CEC / BARMINT</td>
<td>799</td>
</tr>
<tr>
<td>CEC / COPERNICUS THERMINIC</td>
<td>565</td>
</tr>
<tr>
<td>CEC / COPERNICUS FUTEC</td>
<td>299</td>
</tr>
<tr>
<td>CEC / AMATIST</td>
<td>1,092</td>
</tr>
<tr>
<td>CEC / GRASS</td>
<td>142</td>
</tr>
<tr>
<td>CEC / CHIPSHOP</td>
<td>701</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC 6</td>
<td>1,103</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC 8</td>
<td>2,887</td>
</tr>
<tr>
<td>MIPTCE / JESSI AE 11</td>
<td>526</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>570</td>
</tr>
<tr>
<td>SGS-THOMSON / CIFRE</td>
<td>90</td>
</tr>
<tr>
<td>CNET / PSYCOS</td>
<td>1,200</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>300</td>
</tr>
<tr>
<td>DRET / ASTER INGENIERIE</td>
<td>156</td>
</tr>
</tbody>
</table>

**Total** | 14,296 |

**TABLE XXVI** - Contracts signed in 1994 (kFF, excluding VAT)
In 1995, the budget has been 15,018.00 kFF (excluding VAT). The Table XXVII gives the distribution, and the Figure 56 represents it. In 1995, the contractual part represents approximately 37 %.
The CEC part represents 18 %, and the JESSI part represents 65 %.
The Table XXVIII gives the list of contracts signed in 1995.

<table>
<thead>
<tr>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>235</td>
<td>600</td>
<td>62</td>
<td>0</td>
<td>897</td>
</tr>
<tr>
<td>17</td>
<td>2010</td>
<td>0</td>
<td>0</td>
<td>2027</td>
</tr>
<tr>
<td>5089</td>
<td>1381</td>
<td>0</td>
<td>0</td>
<td>6470</td>
</tr>
<tr>
<td>0</td>
<td>4994</td>
<td>0</td>
<td>630</td>
<td>5624</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>8975</strong></td>
<td><strong>62</strong></td>
<td><strong>630</strong></td>
<td><strong>15,018</strong></td>
</tr>
</tbody>
</table>

TABLE XXVII - Budget 1995 (kFF, excluding VAT)

Figure 56 - Budget 1995
<table>
<thead>
<tr>
<th>Contract Code</th>
<th>Amount (kFF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / CHIPSHOP</td>
<td>350</td>
</tr>
<tr>
<td>CEC / KIT 106 &quot;ARCOS&quot;</td>
<td>124</td>
</tr>
<tr>
<td>CEC / KIT 107 &quot;ATAME&quot;</td>
<td>110</td>
</tr>
<tr>
<td>CEC / OMI</td>
<td>442</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC 6</td>
<td>808</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC 8</td>
<td>1788</td>
</tr>
<tr>
<td>SGS-THOMSON / JESSI AE 102/103</td>
<td>1032</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>340</td>
</tr>
<tr>
<td>AEROSPATIALE</td>
<td>300</td>
</tr>
<tr>
<td>SODERN</td>
<td>330</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>5624</strong></td>
</tr>
</tbody>
</table>

**TABLE XXVIII** - Contracts signed in 1995 (kFF, excluding VAT)
If we consider 1989, 1990, 1991, 1992, 1993, 1994, 1995 together, then we get the global data given in Table XXIX and represented by Figure 57. Such data are more representative of the reality. Now, we get a part of the contracts which is 58% of the budget, and the CEC part is 56%. JESSI accounts for 28%, but JESSI activities are reported from 1991 only.

![Pie chart showing budget distribution]

**Figure 57 - Budget 1989 - 1995**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>3 509</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>16 322</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>18 345</td>
</tr>
<tr>
<td>Contracts</td>
<td>52 637</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>90 813</strong></td>
</tr>
</tbody>
</table>

**TABLE XXIX - Budget 1989-1995 (kFF, excluding VAT)**
V - COOPERATIVE ACTIVITIES

V-1 Contracts

Public Institutions:

MAE, MESR (CNFM), MIPTCE (SERICS), France Telecom (CNET).

Industrial contracts:

SGS THOMSON, AEROSPATIALE, SODERN, MENTOR GRAPHICS, ASTER.

V-2 European Projects

V-2.1 Summary

In the past, members of the Laboratory participated to CEC Projects like CASCADE and CVT. Presently, or recently, the Laboratory participates or has been participating to the following projects:

ESPRIT PROJECTS:

ESPRIT I : ADVICE, AIDA, SPAN
ESPRIT II BASIC RESEARCH : ASCIS, EUROCHIP
ESPRIT III BASIC RESEARCH : ARCHIMEDES, FASED, BARMINT, AMATIST, GRASS
ESPRIT III RESEARCH AND DEVELOPMENT : CHIPSHP
ESPRIT III KIT : ARCOS, ATAME
ESPRIT IV OMI : IUN2, EUROMIC

CEC/NSF Cooperation: NDIMST, CSLS

JESSI PROJECTS:

JESSI : AC6, AE11, AC8

COMETT PROJECTS:

COMETT I : COMET
COMETT II : EUROSYSTEMS, EPIQCS
EUREKA PROJECT:

EUREKA : MITHRA

TEMPUS PROJECTS:

TEMPUS

- Advanced JEP for Microelectronics Design Methodology,
- MECC,
- Initiation of Formal Training in CAEE in Romanian Universities,
- Computer-aided Methods and Technical Management in Electrical Engineering Education
- Digital System Design Based on PLD-Technology
- Education for Quality Control in Electrical Industry
- Postgraduate Education in ASIC Design

COPERNICUS (PECO) PROJECTS:

COPERNICUS (ex PECO)

- EDAC-EAST : Attendance of Central and Eastern European Engineers and Researchers to the EDAC Conference
- Design of VLSI self-checking digital circuits
- Developing design automation technique in ASIC and VLSI Design
- CAD/CAT tools integration for sensor-based microsystems
- Dependability Analysis of Complex Electronic Components and Systems
- East European Microelectronics Cooperation Network of support and competence centres of Central and Eastern European countries
- Functional test generation and diagnosis
- EUROEAST: Extension of EUROCHIP services to Central and Eastern European Countries
- THERMINIC: New Methods for Thermal Investigation of Integrated Circuits

HUMAN CAPITAL MOBILITY PROJECT:

HCM : GARDEN

LATIN AMERICA HIGHER EDUCATION:

ALFA

- HUERTA: Higher University Education and Research Training Action

Y-2.2 Details

ESPRIT-I

ADVICE

(CSELT, British Telecom, CNET, TIMA/INPG, Trinity College), 1984-1989 (ADVICE I)

Automatic Design Validation of Integrated Circuits using Electron Beam
Currently, the e-beam probe is the only viable method for obtaining timing resolution and voltage information from the internal nodes of single and multilevel VLSI circuits. However, the systems available at present are essentially manually operated and the procedure for fault diagnosis can be extremely time consuming. By making use of CAD software, the ADVISE project will enable the diagnostic investigation to be automated, thereby significantly reducing the circuit development time.

The Laboratory is mainly involved in CAD-EBT interface, controllability using e-beam and diagnostic tools.

AIDA

(SIEMENS, ICL, SGS THOMSON, TIMA/INPG, University of Manchester), 1986-1990

Advanced Integrated-circuit Design Aids

The objective of the project is to master the complexity of VLSI chips (more than one million transistors within the next few years) by obtaining a drastic improvement in design methods. CAD tools, new methods and concepts will be defined, proved on experimental software and finally developed into industrial tools integrated into the existing CAD environments of the partners. AIDA intends to explore the application of modern programming techniques and knowledge-base engineering to CAD tool development. It will constitute a design assistant that proposes solutions rather than merely records and validates the designer's ideas. This will allow the designer to apply his creativity where it is most efficient, leading to improved design quality. Modern programming techniques will be applied (e.g. those developed for expert systems to VLSI-CAD tools).

More specifically, the Laboratory is in charge of exploring the design of structured control-sections and/or structured datapaths in order to make them self-checking and give them built-in testability.

SPAN

(THORM-EMI, CIMSA-SINTRA, CTI, INESC, PCS, TIMA/INPG, University College London), 1987-1990

Parallel Computer Systems for Integrated Numeric and Symbolic Processing

The objective of the Project is to investigate programming languages and parallel architectures for the integration of symbolic and numeric processing, and to develop a common virtual machine. The project is organized in distinct layers: application software packages, high level languages and tools, the "virtual machine" kernel system, and parallel architectures.

The Laboratory is specifically involved in the architecture of a Prolog system, integrating numeric processing.

At the time of writing this report, proposals are being submitted to the ESPRIT II Programme, mainly on fault-tolerant, real time, embedded architectures.
**ESPRIT-II Basic Research**

**ASCIS**


Architecture Synthesis for Complex Integrated Systems

The research in ASCIS is aimed at addressing future ICs which will contain the equivalent in logic of 16 million memory cells. Currently complex systems are mapped into Silicon starting from an architectural description level. However, the bottleneck in such mega-chip designs lies not in realizing the layout from this register-transfer level description, but in mapping the behaviour intended into a suitable architecture. Therefore, in order to fully exploit the integration complexity of future fabrication technologies it is crucial to provide a specification at the highest system level.

Problems related to this change of specification level are fundamental in nature.

The topics to be addressed are the system definition, the system partitioning, the mapping of subsystems into architectures, and the architectural synthesis of control sections.

The Laboratory will focus on behavioral partitioning, architectural exploration and cooperative datapaths.

**EUROCHIP**

(GMD, CMP, IMEC, University of Lyngby, RAL), 1989-1994

Service organisation of the VLSI Design Action

This service will provide European Universities with a number of services including access to chip manufacture and procurement of additional workstations, test equipment and CAD software.

CMP is a member of the Service Organisation.

**ESPRIT-III Basic Research**

**ARCHIMEDES**

(INPG/TIMA, Univ. of Karlsruhe, Montpellier, Hannover, Bologna, Barcelona, & INESC) 1992-1995

ARCHItechntural MEthodologies for aDvanced tEsting of VLSI Systems.

This project takes place in the framework of: "Algorithms for design methodologies for complex circuits and digital optical systems" (area V - Basic Research).

The objective is to develop methodologies in order that the advances allowed by the technology and the use of powerful CAD tools will not be jeopardized by the testing bottleneck.

The project goes deeper in the research by considering:
- architectural synthesis
- on-line and off-line testing together
- built-in test of analog parts
- defect modeling, from process simulation to circuit simulation
- IC defects-based back annotation of circuit faults
- combined detection techniques (voltage and current testing)
- IC defects-based fault models for analogue building blocks
- advanced fault simulation of CMOS compatible designs (BiCMOS)
- optimized built-in test generation for BIST
- automatic design rule checking for self-checking circuits.

FASED

(IMS, INPG/TIMA, Politecnico di Milano)
1992-1994

Failsafe Integrated Digital Electronics with Semicustoms

Electronic components are increasingly being employed in safety critical systems. The introduction of application specific VLSI circuits to these areas is hampered by long design times and consequently high cost of self-checking and fail-safe integrated circuits. In this proposed basic research action, these issues are to be addressed by extending the use of semicustom technologies to fail-safe circuits.

BARMINT

(LAAS Toulouse, INPG/TIMA, INPG/TIMC, TH Darmstadt, TU Budapest, CNM Bellaterra, LCMM Barcelona, NMRC Cork, TU Lodz)
1994-1997

BAsic Research for Microsystems INTegration

Microsystems that integrate data processing along with sensors and actuators will face an important development during the next years. The objective of the BARMINT project is to participate to the development of microsystems along three main axes: a) the tools for top-down design that bring methods for developing microsystems in a way similar to present ASICs, b) the technological compatibilities between silicon based VLSI, micromachined silicon in micromechanics, integrated optics obtained by micromachining of silicon or of special polymers, and chemical sensors with membranes, c) the assembly operations that focus on typical compatibility problems for including various components within a single multichip microsystem.

AMATIST

(CNM Sevilla, MESA Institute - Univ. of Twente, INPG/TIMA, Univ. of Cantabria, Univ. of Lancaster, Univ. of Pavia)
1994-1997

Analogue & Mixed-signal Advanced Test for Improving System-level Testability

This project intends to develop new concepts enabling to improve the performance of mixed-signal integrated systems through the incorporation of on-line test functionality. This will be carried out by addressing three different issues: a) the introduction of circuit architectures which can be used to ensure a continuous signal monitoring during the system field operation, b) the development of Design-For-Testability and off-line test generation methods especially tailored to the systems under study, and c) the validation of the new architectures and methods by using them to implement actual integrated applications.
GRASS (Working Group)
(Univ. de Las Palmas de Gran Canarias, INPG/TIMA, Middlesex University, Techn. Univ. of Denmark, EPFL, Fraunhofer-Gesellschaft Erlangen)
1994-1997

Gallium arsenide Research action on ASIC Synthesis

The emerging commercial markets in the communication, computer, automotive and broadcast industries will produce an increase of more than 30% every year in both the digital and analogue GaAs device markets. The aim of this project is to improve the knowledge of European researchers on mixed mode Gallium Arsenide VLSI integrated circuit design, and to generate facilities for allowing the reliable design of such circuits. Effort is targeted for fast digital signal processing and other very high speed applications such as broadband telecommunications, hardware accelerators and workstations. It aims at delivering a design environment with the same level of performance in quality and design time for GaAs as is available for silicon to ASIC designers in Telecom and Information Processing fields.

ESPRIT-III Research and Development

CHIPSHOP

(SCME, FhG-IIS, LETI, CMP, CNR-PF, IAM, GAME, INESC, INTRACOM, ElektronikCentralen, CNM, Nordic VLSI, ERA, ULVC)
1992-1994

A low-cost IC prototyping production service for small and medium sized enterprises.

CHIPSHOP is a pan-European initiative supported by the Commission of the European Communities in the framework of the ESPRIT programme to provide MPW services to SMEs from EC and EFTA countries, in connection with the JESSI-SMI Project and with Special Actions in Greece, Portugal, Italy and Spain. Chip fabrication is carried out by 5 different foundries and testing interfaces: CMP in France, Fraunhofer-Institute for Integrated Circuits (FhG-IIS) in Erlangen in Germany, CNM in Spain, Nordic VLSI in Norway, ElektronikCentralen in Denmark and CSATA in Italy. CMOS and BiCMOS technologies will be offered to support analog, digital, mixed, high voltage and high frequency applications. CHIPSHOP offers more services besides prototype fabrication: testing, small volume production, CAD software, FPGA migration.

ESPRIT-III KIT ("Keep-In-Touch")

ARCOS

(IMEC, INPG/TIMA, University of Sao Paulo)
1995-1997

ARChitectural synthesis of COMplex Systems on silicon

The main goal of the project is to assess, optimise and transfer a new design methodology for complex systems on ASIC's by using high level synthesis techniques. This goal will be
reached by selecting several relevant applications, defined by the non-EU site and perform the complete design process as a driving test vehicle for the software developments of the high level synthesis systems CATHEDRAL and AMICAL. During this project, experts of different fields will work together, i.e. algorithm developers, hardware architects and CAD software specialists. It is clearly understood that today the combination of expertise from these three gravitation centres is what makes human designer teams (and their designs) successful. At the start of this project, two powerful high level synthesis environments are made available by the EU-sites. These include CATHEDRAL, a high level synthesis environment for the realisation of data flow dominated DSP algorithms and AMICAL, a high level synthesis environment for architecture synthesis of control oriented applications. The research activities proposed in this project will produce new tools that will be integrated in the existing environment, leading to more powerful compilers. These new activities result from the feedback that is collected from application studies that will be undertaken by the non-EU site.

ATAME

(IMEC, INPG/TIMA, Polytechnical Univ. of Madrid, Institute of Microelectronics - Singapore National University)
1995-1997

Advanced Telecom And Multimedia design technology Environment

The activities in this project are aimed at improving the design productivity for the implementation of telecommunication and multimedia systems in hardware and software. Due to the competitiveness in these application fields, reducing both the design time as well as the risk of re-design is of key importance. The goal of the project is to apply advanced design technology tools to new product developments, such that optimized designs can be delivered in a minimal time. Thereby the key point is that it is not possible to use a single software technique to accomplish every task, but to achieve the closest possible integration of powerful, specialized software design tools.

ESPRIT-IV OMI

IUN2

(CMP, UNED, Archimedes, IMEC, OMIMO, Sussex University, TODITEC and UPM)
1995-1996

Inter University Network

The IUN2 project is part of a OMI global dissemination strategy that connects Universities all over the world interested in the OMI activities. The partners will achieve this goal using their strong links with the academic world. Up to now more than 300 European institutions are members of the IUN2 project. This network will be extended to non-EU European Countries as well as the rest of the world. The partners will promote the use and fast dissemination of technologies emerging from the OMI initiative.

EUROMIC

(CMP, FhG, IMEC, OMIMO, Sussex University and UPM)
1996-1997
EUROpean OMI Centres

The EUROMIC project aims to act as a gateway to foster relationships between all members of the OMI community. The goal of this project is to allow European industries to fabricate their integrated systems at a reduced cost in an easy and fast way. To achieve it they will set up a network of OMI user support nodes which provide services to meet the needs of SMEs including training, design support, licensing issues, manufacturing and promotion of best practices in application systems design. The network will act as a brokerage service between users and suppliers of microprocessor technology.

CEC/NSF Cooperation

NDIMST

(University of Texas at Austin, INPG/TIMA)
1993-1995

New Directions In Mixed Signal Test

The objective of the proposed cooperation is to find new approaches to deriving high quality tests for mixed-signal circuits. Much of the work in test has been focused on digital circuits. With the increasing levels of integration, and applications such as automotive, notebook computers, and communications, analog and digital functions are being integrated on a single chip. Appropriate fault models and efficient test generation algorithms need to be generated for mixed-signal circuits if we are to produce defect-free chips, and on-line detection.

CSLS

(University of California at Irvine, INPG/TIMA)
1994

Circuit and System-Level Synthesis

The goal of this cooperation is to develop a global solution for behavioral and System-Level Synthesis. This cooperation will be based on the integration of SpecChart, the system-level synthesis tool developed at Irvine, and AMICAL, the behavioral synthesis tool developed at Grenoble. This integration will produce a unified synthesis environment for circuit and system design.

JESSI


Industrial partners :
Philips, Eindhoven/Hamburg
Siemens, Munich
SNI, Munich
EZM, Villach
SGS Thomson, Grenoble
Thomson-CSF/TMS
Alcatel/Bell, Antwerp
Associated partners:
- University of Karlsruhe together with "Forschungszentrum-Informatik" in Karlsruhe
- University of Hannover
- Technical University of München
- University of Erlangen-Nürnberg
- TIMA/INPG
- Twente University of Technology, Enschede, The Netherlands
- Bennetts Associates, Southampton.


Industrial partners:
- Bosch, Reutlingen
- SGS-Thomson, Grenoble
- Siemens, München
- SEL-Alcatel, Stuttgart
- Porsche, Weinhach

Associated partners:
- University of Hannover
- TIMA/INPG

AC8: Integrating AMICAL within industrial CAD environment, 1993-1994

Industrial partners:
- AHL
- Bosch
- Bull
- Philips
- Siemens
- Siemens-Nixdorf
- SGS-Thomson
- Synthesia
- Thomson-TCS

Associated partners:
- TIMA/INPG

**COMETT I**

**COMET**

(IMEC, TIMA/INPG, Universities of Darmstadt, Limerick, Lyngby, Madrid), 1988-1990

Consortium for microelectronic training

This project is aimed at providing education on ASICs at several levels and for several interest groups, but especially for the SMIs in each country.
COMETT II

EUROSYSTEMS

(University of Darmstadt, IMEC, University of Lyngby, TIMA/INPG).

This project is a complete programme for advanced microelectronics system design fulfilling the future trends of European industry.

EPIQCS: MASTERS DEGREE SPECIALIZED IN QUALITY OF COMPLEX INTEGRATED SYSTEMS

(INPG, Imperial College of London, Universities of Darmstadt and Eindhoven)

This project aims at providing a Masters Degree in cooperation with 3 main academic partners and numerous industrial partners. The 4 platforms will be specialized in Software, Telecom, Hardware and Space.

EUREKA

MITHRA

(BROSSARD, BERTIN, ITMI, SEIV, LAMM, ELKRON, OLMAT, SEPA, EPFL, CERBERUS, TIMA/INPG), 1988-1990

MITHRA deals with integrated electronics for surveillance mobile robots. It is a project in which industrial firms from France, Italy and Switzerland are participating. Several research laboratories from INPG and LAMM at Montpellier are also participating. The experience of the Laboratory might be used to design circuits to replace several printed circuits boards.

TEMPUS

ADVANCED JOINT EUROPEAN PROGRAMME FOR MICROELECTRONICS DESIGN METHODOLOGY

(University of Darmstadt, Technical University of Budapest, IMEC, University of Lyngby, TIMA/INPG, Institute of Electron Technology of Warsaw)

This is a transeuropean programme on microelectronics.

MECC (Management, Electronics, Computer science)

This is a transeuropean programme on management, electronics, computer science.

INITIATION OF FORMAL TRAINING IN COMPUTER AIDED ELECTRICAL ENGINEERING IN ROMANIAN UNIVERSITIES

(TIM/A/INPG, ENSIEG/INPG, Univ. of Bucuresti, Bath, Genova, Cassino, Paris 6 & 11, Graz, EDF, Politecnico di Torino)

This is a transeuropean programme for the development of education capabilities at higher education level in applied sciences in engineering areas.

COMPUTER-AIDED METHODS AND TECHNICAL MANAGEMENT IN ELECTRICAL ENGINEERING EDUCATION

(Technical Univ. Budapest, Univ. Karlsruhe, Univ. Erlangen-Nürnberg, University College London, TIMA/INPG, Univ. of Pisa, Techn. Univ. of Delft, MOTOROLA GmbH, TEXAS INSTRUMENTS DEUTSCHLAND, HEWLETT PACKARD, DIGITAL EQUIPMENT, IBM)

This is a transeuropean programme for updating technical and technical-management studies.

DIGITAL SYSTEM DESIGN BASED ON PLD-TECHNOLOGY

(Technische Hochschule Darmstadt, TIMA/INPG, Tallinn Technical Univ.)

This is a transeuropean programme for introducing into university education the methodology and concepts of designing semicustom ASICs.

EDUCATION FOR QUALITY CONTROL IN ELECTRICAL INDUSTRY

(Technical Univ. of Brno, Czech Technical University of Prague, Technical Univ. of Ostrava, Leeds Metropolitan Univ., Bournemouth Univ., TIMA/INPG, Univ. of Hull)

The objective of this project is to upgrade the university education, new degree courses for Quality management, training courses, students and lecturers mobility.

POSTGRADUATE EDUCATION IN ASIC DESIGN

(Warsaw Univ. of Technology, Technical Univ. of Lodz, Univ. of Mining and Metallurgy of Krakow, TIMA/INPG, Technische Hochschule Darmstadt, Eindhoven Univ. of Technology, Helsinki Univ. of Technology)

Preparation of the teaching staff for a centre for postgraduate training in ASIC design.

COPERNICUS

COPERNICUS : Cooperation in science and technology with Central and Eastern European countries.

European Conferences, workshops and training seminars:
EDAC-EAST: ATTENDANCE OF CENTRAL AND EASTERN EUROPEAN ENGINEERS AND RESEARCHERS TO THE EDAC CONFERENCE

Mobility scheme for scientists:

DESIGN OF VLSI SELF-CHECKING DIGITAL CIRCUITS
(Stanislaw PIESTRAK, Technical University Wroclaw, Poland)

DEVELOPING DESIGN AUTOMATION TECHNIQUE IN ASIC AND VLSI DESIGN
(Tania VASSILEVA, Technical University Sofia, Bulgaria)

CAD/CAT TOOLS INTEGRATION FOR SENSOR-BASED MICROSYSTEMS
(Teodor CALIN, Polytechnical Institute of Bucharest, Romania)

DEPENDABILITY ANALYSIS OF COMPLEX ELECTRONIC COMPONENTS AND SYSTEMS
(Ioan BACIVAROV, Polytechnical Institute of Bucharest, Romania)

Pan European Scientific Networks:

EAST EUROPEAN MICROELECTRONICS COOPERATION NETWORK OF SUPPORT AND COMPETENCE CENTRES OF CENTRAL AND EASTERN EUROPEAN COUNTRIES


Joint Research Proposals:

FUNCTIONAL TEST GENERATION AND DIAGNOSIS (FUTEG)

(Technical University of Tallinn - Estonia, Kанныs University of Technology - Lithuania, Institute of Computer Systems Bratislava, Technical University of Budapest, INPG/TIMA, FhG-IIS-EAS Dresden)

1994-1997

The focus of the project is directed towards the investigation of functional and behavioral test generation and diagnosis at the system level. The different partners will put in common their expertises in this area, in order to provide different approaches to this topic. These approaches will be validated by experiments and comparatively analyzed. Finally, their integration into a combined methodology is intended. This project, which manpower is 25 persons-year, over a duration of 36 months, is expected to start in January 1994.
EUROPEAN: EXTENSION OF EUROCHIP SERVICES TO CENTRAL AND EASTERN EUROPEAN COUNTRIES

(GMD, CMP, DTH, IMEC, RAL, Polytechn. Bucharest, ITME Warsaw, Warsaw University, Silesian Tech. Univ., Slovak Tech. Univ.)

NEW METHODS FOR THERMAL INVESTIGATION OF INTEGRATED CIRCUITS (THERMINIC)

(Technical University of Budapest, Hungary, Technical University of Lodz, Poland, Technical University of Lviv, Ukraine, SEMILAB Budapest, Hungary, INPG/TIMA)

1995-1997)

One of the greatest challenges of our days in microelectronics are the overheating problems. The increase in the power density in integrated circuits, caused by the actual small features sizes, moreover the advent of 3D packages cause severe heat dissipation problems. This project intends to treat this problem in its complexity and approximate it in different ways, resulting in the development of new thermal monitoring methods and elements as well as new thermal investigation methods and tools.

HUMAN CAPITAL AND MOBILITY

GARDEN

(Univ. de Las Palmas de Gran Canarias, INPG/TIMA, PHILIPS Electr. Laboratories, Middlesex University, Techn. Univ. of Denmark, EIDG. Technische Hochschule at Zurich, Fraunhofer Institut für Angewandte Festkörperphysik at Freiburg, Fraunhofer Institut für Integrierte Schaltungen at Erlangen, GIGA at Brondby, Thomson CSF)

Gallium Arsenide Reliable Design ENVironment

This project aims at delivering a design environment with the same level of performance in quality and design time for GaAs as available for silicon, to ASIC designers in Telecom and Information Processing fields. This goal will be achieved by two actions. Firstly, a research and cooperation network: “The European Network on Gallium Arsenide VLSI Design”, will be established within the Human Capital and Mobility Programme of the European Community. Secondly, a research and development project will be launched again through the Human Capital and Mobility Programme, which will center cooperation between laboratories in the network and will provide mobility for advanced research and training at each other sites according to special capabilities and expertise.

LATIN AMERICA HIGHER EDUCATION (Amérique Latine Formation Académique (ALFA))

HUERTA

(Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil; Universidade Federal do Rio de Janeiro/COPPE, Rio de Janeiro, Brazil; Universidad del Valle/INTEDI, Cali, Colombia; Universidad Autonoma Metropolitana, Mexico, Mexico; Univ. Catholique de
Higher University Education and Research Training Action

This package concerns two projects, both proposed by the HUERTA network (Brazil, Colombia, Mexico, Belgium, France, Germany, Portugal). The B1 project, entitled "Design, Synthesis and Test of Digital Systems" aims at defining a mobility scheme for PhD and MSc students from Latin America, as well as providing high-level training sessions for Professors in order to disseminate the most recent information on technologies and tools related to the design, synthesis and test of digital systems. The B2 project, entitled "Synthesis of Testable Circuits and Systems", aims at defining common research projects related to high-level synthesis for testability, a current hot research topic. Both projects aim at facilitating the technology transfer between the EU and LA in the field of Microelectronics, which is crucial for the technological development of LA countries, expected to have a strong impact from the social and economical points of view. The three LA countries involved in the HUERTA network will constitute a kernel for scientific and technological information dissemination in the remaining of Latin America.

V-3 International cooperation agreements

The Laboratory is engaged in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations allow to remote researchers at the cooperative location for in-deep fruitful exchanges of results, to organize joint research and Workshops.

University of Texas at Austin, USA
This cooperation takes place in the framework of a project between NSF and ESPRIT with J. ABRAHAM on testing of integrated circuits, with a special emphasis on analog and mixed circuits.

University of California at Irvine, USA
This cooperation takes place in the framework of a project between NSF and ESPRIT with D. GAIJSKI, on statecharts and AMICAL relationships.

Ecole Polytechnique de Montréal, Canada
This cooperation takes place in the framework of a project sponsored by FCAR/GRIAO, with B. KAMINSKA, on testing of integrated circuits, with a special emphasis on analog circuits.

Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with R. REIS, on the automatic design of integrated circuits.

Universidade Federal do Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with A. MESQUITA, on high level synthesis and test of integrated circuits.

University of Washington at Seattle, USA
This cooperation takes place in the framework of the definition of the P1149.4 IEEE standard for the analog extension of the P1149.1 boundary scan, with M. SOMA who is chairing the working
group. The Laboratory is the European center of the distribution of documents (with Ecole Polytechnique Fédérale de Lausanne for Switzerland).

Ecole Nationale d'Ingénieurs de Monastir (ENIM), Monastir, Tunisia
This cooperation takes place in the framework of a project sponsored by the French ministry for education and research and the Tunisian ministry for research and technology, cooperation program which name is "Réseaux Formation-Recherche franco-tunisiens", with S. NASRI, on computer-aided design of communication-dedicated circuits.

Technical University of Budapest, Hungary
This cooperation takes place in the framework of BALATON, between France and Hungary. The project deals with thermal investigations of ICs and systems, with the Department of Electron Devices; V. SZEKELY and M. RENCZ. Renewal of this action has been approved for 1996.

Jožef Stefan Institute, Ljubljana, Slovenia
This cooperation takes place in the framework of PROTEUS, between France and Slovenia. The project deals with test and diagnostic of heterogeneous systems, with F. NOVAK. Renewal of this action has been approved for 1996.

Tomsk State University, Russia
This cooperation takes place in the framework of NATO linkage grants. Those grants allow short stays in NATO countries for foreign researchers.

Warsaw University of Technology
French-Polish scientific and technological cooperation joint projects for year 1996. This cooperation allows short and long visits to France and Poland.

V-4 National cooperation
A network of French Laboratories has been set up by the Ministry for Research and Education in the field of CAD for integrated circuits and systems. These Laboratories are CSI in Grenoble, ENST in Paris, IEMN in Lille (Villeneuve d'Ascq), LIRMM in Montpellier, MASI in Paris, and TIMA in Grenoble acting as the contractor to the Ministry. The goal of the network is to cooperate in the development of researches in CAD of analog and mixed-signal circuits, multi-technologies logic synthesis, hardware-software codesign, architectural synthesis, physical design and portable libraries, verification tools and CAD for microsystems.

V-5 International activities
This section gives an overview of national and international activities to which participated recently the members of the Laboratory.

Participation to Committees for Conferences and Workshops

- European Design for Testability Workshop: 1990 (Segovia), 1992 (Brugge), 1996 (Montpellier)
- European Solid-State Circuits Conference: 1986 (Delft), 1990 (Grenoble), 1995 (Lille)
- International Conference on Microelectronics: 1991 (Cairo), 1992 (Monastir), 1993 (Dahran)
- International Workshop on FPGAs and Applications: 1992 (Vienna), 1994 (Prague), 1996 (Darmstadt)
- European Workshop on Dependable Computing: 1989 (Toulouse)
- CEC CAVE (CAD for VLSI in Europe) workshops: 1983-1988
- Memory Testing: 1993-1995 (San Jose), 1996 (Singapore)
- Asian Test Symposium: 1992 (Hiroshima), 1993 (Beijing), 1994 (Osaka), 1995 (Bangalore), 1996 (Taiwan)
- High Level Synthesis Workshop: 1994 (Niagara Falls), 1995 (Cannes), 1996 (La Jolla)
- EuroDAC-EuroVHDL: 1994 (Grenoble), 1995 (Brighton), 1996 (Geneva)
- Workshop on Hardware-Software Codesign: 1994 (Grenoble)
- Simulation in Electronics: 1994 (Santander)
- Asia Pacific Conference on Hardware Description Languages: 1993 (Brisbane), 1994 (Toyoahashi), 1996 (Bangalore)
- International Conference on Probabilistic Safety Assessment and Management: 1991 (Beverly Hills), 1996 (Greece)
- European Safety and Reliability Conference: 1996 (Greece)
- 2nd International Conference on ASIC: 1996 (Shanghai)
- IEEE Multi-Chip Module Conference: 1995-1996 (Santa Cruz)
- Mixed-Signal Test Workshop: 1996 (Quebec)
- MCM Test: 1995-1996 (Napa Valley)
- SPIE Conference on Micromachining and Microfabrication: 1996 (Austin)
- Diseño de Circuitos Integrados y Sistemas: 1996 (Barcelona)
- Microsystem Design for High Reliability and High Dependability Application: 1996 (Ambleside)
- Low Dimensional Structures and Devices: 1997 (Kuala Lumpur)

Participation to Editorial Boards of Journals

- JETTA: Journal of Electronic Testing: Theory and Applications
- CDTA
- IEEE Transactions on VLSI Systems
- Journal of Microelectronic Systems Integration
- IEEE Design and Test of Computers Magazine
- Quality Engineering Journal
- Reliability Engineering & System Safety
- Quality Observer
- Journal of The Brazilian Microelectronics Society

**Organisation of Conferences**

- Electron and Optical Beam Testing of Integrated Circuits: 1987 (Grenoble, General Chair), 1989 (Duisburg, Program Chair), 1991 (Como, Program Chair), 1993 (Zurich, Program Chair), 1995 (Wuppertaal, Program Chair)
- EUROCHIP Workshop on VLSI Design Training (General Chair): 1991-1992 (Grenoble), 1993 (Toledo), 1994 (Dresden)
- European Conference on Design Automation / EUROASIC: 1993 (Paris, General Chair)
- European Conference on Design Automation / European Test Conference / EUROASIC: 1994 (Paris, Program Co-Chair)
- Rapid System Prototyping Workshop: 1994 (Grenoble, General Chair), 1996 (Thessaloniki, Program Chair)
- International Symposium on System Synthesis: 1995 (Cannes, Program Chair), 1996 (La Jolla, General Chair)
- IEEE Mixed-Signal Test Workshop: 1995 (Grenoble, General Chair)
- IEEE Workshop on On-Line Testing: 1995 (Nice, General Chair), 1996 (Biarritz, General Chair)
- Workshop on Thermal Investigations in ICs ans Systems: 1995 (Grenoble, General Chair), 1996 (Budapest, General Chair)
- VLSI Test Symposium: 1995-1996 (Princeton, Vice-Program Chair)
- Euro-VHDL: 1996 (Geneva, Program Chair)

**Participation to Societies and Working Groups**

- Member of IEEE European Test Technology Technical Committee
- Vice-Chair of Technical Activities of the IEEE Test Technology Technical Committee
- Chairman of the European Design and Automation Association

**Others activities**

- Review of papers for numerous Journals and Conferences
- Review of research proposals for CEC, NSF, NATO, SERC

**V-6 Awards and distinctions**

- IEEE Meritorious service awards (1993)
- Doctor Honoris Causa of the Technical University of Budapest (1994)
Picture 2:
Bernard COURTOIS is being awarded Doctor Honoris Causa of the Technical University of Budapest
VI - TECHNOLOGY TRANSFER ACTIVITIES

Besides their research and service activities, TIMA staff members are also concerned with technology transfer activities. For that purpose, they are regularly solicited to serve as consultant for technical and educational tasks, mainly by industrial companies, but also by foreign universities. Some results of these tasks have already been evoked throughout this report for the sake of consistency of the different sections, others only appear in this section. Up to now, the transfer technology activities have taken the following forms:

VI-1 Technical tasks

VI-1.1 Industrial Transfers

- Standard Mirror Board (SMB) developments, resulting from the research work made within the ADELAIDE project have been transferred to the IMD French company, which is introducing them now on the market. Details can be found in section II of this report, description of the Quality of Complex System Group.

- The AMICAL architectural synthesis system is currently under industrial transfer process: several companies have expressed their interest. Details are given in section II of the report, description of the System Level Synthesis Group.

- The VCI Co-simulation tool has been transferred to SGS-Thomson where it is being productized and used in several divisions in Grenoble and Bristol.

VI-1.2 Patents

The following patents have recently been taken:

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transparent Testing of Integrated Circuits</td>
<td>M. Nicolaidis</td>
<td>03/92</td>
</tr>
<tr>
<td>Implementation Techniques of Self-Checking Arithmetic Operators and Data Paths based on Double-Rail and Parity Codes</td>
<td>M. Nicolaidis</td>
<td>04/92</td>
</tr>
<tr>
<td>Standard Mirror Board (FR 92/12549)</td>
<td>L. Balme</td>
<td>12/92</td>
</tr>
<tr>
<td>Standard Mirror Board (FR 93/09571)</td>
<td>L. Balme</td>
<td>09/93</td>
</tr>
<tr>
<td>SEU Tolerant RAM</td>
<td>F. L. Vargas &amp; M. Nicolaidis</td>
<td>06/94</td>
</tr>
</tbody>
</table>

VI-1.3 Industrial Circuit Fabrication

In addition to its service activity for university and research laboratory circuit fabrication, CMP is offering circuit fabrication services for industrial circuit prototyping and low volume production. Thus 39 industrial prototypes coming from 17 companies were fabricated in 1995. Starting from 1993, more than 140 industrial prototype circuits have been fabricated, in CMOS, BICMOS, and GaAs technologies, for 34 companies and 10 universities/research laboratories. Moreover 24 small volume productions have been fabricated in 1995 (8% of the fabricated circuits), compared to 12 in 1994 and 3 in 1993.

Prices are negotiated directly by CMP with the manufacturer, depending on each request.
VI-1.4 Consulting

The following consulting tasks have recently been achieved:

<table>
<thead>
<tr>
<th>Company</th>
<th>TIMA member</th>
<th>Duration</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMS (Austria)</td>
<td>K. Torki</td>
<td>8 months</td>
<td>91-93</td>
</tr>
<tr>
<td>IN2P3/LAL (France)</td>
<td>K. Torki</td>
<td>5 days</td>
<td>04/92</td>
</tr>
<tr>
<td>Alcatel/Alsthom (France)</td>
<td>M. Nicolaidis</td>
<td>2 days</td>
<td>07/94</td>
</tr>
</tbody>
</table>

VI-2 Educational Tasks

Dealing with problems risen by advanced technologies, and proposing advanced design and test methodologies, TIMA staff members are, as a matter of course, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into five categories: course organization, seminars, support of or participation in foreign university teaching programs, participation in EU educational and technology transfer programs, and finally direction of Ph.D. students employed by French industrial companies (CIFRE program).

VI-2.1 Courses Organization

The following table lists courses that have been organized by members of the laboratory, at different institution request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA staff or externally.

<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Organizer</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT</td>
<td>Paris</td>
<td>02/92</td>
<td>2 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>HP</td>
<td>Grenoble</td>
<td>06/92</td>
<td>1 day</td>
<td>M. Marzouki</td>
<td>Board Testing</td>
</tr>
<tr>
<td>MFQ</td>
<td>Paris</td>
<td>12/92</td>
<td>3 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Grenoble</td>
<td>12/92</td>
<td>5 days</td>
<td>A. Guyot</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td></td>
<td>Tokyo</td>
<td>10/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td></td>
<td>Singapore</td>
<td>12/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>04/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/Chipshop</td>
<td>Grenoble</td>
<td>04/94</td>
<td>3 days</td>
<td>K. Torki</td>
<td>VLSI Design on PC platforms</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Irvine-CA</td>
<td>11/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>12/94</td>
<td>2 days</td>
<td>M. Lubaszewski</td>
<td>Mixed-Signal Testing</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Austin</td>
<td>11/95</td>
<td>2 days</td>
<td>M. Lubaszewski</td>
<td>Mixed-Signal Testing</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/94</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>ST Course</td>
<td>Grenoble</td>
<td>04/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Synthesis</td>
</tr>
</tbody>
</table>
Picture 3: AMICAL seminars
  a) in Tokyo, October 1993
  b) in Singapore, December 1993
VI-2.2 Courses and Seminars

Advanced courses and seminars are a practical way of sensitizing graduate students to state-of-the-art problems and research subjects. The attendance is also often composed by young and senior researchers who want to exchange ideas and views on specific problems of their own field or some related research domains.

In addition to internal seminars, the laboratory regularly invites people from Grenoble academic and industrial environment to attend the talks given by our visiting researchers. These people have recently had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. A.J. Van de Goor</td>
<td>Delit U. of Technology</td>
<td>07/92</td>
<td>Test for SRAMs and FIFOs</td>
</tr>
<tr>
<td>Prof. A.J. Van de Goor</td>
<td>Delit U. of Technology</td>
<td>07/92</td>
<td>Tests for neighborhood pattern sensitive faults</td>
</tr>
<tr>
<td>Dr. G. Venkatesh</td>
<td>ASIC Technologies, Bangalore</td>
<td>09/92</td>
<td>HLS of Asynchronous Speed Independent Controllers</td>
</tr>
<tr>
<td>Prof. D. Kinmont</td>
<td>U. Newcastle Upon Tyne</td>
<td>11/92</td>
<td>Correct Interactive Transformational Synthesis of DSP Hardware</td>
</tr>
<tr>
<td>Prof. F. J. Kurdahi</td>
<td>U. California, Irvine</td>
<td>03/93</td>
<td>Architectural Synthesis of DSP Systems</td>
</tr>
<tr>
<td>Prof. M. Soma</td>
<td>U. Washington, Seattle</td>
<td>04/93</td>
<td>Mixed-Signal Testing and DFT</td>
</tr>
<tr>
<td>Prof. A. Ivanov</td>
<td>U. British Columbia, Vancouver</td>
<td>06/93</td>
<td>BIST Compaction Schemes based on Multiple Signature Checking</td>
</tr>
<tr>
<td>Prof. J. A. Abraham</td>
<td>U. Texas, Austin</td>
<td>06/93</td>
<td>Testing of Analog Circuits</td>
</tr>
<tr>
<td>Prof. E. Aas</td>
<td>The Norwegian Inst. of Technology</td>
<td>07/93</td>
<td>Probabilistic Model of Design Quality</td>
</tr>
<tr>
<td>Mr. J. O'Leary</td>
<td>Cornell U., Ithaca, NY</td>
<td>11/93</td>
<td>Retargeting a Hardware Compiler Proof</td>
</tr>
<tr>
<td>Dr. Y. A. Zorian</td>
<td>AT&amp;T Bell Labs, NJ</td>
<td>03/94</td>
<td>Multi-Chip Module Testing</td>
</tr>
<tr>
<td>Dr. A. Richardson</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>Defect Oriented Testability Analysis and Analog DFT</td>
</tr>
<tr>
<td>Mr. Th. Olbrich</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>BIST and Diagnostics in Safety Critical Microsystems</td>
</tr>
<tr>
<td>Dr. M. Slamani</td>
<td>Ecole Polytechnique de Montreal, Canada</td>
<td>07/94</td>
<td>BIST, Fault Diagnosis and Testability Analysis in Analog ICs based on Sensitivity Concept</td>
</tr>
<tr>
<td>H. Morel &amp; B. Allard</td>
<td>Centre de Génie Electr., Lyon</td>
<td>10/94</td>
<td>Utilisation des graphes de liais et des réseaux de Pétri pour la simulation des systèmes de l'électronique de puissance</td>
</tr>
<tr>
<td>Dr. Rajeev Murgai</td>
<td>FUJITSU Labs of America Inc., San José</td>
<td>03/95</td>
<td>Decomposition of Logic Functions for Minimum Transition Activity</td>
</tr>
<tr>
<td>Prof. N. Yevtushenko &amp; Prof. A. Matrosova</td>
<td>Tomsk State Univ., Russia</td>
<td>04/95</td>
<td>- Testing strategies for communicating FSMs - Random simulation - Design for testability</td>
</tr>
<tr>
<td>Prof. G. de Micheli</td>
<td>Stanford Univ.</td>
<td>05/95</td>
<td>An algebraic approach to system-level modeling and synthesis</td>
</tr>
<tr>
<td>Prof. G. de Micheli</td>
<td>Stanford Univ.</td>
<td>05/95</td>
<td>Optimal synthesis of gated clocks for low power finite state machines</td>
</tr>
<tr>
<td>Prof. V. Uskov</td>
<td>Moscow State Tech. U.</td>
<td>06/95</td>
<td>Multipurpose CAD System GRAPH-PA</td>
</tr>
<tr>
<td>Dr. A. Oraloglu</td>
<td>San Diego Univ.</td>
<td>07/95</td>
<td>Microarchitectural synthesis of self-testable ICs</td>
</tr>
</tbody>
</table>
Concerning participation to external seminars, the following table lists the courses and seminars given by members of the laboratory on their specific research work, following the invitation of various institutions.

<table>
<thead>
<tr>
<th>Institution</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Speaker</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENSIL-LIP</td>
<td>Lyon</td>
<td>01/92</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line Operators</td>
</tr>
<tr>
<td>ENST</td>
<td>Paris</td>
<td>06/92</td>
<td>3h</td>
<td>A. Guyot</td>
<td>On-line Operators</td>
</tr>
<tr>
<td>EPFL</td>
<td>Lausanne</td>
<td>12/92</td>
<td>6h</td>
<td>M. Nicolaidis</td>
<td>Regular Structure Test and BIST - On-line Testing</td>
</tr>
<tr>
<td>ENST-ARCS</td>
<td>Paris</td>
<td>05/93</td>
<td>3h</td>
<td>A. Guyot</td>
<td>On-line Arithmetic Operators</td>
</tr>
<tr>
<td>EPFL</td>
<td>Lausanne</td>
<td>09/93</td>
<td>6h</td>
<td>M. Nicolaidis</td>
<td>Regular Structure Test and BIST - On-line Testing</td>
</tr>
<tr>
<td>CERN</td>
<td>Geneva</td>
<td>01/94</td>
<td>1h</td>
<td>M. Lubaszewski</td>
<td>On-line test extension to IEEE 1149.1</td>
</tr>
<tr>
<td>AFCET</td>
<td>Paris</td>
<td>02/94</td>
<td>1h</td>
<td>M. Marzouki</td>
<td>Boundary Scan Board and MCMs Test</td>
</tr>
<tr>
<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>IC Test - Main Methods</td>
</tr>
<tr>
<td>UFMG</td>
<td>Belo Hor.</td>
<td>09/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>BS Test</td>
</tr>
<tr>
<td>Telebras/CPqD</td>
<td>Campinas</td>
<td>12/94</td>
<td>2h</td>
<td>M. Marzouki</td>
<td>BS Test</td>
</tr>
<tr>
<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>A. Jerraya</td>
<td>Codesign</td>
</tr>
<tr>
<td>UFRJ</td>
<td>Rio de J.</td>
<td>12/94</td>
<td>2h</td>
<td>A. Jerraya</td>
<td>Behavioral synthesis</td>
</tr>
<tr>
<td>UFRGS</td>
<td>P. Alegre</td>
<td>11/94</td>
<td>2h</td>
<td>A. Jerraya</td>
<td>Behavioral synthesis</td>
</tr>
<tr>
<td>ENST</td>
<td>Paris</td>
<td>03/95</td>
<td>1h</td>
<td>A. Jerraya</td>
<td>Codesign</td>
</tr>
</tbody>
</table>

VI-2.3 Support of Universities Teaching Programs

The laboratory has established for many years solid contacts with other research institutions and universities throughout the world. Exchange of students and post-doctoral fellows are very common, and TIMA members are often invited to participate in foreign university teaching programs. The following table lists this kind of activities during the recent academic years.

<table>
<thead>
<tr>
<th>University</th>
<th>Country</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tallinn Technical Univ.</td>
<td>Estonia</td>
<td>05/93</td>
<td>9h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>12/93</td>
<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Inst. for Microel. Stuttgart</td>
<td>Germany</td>
<td>02/94</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line arithmetic operators</td>
</tr>
<tr>
<td>Politecnica Bucharest</td>
<td>Romania</td>
<td>05/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>CMOS VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>06/94</td>
<td>3h</td>
<td>M. Marzouki</td>
<td>Partial Boundary Scan Test</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>12/94</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>02/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Architecture and arithmetic</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>11/95</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>01/95</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Arithmetic</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>02/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>CMOS circuitry</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>03/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>Operators</td>
</tr>
</tbody>
</table>

cont'd
VI-2.4 Participation in EU Educational Programs

TIMA laboratory activities have a strong European profile. In addition to numerous research projects listed in other sections of this report, the following table indicates the involvement of TIMA staff members in educational programs launched by the European Union. This involvement takes the form of organizing and/or teaching courses.

<table>
<thead>
<tr>
<th>Framework</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTTT Comett II</td>
<td>Greece</td>
<td>02/92</td>
<td>15h</td>
<td>A. Guyot</td>
<td>VLSI Design Course teaching</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>France</td>
<td>12/92</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Germany</td>
<td>02/94</td>
<td>3h</td>
<td>M. Nicolaidis</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>JTTT Comett II</td>
<td>Italy</td>
<td>02/94</td>
<td>1h</td>
<td>M. Nicolaidis</td>
<td>European School on High Reliability Integrated Systems</td>
</tr>
<tr>
<td>JTTT Comett II</td>
<td>Greece</td>
<td>12/94</td>
<td>15h</td>
<td>M. Nicolaidis</td>
<td>Advanced Course on VLSI Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>08/94</td>
<td>6h</td>
<td>A. Jerraya</td>
<td>System Design</td>
</tr>
<tr>
<td>Comett</td>
<td>Austria</td>
<td>04/95</td>
<td>3days</td>
<td>C. Liem</td>
<td>Reconfigurable architecture</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>09/95</td>
<td>3days</td>
<td>Jerraya/Kission</td>
<td>System design</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Denmark</td>
<td>08/95</td>
<td>5days</td>
<td>A. Jerraya</td>
<td>Co-design</td>
</tr>
<tr>
<td>Comett</td>
<td>Netherlands</td>
<td>09/95</td>
<td>3days</td>
<td>Kission/Rahm</td>
<td>AMICAL</td>
</tr>
</tbody>
</table>

VI-2.5 University/Industry Joint Research Programs

A French national program, called CIFRE, allows French companies to receive French Ph.D. students. The thesis director must belong to a French university or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company. TIMA staff members have been asked by companies to direct several Ph.D. theses in the CIFRE framework. The most recent ones are listed in the table below.

<table>
<thead>
<tr>
<th>Company</th>
<th>Student</th>
<th>Director</th>
<th>Dur.</th>
<th>Research Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hewlett Packard</td>
<td>P. Dulieux-Verguin</td>
<td>B. Courtois</td>
<td>91-94</td>
<td>Failure Analysis of ICs by Liquid Crystals</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>M. Kodrnja</td>
<td>A. Guyot</td>
<td>92-95</td>
<td>Analog Voltage Controlled Oscillators and Phase-Locked Loops</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>F. Lemery</td>
<td>M. Marzouki</td>
<td>92-95</td>
<td>Analog and Mixed Macromodeling</td>
</tr>
<tr>
<td>IMD</td>
<td>A. Benali</td>
<td>L. Balme</td>
<td>92-95</td>
<td>Electro-optic ATE</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>E. Berrebi</td>
<td>A. Jerraya</td>
<td>93-96</td>
<td>Heterogeneous System Design</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>F. Naçabal</td>
<td>A. Jerraya</td>
<td>95-96</td>
<td>Heterogeneous System Design</td>
</tr>
</tbody>
</table>
VIII - PUBLICATIONS 1994-1995

VIII-1 Books and magazines

1994

AICHOUCHI M., O'BRIEN K.*, JERRAYA A.
Generation and validation of detailed architectures from behavioral VHDL specifications
Arabian Journal for Science and Engineering, October 1994
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Lectures in Computer Science, Field Programmable Logic: Architectures, Synthesis
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Circuits & Devices, January 1994

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Journal of Electronic Testing, Theory and Applications (JETTA), Kluwer Academic
体验
* Minsk Radioengineering Institute, Minsk, Bielorussia

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In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
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Economics of Electronic Design, Manufacture and Test,
Editors: M. Abadir, T. Ambler

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Parallel Processing Letters, Vol. 4, n° 3, 1994
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* LEDA SA, Meylan, France

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IEEE Transactions on Nuclear Science,
December 1995
* LGI, Grenoble, France

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Invited paper in the Journal of Future Electron Devices Institute, Tokyo, Japan, 1995

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* University of Siegen, Germany
** Mc Gill University, Montreal, Canada
*** Max-Planck-Society, Fault Tolerant Computing Group at Univ. of Potsdam, Germany
**** C&RL Laboratory, Univ. of Illinois at Urbana-Champaign, Urbana, USA

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* Ecole Polytechnique de Montréal, Canada

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Guest Editors
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* Technical University of Budapest, Hungary
SZÉKELY V.*, RENCZ M.*, COURTOIS B.
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Special Issue on Thermal Issues in Microsystems
Guest Editors
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*Technical University of Budapest, Hungary

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Quality Effort in Europe, Special issue of the Journal of Quality Engineering
Vol. 8, N°4, Publication by Marcel DEKKER Inc., New York, USA, 1996

* IMD, Bandol, France

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Special Issue on Rapid System Prototyping
Guest Editor
To appear in 1997

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In "Encyclopedia of Microcomputers", a multi-volume work
published by Marcel Dekker Inc. of New-York
To appear in 1997

* Technical Univ. of Budapest, Dept. of Electron Devices, Hungary

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IEEE Transactions on VLSI Systems
Special Issue on Thermal Investigations
Guest Editors
To appear in 1997

* Technical University of Budapest, Hungary

VII-2 Conferences and Workshops

1994

BACIVAROV* I.C., BALME L.
On reliability testing of semiconductor devices
European Safety and Reliability Conference (ESREL 94)
La Baule, France, 30 May - 3 June, 1994

* Visiting Professor on leave from POLITECNICA Univ., Bucharest, Romania

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12th IEEE VLSI Test Symposium
Cherry Hill, USA, April 1994
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Nara, Japan, November 1994

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The European Design and Test Conference (EDAC-ETC-EUROASIC 94)
Paris, France, 28 February - 3 March 1994
ANTEA S.A., Meylan, France

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An approach for hardware-software codesign
International Workshop on Rapid System Prototyping (RSP'94)
Villard de Lans (Grenoble), France, 20-23 June, 1994
* ENIM, Monastir, Tunisia
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COSMOS: a codesign approach for communicating systems
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Grenoble, France, September 1994
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Invited paper at 8th Brazilian Symposium on Integrated Circuits Design
Gramado, Brazil, November 1994

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Microengineering in Medecine, in Biology, and its Application to Minimaly Invasive Techniques for Therapy and Medical Diagnosis
EPFL, Lausanne, Switzerland, 5-7 October 1994
* TIMC, La Tronche, France

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Keynote presentation at Third International Workshop on The Economics of Design, Test and Manufacturing
Austin, Texas, USA, 16-17 May 1994

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Toyohashi, Japan, 24-25 October 1994
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framework of "Informatization of Russia Program"; New information technologies for
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Yalta, Ukraine, 4-13 May 1994

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Trends in fabrication, design and CAD - European perspectives
XXI International Conference and School for young scientists and professionals within the
framework of "Informatization of Russia Program"; New information technologies for
science, education and business (CAD'94)
Yalta, Ukraine, 4-13 May 1994

* Technical University of Budapest, Hungary

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The Services available from CMP
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Rio de Janeiro, Brazil, 10-12 August 1994

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Prague, Czech Republic, September 7-9, 1994

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Grenoble, 19-21 December 1994

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* TH Darmstadt, FG Mikroelektronische Systeme, Germany

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Barcelona, Spain, June 1-3, 1994

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Santa Cruz, California, USA, 15-18 March 1994

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"Premier Forum National Microtechnologies et Microsystèmes"
Paris, France, 15-17 November 1995

KARAM J.M.
Vers les fonderies de microsystèmes
Workshop ESIEE - Les microsystèmes sur la voie de l'industrialisation
Paris, France, 15 June 1995

KARAM J.M., COURTOIS B.
Circuits multi-projets : activité du CMP
Réunion Technique de l'assemblée Générale de l'ISHM
Versailles, France, 18 October 1995

1996

KARAM J.M.
Fabrication collective de microsystèmes - Accès en technologie et outils de simulation
FORUM ISHM 96
Paris, France, 2-3 April 1996

VII-3 Theses

1994

HAMDI Belgacem
Outils CAO pour la génération automatique de parties opératives auto-contrôlables
Thèse de Doctorat INPG - 18 Avril 1994

AICHOUCHEI Mohamed
Etude des liens entre la synthèse architecturale et la synthèse au niveau transfert de registres
Thèse de Doctorat INPG - 20 juin 1994

LUBASZEWSKI Marcelo
Le test unifié de cartes appliqué à la conception de systèmes fiables
Thèse de Doctorat INPG - 20 juin 1994
KEBICHI Omar
Techniques et outils de CAO pour la génération automatique de BIST et DFT pour RAMS
Thèse de Doctorat INPG - 15 juillet 1994

KOLARIK Vladimir
Techniques avancées de test de circuits analogiques et mixtes analogiques-numériques
Thèse de Doctorat INPG - 31 octobre 1994

BEDERR Hakim
Contribution à la conception en vue du test d'opérateurs à structure itérative
Thèse de Doctorat INPG - 23 novembre 1994

VERGUIN Pascale
Industrialisation d'une méthode de localisation de défauts sur circuits intégrés par cristaux liquides
Thèse de Doctorat INPG - 20 décembre 1994

1995

MONTALVO Luis Anibal
Systèmes de numération pour la conception de diviseurs rapides
Thèse de Doctorat INPG - 13 mars 1995

VARGAS Fabian Luis
Amélioration de la fiabilité des systèmes spatiaux basée sur le contrôle de courant
Thèse de Doctorat INPG - 5 mai 1995

BOUDJIT Mokhtar
Algorithmes de testabilité basés sur la description à deux-niveaux "Groupe-E-Concurrente" des fonctions logiques
Thèse de Doctorat INPG - 19 mai 1995

SKAF Ali
Conception de processeurs arithmétiques redondants et en-ligne : algorithmes, architectures et implantations VLSI
Thèse de Doctorat INPG - 11 septembre 1995

LEMERY François
Modélisation comportementale des circuits analogiques et mixtes
Thèse de Doctorat INPG - 20 décembre 1995

1996

BEN ISMAIL Tarek
Synthèse au niveau système et conception de systèmes mixtes logiciels/matériels
Thèse de Doctorat INPG - 9 janvier 1996

TOUATI Mohamed Hédi
Test et diagnostic de cartes et de MCMs partiellement boundary scan
Thèse de Doctorat INPG - 24 janvier 1996

KISSSION Polen
Exploitation de la hiérarchie et de la réutilisation de blocs existants par la synthèse de haut niveau
Thèse de Doctorat INPG - 25 janvier 1996
VII-4 Reports

1995

COURTOIS B.
CAD and testing of ICs and systems: where are we going?
TIMA research report, December 1995 (update)

COURTOIS B.
CAD and testing of ICs and systems: where are we going? (Russian version)
This is a Russian version of the report published previously (in September 1994),
translated by A. PILEROY, Head of Department of Computer Research Institute, Minsk, Belarus.

VII-5 Patents

1994

BALME L. & al.
Smart Power card
US patent 07/937900

VARGAS F., NICOLAIDIS M.
A current monitoring-based technique to detect and correct single-event upsets (SEUs) in
static RAMs for space applications
Brevet CNRS, Grenoble, France, June 1994
VIII.1 What did they do after graduating from the Laboratory (1984-1995) ?

Below is the list of researchers which graduated from the Computer Architecture Group, from 1984.

The first affiliation corresponds to their affiliation right after the thesis. Eventually, successive affiliations are provided.

From 1984 to 1995, 72 theses have been defended.

It might be noticed that (apart from foreign students who returned in their country) several members of the group have been or are working abroad.

**DERANTONIAN H.**
- Génération automatique de parties contrôles de microprocesseurs sous forme de PLA spécialisés.
- BULL - Grenoble

**NICOLAIDIS M.**
- Conception de circuits intégrés ou testables pour des hypothèses de pannes analytiques.
- CNRS - TIMA Laboratory - Grenoble

**LAURENT J.**
- Projet ACIME : Analyse des Circuits Intégrés par Microscopie Electronique.
- CNRS - TIMA Laboratory - Grenoble
- Next: CNRS - IMAG - Grenoble

**HMMID M.**
- Assemblage et génération automatique des dispositifs périphériques de PLA complexes.
- SIEMENS - Munich - FRG

**SAHBATOU M. D.**
- Une méthode de conception de microprocesseurs CMOS : application au 8048 (INTEL)

**CHUQUILLANQUI S.**
- Une nouvelle approche pour l'optimisation topologique et l'automatisation du dessin des masques de PLA complexes.
- BULL Systèmes - Les Clayes Sous Bois
- Next : THOMSON THOM'6 - Paris
- Next : GEC ALSTHOM - Paris la Défense
BOURCIER E.
Conception et réalisation du simulateur de langage de description de circuits intégrés
IRENE C.
SGS THOMSON - Grenoble

JANSCH I.
Conception de contrôleurs autotestables pour des hypothèses de pannes analytiques.
Porto Alegre University - Brazil

BERGHER L.
Analyse de défaillances de circuits VLSI par microscopie électronique à balayage.
SGS THOMSON - Grenoble
Next : BULL Systèmes - Les Clayes Sous Bois
Next : SGS-THOMSON - Grenoble
Next : Thomson TCEC - Grenoble

IANESELLI J.C.
Un opérateur d'unification pour une machine base de connaissance PROLOG.
MERLIN GERIN - Meylan

SUWARDI I.S.
 Mécanismes predictifs d'évaluation des caracteristiques geometriques des circuits VLSI.

SCHOELLKOPF J.P.
SILICIUEL : Contributions à l'architecture des circuits intégrés et à la compilation du silicium.
BULL Systèmes - Les Clayes Sous Bois
Next : SGS THOMSON - Grenoble

BERTRAND F.
Conception descendante appliquée aux microprocesseurs VLSI
BULL Systèmes - Les Clayes Sous Bois
Next : LETI - Grenoble

MARTINEZ F.
CIRENE : Compilateur du langage IRENE

GUIGUET I.
Liaison d'un microscope électronique à balayage aux outils CAO de description des circuits intégrés.
APSIS - Meylan

PEREZ SEGOVIA T.
PAOLA : un système d'optimisation topologique de PLA.
CNET - Meylan
MARINE S.
Un langage pour la description, simulation et synthèse automatique du matériel VLSI
SGS THOMSON - Grenoble
Next : ALCATEL-Alsthom, Marcoussis

BASCHIERA D.
Modélisation de pannes et méthodes de test de circuits intégrés CMOS
TRT - Paris
Next : NORSKDATA - Norway
Next : EPFL - Lausanne - Switzerland
Next : HMT - Brügg b/Biel - Switzerland

ALIOUAT M.
Reprise de processus dans un environnement distribué après pannes matérielles transitoires
ou permanentes
Thèse de Docteur Ingénieur - Avril 1986
University of Constantine - Algeria

OSSEIRAN A.
Définition, étude et conception d'un microprocesseur autotestable spécifique : COBRA
EPFL - Lausanne - Switzerland
Next: University of Geneva, Switzerland

JAMIER R.
Génération automatique de parties opératives de circuits VLSI de type microprocesseur
Thèse de Docteur Ingénieur - Décembre 1986.
SGS THOMSON - Grenoble

DANG W.
Parallélisme dans une machine base de connaissances PROLOG
CRIL - Colombes

VARINOT P.
Compilation de silicium : application à la compilation de parties contrôles
University of Porto Alegre - Brazil
Next : MATRA - Paris

HOCHET B.
Conception de VLSI : Applications au calcul numérique
EPFL - Lausanne - Switzerland
Next : University of Adelaide - Australia
Next : University of Yverdon, Switzerland

ROUGEAUX F. R.
Outils de CAO et conception structurée de systèmes intégrés sur silicium
University of Laval - Canada
Next : IBM - Montpellier
SOUAI M.
Etude d'un moniteur d'un système fonctionnellement réparti.

CAISSO J.P.
Contribution à la vérification des circuits intégrés dans un environnement multivalué.
Mc GILL University - Montreal - Canada
Next : MATRA-MHS - Nantes

BEKKARA N.
Optimisation et compromis surface-vitesse dans le compilateur de silicium SYCO
SGS THOMSON - Grenoble

DUPRAT J.
LAIOS : un réseau multiprocesseur orienté intelligence artificielle
E.N.S. Lyon

MHAYA N.
Compilateur de parties contrôle de microprocesseurs
IFATEC - Versailles
Next: IFATEC - Montigny-le-Bretonneux

FERNANDES A.
Test des PLAs optimisés topologiquement
University of Belo Horizonte - Brazil
Next: Professor at "Universidade Federal de Minas Gerais", Belo Horizonte, Brazil

ZYSMAN E.
Conception de parties contrôles de circuits VLSI - Application au coprocesseur arithmétique
FELIN
EPFL - Lausanne - Switzerland

BERGER-SABBATEL G.
Machines spécialisées et programmation en logique
CNRS - TIMA Laboratory - Grenoble
Next : LGI Laboratory - Grenoble

MICOLLET D.
Etude de la contrôlabilité de circuits intégrés par faisceaux d'électrons
University of Dijon
Next : LIESIB Laboratory - Dijon University
MOISAN F.
Optimisation du contraste image en microscopie optique (application à l'inspection microélectronique)
Direction des Constructions et des Armes Navales (DCAN) - Brest

HORNIK A.
Contribution à la définition et à la mise en œuvre de NAUTILE
Thèse de Doctorat INPG - Juin 1989
APSIS - Meylan
Next : BULL - Echirolles

DARLAY F.
Contribution au test des circuits intégrés CMOS : étude du test des pannes stuck-on et stuck-open
Thèse de Doctorat INPG - 20 novembre 1989
EPFL - Lausanne - Switzerland
Next : École Polytechnique de Montréal, Canada
Next : SGS Thomson, Grenoble

NORAZ S.
Application des circuits intégrés autotestables à la sûreté de fonctionnement des systèmes
Thèse de Doctorat INPG - 20 décembre 1989
MERLIN GERIN - Meylan

BONDONO P.
Contribution à NAUTILE : un environnement pour la compilation de silicium
Thèse de Doctorat INPG - 8 décembre 1989
IBM - Corbeil

JERRAYA A.
Participation à la compilation de silicium et au compilateur SYCO
Thèse d'État - 19 décembre 1989
CNRS - TIMA Laboratory - Grenoble

TORKI K.
L'autotest intégré dans un compilateur de silicium
Thèse de Doctorat INPG - 12 juillet 1990
CMP - Grenoble

PIRSON A.
Conception et simulation d'architectures parallèles et distribuées pour le traitement d'images
Thèse de Doctorat INPG - 4 mai 1990
CENG Division LETI - Grenoble

SAVART D.
Analyse de défaillance de circuits intégrés VLSI par testeur à faisceau d'électrons
Thèse de Doctorat INPG - 27 juin 1990
IMAGERIE INFORMATIQUE - Grenoble

BALME L.
Habilitation à diriger des recherches. 21 mai 1990
On secondment to SGS, Geneva, from 1.1.1991
Next : TIMA Laboratory
CHAUMONTET G.
Etude de faisabilité d'un micro-contrôleur de très haute sécurité
Thèse de Doctorat INPG - 26 octobre 1990
Centre de Compétence en Conception de Circuits Intégrés (C4I), Archamps

MARZOUKI M.
Approches à base de connaissances pour le test de circuits VLSI : application à la
validation de prototypes dans le cas d'un test sans contact
Thèse de Doctorat INPG - 6 février 1991
CNRS - TIMA Laboratory - Grenoble

CONARD D.
Traitement d'images en analyse de défaillances de circuits intégrés par faisceau
d'électrons
Thèse de Doctorat INPG - 11 février 1991
INFI Society (ARM Group) - Paris

COURT T.
Conception d'une famille de coprocesseurs parallèles intégrés pour le traitement
d'images
Thèse de Doctorat INPG - 9 décembre 1991
I2S, Bordeaux

COLLETTE T.
Architecture et validation comportementale en VHDL d'un calculateur parallèle dédié à la
vision
Thèse de Doctorat INPG - 14 septembre 1992
CEA/LEIT/DEIN - GIF sur Yvette

CASTRO ALVES V.
Modélisation de pannes et algorithmes de test pour mémoires RAMs multi-port
Thèse de Doctorat INPG - 10 décembre 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble
Next: Lecturer at Aveiro University - Portugal
Next: Professor at UFRJ - Rio de Janeiro - Brazil

JEMAI A.
Etude d'un processeur RISC pour un système symbolique parallèle
Thèse de Doctorat INPG - 22 juin 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble
Next : ENSI, Tunis, Tunisia

PARK I.
AMICAL : un assistant pour la synthèse et l'exploitation architecturale des circuits de
commande
Thèse de Doctorat INPG - 3 juillet 1992
DAS/ETRI, Daejon, Research Laboratory in Korea

BOURAOUI R.
Calcul sur les grands nombres et VLSI : application au PGCD, au PGCD étendu et à la
distance euclidienne
Thèse de Doctorat INPG - 15 janvier 1993
Bell Northern Research (BNR), Ottawa, Canada
Next: Plaintree Systems Inc., Stittsville, Ontario, Canada
O'BRIEN K.
Compilation de silicium : du circuit au système
Thèse de Doctorat INPG - 31 mars 1993
LEDA S.A., Meylan, France

KUSUMAPUTRI-HORNIK Y.
Opérateurs arithmétiques standards en-ligne à très grande précision
Thèse de Doctorat INPG - 11 mai 1993

BEN OTHMAN M.
Evaluation d'une hiérarchie mémoire pour une machine symbolique
Thèse de Doctorat INPG - 8 septembre 1993

VAUCHER Ch.
Le test haute résolution de circuits imprimés nus
Thèse de Doctorat INPG - 25 novembre 1993
IMD, Grenoble, and TIMA Laboratory

HAMDI B.
Outils CAO pour la génération automatique de parties opératives auto-contrôlables
Thèse de Doctorat INPG - 18 Avril 1994

AICHOUCHI M.
Etude des liens entre la synthèse architecturale et la synthèse au niveau transfert de registres
Thèse de Doctorat INPG - 20 juin 1994

LUBASZEWSKI M.
Le test unifié de cartes appliqué à la conception de systèmes fiables
Thèse de Doctorat INPG - 20 juin 1994
Professor at the UFRGS, Porto Alegre University, Brazil

KEBICHI O.
Techniques et outils de CAO pour la génération automatique de test intégré pour RAMS
Thèse de Doctorat INPG - 15 juillet 1994
Engineer/researcher at TIMA Laboratory - Grenoble

KOLARIK V.
Techniques avancées de test de circuits analogiques et mixtes analogiques-numériques
Thèse de Doctorat INPG - 31 octobre 1994
University of Brno, Czech Republic

BEDERR H.
Contribution à la conception en vue du test d'opérateurs à structure itérative
Thèse de Doctorat INPG - 23 novembre 1994
Post-Doctoral position at AT&T Bell Laboratories, Princeton, USA

VERGUIN P.
Industrialisation d'une méthode de localisation de défauts sur circuits intégrés par cristaux liquides
Thèse de Doctorat INPG - 20 décembre 1994
Primary school teacher
MONTALVO L.  
Systèmes de numération pour la conception de diviseurs rapides  
Thèse de Doctorat INPG, 13 mars 1995  
University of Minnesota, Minneapolis, USA

VARGAS F.L.  
Amélioration de la sûreté de fonctionnement des systèmes spatiaux basée sur le contrôle de courant  
Thèse de Doctorat INPG, 5 mai 1995  
Associated Researcher at U.F.R.G.S., Porto Alegre University, Brazil

BOUDJIT M.  
Algorithmes de Testabilité basés sur la Description à Deux-Niveaux "Groupe-E Concurrente" des Fonctions Logiques  
Thèse de Doctorat INPG, 19 mai 1995

SKAF A.  
Conception de processeurs arithmétiques redondants et en-ligne : algorithmes, architectures et implantations VLSI  
Thèse de Doctorat INPG, 11 septembre 1995  
Lecturer at Aveiro University, Portugal  
Next : HIAST Institute, Damascus University, Syria

LEMERY F.  
Modélisation comportementale des circuits analogiques et mixtes  
Thèse de Doctorat INPG, 20 décembre 1995  
SGS-Thomson Crolles, Central R&D, France

BEN ISMAIL T.  
Synthèse au niveau système et conception de systèmes mixtes logiciels/matériels  
Thèse de Doctorat INPG, 9 janvier 1996  
Hewlett Packard - Bristol, UK

TOUATI M.H.  
Test et diagnostic de cartes et de MCMs partiellement boundary scan  
Thèse de Doctorat INPG - 24 janvier 1996

KISSION Polen  
Exploitation de la hiérarchie et de la réutilisation de blocs existants par la synthèse de haut niveau  
Thèse de Doctorat INPG - 25 janvier 1996  
TIMA Laboratory - Grenoble
VIII.2 Press articles in 1995

In the following are collected copies of articles that appeared in Newspapers in 1995.
Summary

- Le CMP se lance dans les Microsystèmes
  PRESENCES N° 85
  March 1995

- MEMS Prototyping available at low cost
  ELECTRONIC DESIGN
  8 January 1995

- Low-Cost Microelectromechanical Systems Prototyping
  SEMICONDUCTOR INTERNATIONAL Vol. 19, n°1
  January 1996

- Tehnikaülikoolis tegutseb Elektroonika kompetentsuskeskus
  KESTI PÄEVALEHT Nr. 135
  13 November 1995

- Ouverture d’un service de réalisation économique de prototypes de
  Microsystèmes
  ELECTRONIQUE INTERNATIONAL n° 200
  9 November 1995

- Un système d’organisation ad hoc
  Journal de Genève et Gazette de Lausanne
  8 May 1995

- European Design And Test Conference ’95
  ELECTRONIC DESIGN
  6 March 1995

- Laboratorul TIMA din Grenoble - un posibil model al cercetării științifice
  UNIVERS INGINERESC Nr. 5 (Romania)
  1995

Hubert CURiEN, Minister for Research and Technology, in Grenoble in 1986 (Daniel BLOCH, Chairman of INPG, presently Chairman of UJF).
LE CMP SE LANCE DANS LES MICROSYSTÈMES

Le CMP (Circuits multiprojets), centre de conception microélectronique de l'Institut national polytechnique de Grenoble dirigé par Bernard Courtois, dispose désormais des outils de conception nécessaires pour faire fabriquer des microsystèmes qui font cohabiter sur un même substrat électronique et mécanique miniatures. Il est le premier en Europe à ouvrir ce type de service. Les premières applications industrielles sont le médical, l'instrumentation et le spatial. En 1995, le CMP a vu une forte poussée des demandes dans le prototypage d'Asics (circuits intégrés spécifiques) : près de 300 prototypes ont été réalisés, dont 8% fabriqués ensuite en petites séries, pour le compte de 95 clients, dont 30 industriels.
MEMS Prototyping Available at Low Cost

Microelectromechanical systems (MEMS) technology is spreading its wings. Designers now can avail themselves of an inexpensive 1.0-μm CMOS prototyping service for MEMS, available from Circuits Multi-Projets (CMP), Grenoble, France. The service includes double-layer metal and single-layer polysilicon, front-side bulk-micromachined capability using EDP (ethylene-diamine-pyrocathecol) water etching. The processing is performed at the ESIBE (Ecole Superieure d’Ingenieurs en Electrotechnique et Electronique). The Paris university is known for its clean-room capabilities, with 300 m² of Class 10,000 and 100 facilities that include liquid-phase and plasma-etched chemical-vapor-deposition (LPCVD and PECVD) equipment, plus contact optical and double-sided aligners. The facility handles anodic and direct silicon-bonding, as well as anisotropic wet-chemical and plasma reactive-ion etching (RIE). MEMS devices like cantilevers, membranes, microbridges, etc., may be processed together with integrated electronic circuitry. A Cadence Opus design kit is available for layout generation of electronic and non-electronic components. The kit includes design-rule checking and an extended-parameter extractor (from layout to net list). The net list is generated, allowing structures to be electrically simulated as resistances represented in Anadat’s HDLA/ELDO analog hardware-description language. CMP also plans to introduce surface, gallium arsenide, and quartz micromachining, as well as processing of other CMOS technologies. The cost of the service is 1500 French francs per mm² (about $300 per mm²), with 15 samples being delivered to the user, five of which are packaged.

For further information, contact Jean-Michel Karam, CMP, Microsystems Group, 46, avenue Felix Viallet, 38031 Grenoble, Cedex, France; telephone: +33 76 57 46 20; fax: +33 76 47 38 14; or via e-mail at karam@imag.fr. EAI.
Low-Cost Microelectromechanical Systems Prototyping

One way to make microelectromechanical systems (MEMS) technology available to many designers, i.e. to move the technology from the specialized research laboratories to the commercial market, is to offer low cost prototyping. Circuits Multi-Projets, ESIEE Group (Paris, France) introduced microsystems prototyping and small volume production by applying the same principles as those applied 16 years ago for integrated circuits: a multi-project wafer approach, where the cost of a wafer is shared among multiple users. MEMS fabrication is based on CMOS 1 micron front side processes, bulk micromachined by EDP at ESIEE.

MEMS like cantilevers, membranes, and microbridges may be processed together with the electronics. Design rules have been defined and are available to designers upon signature of a confidentiality and license agreement. A design kit is available to allow the generation of a layout including electronic and non-electronic parts. The kit includes an extended parameter extractor (from layout to netlist) distinguishing electronic and non-electronic parts. A netlist is generated allowing an electrical simulation where bridges, cantilevers and membranes are represented by a model. Other CMOS processes, e.g. surface micromachining, GaAs processes, and quartz micromachining will be introduced gradually.

The cost of the service is 1500 FF/mm², 15 samples being returned to the user. Design rules and a basic library are also available. The industrial equipment of ESIEE includes 3000 m² of Class 10,000 and Class 100 cleanrooms, furnaces, LPCVD, PECVD, contact optical aligners, double-side aligner, anodic bonding, silicon direct bonding, anisotropic wet chemical silicon etching and plasma reactive ion etching. MD.
OUVERTURE D’UN SERVICE DE RÉALISATION ÉCONOMIQUE DE PROTOTYPES DE MICROSYSTÈMES

Le CMP (Circuits Multi-Projets) vient d’ouvrir en France pour les microsystèmes un service analogue à celui qui existe déjà pour la réalisation de prototypes de circuits spécifiques. Ce service, qui permet de partager les coûts entre différents projets (plusieurs microsystèmes sont intégrés sur la même tranche de silicium), est adapté à la réalisation de différents types de microsystèmes (membranes, micro-ponts, cantilever, etc.) avec l’électronique associée en technologie CMOS 1 µm (la fabrication se fait à l’Esisa). Il en coûtera 1 500 francs par millimètre carré, y compris la fourniture de 15 échantillons. Le CMP peut aussi fournir un kit de conception pour la génération du layout incluant les parties électroniques et non électroniques. Ce kit inclut un vérificateur de règles (DRC), un extracteur de paramètres et une bibliothèque de cellules de base. D’autres technologies ainsi que des techniques de micro-usinage en surface devraient être introduites progressivement.

Renseignements : B. Courtois,
J. M. Karam, tél. 76 57 46 20,
fax 76 47 38 14, Internet:
Tehnikatäitlikkus tegutseb Elektroonika kompetentsuskeskus

TTÜ professor
Raimund Ubar

Elektrooniline kirjasooks on häädavajalik

"Kompetentsus" keskuse nimes ei vihjatud ettepanekutele, sest oli tähtne, mida hõlmatud aspektite - osakondid ühemust õuest kujulisest ja mõistel sind aitasid, neid nimiab vastas olulisele teosele. Teatud moodus lõpetas keskuse kompetentsuse teose poole, isegi seeläbi poolega, kuna see oli esinekeskwilisest poolega. Algusest saab, et esimesed keskuse tegevused olid seotud elektroniinist ja elektroniseemest.

Disain on kaalutud kui tootmine

Elektroonikakursus on esialduslikult, kuid mitte täielikult õiklased. Osa disainist on õigust kodumajutuslikkompetentsus, kompetentsus on aset teeb esiest investeeringut, tootmise, uuene toodetust ja uued võimalused.

Kompetentsus tuleb hariduse kaudu. Elektroonikaprobleemid, mida on kasulik, saavad alati olla seotud elektroniinist ja elektroniseemest. Osa disainist on õigust kodumajutuslikkompetentsus, kompetentsus on aset teeb esiest investeeringut, tootmise, uuene toodetust ja uued võimalused.
Un système d'organisation ad hoc

Les normes ISO 14 000 développées par l'Organisation internationale de normalisation veulent être une réponse aux besoins exprimés en 1992 lors du Sommet de la Terre de Rio. Elles ont été conçues pour aider les entreprises à gérer leurs activités environnementales. Un système ISO 14 000 est mis en place par une entreprise, pour s'assurer que les services qu'elle fournit sont fabriqués et mis sur le marché de manière respectueuse de l'environnement.


Pour Louis Balme, ISO 14 000 est un dispositif complémentaire de l'engagement à la mise en place d'une solution optimisée. À terme, il est nécessaire que l'entreprise se conforme à la loi dans tous les domaines importants pour l'environnement. Par quelles activités exactement une entreprise peut-elle influencer l'environnement? Quels sont les coûts qui y sont liés? Existe-t-il des risques cachés? L'entreprise est-elle assez bien organisée pour parer aux incidents? Existe-t-il une attribution claire des responsabilités en matière d'environnement? Subsiste-t-il des incertitudes quant au droit environnemental et la responsabilité du fait des produits? La société peut-elle, par un management de l'environnement, améliorer ses relations avec les banques et les assurances? Qu'attendent les collaborateurs, les et l'entreprise publique en matière d'environnement?

ATAG présente le système de management environnemental sous la forme d'un circuit composé de sept modules (voir ci-dessus) et de deux actions: l'écobilan et l'eco-audit. Les sept modules de l'eco-audit concernent les principales répercussions que les activités d'une entreprise peuvent avoir sur l'environnement, y compris en cas de catastrophe. L'objectif de l'eco-audit est de vérifier le rendement écologique de l'entreprise. Cette activité rend possible l'identification d'une documentation relative à tout ce qui a été fait, permettant de se conformer à la loi. Si une entreprise se révèle subordonnée par l'attribution de la responsabilité, le stade final, l'eco-audit est une étude de l'engagement en matière de respect.

Les sept «modules» du système développé par ATAG Ernst & Young.

Journ. de Genève et Gaz. de Lausanne - 8 May 1995

Y.M.
European Design And Test Conference '95

The Practical Side Of Design, Test, And ASIC Technologies Are Covered With A Distinctly European Flair At The Second ED&TC In Paris.

JOHN NOVELLINO

The European Design & Test Conference and Exhibition enters its second year with a stronger emphasis on more applications-oriented presentations. Its goal is to serve both industry- and academic-oriented attendees with the latest information on advances in the design and test of electronic circuits.

The ED&TC will be held Mar. 6-9 at the CNIT Conference and Exhibition Center in Paris, site of last year's event, which was the first that combined the former European Test Conference, European Design Automation Conference (EDAC), and Euro ASIC. Conference officials cite last year's attendance, with more than half of the participants coming from outside France, as evidence of the conference's success.

A total of 136 papers are scheduled for presentation in 41 sessions, with another 28 to be displayed in the poster session. Topics cover the gamut of design and test issues, including digital and system simulation, system synthesis, sequential logic synthesis, mixed-signal design-for-test, built-in self-test, quiescent-current (IqDC) testing, FPGAs, multimedia, and circuit partitioning. Three panel sessions will feature industry experts discussing the change from traditional to more open-architecture automatic test equipment (ATE), simulation versus formal verification, and the effects of mixed-signal technology on the European microelectronics industry (see the table).

"I think the conference has certainly established itself an international event," says general chair Tony Ambler, professor of test technology at Brunel University, Uxbridge, United Kingdom. "But we have been focusing more strongly this year on attracting the more industrial- and applications-oriented type of paper." He specifically highlights the User Forum sessions, a separate track of papers to be presented in parallel with three other more academically oriented tracks.

Attendees should notice the more practical nature of the User Forum presentations. "We set up slightly different criteria for acceptance of these papers," notes Ambler. "We definitely didn't look for sales pitches. We looked for those people in industry who have something useful and interesting to say that the attendees would like to hear, but who don't have quite the time to put together the more rigorous scientific style of paper."

The User Forum papers will be published in proceedings separate from that containing the other session papers. Ambler said this arrangement allowed the User Forum papers to be printed locally with a two-month later deadline for authors. The result isn't only more applications-oriented material, but also more timely information that should better serve the industry-based attendees, he says.

A User Forum on IPaQ and QTAG (the Quality Test Action Group) is a good example, says Ambler. "This particular session is aimed at industry people rather than the more academically oriented attendee. What will it mean for you in terms of
practical realities? What sort of ATE is likely to be available? How long will it be before you can really start using it and will be the benefits for you?”


In keeping with the conference’s three-part charter, a trio of keynote speakers will address issues in CAD, testing, and semiconductors. William Lattin, senior vice president for corporate marketing at Synopsys, will lead off, discussing “Modeling, the key to design reuse.” His talk will focus on design reuse as the cornerstone of future semiconductor markets, such as embedded processors and other areas where the protection of intellectual property is important. Further merging of modeling and design reuse will occur as design complexity continues to increase, according to Lattin.

### EUROPEAN DESIGN AND TEST CONFERENCE PROGRAM

<table>
<thead>
<tr>
<th>Monday Mar. 6</th>
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</thead>
<tbody>
<tr>
<td>9:00-10:30 A.M.</td>
<td>High-level synthesis (tutorial)</td>
<td>Programmable-logic technologies, architectures, and trends (tutorial)</td>
<td>Mixed-signal test (tutorial)</td>
<td>Design and test of MCMs (tutorial)</td>
</tr>
<tr>
<td>10:30-11:30 A.M.</td>
<td>VHDL-A: Concepts and constructs of the analog extension to VHDL (tutorial)</td>
<td>I2C testing of VLSI circuits (tutorial)</td>
<td>Test generation: The practical side of DFT (tutorial)</td>
<td>Low-power design: Clocking or asynchronous control (tutorial)</td>
</tr>
<tr>
<td>Tuesday Mar. 7</td>
<td>Room A</td>
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<td>Room D</td>
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<tr>
<td>11:00 A.M.-12:30 P.M.</td>
<td>Session 1A</td>
<td>Session 1B</td>
<td>Session 1C</td>
<td>Session 1D</td>
</tr>
<tr>
<td></td>
<td>DSP and multimedia</td>
<td>Mixed-signal DFT</td>
<td>Exact methods in architectural timing organization</td>
<td>Non-trends in FPGAs (user forum)</td>
</tr>
<tr>
<td>1:30-2:30 P.M.</td>
<td>Session 1E</td>
<td>Session 1F</td>
<td>Session 1G</td>
<td>Session 1H</td>
</tr>
<tr>
<td></td>
<td>Circuit positioning</td>
<td>AT&amp;F in dead-locked live automated test (panel)</td>
<td>Combinational logic synthesis</td>
<td>Academic experiences in designing on programmable logic (user forum)</td>
</tr>
<tr>
<td>2:30-3:30 P.M.</td>
<td>Session 1I</td>
<td>Session 1J</td>
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<td>Session 1L</td>
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<tr>
<td></td>
<td>Design and tools for analog and mixed-signal ICs</td>
<td>Memory testing</td>
<td>Sequential logic synthesis</td>
<td>Low-power test issues and CGA session</td>
</tr>
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<td>Wednesday Mar. 8</td>
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<tr>
<td>9:00-10:30 A.M.</td>
<td>Session 2A</td>
<td>Session 2B</td>
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<tr>
<td></td>
<td>High-speed telecom design</td>
<td>System synthesis</td>
<td>Code generation</td>
<td>Academic ASIC presentation I (user forum)</td>
</tr>
<tr>
<td>1:30-2:30 P.M.</td>
<td>Session 2E</td>
<td>Session 2F</td>
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<tr>
<td></td>
<td>Digital and system simulation</td>
<td>Sequential ATPG and diagnosis</td>
<td>Sequential ATPG and diagnosis</td>
<td>Academic ASIC presentation II (user forum)</td>
</tr>
<tr>
<td>2:30-3:30 P.M.</td>
<td>Session 2I</td>
<td>Session 2J</td>
<td>Session 2K</td>
<td>Session 2L</td>
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<tr>
<td></td>
<td>CAD frameworks</td>
<td>Simulation versus formal verification (panel)</td>
<td>Test generation and testability</td>
<td>Industrial design methodologies I (user forum)</td>
</tr>
<tr>
<td>3:30-4:30 P.M.</td>
<td>Session 2M</td>
<td>Session 2N</td>
<td>Session 2O</td>
<td>Session 2P</td>
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<tr>
<td></td>
<td>Applications of symbolic traversal techniques</td>
<td>Handling physical constraints in architectural synthesis</td>
<td>Self-checking approaches</td>
<td>Industrial design methodologies II (user forum)</td>
</tr>
<tr>
<td>Thursday Mar. 9</td>
<td>Room A</td>
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<td>Room D</td>
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<tr>
<td>9:00-10:30 A.M.</td>
<td>Session 3A</td>
<td>Session 3B</td>
<td>Session 3C</td>
<td>Session 3D</td>
</tr>
<tr>
<td></td>
<td>Design methodologies</td>
<td>Power and delay issues in logic synthesis</td>
<td>BIST methodologies</td>
<td>New electronics: The impact of ASIC high-level design methodology, Part I: Case studies (user forum)</td>
</tr>
<tr>
<td>1:30-2:30 P.M.</td>
<td>Session 3E</td>
<td>Session 3F</td>
<td>Session 3G</td>
<td>Session 3H</td>
</tr>
<tr>
<td></td>
<td>New developments in logic nonintrusive and verification techniques</td>
<td>New developments in mixed-signal verification techniques</td>
<td>Test preparation for mixed-signal systems</td>
<td>New electronics: The impact of ASIC high-level design techniques on design methodology, Part II: Discussion forum (user forum)</td>
</tr>
<tr>
<td>2:30-3:30 P.M.</td>
<td>Session 3I</td>
<td>Session 3J</td>
<td>Session 3K</td>
<td>Session 3L</td>
</tr>
<tr>
<td></td>
<td>Hierarchical layout</td>
<td>Modeling and design of ASICs (application-specific instruction-set processors)</td>
<td>Delay testing and diagnosis</td>
<td>Industrial test and testability strategies (user forum)</td>
</tr>
<tr>
<td>3:30-4:30 P.M.</td>
<td>Session 3M</td>
<td>Session 3N</td>
<td>Session 3O</td>
<td>Session 3P</td>
</tr>
<tr>
<td></td>
<td>New applications of analog simulation algorithms</td>
<td>Design problems in pipelines</td>
<td>I2C testing</td>
<td>Error detection, debugging and test equipment (user forum)</td>
</tr>
</tbody>
</table>
He notes that increasing design complexity and time-to-market pressure are already reshaping the electronic design industry, including component modeling. As new tools become available, modeling requirements change. In one example, he cites how the wide use of ASICs and FPGAs has changed model requirements for board and system design and created a need for different types of models like VHDL source models, compiled binary models, and hardware models. The types of models required are influenced by the degree of intellectual property protection needed, says Lattin.

The test area will be handled by Keith L. Barnes, president of Integrated Measurement Systems Inc., Beaverton, Ore. In his address, "The renaissance of test," he will describe how the test industry has matured in recent years and is operating under new value paradigms. "For many years, the test industry has been accused of adding value to the manufacturing or product-development process," explains Barnes. "And as the cost of testers has soared in recent years, so has the cost of the devices tested."

In response, vendors have specialized their testers for specific market areas and developed new design-for-test and test-development software.

"With today's computing capability and simulation capability, we've moved test development into a virtual world," says Barnes. "This is really where the renaissance is taking place. We are putting together products for this virtual world that will allow customers to reduce their time to test, time to market, and therefore total cost."

Jean-Philippe Dauvin of SGS-Thomson Microelectronics, France. Dauvin will discuss BiCMOS semiconductor market trends. He notes that the sharp recovery of the last two years was driven by factors that also will affect the industry's future. Although we are in the same cycle, the upswing seems to be leveling off, he says, and future cycles will be less pronounced.

Much of the recent growth in the semiconductor market was due to technological progress, which was linked to the rapid increase in the semiconductor content of systems, says Dauvin. This trend will continue, he predicts, with semiconductors rising from 14% of total value of systems to 20% by the year 2000.

The European market is regaining momentum, says Dauvin, with new products like cellular telephones allowing the continent to maintain its 15%-20% share of the worldwide sales of semiconductors. Lastly, Dauvin points out that investment by semiconductor manufacturers totaled nearly $32 billion last year, representing almost 20% of sales. Manufacturers must continue to invest, between $700 and $800 million a year to be successful in the semiconductor business, he concludes.

Along with the technical sessions, the conference's organizers have put together an interesting set of eight tutorials, scheduled for Monday, March 6. Each is three hours long, and one allows attendance at a morning and an afternoon session.

One tutorial deals with a particularly hot topic for designers of portable equipment. In "Low-power design—clocked or asynchronous control," S.B. Furber of the University of Manchester, United Kingdom, will question the use of globally clocked circuits and make a case for asynchronous control as a power-saving technique. Although asynchronous logic is considered hard to design and test, Furber will present information on recent advances that have eased design problems and made asynchronous logic feasible for large-scale circuits.

Designers working on analog and mixed-signal circuits may find "VHDL-A: Concepts and constructs of the analog extension to VHDL" of
Laboratorul TIMA
din Grenoble - un
posibil model al
cercetării științifice

Ioan C. Bacivarof
Universitatea "Politehnica" București

În contextul dezbatelor - firești pentru această perioadă de transiție-privind perspectivele cercetării științifice, autohtone și modalitățile de organizare și finanțare a acestia, credem că nu este lipsită de interes prezentarea uneia dintre unitățile de eliber ale cercetării științifice din Franța: laboratorul TIMA din Grenoble, la activitățile căruia un avut primul să participă în mai multe rânduri în cadrul unor proiecte educaționale și de cercetare științifică ale Uniunii Europene. Se știe că Franța este una dintre părțile care se află în topul cercetării științifice mondiale (locul 4, după Japonia, S.U.A. și Germania), alocând anual caa. 2,5% din PIB în acest scop; conform unor statistiche recente, 51% din resursele necesare cercetării științifice francoze provin din fonduri publice, iar restul din sectorul privat.

Situat în piețele oraș Grenoble, important centru universitar și considerat ca unul dintre polii cercetării științifice în domeniul ingineriei din Franța (adesea ca importanță după Paris), laboratorul TIMA (Technici ale Informației și ale Microelectronicii pentru Arhitecturi de calculatoare) are o dublă subordonare, fiind afiliat atât organismului național francez în domeniul cercetării științifice, Centre National de la Recherche Scientifique (CNRS), cât și principalelor universităților din Grenoble (Institut National Polytechnique și Universitate Joseph Fourier). Este o soluție eficientă, des utilizată în părăzitele dezvoltate economice, deoarece permite o valorificare sinergică a inteligențelor creațoare atât ale profesorilor și cercetătorilor, cât și ale doctoranților și studentilor din ciclul de studii aprofundate (DEA), pentru soluționarea unor teme de cercetare științifică de vârf.

Laboratorul TIMA are o tradiție de peste 20 de ani în cercetarea științifică de înalt nivel, fiind la ora actuală structură în peste mii de recetați și asușai:
- Calitata sistemelor integrate complexe (coordonator: dr. Louis Balme);
- Proiecția sistemelor integrate (coordonator: prof. dr. Alain Guyot);
- Sisteme integrate fiable (coordonator: dr. Michael Nicolaidis);
- Sistemul al nivelului sistem (coordonator: dr. Ahmed Jermya);
- Metode de testare avansate (coordonator: prof. dr. Bernard Courtois și dr. Marcelo Lubaszewski);
- Diagnoza sistemelor complexe (coordonator: dr. Meryem Morzojou).

Directorul laboratorului, prof. Bernard Courtois, personalitate științifică de prim rang - între altele, președinte Asociației pentru Proiectarea Aplicată în Electronică (EDAA), coordonator al numeroase conferințe și congresuri de științe și editor ai unei reviste internaționale despre tehnologie, a reușit ca, prin un stil managerial dinamic, să impute laboratorul TIMA în topul cercetării științifice europene.

Vom încerca în cele ce urmează să descriem câteva dintre "secretele" succesului TIMA:

* Ancora activității în domeniul prioritar ale cercetării științifice aplicative europene și mondiale, cum sunt proiectarea asistată de calculator a sistemelor electronice complete și în principal a circuitelor VLSI, calitatea și siguranța în funcționare, inclusiv sinteza sistemelor tolerantă la defectii, testarea automată și diagnoza tehnică; aceasta a făcut posibilă finanțarea cercetărilor laboratorului, în proporție de 50%, prin intermediul contractelor cu parteneri industriali importanți (SGS Thompson, France Telecom, Aerospațiale etc).

* Competența managerială - dar mai ales științifică - a scriitorilor, folosind rândul lor personalitatea științifică binecunoscuta, prezentă în domeniul lor de activitate; este suficient să menționăm în acest sens că prof. Louis Balme este unul dintre fondatorii primii proiecte europene în domeniul calității sistemelor complexe - EPiQCS, Dr. M. Nicolaidis este președinte confeționatul IEEE Computer Society în domeniul testării etc.

* Participarea activă (prin comunicare sau prin conducere de secții sau grupuri de lucru) la toate reuniunile științifice naționale și internaționale importantă în domeniul diferitelor membri ai TIMA, ca modalitate eficientă de a face cunoștiune știiințelor proprie, dar și de a stabili conexiuni benefice pentru colaborările viitoare ale laboratorului.

* Lungă deschidere a TIMA pentru cooperare științifică și educațională, aceasta fiind premiata necesară soluționării unor teme de care ar fi prezentă. Este semnificativ faptul că această cooperare are în vedere atât științele cu tradiție în domeniul cercetării (existând cooperatii cu principalele universități și centre de cercetare vest-europene, în cadrul unor proiecte europene comune - ESPRIT, COMETT - sau acorduri bilaterale cu universități americane), cât și, în științei, cu universitățile din țări central și est-europene (în cadrul unor proiecte europene comune ca PECO, COPERNICUS, TEMPUS etc.).

Ceea ce impresionează în cadrul TIMA este eficiența denotată a activității într-un cartier colectiv, de la coordonatorul acesteia și până la secretarele poliglotice și bine cunoscute ale tehnicilor de procesare și transmitere electronice și informații. Laboratorul funcționând asemeni unui angajat bine pus la punct, în care nici o activitate nu este graziosă sau formală, dar, mai ales, trebuie remarcată culturarea, faptă a se face învățată disciplina, a unei atmosfere de încredere, cooperare și armonie, care face ca fiecare membru al laboratorului să se simtă ca într-o "mâna familie"; reuniunile anuale ale TIMA, ca și activitățile sociale comune, sunt numai o fațetă a acesteia. Este și acesta unul dintre cele mai bune...
VIII.3 Social life

Recently, the Laboratory had the pleasure to congratulate some of its members for marriage and births.

Have got married:

- Lydie HEUSCH (SANZ), 25 May 1991
- Masaki NITO, 8 June 1991
- Mokhtar BOUDJIT, 13 June 1992
- Pascale VERGUIN (DULIEUX) 4 July 1992
- François MARTIN, 15 August 1992
- Ahmed Amine JERRAYA 26 September 1993
- Patricia SCIMONE (CHASSAT) 17 juin 1995
- Sylvaine EYRAUD (LAYE) 24 juin 1995

The following will be descendants of Laboratory's members:

- Emeric AMIELH, 12 June 1991
- Luc BERGER SABBATEL, 13 July 1991
- Aurélie GARNIER, 7 September 1991
- Anna KOLARIK, 20 September 1991
- Florian HEUSCH, 2 November 1991
- Moussab BEN OTHMAN, 21 November 1992
- Thaïs CASTRO ALVES, 2 October 1993
- Natasha LUBASZEWSKI 3 May 1993
- Aladin SKAF 2 August 1994
- Gabriel GARNIER 28 August 1994
- Andressa LUBASZEWSKI 11 December 1994
- Lydia JERRAYA 3 February 1996
- Ceyla SIMEU 14 March 1996

Some have even found their wife/husband in the Laboratory itself:


As for funds, the Laboratory has recurrent social events and exceptional social events. The meehoun's party is a traditional annual party. The Laboratory has been a few times horse-riding, even those being very beginners. Visitors are often taken for walks in the mountain. The following pictures are examples of this social life.
Picture 4: Horse-riding across Vercors
Picture 5: Annual party
Picture 6: Walk in the mountain with visitors: for example Janusz RAJSKI, McGill University (1st plan, with a hat) and his family.

Picture 7: Skiing excursion
Picture 8: The TIMA football team (that beat CSI 5-0 in June 1992)