TIMA Laboratory
ANNUAL REPORT 1994
B. COURTOIS - April 1995

Techniques de l'Informatique et de la Microélectronique pour l'Architecture d'Ordinateurs
Techniques of Informatics and Microelectronics for Computer Architecture
ABSTRACT

This is the 1994 annual report of the TIMA Laboratory (Techniques of Informatics and Microelectronics for Computer Architecture). The Laboratory is approximately 60 people large.

The Laboratory is organized in research groups: Analog Test Methods (ATM), Diagnosis of Complex Systems (DCS), Integrated Systems Design (ISD), MicroSystems (MCS), Quality of Complex Integrated Systems (QCS), Reliable Integrated Systems (RIS), System Level Synthesis (SLS). The Laboratory is also hosting the CMP Service, serving chips and microsystems fabrication.

Key achievements in 1994 have been theoretical and practical results on the design of self-checking analogue circuits, the full range operation of ARCHIMEDES and BARMINT Basic Research projects on Testing and Microsystems, respectively, and the approval of a Basic Research project on Analog and Mixed-Signal Testing, AMATIST. Also, the architectural synthesis software AMICAL has been transferred to SGS-Thomson for industrial use. The Laboratory is organizing in 1995 the System Synthesis Symposium in Cannes and focused Workshops on Mixed-Signal Testing, On-Line Testing and Thermal Investigations.

This year, the report has been reorganized into 8 main sections including the Research and Service activities, the Resources and the Technology Transfer activities.

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<table>
<thead>
<tr>
<th>CONTENTS</th>
</tr>
</thead>
</table>

### I  
**OVERVIEW - GENERAL INFORMATION**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>I-1</td>
<td>ORGANIZATION</td>
</tr>
<tr>
<td>I-2</td>
<td>RESEARCH THEMES</td>
</tr>
<tr>
<td>I-3</td>
<td>SOME PAST AND RECENT REALIZATIONS OF THE LABORATORY</td>
</tr>
<tr>
<td>I-4</td>
<td>SOME DATA ON THE GRENOBLE’S ENVIRONMENT</td>
</tr>
</tbody>
</table>

### II  
**RESEARCH ACTIVITIES**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>II-1</td>
<td>ANALOG TEST METHODS (ATM)</td>
</tr>
<tr>
<td>II-2</td>
<td>DIAGNOSIS OF COMPLEX SYSTEMS (DCS)</td>
</tr>
<tr>
<td>II-3</td>
<td>INTEGRATED SYSTEMS DESIGN (ISD)</td>
</tr>
<tr>
<td>II-4</td>
<td>MICROSYSTEMS (MCS)</td>
</tr>
<tr>
<td>II-5</td>
<td>QUALITY OF COMPLEX INTEGRATED SYSTEMS (QCS)</td>
</tr>
<tr>
<td>II-6</td>
<td>RELIABLE INTEGRATED SYSTEMS (RIS)</td>
</tr>
<tr>
<td>II-7</td>
<td>SYSTEM LEVEL SYNTHESIS (SLS)</td>
</tr>
</tbody>
</table>

### III  
**SERVICE ACTIVITY : CMP**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
</table>

### IV  
**RESOURCES**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>IV-1</td>
<td>HUMAN RESOURCES</td>
</tr>
<tr>
<td>IV-1.1</td>
<td>MEMBERS OF THE LABORATORY</td>
</tr>
<tr>
<td>IV-1.2</td>
<td>BIOGRAPHIES OF STAFF MEMBERS</td>
</tr>
<tr>
<td>IV-1.3</td>
<td>CURRICULUM VITAE OF DOCTORATE CANDIDATES</td>
</tr>
<tr>
<td>IV-2</td>
<td>EQUIPMENTS</td>
</tr>
<tr>
<td>IV-3</td>
<td>FINANCIAL RESOURCES</td>
</tr>
</tbody>
</table>

### V  
**COOPERATIVE ACTIVITIES**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>V-1</td>
<td>CONTRACTS</td>
</tr>
<tr>
<td>V-2</td>
<td>EUROPEAN PROJECTS</td>
</tr>
<tr>
<td>V-2.1</td>
<td>SUMMARY</td>
</tr>
<tr>
<td>V-2.2</td>
<td>DETAILS</td>
</tr>
<tr>
<td>V-3</td>
<td>COOPERATION AGREEMENTS</td>
</tr>
<tr>
<td>V-4</td>
<td>INTERNATIONAL ACTIVITIES</td>
</tr>
<tr>
<td>V-5</td>
<td>AWARDS AND DISTINCTIONS</td>
</tr>
</tbody>
</table>
VI TECHNOLOGY TRANSFER ACTIVITIES

VI-1 TECHNICAL TASKS
   VI-1.1 INDUSTRIAL TRANSFERS 163
   VI-1.2 PATENTS 163
   VI-1.3 INDUSTRIAL CIRCUIT FABRICATION 163
   VI-1.4 CONSULTING 164

VI-2 EDUCATIONAL TASKS
   VI-2.1 COURSES ORGANISATION 164
   VI-2.2 COURSES AND SEMINARS 166
   VI-2.3 SUPPORT OF FOREIGN UNIVERSITIES TEACHING PROGRAMS 167
   VI-2.4 PARTICIPATION IN EU EDUCATIONAL PROGRAMS 167
   VI-2.5 UNIVERSITY/INDUSTRY JOINT RESEARCH PROGRAMS 168

VII PUBLICATIONS

VII-1 BOOKS AND MAGAZINES 169
VII-2 CONFERENCES AND WORKSHOPS 171
VII-3 THESIS 183
VII-4 REPORTS 184
VII-5 PATENTS 184

VIII MISCHELANNEOUS

VIII-1 WHAT DID THEY DO AFTER GRADUATING FROM THE LABORATORY (1984-1994) 187
VIII-2 PRESS ARTICLES IN 1994-1995 195
VIII-3 SOCIAL LIFE 217
I - OVERVIEW - GENERAL INFORMATION

I-1 Organization

Since 1971 this research organization targeted successively the design of the following pieces of hardware:

- Computers:
  + the geo-physical machine GEOPROCESSOR (1970/1975)
  + the PASCAL machine PASCHILL (1972/1981)

- Group microprocessor architectures:
  + electronic exchange system CANOPUS
  + the CORAIL machine
  + the CRESUS project

- Microprocessor type circuits:
  + microsequencer MSQ
  + microprocessor 8 bits NMOS P68
  + microcomputer 4 bits SOS MOM 400
  + the MOSAIC project for the architecture of VLSI systems
  + series line control by LISA microcontroller
  + microprocessor 8 bits POPY
  + microprocessor 8048 CMOS
  + microcontroller COBRA
  + mathematical coprocessor FELIN
  + compiled microprocessor 6502
  + MAPS controller
  + 1553 controller

- AI oriented machines
  + OPALE machine
  + LAIOS lattice
  + SPAN mechanisms
  + SYMBION architecture

- VLSI

- Macrosystems and Microsystems.

In 1994, the Laboratory was organized in 7 research groups, as listed below:

+ Analog Test Methods (ATM), B. COURTOIS / M. LUBASZEWSKI
+ Diagnosis of Complex Systems (DCS), M. MARZOUKI
+ Integrated Systems Design (ISD), A. GUYOT
+ MiCroSystems (MCS), B. COURTOIS / J.M. KARAM
+ Quality of Complex Integrated Systems (QCS), L. BALME
+ Reliable Integrated Systems (RIS), M. NICOLAIDIS
+ System Level Synthesis (SLS), A.A. JERRAYA

In addition, the Laboratory is hosting the CMP service activity.
I-2 Research themes

Each topic of the research group is briefly described below:

* Analog Test Methods (B. COURTOIS, M. LUBASZEWSKI)
  This research group addresses the following topics:
  + boundary scan for on line testing
  + testability of analog and mixed signal circuits
  + design of radiation hardened circuits and sensors
  + deterministic built-in self test
  + multi-level test pattern generation

* Diagnosis of Complex Systems (M. MARZOUKI)
  This research group addresses the following topics:
  + knowledge-based approaches and non-classic logic for test and diagnosis
  + MCM and partial boundary scan board test and diagnosis
  + mixed-system behavioral modeling
  + analog fault diagnosis
  + synthesis for testability

* Integrated Systems Design (A. GUYOT)
  This research group addresses the following topics:
  + arithmetic operators
  + full custom VLSI design
  + on-line operators
  + application of redundant number systems
  + digital signal processing
  + arithmetic operators testing

* MiCroSystems (B. COURTOIS, J.M. KARAM)
  This research group addresses the following topics:
  + silicon compatible micromachining
  + CAD tools for micromechanical systems
  + microsystems for safety critical applications
  + thermal modeling

* Quality of Complex integrated Systems (L. BALME)
  This research group addresses the following topics:
  + modelling of complex integrated systems
  + total quality management window concept
  + surface mounted technology
  + automatic testing equipment
  + smart power card

* Reliable Integrated Systems (M. NICOLAIDIS)
  This research group addresses the following topics:
  + self-checking circuits
  + built-in self test
  + test patterns for regular structures
  + CAD tools for testability
* System Level Synthesis (A.A. JERRAYA)
  This research group addresses the following topics:
  + hardware/software co-design
  + system-level modelling
  + partitioning
  + communication synthesis
  + behavioral synthesis based on VHDL
I-3 Some past and recent realizations of the Laboratory

The following pictures illustrate some past and recent realizations of the Laboratory.

a) Cooperation with THOMSON led to the design of a self-checking, self-testing circuit (CMOS, 1.2 μ, 2 metallization layers, 650,000 transistors). The circuit is testable at the "transistors, metallizations, etc..." level (1985).

b) The SYCO silicon compiler took as input a behavioural ("Pascal like") description of the algorithms to be implemented in the silicon. b-1 is a 6502 CMOS control section compiled by the CPC specialized control section compiler; b-2 is a 6502 NMOS data path compiled by the APOLLO specialized datapath compiler (ca. 1988).

c) Electron-beam testing has been experimented through two equipments: a CAMECA ST-15 electron-beam tester and a JEOL 35C scanning electron microscope equipped for voltage contrast. Those equipments have been served by a SUN and an IBM workstation, respectively (1987-1993).

d) The FELIN circuit was a design resulting from a cooperation with the Parallel Algorithmic Laboratory. It is aimed at the calculation of elementary functions like sine, cosine, etc... The circuit involved approximately 100,000 transistors, fully generated by a program describing the circuit (1987).

e) CMP National Service gives the possibility to Research Centers, Universities and Commercial Firms to have their circuits manufactured. The Université Catholique de Louvain, CNET-CNS, THOMSON, MHS, ES2, TCS, AMS have manufactured bipolar, GaAs, NMOS and CMOS circuits for the CMP since 1981. One 4 inches wafer holds 73 CMOS different projects (15 wafers) and one 5 inches wafer holds 40 CMOS projects (5 wafers). Both have been processed by MHS, in 1986 and 1987, respectively.

f) The computing room regrouped computers that were not distributed in offices. Here are several SM 90, a SPS 9, and a MicroVAX. The air conditioned room had been fully remodeled in 1987 (electric power, floor, etc...). Today, all computers are distributed in offices.

g) In the past, computers have been designed. g-1 shows the GEOPROCESSEUR (1970) which resulted from a cooperation with IFP, g-2 depicts the PASCHELI (1976) language-oriented computer, and g-3 shows the CANOPUS (1980) system which resulted from a cooperation with CNET-LAA. Presently the computer architecture projects are dealing with parallelism and with a logic - numeric integration.

h) ADELAIDE was a project aimed at testing PCB populated by SMT devices. A prototype demonstrated the feasibility of an ATE, which uses extensively anisotropic elastomer conductors. Such a tool would allow a resolution of 10/1000 inches. The project has now been passed to industry.

i) Circuit synthesized by AMICAL (1993). This circuit is a PID synthesized by AMICAL (300 behavioral VHDL lines as input, 4000 RTL VHDL lines as output) feeding a commercial logic synthesis tool generating 50,000 transistors (20 mm², 8μ CMOS). Design time: 1 week. This design results from a hierarchical use of AMICAL. One of its components is a fixed point arithmetic unit that has been designed using AMICAL.

k) Microelectronics for Physics. BiCMOS wafer from CMP.

l) Micromachining by CMP. Process at industrial manufacturers, post-process at Central Laboratories.
a - Participation to a THOMSON project

c - Electron beam testing

d - FELIN project

e - CMP service

f - computing room

h - SMT PCB tester

Picture 1
1 - 6502 Control section

2 - 6502 Datapath

b - SYCO silicon compiler
1 - GEOPROCESSEUR computer

2 - PASCHLL computer

3 - CANOPUS Distributed system

g - Past computer projects
i - Circuit synthesized by AMICAL.

j - GaAs wafer from CMP.
1 - Micromachining by CMP

k - Microelectronics for Physics
I-4 Some data on Grenoble's environment

Grenoble offers a very good environment in terms of Education, Research, High Tech Activities, Industry.

* **Education**

Grenoble has been awarded the "European University" title within the University 2,000 Project.

* 40,000 students
* 5,500 foreign students
* 1,500 science degrees awarded each year
* 1,000 engineers graduate each year
* 600 "Erasmus" scholarship students
* 1 International secondary school

* **Research**

Grenoble is the first French research center in Engineering Sciences, the second in Physics, the third in Mathematics.

* 8,500 researchers (the largest concentration of CNRS researchers in Engineering Sciences after Paris)
* 1,500 foreign researchers
* 250 laboratories
* 5 European research centers:
  - ESRF, European Synchrotron Radiation Facility
  - ILL, Laue Langevin Institute
  - IRAM, Millimetric Radio Astronomy Institute
  - SNCI, National Service for Intense Magnetic Fields
  - EMBL, European Molecular Biology Laboratory
* 4 National research centers
  - CNRS, National Center for Scientific Research
  - CENG, Grenoble Nuclear Research Center
  - CNET, National Center in Telecommunications Research
  - CRSSA, Research Centre for the Army Health Services
* 1 research center of international proportions acquired every 10 years since 1946

* **High tech Activities**

* Electronics 470 industrial companies, 13,250 jobs
* Biomedical technologies 104 industrial companies, 2,600 jobs
* Imaging technologies 50 industrial companies, 800 jobs
* 1 Technopole of 65 ha housing 200 companies and 5,000 jobs (ZIRST Meylan)

**Industry**

* 3,500 companies created each year
* 64 foreign companies
* 1 Business District to welcome company headquarters and professional services (EUROPOLE)

**Electronics**

* Education: Engineering schools of INPG and UJF
  - ENSERG
  - ENSIEG
  - ENSPG
  - ENSEEG
* Research Laboratories of CNRS, INPG, UJF
  - ARTEMIS
  - CSI
  - LEMO
  - LEPES
  - LMGP
  - LPCS
  - TIMA
* Infrastructures for research and education
  - CIME
  - CMP

* Applied research LETI, a division of the French Atomic Energy Commission (CEA)
  - CNET, a laboratory of France Telecom

**Industry**

SGS Thomson, Thomson Specific Components, Thomson Electronic Tubes, Thomson Consumer Electronics, Thomson LCD, Merlin Gerin, ANACAD, AURIS, Dolphin Integration, SOFRADIR, RADIALL

**History**

43 B.C.: 1st mention of CULARO, a small town modestly built by the Celts to get across the Isère river, by Lucius Munatius Plancus in his correspondence to Ciceron.

III century a.c.: Construction of the first rampart.

379: Emperor Gratien promotes CULARO to the rank of chief town city and gives it its name: GRATIANTINOPOLIS.
VI century: Construction of a Christian funerary complex on the right bank of the Isère river.

1012: The Saint-Laurent group (right bank) is given to the benedictine monks of Saint Chaffre en Velay: founding of the Saint-Laurent priory and then, the development of a suburb.

c.1140: Rebuilding of the cathedral and its cloister.

1219: Flood; the bridge is taken away.

1228: Construction of the Collegiate Church Saint André: the "Dauphins" set up their administration at Grenoble.

1339: Creation of a University in Grenoble, including four sections: medicine, liberal arts (sciences and literature), canon law and civic law.

1391-1418: Construction of the Island Tower, first Town Hall.

1453: The setting up of the parliament of Grenoble: the town is officially recognised as a regional capital.

1593-1606: Construction of the wall of Lesdiguières.

1709: Birth of Jacques DE VAUCANSON, biomechanist. His automata (Le Joueuse de Flute, 1738) were aimed at "reproducing means in view to obtain the experimental intelligence of a biological mechanism".

1712: Birth of Joseph FOURIER, mathematician and prefect of Isère department. In 1811 Joseph FOURIER sets up the Faculty of Sciences. In 1987, the Scientific, Technologic and Medical University of Grenoble will take the name "Université Joseph FOURIER".

1783: Birth of Henri BEYLE, so-called STENDHAL, novelist.

7 June 1783: Day of the "Tuiles".

c. 1830: Construction of the HAXO fortifications.

1869: Invention of the hydro-electric power, the "White Coal", by Aristide BERGES.


1955: Grenoble Nuclear Research Center (CENG).

1963: First laboratory integrated circuit at LETI.

1965: First industrial integrated circuit at SESCOSEM. First computer LAG/INPG-MORS.

1966: Laîche Langevin Institute (ILL).

1970: Louis NEEL is Nobel Prize in Physics. Louis NEEL has been President of Institut National Polytechnique de Grenoble (formerly Institut Polytechnique de Grenoble), from 1954 to 1976; he is now Honorary President of INPG.


1985: Nobel Prize awarded to Klaus von Klitzing.

1986: European Synchrotron Radiation Facility (ESRF).

1988: Research Centre for the Army Health Services (CRSSA).

1994: The European Synchrotron Radiation Facility is available to research scientists from virtually all countries.
II - RESEARCH ACTIVITIES

II-1 Analog Test Methods (ATM)

Group Leaders: B. COURTOIS / M. LUBASZEWSKI
(e-mail for B. Courtois: Bernard.Courtois@imag.fr)
(e-mail for M. Lubaszewski: Marcelo.Lubaszewski@imag.fr)

Members: B. COURTOIS, P. DULIEUX-VERGUIN,
V. KOLARIK*, M. LUBASZEWSKI**, S. MIR, C. NIELSEN, F. VINCI DOS SANTOS

Research areas:

This group investigates the testability of analogue and mixed-signal circuits, printed circuit board testing, design of radiation-hardened circuits.

Contracts:

European: ARCHIMEDES (ESPRIT-III Basic Research),
AMATIST (ESPRIT-III Basic Research),
NDIMST (ESPRIT/NSF cooperation).

Topics:

This group investigates several advanced topics in testing, design for test, built-in test of analog/mixed-signal circuits and systems.

II-1.1. Unified Testing of Analogue and Mixed-Signal Integrated Circuits

Members: V. KOLARIK, S. MIR, M. LUBASZEWSKI, C. NIELSEN and B. COURTOIS

The test and diagnosis of analogue circuits is still an open problem. Unlike digital circuits, analogue ones operate with signals continuous in time and levels and thus the decision if the circuit performs a good function cannot be made upon the simple comparison to a "gold" circuit (that is usually the case for digital circuits). An important issue is thus test robustness taking into account the element tolerances.

II-1.1.1. Self-Testing and Self-Checking Fully Differential Circuits

The use of fully differential circuits in analogue designs has contributed both to increase the dynamic range and to ease the design. In addition it leads to a first order cancellation of the charge injection offset and capacitance/voltage coefficients. Thus this class of circuits is widely used in high performance designs where the primary issue is the high linearity and/or the signal-to-noise ratio (eg. continuous filters, switched-capacitor filters, A/D converters).

Taking into account that all signals crossing a fully differential linear circuit are symmetrical with respect to the analogue ground (middle of power rails), a balance property is defined. This property is such that:

* Now with the Technical University of Brno - Czech Republic.
** Now with the Federal University of Rio Grande do Sul - Brazil.
the inputs and outputs of every circuit stage belong to the space of common mode signals that do not exceed a given tolerance (right figure 1), and
- the operational amplifier inputs are virtually connected to the analogue ground (left figure 1).

Figure 1: Fully differential circuit stage (on the left), differential code space (on the right)

Considering the balance property of fully differential circuits and the other properties necessary for self-testing and self-checking circuits, solutions for the following problems are searched:
- the choice of observation nodes to ensure the off-line detection and diagnosis of faults internal to the functional parts of the circuit;
- the choice of input stimuli to ensure the off-line detection and diagnosis of faults affecting the functional circuit and the checker;
- the choice of observation nodes to ensure the on-line detection of faults affecting the behaviour of the functional parts of the circuit; and,
- the design of analogue checkers that do not introduce important performance degradation, that do not result in high surface overheads and that generate error indications compliant with those of digital checkers.

A switched-capacitor biquadratic filter was implemented using the AMS 1.2μm CMOS technology as the means to validate the self-testing and self-checking properties of fully differential circuits. The design includes fault-free copies (with and without checker) and many faulty copies of the filter (all with checker) in order to evaluate both the fault coverage and the performance degradation introduced by our analogue testing strategy. A very small analogue checker was used that is primarily aimed for on-line testing and that results in less than 3% surface overhead. Although the filter design has presented a problem in terms of analogue ground deviation, after some external compensation all the fault simulation results could be obtained in practice by observing the error indicators of the fabricated chips. The checker connection to the biquadratic filter produced a worst case performance degradation of about 2% for the range of normal operation frequencies.

Since our ultimate goal is to ensure through an unified strategy all the tests necessary during the circuit’s lifetime, the design of waveform generators for BIST and the possibility of sharing the checkers between the off-line and the on-line testing phases are also investigated.

II-1.1.2. Self-Exercising Analogue Checkers with Absolute and Relative Tolerances

The design of checkers suitable for concurrent error detection in analogue and mixed-signal circuits is addressed. These checkers can on-line test duplicated and differential analogue functional circuits and comply with existing digital self-checking parts.

In order to take into account the imperfections resulting from the implementation of the checking circuitry, we define a coded sampled-signal composed of successive samples. Each sample falls in one of the following regions: code sample, proxy sample and noncode sample. Although a proxy sample is not exact, it is acceptable during a certain time interval before a precise off-line testing or tuning procedure is applied. Since the proxy sample value is close to the correct one, the checker does not go outside the safe operation region.
In general the design of a checker can be based on a comparator replicated in time or in space. We bring in an intermediate solution based on a voltage comparator with a duplicated input stage and a single output stage (see the figure 2). The input signal is first preamplified by two amplifiers with different offset values $+e$ and $-e$. The results, $x_1$ and $x_2$, are subtracted and compared with the reference $x_i$. Different implementations were studied. The first one is based on an operational amplifier in an open-loop configuration, and the second one is based on a chain of inverters followed by a latch.

![Figure 2: Window comparator with duplicated input stage](image)

In order to ensure that the first erroneous output of the functional circuit is signalled via the checker (totally self-checking goal), the checker must be designed such that it signals its own faults, or it maps noncode inputs into noncode outputs even when it is affected by undetected faults. In order to achieve this property, we propose that a checker off-line testing phase is integrated into the circuit. This testing phase would periodically apply two noncode samples to the checking circuitry inputs.

The analogue checkers so far considered implement an absolute acceptance window of width $2e$. In this case, the deviation accepted for a coded signal is the same for large and for small signal values. While this approach is acceptable for signals that have a small range of amplitudes, it can become too constraining for signals with a larger swing. For large signals, errors would be signalled even for small relative deviations. To avoid this problem, the acceptance window must be made relative to signal amplitude. An important advantage of implementing this new functionality is that error detection can be directly linked to relative deviations of circuit components since it does not depend on signal amplitude. A sample-and-compare checker for testing relative deviations in differential signals and the modifications which are required for implementing its counterpart for duplicated signals have been proposed.

In respect to the checkers based on full duplication and on time replication, the partial space replication employed in our absolute tolerance checkers is a suitable approach for saving silicon surface and for improving the comparison speed. Nevertheless, a lower bound for the window width exists, below which the comparison slows down rapidly. For analogue applications requiring a small voltage swing, an absolute tolerance checker is in general a practical solution. If the analogue circuit has large swings, it may be necessary to move to relative tolerance checkers. In any case, the choice of checker strongly depends on each particular application. Although relative tolerance checkers appear to present advantages with respect to absolute tolerance checkers, it is necessary in practical implementations to provide means of dealing with glitches which can occur for very small signals.

II-1.1.3. Automatic Test Pattern Generation for Linear Analogue Circuits

This work is concerned with the generation of test patterns for linear analogue circuits. Over the recent years, the growing importance of mixed-signal systems has emphasised the lack of tools which can address the test of the analogue parts. Few works aimed at test generation for analogue circuits have been published until now.

Test Generation Procedure

An analogue test generation procedure is currently under development in the research group. The work has been initially targeted to linear analogue circuits which include both frequency-dependent (e.g. active filter) and frequency-independent (e.g. difference amplifier) circuits.
The transfer function of the linear circuit together with a list of the faults to be analysed and the test measures that can be considered are given to the system. The faults that can be considered include AC hard/soft faults in all circuit components. The system computes the effect of all faults in the test measures.

Next, the procedure automatically selects a minimal set of test measures and a minimal set of frequency tests which guarantee maximum fault coverage and maximal diagnosis for the faults in the fault list. Faults which result in non-linear behaviour of the circuit can also be considered if their effect is frequency-dependent.

Evaluation of the Procedure

Currently, a tool has been produced using the Sicstus Prolog environment for rapid prototyping. The tool has been applied to several self-test approaches which have been used worldwide for analogue circuits. With this, it has been possible to validate the prototype tool at the same time that the potential of the different self-test approaches with respect to both fault detection and fault diagnosis has been evaluated.

As an example, consider the biquadratic filter of figure 3. An input signal \( I \) is filtered by the circuit and the output signal \( Y \) is produced. The case of hard faults (shorts and opens) in all passive components is considered as an example. The circuit is frequency-dependent and therefore most faults are not observable in the whole frequency range.

![Figure 3 - Example of biquadratic filter](image)

A known method for the self-test of analogue circuits consists on embedding special circuitry which detects deviations of circuit parameters during an off-line test. Examples of these detectors include gain and phase detectors as shown in the example of figure 4. The input \( I \) and output \( Y \) from the circuit of figure 3 are fed to the detectors. The test circuitry compares the gain and phase of the circuit with nominal tolerance values of gain and phase deviations for a given input \( I \).

![Figure 4 - Typical off-line test approach](image)
The fault detection and fault diagnosability of these approaches can then be evaluated by means of the ATPG tool developed. TABLE I(a) shows the results of the test procedure when a gain deviation detector is considered at the output of the circuit. A fault is detected if the gain deviation exceeds in $\pm$ 100 mVolts the nominal value. It can be seen that four frequencies are required to detect all faults and to achieve maximum fault diagnosis with this approach. TABLE I(b) shows the results when a phase deviation detector is used instead. A fault is detected when the phase deviation exceeds $\pm$ 10 degrees. In this case, one fault is not detectable at all.

![Table I(a)](image)

![Table I(b)](image)

**TABLE I - Test sets generated:**
(a) for gain detector, and
(b) for phase detector

**Further work**

Further work is still required in a number of directions. First, the system procedure must be improved in order to automatically deal with faults which result in non-linear behaviour and to improve the facilities for specifying test measures. Optimal fault diagnosis is currently not guaranteed if several test measures are considered at the same time. Next, work is required in order to provide a facility which can capture the transfer function of an analogue circuit from the circuit schematics. Further work can also be considered to extend the test generation procedure to automatically cope with sampled circuits. Finally, integration of the tool in a real test environment is the ultimate goal of this work.

**II-1.2. Design of Reliable Fail-Safe Mixed-Signal Systems**

*Members: M. Lubaszewski and B. Courtois*

Several hard problems related to self-checking designs are proved to be solved by adding Built-In Self-Test (BIST) capabilities to circuits, which must be activated periodically during the system application. This unification of on-line and off-line aspects leads to an application range that goes from manufacturing test to in-use circuit checking. A significant example of such unification is the Unified BIST (UBIST) technique for digital circuits.
On their ultimate stage, real-life critical systems have to activate several actuators, delivering signals that are either correct or at least safe. Recently, it has been shown that it is possible to implement integrated circuits with fail-safe interfaces, transforming a self-checking circuit into a fail-safe one.

When thinking about the design of high safety systems, the self-checking capability of its units must be ensured with basis on a high quality of tests applied to them. Furthermore, this capability must be extended from circuits to board and module levels, in order to obtain an actual self-checking system.

The boundary scan architecture helps in reaching part of this goal: efficient means of off-line testing chips and board interconnects are provided. The concurrent error detection at the board level can be achieved by merging boundary scan and UBIST (B^2UBIST - Boundary scan Board Unified BIST) for the digital parts and fully differential self-checking circuits for the analogue parts. The merge of UBIST and fully differential functional blocks results in the architecture given in figure 5 for a mixed-signal self-checking circuit.

![Figure 5: Self-checking mixed-signal circuit](image)

At the board level, since the boundary scan path is not used during normal operation of circuits, it may carry their on-line error indicators. Depending on the application speed requirements, either circuit error indicators may be propagated and compressed across the board by cascading them through circuit global checkers, or they may be verified by a specific board checker in a parallel way (figure 6). Board interconnects are to be on-line tested as well, and so built-in checkers designed at circuit input interfaces (figure 5) will be charged of verifying the data-code sets related to them.

Given this context, the packages that sum up to achieve the design of state-of-the-art high safety circuits would be UBIST + boundary scan (B^2UBIST), fully differential self-checking blocks and fail-safe interfaces. The integration of all those concepts together makes possible in our days the design of efficient self-checking boards for high safety applications. Furthermore, since the board controllers for boundary-scan testing can be designed according to the above techniques, a module composed of self-checking boards can be made self-checking by communicating their controllers as shown in figure 6. Thus the design of self-checking systems is feasible, where a high degree of safety is guaranteed by the embedded modules.

Nevertheless, it is common knowledge that, even for missions of short duration, the hardware redundancy employed to improve the safety of the simplex system will also contribute to decrease the availability of the resulting self-checking system. Then, self-checking systems will be competitive with respect to their safety but certainly not with respect to their reliability.

A solution to overcome this situation would be on a technique for fault-tolerance, which ensures the reliability competitiveness of self-checking systems in the execution of short missions, and that ensures also the preservation of the safety inherent to their self-checking parts. A fault-tolerant scheme based on two replicas of a self-checking module and on a fail-safe mixed-signal interface is expected to cost as much as a triplicated system in terms of hardware. On one hand, such a scheme can be proven to achieve a higher reliability than a triplicated modular redundant system for self-
checking module overheads smaller than 73%. On the other hand, a digital-dominant interface for fault-tolerance can be designed which is capable of mapping the erroneous outputs of the resulting system onto a safe output state. It can be shown that this interface can tolerate a large part of its own faults and map them into a safe output state by embedding appropriate BIST capabilities (in much the same way as in UBIST chips). The design of an analogue-dominant interface achieving the same as its digital counterpart is still a problem to be addressed.

![Diagram](image_url)

(a) cascading error indicators

![Diagram](image_url)

(b) parallel verification of error indicators

**Figure 6**: Self-checking board

Besides a higher reliability, other advantages of our system over triplicated structures are that: it is more suitable for the detection of double-errors (and thus for the detection of pairwise shorts between wires connecting two different modules to the system output interface) and, repair is made simpler since the unit to be replaced (a circuit, a board or even a module) can be easily identified by looking into error indicators.

Especially due to the difficulty of design, the development of a wide range of self-checking systems will be feasible and economically viable, only when a sufficient number of potential users and support tools exist. Since the number of applications needing high quality on-line testing is growing rapidly and the increasing complexity of systems is making it more and more difficult to ensure this requirement using any other method, we believe that in the near future, an environment for automatic generation of complex mixed-signal self-checking circuits being available (we have been working on that!). self-checking circuits, boards, modules and systems will be designed by the electronic industry.

**II-1.3. Design-for-Testability of Switched-Capacitor Filters**

*Members: M. SOMA* and V. KOLARIK

This work concerns a design-for-testability (DFT) technique for switched-capacitor (SC) filters to improve controllability and observability of internal nodes. Timing strategies employing existing clock phases in SC circuits are used to sensitize signal propagation paths, thus enhancing the circuit

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testability. The overhead in terms of extra control logic is small. Since there are no extraneous devices inserted in the analogue signal path, there is no performance penalty in the normal operation of the filters.

Signal propagation is a critical requirement for any testability analysis or test generation algorithms. Unless signal paths can be established to enable fault excitation and fault propagation, it would be useless to attempt to generate tests for any given circuit.

A previous work on continuous-time filters illustrates that this prediction can be carried out based on simulation once the additional DFT devices are incorporated and the circuit is properly set in the test mode. These DFT devices are MOS switches which, by reducing the capacitors' effect on the continue-time filter bandwidth, sensitize paths through the filter structures by converting them to the simple gain stages. The MOS switches are already built into SC structures and thus the basic thesis is that signal propagation can be accomplished by timing methodology that takes into account not only the timing conditions for the proper operation of the SC circuits but also the test requirements of propagating signals through these circuits.

The circuit in the figure 7 is a low-pass one-stage SC filter. To propagate the input signal to the output during the test mode, a path can be sensitized through the circuit: 1. by disconnecting all the switches used for grounding the capacitor terminals and 2. by closing the switches in series with each capacitor.

![Figure 7: A low-pass 1-stage SC filter with path sensitization](image)

The frequency response of both the original and the modified filter was simulated. Two test configurations of the circuit were investigated: sampled operation (dynamic testing mode) and continuous operation (static testing mode). Sampled-signal filters are nonlinear circuits and AC analysis is not suitable for the evaluation of the frequency response. Instead, a multiple transient analysis with input sine waves of different frequencies was run. Output amplitudes from different runs were collected.

The implemented circuit consists of three blocks: a waveform generator, a clock decoding circuit, and a simple filter stage. The waveform generator produces two non-overlapping clocks, \( \Phi_1 \) and \( \Phi_2 \), that are connected to the inputs of the clock decoding circuit. The decoder delivers the clock signal suitable for the filter. Inputs \( T_1 \) and \( T_2 \) select the operating mode of the filter.

The circuit was implemented in AMS 1.2\( \mu \)m CMOS technology through MPC services. The core size is of 540\( \times \)450\( \mu \)m. The design includes both standard cells and full custom cells. Fabricated chips were tested and 100\% functionality was observed. It should be noted that in both testing modes the operational amplifier goes saturated within a few seconds due to no DC path to the operational amplifier input.

II-1.4. Frequency-based BIST for Analogue Circuit Testing

Members: S. KHALED*, B. KAMINSKA, B. COURTOIS, M. LUBASZEWSKI and S. MIR

* École Polytechnique of the University of Montreal, Canada.
Including a programmable frequency generator at the integrated circuit level will greatly simplify the requirements from an external tester during the manufacturing process and facilitate the chip test in the field. Since our off-line analogue circuit testing approach is based on injecting a sinewave signal at the circuit input and observe the circuit output, the relationship between the input and the output signals is frequency-dependant. Thus the frequency precision of the input test signal is critical to the reliability of the test and must be checked. To validate the oscillation frequency, a frequency-based BIST is need. Note that this same kind of BIST can be applied to any circuit with frequency variation, for example, a voltage-controlled oscillator, a frequency multiplier, etc.

The goal of this activity is to propose a new technique for testing analogue circuits based on employing an embedded sinewave generator with a dedicated frequency BIST (f-BIST). Several types of oscillators have been investigated: relaxation oscillators, switched-capacitor oscillators, current conveyor based oscillators, etc. For these many possible implementations, three types of BIST have been investigated.

The first one is an extension of the Translation-BIST, which is based on the frequency conversion to a DC voltage. The second f-BIST that we propose is more digital-oriented and is based on zero-crossing counting. The third approach is based on a fully differential implementation of the oscillator and the check of its balance by means of an analogue checker.

We have carried out some experiments and the results show that every of the three proposed f-BIST approaches fit very well specific low and medium-frequency applications. Research must continue in order to propose a BIST solution for high-frequency circuits.

II-1.5. Design of Radiation-Hardened Circuits

Members: F. VINCI DOS SANTOS, M. LUBASZEWSKI and B. COURTOIS

A research activity recently started centers on radiation hardening of analogue and digital integrated circuits. The aim of this work is to develop design methodologies that reduce circuit sensitivity to both immediate and long-term effects of radiation, relying as little as possible in modifications of the fabrication processes.

Solutions to two major problems associated with radiation exposure are being pursued. One of the problems is the radiation induced threshold voltage shift that plagues CMOS circuits. This shift is caused by the creation of trapped charges within SiO₂ layers, and interfacial traps in the transistor channel, and is cumulative (total dose effect). The circuit will eventually fail to meet the design specifications (logic function, speed, power consumption, etc). The objective of the research being carried out is to develop general circuit configurations that may minimize the impact of the Vₜₙ shift and postpone system failure.

The second problem is the perturbation of the information stored in a CMOS static RAM cell by the charge deposited by a traversing particle (single event upset). The amount of deposited charge capable of causing an erroneous change of cell state is roughly proportional to the cell size. As memory density increases there’s a greater probability of such an event, so at a certain point error correction schemes will become impractical. In view of this situation a study of SRAM cell architectures is being undertaken, seeking designs that are inherently less sensitive to the charge collection phenomena which are at the origin of the upset.
II-2 Diagnosis of Complex Systems (DCS)

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Contracts:
FUTEG (EC - COPERNICUS N. 9624), PROTEUS (French-Slovenian Proteus action N. 95010).

Research fields:
Knowledge-Based, Multi-Level and Non-Classic Logic Approaches for System Testing and Diagnosis,
Mixed-System Modeling, MCM and Partial BS Board Test and Diagnosis, Synthesis for Testability.

II-2.1. Introduction

The DCS group has started in 1992 its own activities. Research activities of the group deal with new
approaches of test and diagnosis of VLSI circuits and electronic systems in general. Starting from 1993,
analog and mixed-signal systems have been studied from the modeling and simulation point of view in
the one hand, and from the test and diagnosis point of view in the other hand. In 1994, a new activity
has been started on synthesis for testability.

II-2.2. Test and diagnosis of complex heterogeneous systems

At the system level, the test and diagnosis of complex heterogeneous system activity aims at studying
how to build a common testing and diagnosis environment for heterogeneous systems. The novelty of
this work is directly related to the kind of addressed devices.

II-2.2.1. Definitions and objectives

Heterogeneous system size and complexity are ranging from those of whole systems to those of
integrated circuits. They are referred to as heterogeneous since they are composed by subsystems which
differs from the following points of view: design, fabrication process, technology, testability level,
quality assurance, internal information confidentiality, ...

When the system is a MultiChip Module, for example, subsystems to consider are bare dies, which may
be designed and fabricated by different companies, using different processes. These dies may be
standard ICs or custom ASICs, they may be digital or analog dies, they can be fabricated using different
technologies (CMOS, Bipolar, GaAs, ...), some of them may include testability features (Boundary
Scan logic, BIST principles, ...), some of them may be guaranteed by high quality assurance provided
by their supplier, etc.

These differences make heterogeneous a given kind of system. But differences between kinds of
systems must also be taken into account, they are mainly related to the following features, which are
conditioning the testability and diagnosability level of the system: assembly substrate, interconnects,
subsystem package, subsystem bonding, ...

Many kinds of systems have been separately studied from a testing and diagnosis point of view.
Methods and tools are already available, but the purpose of this activity is to study how choosing and
applying the best method, how choosing and using the best tool, according to the kind of system we
have to deal with, and how these tools and methods can be consistently used to cope with heterogeneity.

II-2.2.2. Partial boundary scan boards and MCMs

In this activity, heterogeneity comes from different degrees of testability within the system components.
The considered systems are partial boundary scan boards and multichip modules (MCMs).
Developments reported in this section have been mainly achieved by Mohamed Hédi Touati, in the framework of his PhD Thesis. This work is supported by the EC-COPERNICUS FUTEG project N. 9624. Firas Mohamed has provided his contribution on fuzzy logic concepts.

In this context, test and diagnosis of boards with partial boundary scan (BS) has been previously investigated, in collaboration with Marcelo Soares Lubaszewski (ATM group). This kind of boards is populated by BS circuits and non BS clusters.

Trying to come with a pragmatic solution, we have proposed to reuse an already available tool, the knowledge-based system designed in the laboratory for integrated circuit diagnosis in an electron-beam testing environment, which is versatile enough to become almost directly applicable to mixed boards today.

A methodology for fault detection and diagnosis using this tool has then been developed. The main characteristics of this methodology are that:

- it identifies the following fault types: (1) faulty cluster circuits, (2) interconnect shorts and opens inside clusters, (3) shorts between clusters, (4) shorts between clusters and full BS parts, (5) interconnect shorts and opens on full BS parts, and (6) faulty BS circuits.
- it unifies the circuit and interconnect test of a cluster, since the testing of a cluster's internal nodes and its outputs usually can only be carried out by means of the activation of the function performed by the cluster circuits.
- whenever feasible, it tests multiple clusters and BS interconnects in parallel in order to avoid inefficient accesses to the board scan path. BS circuits are checked in a later step, since the same accessibility means are necessary for testing clusters and BS interconnects.
- it uses as far as possible the same test sequences for both fault detection and first fault diagnosis processes.
- it applies the same test and diagnosis procedure for board manufacturing, prototype debugging and maintenance.

Nevertheless, the results of this methodology are only fault candidates, which have still to be discriminated, in order to reduce the diagnosis ambiguity.

The methodology presented above for partial boundary scan boards has been adapted to MCMs populated by dies belonging to two categories: (1) dies designed with chip level BS (some of them possibly including BIST features) and (2) dies without any testability feature.

This methodology has been implemented in a software, and obtained results with combinational benchmarks have already been published.

New developments on fault diagnosis have been achieved in 1994 to improve this method, and refine the diagnosis.

The first list of fault candidates give a rough faultiness estimation for each candidate. From this list, a qualitative reasoning process allows to update the faultiness estimations, in order to discriminate between candidates. The estimation values are elements of the following set: {Correct, Assumed Correct, Tending to Correct, Ambiguous, Tending to Faulty, Assumed Faulty, Faulty}.

Nevertheless, a pure qualitative process may not allow reaching an efficient discrimination. We have then adopted a semi-qualitative method based on fuzzy sets to enhance the fault diagnosis accuracy. This method assumes the ability to observe some internal nodes of the module under test, and defines a "best test point finding" strategy.

This strategy is based on a heuristic using three parameters:

- Cfout : the cardinal of the fanout cone which is the set of components that may be influenced by the node.
- Cfin : the cardinal of the fanin cone which is the set of components that may influence this node.
- the fuzzy entropy.

The reasons for which we made the choice of these parameters are the following:

- The entropy has several important properties. For likely correct components or likely faulty components, it is minimal; such candidates are cheap to identify. By contrast, for ambiguous candidates, it is maximal; unlikely candidates are expensive to identify. Since our data are fuzzy estimations, for each set of candidates we calculate the average fuzzy entropy in order to isolate the
influence of the different cardinalities of candidate sets; the minimum result will be considered as the best one, because the lower is the entropy, the lower is the ambiguity.

- If a probed node is found correct, this means that the fault would be inside the fanout cone and the ambiguity about the covering (fanin) cone is reduced.

- If a probed node is found faulty, this means that the fault would be inside the fanin cone and thus the ambiguity about the fanout cone is reduced.

The heuristic consists of the computation of a cost function that gives a topological evaluation of the importance of each node in the diagnosis process by making the synthesis of these information.

The final decision depends on two results:

- the entropy which has to be minimum
- the degree of influence Df (a function of Cfout and Cfin), which has to be maximum. Df is chosen to be (Weak*Cfin)+(Middle*Cfout), where Weak and Middle are the fuzzy weights of the parameters.

The problem can be formulated as follows: for n test points (each point characterizes a set of candidates), we calculate its average fuzzy entropy and its degree of influence. Thus, we will have two vectors (Ent(i=1,n)) and (Df(j=1,n)) containing the previous results.

Suppose that E is \(\min(\text{Ent}(i=1,n))\), and D is \(\max(\text{Df}(j=1,n))\). It is then obvious that the optimal test point P is the one which verify: \(\text{Ent}(P) = E\) and \(\text{Df}(P) = D\). But this condition is not always verified, so we have to look for the best one which can be the nearest to the optimal. For this purpose, the Hamming distance is calculated. Alternatively, we can minimize the result of a cost function defined as 

\[\text{Cost}(\text{Df}, \text{Ent}) = (a^*\text{Ent}) + (b^*(1/\text{Df}))\]

where a and b are fuzzy weights.

Results obtained till now with the software implementing this method are very promising, and experiments are going on.

Apart from these developments on diagnosis, some efforts have been put on the automation of the test vector scheduling process for one cluster, which could be composed of many interconnected circuits. It is assumed that the internal structure of these circuits is not necessarily known, the only information required being that a set of test vectors or test sequences is given for each circuit.

The test scheduling problem at the cluster level can then be formulated as follows:

Given the knowledge of a set of test vectors or test sequences, and their fault coverage with respect to the logical stuck-at fault model for each circuit of the cluster, and given the knowledge of how these circuits are interconnected to form the cluster, the objective is to generate a set of test vector sequences to be applied to the whole cluster in order to ensure both detection of faulty circuits inside a cluster and faults (opens or shorts) on interconnections inside a cluster.

This test scheduling problem at the cluster level can also be seen as a conventional board (only made up of non boundary scan circuits) test scheduling problem. This problem is normally tackled using functional test generation methods. However, the context of boundary scan testing, as well as the fault models that we need to take into account, implies that a structural test generation method must be adopted.

A very simple method has been defined for this purpose. This method is based on a matrix representation of the stuck-at coverage on primary inputs and outputs obtained with the test patterns available for each circuit. Then, with the knowledge of the cluster structure (how the circuits are interconnected), we define for each circuit the constraints on the upstream and downstream circuits to make it observable and controllable, and we can obtain, by combining the matrices, a scheduled test sequence that can test the whole cluster.

The automation of this method is on the way, and will be achieved by Fernando Morgado, who is working towards his DEA degree in Microelectronics.

II-2.2.3. Analog and mixed-signal systems (modeling and simulation)

Other kinds of heterogeneous systems that must be addressed are analog and mixed-signal systems. This section deals with their modeling and simulation.

Developments reported hereafter have been mainly achieved by François Lemery, in the framework of his PhD Thesis. A collaboration with SGS-Thomson Microelectronics has started in early 1993 on this subject, through a CIFRE grant (French University-Industry Joint Program).

The results achieved in 1993 are concerned with macromodeling, behavioral modeling languages and behavioral model generation. Macromodeling has been addressed for simulation purposes at the system
level, and library models have been written using ELDO-FAS. Different behavioral modeling languages have been studied and compared. Their specificities have been analyzed, and a prototype of a translator between ELDO-FAS (from Anacad) and SABER-MAST (from Analogy) has been developed. A tool translating models written in ELDO-FAS into ELDO-CFAS (Anacad) has been designed as well. For future purposes of translation, the evolution of the VHDL-A language definition process (analog extension to VHDL) is actively followed.

These results have served as a basis for the study of a tool for automatic generation of behavioral models. The main result achieved in 1994 has been the development of a tool for the automatic characterization of analog and mixed-signal devices and the automatic generation of their behavioral models.

This tool takes as input the results of the analog simulation of a circuit described at the transistor level, and a library of macroblocks defining different stages, such as input, gain, or output stages. Several elements of this library have been designed during 1993. The library is provided with the tool.

The main steps achieved by the tool are the following:

- Characterization schematic building: this step has the purpose of helping the designer in specifying elements and simulation parameters, extraction functions and output parameters. Then this schematic is checked and finally stored in a database.
- Datasheet generation: the characterization schematics that have been stored in the database are executed at this step, with respect to hierarchy, some schematics being parameterized by other ones.
- Macromodel generation: in this final step, the designer specifies a macromodeling schema based on the parameterized macroblocks existing in the stage library. Parameters of the different stages are expressed as functions of the relevant characterization schematics. Finally, the macromodel code is automatically produced, either in SPICE or in ELDO-FAS language, after the stage parameters have been calculated.

This tool for characterization and automatic macromodel generation is based on the CADENCE design environment and the ELDO analog simulator.

Apart from the design of this tool, the behavioral modeling of a complex mixed-signal system, an airbag system (in the framework of the EC-JESSI AC3 project) has been made in the HDL-A language, and several models have been written for this purpose. Finally, a translation tool from ELDO-FAS to HDL-A language has been developed.

II-2.2.4. Analog systems (test and diagnosis)

This section addresses analog systems from the test and diagnosis points of view. Developments reported hereafter have been mainly achieved by Firas Mohamed, in the framework of his PhD Thesis. A collaboration with Franc Novak et al. from the Computer Systems Department of the Jožef Stefan Institute (Ljubljana, Slovenia) has been set up on this subject, through the French-Slovenian Proteus actio N. 95010.

The group has begun in late 1993 investigating artificial intelligence approaches and non classic logic for the test and diagnosis of analog systems.

Given the intrinsic complexity of this kind of devices, especially the continuous values of signals as opposed to the discrete ones for digital systems, new approaches should allow to define and tune notions like the "acceptance window" for different parameter values, thus providing an adequate paradigm for test and diagnosis methodologies.

The particular interest of the group is to study and compare to which extent different artificial intelligence approaches can help in this context. The three following approaches have been studied:

Model-based reasoning techniques: model-based reasoning is reasoning on a reference model built from the structure of the device, its components, their interconnections, and their correct behavior. A fault is defined by excluding "anything other than expected behavior", so it covers a wide class of faults. This approach is strongly device independent and can be less costly to use than e.g. fault dictionary approaches.

Numerous systems have embedded this approach. All these systems partially fail when they deal with dynamic systems and more difficulties arise when dealing with analog circuits.

- Qualitative reasoning techniques: as to qualitative reasoning, three approaches mainly cover this research area, each one being represented by one system. The essential difference between them lies in
the ontological primitives they use for describing a physical system. They are so much qualitative that they fail in handling analog circuits.

- fuzzy logic techniques: the principal objective of fuzzy logic is the treatment of inaccuracy and uncertainty of information.

A fuzzy set $A$ is defined on a domain $T$ by giving a function operating from $T$ to $[0,1]$. The result of this function is the membership degree of a given element of $T$ to the set $A$.

In practice, a fuzzy interval will be defined by a 4-tuple $[m_1,m_2,a,b]$, where $[m_1,m_2]$ is the core, and $a$ and $b$ are the boundaries. A real number $m$ can be defined by $[m,m,0,0]$, a crisp interval $[a,b]$ by $[a,b,0,0]$, and a fuzzy number $m$ by $M=[m,m,a,b]$.

We have programmed the main fuzzy logic operation, and have tried them on examples of analog circuits described by their behavioral models. Most famous systems developed for analog fault diagnosis have been also studied, and their results have been compared against those we have obtained using fuzzy logic. It appears that fuzzy sets allow to define the operators of order-of-magnitude in a more quantitative and accurate manner.

Crisp intervals contain all sorts of inaccuracy without any distinction, which can cause an explosion in the value propagation through the circuit.

A value which oversteps the boundaries of the interval will be considered as faulty, but possibly true in order-of-magnitude. With fuzzy intervals, it will simply be a fault with a given membership degree.

The conclusion we have reached is that using fuzzy logic is an adequate paradigm for the test and diagnosis of analog systems. We then suggest replacing crisp intervals by fuzzy intervals. This representation is more general, since it can represent the knowledge embedded in the soft boundaries of the interval and since there is no exclusivity of values. Moreover, it allows to distinguish between different types of imprecision: this of the human expert, these of the components, or that of the measuring equipment. Each value from the fuzzy interval has a membership degree which, for us, gives its acceptance degree.

Future work will be directed towards building a fuzzy logic based expert system; the model-based approach, a fuzzy ATMS which propagates fuzzy intervals will be used; a unit containing fuzzy qualitative rules and component fault modes may be added. Finally, this system could be able to learn from experience.

II-2.3. Synthesis for testability

High-Level Synthesis for Testability (SFT) is a new activity of the group, started in 1994. A collaboration with Vladimir Castro Alves et al. from COPPE/UFRJ (Rio de Janeiro, Brazil) has been set up on this subject, through the CAPES/COFECUB (joint French-Brazilian university cooperation program) project N. 144/94.

While test synthesis is the process of automatic generation of a particular test structure, high-level SFT is a much more complex process that can be viewed as the automatic generation of testable architectures, which involves in one hand the choice of the suitable test structures to be allocated to a target test methodology, and according to a set of constraints dealing with cost and performances; in the other hand, SFT involves a global test scheduling process.

II-2.3.1. Assessment and prerequisites of SFT

The current challenge in SFT can be seen like the challenge faced in the early 80s by DFT approaches. The cause is the same, that is, the trends in technology progress, being now exacerbated by a higher order of magnitude.

The trend in technology progress is well-known: more transistors can be integrated on the same area, and 0.5 micron technology is currently available in industry. Following the trend in technology, and starting from the 70s, commercial tools were available, roughly gaining one level of abstraction every 10 years.

While design and synthesis is mostly (and "naturally") a top-down activity, testing is mostly a bottom-up activity, since it is directed towards fault detection (and fault location when diagnosis is also foreseen).

The challenge in SFT comes from the design trend, coming itself from the development of the manufacturing possibilities, and from the level where fault hypotheses have to be considered. There are
more and more transistors to be designed, and this results in a continuously increasing number of faults to be considered. How can the design trend be then cope with the quality required in testing?

Analyzing the most widely adopted methodologies and the most successful industrial tools within the last decade, both in the field of High-Level Synthesis (HLS) and in the field of DFT, three main principles can be derived: these methods and tools are pragmatic in their objectives, they are systematic in their approaches, they are flexible in their use. An efficient SFT methodology should obviously be driven by these three principles too.

The pragmatic objective is related to economics and to the market evolution. To reach this objective, firstly, an SFT approach should fit a particular HLS environment, but HLS choices like target architecture and application must be seen as constraints to SFT. Secondly, SFT should be characterized by intensive design and DFT reuse, and thirdly the SFT process should cope with the lack of some testable versions of building blocks in libraries.

The systematic approach implies that the SFT process should not be restricted to some parts of the device (control parts or datapaths), and must take into account the whole device, including the communication network between its components or even with its external environment. A given testability method should also be targeted, and the process should allow testability evaluation.

Finally, the flexibility requirements means that interactivity of the system, together with user-friendliness should be key aspects to enable the designer making trade-offs between different alternatives.

II-2.3.2. Global view of the SFT approach

The defined SFT approach tries to embed these three principles, in conjunction with the use of the HLS system AMICAL developed within TIMA lab, and described in the SLS group activity report.

The first question to solve has been what is the earlier step of the HLS process to introduce SFT features. Given AMICAL steps, and since our objective is to use a systematic approach with as much design and DFT reuse as possible, it appears that our SFT approach should most efficient interact with the HLS system during the allocation step, and this decision makes the SFT starts as early as possible during the synthesis process.

The AMICAL allocation step is then transformed into an allocation for testability step, which encompasses the following phases:

- Functional unit allocation for test
- Trade-off database feeding: the study of the database structure and its related management features will be mainly the work of Hong-Xue Cai, who has started in December 1994 his two-year research stay at TIMA laboratory, in the framework of a joint French-Chinese scientific cooperation agreement.
- Trade-off decision making
- Top controller testability ensuring
- Additional test structure generation
- Test plan generation
- Test controller synthesis
- Micro-scheduling
- Register placement
- Connection allocation
- Evaluation of the global test architecture

All these phases are then replacing the previous allocation step of the HLS process. After this step, AMICAL normally performs architecture generation. The SFT approach will perform instead a testable architecture generation step, which, in addition to normal architecture generation, includes the two remaining phases:

- Linking the test controller to the test environment: the study of this task will be the work of Walid Maroufi, who is working towards his DEA degree in Microelectronics
- Generating boundary scan architecture: this will be the work of Ana Antunes, who is working towards her DEA degree in Microelectronics too.

A case study of synthesis for BIST of bus-based architectures, implementing the whole approach, has been started in cooperation with our partners from LPC laboratory at COPPE/UFRJ, Rio de Janeiro.
II-3 Integrated Systems Design (ISD)

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Research areas:

The integrated system design group concentrate on circuit design issues.  
It investigates the use of redundant notation in the design of VLSI circuits for high speed or high precision arithmetic operators.  
It explores also the problems posed by new circuitries or new technologies.

Contracts:

European: BARMINT (Esprit III Basic Research), GARDEN (Human Capital and Mobility),  
GRASS (Esprit III Working Group).
French: MICROSYSTEMS (GDR CNRS).

II.3.1 On-line functions generator

Members: J.C. BAJARD, J.M MULLER (from LIP, Lyon), A. SKAF, A. GUYOT,

Fast evaluation of polynomials is a major goal in computer science, because most algorithms of numerical analysis need polynomials and also because any continuous function, including every elementary function, can be approximated as accurately as desired by a polynomial (theorem due to Weierstrass). So most of the scientific computers offer some support for evaluation of polynomials by the Horner's scheme, that means sequentially:

\[ P(x) = \sum_{i=0}^{n} a_i x^i = (((a_n x + a_{n-1})x + a_{n-2})x + \ldots + a_0) x. \]

The circuit below uses on-line operators binomers, and takes advantage of their inherent parallelism. A circuit for exponential, trigonometric and hyperbolic functions with a precision of 32 digits and a delay of 11 clock cycles has been designed in 1.2\(\mu\) CMOS.  
The CORDIC scheme for elementary functions is very elegant but becomes difficult when redundant notations, demanded by on-line operators, are used. Redundant notation leads to the loss of accurate comparison. This loss must be compensated either in time (more steps) or in area (more operators). Nevertheless the complex exponential function does not suffer the same problems. A general purpose elementary functions on-line processor, base on complex exponential, has been designed in 1.2\(\mu\) CMOS.

* Institute of Informatics Systems, Russian Academy of Science, Novosibirsk, Russia  
** University of Sofia, Bulgaria
Figure 8: On-line polymonomer

Figure 9: On line complex exponential function
II.3.2. On-line operators for digital signal processing

Members: A. VACHER, A. SKAF, A. GUYOT

For on-line algorithms, the operands as well as the result flow through the operators serially with a small latency. On-line operators make pipelining possible down to the digit level, thus allowing a high degree of functional parallelism. Besides, serial transmissions relieve the routing problem. The benefits of on-line circuits in the field of digital signal processing have been widely publicised. Chaining on-line operators for a long series of operations may be significantly faster than other approaches. The need for faster Fourier transform on a larger number of samples is paramount among physicists. Many circuit implement the FFT with serial operators, all starting with the least significant digit first. The goal of this project is to design a board for a 100x100x100 cubic Fourier transform, using on-line most significant digit first adder/multiplier for butterflies, since the on-line delay of this operators is far smaller than with the least significant digit first approach.

Figure 10: The parallel FFT

II.3.3 Design of testable operators

H. BEDERR, M. NICOLAIDIS from RIS Group, TIMA, A. GUYOT

The test of the above mentioned on-line operators is a part of the research of test algorithms for regular structures carried out in the Reliable Integrated System Group of TIMA. It has been shown that due to their low observability and controllability as well as their sequential behaviour, on-line operators are difficult to test. Nevertheless, when redesigned with a low overhead for testability, they can be tested in a constant time. This project is a part of the thesis of H. Bederr.

II.3.4. Fast arithmetic divider

Members: L. MONTALVO, I. MOUSSA, T. VASSILEVA, A. SKAF, A. GUYOT

The speed of computers will always rely on the speed of hardware arithmetic operators. But according to Moore's and Amdahl's law, more and more transistors can be devoted to a unique function. Some arithmetic operators, like inversion, division, square-root extraction, etc., rely on algorithms that are inherently sequential due to a decision taken on each partial result. Fast implementations are based on carry-propagation-free addition/subtraction. Going to higher-order radices allows to get several quotient bits at a time but in turn leads to a complex decision table and consequently to a long critical
path. Mixing the notations (different notations for partial remainder, divisor and quotient) gives more design freedom. The theory of hybrid notation division algorithm has been developed. Most of the algorithms currently used are individual cases of this theory. Besides, a new algorithm has been proposed and experimented. This project is a part of the thesis of L. Montalvo. Dividers using redundant notations either radix 2 or radix 4, including fast converter from redundant to standard notations has been designed in 1.2\(\mu\)m, 1.0\(\mu\)m and 0.5\(\mu\)m full custom CMOS as well as a technology independent macrocell generator.

Figure 11: Hybrid radix-4 divider

II.3.5. Self timed arithmetic operator

Members: M. RENAUDIN (from CNET),
B. EL HASSAN (from France - Telecom Bretagne, CNET), A. GUYOT

Asynchronous circuits have been investigated at "CNET" in Grenoble through a collaboration with "Telecom Bretagne" for more than three years. The goal of this work is to explore the application of self-timed operators in digital signal processing, in order to obtain lower power dissipation, no clock distribution and fast processing. The collaboration between CNET and TIMA intends to investigate self timed or asynchronous arithmetic operators. This project will be a part of the thesis of B. El Hassan.

New asynchronous adder structures with high performances and low cost have been designed. The potentialities in terms of speed and complexity of Asynchronous Carry Select Adders, Carry Skip Adders, Carry Look Ahead Adders have been compared. All the structures use DCVS Logic circuitry optimised for speed-power trade-off.

A parallel multiplier-accumulator, devoted to high speed digital signal and video processing has also been designed. It can run at up to 100 MHz and operates in asynchronous or synchronous mode.

The division and square-root extraction algorithms has to be adapted to a self-timed ring architecture. The layout of the 32 bit self-timed ring divider is presented below in Figure 9. It is currently under fabrication at the SGS-Thomson Crolles plant, near Grenoble, in three-metal .5 \(\mu\)m CMOS technology (3.3 Volts). It is expected to complete a 32-bit square root or division in about 100 ns. The result is in conventional binary notation.
II.3.6. GaAs circuits design methodology

Members: I. MOUSSA, R. PEREZ-RIBAS, A. GUYOT

This project was started in February 1994. Thomson-TCS in the suburb of Grenoble is the only European digital GaAs foundry. Its technology is compatible with VITESSE. The CMP has set up a brokerage service for digital GaAs, it is organising courses and taking part in the development of a standard cells library. The integrated system design group is a partner in two actions: Grass and Garden.

The Human Capital Program of the European Economic Community aims at promoting cooperation in research through the organisation of networks. The purpose of the network GARDEN (Gallium Arsenide Reliable Design Environment) is to improve the knowledge of researcher on mixed mode GaAs VLSI integrated circuits and to generate facilities for allowing the reliable design of such circuits.

The main objectives of ESPRIT Basic Research are to replenish the reservoir of new knowledge and expertise from which industrial research can draw to ensure tomorrow’s innovation and to ensure the environment for training tomorrow’s researchers through research itself. The purpose of the Working Group GRASS (Gallium Arsenide Research Action on aSiC Synthesis) is to reinforce the already exiting cooperation among European Universities to realise a coordinate synergy on important issues on GaAs IC design.

Figure 13: A GaAs radix-2 16x16bit divider
II.3.7. Operator for Unlimited Precision

*Members: V. COISSARD, J.L. ROCH from IMAG-LMC laboratory, A. GUYOT*

This project was started in October 1994. It aims at the design of a general purpose arithmetic processor that can perform the four basic operations plus some internal management without any truncation or rounding. This project will be a part of the thesis of V. Ceissard.

II.3.8. Delay modelling in arithmetic operation

*Members: T. VASSILEVA, V. TCHOUMATCHENKO, A. GUYOT*

Optimisation of speed, power consumption and area of arithmetic operators can be done only if the gate delay is accurately modelled according to the transistor size.

II.3.9. Design portability

*Members: J. FREHEL from SGS-Thomson Microelectronics, Z. APANOVICH from the Russian Academy of Sciences, I. BOUTAMINE, A. GUYOT*

This project was started in February 1994. The reuse of old design with new technologies is vital for design houses. The migration problem is more or less solved by homothetic shrink follow by erosion or dilatation for migration from a technology to a compatible one. The problem becomes more difficult to take full advantage of a new technology that offers more interconnection layers and stacked contacts. The research is carried on with J. FREHEL from SGS-Thomson and will be part of the thesis of H. Boutamine.
II-4 MicroSystems (MCS)

**Group Leaders:** B. COURTOIS / J. M. KARAM
(e-mail for B. Courtois: Bernard.Courtois@imag.fr)
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**Members:** L. BUATHIER, B. CHUBB*, B. COURTOIS,
M. DUMITRESCU**, J. M. KARAM, Z. KOHARI***,
C. MARTA***, W. LAFFRAT, J. M. PARET, T. PIGNOL,
M. RENCZ****, B. TUDOR **

Research areas:

Silicon compatible micromachining. CAD tools for microelectromechanical systems. Thermal modeling. Smart sensors design.

Contracts:

European: BARMINT (ESPRIT-III Basic Research), THERMINIC (COPERNICUS)
French: MICROMED (GDR Microsystèmes CNRS)

Memberships: NEXUS, NETPACK, MEMS Discussion Group

Industrial Partners:

AMS (Austria), ANACAD (France), ES2 (France), SEMILAB (Hungary).

Topics:

The market of microsystems is quickly expanding and new products are continuously being developed and new applications identified. Many signal say that the markets will continue to expand throughout this decade and into the next century.

But two issues must be addressed in order to move microsystems from research prototypes to industrial development: low-cost foundries and CAD tools. Hence the microsystems group within TIMA Laboratory is fully involved in the development of design methodologies, tools and technologies necessary for designing and fabricating microsystems.

II-4.1. Silicon compatible micromachining

**Members:** B. COURTOIS, J. M. KARAM, J. M. PARET, T. PIGNOL

There are two ways to manufacture microsystems: to develop processes specific to microsystems (hence these processes can address requirements specific to microsystems) or to use processes that have been developed for microelectronics. Among those later processes, some can be targeted to microsystems, again to address specific requirements, or it is possible to add special process steps to accommodate microsystems within integrated circuits. This later way will allow to collectively fabricate microsystems including the microelectronics part at a low-cost. This is the way addressed by TIMA. The fabrication of silicon compatible micromechanical structures involves the deposition, doping of the necessary material and the selective etching of the underlying support. Two main methods can be used; bulk micromachining where structures are etched in the substrate, and surface micromachining where the micromechanical layers are formed from layers deposited on the surface.

* On leave from Southampton University, United Kingdom
** On leave from Bucharest University, Romania
*** On leave from Technical University of Budapest, Hungary
**** Technical University of Budapest, Hungary
Microsystem designs are fabricated on a multi-project wafer using industrial production lines, and the post-processing maskless anisotropic etch is performed in central laboratories. This concerns bulk micromachining, where designs have been successfully tested on the 1.2 m and 1.0 m CMOS double layer metal technology (DLM) from ES2 and 1.2 m CMOS double layer metal and double layer polysilicon technology (DLP, DLM) from AMS. The software support is CADENCE (Edge editor). This choice is arbitrary, and in the future other software could be used. The etching is performed using EDP (ethylenediamine-pyrocatheol-water), TMAH (tetramethylammonium hydroxide) and KOH (potassium hydroxide).

Experiments for the realization of suspended microstructures using surface micromachining are in progress.

![Figure 14: Structures realized using a 1.2 \( \mu \) CMOS double layer metal technology (DLM) from ES2](image)

### II-4.2 CAD tools for MEMS

**Members**: B. COURTOIS, M. DUMITRESCU, J. M. KARAM, W. LAFFRAT, B. TUDOR

Besides foundry facilities, CAD tools are also required to move microsystems from research prototypes to an industrial market. CAD tools for microelectronics have been developed for 20 years, in the fields of the design and in the fields of process modeling. Interestingly, it is to be noted that usually a single microelectronics engineer use either design tools or process tools, but not both. This exemplifies the difference between a microelectronics engineer and a microsystems engineer. Actually, a microsystems engineer needs to be a more multidisciplinary engineer: he needs not only to use design and process tools, but also tools dealing with the other disciplines needed for the design of microsystems: mechanics, optics, fluidics, ...
The art of microsystem design and modeling is still in its infancy. In microelectronics, CAD has already attained a highly sophisticated and professional level, where complete fabrication sequences are simulated and the device and system operation is completely tested. However, at least for the numerical simulation of the operation of single MEMS components, such as mechanical resonators, thermoelements, elastic diaphragms, reliable simulation tools are available.

In general there are two different approaches to overcome this limitation: the first possibility would be to develop a new framework tailored for microsystem-engineering. The second approach much more realistic would be to use existing CAD-tools which contains the most promising features and to extend these tools so that they can be used for the simulation and verification of microsystems and of the devices involved.

The state of the art in CAD tools for microsystems is that this tools have been developed for every discipline needed, hence no fundamental research is needed, but these tools have to be put together in a single framework.

MCS group investigates a CAD system for Microsystems based on selected existing software packages, linked with specialized interfaces and databases.

In such a project, two main axes have to be identified and treated: Design and Simulation.

In term of design, the CAD tools should allow:

- A layout generation of the whole microsystem (electronic and non-electronic parts) and a design rules checker. This should be linked to a technology.
- A parameter extraction enabling model generation.

In term of simulation, several kinds of simulation must be provided:

- full verification of the design functionality;
- electrical simulation which leads to the verification of the circuit design;
- mechanical simulation: the software must include large capabilities for analysis:
  - structural analysis (static and dynamic) which is used to determine the displacements, stresses, strains and forces that occur in a structure or a component as a result of applied loads;
  - structural buckling analysis which permits the determination of the load level at which a structure becomes unstable;
  - kinematic analysis which is a branch which deals with motion in the abstract, without reference to force or mass;
- optical simulation which provides the analysis of passive and active guided-waves devices and circuits;
- thermal simulation; the software must deal with the basic methods of heat transfer: conduction, convection, and radiation;
- technological simulation: micro-machining, wafer bonding, 3D assembly, packaging, ... 
- a post-physical simulation; it will be used to couple different aspects like heat expansion on mechanical behaviour influence.

The CAD structure consists of the following:

- The CADET package including the electro-thermal simulator, the component library, specific graphical interfaces, silicon anisotropic etching simulator.
- Technological files realising the extension of the IC framework, such as Cadence DF2 or Mentor Falcon Framework, to microsystems technology, and the parameter extension.
- Options tools that could be interfaced:
  i) Optics simulator
  ii) Micro-wave simulator
  iii) Model translator: ABSYNT or the FEM to VHDL-A translator
Based on the FEM simulation results in the predesign phase, simulation models of available standard components will be developed and included into the standard component VHDL-A library. The Electro-Thermal Simulator, which is the central simulation engine, accommodate any component model easily.

It should be distinguished between two different types of users: the system engineer is an expert in solving the problems on the system level while the component designer will be in charge of providing the necessary technological background for the system designer.

![Diagram of CADET simulation environment]

**Figure 15: Microsystem simulation environment**

To be able to design microsystems which include microscopic optical circuits that integrate transceivers, switches, multiplexers, wave guides and photo-voltaic converters, advanced numerical methods are essential. The group investigates optoelectronic simulation methods and define a software approach which is modular - consisting of preprocessors, solvers and post-processors - and offers the flexibility needed for expansion. The Beam Propagation Method (BPM) has been implemented and tested. This software will be interfaced to the whole package.
II-4.3 **Thermal modeling**

*Members: B. COURTOIS, J. M. KARAM, Z. KOHARI, C. MARTA, M. RENCZ*

This theme is developed in cooperation with the Technical University of Budapest (TUB), department of Electron Devices.

One of the greatest challenges of our days in microelectronics are the overheating problems. The increase in the power density in integrated circuits, caused by the actual small feature sizes, moreover the advent of 3D packages cause severe heat dissipation problems.

In this area, the microsystems group investigates new thermal monitoring methods, innovative temperature sensors and transient thermal mapping of integrated circuits and package structures.

II-4.4 **Microsystem design for safety critical applications**

*Members: L. BUATHIER, B. CHUBB, B. COURTOIS, J. M. KARAM*

Microsystems technology is having a large impact in a wide range of applications mostly safety critical, like in medical, automotive and aerospace domains. The next generations of microsystems will integrate test strategies and diagnostic functions.

In this domain, the microsystems group works in collaboration with the Advanced Testing Methods group within TIMA laboratory to ensure the migration of available techniques from the VLSI domain to the microsystem domain.

Some other works has been initiated in the design of smart sensors using switched current and switched capacitors techniques.
II-5 Quality of Complex integrated Systems (QCS)

Group Leader : L. BALME
(e-mail : secr@archi.imag.fr)

Members : I. BACIVAROVIĆ, L. BALME, A. BENALP, J. KAESTLI, M.L. SORDAGE, C. GUILLERMOU, R. STEFANI, Ph. TOUREILLE, C. VAUCHER

Research areas :

Contracts :

Industrial Partners :
Bull (France), CSEM (Switzerland), Dassault (France), European Spatial Agency (Europe), Hydroquebec (Canada), IMD (France), SGS (Switzerland), SGS-Thomson Microelectronics (France), Yusa (Japan).

Topics :
Because of the increasing complexity of today's industrial products, the design and manufacture of high quality products is becoming a crucial preoccupation of many companies in the world.

Complexity is the combined result of 4 different factors :

1/ The disappearance of traditional boundaries between technological fields such as mechanics, electronics, software and new materials. In a modern product, it is more and more difficult to identify subparts belonging exclusively to a specific technology.

2/ The interdependence of the sub-parts. The integrity of a product and therefore, its long term reliability, can be threatened by another product, much smaller, far less powerful, without any physical connection. This issue is particularly true for EMI/EMC for which an European Directive entitled "Electro-magnetic Compatibility and Interference" (89/336 EEC) was decided in 1989, with a transition period until the end of 1995.

As a result of this situation, the generally accepted law whereby, in order to make a total product of high quality, one only needs to make parts of high quality is no longer true.

1 - Visiting Professor from POLYTECHNICA UNIVERSITY, Bucharest, Romania
2 - IMD CIFRE Engineer, PhD student
3 - SGS Engineer, PhD Student
4 - SGS Thomson Engineer, Professional Thesis, EPIQCS
5 - DASSAULT Aviation Engineer, Professional Thesis, EPIQCS
6 - Professional Thesis, EPIQCS
7 - IMD Engineer
8 - IMD Engineer, Head of ATE team
3/ **The software integration.** In most of the today's products, in addition to managing the hardware, software has become an integral part of the product, with a fundamental difference compared with other technical sub-parts: software is a direct output of the human brain, with no intermediary transformation phases and with a very high risk of conceptual failure. Because writing software is a purely logical exercise, one could consider that there is nothing intrinsically uncertain about it. It is now demonstrated how the process of successive failures of a program can also be considered just as random as that of a hardware device, leading to the idea of a use of a probability-based reliability measure.

4/ **The "systemic" environment of the product.** Long term reliability is more and more often a parameter also dependent on the environmental use of the product. The neologism "dependability" expresses well this concept. Nowadays products have to be considered as part of a more complex system, where the user himself and the environment of the product have a fundamental influence on its long term reliability.

QCS team within TIMA Laboratory is fully involved in the development of basic and applied research around the concept of quality of complex integrated systems, by:
- basic research : development of computerized models simulating and predicting the long term reliability of complex systems,
- applied research : development of applications in the area of SMT ATE and Smart Power Card project.

**II-5.1 Smart power card**

*Topic leader : L. BALME*

*Members : I. BACIVAROV, L. BALME*

The general tendency in microelectronics is to equip systems with their own power supply (primary or secondary battery). This is true for consumer electronics (pocket calculators, cameras and video cameras, walkman, cellular telephones, etc) as well as professional uses (wireless tools, note books for example).

In this type of use, secondary batteries represent a significant improvement, but still insufficient compared with the sophistication of the associated electronics.

The "Accumulateur à Electrolyte Polymère tout solide" technology called ACEP, was discovered by Dr M. ARMAND from the Laboratoire d'Ionique et d'Electrochimie du Solide de Grenoble, a laboratory of INPG-CNRS. It gathers the thin film technology with highly energetic materials and thus allows to create a new generation of all solid miniaturized batteries. This invention opened great new possibilities in various sectors. Smart Power Card is one of these in the field of microelectronics.

Smart Power Card is a portable stand-alone power source device integrating an ACEP battery made of an all solid thin film of conducting polymer, and a control system which pilots battery status indicators and/or data I/O. The same control system can be used for the surveillance of an external device or equipment.

Depending on the microelectronic system powered, Smart Power Card brings innovative solutions to:

**II-5.1.1. Secondary batteries for consumer and professional electronics**

This market is expecting:
- a highly efficient battery : ACEP
- a physical standard format : the ISO smart card format with connector have been chosen for Smart Power Card,
- a reliable battery giving key informations to the user: charge level, real time consumption and life capital are the 3 parameters shown to the user on micro LCD in the Smart Power Card.

**II-5.1.2 Multipurpose smart IC cards as defined by the ISO standards**

This fast growing market is expecting an integrated reliable power supply providing energy to IC cards while respecting ISO thickness (0,76 mm). The ACEP thin film technology allows to integrate power on
smart cards and thus opens great new fields of applications, particularly in the management and the surveillance of complex integrated systems.

The Smart Power Card concept is protected by a French patent entitled "Composant d'alimentation du type carte de crédit" deposited in February 1991 and extended (Europe, US, Japan, South Korea, Canada) in co-ownership between INPG and ACEP Inc. (the company owning the exploitation rights of the ACEP battery technology, joint venture between HYDRO-QUEBEC (Canada) and YUASA (Japan).

The feasibility study on Smart Power Card was carried out during 1990, the building of a first prototype using PCB technology was finalized during 1992-1993.

II-5.1.3 Recent developments

- New progresses have been made in 1994 in order to apply SPC concept and architecture to the management and the surveillance of complex integrated systems. The second ultraminiaturized generation of SPC should be finalized by the end of 1996.

- Acceptance of the US patent (US # 07-937.900)

- External event: joint development between INTEL Corp. and DURACELL Inc. of the Smart Battery Data (SBD) and System Management Bus (SMB) specifications which are in line with SPC architecture.

Figure 16 - SPC internal architecture
II-5.2 Automatic test equipment (bare boards \textit{(ADELAIDE)} and loaded boards \textit{(ISMB)})

\textit{Topic leader : Ch. VAUCHER}

\textit{Members : L. BALME, A. BENAIJ, Ch. VAUCHER, Ph. TOUREILLE}

II-5.2.1 - Bare board testing \textit{(ADELAIDE)}

Introduction

\textit{ADELAIDE (ADvanced ELAstomer using Integrated DEvice)}

\textit{ADELAIDE} is a project dealing with the test of bare printed Circuits boards (PCBs). More and more, it becomes easier to manufacture a product than to test it. It is true in electronics and especially in bare board manufacturing. We currently can see a flood of 20 mil pitch components in mass production (New RAM chips). We begin to see 16 mil and 12.5 mil pitch components in small quantities. LCD driver PCB connectors pitch is now industrially 10 mil. Today, bare Printed Circuit Boards (PCB) can not be tested in a reliable and cost effective way under the pitch of 25 mil.

Two dimensions must be considered:
- the technical dimension : it is very difficult to electrically (thus mechanically) access boards when they contain at least one component with less than 25 mil pitch.
- the economical dimension : it is very expensive (when possible) to access boards under 25 mil pitch.

\textit{TIMA} has developed a method to interface in a very reliable and cheap way complex boards with anykind of bare board testers.

\textit{The solution : Standard Mirror Boards}

In 1988, we started to develop a testing equipment using anisotropic conductive elastomers. The original idea was to build a complete transgrid board of the PCB to be tested. On one side, there was the image of the side to be tested, and on the other side, there were spread test points, easily accessible by a standard bed of nails (the minimum distance between two test points was 50 mil), and, in between, a layer of
elastomer, made of micro conductive cylinders, with anisotropic conductivity. The basic concept was successfully tested in the laboratory, but difficult to apply to industrial ATE for the following reasons:
- the use of conductive rubber requires very good planeity and controlled pressure everywhere. This is very difficult to achieve, because of the variable thickness of a PCB, and the warpage.
- the mirror board is long to build, expensive, and therefore not suitable for small and medium range production runs. Furthermore, it is as complex as the PCB to be tested.
- the conductive rubber is expensive and was rapidly damaged.
- there were contact problems with boards using solder resist.

Consequently, we decided to improve the method, considering this experience, and the experience of the standard way of fixturing. We also did not want to change the habits of the PCB manufacturers, because of the level of investment involved.

We decided to split the test points into two categories:
- standard test points, (50 mil minimum pitch)
- complex test points (under 50 mil pitch). One must consider that these points can only be Surface Mounted Test Points (through-hole components have a pitch greater than 50 mil). That is to say that they are organised in standard lines.

Standard test points are easy to reach with a standard bed of nails.
So we thought that if we found a solution that would allow mixing the standard bed of nails fixture and a means of accessing fine pitch lines, it would be the final solution.
We decided to apply the technology of the mirror board to these standard lines. We defined what we call Standard Mirror Boards (or SMBs), as shown in the figure 18 hereafter.
On one side is part of the image of the pads to be accessed. On the other side, we find test pads whose minimum pitch is 50 mil, that is to say easily accessible by standard bed of nail fixtures. Test points are in fact artificially STAGGERED.
The SMB pad's length is very small, and is comparable to the length of the pads to be accessed. Indeed, the contact zone on one Standard Mirror Board needs to be very small (0.1 mm2 is enough).
Their thickness is about 20 mil (0.5 mm) : regarding the standard travel of a spring probe (used with the bed of nails), 4 mm, we can assume that we can use the same pins as for standard test points.
The SMBs are mounted in a matter of seconds on the TOP plate of the traditional fixture, using a thin epoxy plate, called Support-Card, on which are fixed the SMBs. The Support-Card is drilled in the same operation as the Top plate.

Figure 18 - Standard Mirror Board architecture
All the disadvantages we found with the complete transgrid board version disappear, keeping their advantages:
- the contact between one SMB and the PCB to be tested is very local (a few mm), thus it is very reliable.
- to access all kinds of PCBs it is only necessary to build a dozen of references (one per pitch). So the SMBs are standard (thus very cheap), and can be ex-stock.
- we only use very little conductive rubber (only where it is necessary), so it is very cost effective. Furthermore, the elastomer is protected by spacers, and is not damaged, because always compressed by the same amount.
- SMBs are re-usable on other fixtures.

Furthermore, this technology brings the following new advantages:
- fully compatible with all test systems and traditional fixtureing.
- reliable access on very thin pads, up to 4 mil width.
- using inner-component ETGs location —> reducing the problems when 2 components are very close.
- spreading test points allows the use of standard 50 mil pins.
- reducing the number of plates needed.

- artificially increasing the grid density by a factor of 2, because of the spread test point locations, thus avoiding having to buy a double density grid tester.

**Global Mirror boards**

This is a new evolution of Standard Mirror boards, that has been developed in 1994. For extra-high density boards (Mobile phone boards, computers, FPD drivers, etc...), it is sometimes worth using a Global Mirror Board (GMB) instead of Standard Mirror Boards (SMB).

A Global Mirror Board is specific to the Printed Circuit Board (PCB) to be tested. It optimises the concept of the Mirror Board Technology to a dedicated board.

![Global Mirror Board](image)

**Figure 19 - Global Mirror Board architecture**

On a Global Mirror Board, test points can be spread further than on Standard Mirror Boards, for instance in an area where there are only a few test points, therefore eliminating local density problems.
**Project Status:**

Current commercialization by IMD, a French company (ZAC de la Fontaine de Jouvene, 8 rue Joly de Bammeville, 91460 Marcoussis, France, Tel : (33) 1 69 80 93 71, Fax : (33) 1 69 80 93 50).

**II-5.2.2 - Loaded board testing (ISMB for in situ mirror boards)**

**Introduction**

Loaded boards are traditionally accessed through a "bed of nail", that is to say a fixture where are inserted spring probes, that will contact a dedicated area on the board, called "test point". Each spring probe is wire-wrap and linked to the ATE (cf fig. Traditional fixture).

One can find very often several hundred test points on a fixture, each occupying an area of more than 2 mm², that is to say, for a fixture containing 1000 test points, 20 cm² of board surface only dedicated to test!

For some customer, it is still acceptable, but for the other ones, like in automotive industry, mobile phones or computers, where the room available is also a question of feasibility of the product, it is not accepted anymore.

After having developed the Mirror Board concept for bare board testing, it was natural to imagine an application for loaded board testing.

Instead of accessing the pads on the bare board, we imagined to directly access the components leads, eliminating the need of adding many test points on the board.

We developed a new version of SMBs, we call ISMB (In Situ Mirror Boards) (cf Fig. ISMB fixtureing): ISMB are mounted on a dedicated mechanic. ISMB can be use on a fixture in addition to standard test pins.

The first trials we made showed a relative reliability, because of the metal on metal contact: we achieved only several hundreds cycles without any problems. Further, we observed the deposition of metal oxides (lead oxyde, etc...), and other materials like solder residues, that lead to bad contacts.

We try to think about a material that would chemically eliminate these residues, and we had the idea to use polymeric materials.

![Traditional fixtureing and ISMB fixtureing](image)

*Figure 20 - In Situ Mirror Board (ISMB) architecture*

**The use of polymeric materials**

Research in the last decade has brought to light a new class of polymeric materials with very attractive properties: these materials are able now to combine the electrical conductivity and the mechanical properties of the plastic physical state. From the attractive polymers, polyaniline seems to be the most interessant. Polyaniline is obtained from oxidation of aniline leading to the emeraldine, the most
conductive form. Polyaniline can be synthesized chemically or electrochemically. The obtained polymer can be blended with specific olefins to obtain various physico-chemical properties such as elasticity, plasticity and surface acidity.
In addition, electrochemically obtained form leads to electrically-conductive polymer with good adhesion. Therefore, we patented [6] a method using polymeric materials. We then developed the right polymer material, in order to establish reliable contact, with the following properties:
- metallic conductivity
- elasticity
- chemical action (oxyde depassivation, etc ...)
- industrial deposition
The first results regarding the application of this method to electrical contact are very encouraging.

Project Status
Under development.

II-5.2.3 - 1995 developments
- ISMB presentation to IEEE International Test Conference, Baltimore (United States, Oct 95).
- Global Mirror Board Market launch by IMD in PRODUCTRONICA, Munchen, November 95.
- Software optimizations, automatic fixture generation software, with custom data-base architecture.
- scan + image processing of mylar films in order to rebuilt lost or unavailable datas (GERBER or HPGL files).
- upgrade of Mirror Board technologies in replacing elastomers by polymers.

II-5.3 Dependability Analysis of Complex Components and Systems

Topic leader: I. C. BACIVAROV

Members: I.C. BACIVAROV, L.BALME, M. L. SORDAGE

II-5.3.1 Dependability modeling and evaluation of complex systems

The ever-increasing complexity of modern electronic and communication components and systems and the importance of the operating duties they have to accomplish calls for systematic research concerning their dependability (reliability, maintainability, safety) analysis and evaluation, based on an equally important theoretical aquisition.

In order to optimize a complex system from the dependability point of view several of these components must be considered; their importance varies as a function of the system type and functional criticity.

The main objectives of this work are the development of efficient models and algorithms for the computer-aided dependability (especially reliability and safety) analysis of complex, high functional importance systems.

In the first phase of our research two problems were studied, namely:

(a) computer-aided structural analysis (using minimal cut set/tie set approach) for complex systems described by their reliability graph (with application to distributed systems);

(b) computer-aided availability/safety evaluation for systems with renewal, modeled by their fault trees.

Some solutions in order to improve the effectiveness of the Failure Modes and Effects Analysis (FMEA) and the Fault Tree Analysis (FTA) techniques using new approaches, including those based on the artificial intelligence, as well the extension of these techniques for the case of the software systems were also investigated.

II-5.3.2 Reliability testing of semiconductor devices
The risk of failure resulting from the combined effects of high temperature, humidity and electrical bias continues to be important for semiconductor devices and requires testing at these stress factors. At the same time, the component manufacturer must have reliable information on the behaviour of his own products at the kind of stress used for screening.

As a result of our researches, based on the modeling of the physical phenomena involved, design curves at temperature cycling both for screening and qualification testing were obtained for several types of semiconductor devices.

A model for the stress (temperature and voltage) dependence of the semiconductor device reliability was developed taking into account the physical aspects of the failure mechanisms involved; this model is useful for the design of reliability accelerated tests.

We have also investigated the influence of humidity on semiconductor device reliability, with two main purposes: to emphasize the role of humidity in the failure process as a stress factor and to model the reliability - humidity relationship. On this basis an original model, a generalized Arrhenius relation was derived. It is important to mention that this model can also be used for the superposition of many stress factors: thermal cycling, pressure and mechanical stress.

II-5.3.3 Recent developments

- Coordination of the Special Issue on "Quality Effort in Europe" (L. Balme and I.C. Bacivarov - Guest Editors) of the international journal "Quality Engineering" (M. Dekker, USA), vol.9, to appear in 1995;
- The new permanent column "Quality Events in Europe" published by "Quality Engineering" (I.C. Bacivarov, Editor) analysing the scientific (research programmes, conferences, symposia etc), managerial, educational a.o. European events in quality and dependability.

II-5.4 European programme in quality of complex systems (EPIQCS)

Topic leader: L. BALME

Members *: I. BACIVAROV, L. BALME, J. KAESTLI, M.L. SORDAGE, C. GUILLERMOU, R. STEFANI

II-5.4.1 - Presentation

In order to cover new industrial needs in the mastering of quality and dependability of complex integrated systems, an original European Post-graduated Programme specialised in the Management of Quality in Complex Integrated Systems has been created in 1991, with the collaboration of the Consortium Linking Universities of Science and Technology for Education and Research (CLUSTER) and the European Program COMETT II, by several major Technical Universities and Industrial Groups:

UNIVERSITIES:

Key Members:
- Ecole Nationale Supérieure d'Arts et Métiers, Paris, France
- Institut National Polytechnique de Grenoble, France
- Technische Hochschule, Darmstadt, Germany
- Universidad Politecnica, Escuela Tecnica Superior de Ingenieros Industriales, Madrid, Spain.

Associated Members:
- University POLYTECNICA, Bucharest, Romania
- Ecole Nationale de l'Industrie Minérale, Rabat, Morocco.

* List of EPIQCS members only involved in research activity within TIMA Laboratory. Complete list of Steering Committee members and previous research works available upon request from L. BALME.
INDUSTRIAL PARTNERS:

Several Industrial Partners, Quality and Professional Associations are involved in the definition of the courses as well as in the management of the Programme:

Key Members:
- BULL S.A., Paris, France
- CSEM, Centre Suisse d’Electronique et de Microélectronique S.A., Neuchâtel, Switzerland
- DASSAULT Aviation, Paris, France
- ESA, European Space Agency, Noordwyk, The Netherlands
- Grupo CIAT, Madrid, Spain
- Société Générale de Surveillance, Geneva, Switzerland
- European Foundation for Quality Management (EFQM), Brussels, Belgium
- European Organisation for Quality (EOQ), Bern, Switzerland
- Deutsche Gesellschaft für Qualität, Frankfurt am Main, Germany
- Mouvemen Français pour la Qualité, Paris, France
- Conférence des Grandes Ecoles, Paris, France.

The CLUSTER organisation is composed of 10 Universities:
- École Polytechnique Fédérale de Lausanne, Switzerland
- Eindhoven University of Technology, The Netherlands
- Imperial College, London, England
- Institut National Polytechnique de Grenoble, France
- Politecnico di Torino, Italy
- Royal Institute of Technology, Stockholm, Sweden
- Technische Universität, Darmstadt, Germany
- Trinity College, Dublin, Ireland
- Universität (TH) Karlsruhe, Germany
- Université Catholique de Louvain-la-Neuve, Belgium.

II-5.4.2 - EPIQCS objectives and organisation

EPIQCS is a voluntary, non profit European Association gathering Technical Universities, Business Schools as well as Industries, Service Companies and European & National Quality Associations.

The aims of the association are:

- Issue the European Master’s Degree specialised in Quality of Complex Integrated Systems. The European Master’s Degree EPIQCS is recognised by the Universities as well as by the Industrial Partners and the Quality Associations, members of EPIQCS Programme.

- Assist any of its members in the evaluation of linguistic and technical skills of candidates to Quality Degrees and Certificates of Competence.

The European Master’s Degree specialised in Quality of Complex Integrated Systems is accessible to any individual candidate as well as to candidates presented by Universities, Companies and Quality Associations who fulfil the following requirements:

A) Initial requirements

  a) Education

  Engineer degree, master degree, business school degree or equivalent.

  b) Language

  Fluent in the language of the country of practice and English.
B) Complementary requirements

a) Common Core Syllabus on Total Quality Management

Candidates must have followed a complementary training devoted to Total Quality Management, composed of at least 200 hours of courses, practical training and case studies and total syllabus having been approved by the EPIQCS Steering Committee.

b) Specialised Options

In the different options offered by EPIQCS, candidates, after having completed the common-core syllabus, must have followed Specialised Courses composed of at least 180 hours of courses, practical training and case studies, and approved by the EPIQCS Steering Committee.

c) Professional Thesis

Finally, candidates must obtain a Professional Thesis which must be situated at the level of graduated studies.
The Professional Thesis must show the ability of the applicant to build an original approach in the resolution of a complex problem belonging to the quality of complex integrated systems.
A large involvement of the Industrial Partners is requested in the management of the Professional Thesis, giving to the work a large feature of application, without sacrificing the fundamental and theoretical basis typical of academic work.
The Professional Thesis must be prepared for a period of at least 9 months, preferentially after completion of the common core syllabus and the specialised option, under the management of two tutors, one from Industry, one from University, nominated by the Director of the Degree.

C) Issue of the European Master's Degree specialised in Quality of Complex Integrated Systems

On the evidence brought by the candidate that he/she fulfills the above requirements, a Jury composed of at least 3 members of the EPIQCS Steering Committee, 2 of whom belonging to the University issue the Certificate of Competence named: "European Master's Degree specialised in Quality of Complex Integrated Systems", in different options.

II-5.4.3 - EPIQCS results

Until now, EPIQCS has issued 40 degrees, to postgraduate students from Grenoble and Madrid.

The current EPIQCS research works are dealing with the application of ISO 9000 to service industries strongly dependent on their information system, advanced quality assurance modelling in ICs manufacturing, quality assurance in aeronautics CAD-CAM and RAMs modelling applied to service industries.
II-6 Reliable Integrated Systems (RIS)

Group Leader: M. NICOLAIDIS
(e-mail: Michael.Nicolaidis@imag.fr)


Research areas:

This group investigates self-checking circuits, UBIST techniques, BIST techniques, CAD tools for testability, current testing, reliable circuits for space applications, system level test generation.

Contracts:

European:
JESSI AC6, JESSI AC11, ARCHIMEDES (ESPRIT-III Basic Research), FIDES (ESPRIT-III Basic Research Working Group).

II-6.1. Self-checking circuits

Members: H. BEDERR, M. BOUDJIT, O. KEBICHI, M. NICOLAIDIS, F. VARGAS

Periodic off-line testing of VLSI circuits may be used to ensure hardware failure detection. However, errors produced by hardware faults will remain undetected until the test phase. Also, off-line testing is not effective against transient faults. On the other hand, concurrent error detection techniques are able to detect errors due to both hardware faults and transient faults as and when they occur. Concurrent error detection based on software encoding techniques needs special software development and will significantly decrease the system speed. Alternatively, hardware encoding based on special-designed self-checking circuits may be used. One advantage of self-checking circuits is that they may be designed to cover well known models of hardware faults.

A self-checking block is composed by a functional block which generates encoded outputs and a checker which verifies these outputs. The checker delivers a two output error indication signal (01 and 10 mean correct functioning and the other values mean error detection). The objective of designing self-checking circuits is to achieve the totally self-checking goal, i.e. the first erroneous output of the functional block must signalized by the checker. To ensure this goal, functional blocks and checkers must verify well defined mathematical properties introduced by W. C. Carter and later defined by D. A. Anderson. J. E. Smith and G. Metze have defined the largest class of functional circuits (i.e. strongly fault secure circuits) and, more recently, we have defined the largest class of checkers (i.e. strongly code disjoint checkers) necessary to ensure the TSC goal.

Complex self-checking systems can be designed by assembling several self-checking blocks. In that case a global double-rail checker is used in order to reduce the error indications of the different self-checking blocks into a single error indication.

Several projects are in development in this area concerning the development of new efficient designs of self-checking functional blocks like PLAs, adders, ALUs, RAMs, ROMs, ..., and the development of tools for automatic generation of such circuits.

II-6.1.1. Implementation techniques and tools for self-checking data paths

Recent investigations in the group led to the development of low hardware cost TSC data paths. These developments include the carry checking / parity prediction scheme for adders, ALUs, multipliers and dividers and parity prediction for shifters and barrel shifters. These schemes require low extra hardware
and are compatible with parity checked data paths and memory systems. Thus, the obtained TSC data
paths based on parity checking require low extra hardware.
The carry checking parity prediction arithmetic operators can be designed using standard cells only or
they also can use some full custom two-output static CMOS gates to reduce hardware cost.
A self-checking data path generator using standard and full custom cells has been developed. A
Generator using standard cells only is under development.

II-6.1.2. Tools for generation of self-checking PLAs

We have proposed new implementations of self-checking PLAs derived from the Mak’s scheme. These
implementations allow to reduce drastically the area overhead. A tool has been implemented allowing
the automatic generation of such PLAs. The tool has been experimented over a set of Benchmark PLAs.
The resulting mean area overhead is 19.6%.

II-6.1.3. Synthesis of self-checking multilevel circuits

We believe that this topic is nowadays the most important topic in the area of self-checking circuits.
Tools that synthesize low cost multilevel circuits will allow (together with the generators of self-
checking data paths) the design of cost effective self-checking VLSI circuits, making these techniques
very attractive for industrial use.
PLAs were widely used in the past to automatize the design of VLSI circuits. However, with the
development of efficient tools for synthesis of multilevel circuits, PLAs are loosing interest. In order to
have a complete set of tools that automatize the design of self-checking circuits, we need to develop
tools for synthesis of combinational and sequential multilevel self-checking circuits.
Some investigations by a few research groups on this area have already been done. However, the extra
hardware required for the synthesized circuits is not low enough to make these first tools attractive for
industrial applications.
We believe that there is no single self-checking solution that always lead to the best result. Our objective
on this starting project is to develop various tools leading to various self-checking solutions. The tool
will try all the solutions for each target circuit and will select the one resulting on the lower hardware
cost.

II-6.1.4. Fast output code space computation and self-checking properties verification

A tool allowing fast computation of the output code spaces of embedded blocks in complex self-
checking systems has been developed. The output code spaces can be used in order to verify the self-
checking properties of embedded functional blocks and checkers. Experiments of output code space
computation have been done over a complex system and self-checking properties verification for self-
checking PLAs and for Berger code checkers has been performed for a set of Benchmark PLAs.

II-6.1.5. Theory of analog self-checking circuits

This topic analyses the fundamental constraints involved by the implementation of analog/mixed signals
functional block and checkers and it shows that the design of TSC or SCD checkers cannot be
accomplished. To cope with this problem, a technique based on the concept of self-exercising checkers
is proposed and is illustrated in the case of current/voltage checkers and voltage comparators.

II-6.2. Unified BIST (UBIST) techniques

Members: M. BOUDJIT, O. KEBICHI, M. NICOLAIDIS

We have developed a technique allowing to merge self-checking and BIST designs. This technique
ensures all tests needed for integrated circuits, e.g. off-line test (design verification, manufacturing,
maintenance test) and on-line concurrent error detection.

II-6.2.1. UBIST RAM implementation

Previously we have proposed the bases of the UBIST technique, as well as efficient UBIST
implementations for microprocessor sequencing parts.
Our latest development on UBST addresses RAM blocks. A self-checking RAM implementation is developed. It requires low area overhead and allows to check both the word array and the decoder (usually only the word array is checked). This design is combined with a transparent (i.e. state preserving) BIST implementation. The two implementations are merged according to the UBST technique.

II-6.3. BIST Techniques

Members: O. KEBICHI, B. MAAREF, M. NICOLAIDIS

This project is aimed at developing new BIST techniques and tools for automatic generation of BISTed circuits. In the present phase the project is concentrated on memories.

II-6.3.1. BIST for single-port RAMs

In earlier developments we have proposed an efficient architecture for BISTed RAMs. This work was one of the very first works on RAM BIST. It uses a hierarchical decomposition of the RAM test algorithms and uses a particular block to implement each level of hierarchy. It results a BIST implementations requiring low area overhead. For a more efficient implementation we have introduced the design of Up/Down LFSRs. Recently we have developed a tool allowing the automatic generation of BISTed RAMs based on this architecture and implementing the Marinescu’s RAM test algorithm.

II-6.3.2. Fault modeling, test patterns and BIST for multi-port RAMs

We have shown that, due to the concurrent writes on several RAM words the standard coupling fault model is not accurate for multiport RAMs.
New fault models (complex couplings and concurrent couplings) have been defined to cope with this problem.
Algorithms allowing to detect all single and multiple complex couplings and concurrent couplings have been developed. The topological reduction of these algorithms has been developed to obtain a O(n) test length.

An efficient BIST architecture has been proposed and an automatic generator of BISTed multiport RAMs has been developed for Thomson (TMS) by using the GDT CAD tools and the CSAM (TMS ASIC compiled function library). This tool uses the test algorithms for multi-port RAMs developed in the group.

II-6.3.3. Transparent BIST for RAMs

RAM transparent BIST allows to test a RAM without destroying its contents. This technique allows to use the BIST circuitry in order to test periodically the RAM in the context of the application execution.
We have developed a technique allowing to transform any RAM test algorithm to a transparent one. We have introduced a symmetric property for RAM fault models and we have shown that if the fault model verifies this property, then, the transparent test algorithms offer the same fault coverage as the standard algorithms. We have shown that all the complete RAM fault models as well as the fault models resulting by topological reduction of the standard models are symmetric. Most of the other known reduced fault models are symmetric, only one of these reduced fault models (proposed by Papachristou) has been discovered not to be symmetric. Thus, for modeled faults, transparent BIST offers the same fault coverage as the standard BIST. However, for unmodeled faults, transparent BIST is superior, since the data background changes at each test phase.
We have proposed a transparent BIST architecture and we have developed a tool allowing automatic generation of transparent BISTed RAMs.

II-6.4. Current testing

Members: F. VARGAS, R. OLIVEIRA-DUARTE, T. CALIN, M. NICOLAIDIS

II-6.4.1. Idq current computation based on quality requirements
In the literature, Iddq computation supposes that the faulty device resistance value is known. However, it is very difficult to have data concerning this value. Furthermore, it is likely that the resistance value of faulty devices can take values within a broad range (indeed from zero to infinite). In this work, we consider that the faulty device resistance can take any possible value. Then the computation of the Iddq current is given as following: the designer determines the quality required for the circuit signals (a range of electrical values guaranteeing desired noise margins). Then, our technique determines the reference current for the Built-In Current Sensor (BICS) that allows the detection of any fault which does not meet these requirements. Alternatively, the technique can determine the reference current using as quality parameter the total circuit delay.

A tool for automatic Iddq estimation, QUIEST (QUescent ESTimation), has been developed. This tool was implemented in C and in SKILL languages, and it was installed in the CADENCE CAD framework. The designer provides as inputs for QUIEST the desired quality parameters in terms of maximum gate output voltage degradation under which the circuit is considered to be good. The implemented tool has a library of Iddq models for the ES2 standard cells available in the CADENCE framework. QUIEST uses HSPICE to simulate these models. At the end of the process, QUIEST provides the minimum Iddq estimated, with respect to the quality parameters provided by the designer, for the circuit in development.

II-6.4.2. On-line current monitoring

When integrated circuits are intended to be used in space, they must provide protection against radiation. Types of radiations like ionization (total-dose), displacement damage, single-event upset (SEU) or soft-error and their effects on electronic systems must be considered. This research project is mainly concerned with the reliability improvement of bulk/epi and SOS/SOI static CMOS circuits with respect to total-dose and in particular, it is also concerned with the reliability improvement of SRAMs with respect to heavy-ion strikes (SEUs):

I) Total-dose: in the past, the design of circuits that are reliable in total-dose environments has been based on fault avoidance techniques (radiation-hardened circuits). Fault detection (the other fundamental technique for designing reliable electronic systems) has not been explored for faults induced by total-dose. In this topic, we propose an approach based on current testing for concurrent checking of these faults in static CMOS circuits. It performs concurrent monitoring of static current by means of Built-In Current Sensors (BICS) and detects the leakage current (Iddq) which accompanies the parametric shifts. In addition to this fundamental benefit, using BICS allows the selection of high quality circuits during manufacturing testing, resulting in higher mean time to failure.

II) SEUs: conventional techniques use SEU-hardened designs and error detecting and correcting (EDAC) codes for RAMs and memory elements. In this topic, we propose a new technique to improve the reliability of SRAMs used in space radiation environments. This new technique deals with the SRAM power-bus monitoring by using Built-In Current Sensor (BICS) circuits that detect fast transient current in the memory power-bus. This transient current is the result of a single-event upset (SEU) in the memory and it is generated during the inversion of the data stored in the memory cell being upset. The current checking is performed on the SRAM columns and is combined with a single-parity-bit per RAM word, so that abnormal current detection can be followed by error correction.

The techniques described above have also the advantage to perform concurrent checking for permanent faults due to the fabrication process and/or to circuit aging (i.e. bridging faults, gate-oxide shorts, etc.) as well as for soft faults induced by electromagnetic noise. Therefore, they are very suitable for designing highly reliable systems.

The proposed techniques have been validated through fabrication and testing of a fault tolerant RAM prototype.

In addition to the above topics, this project is also concerned with the design of SEU-hardening techniques for latches and flip-flops. Two ways are usually jointly used for hardening circuits: the selection and adoption of the process, and the design itself. This project is mainly concerned with design techniques for hardening integrated circuits, process-related issues are only documented.
II.6.5. *Fail-safe circuits*

*Members: L. F. COSTA, M. NICOLAI DIS*

Fail-safe systems are implemented using a processing part checked using some kind of hardware or software redundancy and by a fail-safe interface which transforms the outputs of the processing part into fail-safe signals (i.e. signals which are either correct or safe). Conventionally, the fail-safe interface is implemented using specific fail-safe discrete components. Such implementations have high cost and are very cumbersome. This work presents VLSI implementable fail-safe interfaces for self-checking systems using duplication or other error-detecting code techniques, and for fault tolerant systems based on triplication. With respect to a scheme that we have proposed in the past, the new scheme uses concurrent checking techniques instead of periodic testing based on BIST implementation.

II.6.6. *Automatic test pattern generation*

*Members: M. BOUDJIT, M. NICOLAI DIS*

II-6.6.1. *System level ATPG*

This tool starts from a two-level description of the combinational part of the blocks of complex VLSI systems. An efficient algorithm is used to transform this description to another one named E-group noncurrent two-level circuit description. This description allows concurrency within any group of product terms having equal outputs. Based on this description, we have developed algorithms allowing ultra fast backward and forward propagation within complex VLSI systems. Experimental results over complex systems shown that the tool is drastically more efficient than existing ATPG tools.

II-6.6.2. *Test for path delay faults*

This work is done in collaboration with the NCSR Democritos and the University of Athens. In this work it has been shown that the set of paths of a circuit can be viewed as a vectorial space having bases with cardinality equal to the total number of gate inputs plus the number of primary outputs minus the number of gates. The delay of any path of the circuit can be computed, by using linear equations over the delays of the paths of any of the existing bases. Thus, only a small number of paths has to be tested, improving drastically the ATPG and the fabrication test process for path delay faults.
II-7 System-Level Synthesis (SLS)

Group Leader: A. A. JERRAYA
(e-mail: Ahmed-Amine.Jerraya@imag.fr)

A.A. JERRAYA, P. KISSION, C. LIEM, G. MARCHIORO, R. PISTORIUS, M. RAHMOUNI, M. ROMDhani,
C. VALDERRAMA, V. VIJAYA RAGHAVAN.

Research areas:

This group investigates hardware-software co-design, system level modeling, partitioning, communication synthesis, behavioral synthesis based on VHDL and, structured design methodology for high-level synthesis.

Contracts:

JESSI AC 8, AEROSPATIALE, FRANCE TELECOM, SGS-THOMSON, ESPRIT-NSF, DRET.

II-7.1. System_level_synthesis

The integration of modular and flexible components is becoming a bottle neck when designing modern embarqued electronic systems. For instance, the Airbus A340 includes more than 100 embarqued computers running 20 MB software. In order to master this growing complexity, modular and flexible design methods acting at an early stage of the design process are then essential.

The use of separate tools and methodologies for the design and specification of hardware and software leads to the well-known 90/50 rule. This rule states that 90% of ASICs work first time according to their logic specification. Unfortunately, about 50% of these ASICs need to be reworked because they fail when inserted into their environment. The complexity of today's design and in particular heterogeneous systems implies that global system approaches dealing with both software and hardware are essential in order to solve this problem. It is now commonly admitted that most of these failures could be avoided if circuit design was integrated with system design.

The main objective of this work is to develop COSMOS, a co-design methodology and tools aimed at the design and synthesis of complex mixed hardware-software systems. The system design process starts with a system-level specification that may be given in an existing language such as SDL, State Charts, ESTELLE or LOTOS. Our philosophy is to allow the designer to use one or more of these languages and to translate these descriptions into a common intermediate form, called SOLAR, capable of modeling the main concepts handled by system-level specification languages (concurrency, high-level communication, synchronisation and exceptions). This intermediate form then acts as an input to the system-level synthesis tools.

As shown in Figure 21, the design process in the COSMOS environment is decomposed into four refinement steps: system-level specification, system-level partitioning, communication synthesis (including channel binding and channel mapping), and architecture generation (including virtual prototyping and architecture mapping).

* On leave from University of Monastir, Tunisia
** On leave from University of Sidi Bel Abbes, Algeria
*** SGS-THOMSON, France
**** On leave from NTT, Japan
***** On leave from Danish Technical University, Denmark
All the intermediate models (between system-level specification and C/VHDL) are represented in a design representation called SOLAR. SOLAR is an intermediate form for system-level concepts, which allows several levels of description.

The first step in COSMOS is the translation of the initial description into SOLAR. At this level, a system is represented as a set of communicating processes. The next step in the design flow is partitioning. The goal is to distribute the previous model into a set of communicating modules that will be mapped onto separate processors in the final prototype. This step produces a refined model composed of a set of communicating and heterogeneous processes organized in a graph where the nodes may be either processors or communication units. This step also fixes which technology (hardware or software) will be used for the implementation of each unit. This model needs to be refined in order to fix the communication models. The communication synthesis is composed of two operations. The first one, called channel binding, selects an implementation protocol for each communication unit. The second one, called channel mapping, distributes the protocol among the processors and specific communication controllers. The result is a set of interconnected processes communicating via signals and having the control of the communication distributed among the processes.

The final step is the architecture generation step. It starts with a set of interconnected hardware/software sub-systems (output of communication synthesis) and makes use of two methods in order to produce a prototype. The first method produces a virtual prototype that can be used for simulation. The virtual prototype is an abstract architecture represented by VHDL for the hardware elements and by C for the software. This description is finally mapped onto a multi-processor architecture.
Of course the design process will include lots of feedback loops in order to redesign parts or the full system. At any stage of the design, the user can cancel one or several design steps in order to explore new choices.

II-7.1.1. System-level modeling

Members: T. BEN ISMAIL, M. ROMDHANI, G. MARCHIORO

The aim of this work is the definition of SOLAR, a design representation for high level concepts in system synthesis. It is composed of a data representation model and a textual language. Although human readable, SOLAR is not a hardware description language, but an intermediate format only. SOLAR embodies a series of new concepts which we feel are essential for the next generation of complex hardware systems specification and synthesis. The main motivation behind the development of SOLAR is to link CASE tools and IC CAD tools, thereby allowing mixed hardware/software systems' design and synthesis. The goal is to use this representation for the design of complex systems, and more precisely, a network of communicating systems. In order to achieve these goals SOLAR supports High-Level concepts such as hierarchical and interacting FSMs and high-level communication.

The SOLAR system model is designed to accommodate the properties of all system-level specification languages (ESTELLE, LOTOS, SDL, CSP, OCCAM, ESTEREL, StateCharts, SpecChart, etc.) that are relevant to synthesis. Of course, some restrictions on the permissible input will apply in order to have predictable and coherent results. This includes only allowing subsets of the description languages to be used. The objectives of SOLAR are twofold. Firstly, the identification of a basic data-structure that will allow all of the aforementioned requirements to be accommodated. Secondly, the development of system-level synthesis tools, including partitioning and communication synthesis, that will produce a set of interconnected FSMs that may feed existing silicon compilers.

Figure 22 shows a framework example where such a representation may be useful. Although textual, SOLAR is not intended to be a new specification language. Such languages already exist. For example, the behavior of the hardware may be more easily described in a dedicated HDL such as VHDL. On the other hand, system software specifications can be readily represented in existing languages, such as ESTELLE, LOTOS and SDL for communication protocols, CSP and OCCAM for concurrent systems, ESTEREL and StateCharts for real time systems and so on. What SOLAR provides is an intermediate, unifying format for several such languages, that allows mixed hardware/software designs to be represented in a form suitable for their eventual synthesis.

Where SOLAR differs from other system-level representations is in its ability to accommodate system-level communication concepts such as communicating protocols, message passing and channels of communication, thereby allowing it to model most communication schemes. The channel model mixes the principles of monitors and message passing, it is known as the remote procedure call model. The channel in SOLAR allows communication between any number of processes.

During the synthesis process, COSMOS uses an external library of ChannelUnits. A ChannelUnit corresponds to either a standard protocol or a customized protocol described by the user. During partitioning and communication synthesis an abstract model of the channel is used. At the architecture mapping step, an implementation of the channel is needed. This implementation may be the result of an early synthesis step using COSMOS or another design method. It may also correspond to an existing architecture.

Results: A prototype of a SOLAR based environment exists. Interfaces to SDL, StateChart and VHDL have been developed. SOLAR is used for the development of COSMOS.
II-7.1.2. Hardware/Software Partitioning

Members: T. BEN ISMAIL, G. MARCHIORO

Partitioning can be seen as a mapping of functional sub-systems onto abstract processors. During this step a behavior may be distributed among several abstract processors. Each abstract processor may include several behaviors. A partitioning system may be either automatic or interactive. The partitioning starts with two inputs: a system specification and a library of communication models. The output is a new model composed of a set of processors and a set of communication units. The library may be restricted to predefined models or extended with user defined models.

The partitioning step also determines which technology will be used for the implementation of each processor. For example, a design unit may be implemented in pure hardware, in software running on an operating system or in micro-code adapted for a standard microprocessor. The choice is based on criteria such as execution time, rate of use, re-programmability, re-use of existing components and technology limitation.

Results:

In COSMOS, this step is achieved by a partitioning tool box called PARTIF. PARTIF starts with a set of communicating processes organized in a hierarchical manner and described in SOLAR. Each process represents an extended FSM. Another input to PARTIF is a library of SOLAR communication models. The result of system-level partitioning is a set of communicating and heterogeneous processors organized in a graph where the nodes may be either design units or channel units and where the vertices of the graph may be signals or channel accesses.

PARTIF allows an interactive partitioning by means of five system-level transformations primitives. The first three primitives MOVE, MERGE, and CLUSTER allow the reordering of processes within the hierarchy and the merging of processes to form a single process. The following two primitives are SPLIT and CUT. These allow splitting up one design unit to form inter-dependent design units for distribution purposes.
II-7.1.3. Communication synthesis

Members: T. BEN ISMAIL, J.M. DAVEAU

The objective of communication synthesis is to transform a system containing a set of processes communicating via high-level primitives through channels into a set of interconnected processes communicating via signals and having the control of this communication distributed among the processes. As stated above, this activity may be decomposed into two tasks: channel binding and channel mapping.

The channel binding algorithm is assumed to choose the appropriate set of channel units from the library of communication models to carry out the desired communication. The main function of this step is to assign a communication unit for each communication primitive.

A channel unit, taken from this library, is selected in order to provide the desired services required by the communicating design units. This is similar to the binding/allocation of functional units in classic high-level synthesis tools. The communication between the sub-systems may be executed by one of the schemes (synchronous, asynchronous, serial, parallel, etc.) described in the library. The choice of a given channel unit will not only depend on the communication to be executed but also on the performances required and the implementation technology of the communicating design units. The result of channel binding is an hyper-graph where the edges are either abstract processors or channel unit instances and the vertices correspond to channel accesses.

Results: A communication synthesis methodology has been developed. It combines both channel selection and interface synthesis (channel mapping).

II-7.1.4. Virtual Prototyping

Members: C. VALDERRAMA

A virtual prototype is an executable description of the system implementation. In COSMOS, a virtual prototype is composed of three kinds of modules: Software modules in C, Hardware (HW) modules in VHDL, and communication components that may be described in C or in VHDL.

The goal of this work is the definition of a joint environment co-synthesis and co-simulation. This poses the following challenges:
1- communication between the HW and SW modules,
2- coherence between the results of co-simulation and co-synthesis and
3- support for multiple platforms aimed at co-simulation and co-synthesis.

Results:

In COSMOS, virtual prototyping corresponds to the translation of SOLAR into executable code (VHDL and/or C). Each sub-system is translated independently. The output of virtual prototyping is an heterogeneous architecture represented by VHDL for the hardware elements (virtual hardware processors), C for the software elements (virtual software processors), and communication controllers (library components).

II-7.1.5. Prototyping

Members: A. CHANGUEL, M. ABID

Prototyping is the mapping of a virtual prototype onto an architecture that implements the specification.

The architecture mapping may be achieved using standard code generators to transform software parts into assembler code and hardware synthesis tools in order to translate hardware parts into ASICs or virtual hardware processors (emulators). The result is an architecture composed of software components, hardware components and communication components.
Results:

COSMOS uses a modular and flexible architectural model. The general model is composed of three kinds of components: (1) Software components, (2) Hardware components, and (3) communication components. This model serves as a platform onto which a mixed hardware/software system is mapped.

Communication modules come from a channel unit library, they correspond to existing communication models that may be as simple as handshake or as complex as a layered network. For example, a communication controller may correspond to an existing interface circuit, an ASIC or some micro-code executing on a dedicated microprocessor.

The proposed architecture model is general enough to represent a large class of existing hardware/software platforms. It allows different implementations of mixed hardware/software systems. A typical architecture will be composed of hardware modules, software modules, and communication modules linked with buses.

II-7.2. Architectural synthesis based on VHDL

The goal of this work is to develop AMICAL a behavioral synthesis tool that combines behavioral synthesis with methodologies allowing design re-use. AMICAL is based on pragmatic concepts allowing:

1- a close interaction with the designer
2- to handle complex and heterogeneous design through hierarchical design and design re-use
3- an easy integration within CAD environments and design methodologies.

Starting with a pure VHDL input, AMICAL produces a full specification for existing logic and RTL synthesis tools.

Classical synthesis systems usually run in an almost automatic push-button manner, therefore their performances lie on the algorithms implemented. The designer has little freedom in orienting the result. Moreover existing behavioral synthesis tools usually restrict the functional unit concept to modules executing predefined operations of the initial behavioral specification. This kind of push-button behavioral compiler that restrict component to predefined arithmetic and logic operators is convenient for narrow application domain (e.g. regular DSP operators such as filters), but suits less for non regular designs such as complex ASICs that make use of existing designs such as memories with complex protocols, I/O units or more generally complex sub-systems. What is really needed for the design of complex ASICs starting from behavioral description is an interactive environment allowing the user to refine his design through an iterative design process.

AMICAL gets around these limitations of classical behavioral compilers. In addition to a pure automatic execution mode, it allows interactivity. Moreover AMICAL brings a generalization of the concept of functional unit leading to the use of coprocessors as functional units.

The AMICAL design-flow is illustrated by the figure 23. The two kinds of information required for synthesis are a behavioural specification and a functional unit library. AMICAL then generates a register transfer level (RTL) description that can feed existing RTL and logic synthesis and simulation tools.

The behavioural description model allows to handle very large designs based on hierarchical specification. The basic idea behind this model is that a complex system is generally composed of a set of sub-systems performing specific tasks. A high-level specification of such a system needs only to describe the sequencing of these tasks, consequently the coordination of the different sub-systems. Each sub-system is modelled as a functional module designed (or selected) to perform a set of specific operations. Therefore the behavioural specification may be seen as a coordination of the activities of the different sub-systems. The decomposition of a system specification into a global control and detailed tasks allows to handle very complex design through hierarchy.
AMICAL is based on a flexible architecture model allowing hierarchy and design re-use. The target architecture of AMICAL is composed of a top controller, a set of functional units and a communication network. These last two constitute the data-path. The communication network is composed of buses, multiplexers and registers. The network is built in order to allow the communication between functional units, and with the external world. The number of buses and multiplexers is fixed according to the parallel transfers required by the architecture.

The behavioural description is given as a standard VHDL file following a specific style. The use of complex sub-systems is made through procedure and function calls. For each procedure or function used, the library must include at least one functional unit able to execute the corresponding operation. In figure 23, the VHDL description makes call to a DCT function and uses a memory with a complex protocol (mread, mwrite). The library includes a memory, an ALU, and a DSP processor able to execute these operations. Of course, for each operation we may have several modules able to execute it. The system will select automatically the best solution. During the different steps involved in the behavioural synthesis, the functional units are used as black boxes. These may correspond to already designed complex systems. The different steps involved in the synthesis process are: scheduling, allocation and architecture generation.

![Figure 23: AMICAL design-flow](image)

**Results:**

The behavioural synthesis system AMICAL is pragmatic and seems to correspond to designers' needs. The most important feature of AMICAL is the fact that it combines traditional behavioural level synthesis algorithms with the ability to allow designer intervention at almost any stage of the synthesis process. The use of powerful architecture allows AMICAL to handle complex design. Several large examples, including the MPEG-AUDIO decoder, an answering machine and a PID have also been used for AMICAL evaluation. The PID circuit makes use of several complex operators including a fixed point unit that have been compiled with AMICAL itself. More recently two very large designs have been achieved using AMICAL. A motion estimator for an MPEG2 video decoder has been designed in cooperation with SGS-Thomson. This design makes use of two memory units with sophisticated protocols, of a DSP processor designed by CATHEDRAL and of 2 clocks of different frequencies. The other design is an adaptive speed controller aimed to drive up to 18 motors. The design makes use of a fuzzy logic model to implement the adaptive control. These experiments have shown that the use of AMICAL allows an increase of productivity by a factor of 5 to 10.
II-7.2.1. Scheduling and Optimization for the Synthesis of Control Flow Dominated Design

Member: M. RAHMOUNI

Scheduling is one of the central tasks in high level synthesis, it consists on partitioning the design behavior into control steps such that all operations in a control step execute in clock cycle. We consider the problem of scheduling descriptions represented by control flow graphs.

Path-based scheduling algorithms (PBS) have proved themselves to be much more efficient than classical approaches when dealing with descriptions of control-flow dominated circuits. The first application of PBS to synthesis was made by Camposano and was based on algorithms first proposed for microcode compaction.

Results:

Around PBS, we have developed two heuristics named Dynamic Loop Scheduling (DLS), and Pipeline Path-based Scheduling (PPS). DLS comes to reduce the complexity of PBS which is exponential, by resolving the problem of path explosion by cutting the path on the fly. PPS concentrates on optimizing the execution of loops. In real time applications, loops are the most time critical part. PPS uses a new technique for pipelining loops in order to identify any parallelism that may exist beyond loop boundaries.

II-7.2.2. Interactive behavioral synthesis

Member: H. DING

The goal of this work is to make behavioral synthesis flexible and practical for architecture exploration.

AMICAL is organised as an interactive environment with the ability to allow designer intervention almost any stage of the synthesis process. The designer can simultaneously view both the control section and the data-path as well as their inter-relation. For each synthesis step, the designer can choose between automatic, manual or step-by-step execution. If either of the latter two modes is selected, AMICAL verifies that all modifications comply with a set of rules corresponding to the particular synthesis task. AMICAL also generates a statistical evaluation of each design configuration. In addition, all of the synthesis steps are performed in real-time making the system truly interactive. The combination of automatic and manual synthesis allows a quick and broad exploration of the design space in real time.

Additionally the user can select between several architectural styles for the data-path (Bus-based, Mux-based), for the controller (Mixed FSM, programmable controller) and for synchronization (different pipelining scheme).

Results:

A full interactive synthesis environment has been developed. Its being used for the design of industrial complex CMOS circuits.

II-7.2.3. Linking behavioral synthesis with existing CAD environments

Member: V. VIJAYA RAGHAVAN

The goal of this work is to define methods and tools in order to ease the link between AMICAL and existing CAD environments. This work addresses three tasks:

* Mixing synthesizable and non synthesizable specification. This is made through a powerful programmable personalisation method allowing to combine the output of AMICAL with the non synthesizable parts of the design.
* Pre-Floor planning: Decomposition of the output of AMICAL into regular datapaths and suited for data-path compilers and control blocks suited for logic synthesis.

* Libraries: A library of abstract components is used. End user libraries are supported for both fixed and generic components which may correspond to mega-cores.

Results:

This work constitutes the back-end of AMICAL. Several tools have already been developed and used for the synthesis of real-life designs.

II-7.2.4. Behavioral synthesis for structured design methods and design re-use

Member: P. KISSION

In order to cope with designs of increasing size and complexity, it is then clear that we need improvements of the design quality and designers' productivity. This may be achieved in two ways that can be combined:

1) Using more structured design methodologies for an extensive re-use of existing components and sub-systems. It seems that 70% of new designs correspond to existing components that cannot be reused because of a lack of methodologies and tools.

2) Providing higher level design tools allowing to start from a higher level of abstraction. After the success and the widespread acceptance of logic and RTL synthesis, the next step is behavioural synthesis, commonly called architectural or high-level synthesis.

The goal of this work is to combine structured design methodology and AMICAL in order to design complex heterogeneous systems.

Structured design methodology allows to handle very complex design with hierarchical approach. Hierarchical design proceeds by partitioning a system into modules. The implementation details of these modules are hidden. Proper partitioning allows independence between the design of the different parts. The decomposition is generally guided by structuring rules aimed to hide local design decisions, such that only the interface of each module is visible.

The main steps involved in structured design methodology for high-level design are shown by figure 24. They include a system-level analysis and partitioning step and a high-level design step. The system-level analysis and partitioning step starts with the high-level specification; its aim is:

1) To structure the design in order to produce a hierarchical decomposition of the initial specification. This leads to the isolation of sub-systems that will be design independently as well as that of sub-functions that will be executed on specific functional units.

2) To select the components to be used; these may either be standard existing functional units or specific modules that have to be designed.

These two aspects are inter-related. The hierarchical decomposition may be influenced by the set of already existing components. On the other side, the selection of the components is influenced by the hierarchical decomposition of the design.

Results:

This methodology has been used successfully for the design of several large examples.
II-7.2.5. Methodology for the design of complex and heterogeneous design using behavioral synthesis

Members: E. BERREBI, J. FREHEL

The design of complex modules such as an integrated system on chip may need the use of different behavioral synthesis tools corresponding to the different functions implemented by the system. Complex and intensive data computation may need throughput oriented synthesis tools such as cathedral whereas the design of complex control function is made using AMICAL. Of course the system may include blocks described at the RTL and netlist level.

This work is aimed at the definition of full design scheme allowing to combine several synthesis tools.

Results:

A complex design has already been designed using this approach. A motion estimator circuit has been designed using AMICAL. This design makes use of 2 memories with sophisticated protocol and a DSP processor designed by CATHEDRAL.

II-7.2.6. Behavioral synthesis of reprogrammable design

Members: P. KISSION, M. BENMOHAMMED, M. RAHMOUNI, H. DING

In order to allow late changes when designing the chip architecture, the controller needs to be programmable. In the present version of AMICAL, a non-programmable system-level controller can be described as a flat FSM. The goal of this work is to develop an extension of AMICAL, which will allow to generate a programmable controller.
AMICAL produces a system composed of a complex datapath and a controller. The data path may include complex functional units. These are described as a co-processor, executing complex procedures and functions. This model allows for design re-use and a recursive design methodology, i.e. a design produced by AMICAL may be used as a component in a more complex design. The main problem when extending AMICAL for the generation of programmable controllers will be to handle these complex functional units.

II-7.2.7. Programmable Architecture Design

Member: C. LIEM

This work is concerned with methodologies for the development of new ASIP architectures. Starting from a set of behavioral level descriptions of typical functions for the application domain, the objective is to determine an instruction-set optimized for the application. In turn, this instruction-set implies the definition of the data path programme sequencer, memory structure, peripherals, etc.

Given that a compiler maps an application to a processor architecture, the compiler could be used as an analysis tool to develop better architectures in the areas of data or control-flow efficiency. The instruction-set of an ASIP is the hardware/software interface and the level at which many trade-offs between speed, flexibility, hardware complexity, and compiler efficiency can be made.

This work looks at applications from a compiler perspective in an attempt to characterize the hardware resource needs for efficient functionality. Naturally, these analyses also lead to better code generation approaches.

II-7.2.8. Behavioral synthesis for low power

Members: H. DING, P. KISSION

The goal of this work is to deal with power issues at the early stage of the design, i.e. during architectural synthesis. While the largest gain is expected at the architectural level, the estimation is most critical here. The goal is to take into account the power consumption evaluation and optimization during the early stages of the design process. At this level the library elements are large cores and complex macro-blocks. We need a macroscopic model for power. Our approach considers the number of switching elements in each library element for each clock cycle. Besides, each component is characterized by a switching level when idle. This model allows to estimate with a large precision the power consumption at the clock cycle. The dynamic nature of power consumption can also be handled by using a kind of power simulation at the clock cycle level. We are planning to use this estimation for guiding the synthesis process in order to select the best solution (allocation, scheduling) in terms of power.
III - SERVICE ACTIVITY

The Laboratory is hosting the CMP Service Activity.

CMP

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Ch. GARNIER, N. KRIM, S. LAYE, B. MERCIER,
JF. PAILLOTIN, K. TORKI

The CMP project (Circuits Multi Projets) is a project undertaken since 1981 by the Laboratory. In 1984, the service became a "Unité de Service et de Recherche", depending on CNRS and INPG. This project allows the Universities, Research Laboratories and Companies to fabricate the integrated circuits that they have designed. The originality of the project consisted originally in the regrouping, on the same slice of silicon, of a large number of circuits. Thus accessible costs of fabrication are obtained.

In addition since 1981, about 1500 circuits for Research Education and Industry have been fabricated for use in France and also other countries.

For each project, the operations to be achieved are the following :

- the collection of circuits described in a common language
- the checking of the circuits (syntax checking and design rules checking)
- the assembly in Macro-blocks (sets of chips)
- the generation of the entry connections for the manufacturer
- subcontracting the fabrication of the circuits
- subcontracting packaging of the chips
- the chip delivery to the users.

Since 1981, 126 MPC projects have been undertaken. The total number of manufactured circuits has passed from 8 in 1981 to 114 in 1992, 197 in 1993, and 251 in 1994. The complexity of the circuits has passed from several thousands transistors in 1981 to more than a hundred thousand transistors since 1985. NMOS technologies were used from 1981 to 1986 and CMOS from 1984 up to now. During the last four years, activities have been widely increased. This is reflected by the TABLE II "CMP Development since 1989". From 1990 to 1994, the number of runs per year has been multiplied by 3.5, the number of circuits has doubled, the number of participating Institutions has tripled, and 10 different technologies are offered instead of 3.

In 1992, 22 projects grouped 114 circuits. In 1993, 25 projects grouped 197 circuits, and in 1994 32 projects grouped 251 circuits. Technologies used in 1994 were CMOS DLM* 1.5 μ, 1.2 μ, 1.0 μ, 0.7 μ of ES2* company, CMOS DLP* DLM 1.2 μ and CMOS DLM 0.8 μ of AMS* company, BiCMOS DLP DLM 1.2 μ of AMS, Bipolar Gate Array of TCS* company, GaAs 0.8μ/0.6μ of VSC* and CMOS 0.5 μ TLM of SGS-Thomson / France Telecom. CMP opened the service to companies in 1990, and in 1994 CMP fabricated 81 industrial prototypes (compared to 23 in 1993), in particular for Small and Medium sized Industries (SMIs), out of a total of 251 circuits.

The CMP project calls upon the multiple competences of all members of the Research group : development of software tools (to check or correct various syntax descriptions), determination of the rules of multitechnological design, working with EDIF* format (a translator EDIF-GDS2-EDIF has been achieved in 1990 for UNIX and VMS systems), library implementation for several softwares and several technologies: since 1992, CMP developed library kits for AMS (1.2 μ and 0.8 μ CMOS, 1.2 μ BiCMOS) on CADENCE and COMPASS softwares. Library kits for PC computers were also
developed: for ES2 1.2 μ and 1.0 μ CMOS and AMS 1.2 μ and 0.8 μ CMOS on TANNER/L-Edit software.

In 1993, CMP introduced a service on digital GaAs, for high speed digital and mixed analog/digital circuits. In 1994, CMP introduced two very advanced industrial processes: CMOS 0.5 μ Triple Layer Metal from SGS-Thomson / France Telecom fabricated at Crolles near Grenoble, and the MMIC GaAs 0.2 μ (based on pseudomorphic High Electron Mobility Transistors) from PML Philips Microwave Liméil, near Paris. Access to new technologies for high performance systems (Multi Chip Modules) continued to be provided and will be developed in 1995.

**TABLE II** shows CMP development since 1989.
**TABLE III (a and b)** lists the centers having submitted circuits to the CMP Service.
**TABLE IV (a and b)** depicts the evolution of CMP projects between 1981 and 1994.

The CMP has been supported in 1994 by the Ministry for Higher Education and Research (MESR*, through the CNFM*), the National Research Center (CNRS*/SPI*), and the Ministry for Industry (MIPTCE*, through the CNFM). CMP is participating to European Initiatives, aimed at serving European Universities and SMIs.

A specific report is available upon request.

France has been a pioneer country in this type of infrastructure since chip fabrication for Universities has been started in 1981 by CMP; the elementary CAD software LUCIE has been provided to 36 Academic Institutions in France and foreign countries in the 80s (see **TABLE V**: distribution of the LUCIE system), industrial CAD software has been distributed to Universities in 1986 by CNFM, testing equipment has been centrally purchased in 1988. As early as 1990, CMP had opened chip fabrication to Industry.

Due to the wide range of technologies offered, due to the fact that these technologies are processed on advanced and industrial lines, and due to the volume of circuits manufactured, CMP has reached an international dimension as well as an established reputation in the world.

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*DLM*: Double Layer Metal  
*DLP*: Double Layer Polysilicon  
*ES2*: European Silicon Structures  
*AMS*: Austria Mikro Systeme International  
*TCS*: Thomson Composants Spécifiques  
*EDIF*: Electronic Design Interchange Format  
*VSC*: Vitesse Semiconductor Corporation  
*LIRMM*: Laboratoire d'Informatique, Robotique et Microélectronique de Montpellier  
*CNFM*: Comité National de Formation en Microélectronique  
*SMIs*: Small and Medium Industries  
*MESR*: Ministère de l'Enseignement Supérieur et de la Recherche  
*CNRS*: Centre National de la Recherche Scientifique  
*SPI*: Sciences pour l'Ingénieur  
*MIPTCE*: Ministère de l'Industrie, des Postes et Télécommunications et du Commerce Extérieur
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<th>YEAR</th>
<th>RUNS</th>
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<td>5</td>
<td>617 mm²</td>
<td>92</td>
<td>20</td>
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<tr>
<td>1990</td>
<td>9</td>
<td>1259 mm²</td>
<td>129</td>
<td>26</td>
<td>ES2 $2\mu$</td>
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<td>x 1.4</td>
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<tr>
<td>1991</td>
<td>13</td>
<td>1695 mm²</td>
<td>137</td>
<td>29</td>
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<td>1992</td>
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<td>1993</td>
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<td>AMS 2$\mu$ 2M2P</td>
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<td>AMS 1.2$\mu$ 2M 2P</td>
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<td>AMS 1.2$\mu$ 2M2P (BiCMOS)</td>
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<td>TCS 0.8$\mu$ Dig. GaAs</td>
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<td>more integration</td>
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<tr>
<td>1994</td>
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<td>251</td>
<td>75</td>
<td>ES2 $1.5\mu$</td>
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<td>ES2 $0.7\mu$</td>
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**TABLE II: CMP Development since 1989**


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TABLE IIIa - French Institutions having submitted circuits to CMP (total : 71)
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<td>Guaratingueta</td>
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TABLE IIIb - Foreign Institutions having submitted circuits to CMP (total: 65 Institutions from 30 countries)
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**TABLE IVa** - CMP projects from 1981 to 1993
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**TOTAL since 1981 : 126 Projects**

1467 circuits:  623 Research circuits  741 Education circuits  103 Industrial circuits
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**TABLE V : Distribution of the LUCIE system**
## IV - RESOURCES

### IV-1 Human resources

#### IV-1.1 Members of the Laboratory

Table VI presents a list of the researchers and engineers involved in the Laboratory, Table VII presents the researchers from Industry working in the Laboratory, Table VIII lists researchers who stayed in the Laboratory during 1994, Table IX lists researchers working in other institutions, but enrolled with the Laboratory for a thesis, and Table X lists researchers whose advisor is a member of the Laboratory for their foreign thesis.

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<tr>
<td>KACZMAREK</td>
<td>Philippe</td>
</tr>
<tr>
<td>KARAM</td>
<td>Jean-Michel</td>
</tr>
<tr>
<td>KEBICHI</td>
<td>Omar</td>
</tr>
<tr>
<td>KISSION</td>
<td>Polen</td>
</tr>
<tr>
<td>KODRNJA</td>
<td>Mure</td>
</tr>
<tr>
<td>KOLARIK</td>
<td>Vladimir</td>
</tr>
<tr>
<td>KRAM</td>
<td>Nadim</td>
</tr>
<tr>
<td>LACFRAT</td>
<td>William</td>
</tr>
<tr>
<td>LAYE</td>
<td>Sylvaine</td>
</tr>
<tr>
<td>LIEM</td>
<td>Cliff</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Contracted Secretary</td>
</tr>
<tr>
<td></td>
<td>DEA</td>
</tr>
<tr>
<td></td>
<td>Associate Professor</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Res. ND / CIFRE IMD</td>
</tr>
<tr>
<td></td>
<td>Contracted Secretary</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Res. ND / CIFRE SGS-Thomson</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Contracted Engineer</td>
</tr>
<tr>
<td></td>
<td>DEA</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
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<td></td>
<td>Contracted Secretary</td>
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<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Res. ND / CIFRE SGS-Thomson</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
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<td>Researcher ND</td>
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<td></td>
<td>Contracted Engineer</td>
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<td>DEA</td>
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<td>Researcher ND</td>
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<td>Researcher ND</td>
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<td></td>
<td>Contracted Secretary</td>
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<td></td>
<td>Researcher ND</td>
</tr>
<tr>
<td></td>
<td>Res. ND / CIFRE SGS-Thomson</td>
</tr>
<tr>
<td></td>
<td>Researcher ND</td>
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<td></td>
<td>DEA</td>
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<td>Contracted Tech</td>
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<td></td>
<td>Researcher ND</td>
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</table>

(cont’d)
<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Country</th>
<th>Duration for 1994</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABID</td>
<td>Mohamed</td>
<td>Tunisia</td>
<td>1 month</td>
</tr>
<tr>
<td>ALJOUAT</td>
<td>Makhlouf</td>
<td>Algeria</td>
<td>6 months</td>
</tr>
<tr>
<td>APANOVICh</td>
<td>Zinaida</td>
<td>Russia</td>
<td>8 months</td>
</tr>
</tbody>
</table>

**TABLE VI - Members of the Laboratory (for 1994)**

- **DEA** = involved in Pre-research Degree
- **ND** = involved in Doctorate Degree
- **DE** = involved in "Thèse d'État" Degree
- **ATER** = Teaching and Research Assistant

**TABLE VII - Researchers from Industry working in the Laboratory (for 1994)**

- **FREHEL**
  - Jean
  - SGS-Thomson
- **VAUCHER**
  - Christophe
  - IMD
- **TOURON**
  - Philippe
  - IMD
<table>
<thead>
<tr>
<th>Trainees Name</th>
<th>First Name</th>
<th>Country</th>
<th>Duration For 1994</th>
</tr>
</thead>
<tbody>
<tr>
<td>BACIBAROV</td>
<td>Ioan</td>
<td>Romania</td>
<td>3 months</td>
</tr>
<tr>
<td>BEN MOHAMMED</td>
<td>Mohamed</td>
<td>Algeria</td>
<td>4 months</td>
</tr>
<tr>
<td>CAI</td>
<td>Hong Xue</td>
<td>China</td>
<td>1 month</td>
</tr>
<tr>
<td>CASTRO ALVES</td>
<td>Vladimir</td>
<td>Brazil</td>
<td>2 weeks</td>
</tr>
<tr>
<td>DRAKEK</td>
<td>Vladimir</td>
<td>Czech Republic</td>
<td>2 weeks</td>
</tr>
<tr>
<td>FERNANDES</td>
<td>Antonio</td>
<td>Brazil</td>
<td>2 weeks</td>
</tr>
<tr>
<td>FURUHASHI</td>
<td>Goro</td>
<td>Japan</td>
<td>9 months</td>
</tr>
<tr>
<td>JEMAI</td>
<td>Abderrazak</td>
<td>Tunisia</td>
<td>1 month</td>
</tr>
<tr>
<td>KEVALLIK</td>
<td>Andreas</td>
<td>Estonia</td>
<td>2 weeks</td>
</tr>
<tr>
<td>NASRI</td>
<td>Salem</td>
<td>Tunisia</td>
<td>1 week</td>
</tr>
<tr>
<td>NEMCHENKO</td>
<td>Vladimirc</td>
<td>Ukraine</td>
<td>1 week</td>
</tr>
<tr>
<td>ROUSTINOV</td>
<td>Vladimirc</td>
<td>Ukraine</td>
<td>1 week</td>
</tr>
<tr>
<td>RENCZ</td>
<td>Marta</td>
<td>Hungary</td>
<td>2 months</td>
</tr>
<tr>
<td>RICHARDSON</td>
<td>Andrew</td>
<td>England</td>
<td>5 months</td>
</tr>
<tr>
<td>STRUM</td>
<td>Marius</td>
<td>Brasil</td>
<td>1 week</td>
</tr>
<tr>
<td>SZKELES</td>
<td>Vladimir</td>
<td>Hungary</td>
<td>2 weeks</td>
</tr>
<tr>
<td>TUDOR</td>
<td>Bogdan</td>
<td>Romania</td>
<td>3 months</td>
</tr>
<tr>
<td>UBAR</td>
<td>Raimund</td>
<td>Estonia</td>
<td>2 months</td>
</tr>
<tr>
<td>VASSILEVA</td>
<td>Tania</td>
<td>Bulgaria</td>
<td>2 months</td>
</tr>
<tr>
<td>BENEDEK</td>
<td>Zsolt</td>
<td>Hungary</td>
<td>2 months</td>
</tr>
<tr>
<td>BICA</td>
<td>Adrian</td>
<td>Romania</td>
<td>5 months</td>
</tr>
<tr>
<td>BIOGUSHEVITSH</td>
<td>Helena</td>
<td>Estonia</td>
<td>3 months</td>
</tr>
<tr>
<td>BRIK</td>
<td>Marina</td>
<td>Estonia</td>
<td>3 months</td>
</tr>
<tr>
<td>CARRO</td>
<td>Luigi</td>
<td>Brazil</td>
<td>3 weeks</td>
</tr>
<tr>
<td>CHUBB</td>
<td>Bertrand</td>
<td>Spain</td>
<td>2 months</td>
</tr>
<tr>
<td>DOGANU</td>
<td>Radu</td>
<td>Romania</td>
<td>2 months</td>
</tr>
<tr>
<td>DUMITRESCU</td>
<td>Mihail</td>
<td>Estonia</td>
<td>3 months</td>
</tr>
<tr>
<td>DUSHINA</td>
<td>Julia</td>
<td>Denmark</td>
<td>3 months</td>
</tr>
<tr>
<td>HALD</td>
<td>Bjarte</td>
<td>Tunisia</td>
<td>5 months</td>
</tr>
<tr>
<td>JEGUIRIM</td>
<td>Nabil</td>
<td>Algeria</td>
<td>1 week</td>
</tr>
<tr>
<td>KCCI-AISSA</td>
<td>Salim</td>
<td>Hungary</td>
<td>2 months</td>
</tr>
<tr>
<td>KOHARI</td>
<td>Zsolt</td>
<td>Hungary</td>
<td>3 months</td>
</tr>
<tr>
<td>KOVACS</td>
<td>Laszlo</td>
<td>Germany</td>
<td>2 months</td>
</tr>
<tr>
<td>LEVERING</td>
<td>Volker</td>
<td>Hungary</td>
<td>4 months</td>
</tr>
<tr>
<td>MARTA</td>
<td>Csaba</td>
<td>Denmark</td>
<td>2 months</td>
</tr>
<tr>
<td>MORTENSEN</td>
<td>Lars Bo</td>
<td>Tunisia</td>
<td>3 months</td>
</tr>
<tr>
<td>MTIBAA</td>
<td>Abdellatif</td>
<td>Estonia</td>
<td>9 months</td>
</tr>
<tr>
<td>MYAROSHIN</td>
<td>Pjotr</td>
<td>Denmark</td>
<td>3 months</td>
</tr>
<tr>
<td>NIELSEN</td>
<td>Christian</td>
<td>Germany</td>
<td>1 week</td>
</tr>
<tr>
<td>OELS</td>
<td>Wolfgang</td>
<td>England</td>
<td>3 months</td>
</tr>
<tr>
<td>OLBRICH</td>
<td>Thomas</td>
<td>Hungary</td>
<td>2 weeks</td>
</tr>
<tr>
<td>OLAH</td>
<td>Miklos</td>
<td>Estonia</td>
<td>8 months</td>
</tr>
<tr>
<td>PAOMETS</td>
<td>Pridi</td>
<td>Estonia</td>
<td>3 months</td>
</tr>
<tr>
<td>PAIS</td>
<td>Mart</td>
<td>Estonia</td>
<td>3 months</td>
</tr>
<tr>
<td>PIGNOL</td>
<td>Thierry</td>
<td>France (ENSERG)</td>
<td>3 months</td>
</tr>
<tr>
<td>POLDRE</td>
<td>Juri</td>
<td>Estonia</td>
<td>2 weeks</td>
</tr>
<tr>
<td>RAJK</td>
<td>Jan</td>
<td>Estonia</td>
<td>2 months</td>
</tr>
<tr>
<td>ROJA</td>
<td>Andre</td>
<td>Brazil</td>
<td>4 months</td>
</tr>
<tr>
<td>SAAB</td>
<td>Khaled</td>
<td>Canada</td>
<td>6 weeks</td>
</tr>
<tr>
<td>SLAMANI</td>
<td>Mustapha</td>
<td>Canada</td>
<td>3 weeks</td>
</tr>
<tr>
<td>SUDJITSON</td>
<td>Alexander</td>
<td>Estonia</td>
<td>1 month</td>
</tr>
<tr>
<td>SZEKERES</td>
<td>Csaba</td>
<td>Hungary</td>
<td>3 months</td>
</tr>
<tr>
<td>TCHOUMATCHENKO</td>
<td>Vassily</td>
<td>Bulgaria</td>
<td>4.5 months</td>
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<td>VAINOMAA</td>
<td>Kaido</td>
<td>Estonia</td>
<td>1 month</td>
</tr>
<tr>
<td>YANG</td>
<td>Fengming</td>
<td>Germany</td>
<td>4 months</td>
</tr>
<tr>
<td>ZSOLDOS</td>
<td>Sandor</td>
<td>Hungary</td>
<td>3 months</td>
</tr>
</tbody>
</table>

**TABLE VIII : Visitors and Trainees (for 1994)**

| DULIEUX-VERGUIN      | Pascale     | HEWLETT PACKARD - Grenoble - France |
| EL HASSAN            | Bachar      | CNET - Meylan - France             |
| GUILLERMOU           | Christophe  | DASSAULT - St Cloud - France       |
| KAESTLI              | Jacques     | Société Générale de Surveillance - Genève - Switzerland |
| LEMERY               | François    | SGS-Thomson - Grenoble - France   |
| SORDAGE              | Marie-Line  | SGS-Thomson - Preyvestin - France |
| STEFANI              | Robert      | APAQ- Paris - France              |

**TABLE IX : Researchers working in other institutions, but enrolled with the Laboratory for their thesis in Grenoble**

| ABID            | Mohamed     | UNIV. of Monastir - Tunisia       |
| ALIUAT          | Makhlouf    | UNIV. of Constantine - Algeria    |
| BENMOHAMMED     | Mohamed     | UNIV. of Sidi Bel Abbès - Algeria |

**TABLE X : Researchers whose advisor is a member of the Laboratory for their thesis abroad**
IV-1.2 Biographies of staff members
Louis J. BALME

Born August 23rd, 1951 in Grenoble, France
Married, 3 children
French

**Education**

1972 : Master's Degree - Economics and Politics - IEP Grenoble

1975 : Master's Degree - Electronics - Institut National Polytechnique - Grenoble (INPG)

1976 : PhD Electronics - INPG
"Applications of Spectral Bioimpedometry to EEG and cerebral imagery"

1990 : Habilitation à Diriger des Recherches (French National Authorization to Supervise Research)

**Position**

* Associate Professor in Electronics at Institut National Polytechnique de Grenoble (INPG)

**Current Responsibilities**

* Professor in Signal Processing, Information Theory and Quality of Complex Systems (RAMs)
* Responsible for Quality Complex integrated Systems research group at TIMA Laboratory
* Secretary General of the European Programme in Quality of Complex Integrated Systems

**Previous Positions**

* Director of Corporate Relations of INPG (1984-1991)
* President and CEO of SYMAG Computers (1979-1984)
* Assistant Professor INPG (1974-1979)

**Miscellaneous**

* Registered European Quality Consultant (since 1993)
* Consultant KEYO Corporation (1984-1987)
* President of Synergy Commission at the French computer Industry Association (1984-1987)
* Director of the INPG Master's Degree "Quality of Computers Systems" (1989-1992)
* Vice-President of Merlin Gerin - INPG Economic Interest Grouping (1989-1992)
* 44 publications
* 7 PhDs Management
* 16 Professional Theses Management
* Gold Medal from the International Inventors Exhibition - Brussels 1986
Bernard COURTOIS

Born April 17th, 1948
Married, 2 children
French

Education

1967 - Baccalaureat degree - Mathematics
1968 - Baccalaureat degree - Philosophy
1967 - 1970 Mathematics in Paris
1970 - 1973 National School for Informatics and Applied Mathematics in Grenoble
1973 - Engineer degree
1976 - Doctor-Engineer degree
1981 - Docteur d'Etat degree

Position

"Directeur de Recherches" CNRS

Current responsibilities

* Director of TIMA Laboratory
* Director of CMP Service

Miscellaneous

* Has authored or co-authored many scientific papers
* Has served in many Committees of Conferences & Workshops
* Has served as a reviewer of research proposals to CEC, NATO, NSF, SERC.
Hubert DELORI

Born December 26th, 1946
Married, 5 children
French

Education

1970  Engineer degree from Ecole Centrale de Lyon.

Position

"Ingénieur de Recherche" at CNRS (Centre National de la Recherche Scientifique).

Past activities

1970  Programming at IBM Corbeil-Essonnes.
1972  Teaching in Mathematics and Statistics in Algeria (for the military service).
1973  Engineer at "Cabinet Roland Olivier": working in statistics for a national inquiry about agriculture in Algeria.
1975  Education of physically handicapped young people for social re-insertion.
1978  Engineer at ICARE (Informatique Communale Alpes Rhône) at the town hall of Saint Etienne: responsible of the working of the informatics applications.
1979  Complementary studying in System Programming at "Institut de Programmation de Grenoble" (1 year).
1980  Programming of software tools in Computer Aided Education (in the group of PC SCHOLI, Professor at University of Grenoble).
1981  In the same group, participation to a 2 years project in Computer Aided Education: Study of methods and realization of French lessons for Arabic people.

Current responsibilities

* Technical responsible since 1983 for the CMP (Circuits Multi Projets): national service for manufacturing integrated circuits for all the french Universities and Research Laboratories (about 1500 integrated circuits fabricated since 1981).
Christophe GARNIER

Born November 26th, 1964
Married
French

Education

1988 - DEA Electronics, University of Strasbourg, France
1991 - Ph.D. degree (Microelectronics) "New self-aligned technology for MESFET and TEGFET on GaAs and AlGaAs digital circuits".

Position

Contractual engineer with CMP since January 1991

Current responsibilities

* SGS-Thomson BiCMOS runs
* GaAs runs
**MCM activity.
Alain GUYOT

Born September 11th, 1945
Married, 3 children
French

Education

1970 - Master in Computer Science from Grenoble University
1975 - Ph.D in Computer Science from Grenoble University
1991 - "Habilitation à diriger des Recherches"

Position

Assistant Professor (Maitre de Conférences) at ENSIMAG (Ecole Nationale
Supérieure d'Informatique et de Mathématiques Appliquées de Grenoble) since 1986

Past activities

A. Guyot has been teaching computer architecture and VLSI design mainly at ENSIMAG
and Grenoble University since 1971.

He has been a visiting scholar or invited professor with the CSL group in Stanford
University (Prof. M. Flynn), Microelectronic group in Telecom University, Paris (Prof.
Jutand) and LEG-EPFL in Lausanne (Prof. M. Declercq). He has participated in 1980 to the
starting of the CMP foundry service. He is the author or co-author of more than 50 scientific
publications in Journals, Conference Proceedings, or Research Reports. He has served as a
reviewer for ESSCIRC, VLSI, Computer Arithmetic, EUROASIC, IEEE TC, CAVE and
other conferences, and is a member of several working groups in EUROCHIP.

Current responsibilities

* Responsibility of the Integrated Systems Design Group

* Currently responsible of the project "OCAPI" aimed at the design of a family of
  integrated arithmetic processors, partially supported by the GCIS.
Ahmed Amine JERRAYA

Born August 1st, 1955
Married
French and Tunisian

Education

1980 Engineer degree, Faculté des Sciences de Tunis, Tunisie.
1981 DEA, Computer Science, Institut Polytechnique de Grenoble, (INPG), France
1983 Doctor-Engineer degree, Computer Science, INPG.
1989 Doctorat d'Etat degree, INPG.

Position

Researcher with CNRS, the French National Center for Scientific Research. Section: Computer Science.

Past Activities

- Participated to the LUCIF system, highly successful layout tools, distributed in the early 80s to 20 Laboratories in France and 17 abroad.
- Participated to the definition of the symbolic layout STYX system in the mid 80s, that is still in use with SGS-Thomson.
- Led the APOLLON/SYCO projects, early architectural synthesis tools, 7 Ph.D, more than 20 international publications
- Led the AMICAL project, a highly successful architectural synthesis tool that is being transferred to industry.

Current Responsibilities

- Leader of the System Level Synthesis Group of TIMA at INPG.

Miscellaneous

- Award of "President de la République" 1980, Best Computer Science Engineer Degree
- Served in the Program Committee of EDAC, High-Level Synthesis Workshop, EuroDac, EuroVHDL, VHDL International, APCHDL CODES Workshop and ICCD.
- Several tutorials in international conferences (EuroVHDL 91, EuroVHDL-EURODAC 92)
- Spent one year at Bell Northern Research in Ottawa, Canada
- Technical Program and Organization Chairperson of IESSS'95 Conference.
Jean Michel KARAM

Born November 14th, 1969
Single
Lebanese

Education

1987 - 1989 Mathématiques supérieures & spéciales, Ecole Supérieure d'Ingénieurs de Beyrouth (ESIB), Lebanon
1993 Engineer degree, Ecole Supérieure d'Ingénieurs en Electrotechnique et Electronique (ESIEE), Paris, France
1993 DEA Microelectronics, University of Paris VII, France

Position

Researcher with TIMA laboratory since January 1994

Current Responsibilities

Leader (in share with B. COURTOIS) of the Microsystems group

Miscellaneous

* Researcher with TIMC laboratory (in share with TIMA laboratory)
* Expert for the UK government funding body EPSRC on research involving Microsystems
* IEEE member
Omar KEBICHI

Born September 11th, 1965
Married
Algerian

Education

1989 : Engineer degree in Electronics, Blida University (Algeria)
1990 : DEA Microelectronics, Institut National Polytechnique de Grenoble (INPG), France
1994 : Ph. D. degree in Microelectronics, Institut National Polytechnique de Grenoble (INPG), France
Thesis : "Techniques and CAD Tools for Automatic Generation of BIST and DFT for RAMs"

Position

Contractual research engineer with TIMA/INPG Laboratory since Sept. 94

Current responsibilities

Participation to JESSI AC6, European project

Miscellaneous

* Several publications in international conferences and journals
* Teaching in DEA
* Program Committee Member of the 1st IEEE Int. On-Line Testing Workshop
Nadim KRIM

Born October 3rd, 1965
Bachelor
French

Education

1988 : Master degree in computer science
1989 : DESS microelectronics, PARIS VI Univ. (MASI), PARIS

Position

Contractual engineer with TIMA Laboratory since October 1993.

Current Responsibilities

CAD Manager at CMP.

Miscellaneous

Sylvaine LAYE

Born March 23rd, 1970
Single
French

Education

1994 : Diplôme d'Etudes Supérieures Techniques
d'informaticque d'entreprises (informatics for companies)

Position

Contractual technician with CMP since February 1993.

Current responsibilities

* Management and distribution of CAD tools and all library kits for all CMP
  users.
Marcelo LUBASZEWSKI

Born April 16th, 1964
Married, 2 children
Brazilian

Education

1986 - Engineer degree - Electrical, Federal University of Rio Grande do Sul, Brazil
1990 - Master degree - Computer Science, Federal University of Rio Grande do Sul, Brazil
1994 - PhD degree - Computer Science, INP Grenoble, France
"The Unified Board Testing applied to the Design of Reliable Systems"

Position

Professor at the Electrical Engineering Department of Federal University of Rio Grande do Sul, Brazil, researcher associated to TIMA/INPG

Current Responsibilities

* TIMA technical responsible (in share with B. COURTOIS and M. NICOLAIDIS) for ARCHIMEDES project (#7107 - ESPRIT III - CEC)

* TIMA technical responsible (in share with B. COURTOIS) for AMATIST project (#8820 - ESPRIT III - CEC)

* Leader (in share with B. COURTOIS) of the Advanced Testing Methods group

Miscellaneous

* Courses and lectures on testing in the framework of cooperation with industries
* Technical activities in cooperative projects with the USA, Canada and Brazil
Meryem MARZOUKI

Born April 17th, 1961
Married
French and Tunisian

Education

1986 - Engineer degree (Computer Science) - University of Tunis, Tunisia
1987 - DEA (Computer Science) - INPG, Grenoble, France
1991 - Ph.D. degree (Computer Science) - INPG, Grenoble. "KBS approaches to VLSI circuit testing : application to prototype validation by contactless testing".

Position

Contractual researcher with TIMA Laboratory (August 1986-October 1992) "Chargée de Recherches" with the CNRS (since October 1992)

Past responsibilities

* Responsible for SEM-based fault location project of the GCIS/CNRS national programme.
* Responsible for ICs certification methodologies project (research contract with CNES).
* TIMA Technical Responsible for ADVICE project (# 271 - ESPRIT I - CEC).

Current responsibilities

Benoit MERCIER

Born June 10th, 1966
Single
French

Education

1988 Master degree in Electronics - University of REIMS
1990 Engineer degree in a Electronics-Microelectronics option, I.S.E.N -Lille- France.

Past Activities


Position

Contractual Engineer with CMP

Current Activities

* SGS-Thomson 0.5 μ runs
* Design kits development
* COMPASS tools.
Mihail NICOLAIDIS

Born April 22nd, 1954
Bachelor
French and Greek

Education

1978 Engineer degree - Mecanical-Electrical, Ecole Polytechnique de l'Université de Thessaloniki.
1981 DEA Electronical, Institut Polytechnique de Grenoble (ENSERG).
1984 Doctor-Engineer degree - Data processing
Design of self-testing integrated circuits for analytical failures hypotheses.

Position

"Directeur de Recherche" at CNRS

Current responsibilities

Responsible of the Reliable Integrated Systems Group of TIMA Laboratory.
Jean-François PAILLOTIN

Born October 6th, 1955
Bachelor
French

Education

1978 - Licence Telecommunications - Reims University
1979 - Licence Computer Sciences - UJF Grenoble
1980 - Master Degree Computer Sciences - UJF Grenoble
1981 - DEA Computer Sciences - INP Grenoble
1984 - Doctorate Computer Sciences - INP Grenoble.

Position

Present position : "Ingénieur de Recherche" National Education

Before :

* LCS researcher, INP Grenoble
* Assistant Teacher at IUT of Computer Sciences, Grenoble
* Assistant Teacher at UJF.

Current activities

* Technical responsible since 1985 for the CMP (Circuits Multi Projets) : national service for manufacturing integrated circuits for all the french Universities and Research Laboratories (about 1500 integrated circuits fabricated since 1981).

* ES2 runs responsible.
Richard PISTORIUS

Born October 31st, 1967
Single
German

Education

1993 : Engineer Degree in Microelectronics, IRISA, Rennes, France and "Universität des Saarlandes", Saarbrücken, Germany

Past activities

1993-1994 : Complementary studies in Economics at "Technische Universität", Munich, Germany (1 year)

Position

Contractual engineer with TIMA Laboratory since November 1994.

Current responsibilities

System engineer at TIMA Laboratory.
Participation to the AMICAL project.
Kholdoun TORKI

Born February 21th 1961
Bachelor
Tunisian

Education

1985 : "Maîtrise" degree in physics and electronics, University of Constantine.
1986 : DEA microelectronics, INPG, Grenoble.

Position

Contractual engineer with CMP-TIMA/INPG Laboratory since June 1990.

Responsibilities :

* Managing design-kit developments for different foundries under different CAD/CAE systems
* Participation and technical responsibilities in promoting microelectronics for SMEs
* Contact person at CMP for the AMS foundry
* PC based CAD tools negotiation support and development.
Christophe VAUCHER

Born February 15th 1962
Married, 1 child
French and Swiss

Education

1987 : Engineer degree (Electronics) - ENSERG, INPG, Grenoble
1988 : DEA (Electronic Systems) - ENSERG, INPG, Grenoble
1993 : Ph.D. degree (Microelectronics) - INPG, Grenoble.
"High density bare boards testing"

Position

IMD Test Systems Div. technical director. IMD Test Systems is a company which activity deals with complex loaded and bare boards testing.

Responsibilities :

* In charge of the development of the Test Systems Division at IMD
* In charge of the bare board part of the Quality of Complex Systems activity at TIMA.

Miscellaneous :

Inventor of several international patents.
IV-1.3 Curriculum vitae of Doctorate candidates

Name: ABID, Mohamed
Expected date of degree: 1996 ("Thèse d'Etat")
Previous degrees: PhD degree
Research interests: Hardware/Software Co-Design
Present employment: ENIM (Ecole Nationale d'Ingénieurs de Monastir), Tunisia

Name: AICHOUCHI, Mohamed
Expected date of degree: Completed
Previous degrees: Electronic Engineering degree (1989), U.S.T. Oran, Algeria
DEA in Automatics (1990), LAG, ENSIEG, Grenoble, France
Research interests: Silicon Compiler, RTL synthesis.
Present employment: Algerian Government Scholarship

Name: ALIOUAT, Makhlouf
Expected date of degree: 1995
Previous degrees: Comp. Sci. Engineering (1978), Univ. of Constantine, Algeria
DEA Comp. Sci. (1983), INPG, Grenoble, France
Ph.D. degree (1986), INPG
Research interests: Dependability of computer systems
Present employment: Institute of computing science, Univ. of Constantine, Algeria

Name: BEDERR, Hakim
Expected date of degree: Completed
Previous degrees: Electronics Engineering (1990), USTHB, Algeria
Research interests: Truth Table Verification of ILAs
Present employment: M.R.T. Scholarship

Name: BENALI, Aadil
Expected date of degree: June 1996
Previous degrees: Electronic Engineer (1992), ENSERG, Grenoble, France
DEA degree (1992), ENSERG, Grenoble, France
Research interests: Image Processing - test of bare circuits
Present employment: IMD, Grenoble (France)

Name: BEN ISMAIL, Tarek
Expected date of degree: June 1995
Previous degrees: Computer Science degree (1991), Univ. of Tunis, Tunisia
DEA Computer Science (1992), INPG, Grenoble, France
Research interests: Partitioning, system-level synthesis
Present employment: Tunisian Government scholarship
Name : BENMOHAMMED, Mohamed

Expected date of degree : June 1997
Previous degrees : Computer Science Engineering (1983), INI, Alger, Algeria
Magister in Computer Sc. (1988), Alger, Algeria
Research interests : Silicon compiler, high-level synthesis
Present employment : Institute of Computer Science, Univ. of Sidi Bel-Abbes, Algeria

Name : BOUDJIT, Mokhtar

Expected date of degree : April 1995
Previous degrees : Electronic Engineering Degree (1989), Univ. d'Algiers(Algeria)
DEA in Microelectronics (1990), U.J., Grenoble (France)
Research interests : Built-In Self-Test, Self-Checking circuits
Present employment : /

Name : BOUTAMINE, Hicham

Expected date of degree : June 1996
Previous degrees : DEA CASIAM (1993), Univ. of Montpellier, France
Research interests : Technology migration
Present employment : /

Name : CALIN, Theodor

Expected date of degree : 1996
Previous degrees : Engineer in Electronics and Telecommunications (1977), Politechnica University of Bucharest, Romania
Research interests : Radiation-tolerant CMOS circuit design, current testing, self-testing microsystem architectures
Present employment : /

Name : CHAAHOU, Faouzi

Expected date of degree : November 1996
Previous degrees : DEA in Microelectronics (1993), Univ. of Montpellier, France
Research interests : CAD tools for analog circuits
Present employment : Scholarship from Morocco's government

Name : CHANGUEL, Adel

Expected date of degree : June 1996
Previous degrees : Electronics Engineer (1993), ENIM, Monastir, Tunisia ; DEA in Microelectronics, (1993), INPG, Grenoble, France
Research interests : High level synthesis (HW/SW co-design)
Present employment : Scholarship from Tunisian's government

Name : COISSARD, Vincent

Expected date of degree : 1997
Previous degrees : DEA in Microelectronics (1993), UJF, Grenoble, France
Research interests : Arithmetic coprocessor design
Present employment : MESR (French Ministry for Research and Higher Education) scholarship
<table>
<thead>
<tr>
<th>Name</th>
<th>COSTA, Luiz Fernando</th>
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<tr>
<td>Expected date of degree</td>
<td>September 1996</td>
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<tr>
<td>Previous degrees</td>
<td>Electrical Engineering Degree, Master Computer Science (1985), (UFMG, Belo Horizonte, Brazil); DEA Microelectronics (1993), UJF, Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>Built-In Self-Test</td>
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<tr>
<td>Present employment</td>
<td>CNPQ (Brazil) scholarship</td>
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<tr>
<th>Name</th>
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<td>Research interests</td>
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<tr>
<th>Name</th>
<th>DING, Hong</th>
</tr>
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<tr>
<td>Expected date of degree</td>
<td>June 1995</td>
</tr>
</tbody>
</table>
| Previous degrees                  | Bachelor Computer Science & Engineering (1984), University of Xi'an Jiaotong (China)  
                                    | Master Computer Science & Engineering (1990), University of Xi'an Jiaotong (China)  
                                    | DEA Microelectronics (1992), UJF, Grenoble, France |
| Research interests                | High-level synthesis                   |
| Present employment                | /                                     |

<table>
<thead>
<tr>
<th>Name</th>
<th>DULIEUX-VERGUIN, Pascale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Expected date of degree</td>
<td>Completed</td>
</tr>
</tbody>
</table>
| Previous degrees                  | MST (Maîtrise de Sciences et Techniques) in Materials' Sciences (1989), Joseph FOURIER University, Grenoble  
                                    | DEA (Diplôme d'Etudes Approfondies) in Microelectronics (1990), Joseph FOURIER University, Grenoble |
| Research interests                | Development of a method to locate precisely any defect on Integrated Circuits owing to Liquid Crystals |
| Present employment                | Member of the Failure Analysis Laboratory especially dedicated to the Grenoble Personal Computer Division, HEWLETT-PACKARD FRANCE Society. |

<table>
<thead>
<tr>
<th>Name</th>
<th>EL HASSAN, Bachar</th>
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<tr>
<td>Expected date of degree</td>
<td>June 1995</td>
</tr>
</tbody>
</table>
| Previous degrees                  | Electronic Engineer (1991), Lebanese University, Engineering Faculty (Lebanon)  
<pre><code>                                | DEA degree (1992), INPG, Grenoble, France |
</code></pre>
<p>| Research interests                | Self-timed circuits, asynchronous architecture |
| Present employment                | CNET (France)                         |</p>
<table>
<thead>
<tr>
<th>Name</th>
<th>Expected date of degree</th>
<th>Previous degrees</th>
<th>Research interests</th>
<th>Present employment</th>
</tr>
</thead>
<tbody>
<tr>
<td>GUILLERMOU, Christophe</td>
<td>1996</td>
<td>IDEN Engineer</td>
<td>Quality Assurance in aeronautics CAD-CAM at Dassault Aviation</td>
<td>DASSAULT AVIATION (France)</td>
</tr>
<tr>
<td>HAMIDI, Belkacem</td>
<td>Completed</td>
<td>Electrical Engineering (1988), Univ. of Tunisia</td>
<td>DEA Microelectronics (1990), INPG, Grenoble, France</td>
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<tr>
<td>KAESTLI, Jacques</td>
<td>1998</td>
<td>EPFL Engineer</td>
<td>RAMs modelling applied to service industries</td>
<td>SGS, Geneva, Switzerland</td>
</tr>
<tr>
<td>KEBICHI, Omar</td>
<td>Completed</td>
<td>Electronic Engineering degree (1989), Univ. of Blida, Algeria</td>
<td>DEA Microelectronics (1990), UJF, Grenoble, France</td>
<td>/</td>
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<tr>
<td>KODRNJA, Marc</td>
<td>August 1995</td>
<td>Microelectronic Engineer (1990), Paris-Sud University, Orsay, France ; DEA in Microelectronics (1993), UJF, Grenoble, France</td>
<td>Analog voltage controlled oscillators and phase locked loop</td>
<td>CIFRE scholarship (with SGS-Thomson)</td>
</tr>
<tr>
<td>KOLARIK, Vladimir</td>
<td>Completed</td>
<td>Engineer Microelectronics (1990), INP Brno, Czechoslovakia, DEA degree (1991), UJF, Grenoble, France</td>
<td>Analog and mixed-signal circuits testing</td>
<td>French Government scholarship</td>
</tr>
</tbody>
</table>
Name : LEMERY, François
Expected date of degree : June 1995
Previous degrees : Engineer (1991), Ecole Centrale de Lyon, France
DEA "Devices of integrated electronic" (1991), INSA-UCBL-BCL
Research interests : Analog and mixed macromodeling
Present employment : SGS-Thomson Microelectronics Central R&D, Grenoble, France

Name : LIEM, Clifford
Expected date of degree : June 1997
Previous degrees : Bachelor of Science, Physics (1989), St. Francis Xavier Univ.
(Canada)
Master of Electrical Engineering (1991), Carleton Univ. (Canada)
Research interests : Retargetable code generation, embedded processors
Present employment : Canadian Government Scholarship

Name : MARCHIORO, Gilberto Fernandes
Expected date of degree : September 1997
Previous degrees : Computer Science degree (1987), Brazil
Master in Computer Science (1991), Brazil
Research interests : Hardware/Software Co-Design, High Level Synthesis
Present employment : CAPES (Brazil) scholarship

Name : MOHAMED, Firas
Expected date of degree : 1996
Previous degrees : DEA on Informatics (1993), Univ. of Montpellier (France)
Research interests : A.I. for analog circuits diagnosis
Present employment : Syrian Government Scholarship

Name : MONTALVO, Luis
Expected date of degree : Completed
Previous degrees : Engineer in Electronics and Telecommunications (1982),
National Polytechnique Institute, Quito, Ecuador
Master of Science in Computer Engineering (1986),
Ohio University, USA
Research interests : Computer Arithmetic
Present employment : Professor at the Electrical Engineering Department of the
National Polytechnique Institute, Quito, Ecuador

Name : MOUSSA, Imed
Expected date of degree : June 1995
Previous degrees : Engineer on Electronics and Telecommunications (1990),
National Engineers University, Tunisia
EA (Etudes Approfondies) in Telecommunications (1991),
National Engineers University, Tunisia
DEA on Electronics and Systems (1992), Clermont II Univ.,
France
Research interests : Computer Arithmetic on GaAs Technology
Present employment : /
<table>
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<tr>
<th>Name</th>
<th>OLIVEIRA DUARTE, Ricardo</th>
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<tr>
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<td>September 1996</td>
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<tr>
<td>Previous degrees</td>
<td>Electronic Engineering degree (1990), UFRJ (Brazil); Master of Sc. in Microelectronics (1992), COPPE-UFRJ, Rio de Janeiro, Brazil</td>
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<tr>
<td>Research interests</td>
<td>FPGA testing, current testing, and self-checking circuits</td>
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<td>Present employment</td>
<td>CNPQ (Brazil) scholarship</td>
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<th>PARET, Jean-Marc</th>
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<td>Previous degrees</td>
<td>Engineer degree, ENSERG/INPG, France; DEA Microelectronics, UJF, France</td>
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<tr>
<td>Research interests</td>
<td>Silicon compatible micromachining</td>
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<td>Present employment</td>
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<td>Previous degrees</td>
<td>Electronic Engineering degree (1991), UFRGS (Brazil); Master of Science in Electronic Engineering (1994), UNICAMP, Campinas, Brazil</td>
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<tr>
<td>Research interests</td>
<td>Self-timed circuits, GaAs digital design</td>
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<tr>
<td>Present employment</td>
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<tr>
<th>Name</th>
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<tr>
<td>Expected date of degree</td>
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<tr>
<td>Previous degrees</td>
<td>Computer Science Engineering degree (1992), Univ. of Tunis, Tunisia; DEA in Computer Science (1993), INPG, Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>Scheduling in high level synthesis</td>
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<td>Present employment</td>
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<tr>
<th>Name</th>
<th>ROMDHANI, Mohamed</th>
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<td>Expected date of degree</td>
<td>June 1996</td>
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<tr>
<td>Previous degrees</td>
<td>Engineer in Informatics (1992), DEA (1993)</td>
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<tr>
<td>Research interests</td>
<td>System level modelling &amp; synthesis</td>
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<tr>
<td>Present employment</td>
<td>Tunisian Government Scholarship</td>
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<tr>
<th>Name</th>
<th>SKAF, Ali</th>
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<tbody>
<tr>
<td>Expected date of degree</td>
<td>June 1995</td>
</tr>
<tr>
<td>Previous degrees</td>
<td>Electronic Engineering degree (1990), ENSERG, Grenoble, France; DEA in Microelectronics (1991), UJF, Grenoble, France</td>
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<tr>
<td>Research interests</td>
<td>IC design and test</td>
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<td>Present employment</td>
<td>MRT scholarship</td>
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</table>

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<tr>
<th>Name</th>
<th>SORDAGE, Marie-Line</th>
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<tr>
<td>Expected date of degree</td>
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<tr>
<td>Previous degrees</td>
<td>PhD in Microelectronics</td>
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<td>Research interests</td>
<td>Advanced Quality Assurance modelling in ICs manufacturing</td>
</tr>
<tr>
<td>Present employment</td>
<td>SGS-Thomson (France)</td>
</tr>
</tbody>
</table>
Name: STEFANI, Robert
Expected date of degree: 1995
Previous degrees: BULL Engineer
Research interests: Application of ISO 9000 to service industries strongly dependent on their information system
Present employment: /

Name: TOUATI, Mohamed Hédi
Expected date of degree: June 1995
Previous degrees: DEA degree (1992), USTL-LIRM, Montpellier, France
Research interests: Test and diagnosis of partial boundary scan boards
Present employment: /

Name: VACHER, André
Expected date of degree: June 1995
Previous degrees: DEA in Microelectronics (1992), UJF, Grenoble, France
Master degree - Electronic, Electrical Engineering and Automatic - Scientific and Medical University, Grenoble, France
Research interests: Integrated circuits for calculation of Fast Fourier Transform
Present employment: French State employee (CNRS, Laboratory of Cristallography), retainting period

Name: VALDERRAMA, Carlos Alberto
Expected date of degree: June 1997
Previous degrees: Electronic Electrical Engineer (1989), National Univ. of Cordoba (Argentina); Master of Science degree (1993), Federal Univ. of Rio de Janeiro (Brazil)
Research interests: System level synthesis, codesign
Present employment: CNPq (Brazil) scholarship

Name: VARGAS, Fabian Luis
Expected date of degree: April 1995
Research interests: Radiation hardened systems for space applications, current testing for CMOS circuits, DFT for RAMs.
Present employment: CPGCC-UFRGS, Porto Alegre - RS, Brazil

Name: VIJAYA RAGHAVAN, Vijay
Expected date of degree: June 1996
Previous degrees: Electrical Engineering degree (1984), Indian Institute of Science
DEA Microelectronics (1993), UJF, Grenoble, France
Research interests: Linking high level synthesis (AMICAL) with industrial CAD systems
Present employment: /
<table>
<thead>
<tr>
<th>Name</th>
<th>VINCI DOS SANTOS, Filipe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Expected date of degree</td>
<td>September 1997</td>
</tr>
<tr>
<td>Research interests</td>
<td>Radiation hardened circuits, on-line analog self-test, integrated detectors</td>
</tr>
<tr>
<td>Present employment</td>
<td>CAPES (Brazil) scholarship</td>
</tr>
</tbody>
</table>
IV-2 TIMA network and computer equipment

IV-2.1 Computer equipment

This equipment is made up of servers, workstations, X terminals, terminal concentrator, alphanumeric terminals, and personal computers. Laser printers are also available, as well as other peripherals like CD-ROM and Hexabyte drivers.

The list follows:

Server:
1 Sparc SS20 (Sun)

Workstations:
2 Sparc SS10/30
2 Sparc IPC (Sun)
1 Sparc IPX (Sun)
1 Sparc 1+ (Sun)
1 MicroVax II (DEC)

Micro Computers:
4 Mac II (Apple)
2 Mac LC (Apple)
5 Mac IIci (Apple)
5 Mac+ (Apple)
6 Mac LC III (Apple)
1 Mac SE (Apple)
1 Classic II (Apple)
2 PowerBook 540 (Apple)
1 PowerBook 160 (Apple)
1 PowerBook 170 (Apple)
1 PowerBook 180 (Apple)
1 Z433D (Zenith Data System)

Terminal Concentrator:
1 Annex II UX - 16 ports (Xylogics)

X Terminals:
1 NCD 19 (NCD)
4 NCD 19r (NCD)
3 NCD 15b (NCD)
7 NCD 15r (NCD)

Alphanumeric Terminals:
10 Infinity (Falco)

IV-2.2 Network wiring and topology

In summer 1992, the network has been completely restructured, physical support (wiring) and topology. The thick Ethernet (10b5) bus has been replaced by a star topology based on Unshielded Twisted Pair (IEEE 802.3/10bT) Ethernet wiring network. The AppleTalk network has been also restructured: a star topology PhoneNet network on Unshielded Twisted Pair has replaced the former LocalTalk bus. Apart from its evolutive feature, this new wiring allows each room of the laboratory to be indifferently connected to any kind of existing resources (AppleTalk/PhoneNet, Ethernet/10bT, RS232 server/concentrator serial lines), through RJ45 connectors.
IV-2.3 Network equipment

The new wiring and topology choice has implied the acquisition of some active network equipments, for both Ethernet and AppleTalk/PhoneNet networks, and for their interconnection. This equipment is detailed in the following:

3 SNMP Hubs (David Expressnet from David Systems)
1 Ethernet-AppleTalk Gateway (GatorBox from Cayman)
1 PhoneNet StarController (from Farallon)
AUI/10bT Micro Transceivers (Allied Telesys)
PhoneNet StarConnectors (from Farallon)

IV-2.4 Interconnections, protocols, and services

TIMA network is interconnected with all other laboratories and schools of Felix Viallet site (downtown) with optic fiber wiring via a Cisco Ethernet router. This router also allows this site to be connected to the ARAMIS network ("Association Rhône-Alpine des Moyens d'Interconnexion Scientifique": the Rhône-Alpes region branch of French national scientific research network), through French Telecoms specialized lines (2 Mb/s). The main used protocol is Internet. This makes TIMA able to reach (and be reached by) any site in the world. Full Internet services are available (telnet, ftp, electronic mail, Usenet news,...).

IV-2.5 Interconnection schemas

Three schemas are given in the following pages in order to illustrate TIMA network and its external interconnections. The first schema ("TIMA NETWORK") illustrates our own network and its link to one of the Ethernet router lines. The second schema (INPG - Site Viallet) - reprinted by courtesy of Claire Rubat du Mérac, INPG network responsible - shows how all of the laboratories (including TIMA) and schools of Felix Viallet site are interconnected, and how they are connected to ARAMIS network. The last schema (ARAMIS network) - reprinted by courtesy of Pierre Laforgue, IMAG network responsible, and the CICG - gives an overview of the different components of ARAMIS network.

IV-2.6 Contacts

Network, Server/WStations, MacIntoshes: Richard Pistorius (Richard.Pistorius@imag.fr)
ARAMIS
Le réseau régional Rhône-Alpes

Figure 27
IV-3 Financial resources

Some data are given below on financial aspects. They are provided for 1989-1994 budget years, to allow comparisons.

In 1989, the budget of the Laboratory has been 9 118 kFF (excluding VAT). This amount does not include salaries of government employees, like CNRS researchers and Professors.

This budget comes from research funds provided by CNRS or Universities (INPG and UJF), from contracts signed with industrial firms or CEC, and from "exceptional" funds or "exceptional" invoices (emitted for example against services). Those funds are accounted by either CNRS, or INPG or UJF. The Table XI gives the distribution, and the Figure 28 represents it. It is to be noted that the input for contracts represent the total amount of the contracts which are signed in 1989, even if the contract will last for several years.

The contractual part represents approx. 80 % of the budget in 1989. The Table XII gives the list of contracts signed in 1989. The CEC part represents approx. 80 % of the contracts.

<table>
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<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>Total</th>
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<td>Research funds</td>
<td>100</td>
<td>182</td>
<td>8</td>
<td>290</td>
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<tr>
<td>Exceptional funds</td>
<td>140</td>
<td>705</td>
<td>-</td>
<td>845</td>
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<tr>
<td>Exceptional invoices</td>
<td>569</td>
<td>239</td>
<td>-</td>
<td>808</td>
</tr>
<tr>
<td>Contracts signed in 1989</td>
<td>335</td>
<td>6 840</td>
<td>-</td>
<td>7 175</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td><strong>1 144</strong></td>
<td><strong>7 966</strong></td>
<td><strong>8</strong></td>
<td><strong>9 118</strong></td>
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**TABLE XI - Budget 1989 (kFF, excluding VAT)**
Figure 28 - Budget 1989

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<th>Contract</th>
<th>Amount</th>
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<td>CEC EUROCHIP</td>
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<td>CEC ASICS</td>
<td>1,853</td>
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<td>SGS - Thomson</td>
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<td>CSEE</td>
<td>115</td>
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<tr>
<td>GCIS</td>
<td>335</td>
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</tbody>
</table>

TABLE XII - Contracts signed in 1989 (kFF, excluding VAT)
In 1990, the budget has been 8,582 kFF (excluding VAT). The Table XIII gives the distribution, and the Figure 29 represents it. Again, the input for contracts represents the total amount of contracts signed in 1990, even if those contracts last for several years.

In 1990, the contractual part represents approximately 43% of the budget. The Table XIV gives the list of contracts signed in 1990.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>162</td>
<td>3</td>
<td>265</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>210</td>
<td>3,404</td>
<td>-</td>
<td>3,614</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>766</td>
<td>210</td>
<td>-</td>
<td>976</td>
</tr>
<tr>
<td>Contracts signed in 1990</td>
<td>-</td>
<td>2,782</td>
<td>-</td>
<td>3,727</td>
</tr>
<tr>
<td>TOTAL</td>
<td>2,196</td>
<td>6,558</td>
<td>-</td>
<td>8,582</td>
</tr>
</tbody>
</table>

Table XIII - Budget 1990 (kFF, excluding VAT)

Figure 29 - Budget 1990
<table>
<thead>
<tr>
<th>Contract</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNES</td>
<td>500</td>
</tr>
<tr>
<td>TMS</td>
<td>240</td>
</tr>
<tr>
<td>MATRA ESPACE (CNES)</td>
<td>292</td>
</tr>
<tr>
<td>IBM</td>
<td>285</td>
</tr>
<tr>
<td>CNES</td>
<td>150</td>
</tr>
<tr>
<td>GCIS</td>
<td>945</td>
</tr>
<tr>
<td>MIAT (JESSI)</td>
<td>1 315</td>
</tr>
<tr>
<td></td>
<td>3 727</td>
</tr>
</tbody>
</table>

TABLE XIV - Contracts signed in 1990 (kFF, excluding VAT)

The key issue when comparing data for 1989 and for 1990 is that the CEC EUROCHIP contract is financially important for 1989. In 1990, the part of industrial contracts has been increased. Those data are nevertheless partially sounded, because of the criterion consisting in account a contract once, the year it is signed.
In 1991, the budget has been 9,322 kFF (excluding VAT). The Table XV gives the distribution, and the Figure 30 represents it. In 1991, the contractual part represents approximately 44%. The CEC part represents 60% through ESPRIT Basic Research, and the JESSI part represents 38%. The Table XVI gives the list of contracts signed in 1991.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>100</td>
<td>165</td>
<td>-</td>
<td>265</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>712</td>
<td>2238</td>
<td>-</td>
<td>2950</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1884</td>
<td>85</td>
<td>-</td>
<td>1969</td>
</tr>
<tr>
<td>Contracts signed in 1991</td>
<td>-</td>
<td>4138</td>
<td>-</td>
<td>4138</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2696</td>
<td>6626</td>
<td>-</td>
<td>9322</td>
</tr>
</tbody>
</table>

**TABLE XV - Budget 1991 (kFF, excluding VAT)**

**Figure 30 - Budget 1991**
In 1992, the budget has been 12,118 kFF (excluding VAT). The Table XVII gives the distribution, and the Figure 31 represents it. In 1992, the contractual part represents approximately 54%. The CEC part represents 68% through ESPRIT Basic Research, and the JESSI part represents 32%. The Table XVIII gives the list of contracts signed in 1992.
Figure 31 - Budget 1992

<table>
<thead>
<tr>
<th>Contract</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC EUROCHIP</td>
<td>4484</td>
</tr>
<tr>
<td>CEC ARCHIMEDES</td>
<td>712</td>
</tr>
<tr>
<td>JESSI MICE / AC 6</td>
<td>880</td>
</tr>
<tr>
<td>JESSI MICE / AC 11</td>
<td>404</td>
</tr>
<tr>
<td>CEC FASED</td>
<td>126</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>6606</strong></td>
</tr>
</tbody>
</table>

TABLE XVIII - Contracts signed in 1992 (kFF, excluding VAT)
In 1993, the budget has been 17,403 kFF (excluding VAT). The Table XIX gives the distribution, and the Figure 32 represents it. In 1993, the contractual part represents approximately 64%. The CEC part represents 61%, and the JESSI part represents 36%.
The Table XX gives the list of contracts signed in 1993.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>166</td>
<td>568</td>
<td>-</td>
<td>734</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>171</td>
<td>2,321</td>
<td>-</td>
<td>2,492</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>2,859</td>
<td>247</td>
<td>-</td>
<td>3,106</td>
</tr>
<tr>
<td>Contracts signed in 1993</td>
<td>99</td>
<td>10,972</td>
<td>-</td>
<td>11,071</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>3,295</td>
<td>14,108</td>
<td>-</td>
<td>17,403</td>
</tr>
</tbody>
</table>

**TABLE XIX - Budget 1993 (kFF, excluding VAT)**

![Figure 32 - Budget 1993](image)
In 1994, the budget has been 19 253 kFF (excluding VAT). The Table XXI gives the distribution, and the Figure 33 represents it. In 1994, the contractual part represents approximately 74%, the CEC part represents 52%, and the JESSI part represents 32%. The Table XXII gives the list of contracts signed in 1994.

<table>
<thead>
<tr>
<th></th>
<th>CNRS</th>
<th>INPG</th>
<th>UJF</th>
<th>ADR</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>185</td>
<td>518</td>
<td>0</td>
<td>0</td>
<td>703</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>40</td>
<td>1 824</td>
<td>0</td>
<td>0</td>
<td>1 864</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>1 935</td>
<td>454</td>
<td>0</td>
<td>0</td>
<td>2 389</td>
</tr>
<tr>
<td>Contracts signed in 1994</td>
<td>0</td>
<td>13 431</td>
<td>565</td>
<td>300</td>
<td>14 296</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>2 160</td>
<td>16 227</td>
<td>565</td>
<td>300</td>
<td>19 252</td>
</tr>
</tbody>
</table>

**TABLE XXI - Budget 1994 (kFF, excluding VAT)**

4% RESEARCH
22% EXCEPTIONAL
74% CONTRACTS

**Figure 33 - Budget 1994**
<table>
<thead>
<tr>
<th>Project Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC/EUROCHIP</td>
<td>4,258</td>
</tr>
<tr>
<td>CEC/NSF - CLC</td>
<td>325</td>
</tr>
<tr>
<td>CEC/NSF - NDIMST</td>
<td>119</td>
</tr>
<tr>
<td>CEC/COPERNICUS 93 n°9093</td>
<td>97</td>
</tr>
<tr>
<td>CEC/ARCHIMEDES</td>
<td>915</td>
</tr>
<tr>
<td>CEC/HCM - GARDEN</td>
<td>137</td>
</tr>
<tr>
<td>CEC/CHIPSHOP</td>
<td>743</td>
</tr>
<tr>
<td>CEC/EEMCN</td>
<td>73</td>
</tr>
<tr>
<td>CEC/EDAC-EUROASIC 93-94</td>
<td>99</td>
</tr>
<tr>
<td>MIPTCE/JESSI AC 6</td>
<td>880</td>
</tr>
<tr>
<td>MIPTCE/JESSI AC 8</td>
<td>1,860</td>
</tr>
<tr>
<td>MIPTCE/JESSI AE 11</td>
<td>414</td>
</tr>
<tr>
<td>SGS-THOMSON/JESSI AC8</td>
<td>801</td>
</tr>
<tr>
<td>CNET/SOLIST</td>
<td>350</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>11,071</strong></td>
</tr>
</tbody>
</table>

**TABLE XX - Contracts signed in 1993 (kFF, excluding VAT)**
<table>
<thead>
<tr>
<th>Organisation</th>
<th>Amount (kFF, excl. VAT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEC / EUROCHIP</td>
<td>3866</td>
</tr>
<tr>
<td>CEC / BARMINT</td>
<td>799</td>
</tr>
<tr>
<td>CEC / COPERNICUS THERMINIC</td>
<td>565</td>
</tr>
<tr>
<td>CEC / COPERNICUS FUTEG</td>
<td>299</td>
</tr>
<tr>
<td>CEC / AMATIST</td>
<td>1092</td>
</tr>
<tr>
<td>CEC / GRASS</td>
<td>142</td>
</tr>
<tr>
<td>CEC / CHIPSHOP</td>
<td>701</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC 6</td>
<td>1103</td>
</tr>
<tr>
<td>MIPTCE / JESSI AC 8</td>
<td>2887</td>
</tr>
<tr>
<td>MIPTCE / JESSI AE 11</td>
<td>526</td>
</tr>
<tr>
<td>SGS-THOMSON / AMICAL</td>
<td>570</td>
</tr>
<tr>
<td>SGS-THOMSON / CIFRE</td>
<td>90</td>
</tr>
<tr>
<td>CNET / PSYCOS</td>
<td>1200</td>
</tr>
<tr>
<td>AEROSPIALETTE</td>
<td>300</td>
</tr>
<tr>
<td>DET / ASTER INGENIERIE</td>
<td>156</td>
</tr>
</tbody>
</table>

**Total**: 14296

**TABLE XXII - Contracts signed in 1994 (kFF, excluding VAT)**
If we consider 1989, 1990, 1991, 1992, 1993, 1994 together, then we get the global data given in Table XXIII and represented by Figure 34. Such data are more representative of the reality. Now, we get a part of the contracts which is 62% of the budget, and the CEC part is 60%. JESSI accounts for 24%, but JESSI activities are reported from 1991 only.

![Pie chart showing budget distribution](image)

**Figure 34 - Budget 1989 - 1994**

<table>
<thead>
<tr>
<th>Type</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research funds</td>
<td>2 612</td>
</tr>
<tr>
<td>Exceptional funds</td>
<td>14 295</td>
</tr>
<tr>
<td>Exceptional invoices</td>
<td>11 875</td>
</tr>
<tr>
<td>Contracts</td>
<td>47 013</td>
</tr>
</tbody>
</table>

**TABLE XXIII - Budget 1989-1994 (kFF, excluding VAT)**
V - COOPERATIVE ACTIVITIES

V-1 Contracts

Public Institutions:

MAE, MESR (CNFM), MIPTCE (SERICS), France Telecom (CNET).

Industrial contracts:

SGS THOMSON, HEWLETT PACKARD, AEROSPATIALE, ASTER.

V-2 European Projects

V-2.1 Summary

In the past, members of the Laboratory participated to CEC Projects like CASCADE and CVT. Presently, or recently, the Laboratory participates or has been participating to the following projects:

ESPRIT PROJECTS:

ESPRIT I : ADVICE, AIDA, SPAN
ESPRIT II BASIC RESEARCH : ASCIS, EUROCHIP
ESPRIT III BASIC RESEARCH : ARCHIMEDES, FASED, BARMINT, AMATIST, GRASS
ESPRIT III RESEARCH AND DEVELOPMENT : CHIPSHOP

CEC/NSF Cooperation : NDI MST, CSLS

JESSI PROJECTS:

JESSI : AC6, AE11, AC8

COMETT PROJECTS:

COMETT I : COMET
COMETT II : EUROSYSTEMS, EPIQCS

EUREKA PROJECT:

EUREKA : MITHRA
TEMPUS PROJECTS:

TEMPUS
- Advanced JEP for Microelectronics Design Methodology,
- MECC,
- Initiation of Formal Training in CAEE in Romanian Universities,
- Computer-aided Methods and Technical Management in Electrical Engineering Education
- Digital System Design Based on PLD-Technology

COPERNICUS (PECO) PROJECTS:

COPERNICUS (ex PECO)
- EDAC-EAST: Attendance of Central and Eastern European Engineers and Researchers to the EDAC Conference
- Design of VLSI self-checking digital circuits
- Developing design automation technique in ASIC and VLSI Design
- CAD/CAT tools integration for sensor-based microsystems
- Dependability Analysis of Complex Electronic Components and Systems
- East European Microelectronics Cooperation Network of support and competence centres of Central and Eastern European countries
- Functional test generation and diagnosis
- EUROEAST: Extension of EUROCHIP services to Central and Eastern European Countries
- THERMINIC: New Methods for Thermal Investigation of Integrated Circuits

HUMAN CAPITAL MOBILITY PROJECT:

HCM
- GARDEN

INTERNATIONAL ASSOCIATION FOR THE PROMOTION OF COOPERATION WITH SCIENTISTS FROM THE INDEPENDENT STATES OF THE FORMER SOVIET UNION (INTAS):

INTAS
- Network to support high level systems design research

V-2.2 Details

ESPRIT-I

ADVICE
(CSELT, British Telecom, CNET, TIMA/INPG, Trinity College), 1984–1989 (ADVICE I)

Automatic Design Validation of Integrated Circuits using Electron Beam

Currently, the e-beam probe is the only viable method for obtaining timing resolution and voltage information from the internal nodes of single and multilevel VLSI circuits. However, the systems available at present are essentially manually operated and the
procedure for fault diagnosis can be extremely time consuming. By making use of CAD software, the ADVICE project will enable the diagnostic investigation to be automated, thereby significantly reducing the circuit development time.

The Laboratory is mainly involved in CAD-EBT interface, controllability using e-beam and diagnostic tools.

AIDA

(SIEMENS, ICL, SGS THOMSON, TIMA/INPG, University of Manchester), 1986-1990

Advanced Integrated-circuit Design Aids

The objective of the project is to master the complexity of VLSI chips (more than one million transistors within the next few years) by obtaining a drastic improvement in design methods. CAD tools, new methods and concepts will be defined, proved on experimental software and finally developed into industrial tools integrated into the existing CAD environments of the partners. AIDA intends to explore the application of modern programming techniques and knowledge-base engineering to CAD tool development. It will constitute a design assistant that proposes solutions rather than merely records and validates the designer's ideas. This will allow the designer to apply his creativity where it is most efficient, leading to improved design quality. Modern programming techniques will be applied (e.g. those developed for expert systems to VLSI-CAD tools).

More specifically, the Laboratory is in charge of exploring the design of structured control-sections and/or structured data paths in order to make them self-checking and give them built-in testability.

SPAN

(THORM-EMI, CIMSA-SINTRA, CTI, INESC, PCS, TIMA/INPG, University College London), 1987-1990

Parallel Computer Systems for Integrated Numeric and Symbolic Processing

The objective of the Project is to investigate programming languages and parallel architectures for the integration of symbolic and numeric processing, and to develop a common virtual machine. The project is organized in distinct layers: application software packages, high level languages and tools, the "virtual machine" kernel system, and parallel architectures.

The Laboratory is specifically involved in the architecture of a Prolog system, integrating numeric processing.

At the time of writing this report, proposals are being submitted to the ESPRIT II Programme, mainly on fault-tolerant, real time, embedded architectures.
ESPRIT-II Basic Research

ASCIS

Architecture Synthesis for Complex Integrated Systems

The research in ASCIS is aimed at addressing future ICs which will contain the equivalent in logic of 16 million memory cells. Currently complex systems are mapped into Silicon starting from an architectural description level. However, the bottle-neck in such mega-chip designs lies not in realizing the layout from this register-transfer level description, but in mapping the behaviour intended into a suitable architecture. Therefore, in order to fully exploit the integration complexity of future fabrication technologies it is crucial to provide a specification at the highest system level.

Problems related to this change of specification level are fundamental in nature.

The topics to be addressed are the system definition, the system partitioning, the mapping of subsystems into architectures, and the architectural synthesis of control sections.

The Laboratory will focus on behavioral partitioning, architectural exploration and cooperative datapaths.

EUROCHIP

(GMD, CMP, IMEC, University of Lyngby, RAL), 1989-1994

Service organisation of the VLSI Design Action

This service will provide European Universities with a number of services including access to chip manufacture and procurement of additional workstations, test equipment and CAD software.

CMP is a member of the Service Organisation.

ESPRIT-III Basic Research

ARCHIMEDES

(INPG/TIMA, Univ. of Karlsruhe, Montpellier, Hannover, Bologna, Barcelona, & INESC), 1992-1995

ARCHIitectural MEthodologies for aDvanced testing of VLSI Systems.

This project takes place in the framework of: “Algorithms for design methodologies for complex circuits and digital optical systems” (area V - Basic Research).

The objective is to develop methodologies in order that the advances allowed by the technology and the use of powerfull CAD tools will not be jeopardized by the testing bottleneck.

The project goes deeper in the research by considering:
- architectural synthesis
- on-line and off-line testing together
- built-in test of analog parts
- defect modeling, from process simulation to circuit simulation
- IC defects-based back annotation of circuit faults
- combined detection techniques (voltage and current testing)
- IC defects-based fault models for analogue building blocks
- advanced fault simulation of CMOS compatible designs (BiCMOS)
- optimized built-in test generation for BIST
- automatic design rule checking for self-checking circuits.

FASED

(IMS, INPG/TIMA, Politecnico di Milano)
1992-1994

Failsafe Integrated Digital Electronics with Semicustoms

Electronic components are increasingly being employed in safety critical systems. The introduction of application specific VLSI circuits to these areas is hampered by long design times and consequently high cost of self-checking and fail-safe integrated circuits. In this proposed basic research action, these issues are to be addressed by extending the use of semicustom technologies to fail-safe circuits.

BARMINT

(LAAS Toulouse, INPG/TIMA, INPG/TIMC, TH Darmstadt, TU Budapest, CNM Bellaterra, LCMM Barcelona, NMRC Cork, TU Lodz)
1994-1997

Basic Research for Microsystems INTegration

Microsystems that integrate data processing along with sensors and actuators will face an important development during the next years. The objective of the BARMINT project is to participate to the development of microsystems along three main axes: a) the tools for top-down design that bring methods for developing microsystems in a way similar to present ASICs, b) the technological compatibilities between silicon based VLSI, micromachined silicon in micromechanics, integrated optics obtained by micromachining of silicon or of special polymers, and chemical sensors with membranes, c) the assembly operations that focus on typical compatibility problems for including various components within a single multichip microsystem.

AMATIST

(CNM Sevilla, MESA Institute - Univ. of Twente, INPG/TIMA, Univ. of Cantabria, Univ. of Lancaster, Univ. of Pavia)
1994-1997

Analogue & Mixed-signal Advanced Test for Improving System-level Testability

This project intends to develop new concepts enabling to improve the performance of mixed-signal integrated systems through the incorporation of on-line test functionality. This will be carried out by addressing three different issues: a) the introduction of circuit architectures which can be used to ensure a continuous signal monitoring during the system field operation, b) the development of Design-For-Testability and off-line test generation methods especially tailored to the systems under study, and c) the validation of the new architectures and methods by using them to implement actual integrated applications.
GRASS (Working Group)

(Univ. de Las Palmas de Gran Canarias, INPG/TIMA, Middlesex University, Techn. Univ. of Denmark, EPFL, Fraunhofer-Gesellschaft Erlangen)
1994-1997

Gallium arsenide Research action on ASIC Synthesis

The emerging commercial markets in the communication, computer, automotive and broadcast industries will produce an increase of more than 30% every year in both the digital and analogue GaAs device markets. The aim of this project is to improve the knowledge of European researchers on mixed mode Gallium Arsenide VLSI integrated circuit design, and to generate facilities for allowing the reliable design of such circuits. Effort is targeted for fast digital signal processing and other very high speed applications such as broadband telecommunications, hardware accelerators and workstations. It aims at delivering a design environment with the same level of performance in quality and design time for GaAs as is available for silicon to ASIC designers in Telecom and Information Processing fields.

ESPRIT-III Research and Development

CHIPSHOP

(SCME, FhG-IIS, LETI, CMP, CNR-PF, IAM, GAME, INESC, INTRACOM, ElektronikCentralen, CNM, Nordic VLSI, ERA, ULVC)
1992-1994

A low-cost IC prototyping production service for small and medium sized enterprises.

CHIPSHOP is a pan-European initiative supported by the Commission of the European Communities in the framework of the ESPRIT programme to provide MPW services to SMEs from EC and EFTA countries, in connection with the JESSI-SMI Project and with Special Actions in Greece, Portugal, Italy and Spain. Chip fabrication is carried out by 5 different foundries and testing interfaces : CMP in France, Fraunhofer-Institute for Integrated Circuits (FhG-IIS) in Erlangen in Germany, CNM in Spain, Nordic VLSI in Norway, ElektronikCentralen in Denmark and CSATA in Italy. CMOS and BiCMOS technologies will be offered to support analog, digital, mixed, high voltage and high frequency applications. CHIPSHOP offers more services besides prototype fabrication : testing, small volume production, CAD software, FPGA migration.

CEC/NSF Cooperation

NDIMST

(University of Texas at Austin, INPG/TIMA)
1993-1995

New Directions In Mixed Signal Test

The objective of the proposed cooperation is to find new approaches to deriving high quality tests for mixed-signal circuits. Much of the work in test has been focused on
digital circuits. With the increasing levels of integration, and applications such as automotive, notebook computers, and communications, analog and digital functions are being integrated on a single chip. Appropriate fault models and efficient test generation algorithms need to be generated for mixed-signal circuits if we are to produce defect-free chips, and on-line detection.

CSLS

(University of California at Irvine, INPG/TIMA)
1994

Circuit and System-Level Synthesis

The goal of this cooperation is to develop a global solution for behavioral and System-Level Synthesis. This cooperation will be based on the integration of SpecChart, the system-level synthesis tool developed at Irvine, and AMICAL, the behavioral synthesis tool developed at Grenoble. This integration will produce a unified synthesis environment for circuit and system design.

JESSI


Industrial partners:
- Philips, Eindhoven/Hamburg
- Siemens, Munich
- SNL, Munich
- EZM, Villach
- SGS Thomson, Grenoble
- Thomson-CSF/TMS
- Alcatel/Bell, Antwerp

Associated partners:
- University of Karlsruhe together with "Forschungszentrum-Informatik" in Karlsruhe
- University of Hannover
- Technical University of München
- University of Erlangen-Nürnberg
- TIMA/INPG
- Twente University of Technology, Enschede, The Netherlands
- Bennetts Associates, Southampton.


Industrial partners:
- Bosch, Reutlingen
- SGS-Thomson, Grenoble
- Siemens, München
- SEL-Alcatel, Stuttgart
- Porsche, Weinach
Associated partners:
University of Hannover
TIMA/INPG

AC8 : Integrating AMICAL within industrial CAD environment, 1993-1994

Industrial partners:
AHL
Bosch
Bull
Philips
Siemens
Siemens-Nixdorf
SGS-Thomson
Synthesia
Thomson-TCS

Associated partners:
TIMA/INPG

COMETT I

COMET

(IMEC, TIMA/INPG, Universities of Darmstadt, Limerick, Lyngby, Madrid), 1988-1990

Consortium for microelectronic training

This project is aimed at providing education on ASICs at several levels and for several interest groups, but especially for the SMIs in each country.

COMETT II

EUROSYSTEMS

(University of Darmstadt, IMEC, University of Lyngby, TIMA/INPG).

This project is a complete programme for advanced microelectronics system design fullfilling the future trends of European industry.

EPIQCS : MASTERS DEGREE SPECIALIZED IN QUALITY OF COMPLEX INTEGRATED SYSTEMS

(INPG, Imperial College of London, Universities of Darmstadt and Eindhoven)

This project aims at providing a Masters Degree in cooperation with 3 main academic partners and numerous industrial partners. The 4 platforms will be specialized in Software, Telecom, Hardware and Space.
EUREKA

MITHRA

(BROSSARD, BERTIN, ITMI, SEIV, LAMM, ELKRON, OLMAT, SEPA, EPFL, CERBERUS, TIMA/INPG) 1988-1990

MITHRA deals with integrated electronics for surveillance mobile robots. It is a project in which industrial firms from France, Italy and Switzerland are participating. Several research laboratories from INPG and LAMM at Montpellier are also participating. The experience of the Laboratory might be used to design circuits to replace several printed circuits boards.

TEMPUS

ADVANCED JOINT EUROPEAN PROGRAMME FOR MICROELECTRONICS DESIGN METHODOLOGY

(University of Darmstadt, Technical University of Budapest, IMEC, University of Lyngby, TIMA/INPG, Institute of Electron Technology of Warsaw)

This is a transeuropean programme on microelectronics.

MECC (Management, Electronics, Computer science)


This is a transeuropean programme on management, electronics, computer science.

INITIATION OF FORMAL TRAINING IN COMPUTER-AIDED ELECTRICAL ENGINEERING IN ROMANIAN UNIVERSITIES

(TIMA/INPG, ENSIEG/INPG, Univ. of Bucuresti, Bath, Genova, Cassino, Paris 6 & 11, Graz, EDF, Politecnico di Torino)

This is a transeuropean programme for the development of education capabilities at higher education level in applied sciences in engineering areas.

COMPUTER-AIDED METHODS AND TECHNICAL MANAGEMENT IN ELECTRICAL ENGINEERING EDUCATION

(Technical Univ. Budapest, Univ. Karlsruhe, Univ. Erlangen-Nürnberg, University College London, TIMA/INPG, Univ. of Pisa, Techn. Univ. of Delft, MOTOROLA GmbH, TEXAS
INSTRUMENTS DEUTSCHLAND, HEWLETT PACKARD, DIGITAL EQUIPMENT, IBM)

This is a transeuopean programme for updating technical and technical-management studies.

DIGITAL SYSTEM DESIGN BASED ON PLD-TECHNOLOGY

(Technische Hochschule Darmstadt, TIMA/INPG, Tallinn Technical Univ.)

This is a transeuopean programme for introducing into university education the methodology and concepts of designing semicustom ASICs.

COPERNICUS

COPERNICUS: Cooperation in science and technology with Central and Eastern European countries.

European Conferences, workshops and training seminars:

EDAC-EAST: ATTENDANCE OF CENTRAL AND EASTERN EUROPEAN ENGINEERS AND RESEARCHERS TO THE EDAC CONFERENCE

Mobility scheme for scientists:

DESIGN OF VLSI SELF-CHECKING DIGITAL CIRCUITS
(Stanislaw PIESTRAK, Technical University Wroclaw, Poland)

DEVELOPING DESIGN AUTOMATION TECHNIQUE IN ASIC AND VLSI DESIGN
(Tania VASSILEVA, Technical University Sofia, Bulgaria)

CAD/CAT TOOLS INTEGRATION FOR SENSOR-BASED MICROSYSTEMS
(Teodor CALIN, Polytechnical Institute of Bucharest, Romania)

DEPENDABILITY ANALYSIS OF COMPLEX ELECTRONIC COMPONENTS AND SYSTEMS
(Ioan BACIVAROV, Polytechnical Institute of Bucharest, Romania)

Pan European Scientific Networks:

EAST EUROPEAN MICROELECTRONICS COOPERATION NETWORK OF SUPPORT AND COMPETENCE CENTRES OF CENTRAL AND EASTERN EUROPEAN COUNTRIES

Joint Research Proposals:

FUNCTIONAL TEST GENERATION AND DIAGNOSIS (FUTEG)

(Technical University of Tallinn - Estonia, Kannas University of Technology - Lituania, Institute of Computer Systems Bratislava, Technical University of Budapest, INPG/TIMA, FlhG-IIS-EAS Dresden)

1994-1997

The focus of the project is directed towards the investigation of functional and behavioral test generation and diagnosis at the system level. The different partners will put in common their expertise in this area, in order to provide different approaches to this topic. These approaches will be validated by experiments and comparatively analyzed. Finally, their integration into a combined methodology is intended. This project, which manpower is 25 persons-year, over a duration of 36 months, is expected to start in January 1994.

EUROEAST: EXTENSION OF EURCHIP SERVICES TO CENTRAL AND EASTERN EUROPEAN COUNTRIES

(GMD, CMP, DTH, IMEC, RAL, Polytechn. Bucharest, ITME Warsaw, Warsaw University, Silesian Tech. Univ., Slovak Tech. Univ.)

NEW METHODS FOR THERMAL INVESTIGATION OF INTEGRATED CIRCUITS (THERMINIC)

(Technical University of Budapest, Hungary, Technical University of Lodz, Poland, Technical University of Lviv, Ukraine, SEMILAB Budapest, Hungary, INPG/TIMA)

1995-1997

One of the greatest challenges of our days in microelectronics are the overheating problems. The increase in the power density in integrated circuits, caused by the actual small features sizes, moreover the advent of 3D packages cause severe heat dissipation problems. This project intends to treat this problem in its complexity and approximate it in different ways, resulting in the development of new thermal monitoring methods and elements as well as new thermal investigation methods and tools.

HUMAN CAPITAL AND MOBILITY

GARDEN

(Uinv. de Las Palmas de Gran Canarias, INPG/TIMA, PHILIPS Electr. Laboratories, Middlesex University, Techn. Univ. of Denmark, EIDG, Technische Hochschule at Zurich, Fraunhofer Institut für Angewandte Festkörperphysik at Freiburg, Fraunhofer Institut für Integrierte Schaltungen at Erlangen, GIGA at Brondby, Thomson CSF)

Gallium Arsenide Reliable Design ENvironment

This project aims at delivering a design environment with the same level of performance in quality and design time for GaAs as available for silicon, to ASIC designers in Telecom and Information Processing fields. This goal will be achieved by
two actions. Firstly, a research and cooperation network: "The European Network on Gallium Arsenide VLSI Design", will be established within the Human Capital and Mobility Programme of the European Community. Secondly, a research and development project will be launched again through the Human Capital and Mobility Programme, which will center cooperation between laboratories in the network and will provide mobility for advanced research and training at each other sites according to special capabilities and expertise.

INTERNATIONAL ASSOCIATION FOR THE PROMOTION OF COOPERATION WITH SCIENTISTS FROM THE INDEPENDENT STATES OF THE FORMER SOVIET UNION (INTAS)

INTAS

(NEuW Limited, Oldham, UK ; Academy of Science of Russia, Institute of Information Problems, Moscow, Russia ; Polytechnical Institute of Kharkov, Ukraine ; Institute of Opetaining System, Moscow, Russia ; Academy of Sciences of Belarus, Inst. of Engineering Cybernetics, Minsk, Republic of Belarus ; St Petersburg Electrical Engineering Institute, Russia ; Information System Research Institute of Russia, Moscow, Russia ; Technical University of Tallinn, Estonia ; NICEVT Science & Research Centre on Computer Technology, Moscow, Russia ; Cialab, Paderborn, Germany ; INPG/TIMA ; Eindhoven University of Technology, Faculty of Electrical Engineering, Eindhoven, The Netherlands ; Univ. of Manchester, UK ; Univ. of Newcastle Upon Tyne UK ; National Microelectronics Research Centre, University College, Cork, Ireland ; BULL SA, France ; ESIM, Marseille, France ; GMD, St Austenin, Germany ; University of Cantabria, Santander, Spain).

1994-1996

Network to support high level systems design research

This is a network that will promote communication and advancement in research of Electronics Systems Design. This project will also sustain the key systems design research groups currently active in the New Independent States (NIS). Contact has already been established with the groups in the NIS and networking is ready to start. Through partnership with the leading systems design research Institutes in Europe, we will create a communication network that enables open and free exchange of the most advanced research ideas and experiences. Communications will be enhanced by placing NIS researchers in European Institutes to take part in research of common interest to the groups. The relationships established will further enhance the operation of the network. An annual 50 men Workshop will be held to share the research results and experiences of members of the network. Funding will be provided to the NIS research groups to ensure their continued activity in this research area. Combining the expertise available in Europe with the NIS groups preeminence in discovering new algorithms and analytical approaches to high level systems design will generate important and valuable new results.

V-3 Cooperation agreements

The Laboratory is engaged in a number of cooperations, some of them being officially recognized. They are listed below. These cooperations allow to remote researchers at the cooperative location for in-deep fruitful exchanges of results, to organize joint research and Workshops.
University of Texas at Austin, USA
This cooperation takes place in the framework of a project between NSF and ESPRIT with J. ABRAHAM on testing of integrated circuits, with a special emphasis on analog and mixed circuits.

University of California at Irvine, USA
This cooperation takes place in the framework of a project between NSF and ESPRIT with D. GAJSKI, on statecharts and AMICAL relationships.

Ecole Polytechnique de Montréal, Canada
This cooperation takes place in the framework of a project sponsored by FCAR/GRIAO, with B. KAMINSKA, on testing of integrated circuits, with a special emphasis on analog circuits.

Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with R. REIS, on the automatic design of integrated circuits.

Universidade Federal do Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil
This cooperation takes place in the framework of a project sponsored by CAPES/COFECUB, with A. MESQUITA, on high level synthesis and test of integrated circuits.

University of Washington at Seattle, USA
This cooperation takes place in the framework of the definition of the P1149.4 IEEE standard for the analog extension of the P1149.1 boundary scan, with M. SOMA who is chairing the working group. The Laboratory is the European center of the distribution of documents (with École Polytechnique Fédérale de Lausanne for Switzerland).

Ecole Nationale d'Ingénieurs de Monastir (ENIM), Monastir, Tunisia
This cooperation takes place in the framework of a project sponsored by the French ministry for education and research and the Tunisian ministry for research and technology, cooperation program which name is "Réseaux Formation-Recherche franco-tunisiens", with S. NASRI, on computer-aided design of communication-dedicated circuits.

Technical University of Budapest, Hungary
This cooperation takes place in the framework of BALATON, between France and Hungary. The project deals with thermal investigations of ICs and systems, with the Department of Electron Devices: V. SZEKELEY and M. RENCZ.

Jozef Stefan Institute, Ljubljana, Slovenia
This cooperation takes place in the framework of PROTEUS, between France and Slovenia. The project deals with test and diagnostic of heterogeneous systems, with F. NOVAK.

Tomsk State University, Russia
This cooperation takes place in the framework of NATO linkage grants. Those grants allow short stays in NATO countries for foreign researchers.

V-4 International activities

This section gives an overview of national and international activities to which participated recently the members of the Laboratory.
Participation to Committees for Conferences and Workshops

- Built-in Self-Test workshop: 1984-1993 (Charleston)
- European Design for Testability Workshop: 1990 (Segovia), 1992 (Brugge)
- ICCAD: 1991-1993 (Santa Clara), 1994 (San Jose), 1995 (Santa Clara)
- European Solid-State Circuits Conference: 1986 (Delft), 1990 (Grenoble)
- International Conference on Microelectronics: 1991 (Cairo), 1992 (Monastir), 1993 (Dahran)
- International Workshop on FPGAs and Applications: 1992 (Vienna), 1994 (Prague)
- Workshop France-Brazil: 1992 (Paris)
- European workshop on Dependable Computing: 1989 (Toulouse)
- Rapid System Prototyping workshop: 1990-1993 (Raleigh), 1994 (Grenoble)
- CEC CAVE (CAD for VLSI in Europe) workshops: 1983-1988
- Memory Testing: 1993-1994 (San Jose)
- Asian Test Symposium: 1992 (Hiroshima), 1993 (Beijing), 1994 (Osaka), 1995 (Bangalore)
- High Level Synthesis Workshop: 1994 (Niagara Falls), 1995 (Cannes)
- EuroDAC-EuroVHDL: 1994 (Grenoble)
- Workshop on Hardware-Software Codesign: 1994 (Grenoble)
- Simulation in Electronics: 1994 (Santander)
- Asia Pacific Conference on Hardware Description Languages: 1993 (Brisbane), 1994 (Toyohashi), 1996 (Bangalore)
- International Conference on Probabilistic Safety Assessment and Management: 1991 (Beverly Hills), 1996 (Greece)
- European Safety and Reliability Conference: 1996 (Greece)
- 2nd International Conference on ASIC: 1996 (Shanghai)
- IEEE Multi-Chip Module Conference: 1995 - 1996 (Santa Cruz)

Participation to Editorial Boards of Journals

- CDTA
- IEEE Transactions on VLSI Systems
- Journal of Microelectronic Systems Integration
- IEEE Design and Test of Computers Magazine
- Quality Engineering Journal
- Reliability Engineering & System Safety
- Quality Observer
Organisation of Conferences

- Electron and Optical Beam Testing of Integrated Circuits: 1987 (Grenoble, General Chair),
  1989 (Duisburg, Program Chair), 1991 (Como, Program Chair), 1993 (Zurich, Program Chair),
  1995 (Wuppertal, Program Chair)
- EUROCHIP Workshop on VLSI Design Training (General Chair): 1991-1992 (Grenoble), 1993
  (Toledo), 1994 (Dresden)
- European Conference on Design Automation / EUROASIC: 1993 (Paris, General Chair)
- European Conference on Design Automation / European Test Conference / EUROASIC: 1994
  (Paris, Program Co-Chair)
- Rapid System Prototyping Workshop: 1994 (Grenoble, General Chair)
- International Symposium on System Synthesis: 1995 (Cannes, Program Chair)
- IEEE Mixed-Signal Test Workshop: 1995 (Grenoble, General Chair)
- IEEE Workshop on On-Line Testing: 1995 (Nice, General Chair)
- Workshop on Thermal Investigations in ICs and Systems: 1995 (Grenoble, General Chair)

Participation to Societies and Working Groups

- Member of IEEE European Test Technology Technical Committee
- Vice-Chair of Technical Activities of the IEEE Test Technology Technical Committee
- Chairman of the European Design and Automation Association

Others activities

- Review of papers for numerous Journals and Conferences
- Review of research proposals for CEC, NSF, NATO, SERC

V-5 Awards and distinctions

- IEEE Meritorious Service Awards (1993)
- Doctor Honoris Causa of the Technical University of Budapest (1994).
Picture 2:
Bernard COURTOIS is being awarded Doctor Honoris Causa of the Technical University of Budapest
VI - TECHNOLOGY TRANSFER ACTIVITIES

Besides their research and service activities, TIMA staff members are also concerned with technology transfer activities. For that purpose, they are regularly solicited to serve as consultant for technical and educational tasks, mainly by industrial companies, but also by foreign universities. Some results of these tasks have already been evoked throughout this report for the sake of consistency of the different sections, others only appear in this section. Up to now, the transfer technology activities have taken the following forms:

VI-1 Technical tasks

VI-1.1 Industrial Transfers

- Standard Mirror Board (SMB) developments, resulting from the research work made within the ADELAIDE project have been transferred to the IMD French company, which is introducing them now on the market. Details can be found in section II of this report, description of the Quality of Complex System Group.

- The AMICAL architectural synthesis system is currently under industrial transfer process: several companies have expressed their interest. Details are given in section II of the report, description of the System Level Synthesis Group.

VI-1.2 Patents

The following patents have recently been taken:

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transparent Testing of Integrated Circuits</td>
<td>M. Nicolaidis</td>
<td>03/92</td>
</tr>
<tr>
<td>Implementation Techniques of Self-Checking Arithmetic Operators and Data Paths based on Double-Rail and Parity Codes</td>
<td>M. Nicolaidis</td>
<td>04/92</td>
</tr>
<tr>
<td>Standard Mirror Board (FR 92/12549)</td>
<td>L. Balme</td>
<td>12/92</td>
</tr>
<tr>
<td>Standard Mirror Board (FR 93/09571)</td>
<td>L. Balme</td>
<td>09/93</td>
</tr>
<tr>
<td>SEU Tolerant RAM</td>
<td>F. L. Vargas &amp; M. Nicolaidis</td>
<td>06/94</td>
</tr>
</tbody>
</table>

VI-1.3 Industrial Circuit Fabrication

In addition to its service activity for university and research laboratory circuit fabrication, CMP is offering circuit fabrication services for industrial circuit prototyping and low volume production. Starting from 1993, more than 100 industrial prototype circuits have been fabricated, in CMOS, BICMOS, and GaAs technologies, for 25 companies and 10 universities/research laboratories. Several small volume production (10-200 pieces) and two low volume productions (3000 and 1400 pieces) have been concluded. Prices are negotiated directly by CMP with the manufacturer, depending on each request.
VI-1.4 Consulting

The following consulting tasks have recently been achieved:

<table>
<thead>
<tr>
<th>Company</th>
<th>TIMA member</th>
<th>Duration</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMS (Austria)</td>
<td>K. Torki</td>
<td>8 months</td>
<td>91-93</td>
</tr>
<tr>
<td>IN2P3/LAL (France)</td>
<td>K. Torki</td>
<td>5 days</td>
<td>04/92</td>
</tr>
<tr>
<td>Alcatel/Alstom (France)</td>
<td>M. Nicolaïdis</td>
<td>2 days</td>
<td>07/94</td>
</tr>
</tbody>
</table>

VI-2 Educational Tasks

Dealing with problems risen by advanced technologies, and proposing advanced design and test methodologies, TIMA staff members are, as a matter of course, very concerned in growing public awareness of these topics. Continuing education is the principal form of advanced knowledge dissemination achieved by the laboratory, and many teaching sessions have been given to industry (engineers) and academy (teachers and post-graduate students) people. These activities are classified in the sequel into five categories: course organization, seminars, support of - or participation in - foreign university teaching programs, participation in EU educational and technology transfer programs, and finally direction of Ph.D. students employed by French industrial companies (CIFRE program).

VI-2.1 Courses Organization

The following table lists courses that have been organized by members of the laboratory, at different institution request. The course detailed program and duration are established by the organizer, given the requested subject and the audience profile. If needed, additional speakers are solicited, either among TIMA staff or externally.

<table>
<thead>
<tr>
<th>Request. Inst.</th>
<th>Location</th>
<th>Date</th>
<th>Dur.</th>
<th>Organizer</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT</td>
<td>Paris</td>
<td>02/92</td>
<td>2 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>HP</td>
<td>Grenoble</td>
<td>06/92</td>
<td>1 day</td>
<td>M. Marzouki</td>
<td>Board Testing</td>
</tr>
<tr>
<td>MFQ</td>
<td>Paris</td>
<td>12/92</td>
<td>3 days</td>
<td>M. Marzouki</td>
<td>System Test and Testability</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Grenoble</td>
<td>12/92</td>
<td>5 days</td>
<td>A. Guyot</td>
<td>ASIC Testing</td>
</tr>
<tr>
<td>--</td>
<td>Grenoble</td>
<td>06/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>--</td>
<td>Tokyo</td>
<td>10/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>--</td>
<td>Singapore</td>
<td>12/93</td>
<td>1 day</td>
<td>A. A. Jerraya</td>
<td>Architectural Synthesis &amp; AMICAL</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Grenoble</td>
<td>04/94</td>
<td>2 days</td>
<td>A. A. Jerraya</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/Chipshop</td>
<td>Irvine-CA</td>
<td>11/94</td>
<td>2 days</td>
<td>M. Lubaszewski</td>
<td>VLSI Design on PC platforms</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Irvine-CA</td>
<td>12/94</td>
<td>2 days</td>
<td>M. Lubaszewski</td>
<td>Amical/SpecCharts-SpecSyn Systems</td>
</tr>
<tr>
<td>CEC/NSF</td>
<td>Austin</td>
<td>11/95</td>
<td>2 days</td>
<td>A. Jerraya</td>
<td>Mixed-Signal Testing</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/94</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
<tr>
<td>CEC/Eurochip</td>
<td>Leuven</td>
<td>09/95</td>
<td>5 days</td>
<td>A. Jerraya</td>
<td>High-Level Design</td>
</tr>
</tbody>
</table>
Picture 3: AMICAL seminar in Tokyo, October 1993
VI-2.2 Courses and Seminars

Advanced courses and seminars are a practical way of sensitizing graduate students to state-of-the-art problems and research subjects. The attendance is also often composed by young and senior researchers who want to exchange ideas and views on specific problems of their own field or some related research domains.

In addition to internal seminars, the laboratory regularly invites people from Grenoble academic and industrial environment to attend the talks given by our visiting researchers. These people have recently had the opportunity to listen to the following speakers:

<table>
<thead>
<tr>
<th>Speaker</th>
<th>Institution</th>
<th>Date</th>
<th>Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. A.J. Van de Goor</td>
<td>Delft U. of Technology</td>
<td>07/92</td>
<td>Test for SRAMs and FIFOs</td>
</tr>
<tr>
<td>Prof. J. A. Goor</td>
<td>Delft U. of Technology</td>
<td>07/92</td>
<td>Tests for neighborhood pattern sensitive faults</td>
</tr>
<tr>
<td>Dr. G. Venkatesh</td>
<td>ASIC Technologies, Bangalore</td>
<td>09/92</td>
<td>HLS of Asynchronous Speed Independent Controllers</td>
</tr>
<tr>
<td>Prof. D. Kinniment</td>
<td>U. Newcastle Upon Tyne</td>
<td>11/92</td>
<td>Correct Interactive Transformational Synthesis of DSP Hardware</td>
</tr>
<tr>
<td>Prof. F. Kurdahi</td>
<td>U. California, Irvine</td>
<td>03/93</td>
<td>Architectural Synthesis of DSP Systems</td>
</tr>
<tr>
<td>Prof. M. Soma</td>
<td>U. Washington, Seattle</td>
<td>04/93</td>
<td>Mixed-Signal Testing and DFT</td>
</tr>
<tr>
<td>Prof. A. Ivanov</td>
<td>U. British Columbia, Vancouver</td>
<td>06/93</td>
<td>BIST Compaction Schemes based on Multiple Signature Checking</td>
</tr>
<tr>
<td>Prof. J. A. Abraham</td>
<td>U. Texas, Austin</td>
<td>06/93</td>
<td>Testing of Analog Circuits</td>
</tr>
<tr>
<td>Prof. E. Aas</td>
<td>The Norwegian Inst. of Technology</td>
<td>07/93</td>
<td>Probabilistic Model of Design Quality</td>
</tr>
<tr>
<td>Mr. J. O’Leary</td>
<td>Cornell U., Ithaca, NY</td>
<td>11/93</td>
<td>Retargeting a Hardware Compiler Proof</td>
</tr>
<tr>
<td>Dr. Y. A. Zorian</td>
<td>AT&amp;T Bell Labs, NJ</td>
<td>03/94</td>
<td>Multi-Chip Module Testing</td>
</tr>
<tr>
<td>Dr. A. Richardson</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>Defect Oriented Testability Analysis and Analog DFT</td>
</tr>
<tr>
<td>Mr. Th. Olbrich</td>
<td>Lancaster U.</td>
<td>06/94</td>
<td>BIST and Diagnostics in Safety Critical Microsystems</td>
</tr>
<tr>
<td>Dr. M. Slamani</td>
<td>Ecole Polytechnique de Montreal, Canada</td>
<td>07/94</td>
<td>BIST, Fault Diagnosis and Testability Analysis in Analog ICs based on Sensitivity Concept</td>
</tr>
<tr>
<td>H. Morel &amp; B. Allard</td>
<td>Centre de Génie Electr., Lyon</td>
<td>10/94</td>
<td>Utilisation des graphes de liens et des réseaux de Petri pour la simulation des systèmes de l’électronique de puissance</td>
</tr>
<tr>
<td>Dr. Rajeev Murgai</td>
<td>FUJITSU Labs of America Inc., San José</td>
<td>03/95</td>
<td>Decomposition of Logic Functions for Minimum Transition Activity</td>
</tr>
<tr>
<td>Prof. N. Yevtushenko &amp; Prof. A. Matrosova</td>
<td>Tomsk State Univ. Russia</td>
<td>04/95</td>
<td>- Testing strategies for communicating FSMs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Random simulation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Design for testability</td>
</tr>
<tr>
<td>Prof. G. de Micheli</td>
<td>Stanford Univ.</td>
<td>05/95</td>
<td>An algebraic approach to system-level modeling and synthesis</td>
</tr>
<tr>
<td>Prof. G. de Micheli</td>
<td>Stanford Univ.</td>
<td>05/95</td>
<td>Optimal synthesis of gated clocks for low power finite state machines</td>
</tr>
</tbody>
</table>

Concerning participation to external seminars, the following table lists the courses and seminars given by members of the laboratory on their specific research work, following the invitation of various institutions.
### VI-2.3 Support of Foreign Universities Teaching Programs

The laboratory has established for many years solid contacts with other research institutions and universities throughout the world. Exchange of students and post-doctoral fellows are very common, and TIMA members are often invited to participate in foreign university teaching programs. The following table lists this kind of activities during the recent academic years.

<table>
<thead>
<tr>
<th>University</th>
<th>Country</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Title or content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tallinn Technical Univ.</td>
<td>Estonia</td>
<td>05/93</td>
<td>9h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>12/93</td>
<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Inst. for Microel. Stuttgart</td>
<td>Germany</td>
<td>02/94</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line arithmetic operators</td>
</tr>
<tr>
<td>Politechnica Bucharest</td>
<td>Romania</td>
<td>05/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>CMOS VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>06/94</td>
<td>3h</td>
<td>M. Marzouki</td>
<td>Partial Boundary Scan Test</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>12/94</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>02/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Architecture and arithmetics</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>11/95</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>01/95</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Arithmetic</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>02/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>CMOS circuitry</td>
</tr>
<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
<td>03/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>Operators</td>
</tr>
<tr>
<td>Univ. de Las Palmas</td>
<td>Canarias</td>
<td>05/95</td>
<td>4h</td>
<td>A. Guyot</td>
<td>Garden Ws.: Operators in GaAs</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>05/95</td>
<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>École Poly. Fédérale Zürich</td>
<td>Switzerland</td>
<td>05/94</td>
<td>3h</td>
<td>I. Bacivarov</td>
<td>Dependability of distributed systems</td>
</tr>
</tbody>
</table>

### VI-2.4 Participation in EU Educational Programs

TIMA laboratory activities have a strong European profile. In addition to numerous research projects listed in other sections of this report, the following table indicates the involvement of TIMA staff members in educational programs launched by the European Union. This involvement take the form of organizing and/or teaching courses.

<table>
<thead>
<tr>
<th>University</th>
<th>Country</th>
<th>Date</th>
<th>Dur.</th>
<th>Participant</th>
<th>Title or content</th>
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</thead>
<tbody>
<tr>
<td>Tallinn Technical Univ.</td>
<td>Estonia</td>
<td>05/93</td>
<td>9h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>12/93</td>
<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>Inst. for Microel. Stuttgart</td>
<td>Germany</td>
<td>02/94</td>
<td>2h</td>
<td>A. Guyot</td>
<td>On-line arithmetic operators</td>
</tr>
<tr>
<td>Politechnica Bucharest</td>
<td>Romania</td>
<td>05/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>CMOS VLSI design course</td>
</tr>
<tr>
<td>Université de Monastir</td>
<td>Tunisia</td>
<td>06/94</td>
<td>3h</td>
<td>M. Marzouki</td>
<td>Partial Boundary Scan Test</td>
</tr>
<tr>
<td>T Hochschule Darmstadt</td>
<td>Germany</td>
<td>12/94</td>
<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
<tr>
<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>02/94</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Architecture and arithmetics</td>
</tr>
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<td>T Hochschule Darmstadt</td>
<td>Germany</td>
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<td>3h</td>
<td>A. Guyot</td>
<td>Advanced arithmetic operators</td>
</tr>
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<td>ISEN-Conception, Lille</td>
<td>France</td>
<td>01/95</td>
<td>6h</td>
<td>A. Guyot</td>
<td>Arithmetic</td>
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<tr>
<td>CIME-Jessica, Grenoble</td>
<td>France</td>
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<tr>
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<td>France</td>
<td>03/95</td>
<td>8h</td>
<td>A. Guyot</td>
<td>Operators</td>
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<tr>
<td>Univ. de Las Palmas</td>
<td>Canarias</td>
<td>05/95</td>
<td>4h</td>
<td>A. Guyot</td>
<td>Garden Ws.: Operators in GaAs</td>
</tr>
<tr>
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<td>Tunisia</td>
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<td>18h</td>
<td>A. Guyot</td>
<td>VLSI design course</td>
</tr>
<tr>
<td>École Poly. Fédérale Zürich</td>
<td>Switzerland</td>
<td>05/94</td>
<td>3h</td>
<td>I. Bacivarov</td>
<td>Dependability of distributed systems</td>
</tr>
<tr>
<td>Framework</td>
<td>Location</td>
<td>Date</td>
<td>Dur.</td>
<td>Participant</td>
<td>Activity</td>
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<tr>
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<td>--------</td>
<td>-------</td>
<td>-------------</td>
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<tr>
<td>JTTT Comet II</td>
<td>Greece</td>
<td>02/92</td>
<td>15h</td>
<td>A. Guyot</td>
<td>VLSI Design Course teaching</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>France</td>
<td>12/92</td>
<td>3h</td>
<td>M. Nicolaids</td>
<td>ASIC Testing</td>
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<td>EUROCHIP Esprit</td>
<td>Germany</td>
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<td>3h</td>
<td>M. Nicolaids</td>
<td>ASIC Testing</td>
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<tr>
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<td>Italy</td>
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<td>1h</td>
<td>M. Nicolaids</td>
<td>European School on High Reliability</td>
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<td></td>
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<td></td>
<td></td>
<td>Integrated Systems</td>
</tr>
<tr>
<td>JTTT Comet II</td>
<td>Greece</td>
<td>12/94</td>
<td>15h</td>
<td>M. Nicolaids</td>
<td>Advanced Course on VLSI Testing</td>
</tr>
<tr>
<td>EUROCHIP Esprit</td>
<td>Belgium</td>
<td>08/94</td>
<td>6h</td>
<td>A. Jerraya</td>
<td>System Design</td>
</tr>
<tr>
<td>Comett</td>
<td>Graz</td>
<td>04/95</td>
<td>3days</td>
<td>C. Liem</td>
<td>Reconfigurable architecture</td>
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<tr>
<td>Comett</td>
<td>Enschede</td>
<td>04/95</td>
<td>5days</td>
<td>P. Kission</td>
<td>Behavioral synthesis</td>
</tr>
<tr>
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<td>Grenoble</td>
<td>05/95</td>
<td>5days</td>
<td>A. Jerraya</td>
<td>Behavioral synthesis</td>
</tr>
<tr>
<td>Comett</td>
<td>Darmstadt</td>
<td>06/95</td>
<td>5days</td>
<td>F. Kission</td>
<td>Behavioral synthesis</td>
</tr>
</tbody>
</table>

### VI-2.5 University/Industry Joint Research Programs

A French national program, called CIFRE, allows French companies to receive French Ph.D. students. The thesis director must belong to a French university or public research laboratory. The student is employed by the company, and the research theme of the thesis must be of interest to the company.

TIMA staff members have been asked by companies to direct several Ph.D. theses in the CIFRE framework. The most recent ones are listed in the table below.

<table>
<thead>
<tr>
<th>Company</th>
<th>Student</th>
<th>Director</th>
<th>Dur.</th>
<th>Research Theme</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMD</td>
<td>Ch. Vaucher</td>
<td>L. Balme</td>
<td>90-93</td>
<td>PCB Testing</td>
</tr>
<tr>
<td>Hewlett Packard</td>
<td>P. Dulieux-Verguin</td>
<td>B. Courtois</td>
<td>91-94</td>
<td>Failure Analysis of ICs by Liquid Crystals</td>
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<tr>
<td>SGS Thomson</td>
<td>M. Kodrnja</td>
<td>A. Guyot</td>
<td>92-95</td>
<td>Analog Voltage Controlled Oscillators and Phase-Locked Loops</td>
</tr>
<tr>
<td>SGS Thomson</td>
<td>F. Lemery</td>
<td>M. Marzouki</td>
<td>92-95</td>
<td>Analog and Mixed Macromodeling</td>
</tr>
<tr>
<td>IMD</td>
<td>A. Benali</td>
<td>L. Balme</td>
<td>92-95</td>
<td>Electro-optic ATR</td>
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<tr>
<td>SGS Thomson</td>
<td>E. Berrebi</td>
<td>A. Jerraya</td>
<td>93-96</td>
<td>Heterogeneous System Design</td>
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<tr>
<td>SGS Thomson</td>
<td>F. Naçabal</td>
<td>A. Jerraya</td>
<td>95-96</td>
<td>Heterogeneous System Design</td>
</tr>
</tbody>
</table>
VII - PUBLICATIONS 1993-1994

VII-1 Books and magazines

1993

COURTOIS B., KERECSEN-RENCZ M.*
Trends in Microelectronics - European Perspectives
In Journal on Communications, Vol. XLIV, pp. 2-7, July 1993

* Technical University of Budapest, Hungary

JERRAYA A., O'BRIEN K., BEN ISMAIL T.
Linking system design tools and hardware design tools
In Proceedings of the CHDL'93, Ed. D. Agnew, L. Cleasen, R. Camposano,
Publ. Elsevier, 1993

NICOLAIDIS M., VARGAS F., COURTOIS B.
Design of Built-In Current Sensors for concurrent checking in radiation environments
In IEEE Transactions on Nuclear Science, December 1993

O'BRIEN K., PARK I., JERRAYA A., COURTOIS B.
Synthesis for control-flow dominated machines
Chapter in "Novel Architecture and Synthesis Methodologies for Future
Application-Specific Architecture Design: A perspective", 
Ed. F. Catthoor, L. Svensson,

PARK I., O'BRIEN K., JERRAYA A.
AMICAL: architectural synthesis based on VHDL

1994

COURTOIS B.
MPC activities in France (in Japanese)
Invited paper in IEICE Transactions, Japan, 1994

COURTOIS B.
CAD and testing of ICs and systems: where are we going?
In Journal of Microelectronic System Integration, PLENUM Publishing Corporation,
Vol. 2(3), pp. 139-201, 1994

DUARTE DE OLIVEIRA R., NICOLAIDIS M.
A test methodology applied to cellular logic programmable gate arrays
Lectures in Computer Science, Field Programmable Logic: Architectures, Synthesis
and Applications
Spring-Verlag Berlin Heidelberg 1994
Editors: R. W. Hartenstein, M.Z. Servit

JERRAYA A., O'BRIEN K.
SOLAR: an intermediate format for system level modeling and synthesis
KEBICHI O., YARMOLIK* V.N., NICOLAIDIS M.
Zero aliasing ROM BIST

* Minsk Radioengineering Institute, Minsk, Bielorussia

NICOLAIDIS M.
Fault secure property versus strongly code disjoint checkers
In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (CAD/ICAS), May 1994

NICOLAIDIS M., KEBICHI O., CASTRO ALVES V.
Trade-offs in scan path and BIST implementations for RAMs

NICOLAIDIS M., KEBICHI O., CASTRO ALVES V.
Trade-offs in scan path and BIST implementations for RAMs
Editors: M. Abadir, T. Ambler

RAHMOUNI M., O' BRIEN K.*, JERRAYA A.
A loop-based scheduling algorithm for hardware description languages

* LEDA SA, Meylan, France

1995

BACIVAROV I.*, BALME L. (Guest Editors)
Quality effort in Europe
Special issue of the Journal of Quality Engineering, Vol. 9
Publication by Marcel DEKKER Inc., New York, USA, to be published in 1995

* POLITECNICA Univ., Bucharest, Romania

BALME L., BACIVAROV I.*
European programme in quality of complex integrated systems
Special issue of the Journal of Quality Engineering, Vol. 9
Publication by Marcel DEKKER Inc., New York, USA, to be published in 1995

* POLITECNICA Univ., Bucharest, Romania

BEN ISMAIL T., O'BRIEN K.*, JERRAYA A.
PARTIF: an interactive system-level partitioning

LEDA S.A., Meylan, France

BEN ISMAIL T., JERRAYA A.
Synthesis steps and design models for CoDesign
IEEE Computer, special issue on rapid-prototyping of microelectronic systems, February 1995
COURTOIS B.
The activities of Multiproject Chip Service in the world
Invited paper in the Journal of Future Electron Devices Institute, Tokyo, Japan
To appear in 1995

HELLEBRAND S.*, RAJSKI J., TARNICK S., VENKATARAMAN S., COURTOIS B.
Built-in test for circuits with scan based on reseeding of multiple-polynomial linear
feedback shift registers
IEEE Transactions on Computers, Special issue on Fault-Tolerant Computing,
to appear in 1995

* University of Siegen, Germany
** McGill University, Montreal, Canada
*** Max-Planck-Society, Fault Tolerant Computing Group at Univ. of Potsdam, Germany
**** C&SRL Laboratory, Univ. of Illinois at Urbana-Champaign, Urbana, USA

JERRAYA A., BERREBI E., DING H., KISSION P., RAHMOUNI M.,
VIJAYA RAGHAVAN V.
A pragmatic approach to behavioral synthesis
Electronic Engineering Journal
to appear in 1995 (May)

KOLARIK V., MIR S., LUBASZEWSKI M., COURTOIS B.
Analogue checkers with absolute and relative tolerances
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
to appear in 1995

NICOLAIDIS M., CASTRO ALVES V., BEDERR H.
Testing complex couplings in multi-port memories
IEEE Transactions on VLSI Systems, March 1995

NICOLAIDIS M.
Efficient UBST implementation for microprocessor sequencing parts
Journal of Electronic Testing, Theory and Applications (JETTA), Kluwer Academic

VAUCHER C.*, BALME L., BENALI A.
The PPM myth in board assembly
Quality Effort in Europe, Special issue of the Journal of Quality Engineering
Vol. 9, Publication by Marcel DEKKER Inc., New York, USA, to be published in 1995

* IMD, Grenoble, France

VII-2 Conferences and Workshops

1993

BAIARD J.C.*, GUYOT A., MULLER J.M.*, SKAF A.
Design of a VLSI circuit for on-line evaluation of several elementary functions using their
taylor expansion
International Conference on Application Specific Array Processors (ASAP 93)
Venice, Italy, October 1993

* LIP-Ecole Normale Supérieure de Lyon, Lyon, France
BALME L.  
The TQM window concept: an innovative decision aid tool for managers  
World Quality Congress, EOQ, ASQC, JUSE, IAQ,  
Helsinki, Finland, June 14-18, 1993

BOUDJIT M., NICOLAIDIS M., TORKI K.  
Automatic generation algorithms, experiments and comparisons of self-checking PLA  
schemes using parity codes  
EDAC-EUROASIC Conference,  
Paris, France, 22-25 February 1993

BOURAOUI R., GUYOT A., WALKER G.  
Design of an on-line Euclidian processor  
6th International Conference on VLSI design  
Bombay, India, January 1993

BOURAOUI R., GUYOT A., WALKER G.  
On-line operator for Euclidian distance  
EDAC-EUROASIC Conference  
Paris, France, 22-25 February 1993

BUATHIER L.*, COISSARD V.*, HERVET Ph.*, PELLAT B.*, ROUSSEAU T.*,  
GUYOT A.  
Introduction to research in a VLSI design project  
4th EUROCHIP Workshop on VLSI Design Training  
Toledo, Spain, 29 September - 1st October 1993  
* Students

CASTRO ALVES V., KEBICHI O., FERREIRA A.*  
A new class of fault models and test algorithms for dual port dynamic RAM testing  
In Proceedings of the 1993 IEEE International Workshop on Memory Testing  
San Jose, CA, USA, 9-10 August 1993  
* LIP Laboratory, Ecole Normale Supérieure de Lyon, France

COURTOIS B.  
CAD and testing of ICs and Systems: Where are we going?  
Invited presentation at the 2nd ESA Electronics Components Conference at ESTEC  
Noordwijk, The Netherlands, 24-28 May 1993

COURTOIS B.  
The state of the art in CAD  
Invited presentation at the Workshop on Computer Aided Methods and Technical  
Management in Electrical Engineering Education  
Budapest, Hungary, 16-18 June 1993

COURTOIS B.  
Trends in fabrication, design and CAD - European perspectives  
3rd International Conference on VLSI and CAD (ICVC'93)  
Taejon, Korea, 15-17 November 1993

COURTOIS B.  
Perspectives in IC CAD and test  
5th International Symposium on IC Technology, Systems & Applications  
(ISIC 93)  
Singapore, 15-17 September 1993
COURTOIS B.
Future trends for the design and test of microelectronic systems
Invited talk at "25 Jahre UNIDO", Symposium organized to celebrate the 25 years of
Dortmund University
Dortmund, Germany, 16 December 1993

HELEBRAND S.*, TARNICK S.*, RAJSKI J.**, COURTOIS B.
Effiziente Erzeugung deterministischer Muster im Selbsttest
5. ITG/GI/GME-Workshop zum Thema, Test-methoden und Zuverlässigkeit von
Schaltungen und Systemen
Holzhau, Germany, 14-16 March 1993

*University of Siegen, Germany
** Mc Gill University, Montreal, Canada

IOAN D.*, LAZARESCU M.T.*, GUYOT A.
Educational aspects of VLSI training at postgraduate level
4th EUROCHIP Workshop on VLSI Design Training
Toledo, Spain, 29 September - 1st October 1993

* Polytechnical University of Bucharest, Romania

JERRAYA A., PARK I., O'BRIEN K.
AMICAL: an interactive high level synthesis environment
EDAC-EUROASIC Conference
Paris, France, 22-25 February 1993

JERRAYA A.
Bridging the gap between CASE tools and IC CAD tools
Second IFIP International Workshop on Hardware/Software Codesign
Innsbruck, Austria, 24-27 May 1993

JERRAYA A., O'BRIEN K., BEN ISMAIL T.
Linking system design tools and hardware design tools
CHDL'93
Ottawa, Canada, April 1993

KISSON P., CLOSSE E.*, BERGHER L.**, JERRAYA A.
Industrial experimentation of high-level synthesis
EURO-DAC'93 (European Design Automation Conference) with EURO-VHDL'93
Hamburg, Germany, 20-24 September 1993

* Centre National d'Etudes des Télécommunications (CNET), Meylan, France
** Thomson Consumer Electronic Components (TCEC), Meylan, France

KOLARIK V., LUBASZEWSKI M., COURTOIS B.
Towards self-checking mixed-signal integrated circuits
19th European Solid-State Circuits Conference (ESSCIRC'93)
Sevilla, Spain, September 22-24, 1993

LUBASZEWSKI M., CASTRO ALVES V., NICOLAIDIS M., COURTOIS B.
Checking signatures on boundary scan boards
European Test Conference
Rotterdam, NL, April 19-22, 1993
LUBASZEWSKI M., COURTOIS B.
Designing fault-tolerant systems by using self-checking replicas
Built-In Self-Test / Design for Testability Workshop (BIST/DFT)
Kiawah Island, Charleston, SC, USA, March 17-19, 1993

LUBASZEWSKI M., COURTOIS B.
Reliable fail-safe systems
2nd Asian Test Symposium (ATS 93)
Beijing, China, 16-18 November 1993

MARZOUKI M., LUBASZEWSKI M., TOUATI M.H.
Unifying test and diagnosis of interconnects and logic clusters in partial boundary scan
boards
International Conference on Computer Aided Design (ICCAD 93)
Santa Clara, USA, 7-11 November 1993

MORIN J.P.*, LEMERY F., NERCESSIAN E.*, SHARMA V.*, BENKOSKI J.*, SAMANI D.*
A practical approach to top/down analog circuit design
19th European Solid-State Circuits Conference (ESSCIRC'93)
Sevilla, Spain, September 22-24, 1993

* SGS-Thomson Microelectronics, Grenoble, France

MOUSSA I., SKAF A., GUYOT A.
Design of a GaAs redundant divider
VLST'93 Conference
Grenoble, France, 7-9 September 1993

MOUSSA I., ROST P., GUYOT A.
Design and comparison of GaAs and CMOS redundant divider
19th European Solid-State Circuits Conference (ESSCIRC 93)
Sevilla, Spain, 22-24 September 1993

NICOLAIDIS M.
Finitely self-checking circuits and their application on current sensors
11th IEEE VLSI Test Symposium
Atlantic City, USA, April 1993

NICOLAIDIS M., CASTRO ALVES V., KEBICHI O.
Trade-offs in scan path and BIST implementations for RAMs
European Test Conference, Rotterdam, The Netherlands, April 1993
and International Workshop on the Economics of Design, Test and Manufacture, Austin,
Texas, USA, 10-11 May 1993

NICOLAIDIS M.
Efficient implementations of self-checking adders and ALUs
23rd IEEE International Symposium on Fault Tolerant Computing
Toulouse, France, June 1993

NICOLAIDIS M., VARGAS F., COURTOIS B.
Design of reliable current sensors for radiation exposed environments
30th Annual International Nuclear and Space Radiation Effects Conference (NSREC'93)
Snowbird, Utah, USA, July 19-23, 1993
O'BRIEN K., RAHMOUNI M., JERRAYA A.
DLS: a scheduling algorithm for high-level synthesis in VHDL
EDAC-EUROASIC Conference,
Paris, France, 22-25 February 1993

O'BRIEN K., BEN ISMAIL T., JERRAYA A.
A flexible communication modelling paradigm for system-level synthesis
Handouts of International Workshop on Hardware-Software Co-design
Cambridge, MA, USA, October 1993

SKAF A., BAJARD J.C.*, GUYOT A., MULLER J.M.*
A VLSI circuit for on-line polynomial computing: application to exponential, trigonometric
and hyperbolic functions
VLSI 93, Grenoble, France, September 1993

* LIP-Ecole Normale Supérieure de Lyon, Lyon, France

SKAF A., GUYOT A.
VLSI design of on-line add/multiply algorithms
International Conference on Computer Design (ICCD'93)
Cambridge, Massachusetts, USA, 4-6 October 1993

VARGAS F., NICOLAIDIS M., HAMDI B.
Quiescent current estimation based on quality requirements
11th IEEE VLSI Test Symposium
Atlantic City, USA, April 6-8, 1993

VARGAS F., NICOLAIDIS M., COURTOIS B.
Quiescent current monitoring to improve the reliability of electronic systems in space
radiation environments
1993 International Conference on Computer Design (ICCD'93)
Cambridge, Massachusetts, USA, 3-6 October 1993

VAUCHER C., BALME L.
The standard mirror boards (SMBs) concept: an innovative improvement of traditional ATE
for up to 10 mil bare board testing
International Test Conference 1993 (ITC)
Baltimore, Maryland, USA, 17-21 October 1993

YARMOLIK V.N.*, NICOLAIDIS M.
Exact aliasing computation and/or aliasing free design for RAM BIST
In Proceedings of the 1993 IEEE International Workshop on Memory Testing
San Jose, CA, USA, 9-10 August 1993

* On leave from Minsk Radioengineering Institute, Minsk, Bielorussia

1994

BACIVAROV* I.C., BALME L.
On reliability testing of semiconductor devices
European Safety and Reliability Conference (ESREL 94)
La Baule, France, 30 May - 3 June, 1994

* Visiting Professor on leave from POLITECNICA Univ., Bucharest, Romania
BEDERR H., NICOLAIDIS M., GUYOT A.
Design for testability for on-line multipliers
12th IEEE VLSI Test Symposium
Cherry Hill, USA, April 1994

BENALI A., BALME L., VAUCHER Ch.
An image processing based software for bare board test data generation
Asian Test Conference (ATC'94)
Nara, Japan, November 1994

BEN ISMAIL T., O'BRIEN K.*, JERRAYA A.
Interactive system-level partitioning with PARTIF
The European Design and Test Conference (EDAC-ETC-EUROASIC 94)
Paris, France, 28 February - 3 March 1994

LEDA S.A., Meylan, France

BEN ISMAIL T., ABID M.*, O'BRIEN K.**, JERRAYA A.
An approach for hardware-software codesign
International Workshop on Rapid System Prototyping (RSP'94)
Villard de Lans (Grenoble), France, 20-23 June. 1994

* ENIM, Monastir, Tunisia
** LEDA S.A., Meylan, France

BEN ISMAIL T., ABID M.*, JERRAYA A.
COSMOS: a codesign approach for communicating systems
International Workshop on hardware/software codesign (CODES/CASHE)
Grenoble, France, September 1994

* ENIM, Monastir, Tunisia

BEN ISMAIL T., JERRAYA A.
Tutorial: Hardware/software codesign
Invited paper at 8th Brazilian Symposium on Integrated Circuits Design
Gramado, Brazil, November 1994

CINQUIN Ph.*, TROCCAZ J.*, KARAM J.M.
Microsystems and computer assisted medical interventions: prospectives in medical applications
Microengineering in Medicine, in Biology, and its Application to Minimally Invasive Techniques for Therapy and Medical Diagnosis
EPFL, Lausanne, Switzerland, 5-7 October 1994

* TIMC, La Tronche, France

COURTOIS B.
Some trends in CAD, test and fabrication of circuits and systems
Keynote presentation at Third International Workshop on The Economics of Design, Test and Manufacturing
Austin, Texas, USA, 16-17 May 1994

COURTOIS B.
Perspectives in CAD, test and manufacturing of circuits and systems
Keynote presentation at Second Asia Pacific Conference on Hardware Description Languages (APCHDL'94)
Toyohashi, Japan, 24-25 October 1994
COURTOIS B.
The CMP Service
XXI International Conference and School for young scientists and professionals within the framework of "Informatization of Russia Program"; New information technologies for science, education and business (CAD’94)
Yalta, Ukraine, 4-13 May 1994

COURTOIS B., RENCZ M.*
Trends in fabrication, design and CAD - European perspectives
XXI International Conference and School for young scientists and professionals within the framework of "Informatization of Russia Program"; New information technologies for science, education and business (CAD’94)
Yalta, Ukraine, 4-13 May 1994

* Technical University of Budapest, Hungary

COURTOIS B.
The Services available from CMP
Invited paper at IX SBMICRO
Rio de Janeiro, Brazil, 10-12 August 1994

COURTOIS B.
MPC Service:
Invited talk at IEEE Asia-Pacific Conference on Circuits and Systems
(APCCAS’94)
Taipei, Taiwan, 5-8 December 1994

DUARTE R., NICOLAIDIS M.
A test methodology applied to cellular logic programmable gate arrays
4th Field Programmable Logic and Applications (FPL’94)
Prague, Czech Republic, September 7-9, 1994

GUYOT A., BELRHIRI M.*, BOSCO G.*
Adders synthesis
IFIP Workshop on logic and architecture synthesis
Grenoble, 19-21 December 1994

* CSI/INPG, Grenoble

HOFFMANN K.*, KARAM J.M., GLESNER M.*, COURTOIS B.
Entwurf und Simulation von Mikrosystemen
Gründungssitzung der GI-Fachgruppe 3.5.6 Mikrosystemtechnik,
Schloss Dagstuhl, Dagstuhl, Germany, 21-22 November 1994

* TH Darmstadt, FG Mikroelektronische Systeme, Germany

KEBICHI O., YARMOLIK V.*, NICOLAIDIS M.
Aliasing-free signature analysis for RAM BIST
International Test Conference (ITC’94)
Baltimore, Maryland, USA, October 1994

* Minsk Radioengineering Institute, Minsk, Bielorussia
KISSION P., DING H., JERRAYA A.
Structured design methodology for high level design
31st Design Automation Conference (DAC'94)
San Diego, California, USA, 6-10 June, 1994

KISSION P., DING H., JERRAYA A.
Accelerating the design process by using architectural synthesis
5th International Workshop on Rapid System Prototyping (RSP'94)
Villard de Lans (Grenoble), France, 20-23 June, 1994

KOLARIK V., LUBASZEWSKI M., COURTOIS B.
Designing self-exercising analogue checkers
VLSI Test Symposium '94,
Cherry Hill, N.J., USA, April 25-28, 1994

Behavioral models for complex top/down analog/digital system simulation
1994 European Simulation MultiConference - Modelling & Simulation (ESM'94)
Barcelona, Spain, June 1-3, 1994

* SGS-Thomson Microelectronics, Grenoble, France

LUBASZEWSKI M., MARZOUKI M., TOUATI M.H.
A pragmatic test and diagnosis methodology for partially testable MCMs
IEEE Multi-Chip Module Conference (MCMC'94)
Santa Cruz, California, USA, 15-18 March 1994

LUBASZEWSKI M., KOLARIK V., MIR S., COURTOIS B.
Self-checking analogue and mixed-signal fully differential circuits
Design For Testability / Built-In Self-Test Workshop (DFT/BIST)
Vail, Colorado, USA, April 19-22, 1994

LUBASZEWSKI M., COURTOIS B.
On-line&off-line, analogue&digital, circuit&board, safety&reliability :
how to solve the testing puzzle ?
IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS'94)
Taipei, Taiwan, December 5-8, 1994

MARZOUKI M., COURTOIS B., CASTRO ALVES V.*
High-level synthesis for testability: where should we go from ?
1st International Test Synthesis Workshop
Santa Barbara, California, USA, May 18-20, 1994

* University of Aveiro, Portugal

MIR S., KOLARIK V., LUBASZEWSKI M., NIELSEN C., COURTOIS B.
Built-in self-test and fault diagnosis of fully differential analogue circuits
International Conference on Computer Aided Design (ICCAD'94)
San Jose, California, USA, November 6-10, 1994

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International Conference on Computer Design, (ICCD'94)
Cambridge, Massachusetts, USA, 10-12 October 1994
MONTALVO L., BEHNAM B., VASSILEVA T.*, GUYOT A.
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20th European Solid-State Circuits Conference (ESSCIRC'94)
Ulm, Germany, 20-22 September 1994

* "Politechnica", Sofia, Bulgaria

MONTALVO L. GUYOT A.
A minimaly redundant radix-4 divider with operands scaling
IX Congreso de Diseño de Circuitos Integrados "DCIS'94"
Maspalomas, Gran Canaria, Spain, 9-11 November 1994

MOUSSA L., GUYOT A., GARNIER C.
A GaAs Radix-2 borrow-save 16x16 bit divider
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Paris, France, 28 February - 3 March 1994

NICOLAIDIS M., BEDELL H.
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Efficient UBIST for RAMs
12th IEEE VLSI Test Symposium
Cherry Hill, USA, April 1994

NICOLAIDIS M.
Strongly fail-safe interface based on concurrent checking
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Nara, Japan, 15-17 November 1994

SKAF A., GUYOT A.
Power series on-line computing on silicon
The European Design and Test Conference (EDAC-ETC-EUROASIC 94)
Paris, France, 28 February - 3 March 1994

SKAF A., MULLER J.M.*, GUYOT A.
On-line hardware implementation for complex exponential and logarithm
20th European Solid-State Circuits Conference (ESSCIRC'94)
Ulm, Germany, 20-22 September 1994

* LIP/ENSL, Lyon, France

SOMA M.*, KOLARIK V.
A Design for test techniques for switched-capacitor filters
VLSI Test Symposium '94

* University of Washington at Seattle, USA

VACHER A., BENKEBBAB M.*, GUYOT A., ROUSSEAU T.*, SKAF A.
A VLSI implementation of parallel fast FOURIER transform
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Paris, France, 28 February - 3 March 1994

* Students at ENSERG, Grenoble, France
VACHER A., GUYOT A.
Error-speed compromise for FFT VLSI
26th IEEE Southeastern Symposium on System Theory
Athens, Ohio, USA, March 20-22, 1994

VACHER A., GUYOT A.
A VLSI implementation of Fast Fourier Transform for a large number of samples
SPRANN'94,
Lille, France, 25-27 April 1994

VARGAS F., NICOLAIDIS M.
SEU tolerant SRAM design based on current monitoring
24th IEEE International Symposium on Fault Tolerant Computing
Austin, Texas, June 1994

VARGAS F., DUARTE R., NICOLAIDIS M.
A current testing technique to improve IC quality requirements
Congresso da Sociedade Brasileira da Computacao (SBC)
Caxambu, Belo Horizonte, Brazil, August 1994

VOSS M.*, BEN ISMAIL T., JERRAYA A, KAPP K.H.*
Towards a theory for hardware/software кодesign
International Workshop on hardware/software codesign (CODES/CASHE)
Grenoble, France, September 1994

* IMA, Universität Karlsruhe, Germany

1995

BEDERR H., NICOLAIDIS M., GUYOT A.
Analytic approach for error masking elimination in on-line multipliers
IEEE Symposium on Computer Arithmetic
Bath, England, 19-21 July 1995

COURTOIS B.
Trends and perspectives in integrated circuits and systems
Invited paper at 4th International Conference on VLSI and CAD (ICVC'95)
Seoul, Korea, 15-18 October 1995

COURTOIS B., LUBASZEWSKI M.
On-line and off-line testing: from digital to analog, from circuits to boards
Invited paper at European Solid-State Circuits Conference (ESSCIRC'95)
Lille, France, 19-21 September 1995

COURTOIS B., LUBASZEWSKI M.
From digital to analog self-checking circuits
Invited paper at Mixed Design of VLSI Circuits - Education of Computer Aided Design of Modern VLSI Circuits - (MIXVLSI'95)
Krakow, Poland, 29-31 May 1995

COURTOIS B.
Trends and needs in testing integrated circuits and systems
Invited talk at AT&T Conference on Electronic Testing (ACET'95)
Princeton, NJ, USA, 24-25 April 1995
DUMITRESCU M.*, KARAM J.M., COURTOIS B.
Approximation choices for the numerical modeling of some optical guiding structures
Physics and Simulation of Optoelectronic Devices Conference
SPIE's Photonics West'95
San José, California, USA, 4-10 February 1995

* "Politehnica" University, Bucharest, Romania

GUYOT A., MONTALVO L., HOUELLE A.*, MEHREZ H.*, VAUCHER N.*
Comparison of the layout synthesis of Radix-2 and Pseudo-Radix-4 dividers
8th International Conference on VLSI Design (VLSI Design'95)
New Delhi, India, January 4-7, 1995

* Pierre et Marie Curie University, Paris, France

HAMDI B., BEDERR H., NICOLAIDIS M.
A tool for automatic generation of self-checking data-paths
13th IEEE VLSI Test Symposium (VTS'95)
Princeton, New Jersey, USA, 30 April - 3 May 1995

HOUELLE A.*, MEHREZ H.*, VAUCHER N.*, MONTALVO L., GUYOT A.
Application of fast layout synthesis environment to dividers evaluation
IEEE Symposium on Computer Arithmetic
Bath, England, 19-21 July 1995

* MASI Laboratory, Paris, France

KHALED S.*, KAMINSKA B.*, LUBASZEWSKI M., COURTOIS B.
Frequency-based BIST for analogue circuit testing
13th IEEE VLSI Test Symposium (VTS'95)
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* "Ecole Polytechnique de Montréal", Canada

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Area versus error detection latency trade-offs in self-checking RAMs
European Design and Test Conference (EDAC-ETC-EUROASIC'95)
Paris, France, 6-9 March 1995

*AT&T Bell Laboratories, Princeton, USA

KISSION P., DING H., JERRAYA A.
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EURO-VHDL'95
Brighton, UK, 18-22 September 1995

LEMERY F.*, MORIN J.P.*, NERCESSIAN E. **
Analog and mixed modeling with HDL-A - An evaluation
ESIP Workshop on Libraries, Component Modeling and Quality Assurance
Nantes, France, April 1995

* TIMA/SGS-Thomson
** SGS-Thomson
LUBASZEWSKI M., KOLARIK V., MIR S., NIELSEN C., COURTOIS B.
Mixed-signal circuits and boards for high safety applications
European Design and Test Conference (EDAC-ETC-EUROASIC'95)
Paris, France, 6-9 March 1995

MARZOUKI M., CASTRO ALVES V.*, ANTUNES RIBEIRO A.*
Requirements and general framework for an efficient synthesis for testability methodology
2nd International Test Synthesis Workshop
Santa Barbara, CA, USA, May 1995

*Federal University of Rio de Janeiro (UFRJ), Brazil

MONTALVO L., GUYOT A.
Svoboda-Tung division with no compensation
8th International Conference on VLSI Design (VLSI Design'95)
New Delhi, India, January 4-7, 1995

RAHMOUNI M., JERRAYA A.
PPS: a pipeline PATH based scheduler
European Design and Test Conference (EDAC-ETC-EUROASIC'95)
Paris, France, 6-9 March 1995

RAHMOUNI M., JERRAYA A.
Formulation and evaluation of scheduling techniques for control flow graphs
EURO-DAC'95
Brighton, UK, 18-22 September 1995

ROMDHANI M., JEFFROY A.*, DE CHAZELLES P.*, SAHRAOUI A.E.K.,**, JERRAYA A.
Modelling and rapid prototyping of avionics using StateMate
6th IEEE International Workshop on Rapid System Prototyping
Chapel Hill, North Carolina, USA, 7-9 June 1995

*AEROSPATIALE Aircraft, Avionics and Systems Division, Toulouse, France
** LAAS/CNRS, Toulouse, France

ROMDHANI M., JEFFROY A.*, DE CHAZELLES P.*, JERRAYA A.
Composing ActivityCharts/StateCharts, SDL and SAO specifications for codesign
in avionics
EURO-DAC'95
Brighton, UK, 18-22 September 1995

*AEROSPATIALE Aircraft, Avionics and Systems Division, Toulouse, France

SKAF A., GUYOT A.
SAGA: the first general-purpose on-line arithmetic co-processor
8th International Conference on VLSI Design (VLSI Design'95)
New Delhi, India, January 4-7, 1995

VACHER A., GUYOT A.
Radix-8 Butterflies for folded FFT
27th IEEE Southeastern Symposium on System Theory
Starkville, Mississippi, USA, 13-15 March 1995
VACHER A., GUYOT A.
Spread and folded architectures for FFT
27th IEEE Southeastern Symposium on System Theory
Starkville, Mississippi, USA, 13-15 March 1995

VALDERRAMA C.A., CHANGUEI A., P.V. VIJAYA-RAGHAVAN, ABID M.*, BEN ISMAIL T., JERRAYA A.
A unified model for co-simulation and co-synthesis of mixed hardware/software systems
European Design and Test Conference (EDAC-ETC-EUROASIC'95)
Paris, France, 6-9 March 1995

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Ecole Nationale d'Ingénieurs de Monastir (ENIM), Monastir, Tunisie

National Workshops

1994

CINQUIN Ph.*, TROCAZ J.*, KARAM J.M.
Applications médicales des microsystèmes
Capteurs intégrés et microsystèmes
CNET, Meylan, France, 22 November 1994

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TIMC, La Tronche, France

COURTOIS B., KARAM J.M.
Service Multi Projets pour microsystèmes CMPM
Capteurs intégrés et microsystèmes
CNET, Meylan, France, 22 November 1994

VII-3 Theses

1993

BOURAOUI Rachid
Calcul sur les grands nombres et VLSI : application au PGCD, au PGCD étendu et à la
distance euclidienne
Thèse de Doctorat INPG - 15 janvier 1993

O'BRIEN Kevin
Compilation de silicium : du circuit au système
Thèse de Doctorat INPG - 31 mars 1993

KUSUMAPUTRI-HORNIK Yustina
Opérateurs arithmétiques standards en-ligne à très grande précision
Thèse de Doctorat INPG - 11 mai 1993

BEN OTHMAN Mohamed Tahar
Evaluation d'une hiérarchie mémoire pour une machine symbolique
Thèse de Doctorat INPG - 8 septembre 1993

VAUCHER Christophe
Le test haute résolution de circuits imprimés nus
Thèse de Doctorat INPG - 25 novembre 1993
1994

HAMDI Belgacem  
Outils CAO pour la génération automatique de parties opératives auto-contrôlables  
Thèse de Doctorat INPG - 18 Avril 1994

AICHOUCHI Mohamed  
Etude des liens entre la synthèse architecturale et la synthèse au niveau transfert de registres  
Thèse de Doctorat INPG - 20 juin 1994

LUBASZEWSKI Marcelo  
Le test unifié de cartes appliqué à la conception de systèmes fiables  
Thèse de Doctorat INPG - 20 juin 1994

KEBICHI Omar  
Techniques et outils de CAO pour la génération automatique de BIST et DFT pour RAMS  
Thèse de Doctorat INPG - 15 juillet 1994

KOLARIK Vladimir  
Techniques avancées de test de circuits analogiques et mixtes analogiques-numériques  
Thèse de Doctorat INPG - 31 octobre 1994

BEDERR Hakim  
Contribution à la conception en vue du test d'opérateurs à structure itérative  
Thèse de Doctorat INPG - 25 novembre 1994

VERGUI Pascale  
Industrialisation d'une méthode de localisation de défauts sur circuits intégrés par cristaux liquides  
Thèse de Doctorat INPG - 20 décembre 1994

1995

MONTALVO Luis Anibal  
Systèmes de numération pour la conception de diviseurs rapides  
Thèse de Doctorat INPG - 13 mars 1995

VII-4 Reports

1993

COURTOIS B.  
CAD and Testing of ICs and systems : where are we going ?  
TIMA Research Report, May 1993

VII-5 Patents

1993

VAUCHER & al.  
Standard Mirror Board  
September 93 (FR 93/09571)
1994

BALME L. & al.
Smart Power card
US patent 07/937900

VARGAS F., NICOLAIDIS M.
A current monitoring-based technique to detect and correct single-event upsets (SEUs) in static RAMs for space applications
Brevet CNRS, Grenoble, France, June 1994
VIII - MISCELLANEOUS

VIII.1 What did they do after graduating from the Laboratory (1984-1994)?

Below is the list of researchers which graduated from the Computer Architecture Group, from 1984.

The first affiliation corresponds to their affiliation right after the thesis. Eventually, successive affiliations are provided.

From 1984 to 1994, 65 theses have been defended.

It might be noticed that (apart from foreign students who returned in their country), several members of the group have been or are working abroad, especially in Canada and Switzerland.

DERANTONIAN H.
Génération automatique de parties contrôles de microprocesseurs sous forme de PLA spécialisés.

NICOLAIDIS M.
Conception de circuits intégrés ou testables pour des hypothèses de pannes analytiques.
CNRS - TIMA Laboratory - Grenoble

LAURENT J.
Projet ACIME : Analyse des Circuits Intégrés par Microscopie Electronique.
CNRS - TIMA Laboratory - Grenoble
Next: CNRS - IMAG - Grenoble

HMIMID M.
Assemblage et génération automatique des dispositifs périphériques de PLA complexes.
SIEMENS - Munich - FRG

SAHBATOU M. D.
Une méthode de conception de microprocesseurs CMOS : application au 8048 (INTEL)

CHUQUILLANQUI S.
Une nouvelle approche pour l'optimisation topologique et l'automatisation du dessin des masques de PLA complexes.
BULL Systèmes - Les Clayes Sous Bois
Next : THOMSON THOM'6 - Paris
Next : GEC ALSTHOM - Paris la Défense
BOURCIER E.
Conception et réalisation du simulateur de langage de description de circuits intégrés
IRENE C.
SGS THOMSON - Grenoble

JANSCH I.
Conception de contrôleurs autotestables pour des hypothèses de pannes analytiques.
Porto Alegre University - Brazil

BERGHER L.
Analyse de défauts de circuits VLSI par microscopie électronique à balayage.
SGS THOMSON - Grenoble
Next : BULL Systèmes - Les Clayes Sous Bois
Next : SGS-THOMSON - Grenoble

IANESELLI J.C.
Un opérateur d'unification pour une machine base de connaissance PROLOG.
MERLIN GERIN - Meylan

SUWARDI I.S.
Mécanismes prédictifs d'evaluation des caractéristiques géométriques des circuits VLSI.

SCHOELLKOPF J.P.
SILICIEL : Contributions à l'architecture des circuits intégrés et à la compilation du silicium.
BULL Systèmes - Les Clayes Sous Bois
Next : SGS THOMSON - Grenoble

BERTRAND F.
Conception descendante appliquée aux microprocesseurs VLSI
BULL Systèmes - Les Clayes Sous Bois
Next : LETI - Grenoble

MARTINEZ F.
CIRENE : Compilateur du langage IRENE

GUIGUET I.
Liaison d'un microscope électronique à balayage aux outils CAO de description des circuits intégrés.
APSIS - Meylan

PEREZ SEGOVIA T.
PAOLA : un système d'optimisation topologique de PLA.
CNET - Meylan
MARINE S.
Un langage pour la description, simulation et synthèse automatique du matériau VLSI
SGS THOMSON - Grenoble
Next : ALCATEL-Alsthom, Marcoussis

BASCHIERA D.
Modélisation de pannes et méthodes de test de circuits intégrés CMOS
TRT - Paris
Next : NORSKDATA - Norway
Next : EPFL - Lausanne - Switzerland
Next : HMT - Brügg b/Biel - Switzerland

ALIOUAT M.
Reprise de processus dans un environnement distribué après pannes matérielles transitoires
ou permanentes
Thèse de Docteur Ingénieur - Avril 1986
University of Constantine - Algeria

OSSEIRAN A.
Définition, étude et conception d'un microprocesseur autotestable spécifique : COBRA
EPFL - Lausanne - Switzerland
Next: University of Geneva, Switzerland

JAMIER R.
Génération automatique de parties opératives de circuits VLSI de type microprocesseur
Thèse de Docteur Ingénieur - Décembre 1986.
SGS THOMSON - Grenoble

DANG W.
Parallélisme dans une machine base de connaissances PROLOG
CRIL - Colomnes

VARINOT P.
Compilation de silicium : application à la compilation de parties contrôles
University of Porto Alegre - Brazil
Next : MATRA - Paris

HOCHET B.
Conception de VLSI : Applications au calcul numérique
EPFL - Lausanne - Switzerland
Next : University of Adelaide - Australia
Next : University of Yverdon, Switzerland

ROUGEAUX F. R.
Outils de CAO et conception structurée de systèmes intégrés sur silicium
University of Laval - Canada
Next : IBM - Montpellier
SOUAI M.
Etude d'un moniteur d'un système fonctionnellement réparti.

CAISSO J.P.
Contribution à la vérification des circuits intégrés dans un environnement multivalué.
Mc GILL University - Montréal - Canada
Next : MATRA-MHS - Nantes

BEKKARA N.
Optimisation et compromis surface-vitesse dans le compilateur de silicium SYCO
SGS THOMSON - Grenoble

DUPRAT J.
LAIOS : un réseau multiprocesseur orienté intelligence artificielle
E.N.S. Lyon

MHAYA N.
Compilateur de parties contrôle de microprocesseurs
IFATEC - Versailles

FERNANDES A.
Test des PLAs optimisés topologiquement
University of Belo Horizonte - Brazil
Next: Professor at "Universidade Federal de Minas Gerais", Belo Horizonte, Brazil

ZYSMAN E.
Conception de parties contrôles de circuits VLSI - Application au coprocesseur arithmétique
FELIN
EPFL - Lausanne - Switzerland

BERGER-SABBATEL G.
Machines spécialisées et programmation en logique
CNRS - TIMA Laboratory - Grenoble
Next : LGI Laboratory - Grenoble

MICOLLET D.
Etude de la contrôlabilité de circuits intégrés par faisceaux d'électrons
University of Dijon
Next : GERE Laboratory - Dijon University
MOISAN F.
Optimisation du contraste image en microscopie optique (application à l'inspection microélectronique)
Direction des Constructions et des Armes Navales (DCAN) - Brest

HORNIK A.
Contribution à la définition et à la mise en œuvre de NAUTILLE
Thèse de Doctorat INPG - Juin 1989
APRIS - Meylan
Next : BULL - Echirolles

DARLAY F.
Contribution au test des circuits intégrés CMOS : étude du test des pannes stuck-on et stuck-open
Thèse de Doctorat INPG - 20 novembre 1989
EPFL - Lausanne - Switzerland
Next : Ecole Polytechnique de Montréal, Canada
Next : SGS Thomson, Grenoble

NORAZ S.
Application des circuits intégrés autotestables à la sûreté de fonctionnement des systèmes
Thèse de Doctorat INPG - 20 décembre 1989
MERLIN GERIN - Meylan

BONDONO P.
Contribution à NAUTILLE : un environnement pour la compilation de silicium
Thèse de Doctorat INPG - 8 décembre 1989
IBM - Corbeil

JERRAYA A.
Participation à la compilation de silicium et au compilateur SYCO
Thèse d'Etat - 19 décembre 1989
CNRS - TIMA Laboratory - Grenoble

TORKI K.
L'autotest intégré dans un compilateur de silicium
Thèse de Doctorat INPG - 12 juillet 1990
CMP - Grenoble

PIRSON A.
Conception et simulation d'architectures parallèles et distribuées pour le traitement d'images
Thèse de Doctorat INPG - 4 mai 1990
CENG Division LETI - Grenoble

SAVART D.
Analyse de défaillance de circuits intégrés VLSI par testeur à faisceau d'électrons
Thèse de Doctorat INPG - 27 juin 1990
IMAGERIE INFORMATIQUE - Grenoble

BALME L.
Habilitation à diriger des recherches. 21 mai 1990
On secondment to SGS, Geneva, from 1.1.1991
Next : TIMA Laboratory
CHAUMONTET G.
Etude de faisabilité d’un micro-contrôleur de très haute sécurité
Thèse de Doctorat INPG - 26 octobre 1990
Centre de Compétence en Conception de Circuits Intégrés (C4I), Archamps

MARZOUKI M.
Approches à base de connaissances pour le test de circuits VLSI : application à la validation de prototypes dans le cas d’un test sans contact
Thèse de Doctorat INPG - 6 février 1991
CNRS - TIMA Laboratory - Grenoble

CONARD D.
Traitement d’images en analyse de défaillances de circuits intégrés par faisceau d’électrons
Thèse de Doctorat INPG - 11 février 1991
INFI Society (ARM Group) - Paris

COURT T.
Conception d’une famille de coprocesseurs parallèles intégrés pour le traitement d’images
Thèse de Doctorat INPG - 9 décembre 1991
I2S, Bordeaux

COLLETTE T.
Architecture et validation comportementale en VHDL d’un calculateur parallèle dédié à la vision
Thèse de Doctorat INPG - 14 septembre 1992
CEA/LETI/DEIN - Gif sur Yvette

CASTRO ALVES V.
Modélisation de pannes et algorithmes de test pour mémoires RAMs multi-port
Thèse de Doctorat INPG - 10 décembre 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble
Next: Lecturer at Aveiro University - Portugal
Next: Professor at UFRJ - Rio de Janeiro - Brazil

JEMAI A.
Etude d’un processeur RISC pour un système symbolique parallèle
Thèse de Doctorat INPG - 22 juin 1992
Teaching and Research Assistant (ATER) at TIMA Laboratory - Grenoble
Next: ENSI, Tunis, Tunisia

PARK I.
AMICAL : un assistant pour la synthèse et l’exploitation architecturale des circuits de commande
Thèse de Doctorat INPG - 3 juillet 1992
DAS/ETRI, Daejon, Research Laboratory in Korea

BOURAOUI R.
Calcul sur les grands nombres et VLSI : application au PGCD, au PGCD étendu et à la distance euclidienne
Thèse de Doctorat INPG - 15 janvier 1993
Bell Northern Research (BNR), Ottawa, Canada
Next: Plaintree Systems Inc., Stittsville, Ontario, Canada
O'BRIEN K.
Compilation de silicium : du circuit au système
Thèse de Doctorat INPG - 31 mars 1993
LEDA S.A., Meylan, France

KUSUMAPUTRI-HORNIK Y.
Opérateurs arithmétiques standards en-ligne à très grande précision
Thèse de Doctorat INPG - 11 mai 1993

BEN OTHMAN M.
Évaluation d'une hiérarchie mémoire pour une machine symbolique
Thèse de Doctorat INPG - 8 septembre 1993

VAUCHER Ch.
Le test haute résolution de circuits imprimés nus
Thèse de Doctorat INPG - 25 novembre 1993
IMD, Grenoble, and TIMA Laboratory

HAMDI B.
Outils CAO pour la génération automatique de parties opératives auto-contrôlables
Thèse de Doctorat INPG - 18 Avril 1994

AICHOUCHI M.
Étude des liens entre la synthèse architecturale et la synthèse au niveau transfert de registres
Thèse de Doctorat INPG - 20 juin 1994

LUBASZEWSKI M.
Le test unifié de cartes appliqué à la conception de systèmes fiables
Thèse de Doctorat INPG - 20 juin 1994
Professor at the UFRGS, Porto Alegre University, Brazil

KEBICHI O.
Techniques et outils de CAO pour la génération automatique de test intégré pour RAMS
Thèse de Doctorat INPG - 15 juillet 1994
Engineer/researcher at TIMA Laboratory - Grenoble

KOLARIK V.
Techniques avancées de test de circuits analogiques et mixtes analogiques-numériques
Thèse de Doctorat INPG - 31 octobre 1994
Next : University of Brno, Czech Republic

BEDERR H.
Contribution à la conception en vue du test d'opérateurs à structure itérative
Thèse de Doctorat INPG - 23 novembre 1994
Post-Doctoral position at AT&T Bell Laboratories, Princeton, USA

VERGUIN P.
Industrialisation d'une méthode de localisation de défauts sur circuits intégrés par cristaux liquides
Thèse de Doctorat INPG - 20 décembre 1994
"Professeur des Ecoles"
VIII.2 Press articles in 1994-1995

In the following are collected copies of articles that appeared in Newspapers in 1994-1995.
Summary

- European Design And Test Conference'95
  ELECTRONIC DESIGN
  6 March 1995

- Laboratorul TIMA din Grenoble - un posibil model al cercetarii stiintifice
  UNIVERS INGINERESC Nr. 5 (Romania)
  1995

- La bonne réflexion
  CHAMBRE DE COMMERCE ET D'INDUSTRIE DE ST ETIENNE-MONTBRISON
  Transfert de Technologie et de savoir-faire
  1994

- Calitatea in Europa
  UNIVERS INGINERESC Nr. 23 (Romania)
  1994

- "Service, A Low Cost IC Prototyping Service and A Report on the Workshop Conducted"
  IME SINGAPORE NEWSLINK Vol. 1 no 2
  October/December 1994

- GaAs deal adds libraries
  ELECTRONIC TIMES
  17 November 1994

- Eesti vajab mikroelektroonikat
  ÄRIPÄEV (Estonia)
  24 August 1994

- Le test électrique à 100 % divise par 10 le coût de réparation
  ELECTRONIQUE INTERNATIONAL n° 144
  9 June 1994

Hubert CURIEN, Minister for Research and Technology, in Grenoble in 1986 (Daniel BLOCH, Chairman of INPG, presently Chairman of UJF).
• Grenoble accroît sa recherche en électronique
  ELECTRONIQUE INTERNATIONAL n° 143
  2 June 1994

• DISZDOKTOROK
  NEPSZABADSAG (Hungary)
  31 May 1994

• La CAO et le test attirent les foules
  ELECTRONIQUE INTERNATIONAL n° 131
  10 March 1994

• What could be better than a trip to Paris?
  ELECTRONICS TIMES n° 714
  10 March 1994

• Darringer urges EDA collaborations
  ELECTRONICS TIMES n° 713
  3 March 1994

• Première manifestation européenne dédiée CAO et test
  ELECTRONIQUE INTERNATIONAL n° 120
  24 February 1994

• Designs on Europe
  ELECTRONICS TIMES n° 703
  3 February 1994
European Design And Test Conference '95

The Practical Side Of Design, Test, And ASIC Technologies Are Covered With A Distinctly European Flair At The Second ED&TC In Paris.

JOHN NOVELLINO

The European Design & Test Conference and Exhibition enters its second year with a stronger emphasis on more applications-oriented presentations. Its goal is to serve both industry- and academic-oriented attendees with the latest information on advances in the design and test of electronic circuits.

The ED&TC will be held Mar. 6-8 at the CNIT Conference and Exhibition Center in Paris, site of last year's event, which combined the former European Test Conference, European Design Automation Conference (EDAC), and Euro ASIC Conference. Conference officials cite last year's attendance, with more than half of the participants coming from outside France, as evidence of the conference's success.

A total of 136 papers are scheduled for presentation in 41 sessions, with another 28 to be displayed in the poster session. Topics cover the gamut of design and test issues, including digital and system simulation, system synthesis, sequential logic synthesis, mixed-signal design-for-test, built-in self-test, quiescent-current (DPM) testing, FPGAs, multimedia, and circuit partitioning. Three panel sessions will feature industry experts discussing the change from traditional to more open-architecture automatic test equipment (ATE), simulation versus formal verification, and the effect of mixed-signal technology on the European microelectronics industry (see the table).

"I think the conference has certainly established itself as an international event," says general chair Tony Ambler, professor of test technology at Brunel University, Uxbridge, United Kingdom. "But we have been focusing more strongly this year on attracting the more industrial- and applications-oriented type of paper." He specifically highlights the User Forum sessions, a separate track of papers to be presented in parallel with three other more academically oriented tracks.

Attendees should notice the more practical nature of the User Forum presentations. "We set up slightly different criteria for acceptance of these papers," notes Ambler. "We definitely didn't look for sales pitches. We looked for those people in industry who have something useful and interesting to say that the attendees would like to hear, but who don't have quite the time to put together the more rigorous scientific style of paper."

The User Forum papers will be published in proceedings separate from that containing the other session papers. Ambler said this arrangement allowed the User Forum papers to be printed locally with a two-month later deadline for authors. The result isn't only more applications-oriented material, but also more timely information that should better serve the industry-based attendees, he says.

A User Forum on IPDQ and QTAG (the Quality Test Action Group) is a good example, says Ambler. "This particular session is aimed at industry people rather than the more academical attendee: What will it mean for you in terms of..."
practical realities? What sort of ATE will it be? You can start using it and what will be the benefits for you?"


In keeping with the conference's three-part charter, a trio of keynote speakers will address issues in CAD, testing, and semiconductors. William Lattin, senior vice president for corporate marketing at Synopsys, will lead off, discussing "Modeling, the key to design reuse." His talk will focus on design reuse as the cornerstone of future semiconductor markets, such as embedded processors and other areas where the protection of intellectual property is important. Further merging of modeling and design reuse will occur as design complexity continues to increase, according to Lattin.

<table>
<thead>
<tr>
<th>Date</th>
<th>Time</th>
<th>Room A</th>
<th>Room B</th>
<th>Room C</th>
<th>Room D</th>
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<tbody>
<tr>
<td>Monday Mar. 6</td>
<td>9:00-10:30 A.M.</td>
<td>High-level synthesis (tutorial)</td>
<td>Programmable-logic technologies, architectures, and trends (tutorial)</td>
<td>Mixed-signal test (tutorial)</td>
<td>Design and test of MCMs (tutorial)</td>
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<td>2:00-3:30 P.M.</td>
<td>VHDL-A: Concepts and constructs of the analog extension to VHDL (tutorial)</td>
<td>Focal testing of VLSI circuits (tutorial)</td>
<td>Test synthesis: The practicality of DFT (tutorial)</td>
<td>Low-power design: Clocked or asynchronous control? (tutorial)</td>
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<td>4:00-5:30 P.M.</td>
<td>Session 1A: DSP and multimedia</td>
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<td>Tuesday Mar. 7</td>
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<td>Session 2A: Circuit positioning</td>
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<td>4:00-5:30 P.M.</td>
<td>Session 2A: Circuit positioning</td>
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<td>Wednesday Mar. 8</td>
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<td>2:00-3:30 P.M.</td>
<td>Session 5A: Digital and system simulation</td>
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<td>4:00-5:30 P.M.</td>
<td>Session 6A: CAD frameworks</td>
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<td>Thursday Mar. 9</td>
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<td>2:00-3:30 P.M.</td>
<td>Session 9A: Design methodologies</td>
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<td>4:00-5:30 P.M.</td>
<td>Session 10A: Hierarchical layout</td>
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<td>2:00-3:30 P.M.</td>
<td>Session 1A: New applications of analog simulation algorithms</td>
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<td>4:00-5:30 P.M.</td>
<td>Session 1A: New applications of analog simulation algorithms</td>
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CONT'D
Jean-Philippe Dauvin of SGS-Thomson Microelectronics, France. Dauvin will discuss bICMOS semiconductor market trends. He notes that the sharp recovery of the last two years was driven by factors that also will affect the industry's future. Although we are in the same cycle, the upswing seems to be leveling off, he says, and future cycles will be less pronounced.

Much of the recent growth in the semiconductor market was due to technological progress, which was linked to the rapid increase in the semiconductor content of systems, says Dauvin. This trend will continue, he predicts, with semiconductors rising from 14% of total value of systems to 20% by the year 2000.

The European market is regaining momentum, says Dauvin, with new products like cellular telephones allowing the continent to maintain its 18%-20% share of the worldwide sales of semiconductors. Lastly, Dauvin points out that investment by semiconductor manufacturers totaled nearly $2 billion last year, representing almost 20% of sales. Manufacturers must continue to invest between $700 and $800 million a year to be successful in the semiconductor market, he concludes.

Along with the technical sessions, the conference's organizers have put together an interesting set of eight tutorials, scheduled for Monday, March 6. Each is three hours long, and one day allows attendance at a morning and an afternoon session.

One tutorial deals with a particular hot topic for designers of portable equipment. In "Low-power design—clocked or asynchronous control," S.B. Furber of the University of Manchester, United Kingdom, will question the use of globally clocked circuits and make a case for asynchronous control as a power-saving technique. Although asynchronous design is considered hard to design and test, Furber will present information on recent advances that have eased design problems and made asynchronous logic feasible for large-scale circuits.

Designers working on analog and mixed-signal circuits may find "VHDL-A: Concepts and constructs of the analog extension to VHDL" of value. This tutorial, presented by J-M Berge, France Telecom-CNRT, Grenoble, and A. Vachonx, of the Swiss Federal Institute of Technology, will discuss the status of the VHDL-A standardization process and the U.S. Department of Defense architecture documents. The session will then describe how VHDL-A can fit into a global design methodology. Included in the tutorial will be examples of applications involving signals in both the time and frequency domain.

With mixed-signal circuitry growing more common, it's only fitting that the conference includes a tutorial on "Mixed-signal test" by J.A. Abraham of the University of Texas at Austin. The tutorial will address the key issues in developing high-quality manufacturing tests for mixed-signal circuits and design-testability techniques. The discussion will include appropriate fault models and ways to construct fault models in a hierarchical fashion. Abraham will also present a brief section on the forthcoming IEEE-1149.4 mixed-signal test bus standard. Some possible approaches to building in self-test implementations will be shown, along with case studies and examples.

S. Trimberger of Xilinx Corp., San Jose, Calif., notes that rapidly improving FPGA technology has made these devices the most popular technology for implementing complex ASICs. Trimberger's tutorial, "Programmable logic technologies, architectures, and trends," covers four areas of FPGA technology.

First, it discusses implementation techniques and how they affect design capabilities. Then it goes onto major commercial FPGA architectures and their advantages and disadvantages. The third area involves FPGA software from a design-flow point of view. Lastly, Trimberger presents applications issues, which include the difference between FPGA and traditional ASIC design and innovative uses for the arrays.
Laboratorul TIMA din Grenoble - un posibil model al cercetării științifice

Ioan C. Bacivarof
Universitatea "Politehnica" București

În contextul dezvoltărilor - fiecare pentru această perioadă de tranziție - privind perspectivele cercetării științificeurmatoare și modalitățile de organizare și finanțare a acesteia, credem că nu este lipsită de interes prezentaerea uneia dintre unitățile de elita ale cercetării științifice din Franța: laboratorul TIMA din Grenoble, la activitățile căruia am avut prilejul să participe în mai multe rânduri în cadrul unor proiecte educaționale și de cercetare științifică ale Uniunii Europene. Se știe că Franța este una dintre țările care se află în topul cercetării științifice mondiale (local 14, după Japonia, S.U.A. și Germania), atât când anum. ca. 2,5% din PIB în acest scop; conform unei statisticile recente, 51% din resursele necesare cercetării științifice franceze provin din fonduri publice, iar restul din sectorul privat.

Situat în piurea onă Grenoble, importanța universitară și considerată ca unul dintre poli cercetării științifice în domeniul ingineriei din Franța (al doilea ca importanța după Paris), laboratorul TIMA (Technici ale Informatiei ale ale Microelecnței pentru Arhitectura de calculatoare) are o dublă abordare, fiind așa de tehnologic și de organizator de național francez în domeniul cercetării științifice, Centre National de la Recherche Scientifique (CNRS), c/- și principalelor universități din Grenoble (Institut National Polytechnique și Université Joseph Fourier). Este o soluție eficientă, dezvoltată în urma unui proces economic, ocazii că permit să valorifice semnificativ perioadele de cadrul de studii aprofundate (DEA), pentru soluționarea unor teme de cercetare științifică de vârf.

Laboratorul TIMA are o tradiție de peste 20 de ani în cercetarea științifică de înainte, fiind la oarecare structură în sânturi grupuri de cercetare, acestea:
- Centrul teoretic al sistemelor integrate complexe (coordonator: prof. Dr. Louis Balcan);
- Proiectarea sistemelor integrate (coordonator: prof. Dr. Alain Guyot);
- Sisteme integrate fiabile (coordonator: dr. Michael Nikolaidis);
- Sisteme la nivel sistem (coordonator: dr. Ahmed Jerrajay);
- Metode de testare avansate (coordonatori: prof. Dr. Bernard Courtois și dr. Marcelo Lubaszewski);
- Diagnoza sistemelor complexe (coordonator: dr. Meryem Morozouki).

Vom încerca în ceea ce urmează să descriem câteva dintre acestea:

* Ancoarea activității în domeniul prioritar ale cercetării științifice aplicative europene și mondiale, cum sunt proiectarea asistată de calculatoare a sistemelor electronice complexe și în principal a circuitelor VLSI, calitatea și siguranța în funcționarea, inclusiv soluția sistemelor tolerante la defecte, testarea și diagnoza tehnice; aceasta a fost posibilă prin finanțarea cercetărilor laboratorului, în proporție de 60%, prin intermediul contractelor cu partenerii industrii importanți (SGS Thompson, France Telecom, Aereospațiale etc.).

* Competența managerială - dar mai ales științifică - a eșecul coloane, la rândul lor personalități științifice bine cunoscute în domeniul lor de activitate: este suficient să menționăm în acest sens că profesor Louis Balcan este coordonatorul programului european în domeniul calității sistemelor complexe - EPQCS, dr. M. Nicolaidis este președinte al comitetului IEEE Computer Society în domeniul testării etc.,

* Participarea activă (prin comiteturi sau prin conducerea de secțiuni sau grupuri de lucru) la toate reuniunile științifice naționale și internaționale importante în domeniul a diferitelor și TIMA, ca modalitate a de a face cunoscute cercetările proprii, dar și de a stabili contacte benefice pentru colaborația fără vreun al laboratorului.

* Larga desfășurare a TIMA spre cooperare științifică și educațională, aceasta fiind prezentă nevoia de soluționare a unor teme de anvergură. Este semnificativ faptul că această cooperare s-a îngrijit adesea prin împărtășirea de într-un domeniu de cercetare (existând cooperare cu universitățile și centre de cercetare vest-europene, în cadrul unor proiecte europene comune - ES-PRI dự COMETI - sau acorduri bilaterale cu universitățile americane), ceea ce în ultimul an, cu universitățile din țările europene și mondiale (cadrul unor programe europene comune ca PEFO, COPERNICUS, TEMPUS s.p.)

Ceea ce înseamnă că acea laboratorul TIMA este eficienta deosebită a activității integrului colectiv, de la coordonatorul acestuia și până la secundarele poziții și bine cunoscute ale tehnicii de procesare și transmitere electronice și informației, laboratorul funcționând asemeni unui angajăm ent bine pus la punct, în care nici o activitate nu este gratuită sau formală; dar, mai ales, vremea remarcabilă cultivării, fără a se face însă rabat disciplinarie, a unei atmosfere de încredere, cooperare și armonie, care face ca fiecare membru al laboratorului să se simță ca fiind o "mare familie"; reuniunile anuale ale TIMA, ca și activitățile sociale comune, sunt numai o fațetă a acesteia. Este și aceasta unul dintre secretele reușite...
LA
BONNE
REFLEXION

CARTE MIROIR STANDARD IMD
Interface de prise d'informations par contact sur les cartes électroniques pour le test des circuits imprimés nus, et en particulier les circuits pour les technologies CMS. Le système est compatible avec tous les testeurs existants.

L'ENTREPRISE
IMD, PMI d'une trentaine de personnes de la région parisiennne, spécialisée dans la réalisation d'outillages de test des cartes électroniques.

LE LABORATOIRE

LE TRANSFERT DE TECHNOLOGIE
Après une enquête de besoins de tests pour les circuits imprimés CMS, le TIM étudie et conçoit une maquette d'interface testeur-circuit. Il recherche ensuite un partenaire industriel. La société IMD saisit cette opportunité de diversification et crée une entité à Grenoble pour le transfert de technologie et l'industrialisation du nouveau produit.

RETOMBÉES
• avance technologique sur la concurrence dans le domaine du test
• diversification
• ouverture d'un marché mondial sans concurrence sur ce type de produit
CALITATEA ÎN EUROPA

...
A Service, A Low Cost IC Prototyping Service and A Report on the Workshop Conducted

In June 1994, the VLSI department of IME launched Alpha Service, a low cost fabrication service for integrated circuit (IC) prototyping. The service was established to address the need for IC prototyping especially by the institutions in Singapore for research and teaching purposes. The cost of IC prototyping is reduced through sharing the total cost of fabrication across a number of designs.

Services similar to Alpha Service can be found operating in the developed countries. MOSIS in the United States, CENP in France and MIPC in Australia are some of the better known operations. For MOSIS, it was reported that within the first three years of its operation since it was started in 1981, about 2,000 ICs of various complexities from tertiary institutions, research laboratories, and government contractors were fabricated. Such services provide economical route for silicon prototypes of designs to be realised. As such it is often used to train engineers, prove research ideas, and realise IC prototypes of systems.

For Alpha Service, IME acts as a co-ordinator for liaising with companies and organisations providing services needed to fabricate integrated circuits, collating designs from various sources, and pre-processing of the design data collated for IC fabrication. Alpha Service shields users from the complex communication interfaces of companies and organisations providing mask making, wafer fabrication and die packaging services. In order to overcome the problems of securing non-frequent low-volume IC fabrication from silicon foundries with busy schedules, Alpha Service uses multiple sources of support services to obtain IC fabrication.

To coincide with the launch of Alpha Service, a five-day workshop on Alpha Service and VLSI Design for tertiary institutions and statutory bodies was conducted on 16 June 1994 to brief participants about the service and IC design methodology. The workshop was aimed at providing the participants with the necessary design process capabilities to undertake designs in CMOS technology using commercial CAD systems.

The workshop was well received by all the six tertiary institutions and a couple of statutory bodies in Singapore. The participants of the workshop were: Centre for Wireless Communication, Defence Science Organisation, Nanyang Technological University, Nanyang Polytechnic, National University of Singapore, Ngee Ann Polytechnic, Singapore Polytechnic, and Temasek Polytechnic. Altogether, 21 participants attended the workshop.

On the first day, four VLSI technical staff gave lectures on Alpha Service, CMOS process, custom IC design process methodology, and VLSI design with CAD Tools. On subsequent days, the participants were taken through the various components of IC design process, namely schematic capture and simulation, layout and verification, module integration and padding. A simple kitchen timer design was made available to the participants as a workshop project.

The documentation for using the Alpha Service process is available. In addition, the technology files for Alpha Service process are supported for major commercial IC CAD systems. Currently, Alpha Service supports 1.2µm Double Metal Double Poly n-well CMOS process. On the packaging side, Alpha Service supports 28 and 40 DIL packages. The support for more advanced processes and higher pin count packages will be considered if certain level of demand exists.

For further information on Alpha Service, please contact Tan Chong Hoo at 249-7745 or E-mail: alpha@caronas.ime.gov.sg.
GaAs deal adds libraries

European designers will have access to another gallium arsenide technology through a deal between US GaAs design house, Compass Design Automation, and CMP, the French chip prototyping service.

Systems & Processes Engineering of Austin, Texas, has ported its GaAs libraries for Vitesse's HIGaAs III process to Compass tools.

For Fr17 000 (£2085), universities or small companies get 'phantoms' of the libraries without the physical data. For a further £330 per sq mm, users will then get five packaged chips and 20 die from one of the six wafer runs which CMP plans a year.
Eesti vajab mikroelektroonikut

RAIMUND ÜBAR TTÜ Elektroonika Kompetentsuskeskusühing

Maailmamüüjad eeldavad, et mikroelektroonika ja elektroonika kutsumus kasumises kasvab noorte ja täielikult suurendatud kasutusele otse on kolmekordises. Need eeldused on tõhusad, kuna mikroelektroonika ja elektroonika tehnoloogia suurkasutus raskestab kõik kutsumisele asendusele.

Nende eeldustest avati õppetööd ja muul tutvustavatele kursused ehitatud mikroelektroonikatehnikal. Mikroelektroonikatehnikal on tõhus võimalus töötada koos välja tehnikas ja tehnoloogias.

Mikroelektroonika toidab väikefirmad

Elektroonputustehnikas on muidu võimalik, et mikroelektroonika ja elektroonika tehnoloogia suurkasutus kasvab noorte ja täielikult suurendatud kasutusele otse on kolmekordises. Need eeldused on tõhusad, kuna mikroelektroonika ja elektroonika tehnoloogia suurkasutus raskestab kõik kutsumisele asendusele.

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Keskus vahendab informatsiooni

TTÜ juures loodud Elektroonika Kompetentsuskeskus on olnud vahendaja teelt kasutades ülikoolide kaudu. Taiinates Eestis on see keskkond, kus ülikoolitehnikad võivad ise teha tehnoloogia arendamist.

Keskus vahendab disainimise tarkvara


Mikroelektroonika disainimise tarkvara

Keskus vahendab disainimise tarkvara, mida võib kasutada mõningat disainimist.
CIRCUITS IMPRIMÉS

Le test électrique à 100% divise par 10 le coût de réparation

Aujourd'hui, les circuits imprimés à pas fins ne sont pas testés à 100%. Résultat, beaucoup de cartes neuves sont envoyées au câblage alors qu'elles sont défectueuses, et cela coûte très cher. Il existe pourtant des solutions.

Actuellement, les fabricants de circuits imprimés utilisent 100% de leurs produits, sans les cartes imprimées, mais seule une partie est testée à 100%. Résultat, entre 5% et 10% des cartes qui sortent de l'atelier sont non testées. L'association française de l'étiquette de code de contrôle (AVEC) a cherché à améliorer la situation, en testant les cartes imprimées à 100%.

La solution proposée consiste à utiliser un système de test automatisé, appelé "test de circuit imprimé" ou "TIC" (Test In Circuit). Ce système permet de tester toutes les connexions d'une carte imprimée, y compris les connexions internes, en un temps très court.

Dans le cas des cartes imprimées, les circuits imprimés sont testés en utilisant des cartes de test spécifiques qui contiennent des connexions de test prédéfinies. Ces cartes de test sont connectées aux cartes imprimées avant l'assemblage, et le système de test est utilisé pour tester toutes les connexions de la carte imprimée.

Les résultats de ces tests sont ensuite analysés par un logiciel qui génère un rapport détaillé de tous les problèmes de connectivité identifiés. Cette solution permet de réduire de manière significative le nombre de cartes qui doivent être testées à 100%, ce qui a pour effet de réduire le coût de réparation des cartes imprimées.

Les fabricants de circuits imprimés ont dû investir dans de nouveaux équipements de test, mais le rendement de ces équipements est très satisfaisant. En moyenne, une carte imprimée est testée en moins de 10 minutes, ce qui représente une économie de temps et de coût significative.

La solution proposée par l'AVEC permet de tester toutes les cartes imprimées à 100%, ce qui garantit une qualité de production accrue et une satisfaction renforcée des clients. Les fabricants de circuits imprimés peuvent ainsi offrir une garantie plus solide à leurs clients, en réduisant les coûts de réparation et en améliorant la fiabilité des produits finis.
Grenoble accroît sa recherche en électronique

Pour lancer des recherches pluridisciplinaires en électronique, une "fédération" de laboratoires naît à Grenoble. Thèmes retenus: composants de puissance, microsystèmes, véhicule électrique...

Grenoble est en cours de constitution une "fédération" de laboratoires de recherche en électronique qui, d'une façon pluridisciplinaire, va lancer de nouveaux thèmes de R&D. Baptisée Fédération MEGE-ATS (microélectronique, génie électrique, automatique, traitement du signal), la nouvelle structure résulte d'un accord entre le CNRS et l'Institut national polytechnique de Grenoble (INPG). Elle regroupera huit laboratoires de l'INPG (dont sept sont "Unités de recherche associées" du CNRS) — soit, au total, près de 600 personnes, dont 150 chercheurs et 280 thésards.

L'objectif, c'est de concentrer des moyens humains et financiers sur quelques axes de recherche prioritaires, explique Jean-Claude Girardet, l'un des animateurs de la nouvelle fédération. Sept axes ont été retenus: "microélectronique - technologie, conception et test" (cinq "labos" de la fédération travailleront sur ce thème, leurs travaux portant en particulier sur les composants de puissance haute température), "microsystèmes - capteurs, micro-actionneurs, intégration", "analyse de signaux et systèmes complexes", "communication et cognition", "automatique avancée des systèmes électriques", "modélisation et simulation numériques" et "véhicule électrique". Dans ce dernier domaine, les recherches s'orienteront essentiellement dans deux directions: la "chaîne de traction" et le "véhicule intelligent".

Conservant chacun sa personnalité propre, les huit laboratoires de la fédération consacreront à ces divers axes une partie de leurs travaux de recherche. Ces "labos" de l'INPG, parmi lesquels figurent en particulier l'Institut de la communication parlée et le "Tima" (Techniques de l'informatique et de la microélectronique en architecture), sont spécialisés notamment dans l'automatique, l'électrotechnique, l'électromagnétisme, les micro-ondes, l'optoélectronique, la physique des composants à semiconducteurs, le traitement des images et la reconnaissance des formes. Ils dépendent de trois écoles d'ingénieurs de l'INPG : l'Enserg, l'Ensieg et l'Ensimag.

Chacun de ces sept axes retenus par la Fédération MEGE-ATS comportera plusieurs projets de recherche. D'une durée de deux à trois ans, ces projets — décrits à Grenoble comme "cibles" — associeront en moyenne trois des huit "labos" concernés, ainsi que des partenaires extérieurs: industriels et/ou autres centres de recherche en électronique (on cite notamment à l'INPG le LAAS de Toulouse, l'IEEMN de Lille et l'Institut franco-allemand pour les applications de la recherche). Les premiers projets sont encore en phase de définition. Ils seront annoncés dans quelques mois.

Raphaël Font
DÍSZDOKTOROK. A Budapesti Műszaki Egyetem hetfőn díszdoktori címet adományozott a grenoble-i (Franciaország) Bernard Courtois professzornak a mikroelektronika terén, valamint Hans Lenknek, a Karlsruhei Egyetem Filozófiai Intézete professzorának a technikafilozófiai szaktudomány terén kimagasló tevékenységéért. Mindkét professzor rendszeres vendégelőadója a műegyetemnek.
LA CAO ET LE TEST ATTIRENT LES FOULES

Comme prévu, la première manifestation européenne dédiée à la conception et au test de circuits spécifiques a été très marquée par l’aspect CAO du problème.

Près de 650 participants aux conférences (+30 % par rapport à 1992) dont plus de deux tiers d’étrangers, 2700 visiteurs (en augmentation de 25 % par rapport à la précédente édition) ; le succès de la première manifestation européenne dédiée à la conception et au test de circuits spécifiques, ETC-EuroAsic-Edac, qui s’est tenue la semaine dernière à Paris, n’est pas un mythe. Les organisateurs ont donc décidé de reconduire l’événement sous sa forme actuelle, c’est-à-dire rassemblant ETC, Edac et EuroAsic et rebaptisé ETC’94 (European Design & Test Conference), en 1995 et les années suivantes. La manifestation devrait rester à Paris pendant encore plusieurs années (un, précise Jean-Pierre Tudi, président de la conférence cette année : "Pourquoi changer alors que nous sommes dans une logique de suivi ?")

Une ombre au tableau, l’appauvrissement de la partie conception de circuits proprement dite (notamment celle traitant de l’architecture des circuits spécifiques) ; les conférences ont, dans leur grande majorité, boudé l’exposition, et le nombre de visages de ces mêmes de ces dernières années, mais les nouveaux venus, essentiellement des concepteurs de circuits spécifiques, ne sont pas ceux qui promettrent les décisions d’achat. Tout cela paraît loin de l’optima de leur visite à EuroAsic. Il faut dire que ces derniers recherchent plus des outils pour aider dans leur travail que de nouvelles architectures de circuits. Or, de ce côté, ils ont été servis. Les principaux fournisseurs d’outils de CAO étaient devient de plus en plus floue. Peut-on en effet encore parler de microcontrôleur quand les approches qui sont maintenant mises sur le marché permettent d’indiquer à côté d’un noyau central classique une grande variété de fonctions périphériques et de mémoires définies au besoin par les utilisateurs ? A l’inverse, un circuit spécifique intégrant un cœur de microcontrôleur et de circuits spécifiques, n’est-il pas plus un microcontrôleur qu’un circuit spécifique ? Le débat reste ouvert. Cette table ronde a aussi montré que le thème de l’automobile, qui avait pu paraître à priori peu représentatif des problèmes de l’ensemble de l’industrie, est au contraire très exemplaire. Les ratios qui conduisent les fabricants du secteur automobile à adopter les circuits spécifiques sont les mêmes que ceux qui peuvent amener d’autres industries à s’y mettre : réduction des coûts, intégration, etc. Les problèmes sont les mêmes et les solutions passent dans les deux cas par l’établissement de relations de partenariat étroites entre les différents intervenants.

Bull a fait une entrée remarquée au salon EuroAsic avec des cellules sans équivalent sur le marché.

UN CIRCUIT SPÉCIFIQUE ATM POUR LES COMMUNICATIONS À 2,48 GBT/S

Le prix EuroAsic industriel, qui récompense chaque année la réalisation de circuit spécifique la plus originale présentée lors de la conférence, a été remis cette année à une équipe de concepteurs de téléphonie (ESPI) pour le développement d’un circuit destiné à un commutateur ATM fonctionnant à 2,48 GBT/s. Ce circuit, qui intègre 580 000 transistors sur une puce de 12,8x12,1 mm, a été réalisé en technologie CMOS 0,7 µm par ESPI ; il fonctionne à 70 Mhz. Au delà de ces performances, sa principale originalité réside dans la méthodologie de développement utilisée, une méthodologie mettant en œuvre les techniques les plus récentes dans le domaine de la conception de circuits spécifiques : description Verilog, simulation complète et intégration de dispositifs pour le test (EFT).

Le prix EuroAsic pour les universités a, lui, été remis à une équipe de chercheurs de l’INPG (Grenoble) pour le réalisation d’un processeur neuronal développée dans le cadre du projet Esprit GaiaTe. Ce circuit, destiné à des applications de reconnaissance optique de caractères, intègre quatre processeurs et un réseau d’appréciation formant un réseau de plus de 2000 neurones formels et 16 000 synapses. Avec la possibilité d’ester 80 millions de connexions par seconde, il peut reconnaître 3000 caractères par seconde à la fréquence de 50 Mhz. Ce circuit, qui intègre 330 000 transistors sur une puce de 80 mm2, a été réalisé en technologie CMOS 0,7 µm par SGS-Thomson.
What could be better than a trip to Paris? Last week, having failed to organize a fortnight’s holiday for two in the Bahamas—and because the Euroasic exhibition was taking place in the French capital—I went to Paris. I witnessed the coming together of Euroasic, the EDAC design conference and the ECT test conference in what promised to be a powerful combination of learned engineering and the commercial aspects of the design and test of components.

Held at the modern and well-appointed CNT centre at the Grand Place de La Défense at the end of the Metro line, the event had all the makings of a success. The organizers had aimed for 500 conference delegates and 2500 exhibition visitors. Reports suggest the academic conference was well attended but, to judge by the first day crowds, the exhibition must have struggled to meet its target.

The exhibition area was quite small, contained in a grid of four by five aisles, but the quality of exhibitors was high. In the field of EDA just about everyone was there: Cadence, Mentor, Viewlogic, Racal-Redac, Synopsys, Intergraph, Computer Design Automation, GenRad and a little company just starting out in the EDA market, Altim, the EDA sales and marketing arm of IBM.

Unfortunately, for a show named Euroasic, the ASIC vendors were much thinner on the ground. IBM Microelectronics was there, of course—IBM Microelectronics is everywhere at the moment. I also spotted NEC, Raytheon and Alcatel Moteu, but that was about it. Actel was the only FPGA or PLD manufacturer present, despite the fact that design tools for FPGA and PLD seem to be a major theme among the EDA vendors this year.

So where were the European ASIC vendors such as Philips, Siemens, SGS-Thomson, GEC Plessey Semiconductors and ESZ2? Do you remember ESZ2, don’t you?

Perhaps these companies feel that they have saturated the local market, that they know about most of the ASIC design starts or that, as local vendors, they will automatically be asked to bid for ASIC business in Europe. Or perhaps they feel that Euroasic is a parallel event. As one exhibitor told me: “It may have Euro in the title but it’s a French show.” However, that same exhibitor went on to say that his company treats it as such, and is very pleased with the results.

This serves to highlight the problems which still exist as companies, both indigenous and from other continents, try to take a European perspective. For example, we end up with two design automation events, both aspiring to be European but both taking place in France and running the risk of being seen as parochial.

Some people are already calling EuroDAC due to take place from 19-23 September in Grenoble, the SGS-Thomson show because of the company’s major presence in the area. There is an implication, too, that other companies may be less supportive than they were in the past. Already complaints are being heard that Grenoble is a difficult place to reach and the Germans won’t travel there.

It is important that these shows, and more importantly conferences like Euroasic and EuroDAC, continue, prosper and join the ranks of Electronica and Cebit as genuine European events. An effort needs to be made on all sides, including the European vendors, the organizers and the client communities which, at the moment, inhibit their engineers from travelling. Otherwise we Europeans will be yet again delegating ourselves to a secondary position behind the US and Japanese.

Healthy European shows and conferences may be the symptom rather than the cause of a healthy European industry. But the information flow and cross-fertilisation of ideas which come from these events are, undoubtedly, an important ingredient for success.
Darringer urges EDA collaborations

John Darringer, director of EDA at IBM Microelectronics, gave the keynote address at Euroasic in Paris on Tuesday. He stressed the importance of tool developers working with chip and system developers to maintain the innovation in EDA, citing IBM experiences with the PowerPC, large asics and memories.

Compass Design Automation said it had refined its FPGA design software with the launch of X-Syn, which allows HDL input to be synthesised using Xilinx's X-Blox library of functional modules.

The software is based on Compass's datapath synthesis technology, as used in asic and standard product design. X-Syn accepts VHDL and Verilog inputs and, by targeting the X-Blox modules, helps speed up design time by allowing simulation at the behavioural level.

Compass used the Prep suite of circuits to establish the benefits of X-Syn. However in the US a number of synthesis tool vendors are said to have rejected Prep's call for a synthesis benchmarking exercise.

John Miles, European marketing director of Synopsys, said: "We will not participate in the synthesis benchmarking exercise with or without Prep because we do not believe it is an effective way of communicating a tool's features, capability or performance to users."

Also at the show Altim, the EDA arm of IBM, demonstrated TestBench, an automatic test pattern generation tool, and LogicBench, a 'front-end' design suite which includes VHDL entry, simulation and logic synthesis. It also announced its three distributors for Europe. Vizef of High Wycombe, was confirmed as IBM EDA's value added reseller for Northern Europe. Misi has the same role for France and Microm for Germany, Switzerland and Austria. The design centre at IBM's Corbeil-Essonnes fab in France will provide engineering support.
Au Cnit de Paris la Défense, du 1er au 3 mars, se tiendront pour la première fois conjointement ETC, conférence européenne sur le test, EuroAsic, exposition-conférence européenne sur la conception de circuits spécifiques, et Edac, conférence européenne sur la CAO.

ETC-EuroAsic-Edac, qui réunira pour la première fois dans un même lieu, à Paris, les concepteurs de circuits spécifiques et les spécialistes de la CAO et du test, se veut la première (et la seule en Europe) manifestation dédiée à tous les aspects du développement d'un circuit spécifique dans son environnement système, de la conception au test final. Cette manifestation, qui sera reconduite en 1995, apparaît ainsi plus complémentaire que concurrente de l'autre conférence-exposition européenne: EuroDat.

ETC-EuroAsic-Edac regroupe un cycle de conférences scientifiques et techniques et une exposition. Ce sera l'occasion de faire le point sur les derniers développements dans le domaine concerné, en particulier sur les nouveaux outils de placement-routage automatique, de synthèse logique, sur les nouvelles méthodologies de conception, notamment en ce qui concerne la testabilité, et sur les méthodes pour la simulation de fautes et la génération de test. Les organisateurs attendent plus de 500 participants aux conférences et environ 2500 visiteurs à l'exposition, qui regroupera plus de 90 sociétés.

Malgré la présence de grands noms du semiconducteur comme IBM Microelectronics, NS et NEC, de fabricants de systèmes de test et de sociétés de conception, l'exposition EuroAsic sera cette année encore très fortement marquée par la CAO.

cont'd
UNE EXPOSITION TRÈS ORIENTÉE CAO

Malgré une légère augmentation du nombre des sociétés exposantes et représentantes, elles seront plus de 80 cette année (contre 50 en 1993) - et la présence pour la première fois d'un fournisseur d'équipements de test, le salon EuroAsic qui se tiendra au Cnit de Paris la Défense du 1er au 3 mars dans le cadre de la manifestation ETC-EuroAsic. L'exposition est organisée par les roulards de CAO électronique.

Deux des acteurs majeurs de la CAO, qui sont également les organisateurs de l'exposition, sont EDA et ETC. Si EDA, la conférence européenne sur la CAO électronique, EuroAsic l'exposition-conférence sur la conception de circuits spécifiques, et ETC, la conférence européenne sur le test, se tiennent conjointement au Cnit de Paris la Défense du 1er au 3 mars.

TC-EuroAsic EDA se veut la seule (et la première manifestation) européenne dédiée à tous les aspects de la conception électronique d'un circuit intégré, de la conception au test. En ce sens, préside Jean-Pierre Thad, de Bull, président de la conférence, "le plus important aspect de la conférence, notamment le développement d'horizons, ainsi que de la CAO, qui est un outil orienté CAO". Cette manifestation regroupe une exposition (voir article ci-contre) et un cycle de conférences.

En ce qui concerne le test, les présentations scientifiques et techniques se dérouleront cette année à Paris du 1er au 3 mars (l'association avec le test sera reconstituée en 1995 et la participation à cette année sera réservée aux enseignants de l'enseignement supérieur et de l'enseignement supérieur ainsi que de la CAO, de la conception et du test, et 34 représentatives de réalisations industrielles dans ce même secteur. Parmi les dix dernières figures, le plus récent concerne la simulation de circuits qui concourent, comme une année après l'autre, pour le prix EDA EuroAsic, avec notamment le circuit intégré le plus complexe jamais réalisé: il s'agit d'un microprocesseur avec antennes développé par Bull et l'intègre 5 mil-}

PREMIÈRE MANIFESTATION EUROPÉENNE DÉDIÉE CAO ET TEST

ions de transistors sur une puce). Dans la partie outils CAO, l'accent sera surtout mis sur la conception à haut niveau et les outils de vérification (avec, entre autres, la présentation du premier automate fonctionnel de l'Asil - voir encadré), mais des informations sur les derniers développements en matière de synthèse logique et d'automatisation du placement-routage feront aussi l'objet d'un certain nombre de présentations.

Une section spéciale pour les joueurs sur le thème de "l'assemblage par conception" sera dédiée à l'intégration de logiciels spécifiques et de logiciels de conception avec les outils de conception.

MODÉLISATION COMPORTEMENTALE ANALOGIQUE BASEÉE SUR LE VHDL

Modélisation comportementale analogique basée sur le VHDL

Analogue Electrical Engineering Software, spécialisé dans le simulation mixte, introduit la première version de son système de modélisation comportementale analogique, HDA, basé sur le langage VHDL et destiné à être utilisé avec son simulateur EDA. HDA est un système en code compilé. Les codes de description de matériaux analogiques et numériques sont tous deux compilés en C et reliés automatiquement. Selon la société, son système permettrait pour la première fois de déterminer de plus de deux composants analogiques et numériques, en utilisant le code VHDL, le tout au sein d'un même environnement. Les modèles ne sont pas limités au domaine électrique, mais supportent également les composants mécaniques, fluidiques, rotationnels, magnétiques et thermiques. HDA est également capable d'automatique développé par Bull et intégré 5 mil-

LE PREMIER ABSTRAITFUNCTIONNEL DISPLAY-OUT

C'est un autre exemple de la méthode "voir et vérifier" de VHDL, avec un certain nombre d'automations logiques et de représentations de circuits qui concourent, comme une année après l'autre, pour le prix EDA EuroAsic, avec notamment le circuit intégré le plus complexe jamais réalisé: il s'agit d'un microprocesseur avec antennes développé par Bull et l'intègre 5 mil-
Designs on Europe

At the end of this month three European events come together. A conference on design and test will be staged alongside the EUROASIC exhibition. Peter Clarke picks out conference highlights.

This year will see the merging of Europe's premier academic conferences on design automation (EDAC) and test (ETC) alongside the EUROASIC exhibition. The event takes place on 28 February to 3 March at the CNIT conference and exhibition centre, La Defense, Paris.

The exhibition is expected to attract over 60 exhibitor companies covering EDA, ASIC design, test and ATE. Companies set to attend include IBM EDA, Bull, GenRad, Synopsys, Hewlett-Packard, Texas Instruments and Alcatel Mietec. The European collaborative research organisation Essi is also set to show the results of projects in areas such as analogue design, EMC and frameworks.

The conference includes over 100 papers covering topics which include mixed-signal design, system-level synthesis, verification and test techniques. Three of the papers are highlighted here.
VIII.3 Social life

Recently, the Laboratory had the pleasure to congratulate some of its members for marriage and births.

Have got married:

- Lydie HEUSCH (SANZ), 25 May 1991
- Masaki NITO, 8 June 1991
- Mokhtar BOUDJIT, 13 June 1992
- Pascale VERQUIN (DULIEUX) 4 July 1992
- François MARTIN, 15 August 1992

The following will be descendants of Laboratory's members:

- Emeric AMIELH, 12 June 1991
- Luc BERGER SABBATEL, 13 July 1991
- Aurélie GARNIER, 7 September 1991
- Anna KOLARIK, 20 September 1991
- Florian HEUSCH, 2 November 1991
- Moussab BEN OTHMAN, 21 November 1992
- Thaís CASTRO ALVES, 2 October 1993
- Natasha LUBASZEWSKI 3 May 1993
- Aladin SKAF 2 August 1994
- Gabriel GARNIER 28 August 1994
- Andressa LUBASZEWSKI 11 December 1994

Some have even found their wife/husband in the Laboratory itself:


As for funds, the Laboratory has recurrent social events and exceptional social events. The mechouli's party is a traditional annual party. The Laboratory has been a few times horse-riding, even those being very beginners. Visitors are often taken for walks in the mountain. The following pictures are examples of this social life.
Picture 4: Horse-riding across Vercors
Picture 5: Annual party
Picture 6: Walk in the mountain with visitors: for example Janusz RAJSKI, Mc Gill University (1st plan, with a hat) and his family.

Picture 7: Skiing excursion
Picture 8: The TIMA football team (that beat CSI 5-0 in June 1992)