A capacitive DAC with custom 3-D 2-fF MOM unit capacitors optimized for low surface and low power SAR ADCs in 130nm STM technology

Members: M. Barragán, M. Diallo, D. Dzahini, S. Manakli, S. Mir, F. Pancher, E. Simeu

Cooperation: XDIGIT

Contract: PYXCAD — XDIGIT/TIMA Common Research Laboratory

Summary

A new custom 2-fF MOM unit has been proposed with low parasitic capacitances using 3 metal layers (M1, M2, M3) in technology STM 130nm. A 10-bit DAC has been designed using this type of units and the simulation results have shown improved linearity and dynamic performance. This DACs are used in a high-resolution ADC architecture.

1. Structure of capacitive DAC

The design of DACs based on standard MOM capacitance in technology STM 130nm has important constraints for our applications, such as pitch, area and consumption. A solution to overcome these constraints is the use of the designed 2fF unit that has low parasitic capacitances. A 10-bit DAC with this structure has been designed. Six layout versions have been studied to improve performance. Figure 1 shows the layout view of the 10-bit DAC version 0. The layout version 5 has been proposed to ensure good capacitor matching as shown in Table 1.

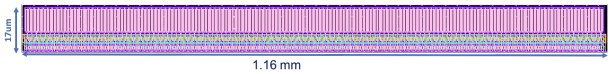

Figure 1. Layout view of the 10-bit DAC (version 0).

Type	Version	Long(mm)	Pitch(um)	Matching	Cp /C	INL max (LSB)	DNL max (LSB)
MOM (M3)	0	1.16	**17**	Correct	**2.4%**	**0.35**	**0.31**
MOM (M3) & MOM(M1,M2,M3)	1	**0.6**	**17**	Correct	**0.8%**	0.28	0.53
MOM (M3) & MIM	2	**0. 32**	**17**	Correct	**0.86%**	0.42	0.52
MOM(M2,M3) D	3	**0.54**	**17**	Correct	7.2%	**0.15**	**0.17**
MOM (M2,M3)	4	**0.54**	**17**	Correct	5.1%	**0.07**	**0.08**
MOM(M2,M3)	5	**0.51**	**17**	**Good**	6.1%	**0.23**	**0.24**

Table1. Comparison of the characteristics of six 10-bit layout versions.

2. Simulation results

Simulation results have been obtained with an RC extraction at 10 MHZ for a single channel (version 5) showing an improved performance with respect to previous designs.

2.1 Linearity and gain

Figure 2 shows the INL and DNL of the DAC. INLmax and DNLmax are smaller than 0.25 LSB. The variation of the reference voltage can be as high as 80mV. With these results, it is possible to obtain a 14-bit resolution in the target hybrid ADC architecture.

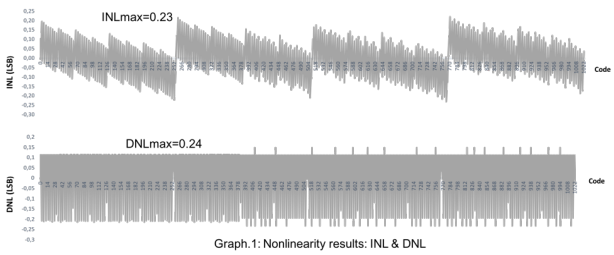

Figure 2. INL and DNL of the 10-bit DAC.

The performance of the circuit depends on the total parasitic capacitance. The proposal solution of custom MOM capacitors reduces this parasitic capacitance that determines the error gain. In this case the value of error gain is 6.7%.

2.2 Frequency behavior

A structure based on PMOS switches has been considered to obtain a low reference voltage variation of 80mV. The transistors are sized to have a correct settling time up to 125 MHZ. Table 2 shows the values of INL and DNL from 10 MHz to 200 MHz obtained from post-layout simulations with extracted parasitic capacitors.

Fréquence (MHZ)	INL max (LSB)	DNL max (LSB)
10	0.23	0.24
20	0.23	0.24
50	0.22	0.23
100	0.23	0.27
125	**0.39**	**0.39**
200	1.92	1.92

Table 2. INL and DNL from 10 MHz to 200 MHz

2.3 Crosstalk

Six methods have been proposed to minimize the crosstalk effect illustrated by means of 3 channels in Figure 3.

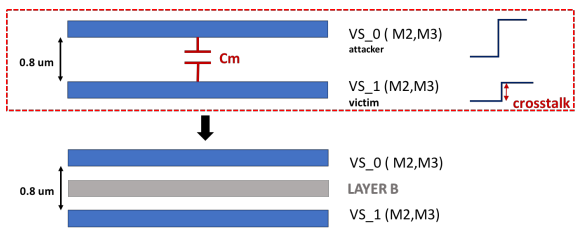

Figure 3. Crosstalk effect.

Table 3 shows post-layout simulation results to quantify the crosstalk effect due to the coupling capacitance from neighboring channels.

LAYER B	TYPE	INLmax (LSB)	DNLmax (LSB)	Er. Gain (%)	$\Delta Vref$ (mV)	LSB (uV)	Crosstalk (LSB)
M1	GND	0.23	0.24	11.03	80	78	20.6
M1	FLOT	0.24	0.24	10.73	80	78	20.6
M1,M2,M3 (disc)	GND	0.24	0.25	12.65	80	78	6.86
M1,M2,M3 (disc)	FLOT	0.25	0.24	11.3	80	78	7
M2,M3 (c)	GND	0.23	0.25	11.36	80	78	0.001
M2,M3 (c)	FLOT	0.22	0.25	8.28	80	78	0.001

Table 3. INL, DNL, gain error and crosstalk effect with different shielding options.

According to these results, the continuous shielding with metal M2 and M3 is the best method to limit the effect of crosstalk. Metal can be floating to ensure the best gain error of 8.23 %.

Conclusion

The 10-bit DAC presents the required characteristics for its use in a 14-bit SAR ADC. Others DAC structures with MIM capacitances will be studied in the future.

Experimental test bench for the characterization of MASSAR ADC

Members: M. Barragán, M. Diallo, D. Dzahini, S. Manakli, S. Mir, F. Pancher, E. Simeu

Cooperation: XDIGIT

Contract: PYXCAD — XDIGIT/TIMA Common Research Laboratory

Introduction

The Applicos test equipment is an industrial flexible set of instruments optimized for testing converters (ADCs and DACs). It is composed of several racks including power supplies, reference voltage generators, input signal generator and input/output interface. A dedicated software application has been developed following the specifications of the MASSAR converter. This tool is constantly improved following the characterization needed for the different versions of the MASSAR test chips and depending also on different applications targeted by Xdigit with MASSAR chips. This tool controls each element included in the Applicos test bench, for signal generation and data processing to display the final values of each parameter needed.

1. Testing methodology

Our testing methodology requires the generation of a high-resolution ramp as input signal for the ADC under test. The ADC samples the input signal and produces a corresponding digital output code. Each step of conversion is repeated many times to produce a DC transfer characteristic taking advantage of noise averaging facilities.

A complete full range testing, taking into account all significant bits, leads to the acquisition of tens of millions of samples per ADC channel (the present version of MASSAR circuit includes 32 ADC channels), which requires hours of acquisition. This test application software controls all the set-up for a full test campaign. In the near future the test bench will work in an autonomous mode for the data acquisition period which can last several hours or days before switching off automatically. Log files including both raw data and processing results are stored allowing further analysis.

2. Data analysis

During the test execution and after its completion, the software displays several graphs for the analysis of the acquired data:

- Full raw data. A transformation from 15 to 14 bits can be applied for each acquired data set.
- An average value is processed for each step in the transformation from 15 to 14-bit raw data sets. About 1000 values are acquired for each step.
- A Root Mean Square value is calculated for each step, taking into account all acquired data for each step. Many RAW data files can be merged to allow accurate mean and RMS values extraction.
- For each step, the minimum and maximum values of the distribution are provided as well.

A histogram of the number of occurrences for each digital value is obtained and a linear fit curve $y = ax + b$ is calculated using the average values. Then the INL is calculated $(INL = current\ average\ value - current\ FIT\ value)$ and the Min and Max values displayed in a window.

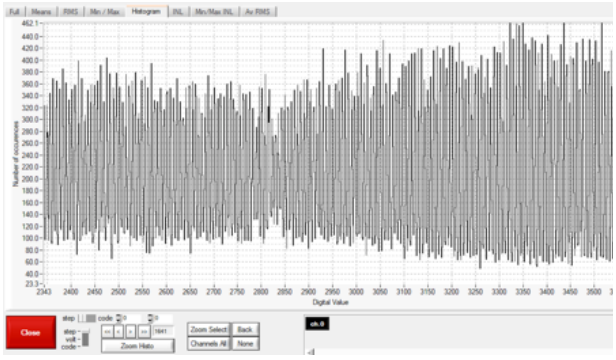

Figure 1. Histogram of ADC values.

Conclusion

This specific software for ADC test application is currently working and was successfully used in 2019 to fully characterize two versions of MASSAR chips. The test chip provided by Applicos and based on the AD9244 was also successfully checked with the application. Even if the application was initially designed to be as modular as possible, mainly by the use of a configuration file that can be saved or loaded from the test application, several code modifications of the test application will be required for the evaluation of future versions of MASSAR chips.