Call for applications - PhD candidate

Test and Reliability of Emerging Memory-based Spiking Neural Networks

Location: TIMA Laboratory *(AMfoRS team),* ***Grenoble, France***
Funding: *3-year PhD grant,* ***~1800€/month (brut)*** *– ANR research grant*
Starting date: *Autumn/Winter 2020*

Key-words: spiking neural networks, test, reliability, emerging memories

Context

The computing performance needed by emerging electronic applications (such as Internet-of-Things and Big Data analytics) is posing a serious challenge to current computer architectures and technologies, which are required to provide increasing computing power while withstanding severe constraints on size, energy consumption and reliability. Conventional Von-Neumann architectures and memories are not likely to fulfil all the needs of modern applications, due to inherent technological and conceptual limitations. Hence, in order to be at the forefront of the electronic industry in terms of design and manufacturing capabilities, it is essential to focus research and innovation efforts on the development of novel non-Von Neumann architectures enabled by emerging technology devices.

In this context, the neuromorphic computing paradigm has a huge potential when it makes use of emerging NV technologies (STT-MRAM, memristors), however, reliable and testable HW designs enabling the neuromorphic computing are still missing.

This PhD thesis will focus on the robustness of hardware implementations of bio-inspired neural networks (Spiking Neural Networks) by using emerging technologies (memristors and/or spintronic devices).

The **innovative aspects** of this research topic are related to the test and reliability aspects for HW implemented Spiking Neural Networks with on-line, unsupervised learning.

The **main objectives** of this thesis are:

Provide an in-depth study of meaningful robustness threats in SNNs: complete analysis of the faults that can occur in a Spiking Neural Network (SNN) and the assessment of fault-tolerance quality of such a network

Conduct a reliability estimation campaign: At gate level, evaluate the effect of aging phenomena, noise injection, and severe operation and environmental conditions. This analysis will culminate in a fault injection campaign. Faults will be injected in the network architecture and the system behavioral and its robustness, failure rate and mean time to failure (MTTF) will be evaluated.

Provide a manufacturing test strategy and design-for-test solutions: Both functional and structural test strategies will be targeted.

Provide a strategy for architecture robustness improvement: demonstrate the characteristics of a testable, reliable architecture of SNN with on-line learning and optimize the architecture for fault tolerance, accuracy, size and power consumption.

Profile: Master degree or equivalent in the area of either Electronic Engineering or Computer Engineering.

Expected skills

Technical: Analog/Digital integrated electronics (design, HDL modeling languages, CAD tools), VLSI Testing, C/C++ and scripting.
Personal: Determination, perseverance, trustworthiness, autonomy, adaptability, initiative, good communication skills
Languages: English: at least B2 equivalent, excellent reading and writing level, good speaking level.

About TIMA

TIMA Laboratory is a public joint research laboratory located in Grenoble, France, and held jointly by Institut Polytechnique de Grenoble (Grenoble INP), University Grenoble-Alpes and French National Research Council (CNRS). TIMA is a multinational team of over 100 people, with members and interns from all over the world. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end.
This call is from the AMfoRS team, and targets people motivated by hardware design and test. More information about the team is available at http://tima.imag.fr/tima/en/AMfoRS/AMfoRSoverview.html

Advisors

Thesis advisor: Elena Ioana Vatajelu, CNRS Researcher
Thesis director: Lorena Anghel, Professor, Grenoble INP
The work will be carried out in strong cooperation with the other members of the laboratory with large experience background in VLSI design and test.

To apply, send a mail to **ioana.vatajelu@univ-grenoble-alpes.fr** and lorena.anghel@univ-grenoble-alpes.fr, with the following attachments (in English):
- Detailed curriculum vitae
- Application letter with clear motivations
- Academic transcripts for the last two years of study
- 2 or 3 recommendations (letters or reference persons with e-mail addresses)