Post-doc title: Design of low-power analog and mixed-signal IPs in 28 nm FDSOI technology

Post-doc supervisor: Manuel J. Barragán (manuel.barragan@univ-grenoble-alpes.fr)

Location: TIMA Laboratory, Reliable Mixed-Signal Systems group (CNRS – Université Grenoble Alpes), Grenoble, France.

Funding: Post-doc contract with a net salary between 1940 Euro/month to 2420 Euro/month, depending on the candidate experience.

Starting date: Beginning of 2019.

Duration: 1 year, with the possibility of a second year.

In collaboration with: CMP, Multi-Project Circuits, Grenoble, France.

Context and description: The integration capabilities offered by current nanoscale CMOS technologies enable the fabrication of complete and very complex mixed-signal systems on a single die. The design of complex mixed-signal systems relies on the reuse of Intellectual Property blocks, the so-called IPs, as basic building blocks. In this line, this post-doc project envisages the design and validation of a library of basic analog and mixed-signal IPs in STMicroelectronics 28 nm FDSOI technology. The final goal of the project is to open this IP library to CMP customers around the world, so the developed IPs can be freely used to enable high-performance mixed-signal designs. The intended IP library will contain basic blocks such as operational amplifiers, comparators, reference generators, switches, etc.

Analog and mixed-signal design in state-of-the-art 28 nm FDSOI technology is a challenging task, but at the same time, FDSOI technologies open the door to low-power and high-performance applications that were unachievable in previous CMOS technologies. Indeed, the ability to adapt the body bias voltage may enable significant power savings if properly optimized. In the context of this post-doc project, we intend to explore optimization techniques for low-power and high performance analog and mixed-signal circuits in FDSOI technologies.

Skills: The prospective candidate should be highly motivated, have a PhD in Electrical and Electronics Engineering, Microelectronics or equivalent subject, have a good publication track in related fields, should be proficient in analog and mixed-signal integrated circuit design, and have experience with computer-aided design tools (e.g. Cadence). Experience on FDSOI technologies is also a plus.

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