Research engineer position in digital hardware for AI, SLS Team, TIMA Lab, Grenoble

In short : According to the GAFAM, AI tasks need a 100x power reduction in the coming years to be sustainable. This post-doc position focuses on highly energy efficient hardware/software architectures integration of AI and deep-learning to take up this challenge.

Context : The main challenges address the tight integration of AI accelerators in software-intensive systems bearing in mind non-functional requirements: low to very low power consumption, easy system-level co-processor usage, results reproducibility, real-time and low latency computations, AI functions virtualization for deployment on diverse execution platforms, compatibility with academic or industrial machine learning frameworks, etc. All production grade hardware IA accelerators (TPU, Nervana, DGX, Inferencia, etc) or IPs available for integration use classical digital CMOS, which will for some time still be the dominant hardware integration technology. Gaining a 100x in energy efficiency in this context will come from the architectural side: mathematical changes implied by the hardware constraints, hardware/software integration, and digital hardware implementation. The work takes place in the context of the European project AI4I.

Subject : The objective of this work is to design a full-custom digital accelerator to efficiently perform computations for neural networks using balanced ternary (e.g. taking their value in {-1, 0, 1}) or balanced binary ({-1, 1}) weights and activations. The principle of the architecture is defined , however there are still many design and implementation choices to be done, particularly regarding the handling of variability and . The target technology is STMicroelectronics 28 nm FDSOI.

Duration : 1 year.
Prerequisits :

- MSC/Engineering degree in computer engineering or electrical engineering
- Good knowledge of digital hardware architectures and CAD tools for the design and implementation of digital ASICs
- Good knowledge (at least theoretically) of static memory architectures
- CMOS transistor level design, implementation and simulation

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Lab, team and place:
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