LATS 2017
18th IEEE Latin-American Test Symposium
Bogota, Colombia, 13th - 15th March 2017

TECHNICAL PROGRAM
The Organizing, Program and Steering Committees, including the General and Program Chairs warmly welcome all the participants to the 18th IEEE Latin-American Test Symposium (LATS 2017). This year the conference is held in Bogota, Colombia. LATS (previously named Latin-American Test Workshop - LATW) is a well-recognized forum for design, test and fault tolerance professionals from all over the world particularly from Latin America, to present and discuss various aspects of system, board, and component test and fault-tolerance with design, manufacturing and field considerations in mind.

This year LATS offers an excellent Technical Program, which is composed of 11 Regular Paper Sessions, 1 Special Session, 1 Poster Session, 1 Keynote Address, 2 Panels, and 4 Invited Talks. The Regular Paper Sessions cover contributions on test pattern generation, analog and mixed-signal test, aging and FinFETs testing, board testing and built-in self-test, post-silicon verification and validation, radiation effects, industrial applications, Hardware Security and trust, network-on-chip testing, single and multiple event upsets, software-based hardening techniques and fault-injection techniques.

This year’s symposium features an up-to-date Keynote Address entitled “Quality and Reliability Challenges in the Internet of Things” presented by Yervant Zorian from Synopsys Corp, USA. Four Invited talks in highly important novel topics are proposed: “Emerging Spin Transfer Torque Devices Memories and Logic” given by Kaushik Roy from Purdue University, USA, “Fault Handling in Embedded Processors: Limits, Benefits, and Challenges” given by Mario Schölzel, IHP and University Potsdam, Germany, “Approximate Computing” given by Alberto Bosio, LIRMM, France and “STEM Robotics UMD. An innovative strategy to promote the learning of Math, Technology, Sciences and Engineering skills in public high schools, incubated by the Social Innovation Science Park” given by Miguel Angel González Palacios, Corporación Universitaria Minuto de Dios, Colombia. The Special Session this year is entitled “Radiation Facilities in Latin America”. The realization of LATS 2017 could not be possible without the work of very dedicated volunteers. We deeply and sincerely thank the members of the various committees, the authors, the reviewers, the session chairs, the secretariat and the technical support personnel for their valuable contributions. Finally, we would like to thank the IEEE Colombia Chapter for their organizational support and financial sponsorship, and IEEE Council on Electronic Design Automation (CEDA) and the IEEE Test Technology Technical Council (TTTC) for their technical co-sponsorship.

We hope that you will find the LATS 2017 Technical Program beneficial. We also hope that you enjoy Bogota.

General Chairs:
Raoul Velazco
TIMA, France
Yervant Zorian
Synopsys, USA

Program Chairs:
Ernesto Sanchez
Politecnico di Torino, Italy
Tiago Balen
UFRGS, Brazil
Monday, 13th March 2017

08:00 - 09:00  Registration

09:00 - 09:20  Opening Session
General Chairs:
Raoul Velazco – TIMA, France;
Yervant Zorian – Synopsys, USA
Program Chairs:
Ernesto Sanchez – Politecnico di Torino, Italy;
Tiago Balen – UFRGS, Brazil

09:20 - 10:00  Keynote Talk
Quality and Reliability Challenges in the Internet of Things
Yervant Zorian – SYNOPSYS, USA
Chair: Benjamin Schaefer, UT Dallas, USA

10:00 - 10:20  Coffee Break

10:20 - 11:20  Session 1
Analog and mixed signal testing
Chair: Ioannis Savidis, Drexel University, USA
Mixed Signal Verification to Avoid Integration Mismatch in Complex SoCs
Vinicius A. O. Martins and Wang J. Chau. USP - University of São Paulo, Brazil
Analysis of the Implications of Stacked Devices in Nano-Scale Technologies for Analog Applications
Ismael Lomeli-Illlescas, Sergio A. Solis-Bustos and José E. Rayas-Sánchez. Intel Tecnología de México, ITESO - The Jesuit University of Guadalajara, México.
Evaluation of a Mixed-Signal Design Diversity System under Radiation Effects
Carlos González Aguilera, Rafael Galhardo Vaz, Cristiano Chenet, Matheus Budelon, Odair Gonçalez and Tiago Balen. UFRGS, IEAv/DCTA, Brazil.

11:20 - 12:20  Session 2
Test pattern generation
Chair: Paolo Bernardi, Politecnico di Torino, Italy
Evaluating the Effectiveness of D-Chains in SAT based ATPG
Jan Burchard, Felix Neubauer, Pascal Raiola, Dominik Erb and Bernd Becker. University of Freiburg, Germany.
Testing Multiple Stuck-at Faults of ROBDD Based Combinational Circuit Design
Toral Shah, Anzhela Matrosova, Binod Kumar, Masahiro Fujita and Virendra Singh. IIT Bombay, India; Tomsk State University, Russia; University of Tokyo, Japan.

12:20 - 14:00  Lunch

14:00 - 14:40  Invited Talk 1
Emerging Spin Transfer Torque Devices - Memories and Logic
Kaushik Roy, Purdue University, USA
Chair: Alberto Bosio, LIRMM, France

14:40 - 15:40  Session 3
Aging and FinFETs testing
Chair: TBD
Analysis of Short Defects in FinFET Based Logic Cells
Freddy Forero, Michel Renovell, Jean-Marc Galliere and Victor Champac. INAOE México; LIRMM France.
Handling Manufacturing and Aging Faults with Software-based Techniques in Tiny Embedded Systems
Felix Mühlbauer, Patryk Skoncej, Lukas Schröder and Mario Schölzel. University of Potsdam, IHP GmbH, Germany.
Identifying High Variability Speed-Limiting Paths under Aging
Ankush Srivastava, Virendra Singh, Adit Singh and Kewal Saluja. NXP Semiconductor Inc, India; Indian Institute of Technology (IIT) Bombay, India; Auburn University, USA; University of Wisconsin, USA.

15:40 - 16:00  Coffee Break

16:00 - 16:40  Session 4
Board testing and Built-in-Self Test
Chair: Mario Schölzel. University of Potsdam, IHP GmbH, Germany
Linear Feedback Shift Register and Phase Shifter Computation for 2-Dimensional Test Pattern Generation
Oscar Acevedo Patiño and Juan Carlos Martinez Santos. Univ. Tecnológica de Bolívar, Colombia.
On the detection of board delay faults through the execution of functional programs
Gaiping An, Riccardo Cantoro, Ernesto Sanchez and Matteo Sonza Reorda. Politecnico di Torino, Italy.
16:40 - 17:20  Session 5
Post-silicon verification and validation
Chair: Adit Singh, Auburn University, USA

An automatic approach to perform the verification of hardware designs according to the ISO26262 functional safety standard
Enea Bagalini, Jacopo Sini, Matteo Sonza Reorda, Massimo Violante, Peter Sarson and Herwig Klimesch. Politecnico di Torino, Italy; AMS, Austria.

Post-silicon Observability Enhancement with Topology Based Trace Signal Selection
Binod Kumar, Ankit Jindal, Masahiro Fujita and Virendra Singh. IIT BOMBAY, India; University of Tokyo, Japan.

17:20 - 18:20  Panel 1
Test challenges of advanced technologies
Moderator: Victor Champac, INAOE, Mexico

Panelists:
Adit Singh, Auburn University, USA
Matteo Sonza Reorda, Politecnico di Torino, Italy
Yervant Zorian, Synopsys, USA

Tuesday, 14th March 2017

09:00 - 09:40  Invited Talk 2
Fault Handling in Embedded Processors: Limits, Benefits, and Challenges
Mario Schölzel, IHP & University Potsdam, Germany

Chair: Siddharth Garg, NYU, USA (TBC)

09:40 - 10:40  Session 6
Radiation effects
Chair: Felipe Restrepo Calle, Universidad Nacional de Colombia

Ionizing Radiation Effects on a COTS Low-Cost RISC Microcontroller

SEU Impact in Processor's Control-Unit: Preliminary Results Obtained for LEON3 Soft-Core
Thierry Bonnoit, Alexandre Coelho, Nacer-Eddine Zergainoh and Raoul Velazco. Laboratoire TIMA, University of Grenoble Alpes (UGA), France.

Evaluating the Behavior of Successive Approximation Algorithms Under Soft Errors
Gennaro Rodrigues and Fernanda Kastensmidt. UFRGS, Brazil.

10:40 - 11:00  Coffee Break

10:40 - 11:00  Poster Session
Low Cost Automatic Test Vector Generation for Structural Analog Testing
André Chinazzo, Paulo Comassetto de Aguirre and Tiago Balen. Technische Universität Kaiserslautern, Germany; Unipampa, UFRGS, Brazil.

An Approach to LFSR-Based X-Masking for Built-In Self-Test
Daichi Shimazu and Satoshi Ohtake. Oita University, Japan.

Fault Injection Methodology for Single Event Effects on Clock-gated ASICs
Luis Alberto Contreras Benites and Fernanda Lima Kastensmidt. UFRGS, Brazil.

Exploring BDDs to Reduce Test Pattern Set
Gabriel Porto, Paulo F. Butzen and Denis Franco. FURG, Brazil.

11:00 - 12:00  Session 7
Industrial applications
Chair: Maurizio Rebaudengo, Politecnico di Torino, Italy.

Practical Experience Designing and Debugging a FPGA for a Real-Time Ethernet Industrial Bus
Matheus Oliveira, João de Moraes, Sergio Cechin, Taisy Weber and João Netto. UFRGS, Brazil.

Specification, model and implementation in Hiles designer of a test equipment for an aircraft 28 VDC generator control unit
Armando Mateus, Fabian Eduardo Pérez Gordillo, José Fernando Jimenez and Rubby Casallas. Universidad Santo Tomás, Universidad de los Andes, Colombia.

A DMA and CACHE-Based Stress Schema for Burn-In of Automotive Microcontroller
Marco Restifo, Davide Appello, Paolo Bernardi, Riccardo Cantoro, Ernesto Sanchez, Federico Venini and Lorenza Gianotto. Politecnico di Torino, Italy.

19:00 - 20:30  Welcome Cocktail
12:00 - 13:00  Panel 2
Hardware Security and Trust
Moderator: Ramesh Karri, New York University, USA
Panelists:
Siddharth Garg, NYU, USA
Benjamin Schaefer, UT Dallas, USA
Ioannis Savidis, Drexel University, USA

13:00 - 14:00  Lunch

14:00  Social Event
visit to the Salt cathedral of Zipaquira
Completely carved in a salt cave, the Cathedral is unique and presents visitors with a majesty unparalleled view. Placed at 180 meters underground, it is a beautiful place away from everyday life that invites reflection, and selfdiscovery.

20:00  Gala Dinner

Wednesday, 15th March 2017

09:00 - 09:40  Session 8
NOC testing
Chair: Johan Sebastian Eslava Garzon, Universidad Nacional de Colombia (TBC)

Analysis of Routing Algorithms Generation for Irregular NoC Topologies
Ronaldo Tadeu Pontes Milfont, Paulo César Cortez, Alan Cadore Pinheiro, João Marcelo Ferreira, Jarbas Arvel Nunes Da Silveira, Rafael Gonçalves Mota and César Marcon. Federal University of Ceara, Pontifical Catholic University of Rio Grande do Sul, Brazil.

MINI-ESPADA: A Low-Cost Fully Adaptive Routing Mechanism for Networks-on-Chips
Amir Charif, Alexandre Coelho, Nacer-Eddine Zergainoh and Michael Nicolaidis. TIMA Laboratory, France.

09:40 - 10:40  Session 9
Single and Multiple event Upsets
Chair: Matteo Sonza Reorda, Politecnico di Torino, Italy.

SEU Susceptibility Analysis of a Feedforward Neural Network implemented in SRAM-based FPGA
I. Lopes, F. Kastensmidt and A. Susin. UFRGS, Brazil.

10:40 - 11:00  Coffee Break

Contrast of a HDL model and COTS version of a microprocessor for Soft-Error Testing

Analysis of SEU Sensitivity in a Commercial FPGA

11:00 - 11:40  Session 10
Software-based hardening techniques
Chair: Fernanda Kastensmidt, UFRGS, Brazil

An Effective Strategy for Selective Hardening of Software
Felipe Restrepo-Calle, Sergio Cuenca-Asensi and Antonio Martínez-Álvarez. Universidad Nacional de Colombia, University of Alicante, Spain.

TMR Technique for Mutex Kernel Data Structures
Alejandro Velasco, Bartolomeo Montrucchio and Maurizio Rebaudengo. Politecnico di Torino, Italy.

11:40 - 12:40  Special Session 1
Radiation Facilities in Latin America
Chair: Raoul Velazco, TIMA, France

Martin Alurralde - Facilities for radiation effects characterization at the Tandar Laboratory (Argentina)
Fabian Vargas - FPGA tests using heavy ions, X-rays and electromagnetic compatibility
Marcilei Silveira - New X-ray facility at LERI and general tests using alpha sources / Radiation tests using IEAv facilities
Nilberto Medina - São Paulo University Facilities to study SEE.
### 12:40 - 14:00  
**Lunch**

### 14:00 - 14:40  
**Invited Talk 3**  
**Approximate Computing**  
*Alberto Bosio, LIRMM, France*

*Chair: Ernesto Sanchez, Politecnico di Torino, Italy*

### 14:40 - 15:40  
**Session 11**  
**Fault injection techniques**  
*Chair: Fabian Vargas, PUCRS, Brazil*

**On the Development of a High Level Fault Simulator for the Analysis of Performance Faults on Speculative Modules**  
A. Floridia, R. Margelli and Ernesto Sanchez. Politecnico di Torino, Italy.

**Evaluation of Fault Attack Detection on SRAM-based FPGAs**  
Fabio Benevenuti and Fernanda Lima Kastensmidt. UFRGS, Brazil.

**Preliminary Results of NETFI-2: An Automatic Method for Fault Injection on HDL-Based Designs**  
Alexandre Coelho, Miguel Solinas Jr, Juan Fraire, Nacer-Eddine Zergainoh, Raoul Velazco and Pablo Ferreyra. TIMA, France; Universidad Nacional de Córdoba, Argentina.

### 15:40 - 16:00  
**Coffee Break**

### 16:00 - 17:00  
**Invited Talk 4**  
**STEM Robotics UMD**  
*Miguel Angel González Palacios, Parque Científico de Innovación Social Corporación Universitaria Minuto de Dios, Colombia*

*Chair: Tiago Balen, UFRGS, Brazil*

### 17:00  
**Closing Remarks**