THE EPI PROCESSOR AND ITS ROBUSTNESS REQUIREMENTS

YING-CHIH YANG AT FEDFRO’2019
EPI LEAD ARCHITECT
EPI STREAM 2 LEADER
EPI – EUROPE'S AMBITION

- Design a roadmap of future European low power processors targeting
  - Extreme scale computing,
  - High performance big data,
  - Emerging applications

- FPA answering EU Horizon 2020 (FP8) ICT-42-2017 call

* FPA : Framework Partnership Agreement
EPI – MISSION

- **European Independence** in High Performance Computing Processor Technologies
  - Goal: EU ExaScale machines based on EU processor by 2023
  - Pre-ExaScale level pilot in 2021 with Gen1 processor

**AND**

- Based on a solid, long-term economic model
  - Go beyond the HPC market (not large enough)
  - Address the needs of European Industry ➔ Car manufacturing market
EPI ROADMAP

Rhea Family - Gen1 GPP
EPI Common Platform
ARM & RISC-V
External IPs
HPC System PreExascale
Automotive PoC

2021

Cronos Family - Gen2 GPP
EPI Common Platform
ARM & RISC-V
HPC System Exascale
Automotive CPU

2021-2022

EPI IP’s Launch Pad & Pan European Research Platform for HPC and AI

2022-2023

Gen3 GPP Family

2024-...
EPI 26 PARTNERS, FROM RESEARCH TO INDUSTRY

Proof of concept by EPI project
- EPI Common Platform PCIe card
- EPI HPC blade
- EPI mother board
- EPI Automotive PoC
- System vendors

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EPI KPIS

- Energy Efficiency
  * Pre-ExaScale level with general-purpose CPU core in the first EPI GPP chip
  * Develop acceleration technologies for better DP GFLOPS/Watt performance
  * Inclusion of MPPA for real-time application acceleration
  * Develop a Common Platform to enable EPI accelerations

- Easy to use
  * Adopt Arm general-purpose CPU core with SVE / vector acceleration in the first EPI chip
  * Supply sufficient Memory Bandwidth (Byte/FLOP) to support the GPP application
  * in SGA1, focus on programming models to include accelerations.

- Reliability
  * (to-be-engineered)
CHALLENGES FOR ADVANCED COMPUTING

PERFORMANCE

100 EFLOPS
10 EFLOPS
1 EFLOPS
100 PFLOPS
10 PFLOPS
1 PFLOPS
100 TFLOPS
10 TFLOPS
1 TFLOPS

ENERGY PER OPERATION*

Source: Top500

* assuming 20 MWatt supercomputer

10^18 FLOPs @ 20MW?

10x energy efficiency improvement every 4 years

/10 every 4 years

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Max. frequency reached

Max. power reached

Max. nb of transistors reached

Source from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanovic.
HAPPY SCALING

Transistor nb +++
Frequency +
Power density =

Source from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanovic,
MAX. POWER

Transistor nb ++
Frequency =
Power density =

Source from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanovic.
HETEROGENEOUS ARCHITECTURES

Today and next generation

Source from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanovic.
RACE TO EXASCALE

- CPU architecture choice
  - x86 + accelerator (heterogeneous)
  - Arm/SVE (homogeneous)
  - Others

EPI takes 2-step approach
- step#1: homogeneous with Arm core+SVE
- step#2: heterogeneous with additional EPI accelerators
EPI OBJECTIVES

- Architect of the common platform to accommodate the developed technologies
  - CoDesign Methodology, Platform for hardware and software, Power management, Modeling and Simulation
- Build a GPP processor chip ready for Preexascale level machines (RheaRI)
- Develop Accelerator technologies for HPC workload (EPAC)
- Implementation of a Real-time acceleration PoC based on the first EPI GPP Processor (MPPA)
- Interfacing with the Automotive MCU
- Development efficient power conversion technologies
- Software activities based on the platform built
- PoC systems (test-chip; ref. board, HPC blades, PCIe card and automotive PoC)
- Related research around the EPI project scopes
EPI COMMON PLATFORM

Board / System level

Package level

Chip level

Functional Block level

PCIe gen5 links
HSL links
D2D links to adjacent chiplets

Arm Core
MPPA
eFPGA
EPAC
HBM memories
DDR memories
ACCELERATOR #1: EPAC
EPI ACCELERATOR BASED ON RISC-V

- EPAC - EPI Accelerator
- VPU – Vector Processing Unit
- STX – Stencil/Tensor accelerator
- VRP - VaRiable Precision co-processor
EPI STREAMS

S1 - Common Stream: Codesign, Architecture, System software and key technologies for the Common Platform

S2 - GPP Processor: Design and implement of the processor chip(s) and PoC system

S3 - Acceleration: Foster acceleration technologies and create building blocks

S4 - Automotive: Address automotive market needs and create a pilot eHPC system

S5 - Administration: Manage and support activities
EPI CO-DESIGN

Architects within Streams

Model and Modeling

+ 

Requirements
Benchmarks
Simulator, Eval. requirements
Eval. results

Application Experts

S2 - GPP Processor
S3 - Acceleration
S4 - Automotive
EPI MODELING

- Virtual prototyping framework
- Large and flexible IP portfolio
  - Supports models from native library & ext. providers (QEMU, ARM Fast Models)
- SystemC / TLM 2.0 simulations
  - Co-simulation & co-emulation for RTL valid.
  - Co-simulation with 3rd-party tools (FMI standard)
- Designed to run full software stacks
  - Firmware, bootloader, hypervisor, OS kernel, user applications
  - Develop, debug, profile using std. tools
EPI PROCESSOR AND ITS ROBUSTNESS CHALLENGES
ROBUSTNESS CHALLENGES IN EPI

- Robustness / reliability requirement of HPC processor chips
- Robustness to automotive environment
- Challenges
ROBUSTNESS IN HPC SYSTEM

- Controlled Physical Environment but with Large-scale scaling
- Applications sharing nodes and resources
- Target
  - Reliability of the system (MTTI)
    - MTBF / MTTF of components
    - Fault tolerant techniques
  - Secured computing
    - Segregation of the applications

Node with MTBF $\mu_{\text{node}} = 10\text{yrs}$

Worst case MTTI for a 50K-node system $\mu = 10\text{yrs}/50K = 1.75\text{hrs}$
ROBUSTNESS IN AUTOMOTIVE

Background

- Tough Environmental and Electrical requirement
  - No longer controlled / hostile environment: Temperature/Thermal cycle and Vibration...
  - Owned and maintained by the user
  - Mission profiles: Lifetime/Operating-hour/Mileage
- Long product design cycle
- ADAS and infotainment needs

Target

- Zero-defect / No-defect programs
- From Fail-safe to Fail-operational
- Energy efficient computing
- Modular computing
- Secured computing
AUTOMOTIVE EHPC PLATFORM – EPI

* eHPC – embedded HighPerformanceComputing
ROBUSTNESS CHALLENGES TO EPI

Challenges

- Highly integrated chip in adv. Silicon Process
  => Manufacturing Defect and Variation
- Energy efficiency
  => Supply Voltage Reduction
  => Efficient Power Delivery
- Product lifetime and mission profile
  => Aging in advanced Silicon Process
- Application required Safety and Security

Need solutions for

- How to design and verify
- How to implement
- How to signoff
- How to manufacture
- How to do qualification
- How to test / repair
- How to use it during runtime / software and system
REDUCTION OF THE SUPPLY VOLTAGE

- Scaling in voltage for better energy efficiency

- Today’s PD solutions
  - Power gating or On-chip/On-die regulation
  - Low loss conversion

- Challenges
  - Less headroom for the gating / regulation
  - Extra loss in the gating devices
  - Less margin to the noise

- Evaluating solutions now

Existing solution in the market
DESIGN – EPI

For ext. IPs
- Source IPs with RAS features
  - Tolerant of error(s)
  - Capable of retry

For newly designed functions
- Memory with redundancy
- Memory with low-voltage capability
- Parity / ECC on memory or datapaths
- Other fault-detect and Fault-tolerant techniques
IMPLEMENTATION – EPI

Challenges

- Std. cell Library characterized at new operating points
- IR drop / power distribution and power grid planning
- Clock distribution and clock/power domain partition

Luckily..

- Vendors are working on solutions to cover them..
  - fast turnaround time
  - integrated tools
More corners and conditions
- OCV-aware / OCV-smart
- Non-Gaussian distributed delay at near-threshold
- Wire delay variation
- Aging
- New DFM issues

Faster and smarter tool
- LVF (Liberty Variance Format) and LVF with moments models non-Gaussian distributions
MANUFACTURING

- Silicon Process, Assembly and the Supply chain

- 2.5D or 3D-IC integration
  - Near memory and more compact systems
  - Integration of new power delivery scheme / devices

- Challenge to vibration and hostile environments
QUALIFICATIONS, TEST AND REPAIRING

Today

- JEDEC wafer qualification and package qualifications
  - HAST/HTOL, TC, ..
- Vendor-specific qualifications (for automotive or other operating conditions)
- Automotive grade screening

In addition

- Testability for the amount of devices
- Repairing/replacement for yield improvement
SOFTWARE AND SYSTEM

Today

- Check point
- Fault-tolerant libraries
- Power management with defined Power policies
- PVT monitoring and thermal-throttling

Need solution

- Smart use of the energy
- Aging prediction, monitoring
- Possible Wear-leveling
SECURITY IN EPI PROCESSOR

- Root of trust
- Security domains
- Security services
- Advanced cryptographic functions
- Various monitors for fault-injection, physical intrusion and other conditions
SUMMARY

- EPI is
  - Developing a Common Platform to integrate heterogeneous technologies
  - Developing acceleration technologies for HPC workload
  - Developing automotive compatible acceleration technologies
  - Developing a low-power GPP processor chip targeting HPC application and automotive industry

- Where one of the main challenges is robustness/reliability
  - Integration and Reduction of supply voltage in adv. Silicon Process
  - Security

- Robust engineering is one of key pillar in EPI and future industries
WE ACCELERATE ACCELERATORS !!!!

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EPI TUTORIAL IN BARCELONA

- 17 July 2019 at Barcelona

- Co-located with

ACM Europe Summer School
HPC Computer Architectures
for AI and Dedicated Applications

https://www.european-processor-initiative.eu/event/epi-tutorial-in-barcelona/