

# Monday July 1, 2019

07:30 – 08:30: Registration

08:30 – 09:45: FEDFRO Opening Session

08:30 – 08:45: Welcome Message

08:45 – 09:45: FEDFRO 2019 Keynote Talk

The EPI Processor and its Robustness Requirements  
Ying-Chih Yang (Atos)

09:45 – 10:00: Break

10:00 – 10:15: IOLTS Opening Session

10:15 – 11:15: Session 1 – Soft Errors

- 1.1 Comparison of Radiation Hardness of Stacked Transmission-Gate Flip Flop and Stacked Tristate-Inverter Flip Flop in a 65 nm Thin BOX FDSOI Process, M.Ebara, K.Yamada, J.Furuta, K.Kobayashi (Kyoto Inst. of Techn.)
- 1.2 Machine Learning To Tackle the Challenges of Transient and Soft Errors in Complex Circuits, T.Lange (iRoC), A.Balakrishnan (iRoC/Tallinn U Techn.), D.Alexandrescu, M.Glorieux (iRoC), L.Sterpone (Politecnico di Torino)
- 1.3 Selective Fault Tolerance by Counting Gates with Controlling Value, A.Breitenreiter, S.Weidling, O.Schraper, S.Zeidler (IHP), P.Reviriego (U Carlos III de Madrid), M.Krstic (IHP)

11:15 – 12:15: Session 3 – Posters & Coffee Break

- 3.1 Flight Safety Certification Implications for Complex Multi-Core Processor based Avionics Systems, J.Athavale, R.Mariani, M.Paulitsch (Intel)
- 3.2 A Design for Testability Method for k-Cycle Capture Test Generation, Y.Ishiyama, T.Hosokawa, H.Yamazaki (Nihon U)
- 3.3 An efficient SAT-attack algorithm against logic encryption, Y.Matsunaga (Kyushu U), M.Yoshimura (Kyoto Sangyo U)
- 3.4 Development of FF Circuits for Measures Against Power Supply Noise, Y.Miura, M.Inoue, Y.Kinoshita (Tokyo Metropolitan U)
- 3.5 Efficient Fault Injection based on HDL Slicing Technique, A.C.Bagbaba (Cadence), M.Jenihhin, J.Raik (Tallinn U of Techn.), C.Sauer (Cadence)
- 3.6 Empirical Evaluation on Anomaly Behavior Detection for Low-Cost Micro-Controllers Utilizing Accurate Power Analysis, K.Hasegawa (Waseda U), K.Chikamatsu (Keysight Techn.), N.Togawa (Waseda U)
- 3.7 Fault Modeling and Simulation of Memristor based Gas Sensors, S.Khandelwal, A.Bala (Oxford Brookes U), V.Gupta, M.Ottavi, E.Martinelli (U Rome Tor Vergata), A.Jabir (Oxford Brookes U)
- 3.8 Methodology for Tradeoffs between Performance and Lifetimes of Integrated Circuits, C.Papachristou, D.Weyer, F.Wolff (CWRU)
- 3.9 Implementation of CMOS Logic Circuits with Perfect Fault Detection Using Preservative Reversible Gates, S.Parvin, M.Altun (Istanbul Technical U)

12:15 – 13:15: Special Session S1 – Reliability simulation from device to circuit level

Organizer: F.Cacho (STMicroelectronics),  
Moderator: A.Michard

10:15 – 11:15: Session 2 – Failure and Fault Analysis

- 2.1 Towards Improvement of Mission Mode Failure Diagnosis for System-on-Chip, S.Mhamdi, A.Virazel, P.Girard (LIRMM), A.Bosio (Lyon Inst. of Nanotechnology), E.Auvray, E.Faehn, A.Ladhar (STMicroelectronics)
- 2.2 Automated Die Inking through On-line Machine Learning, C.Xanthopoulos, Y.Makris (UT Dallas), K.-P.Tschernay, A.Neckermann, P.List (ams AG), P.Sarson (Dialog Semiconductor)
- 2.3 Stuck-at-OFF Fault Analysis in Memristor-Based Architecture for Synchronization, M.Escudero-López (UPC), I.Vourkas (U Técnica Federico Santa María), A.Rubio (UPC)

12:15 – 13:15: Special Session S2 – Memory Robustness

Organizer/Moderator: G.Harutyunyan (Synopsys)

- S2.1 A Technique to Achieve Necessary FIT Rate while Maintaining Area, Power

- (STMicroelectronics)
- S1.1 Reliability Challenges with Self-Heating in FinFET Technology, H.Amrouch, V.M.van Santen, O.Prakash, H.Kattan, S.Salamin, S.Thomann, J.Henkel (Karlsruhe Inst. of Techn.)
- S1.2 Global and Local Process Variation Simulations in Design for Reliability approach, A.Michard, F.Cacho, D.Celeste, X.Federspiel (STMicroelectronics)
- S1.3 HCD-Induced GIDL Increase and Circuit Implications, E.Ceccarelli, K.Manning, G.Macera, D.Dempsey, C.Heffernan (Analog Devices)

13:15 – 14:30: Lunch

14:30 – 15:30: Session 4 - Accelerators

- 4.1 Cost-effective Resilient FPGA-based LDPC Decoder Architecture, E.Souza, G.Nazar (UFRGS)
- 4.2 Software-only Diverse Redundancy on GPUs for Autonomous Driving Platforms, S.Alcaide Portet, L.Kosmidis, C.Hernandez, J.Abella (Barcelona Supercomputing Center)
- 4.3 Testing permanent faults in pipeline registers of GPGPUs: A multi-kernel approach, J.Rodriguez Condia, M.Sonza Reorda (Politecnico di Torino)

15:30 – 15:45: Break

15:45 – 16:45: Special Session S3 – Resilient and Secure Mixed-Signal/RF Circuits and Systems

Organizer/Moderator: A.Chatterjee (Georgia Tech.)

- S3.1 Self-Monitoring, Self-Healing Biomorphous Sensor Technology, A.Richardson, D.Cheneler (Lancaster U)
- S3.2 BIST Solutions for Industrial Mixed-signal Circuits, S.Mir (TIMA)
- S3.3 Trusted and Secure Design of Analog/RF ICs: Recent Developments, K.Subramani, G.Volanis, M.-M.Bidmeshki, A.Antonopoulos, Y.Makris (UT Dallas)

- and Performance Ratio, C.Argyrides (AMD), G.Harutyunyan, Y.Zorian (Synopsys)
- S2.2 Variation-Aware Fault Modeling and Test Generation for STT-MRAM, S.M.Nair, R.Bishnoi, M.Tahoori (Karlsruhe Inst. of Techn.), H.Grigoryan, G.Tshagharyan (Synopsys)
- S2.3 Tuning BIST Architecture via Fault Prediction Mechanism, G.Harutyunyan, S.Shoukourian, Y.Zorian (Synopsys)

14:30 – 15:30: Session 5 – Hardware Security

- 5.1 On a Side Channel and Fault Attack Concurrent Countermeasure Methodology for MCU-based Byte-sliced Cipher Implementations, E.Aerabi (LCIS), A.Papadimitriou (U Grenoble Alpes), D.Hely (LCIS INP GRENOBLE)
- 5.2 HATE: a HARDware Trojan Emulation Environment for Microprocessor-based Systems, C.Bolchini, L.Cassano, I.Montalbano, G.Repole, A.Zanetti (Politecnico di Milano), G.Di Natale (TIMA)
- 5.3 Encrypted Physically Unclonable Function, E.Vatajelu (TIMA), G.Di Natale (TIMA), M.S.Mispan, B.Halak (U Southampton)

15:45 – 16:45: Special Session S4 – Emerging Trends in Hardware Margins and Energy-Efficiency

- S4.1 Energy-Efficiency and Margins in Multicore CPUs, D.Gizopoulos, G.Papadimitriou, A.Chatzidimitriou (U Athens)
- S4.2 Energy-Efficiency and Reliability of Manycore Architectures, V.J.Reddi (Harvard U)
- S4.3 FPGAs Undervolting, O.Unsal, B.Salami, A.Cristal (Barcelona Supercomputing Center)

**16:45 – 17:15: Coffee Break**

**17:15 – 18:15: Special Session S5 – Cost-Effective Resilience-I: Advanced Cross-Layer Analysis and Optimization Techniques**

Organizer: M.Shafique (TU Wien), Moderator: P.Kindt (TU Munich)

- S5.1 Resiliency demands on next generation critical embedded systems, J.Abraham (UT Austin)
- S5.2 Studying Aging and Soft Error Mitigation Jointly under Constrained Scenarios in Multi-Cores, F.Kriebel, S.Rehman, M.Shafique (TU Wien)
- S5.3 Bayesian models for early cross-layer reliability analysis and design space exploration, A.Vallero, A.Savino, A.Carelli, S.Di Carlo (Politecnico di Torino)
- S5.4 Energy-Efficient Resilience for On-Chip Systems, A.Garcia-Ortiz (U Bremen)

**20:00: Welcome Reception**

## Tuesday July 2, 2019

**08:30 – 09:30: Special Session S6 – Hardware Security for Emerging Applications**

Organizer: M.Maniatakos (NYUAD),  
Moderator: R.Karri (NYU)

- S6.1 3D Integration: Another Dimension for Hardware Security, O.Sinanoglu (NYUAD)
- S6.2 Reverse Engineering of Flow-Based Microfluidic Biochips, S.Bhattacharjee (NYUAD)
- S6.3 JTAG: A Multifaceted Tool for Cyber Security, M.Maniatakos (NYUAD)

**09:30 – 09:45: Break**

**09:45 – 10:45: Session 6 – Error Correcting Codes**

- 6.1 Efficient Concurrent Error Detection for SEC-DAEC Encoders, J.Li (Harbin Inst. of Techn.), P.Reviriego (U Carlos III de Madrid), L.Xiao (Harbin Inst. of Techn.), C.Argyrides (AMD)
- 6.2 A new DEC/TED code for fast correction of 2-bit-errors, P.-P.Nordmann, M.Goessel (U Potsdam)
- 6.3 A Vulnerability Factor for ECC-protected Memory, L.Jaulmes, M.Moreto, M.Valero, M.Casas (Barcelona Supercomputing Center)

**10:45 – 11:15: Coffee Break**

**11:15 – 12:15: Special Session S8 – Cost-Effective Resilience-II: Reliable Edge Computing**

Organizer/Moderator: M.Shafique (TU Wien)

- S8.1 Reliability-Aware Task Allocation Latency Optimization in Edge Computing, A.Kouloumpris, M.Michael, T.Theocharides (U Cyprus and KIOS)

**08:30 – 09:30: Special Session S7 – Memristors: The Missing Applications Found**

Organizers/Moderators: M.Ottavi (U Rome Tor Vergata), A.Jabir (Oxford Brookes U)

- S7.1 Real Processing-in-Memory using Memristive Memory Processing Unit, S.Kvatinsky (Technion)
- S7.2 Using Memristors for Photovoltaic Array Monitoring, M.Ottavi (U Rome Tor Vergata)
- S7.3 Reliable Sensing with Process Variation Aware Memristor Array, S.Khandelwal (Oxford Brookes U)

**09:45 – 10:45: Session 7 – Attacks**

- 7.1 QuSecNets: Quantization-based Defense Mechanism for Securing Deep Neural Network against Adversarial Attacks, F.Khalid (TU Wien), H.Ali, H.A.Tariq (NUST), M.A.Hanif, S.Rehman (TU Wien), R.Ahmed (NUST), M.Shafique (TU Wien)
- 7.2 TriSec: Training Data-Unaware Imperceptible Security Attacks on Deep Neural Networks, F.Khalid, M.A.Hanif, S.Rehman (TU Wien), R.Ahmed (NUST), M.Shafique (TU Wien)
- 7.3 LED Alert: Supply Chain Threats for Stealthy Data Exfiltration in Industrial Control Systems, D.Tychalas, A.Keliris, M.Maniatakos (NYU-AD)

- S8.2 Towards Scalable Lifetime Reliability Management for Dark Silicon Manycore Systems, V.Rathore (Nanyang Techn. U), V.Chaturvedi (IIT Palakkad), A.K.Singh (U Essex), T.Srikanthan (IIT Palakkad), M.Shafique (TU Wien)

- S8.3 Power-aware Reliable Communication for the IoT, P.H.Kindt, S.Chakraborty (TU Munich)

**12:15 – 12:30: Break**

**12:30 – 13:30: IOLTS 2019 Keynote Talk**

From Research to Product: RAS Features in EPYC and Radeon Instinct  
Vilas Sridharan (AMD)

**13:30 – 15:00: Lunch**

**15:00 – 16:00: Special Session S9 – Advance Radiation-Hard Circuits and Systems – Design and Implementation**

Organizers/Moderators: Z.Stamenkovic, M.Krstic (IHP)

- S9.1 Characterization and Modeling of SET Generation Effects in CMOS Standard Logic Cells, M.Andjelkovic, Y.Li, Z.Stamenkovic, M.Krstic, R.Kraemer (IHP, U Potsdam, Brandenburg U. of Techn.)
- S9.2 Recipes to Build-Up a Rad-Hard CMOS Memory, C.Calligaro, U.Gatti (RedCat Devices)
- S9.3 A Radiation Tolerant 10/100 Ethernet Transceiver for Space Applications, A.Breitenreiter, M.Krstic (IHP), J.López, Ú.Gutierrez, D.González (Arquimea Ingeniería), P.Reviriego (U Carlos III de Madrid), M.Sánchez-Renedo (Thales-Alenia Space)

**16:30: Social Event & Dinner**

## Wednesday July 3, 2019

**08:30 – 09:30: Special Session S10 – Design for Robustness vs Design for Low Power**

Organizer/Moderator: P.Girard (LIRMM)

- S10.1 Energy-quality scaling beyond conventional variation-aware digital design for continued energy scaling, M.Alioto (National U of Singapore)
- S10.2 Meeting the Conflicting Goals of Low-Power and Resiliency Using Emerging Memories, S.Ghosh, K.Nagarajan, S.Sayyah, N.Khan, A.Saki, A.De (Penn State U)
- S10.3 Variation-Resilient Design Techniques for Energy-Constrained Systems, T.-T.Liu (National Taiwan U)

**09:30 – 10:30: Session 10 – Posters & Coffee Break**

- 10.1 A Test Generation Method Based on k-Cycle Testing for Finite State Machines, Y.Kinoshita (Tokyo Metropolitan U), T.Hosokawa (Nihon U), H.Fujiwara (Osaka Gakuin U)
- 10.2 Total Ionizing Dose Effects by alpha irradiation on circuit performance and SEU tolerance in thin BOX FDSOI process, T.Yoshida, K.Kobayashi, F.Jun (Kyoto Inst. of Techn.)
- 10.3 PASCAL: Timing SCA Resistant Design and Verification Flow, L.Xinhui, M.Jenihhin, J.Raik (Tallinn U Techn.), K.Paul (IIT Delhi)
- 10.4 Error Correction Coding of Stochastic Numbers Using BER Measurement, R.Ishikawa, M.Tawada, M.Yanagisawa, N.Togawa (Waseda U)
- 10.5 Control Loop of Image Correction based on Detection and Self-Healing of Defective Pixels, G.Takam Tchendjou, E.Simeu (TIMA)
- 10.6 Securing Scan through Plain-text Restriction, S.Ahlatwari, K.Ahirwar (IIT Bombay), J.Tudu (IIT Tirupati), M.Fujita (U Tokyo), V.Singh (IIT Bombay)
- 10.7 A Novel Simulation-Based Approach for ISO 26262 Hazard Analysis and Risk Assessment, J.Sini, M.Violante (Politecnico di Torino), L.Pecorella, V.Dodde (MCA Engineering), R.Gnaniyah (MCA Engineering)
- 10.8 Efficient Methodology for ISO26262 Functional Safety Verification, F.Augusto Da Silva, A.Cagri Bagbaba (Cadence), S.Hamdioui (Delft U of Techn.), C.Sauer (Cadence)

**10:30 – 11:30: Session 8 – Aging/Wearout**

- 8.1 Identification of Failure Modes for Circuit Samples with Confounded Causes of Failure, S.-H.Hsu, Y.-Y.Huang, K.Yang, L.Milor (Georgia Tech.)

**10:30 – 11:30: Session 9 – Power Issues**

- 9.1 Run-time Detection and Mitigation of Power Noise Viruses, V.Tenentes (U Ioannina), S.Das (ARM), D.Rossi (U Hertfordshire), B.Al-Hashimi (U Southampton)
- 9.2 Analysis on Retention Time and

- 8.2 ICE-RADAR: In-situ, Cost-Effective Razor Flip-Flop Deployment for Aging Resilience, K.-C.Wu, W.-T.Huang (National Chiao Tung U), C.-Y.Huang (Synopsys)
- 8.3 Estimation of oxide breakdown effects by fault injection, C.Sandionigi (CEA), O.Heron (CEA)

- Adaptive Refresh in Embedded DRAMs with Ageing Benefits, D.Rossi, A.Najdi (U Hertfordshire), V.Tenentes (U Ioannina)
- 9.3 iATPG: Instruction-level Automatic Test Program Generation for Vulnerabilities under DVFS attack, K.Zhang, J.Huang, J.Ye, X.Ye, D.Wang, D.Fan, H.Li, X.Li, Z.Zhang (ICT, Chinese Academy of Sciences)

### 11:30 – 11:45: Break

#### 11:45 – 12:45: Session 11 – Timing Issues

- 11.1 A Controller Augmentation Method to Improve Transition Fault Coverage for RTL Data-Paths, Y.Takeuchi, T.Hosokawa, H.Yamazaki (Nihon U), M.Yoshimura (Kyoto Sangyo U)
- 11.2 Application Specific True Critical Paths Identification in Sequential Circuits, L.Jürimägi, R.Ubar, M.Jenihhin, J.Raik, S.Devadze, A.Oyeniran (Tallinn U Techn.)
- 11.3 Compact Modeling of NBTI Replicating AC Stress / Recovery from a Single-shot Long-term DC Measurement, S.Nishizawa, T.Hosaka (Saitama U), R.Kishida (Tokyo U of Science), T.Matsumoto (U Tokyo), K.Kobayashi (Kyoto Inst. of Techn.)

#### 11:45 – 12:45: Session 12 – Error and Attack Detection

- 12.1 Detecting Errors in Convolutional Neural Networks Using Inter Frame Spatio-Temporal Correlation, L.Draghetti, F.Santos, L.Carro, P.Rech (UFRGS)
- 12.2 Hierarchical Check Based Detection and Diagnosis of Sensor and Actuator Malfunction in Autonomous Systems, M.Momtaz, A.Chatterjee (Georgia Tech)
- 12.3 Dual Detection of Heating and Photocurrent attacks (DDHP) Sensor using Hybrid CMOS/STT-MRAM, M.Kharbouche-Harrari, R.Wacquez (CEA), G.Di Pendina (CNRS, CEA, INAC-SPINTEC), J.-M.Dutertre (IMT), J.Postel-Pellerin (Aix Marseille U - IM2NP), D.Aboukassimi (CEA), J.-M.Portal (AMU-IM2NP)

### 12:45 – 14:00: Lunch

#### 14:00 – 14:15: Symposium Closing Remarks