Issues related to on-line testing techniques, and more generally to design for robustness, are increasingly important in modern electronic systems. In particular, the huge complexity of electronic systems has led to growth in reliability needs in several application domains as well as pressure for low cost products. There is a corresponding increasing demand for cost-effective design for robustness techniques. These needs have increased dramatically with the introduction of nanometer technologies, which impact adversely noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating and make mandatory the use of design for robustness techniques for extending yield, reliability, and lifetime of modern chips. Design for reliability becomes also mandatory for reducing power dissipation, as voltage reduction, often used to reduce power, strongly affects reliability by reducing noise margins and thus the sensitivity to soft-errors and EMI, and by increasing circuit delays and thus the severity of timing faults. There is also a strong relation between design for reliability and design for security, as security attacks are often fault-based. The International Symposium on On-Line Testing and Robust System Design (IOLTS) is an established forum for presenting novel ideas and experimental data on these areas. The Symposium is sponsored by the IEEE Council on Electronic Design Automation (CEDA) and the 2017 edition is organized by the IEEE Computer Society Test Technology Technical Council, the University of Athens, and the TIMA Laboratory. IOLTS 2017 is held for second year as part of the 2nd Federative Event on Design for Robustness (FEDfRo – http://tima.imag.fr/conferences/fedfro/fedfro17/).
The location
Thessaloniki has many stories to tell, starting by the moment of its foundation in 316/315 B.C. Fortunate to have royal “blood”, since the new city was named after Thessaloniki, sister of Alexander the Great and daughter of Philip II, King of Macedonia. It was developed rapidly due to its prominent geographical location as one of the most important ports, and economical and commercial centers of Macedonia and the Balkan Peninsula as a whole, advantages maintained for the past 2300 years.

Undeniable witnesses of its long course over the years are its numerous monuments. Open and easily accessible to the public, live alongside its residents and tell interesting stories about different civilizations, religions, eras. We invite you to read the history of Thessaloniki so as to comprehend their significance, before you come across them, walking around the city, and to feel this uniqueness that makes Thessalonians so proud for their past.

(source: https://www.thessalonikitavel/en/ - The official travel guide of Thessaloniki)

The venue
Makedonia Palace 5-star hotel is an iconic hotel of the city of Thessaloniki. It has been completely renovated both functionally and aesthetically. The hotel is conveniently located on the seafront of Thriassios Golf and at short walk from the city center and the main attractions. It provides a dedicated business section that guarantees the success of every business event and demanding conferences like IOLTS and FEDRo 2017.

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H. J. Wunderlich, U. Stuttgart
Y. Zorian, Synopsys
Monday July 3, 2017

07:30 – 08:30: Registration
08:30 – 09:30: FEDFRO Opening Session
08:45 – 08:45: Welcome Message
08:45 – 09:30: FEDFRO Keynote Talk 1

Trends and Challenges in Today’s Safety Critical SoCs, Y.Zorian (Synopsys)

09:30 – 09:45: Break

09:45 – 10:45: IOLTS Opening Session
09:45 – 10:00: Symposium Introduction
M.Nicolaidis (TIMA Lab), A.Paschalis (U Athens), General Chairs
D.Gizopoulos (U Athens), D.Alexandrescu (iRoC), Program Chairs
10:00 – 10:45: IOLTS Keynote Talk
Autonomous Driving and IoT: combining Functional Safety, Reliability, Availability and Security for a Resilient Connected World, R.Mariami (Intel)

10:45 – 11:45: Session 1 – Posters & Coffee Break
1.1 A Cost-Efficient Dependability Management Framework for Self-aware System-on-chips based on IEEE 1687, A.Ibrahim, H.Kerkhoff (U Twente)
1.2 A New 3-Bit Burst-Error Correcting Code, A.Klockmann (U Potsdam), G.Georgakos (Infinineon), M.Gössel (U Potsdam)
1.3 SICTA: A Superimposed In-Circuit Fault Tolerant Architecture for SRAM-based FPGAs, A.Kourafal, A.KuliKarni, D.Stroobandt (Ghent U), D.M.Candinach (ESA)
1.4 Assessment of the Amplitude-Duration Criterion for SET/SEU Robustness Evaluation, M.Andjelkovic, M.Krste, K.Rolf (HPP)
1.6 Controller Augmentation and Test Point Insertion at RTL for Concurrent Operational Unit Testing, T.Hosokawa, S.Takeda, H.Yamaraki (Nihon U), M.Yoshimura (Kyoto Sangyo U)
1.7 Deterministic Network On Chip for Deploying Real-Time Applications on Many-core Processors, S.Esposito, M.Violante (Politecnico di Torino)
1.8 Diagnosis with Transition Faults on Embedded Segments, T.Toulas (Synopsys), S.Tragoudas (Southern Illinois U).

11:45 – 12:45: Session 2 – Soft Errors
Moderator: S.Hellebrand (U Paderborn)
2.1 BPPT – Bulk Potential Protection Technique for Hardened Sequentials, L.Nofal, A.Evans (iRoC), A.Li, G.Guo (China Institute of Atomic Energy), Y.Li (IHP), S.Baeg (Hanyang U), L.Chen, R.Liu, H.B.Wang, M.Chen (U Saskatchewan), S.-J.Wen, R.Wong (Cisco)
2.2 Comprehensive Analysis of Sequential Circuits Vulnerability to Transient Faults Using SMT, G.Bany Hamad, K.Ghaith, O.A.Mohamed, Y.Savaria (Ecole Polytech. Montreal and Concordia U)
2.3 Design-Time Reliability Evaluation for Digital Circuits, M.Abuafalga, A.Bystrov (Newcastle U)

12:45 – 14:00: Lunch

14:00 – 15:00: Session 3 – Characterization & Debug
Moderator: M.Sonza Reorda (Politec. di Torino)
3.1 Relaxing DRAM Refresh Rate through Access Pattern Scheduling; A Case Study on Stencil-based Algorithms, K.Tvetenoglu, D.Nikolopoulos, G.Karakostantis (Queen’s U Belfast)
3.2 Voltage Margins Identification on Commercial x86-64 Multicore Microprocessors, G.Papadimitriou, M.Kalrakis, A.Chatzidimitriou, C.Magalinos, D.Gizopoulos (U Athens)
3.3 A Generic Embedded Sequence Generator for Constrained-Random Validation with Weighted Distributions, XShi, N.Nicolic (McMaster U)

Tuesday July 4, 2017

08:30 – 09:30: Session 6 – Devices Reliability & Debug
Moderator: H.-J.Wunderlich (U Stuttgart)
6.1 An On-line Test Strategy and Analysis for a 1TIR Crossbar Memory, M.Escudero-López, F.Moll, A.Rubio (UPC), L.Vourkas (PUCC)
6.2 Reliability Analysis of MTJ-based Functional Module for Neuromorphic Computing, J.Vatajelu, L.Angel (TIMA Lab)
6.3 Revisiting Random Access Scan for Effective Enhancement of Post-silicon Observability, B.Kumar, A.Jindal, J.Tedu, B.Pandey, V.Singh (IIT Bombay)

09:30 – 10:45: Special Session 6 – Aging
Organizer/Moderator: A.Paschalis (U Athens)
5.1 Variation Tolerant BIST Monitoring in SRAM Cells, Y.Sikou, Y.Tsiafakou (U Ioannina)
5.2 Dynamic aging compensation and Safety measures in Automotive environment, S.Mhira, V.Huard, A.Benhassain, F.Cacho, S.Naudet, A.Jain, C.Parthasarathy (ST), A.Bravaix (ISEN)
5.3 Minimal Exercise Vector Generation for Reliability Improvement, M.Pappireddy, S.Hadjitheophanous, V.Soteriou, P.V.Gratz, M.Michael (Texas A&M U, Cyprus U Technology and U Cyprus)

10:45 – 11:45: Session 7 – On-Line Test
Moderator: A.Troni (Politec. di Torino)
7.1 On-Line Test on a Multicore Processor System, A.C.Codazzi, A.Paschalis (U Athens), E.Panfili (U Siena)
7.2 Over-Flow – An On-line Test Solution for Hardened SRAMs, A.Paschalis (U Athens), P.Oliveira (IPEN, Brazil), V.Loukogeorgakis (Broadcom)
7.3 Reliability Analysis of MTJ-based Functional Module for Neuromorphic Computing, M.A.Eldridge, J.M.Smith, J.Vatajelu, L.Angel (TIMA Lab)
7.4 On-Line BIST/DFP for Embedded Memories, R.Camilleri (SASTRA, India), C.Prasad (SASTRA, India), R.Ipek (University of Illinois)

11:45 – 12:45: Session 8 – New Test Concepts
Moderator: M.Sonza Reorda (Politec. di Torino)
8.1 A Simple and Effective Approach for the Testability Evaluation of DRAMs, A.Ibrahim, H.Kerkhoff (U Twente)
8.2 A New Built-In Monitor for Memory Subsystem, V.Vesely (U Twente), V.Ne spec (U Twente), E.Nowak (U Twente), J.P.Graaf (U Twente)
8.3 An Effective Fault Localization Methodology for Hardened Memories, A.Klockmann (U Potsdam), V.Loukogeorgakis (Broadcom)

12:45 – 14:00: Lunch
09:45 – 10:45: Session 7 – Reliability Evaluation
Moderator: G.Karakonstantis (QUB)
7.1 SIFI: AMD Southern Island GPU Microarchitectural Level Fault Injector, A.Vallero, S.Di Carlo (Politecnico di Torino), D.Gizopoulos (U Athens)
7.3 Simulation-based Analysis of FF Behavior in Presence of Power Supply Noise, Y.Miura, T.Yamamoto (Tokyo Metropolitan U)
10:45 – 11:15: Coffee Break
11:15 – 12:15: Special Session 3 – Robustness in Automotive Electronics - an industrial overview of major concerns
Organizer/Moderator: P.Bernardi (Politecnico di Torino)
S3.1 Online test strategies and ISO 26262, a gap to fill, G.Ballan (Xilinx), F.Venini (Xilinx and Politecnico di Torino)
S3.2 In Field Program Memory Logical Sector Repair Feature for Powertrain Highend Automotive Microcontrollers, K.C.Ramamoorthy, R.Ullman (Infineon)
S3.3 ISO26262 compliant Core Self-Test libraries for automotive, A.Sansonetti (ST Microelectronics), E.Sanchez (PoliTeck)
12:15 – 13:30: Lunch
13:30 – 14:10: Session 8 – Attacks Resilience
Moderator: L.Polian (U Passau)
8.1 Cache-timing attacks countermeasures and error detection in euclidean addition chains based scalar multiplication on elliptic curves, F.-Y.Dosso, P.Veron, (U Toulon)
8.2 Jamming Resistant Encoding For Non-Uniformly Distributed Information, B.Karp, Y.Berkowitz, O.Keren (Bar-Ilan U)
14:10 – 14:45: Break
14:45 – 15:45: Session 9 – FPGAs
Moderator: C.Lopez-Ongil (U Carlos III de Madrid)
9.1 Analysis of Radiation-induced Cross Domain Errors in TMR Architectures on SRAM-based FPGAs, L.Boragno (Politecnico di Torino)
9.2 Field Profiling & Monitoring of Payload Transistors in FPGAs, D.Cheng, A.Majumdar, X.Wang, N.Chong (Xilinx)
16:00: Social Event & Dinner

Wednesday July 5, 2017
08:30 – 09:15: FEDFRO Keynote Talk 2
Rigorous System Design, J.Sifakis (Verimag)
09:15 – 09:30: Break
09:30 – 10:30: Special Session 4 – Cross-Layer Reliability
Organizers/Moderators: M.Shafique (TU Wien) and A.Raghanathan (Purdue U)
S4.1 Design of Efficient Error Resilience in Signal Processing and ControlSystems: From Algorithms to Circuits, J.Ahman (U Texas at Austin), S.Banerjee, A.Chatterjee (Georgia Tech)
S4.2 Reliability of Computing Systems: from Flisp Flops to Variables, GDi Natale, M.Kooli, A.Bosio (LIRMM), M.Portolan, R.Leverge (TIMA Lab)
S4.3 Designing Reliable Reconfigurable Architectures by Exploiting Process Variability, D.Soudris (NTU Athens)
10:30 – 11:30: Session 10 – Posters & Coffee Break
10.1 On Comparison of Robust Configurable FPGA Encoders for Dependable Industrial Communication Systems, P.Feif, F.Hosseinzadeh, H.T.Vierhaus (BTU Cottbus-Senftenberg)
10.3 Handling of Permanent Faults in Dynamically Scheduled Processors, F.Mühlbauer, L.Schröder, M.Scholz (U Potsdam)
10.4 Polyphonic PUF: Exploiting Reconfigurability of CPU+PUF SoC to Resist Modeling Attack, J.Ye, Y.Gong, Y.Hu, X.Li (Chinese Academy of Sciences)
10.5 Soft Error Analysis of MTJ-based Logic-in-Memory Full Adder: Threats and Solution, J.Talafy, H.Zarandi (Amirkabir U of Technology)
10.7 Test Pattern Generation to Detect Multiple Faults in ROBDD-based Combinational Circuits, T.Shah (ITT Bombay), A.Matrosova (Tomsk State U), V.Singh (ITT Bombay)
10.8 Trojan Circuits Preventing and Masking in Sequential Circuits, A.Matrosova, E.Mitrofanov, S.Ostanin, I.Kirienko (Tomsk State U)
11:30 – 12:30: Session 11 – Hardware Security
Moderator: A.Kakarountas (U Thessaly)
11.1 Hardware Trojan Detection and Classification based on Steady State Learning, M.Oya, M.Yanagisawa, N.Togawa (Waseda U and NEC)
11.2 Weighted Logic Locking: A New Approach for IC Piracy Protection, N.Karousos, K.Pexaras, L.Karybali, E.Kalligeros (U Aegean)
11.3 Hardware Trojans Classification for Gate-level Netlists Using Multi-layer Neural Networks, K.Hasegawa, M.Yanagisawa, N.Togawa (Waseda U)
12:30 – 13:45: Lunch
13:45 – 14:45: Special Session 5 – Energy-Efficient Resilience
Organizers/Moderators: M.Shafique (TU Wien) and A.Raghanathan (Purdue U)
S5.2 Energy-efficient and Error-resilient Iterative Solvers for Approximate Computing, A.Scholl, C.Braun, H.J.Wunderlich (U Stuttgart)
S5.3 Temporal Redundancy Latch-based Architecture for Soft Error Mitigation, R.Schmidt, A.Garcia-Ortiz, G.Fey (U Bremen and DLR)
14:45 – 15:00: Break
15:00 – 16:00: Session 12 – Monitoring & Sensing
Moderator: M.Dasgupta (U Western Macedonia)
12.1 Reliable Gas Sensing with Memristive Array, A.Deyymo, A.Jabir (Oxford Brookes U), J.Mathew (IIT Patna), E.Martinei, C.Di Natale, M.Ottavi (U Rome)
12.2 Investigation of Critical Path Selection for In-Situ Monitors Insertion, F.Cacho, A.Benhassain, R.Shah, S.Mhira, V.Huard (STMicroelectronics), L.Angel (TIMA Lab)
12.3 On-Line Monitoring of System Health Using On-Chip SRAMs as a Wearout Sensor, W.Kim, T.Liu, L.Mikos (Georgia Tech)
16:00 – 16:15: Coffee Break
16:15 – 17:15: Session 13 – Fault Detection and Tolerance
Moderator: S.Nikolaidis (Aristotle U Thessaloniki)
13.1 Instruction-Based Self-Test for Delay Faults Maximizing Operating Temperature, N.Hage, R.Galve (IIT Bombay), M.Fujita (U Tokyo), V.Singh (IIT Bombay)
13.2 Fast Power Overhead Prediction for Hardware Redundancy-based Fault Tolerance, S.Scharoba, H.T.Vierhaus (Brandenburg U Technology)
13.3 Probabilistic Error Detection and Correction in Switched Capacitor Circuits Using Checksum Codes, M.Montaz, S.Banerjee, A.Chatterjee (Georgia Tech)
17:15 – 17:30: Symposium Closing Remarks