Wednesday June 27, 2012
07:30 – 09:00: Symposium Registration
09:00 – 10:00: Opening Session
09:00 – 09:15: Welcome Message
  M.Nicolaidis (TIMA Lab), R.Canal (UPC), General Chairs
  D.Gizopoulos (U Athens), X.Vera (Intel Barcelona Research Center), Program Chairs
09:15 – 10:00: Keynote Talk
  Resilient Processors for Reliability and Energy Efficiency
  Antonio Gonzalez (Director, Intel Labs, UPC, Barcelona)
10:00 – 10:20: Coffee Break
10:20 – 11:40: Session 1 – SEU Tolerance
  1.1 Error Detection and Correction of Single Event Upset Tolerant Latch, Norhuzaimin Julai
      (School of Electrical,Electronic and Computer), Alexandra V Yakovlev (University of
      Newcastle upon Tyne), Alexander Bystrov (University of Newcastle Upon Tyne)
  1.2 SETTOFF: A Fault Tolerant Flip-Flop for Building Cost-efficient Reliable Systems, Yang LIN
      (University of Southampton), Mark Zwolinski (Univ. of Southhampton)
  1.3 SEU Tolerant Robust Memory Cell Design, Shayan Mohammed (Indian Institute of Science),
      Virendra Singh (Indian Institute of Science (IISc)), Adit Singh (Auburn University), Fujita
      Masahiro (university of tokyo)
  1.4 Single Event Upset Resilient Logic Design Optimization, Sujan Pandey (NXP
      Semiconductors)
11:40 – 12:00: Coffee Break
12:00 – 13:00: Session 2 – Reconfigurable Logic
  2.1 SEU-X: a SEu Un-eXcitability prover for SRAM-FPGAs, Cinzia Bernardeschi (Department of
      Information Engineering, University of Pisa), Luca Cassano (University of Italy), Andrea Domenici
      (Department of Information Engineering, University of Pisa)
  2.2 Analyzing and Alleviating the Impact of Errors on an SRAM-based FPGA Cluster, Arwa Ben
      Dhia (Telecom ParisTech), Lirida Naviner (Institut Telecom, Telecom ParisTech, CNRS
      LTCI), Philippe Matherat (Telecom ParisTech)
  2.3 Transparent Structural Online Test for Reconfigurable Systems, Mohamed Abdelfattah
      (Universitat Stuttgart), Lars Bauer (Karlsruhe Institute of Technology (KIT)), Claus Braun
      (University of Stuttgart), Michael Imhof (Universitaet Stuttgart), Michael Kochte (University of
      Stuttgart), Hongyan Zhang (Karlsruhe Institute of Technology (KIT)), Joerg Henkel
      (University of Karlsruhe, Germany), Hans-Joachim Wunderlich (Universitat Stuttgart)
13:00 – 14:00: Lunch
14:00 – 14:45: Special Session 1 – Embedded Tutorial: Online Security Monitoring for ICs
  Miron Abramovic (Tiger’s Lair)
14:45 – 15:00: Coffee Break
15:00 – 16:00: Session 3 – Radiation Experiments and Analysis
  3.1 A Real-Case Application of a Synergetic Design-Flow-Oriented SER Analysis, Miguel Vilchis
      (LSI Corporation), Ramnath Venkatraman (LSI Corporation), Enrico Costenaro (iRoC
      Technologies), Dan Alexandrescu (iRoC Technologies)
  3.2 Fault-Based Reliable Design-On-Upper-Bound of Electronic Systems for Terrestrial
      Radiation Including Muons, Electrons, Protons and Low Energy Neutrons, Eishi Ibe (Hitachi,
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Lrd.), Tadanobu Toba (Hitachi, Ltd.), Ken-ichi Shimbo (Hitachi, Ltd.), Hitoshi Taniguchi (Hitachi, Ltd.)

3.3 Neutrons Radiation Test of Graphic Processing Units, Paolo Rech (UFRGS), Caroline Aguiar (UFRGS), Ronaldo Ferreira (Universidade Federal do Rio Grande do Sul), Christopher Frost (ISIS), Luigi Carro (Universidade Federal do Rio Grande do Sul)

16:00 – 16:20: Coffee Break

16:20 – 17:20: Session 4 – Circuit Degradation

4.1 The Influence of Clock-Gating On NBTI-Induced Delay Degradation, Jorge Semiao (Instituto Superior Engenharia - Universidade do Algarve), Jackson Pachito (University of Algarve), Celestino Martins (University of Algarve), Marcelino Bicho Dos Santos (IST/INESC-ID), Isabel Teixeira (INESC-id), Joao Paulo Teixeira (IST, Lisboa Technical University)

4.2 Relation between HCI-induced performance degradation and applications in a RISC processor, Olivier Heron (CEA LIST), Clement Bertolini (CEA Saclay Nano-Innov), Nicolas Ventroux (CEA LIST), François Marc (Université de Bordeaux 1)

4.3 Do More Camera Pixels Result in a Better Picture?, Israel Koren (University of Massachusetts), Zahava Koren (University of Massachusetts at Amherst), Glenn Chapman (Simon Fraser U.)

17:20 – 17:50: Coffee Break

17:50 – 19:15: Special Session 2 – Panel: Cross Layer Reliability - Challenges and Standards Requirements

Organizers/Moderators: Michael Nicolaides (TIMA), Shi-Jie Wen (Cisco)

20:00: Welcome Reception

Thursday June 28, 2012

09:00 – 10:00: Session 5 – Memories and 3D Integration

5.1 Low Power embedded DRAM Caches using BCH code Partitioning, Pedro Revirigoso (Universidad Antonio de Nebrija), Alfonso Sancez-Macias (Universidad Nebrija), Juan Maestro (Universidad Nebrija)

5.2 On the functional test of L2 caches, Matteo Sonza Reordia (Politecnico Di Torino), Ernesto Sanchez (Politecnico di Torino), Michele Riga (Politecnico di Torino)

5.3 Through-Silicon-Via Built-In Self-Repair for Aggressive 3D Integration, Michael Nicolaides (TIMA Laboratory), Vladimir Pasca (TIMA Laboratory), Lorena Anghel (TIMA Laboratory)

10:00 – 10:20: Coffee Break

10:20 – 11:20: Special Session 3 – Variability and Bugs: How to find them?

Organizer: P.Gupta (UCLA)
S3.1 Measuring and Monitoring Variability, P.Gupta (UCLA)
S3.2 Correlating Models and Silicon in the Presence of Variability, V.Chandra (ARM)
S3.3 Effective Post-Silicon Validation, S.Mitra (Stanford U)

11:20 – 11:40: Coffee Break

11:40 – 12:40: Session 6 – Miscellaneous

6.1 Test Access Mechanism for Chips with Spare Identical Cores, Ozugr Sinanoglu (New York University - Abu Dhabi)

6.2 RiIF - Reliability Information, Adrian Evans (Cisco Systems Inc.), Dan Alexandrescu (IoR Technologies), Enrico Costenaro (IoR Technologies)

6.3 On Line Monitoring of RF Power Amplifiers Output Power by means of Embedded Temperature Sensors, Josep Altet (Univ Politecnica de Catalunya), Diego Mateo (DEE - UPC), Didac Gomez (DEE - UPC)

12:40 – 13:40: Lunch

13:40 – 14:40: Special Session 4 – Panel: Reliability of hard real-time systems in 32nm and beyond: who will solve the challenges?

Organizer/Moderator: S.Hamdioui (Delft U)

14:40 – 15:40: Session 7 – Posters

7.1 A Fault Attack Robust True Random Number Generator, Eberhard Boehl (Robert Bosch GmbH), Jorge Merchan (Bosch), Markus Ihle (Bosch)

7.2 Architectural Vulnerability Aware Checkpoint Placement in a Multicore Processor, Atieh Lofti (University of Tehran), Arash Bayat (University of Tehran), Saeed Safari (University of Tehran)

7.3 Built-In Test of MEMS Capacitive Accelerometers for Field Failures and Aging Degradation, Alvaro Gomez-Pau (UPC), Ricardo Sanahuja (UPC), Luz Balado (UPC), Joan Figueras (UPC)

7.4 Evaluation of Test Algorithms Stress Effect on SRAMs under Neutron Radiation, Georgios Tsiliogiannis (Irmr), Luigi Dillilo (LRM), Alberto Bosio (LRM), Patrick Girard (LRM), Aida Todri (LRM), Arnaut Virazel (LRM), Antoine Touboul (IES/UM2), Frederic Wrobel (IES/UM2), Frederic Saigné (IES)

7.5 Event-Driven On-Line Co-Simulation with Fault Diagnostic, Mikhail Baklashov (Intel Corporation)

7.6 Fault Detection Capabilities of a Timing and Control Flow Checker for Hard Real-Time Systems, Julian Wolf (Universitaet Augsburg), Bernhard Fechner (Universitaet Augsburg), Theo Ungerer (Universitaet Augsburg)

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7.7 Fault Missing Rate Analysis of the Residue Number based Fault-Tolerant FIR Design, Zhen Gao, Wenhui Yang (Xiamen University), Xiang Chen (Tsinghua University), Ming Zhao (Tsinghua University), Jing Wang (Tsinghua University)

7.8 Functional Level Embedded Self-Testing for Walsh Transform Based Adaptive Hardware, Ariel Burg (Bar-Ilan University), Osnat Keren (Bar Ilan University)

7.9 Gatewaying IEEE 1149.1 and IEEE 1149.7 Test Access Ports, Francisco Fernandes (FEUP - Faculdade de Engenharia da Universidade do Porto), Ricardo Machado (FEUP - Faculdade de Engenharia da Universidade do Porto), Jose Ferreira (University of Porto), Manuel G. Gericota (ISEP)

7.10 Neutron-Induced Soft Error Rate Estimation for SRAM Using PHITS, Shusuke Yoshimoto (Kobe university), Takuro Amashita (Kobe University), Masayoshi Yoshimura (Kyushu University), Yusuke Matsunaga (Kyushu University), Hiroto Yasuura (Kyushu University), Shintaro Izumi (Kobe University), Hiroshi Kawaguchi (Kobe University), Masahiko Yoshimoto (Kobe University)

7.11 Pilot Symbol Driven Monitoring of Electrical Degradation in RF Transmitter Systems Using Model Anomaly Diagnosis, Sabyasachi Deyati (Georgia Institute of Technology), Aritra Banerjee (Georgia Tech), Abhijit Chatterjee (Georgia Institute of Technology)