CLASS – Clockless Logic, Analysis, Synthesis & Systems

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Motivation

• Development cost of advanced ASICs is becoming too great for low volume, DoD applications

• But DoD applications require capabilities enabled by advanced ASICs

Clockless Logic addresses many of the ASIC Development Cost Drivers

- Improves Reuse
- Simplifies Timing Design
- Reduces Power
- Reduces Noise
- Eliminates Fab Passes
CLASS Program Objectives

- Enable Very Complex SoC Designs by Overcoming Approaching Limits of Clocked Design
  - Timing Closure
  - Noise/EMI
  - IP Reuse
  - Power Management

- Key Program Goals:
  - Enable design of clockless circuits
  - Overcome clocked design inertia
  - Make clockless design available ASAP to DoD
Need for CLASS Program

• CLASS program develops critical enablers for design of clockless circuits
  • ECAD – automated clockless logic implementation and optimization
  • Multiple integrated clockless design styles providing range of power, performance, complexity, robustness
  • IP
  • Methodology

• CLASS Program demonstrates clockless in complex, highly-constrained, DoD system
  • Prove design methodology and tools
  • Provide Direct comparison of clockless system to clocked system
  • Demonstrate benefits of clockless technology in compelling defense application
CLASS Impact

CLASS will move clockless design into the mainstream

Strategy:
- Complete EDA infrastructure
- Support diverse technologies
- Show clear benefits to DoD SoC design houses
- A vs. B (clocked vs. clockless) benchmark
- Provide Compelling SoC Demonstration
- Technology Transfer – Supported by commercial companies
Approach

• Build on proven clockless design toolset from Handshake Solutions
• Support multiple clockless logic styles for increased performance, power, reliability trade space
• Enhance with Optimizations
• Demonstrate value of asynchronous design in compelling DoD application
• Compare asynchronous implementation to equivalent synchronous implementation
• Prime Contractor, Application, Demonstration Chip Design
• Null Convention Logic, Demonstration Chip Design
• Mobius Tool Flow
• Handshake Technology, Tool Flow
• Handshake Optimizations, NCL Optimizations, High-Speed Pipelines
• High-Speed Pipelines
• Locally Clocked Dynamic Logic
• Substrate Noise Coupling
• Integrated Testability Approach
• Combining benefits of broad range of Asynchronous Technologies

• Handshake Circuits
  • Very low power
  • Production design flow
  • Standard Libraries

• Null Convention Logic
  • Very low power
  • Delay insensitive

• Mousetrap High Speed Pipelines
  • Standard libraries
  • Integrated high-speed capability

• Locally Clocked Dynamic Logic
  • Highest speed capability
Clockless Design Tools

Boeing Technology | Phantom Works

CLASS

- Proven Tool Framework from Handshake Solutions
  - Simulation
  - Synthesis
  - Test
- Expanded integration with standard back-end tools
- Support for Artisan 130nm libraries
- Optimizations to push to higher performance capabilities
- Integration of High-speed pipeline (Mousetrap) technology
• Mobius from Codetronix
  • High-level Design
  • Flexibility to incorporate other asynchronous logic styles
  • Path to delay insensitive Null Convention Logic from Theseus Logic

• Integrated test strategy
• Improve power, performance for Handshake circuits and NCL circuits

• Circuit transformations
  • Peephole optimizations
  • Control re-synthesis

• Design Flow optimizations
  • Improved parallelism between data path and control path
  • Constraint driven synthesis and layout
  • Design templates
- Initial Tool Integration & Test Chip – Integrate async design tools into Boeing foundry-flexible design flow and demonstrate in silicon a significant block from the demonstration chip
- Enhanced Tools & Demonstration Chip – Develop & integrate complete async design flow and demonstrate in silicon significant benefits of clockless design using complete ASP
- Horizon Tools & Demonstration – Develop extended tool capabilities necessary to overcome clocked design inertia and demonstrate with ASP
Initial Tools & Test Chip

- Initial tool capabilities installed
- Proven with 3 test chips
- IBM 130nm CMOS8RF
- Released on Trusted Foundry Multiproject Wafer
- Estimated Delivery: May 15

T2 Test Chip
- Handshake Circuits
- 3.2M transistors (async logic)
- 1.5M bits RAM
- 427 I/O
Enhanced Tools

- Initial Optimizations incorporated
  - Handshake Circuits
  - NCL Circuits
- NCL technology integrated into Mobius tools
- Demonstration chip combines
  - Handshake Circuits
  - NCL Circuits
  - LCDL Circuits
  - Synchronous Circuits
• Compelling demonstration of async benefits
  • Improved Design Time
  • Improved Power/Performance
  • Improved Noise Characteristics

• DoD Relevant Circuit
  • Advanced Sensor Processor
  • Mix of processing styles
    – DSP
    – Numerical Methods
  • Integrated memory (25 Mbits)
  • Integration into synchronous system
  • Challenging performance (180 MHz)
  • Challenging complexity (50M XSTRS)

• Trusted Foundry release in IBM 130nm CMOS8RF
• Compare to Equivalent Synchronous Chip
Demonstration
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Lab View Diagnostics
National Instruments

Real-Time

Off-Line

Source Data

Embedded PC
National Instruments

Results

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• Complete development and integration of optimizations
• Complete integration of Mousetrap technology
• Initial system performance analysis capability
• Demonstrated using ASP circuits
Key Products

Clockless Design Infrastructure

A vs. B Comparison

Asynchronous Advanced Sensor Processor ASIC

Real-time Demonstration

Testability Techniques
• Clockless Design is enabler for advanced DoD systems

• CLASS Program is lowering the barriers to adoption of clockless logic

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