A Novel Design Method of Asynchronous Bundled-Data Transfer Circuits Considering Characteristics of Delay Variations

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Objective

Main objective

Developing an SDI-model-based design methodology which utilizes delay information in local parts of a chip

Goal of this presentation

Explain characteristics and models of delay variations in local parts of a chip

Present a new design method of the strobe signal circuit which generates timing information based on asynchronous bundled-data transfer scheme
Agenda

- Introduction
  - Bundled-data transfer circuits based on the Scalable-Delay-Insensitive model
- Characteristics and models of delay variations
- Variation-aware delay cell libraries and selectable delay line
- Evaluation result
- Conclusion
Introduction (1)

- Delay variations have been an issue for VLSI design
  - The characteristics of delay variations caused by various factors are different
  - They have not been considered in traditional delay models or asynchronous design style, therefore, suffered large performance overhead

- Propose a new method for designing high performance asynchronous bundled-data transfer circuits considering \textit{the characteristics of delay variations}
In asynchronous systems, delay model has a great impact on the design and the resulting circuits.

In local parts of a chip, delay models and methodologies which utilize delay information should be used for high performance and dependable circuits.

*Scalable-delay-insensitive* model is a basic delay model considering delay variations due to various factors in local parts of a chip.
SDI–model–based design

Implementation rule

If the relation $K \cdot D_1 < D_2$ holds for a given $K$, $t1$ precedes $t2$ for any possible delay variations that can occur through system’s lifetime.

In the SDI–model–based design, delay scaling variation factor $K (K \geq 1)$ represents the margin that guarantees the correct operations.
Bundled-data transfer circuits based on the SDI model

- **Fast path:**
  - Maximum delay paths in a combinational circuit.
  - Combinational circuits may be constructed by any component.

- **Slow path:**
  - Strobe signal path with delay line
  - Delay line is constructed by AND-gate chains or BUF-gate chains

\[ K \cdot D_{cc\_est} < D_{st\_est} \]

Propose the following two methods to design strobe signal circuits which make \( K \) value to be nearly one
- Variation-aware delay cell libraries
- Selectable delay line
Main sources of delay variations

- **Process variations**
  - Variations due to lack of perfect control of the fabrication process

- **Environmental variations**
  - Supply voltage and threshold voltage change due to DVS (Dynamic Voltage Scaling)
  - Temperature variations due to electric current flowing

- **Temporal variations** due to dynamic signal transitions
  - Crosstalk due to signal transitions between adjacent wires
  - Power noise and IR-drop
Process variation characteristics (1)

- Unpredictable variations
- Delay variations of PMOS transistors are completely different from those of NMOS transistors
- Traditional approach using worst-case static timing analysis methods may sometimes have over-pessimistic results
  - Statistical or probabilistic timing analysis methods have been proposed

- Process variations can be classified as two classes
  - Systematic process variations
  - Random process variations
Process variation characteristics (2)

Process variation features in a chip

- **Systematic variation**
  - Delay variations of neighborhood elements are correlative

- **Random variations**
  - Exhibit almost the completely randomness even in the neighborhood elements

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[Shin-ichi Ohkawa et al. 2004]

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nMOS $V_T$:
$L = 0.1 \mu m$, $W = 0.8 \mu m$
($I_{DS} = 0.8 \mu A$, $V_{DS} = 1.2 V$)

$3^{rd}$-metal Resistance:
$W = 1 \mu m$, $L = 100 \mu m$
($1^{st}$-metal/$3^{rd}$-metal/$5^{th}$-metal)
Process variation models in local parts

**Systematic process variation**
- Both a combinational circuit and the corresponding strobe signal circuit are under the same influence.
- Use the traditional corner models: 
  - $(PMOS,NMOS) = (Center,Center)$, $(Fast,Fast)$, $(Fast,Slow)$, $(Slow,Fast)$, $(Slow,Slow)$

**Random process variations**
- Path delays exhibit a normal distribution with the standard deviation $\sigma$.
- Margin: $\text{Delay (strobe signal)} - 2\sigma > \text{Delay (combinational circuit)} + 2\sigma$
Process variation models in local parts

Systematic process variation
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Random process variations
- Path delays exhibit a normal distribution with the standard deviation \(\sigma\)
- Margin: Delay (strobe signal) \(- 2\sigma >\) Delay (combinational circuit) \(+ 2\sigma\)
Voltage variations due to DVS

- **Characteristics**
  - **Predictable variations**
    - The value of supply voltage and threshold voltage are intentionally changed
    - The performance overhead can be reduced if an appropriate delay line for each voltage is selected
  - **Models in local parts**
    - The whole chip or a block of voltage-islands change uniformly

- Concept of selectable delay line

- The voltage of a combinational circuit is the same as that of the corresponding strobe-signal-generation circuit
Temperature variations

**Characteristics**

- **Temperature can be measured using an embedded temperature sensor**
  - The performance overhead can be reduced if an appropriate delay line for each temperature is selected
- **The sensor and related analog circuits would cause area overheads**
  - Tradeoff between performance and area

**Models in local parts**

- **The temperature of a local part in a chip changes uniformly**
- The temperature of a combinational circuit is the same as that of the corresponding strobe-signal-generation circuit
Temporal variations

- **Characteristics**
  - **Unpredictable variations**
    - Crosstalk, supply voltage noise, IR-drop, etc...
  - **Exhibit almost the completely different even in the neighborhood elements**
    - Depend on dynamic signal transitions

- **Models in local parts**
  - Path delays exhibit a normal distribution with the standard deviation $\sigma$
  - Margin: $\text{Delay (strobe signal)} - 2\sigma > \text{Delay (combinational circuit)} + 2\sigma$
Characteristics and models of delay variations for bundled-data transfer circuits

**Characteristics**
- Each combinational circuit has different delay variation characteristics
- Variation factor characteristics in local parts

<table>
<thead>
<tr>
<th></th>
<th>Predictability (Measurability)</th>
<th>Affect on a combinational circuit and a strobe-signal circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Systematic process</td>
<td>×</td>
<td>Correlative</td>
</tr>
<tr>
<td>Random process</td>
<td>×</td>
<td>Independent</td>
</tr>
<tr>
<td>DVS</td>
<td>○</td>
<td>Correlative</td>
</tr>
<tr>
<td>Temperature</td>
<td>○</td>
<td>Correlative</td>
</tr>
<tr>
<td>Temporal</td>
<td>×</td>
<td>Independent</td>
</tr>
</tbody>
</table>

**Models**
- Correlative: The same affect on both a combinational circuit and the corresponding strobe signal circuit
- Independent: Normal distribution with standard deviation $\sigma$ for path delays and the margin is $4\sigma$
Variation-aware delay cell libraries

- Delay variations of each standard cell are different
- The characteristics of delay variations of combinational circuits are completely different

Propose the following methods to reduce performance overheads due to delay variations

- Design delay cells exhibiting a wide variety of delay variation characteristics in advance
- Select the most appropriate delay cell which has almost the same characteristics of delay variations of a synthesized combinational circuit
Delay cells with a wide variety of delay variations

- The characteristics of delay variations strongly depend on the depth of transistor chain in the direction from the source to the drain.

- **Buffer-Type delay cell**
  - (a) Standard structure
  - (b) NMOS-chained structure
  - (c) PMOS-chained structure
Delay cells with a wide variety of delay variations

- The characteristics of delay variations strongly depend on the depth of transistor chain in the direction from the source to the drain.
- Buffer-Type delay cell

(a) Standard structure

![Diagram of Standard structure](image)

![Graph showing systematic process variation](image)

- **Systematic process variation**
  - **Scaling ratio**
  - **Standard**
  - **NMOS-chained**
  - **PMOS-chained**

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Delay cells with a wide variety of delay variations

The characteristics of delay variations strongly depend on the depth of transistor chain in the direction from the source to the drain.

Buffer-Type delay cell

(a) Standard structure

Systematic process variation

Select PMOS-chained structure

Select NMOS-chained structure
Design flow using variation-aware delay cell libraries

1. Decide standard values and the ranges of variations for each factor
2. Delay values of standard cell libraries and delay cell library are evaluated
3. Synthesize a combinational circuit
4. Evaluate delay variations of the maximum delay paths of the synthesized circuit
5. Select the most appropriate delay cell which $K$ value is the minimum number (nearly one)
Selectable delay line

- In bundled-data transfer circuits, the delay of a strobe signal circuit must be always larger than the delay of the corresponding combinational circuit
- Large overhead due to all the variation factors

- In synchronous circuits, the latency between registers which is given by the inverse number of clock frequency can be changed dynamically
  - Overhead due to predictable delay variations can be reduced

- Need to change the timing signal dynamically according to the predictable environmental changes for high performance bundled-data transfer circuits
Selectable delay line for DVS

- Design the most appropriate delay line for each voltage in advance
- Select an appropriated delay line in accordance with dynamic voltage changes using voltage scaling information

The power consumption is small because only the selected delay line consumes power
Selectable delay line for DVS

- Design the most appropriate delay line for each voltage in advance
- Select an appropriated delay line in accordance with dynamic voltage changes using voltage scaling information

Speculative completion method

- The power consumption is small because only the selected delay line consumes power
Evaluation setup

- **90nm process technologies**: generic version, low-power version
- **Delay evaluation** using HSPICE analog simulator and process model parameters given by a fabrication vendor

<table>
<thead>
<tr>
<th></th>
<th>Standard values</th>
<th>Variation ranges</th>
</tr>
</thead>
<tbody>
<tr>
<td>Systematic process variations (PMOS/NMOS)</td>
<td>(Center / Center)</td>
<td>(Fast/Fast) (Fast/Slow)</td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>1.0</td>
<td>0.8 ~ 1.1</td>
</tr>
<tr>
<td>Temperature [°C]</td>
<td>50</td>
<td>25 ~ 100</td>
</tr>
<tr>
<td>Random process variations and temporal variations</td>
<td>Mean delay</td>
<td>Standard deviation $\sigma$</td>
</tr>
</tbody>
</table>

- **Evaluation target**: ISCAS89 benchmark circuits (30 circuits)
- **Logic synthesis** using the Synopsys Design Compiler
  - Select the minimum “Delay x Energy” circuit
Evaluation result (1): Performance

- Buffer type delay cell, 90nm generic process, $\sigma = 1/20$ mean delay

Using BUF-type delay cell libraries

- K values are between 1.3 and 2.0 for all the benchmark circuits
- The performance overhead which is calculated as $K - 1$ can be reduced 20% using the proposed delay cell library
- It can be reduced about 45% using the proposed selectable delay line
Evaluation result (2): Average performance overhead

- The performance overhead can be reduced about 20% using the proposed variation-aware delay cell library for all the conditions.
- It can be reduced more 20% using the proposed selectable delay line.

\[ \sigma = \frac{1}{20} \text{ mean delay} \]
Evaluation result (3): Energy consumption

Average reduction ratio of energy consumption of strobe-signal-generation circuits

- Energy consumption can be reduced more than 50 percents by using the proposed variation-aware delay cell libraries in the 90nm process technologies.
- The overhead of the select circuit and the merge circuit in the proposed selectable delay line is small.
Evaluation result (4): Wide variety of delay variations

The number of selected delay cell type at the last condition

<table>
<thead>
<tr>
<th></th>
<th>90nm generic</th>
<th>90nm low-power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BUF-type</td>
<td>AND-type</td>
</tr>
<tr>
<td>Standard structure</td>
<td>120</td>
<td>15</td>
</tr>
<tr>
<td>NMOS-chained structure</td>
<td>0</td>
<td>84</td>
</tr>
<tr>
<td>PMOS-chained structure</td>
<td>0</td>
<td>21</td>
</tr>
</tbody>
</table>

- In this 90 generic technology, NMOS transistors are dominant to delay variations.
- In this 90 low-power technology, PMOS transistors are dominant.

The proposed three different structures are effective because the characteristics of delay variations are different according to the technology.
Conclusion

- Proposed variation-aware delay cell libraries which consist of delay cells exhibiting a wide variety of delay variation characteristics
- Proposed selectable delay line in which we can select an appropriate delay line in accordance with dynamic voltage changes
- Show some evaluation results for the variation factor $K$ which represents the margin that guarantees the correct operation based on the SDI model
  - The performance overhead can be reduced about 40% compared to conventional bundled-data transfer circuits
Future work

- Implement a CAD tool that supports determining the appropriate value of K based on the proposed method
- Consider the yield of asynchronous circuits based on the Scalable-Delay-Insensitive model
Affect of random variations

- Average performance overhead using a selectable delay line with variation-aware delay cell libraries

![Bar chart showing average performance overhead for generic AND, generic BUF, lowpower AND, and lowpower BUF with standard deviations σ=1/10, σ=1/20, and σ=0.

- If random variations which include random process variations and temporal variations become more serious, the performance overhead of bundled-data transfer circuits become extremely large.
Selection method

1. Evaluate delay values of standard cells and delay cells under all the combinations of variations.
2. Calculate scaling ratio $R = \frac{D_{act}}{D_{est}}$ for each cell. (delay_cell) (standard_cell)
3. Create some database files for static timing analysis tool.
5. Evaluate maximum delay values of the synthesized combinational circuit under all the combinations of variations.
6. Calculate scaling ratio $R_{cc} = \frac{D_{act_{cc}}}{D_{est_{cc}}}$ (s208)
7. Calculate scaling variation $V = \frac{R_{cc}}{R_{st}}$ in each condition for all the delay cells.
   * The maximum value of $V$ represents the variation factor $K$ for each delay cell.
8. Select the most appropriate delay cell which $K$ value is the minimum number.
Handshake protocols

2phase handshake

Both rising edges and falling edges must be larger than the delay of combinational circuit

⇒ BUF-type delay cell

4phase handshake

Only rising edges must be larger than the delay of combinational circuit

⇒ AND-type delay cell
Delay cells with a wide variety of delay variations (2)

In 4-phase handshake protocol which has the working phase and the idle phase, only rise delay must be larger than the delay of combinational circuits: **AND-type delay cells**

(a) Standard structure

(b) NMOS-chained structure

(c) PMOS-chained structure
Definition of the SDI model

- **Scaling ratio**: \( R = \frac{D_{\text{actual}}}{D_{\text{estimate}}} \)
  - Ratio of actual delay to estimated delay for each component.
  - Scaling ratio is unbounded.

- **Scaling variation**: \( V = \frac{R_1}{R_2} \)
  - Ratio of the scaling ratio of a component C1 to that of another component C2.
  - Scaling variation between any two components is bounded.

- **Variation factor** \( K (K \geq 1) \): \( \frac{1}{K} \leq V \leq K \)
  - A constant value that represents the degree of scaling variation.