DESIGN-FOR-TEST OF MIXED-SIGNAL INTEGRATED CIRCUITS

Adoración Rueda, José L. Huertas

Instituto de Microelectrónica de Sevilla (IMSE-CNMC-CSIC)
University of Seville
rueda@imse.cnm.es, huertas@imse.cnm.es

Outline

Introduction:
- Main test concepts
- Technology Trends
- Design-for-test: a must for present electronic systems?

Functional Test for Mixed-signal ICs:
- Circuit classes and metrics
- Test-on-Chip: signal generation & response acquisition
- Test & BIST approaches

Structural Test for Mixed-signal ICs

Main steps in ICs realization

What does Test mean?

Testing (in general) is the process of verifying that an IC meets the specs for what it was designed.

Testing (alternative) is the process of verifying that the intended behavior of an IC is not affected by a defect.

General causes for IC fail:
- Design Mistakes
  - Human Errors
  - Modelling Oversimplifications
  - Design Rules Violations
- Fabrication Flaws
  - Process fluctuations, mask misalignment
  - Spot defects
  - Handling & Finishing problems
- Operation Damages
  - Aging
  - Mechanical Breaks
  - Thermal Stress
  - Electrical Influences
  - Environmental Changes

Perfect design + Perfect fabrication process yes

but

IC’s are more and more complex (perfect designs not assured)
- process defects exist with different impact on different circuit types

test required

IC test quality?
Depending on the product lifetime testing procedures are different, and have different goals and costs.

**Test Types**

- **Validation:**
  - Specification & Design
  - Design Validation
  - Functional & Design

- **Characterization:**
  - Prototype Characterization
  - Production Test
  - Field Test

- **In-field:**
  - Monitoring & on-line test
  - Diagnosis

**Test Importance (in general):**

- ICs are more and more complex (design not fully simulated)
- Time-to-Market is conditioned by Test Speed/Quality
- Test Cost (test time) is dominating in many Products
- Present Quality Figures decreased (500 ppm --> 1 ppm)

**Factors affecting IC Quality:**

- Improving quality could mean more improvement of test coverage than in manufacturing yield
- The quality level can vary greatly depending on the type of failures occurring and the type of failures targeted by the test approach

**Some models for Quality Level:**

\[ Q_L = (1 - T) \]

\[ Y = 1 - (1 - T(1 - Y_F - (4 - 1)T)^n) \]

**Test Coverage:**

\[ T = \frac{\text{number of faulty parts tested}}{\text{number of faulty parts total}} \]

**Manufacturing Yield:**

\[ Y = \frac{\text{number of defect-free parts tested}}{\text{number of parts total}} \]

**Factors affecting IC Quality:**

- Manufacturing Environment
- Technology Parameters
- IC Product Quality
- Test Evaluation Method
- Test Approach
- DFT Features

**More on Yield & Product Quality**

- **Process Yield:**
  - \( \gamma_P = \frac{\text{number of good fabricated circuits}}{\text{total fabricated circuits}} \)

- **Test Yield:**
  - \( \gamma_T = \frac{\text{number of correctly tested circuits}}{\text{total tested circuits}} \)

- \( Q_L \): Test Coverage
- \( Y \): Manufacturing Yield
- \( n \): average of faults per faulty part
Two Test Approaches

Functional Test
- Specification-based Test
  - The Fabricated Chip Completes Specs
- Testing Environment
  - Response Interpreter
- Defect-oriented Test
  - There is No Defect Provoking an Error

Structural Test
- Structural Knowledge
  - Stimuli Generator
  - Cut
  - Structural Knowledge
- Response Interpreter
  - Defect Effects
- Test experiment
  - I/O Behavior
  - All I/O relationships of interest must be checked out
  - It takes long time
  - It requires quite different instruments

Typical Analog Test
- Validation Test
- Prototype Test
- Production Test
- Typical Digital Test

Yield & PQ for Structural Tests

Process Yield:
- Referred to the Number of Good Fabricated Circuits
  \[ Y_F = \frac{\text{Fabricated - Good Fabricated}}{\text{Fabricated}} \]

Test Yield:
- Referred to the Number of Correctly Tested Circuits
  \[ Y_T = \frac{\text{Tested Correct}}{\text{Tested}} \]

Factors affecting IC Quality:
- Some models for Quality Level:
  \[ QL = 1 - \left( 1 - Y_F \right)^{1 - T} \]

Factors affecting IC Quality:
- The quality level can vary greatly depending on the type of failures occurring and the type of failures targeted by the test approach

Factors affecting IC Quality:
- Relation between faults modeled and yield is needed

Factors affecting IC Quality:
- Improving quality could mean more improvements in test coverage than in manufacturing yield

Factors affecting IC Quality:
- Manufacturing Yield = defect-free parts tested/parts tested
  \[ Y_T = \frac{\text{Tested Correct}}{\text{Tested}} \]

Factors affecting IC Quality:
- n: average of faults per faulty part

Factors affecting IC Quality:
- \( T \): Test Coverage = modeled faults detected/modeled faults

Factors affecting IC Quality:
- \( Y \): Manufacturing Yield = defect-free parts tested/parts tested

Factors affecting IC Quality:
- in average of faults per faulty part

Outline

Technology Trends

Semiconductor industry is changing: fabless companies growth
- Many agents to have care of IC yield, quality and reliability (IP providers, designers, fabs)

System-on-chip (SoC) designs are increasing
- Emerging failure mechanisms
- Different cores with different modelling, different test requirements and different tester languages
- More to test, less test access (less pin/device): yield losses

New Failure and Yield analysis challenges
- Increasing metals and circuit complexity lead to reduction of the traceability of signals: more complex monitor structures
- Increasing wafer size and process variations across wafer

Technology Scaling and the Cost of Test
- Manufacturing cost reduces for each technology generation but test cost remains almost constant: test cost will dominate product cost
- Tester speeds not growing as chip speeds
**Design-for-Test: a solution?**

*Design-for-Test (DfT): any method of improving the testability of a circuit by design*

**Why to enhance Testability?**
- Decreasing Test Time/Cost
- At-Speed Testing
- Alleviating Tester Limitations
- Reducing External Interfaces
- Providing Periodic Re-Testing
- Helping Maintenance
- Increasing Long-term Quality

**How to enhance Testability?**
- Reducing Defect Probability
- Optimizing/simplifying the Test Process
- Re-designing the Circuit (or some parts) to support easier measurements
- Providing/Embedding Test Functions into Chips (BIST)
- Using Circuit Properties to Decrease Test Cost
- Re-configuring the Chip to Speed-up the Test or to test other parts

---

**Mixed-signal DfT Challenges**

Most difficulties for Mixed-signal DfT due to:
- accuracy requirements for measuring analog signals
- lack of “accepted” analog fault models
- access issues for embedded components
- most class of circuits need specific testing methods
- current mixed-signal test requirements exceed available tools and ATEs
- lack of a structured test methodology
- advanced processes not stable: no good process characterization data

**DfT practical trade-offs:**
- fault coverage
- performance impact
- extra area
- design impact
- yield loss
- availability of tools
- test time

Como introducir BIST?
What to test? What to need?

**Functional test**: Parameters related to specs
- standard metrics / standard measurements
- stimulus generation issues
- acquisition issues
- accessibility issues

**Structural test**: Fault coverage and predict future yield problems
- defect-to-fault mapping
- fault models & fault simulations
- stimulus generation issues
- acquisition and response analysis issues
- accessibility issues

Some of these issues: **metrics**

- Static set of metrics
  - Gain error
  - Offset error
  - INL
  - DNL
  - Missing code

- Dynamic set of metrics
  - SFDR
  - SNR
  - THD

- Also: IM distortion, bandwidth, NPR, differential gain and phase, aperture effects, ...

Some of these issues: **methods**

- Code transition location
  - servo-loop
  - ramp histogram
  - sinewave histogram
- Sine-wave fit
  - tree parameters
  - four parameters
- Discrete Fourier transform

- huge number of samples, large records
- high-resolution input signal
- expensive test hardware

How Converter testing has evolved

- Better understanding of error sources
- New standard for parameter definitions and test methods
- Linking testing needs to applications
- Developing test schemes to manage different problems
Some Test Schemes

- HBIST (functional)
- MADBIST (functional)
- OBISt/BISTmax (functional & structural)
- Ad-hoc BIST schemes (func. & struc.)

Some emerging solutions-1

To relax source linearity requirement
- Exponential waveform test signal
  - Proposed as a characterization test: fitting algorithm determines R, C and Vref
  - Histogram
  - Finite resolution ramps + new computational algorithm
  - Ramp equivalent signal: digitally controlled on-chip, use external RC filter

Some emerging solutions-2

To reduce time
- Model-based test
  - Develop linear models with a reduced variable set
  - Measure the parameters of interest only at some points and solve for the reduced variable set (the number of points give the confidence interval)
  - Extrapolate the non-measured (up to $2^n$ values according the model)
  - Check if the specifications are respected
- Short-codes + model-based test

Present situation

- Conventional test approaches inefficient to cope with current test requirements of ADCs (embedded in complex systems or alone)
- Yield loss getting worse as ICs performance reaches ATE performance

Solutions?
- Accurate simplified test
- Parallel test
- Distributed test resources
- Defect-oriented test
Some emerging solutions-3

Precise on-chip generation of sine-waves is challenging:
- Use a DAC, in particular a $\Sigma\Delta$ DAC
- Use a recirculating bitstream of $\Sigma\Delta$ encoded sine-wave + a simple filter
- Use directly the scaled digital bitstream to test $\Sigma\Delta$ modulators

The scaling brings the stimulus noise below the modulator noise.

Some emerging solutions-4

For high-resolution $\Sigma\Delta$ converters
- Use a DAC, in particular a $\Sigma\Delta$ DAC
- Use a recirculating bitstream of $\Sigma\Delta$ encoded sine-wave + a simple filter
- Use directly the scaled digital bitstream to test $\Sigma\Delta$ modulators

Design-spec based BIST

For integrator leakage in SD modulators
- Use a DAC replica
- Use a modified switching scheme

Conclusions

Needs more research for:
- accurate simplified test
- parallel test
- distributed test resources
- better structural test

IMSTW contributions to Converter Testing in 10 years:
- 1995 → 3/45 ADC&DAC papers
- 2003 → 12/46 ADC&DAC papers
Structural Test for Mixed-signal ICs

Functional test has been the unique “widely accepted” approach for mixed-signal ICs (embedded in complex systems or alone), but:

- Yield loss getting worse as ICs performance reaches ATE performance
- Functional test in SoCs is much more costly than for stand-alone parts
- Structural test may become the only viable method for current mixed-signal test requirements, because of:
  - low-cost tester requirements
  - more compatible with IEEE 1149.4 test bus standard
  - easier for BIST implementation
- Structural test may be desirable for in-field test and diagnosis of Microsystems

Industry is now pushing innovations and improvements in mixed-signal structural test

Conventional Structural Test
Fault-based Test Flow: No Specs are, in general, measured

CUT and Test Strategy
- Optimize CUT for Test
- Redesign Test Stimuli
- Modify Test Approach

Fault List
- Simulation Evaluation
- Fault Coverage ok?
- Test Requirements ok?
- Test Cost ok?

As good as fault models and fault simulations are
May be very costly in simulation time

An example
The CUT: A second order SC Bandpass filter ($f_0 = 56.915\text{kHz}, Q=19.233$)
Test strategy: deviations of differential output from the fault-free circuit

Fault coverage for different test signals:
Selection of test stimuli
I\textsubscript{DDQ} Technique

- I\textsubscript{DDQ} Testing is a well structured DfT methodology which is widely used by Semiconductor Industries (mainly for digital circuits).
- I\textsubscript{DDQ} technique is based on the fact that defective circuits produce an abnormally high value of the quiescent power supply current.

Up to now applied to simple analog blocks or as complement of other techniques.

Basic areas to research:
- Instrumentation for I\textsubscript{DDQ} measurement
- Built-in current sensor (BICS)
- Fault models and metrics
- CAD tools
- Transient I\textsubscript{DDQ}
- Signature-based techniques instead of pass/fail threshold
- Power supply partitioning at chip level

Oscillation-based Test (OBT)

Additional feedback added to the system or to some blocks to produce oscillations. Faults are detected from:
- no oscillation, or,
- deviation of the oscillating signal parameters.

Test Information:
- Frequency
- Amplitude
- Input Buffer
- Comparator
- Vector-less method
- Conceptually simple
- No important modifications of the SUT
- Easy to extend to BIST

\textbf{BISTmaxx\textsuperscript{TM}}

- Commercialised (Opmaxx) BIST structure for analog and mixed-signal ICs
- Convert block (filter, opamp, PLL, ADC, DAC, VCO, regulators) into circuit that oscillates at a predetermined frequency
- Frequency is treated as digital signature and is related to functional & structural parameters

OBT in Filters: an example (1)

Analytical relationships for oscillation:
- Oscillation conditions: $\sin(\omega_2 t - \theta_2) = \sin(\omega_1 t - \theta_1)$
- Amplitude of oscillations: $A = \frac{\omega_2 - \omega_1}{\omega_2 + \omega_1}$
- Frequency of oscillation: $f_{osc} = \frac{1}{2\pi} \frac{1}{C_j+1}$

\[ \Phi A = \Phi B \]

\[ |A|H(z) = 1 \]
**OBT in Filters: an example (2)**

**Validation Results:**

<table>
<thead>
<tr>
<th>Type</th>
<th>Notch 1</th>
<th>Notch 2</th>
<th>Notch 3</th>
<th>Notch 4</th>
<th>Notch 5</th>
<th>Notch 6</th>
<th>BP 1</th>
<th>HP 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>fosc</td>
<td>835.0</td>
<td>791.4</td>
<td>603.9</td>
<td>968.6</td>
<td>1182.2</td>
<td>608.3</td>
<td>608.3</td>
<td>1696.9</td>
</tr>
<tr>
<td>A0</td>
<td>830.7</td>
<td>717.1</td>
<td>592.9</td>
<td>967.7</td>
<td>1177.5</td>
<td>601.9</td>
<td>601.9</td>
<td>1694.9</td>
</tr>
</tbody>
</table>

Monte Carlo Analysis to define the minimum deviation that can be considered as faulty behavior.

**OBT in Filters: an example (3)**

Application: Two biquads tested simultaneously

Making use of Sw-opamps

**OBT in Filters: an example (4)**

Design with no OBIST

Design with OBIST & other test facilities

7% area overhead

**OBT in Δ-Σ Converters (1)**

Disconnect the input and modify the structure to build a robust oscillator.
**OBT in Σ-Δ Converters (2)**

Simulation results $A_{OS}$ and $f_{OS}$ as a function of $E_{test}$ and $C_{test}$

**Extension to BIST**

**Reconfiguration-based BIST (1)**

For Σ-Δ modulators [Mir, 97]

**Reconfiguration-based BIST (2)**

For Pipeline ADCs [Peralías, 00]
Emerging solutions for ADC testing

Conventional Test Methods
Aimed to obtain performance parameters

- Code transition location
  - servo-loop
  - ramp histogram
  - sinewave histogram

- Sine-wave fit
  - three parameters
  - four parameters

- Discrete Fourier transform

- huge number of samples, large records
- high-resolution input signal
- diverse and expensive test hardware
- hard for BIST in embedded cores

IEEE Std 1241-2000

How Converter testing has evolved

- Better understanding of error sources
- New standard for parameter definitions and test methods
- Linking testing needs to applications
- Developing test schemes to manage different problems

Some emerging solutions

- Functional test
  - easy interpretation
  - precision limited: acquisition and generation
  - very costly for high resolution ADCs

- Structural test
  - fast and low-cost
  - confidence limited

- Relaxing source linearity requirements:
  - Finite resolution stimulus
  - Other input signals: exponential, noise
  - Alternate test

- Reducing test time:
  - Model-based methods
  - Behavioral model-based Structural Test
  - More efficient BIST solutions
Relaxing input test signals (1)

Finite resolution stimulus + new computational algorithm [Jin, 03 - Yu, 04]

1) Histogram based approach
   Input: two “ramp-like” nonlinear signals
   Histogram-based algorithm
   Static performance: DNL, INL
   Objective: separate the nonlinearity of the ADC from that in the input
   Reported result: 8-bit linear inputs able to test a 16-bit ADC

2) Spectrally Related Excitation (SRE) approach
   Input: two imprecise sinewaves
   FFT-based algorithm
   Spectral performance: THD, SFDR
   Idea: use of the spectral relationship between inputs to separate the distortion of the ADC
   Reported result: 60dB sinewaves able to test 100dB SFDR ADC
   Functional type: Reduce tester cost but not test time
   Only good for partial BIST: generation part

Relaxing input test signals (2)

Exponential waveform test signal [Chen, 02 - Holcer, 03]

based on capacitor discharge --> well-known shape
depend on R and C and Vref
easily implemented
Proposed as a characterization test:
fitting algorithm determines R, C and Vref
Static performance: DNL, INL
Spectral performance: THD, SFDR
Ramp equivalent signal:
4 exponential steps: use of digital PWM
digitally controlled on-chip
use external RC filter
use polynomial fitting algorithm [Sunter97]

Staircase-like exponential waveform test signal [Roy, 02]

Purely digital spec BIST
Almost good test
Test 4 specs (no THD)
At-speed test

Relaxing input test signals (3)

Noise input signal [Flores, 05]

based on multiple tone signal and spectral analysis
valid for static and dynamic functional parameters
needs less output samples than histogram-based

Specific input signal [Ong, 02]

for testing SD modulators
input is a scaled bitstream of the modulator
extract only integrator leakage errors
Also developed with pseudorandom input

Relaxing input test signals (4)

Alternate Test [Variyam, 98-02] [Bhattacharya, 05]

targeted to reduce tester resources requirements
based on developing non-linear regression models
uses the models to find the stimulus and to predict specs from responses
valid for functional or structural techniques
recently applied to high-resolution high-speed ADCs and to RF

Test Flow example
Measure specs from N devices using conventional test
Measure response data from the same devices using proposed stimulus
Build Model function f: M-S using MARS
Test the rest of devices with the stimulus and estimate its specs using the model
Reducing Test Time

- Model-based Test
  - develop linear models with a reduced variable set
  - measure the parameters of interest only at some points and solve for the reduced variable set. (the number of points give the confidence interval)
  - extrapolate the non-measured values according to the model
  - check if the specifications are respected

Behavioral model-based Test

- Do not relax the tester req. but the number of specs to measure
- A good methodology exists

Behavioral model-based Test

Application to \( \Sigma \Delta \) Converters

Block defect effects

- Amplifier DC gain
- Non-linear settling
- Integrator leakage
- Harmonic distortion

Not equally significant for all the amplifier

- Demanding design: small capacitors, high input DC gain, fast settling
- Relaxed design: small capacitors, high input DC gain, slow settling

A Digital BIST for \( \Sigma \Delta \) modulators (1)

- Fully digital BIST based on the behavioral test idea
- The test stimulus: Digital sequences
- The signature analyser: Simple up/down counters
- Targeted to test: Integrator leakages, Amplifier settling errors, Non-linear amplifier gains
A Digital BIST for $\Sigma\Delta$ modulators (2)

Application to a 2-1 cascade modulator

![Diagram showing modifications at switches level](image)

Some signatures

DC gain 1st integrator:

$$\sum (\frac{p}{q} x_{n-1} - \frac{1}{2} X) = 2\Delta (A_{n-1} - b)$$

$N$: number of acquired samples

$Q$: input seq mean value

$p_i$: integrator pole error (leakage)

DC gain 2nd and 3rd integrators

$$\sum (\frac{p}{q} x_{n-1} - \frac{1}{2} X) = 2\Delta (A_{n-1} - b)$$

$L$: input seq period

Amplifier settling error

$$\sum (\frac{p}{q} x_{n-1} - \frac{1}{2} X) = 2\Delta (A_{n-1} - b)$$

A Digital BIST for $\Sigma\Delta$ modulators (3)

Tests set validation

High-level simulation results

- Functional PASS/FAIL limits
- SNRD in dB
- DC gain

A Digital BIST for $\Sigma\Delta$ modulators (4)

Experimental results

Test results analysis

- Functional PASS/FAIL limits
- SNRD in dB
- DC gain

References


[IEEE Standard for a Mixed Signal Test Bus], IEEE Standard 1149.4-1999

Books: